Damage Analysis of Reactive Ion and Atomic Layer Etched Silicon

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List of abbreviations

AFM Atomic Force Microscope

ALD Atomic Layer Deposition

ALE Atomic Layer Etching

Al Aluminum

AM Amplitude Modulation

Ar Argon gas

CHF_3 Trifluoro methane

Cl_2 Molecular Chlorine

Cl Atomic Chlorine

$Cl^{\bullet}$ Radical Chlorine

CPD Contact Potential Difference

DC Direct Current

EPC Etch Per Cycle

E_V Vacuum Energy Level

E_{FS} Sample Fermi Energy Level

E_{FT} Tip material Fermi Energy Level

eV Electron Volt

FM Frequency Modulation

GaAs Gallium Arsenide

HF Hydrofluoric

IC Integrated Circuit

ICP Inductively Coupled Plasma

IED Ion Energy Distribution

IPA ISO propanol

KPFM Kelvin Probe Force Microscopy

MFC Mass Flow Controller

ML Monolayer

N_2 Nitrogen Gas

nm Nanometre

RIE Reactive Ion Etching

RF Radio Frequency

rms Root mean square

SEM Scanning Electron Microscope

Si Silicon

Si-Si Silicon Bonds

SiO_2 Silicon dioxide

SCCM Standard cubic centimetres per minute

TEM Transmission Electron Microscope

UV Ultraviolet

XPS X-ray Photoelectron Spectroscopy

Φ Work Function

Abstract

Dry etching is one of the most important methods of pattern transfer in nanofabrication. There are many dry etching methods, the most commonly used is reactive ion etching (RIE), that is based on a continuous supply of reactive ions and radicals generated in a radio-frequency (RF) plasma discharge. The RIE approach can be very accurate and may provide high resolution etching, below 10 nm in lateral direction. However, as the patterning resolution in lateral and vertical directions increases, the continuous etching approach may not satisfy the new requirements for dry etching.

Atomic Layer Etching (ALE) is one of the most advanced etching techniques due to its layer-by-layer control over the etched materials. The etching in ALE regime can be characterised as a self-limiting. ALE process based on four steps where the surface modification is separated from the etching process. Those ALE steps form the etch process cycles, which are repeated to remove the necessary amount of material.

Dry etching techniques, including RIE and ALE, use energetic ions to remove the etched atoms from the surface. Typically, their energy greatly exceeds binding energy of atoms in crystalline lattice (few eVs) that may result in implantation of impinging ions and/or displacement of the substrate atoms that results in radiation damage. The ion energy in RIE can be in the 100-300 eV range, while ALE requires much lower energy of 20-50 eV. Therefore, one can expect that ALE is a low damage etching technique.

In the current MSc-thesis a comparative study of the radiation damage in Si (100) etched using a conventional RIE with Cl_2/Ar^+ process and a newly developed ALE with the same etch chemistry. Then the surface damage analysed by measuring the contact potential difference (CPD) by Kelvin Force Probe Microscopy (KFPM). The results of these experiments indicate that the damage caused by RIE process was high as the values of CPD and the work function of the etched surface was much lower than the values of ALE samples. While ALE process showed almost minimum damage formation on the etched Si sample according to the CPD values that were close to pristine Si (100). Finally, this project opens the door for further studies of ALE damage in different conditions than it used in this study because of its importance for nanofabrication and semiconductor industry.

1. Introduction.

From long time ago, drawing by etching used to convey a message or commemorating historical moments lived by humans for centuries. However, with the progress of time, etch started to take other dimensions in human life. For example, when people moved to live in houses and palaces, etch started to be used as a means of decorating walls or facades of palaces and temples, and even in decorating tools used in daily life.

In general, etching process is described as removing the layers from the original material in order to transfer a specific geometric pattern onto the base material. Since 1970, the revolution in electronics manufacturing has begun, and the semiconductor industry has emerged as an important and essential factor in building electronic devices. The central processing unit is an example that has witnessed a great development due to the progress made in the transistor industry.

In transistor manufacturing, there is a so-called Moore's law, see Figure 1, which is an observation of doubling the number of transistors in integrated circuits (IC) every two years [22]. Therefore, we started using electronic devices which have the size of a palm or smaller, and their capabilities exceed the capabilities available in the first generation of computers, which were much larger in size than they are today. Recently, Moore’s law has reached its limit because the progress in increasing the number of transistors has slowed down due to the available technology that could not be able to manufacture transistors in a smaller size than we have today. Therefore, there was a need to search for new materials or new technologies to reach sub-10 nm or even atomic scale.

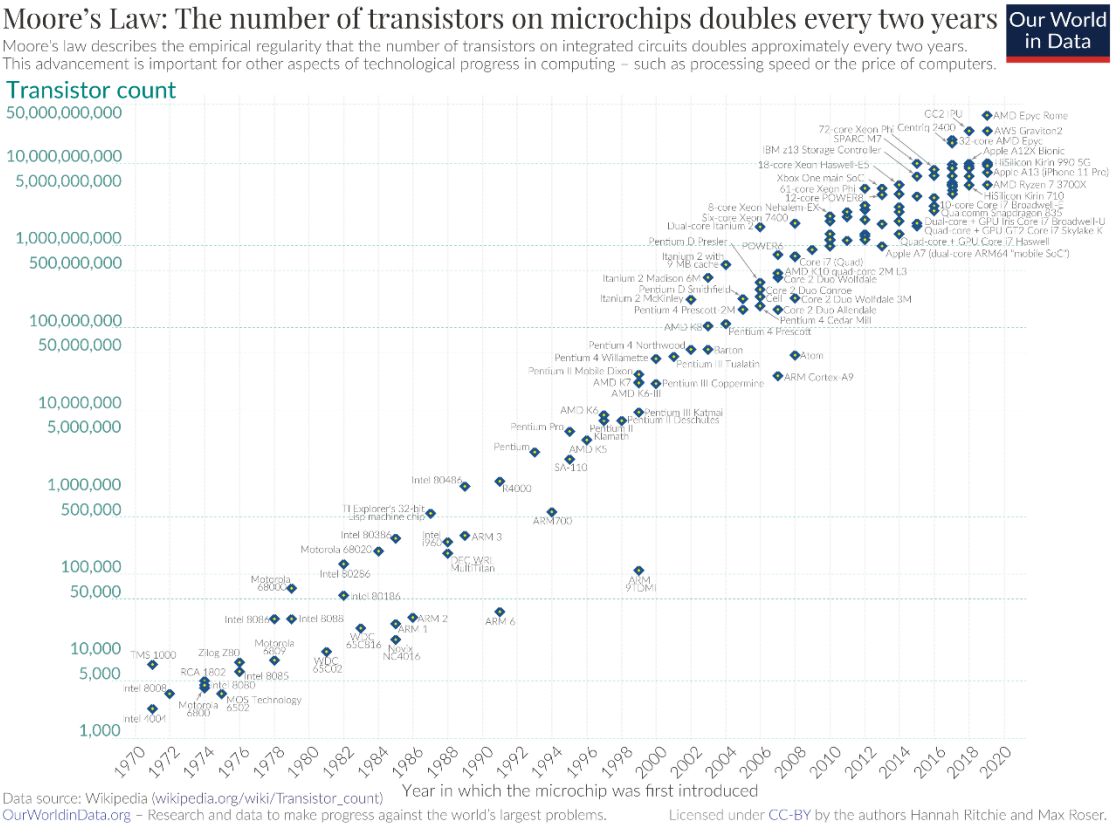


Figure 1. transistor counts for microprocessors against dates of introduction.[34]

Manufacturing of nano-scale devices such as transistors includes several steps based on three main processes: lithography, etching and deposition. Repeating these processes will lead us to the final product. However, the fact that nano-scale devices have larger surface comparing to the bulk material makes the control of manufacturing procedures more important due to the possibility to introduce defects which can negatively affect the optical and electrical properties of the devices.

In this project we are interested in etching process because of its impact on the surface of materials by causing a potential damage. Such damage may lead to a deterioration of optical and electronic properties of micro- and/or nano-devices. Initially, wet chemical etching, based on chemical reactions in a liquid phase, was used in the microelectronics industry. However, wet etching has many drawbacks, including isotropic etching (etching in all direction), insufficient selectivity, potential health safety issues and environmental concerns [1]. For state-of-the-art semiconductor IC processing, such as dynamic random-access memory or microprocessor units with feature size down to nanoscale, the applicability of wet etching is limited.

As a result of the development of electronics industry and reduction of feature sizes of ICs, the need for anisotropic etching (preferential etching in one direction) became a major requirement for further advances in microelectronics. Reactive ion etching (RIE), also called “dry etching” that allowed a highly anisotropic pattern transfer, soon replaced the wet etching due to much better process control.

Nowadays when the sizes of devices are well below tens of nanometres, the requirements to etch very thin layers of material can no longer be fulfilled by a conventional RIE. Being a continuous etching technique, the RIE can not provide a monolayer (ML) control, so other more advanced methods of material removal are urgently needed. One option to provide a ML etching control would be to use self-limiting cyclic processes, similar to the ones in atomic layer deposition (ALD), but in reverse.

Such a process is called atomic layer etching (ALE) which is a cyclic alternative process to RIE. The ALE technique is capable of removing one ML at a time. Also, controlling etching depth makes it ideal for etching atomic scaled features with high precision. Moreover, ALE has an advantage due to smoothing of the etched surface which increases the possibility of achieving high-resolution patterning. At the same time, the ALE is also based on the use of energetic ions, similar to RIE, though with much lower energy. It means that both techniques may be responsible for various types of damage during the etching process.

Moreover, a theoretical study such as Hybrid Plasma Equipment Model HPEM and molecular dynamics MD studies have played a crucial role in advancing our understanding of the ALE process, enabling the development of more precise, selective, and efficient techniques for nanoscale material removal. By providing insights into surface reactions, reaction pathways, surface species, and material-specific behaviour, MD simulations have significantly contributed to the improvement of ALE processes in terms of control, selectivity, and atomic-level precision [20][12].

The surface damage of the sample can be introduced due to several reasons, including the ion bombardment during the etching process and ultraviolet (UV) radiation. Such process parameters, like etching time, the gas mixture, sample temperature, and others will affect the degree of damage. In general, the surface damage can be structural, electrical, or chemical.

The aim of this master thesis is to compare the damage formation between ALE and RIE as etching process where the Si surface will be etched by using chlorine gas Cl_2 and argon ions Ar^+. The damage then will be analysed by Kelvin probe method by measuring the contact potential deference (CPD) for etched and reference surface.

Chapter 2

2. Theoretical Background

2.1 Reactive ion etching

Reactive Ion Etching (RIE) belongs to a dry etching method where the chemical reactions are taking place in the gas phase, unlike the wet etching. In order to create reactive species in the gas phase, the reactive gas molecules must be excited or ionised in a low-temperature plasma. Such plasma can be created at low gas pressures using a DC- or radio-frequency (RF) excitation power. After application of a curtain electrical field strength, one forms many electrons and ions due to gas ionisation process. The plasma is quasi-neutral, i.e., does not contain an excess electric charge, but the ions and electrons can be used for generation of active radicals and other species. Those radicals and ions can easily react with surface of the etched material, e.g., Si to form volatile compounds that are removed via pumping.

$$Si + Cl^{\bullet} \text{---} > SiClx$$

The RIE is using plasma to create active species for gas phase etching and due its advantages it is widely used in the semiconductor electronic industry for integrated circuits (IC) manufacturing. One of the advantages of RIE, is its high etch directionality (etch anisotropy) due to acceleration of ions towards the sample. This is a result of the difference in mobility between ions and electrons, the electrons will be accelerated by the electric field and form a negative DC bias on the sample holder. Therefore, this bias voltage extracts the ions from the bulk plasma and accelerates them with a specific energy toward the target surface.

The performance of RIE depends on a number of parameters, such as RF-power, gas pressure, temperature etc. The RF-power, for example, determines the plasma density, i.e., concentration of ions and thus the etch rate. In simple RIE tools, like parallel-plate etchers, the RF-power will also determine the DC-bias on the sample's holder. However, other designs provide independent control of DC-bias and plasma density that gives more flexibility.

The plasma generated inside the tool chamber contains a mixture of reactive and nonreactive ions in addition to electrons, reactive neutrals, passivating species, and photons. The RF power applied to the cathode is responsible for generating the reactive species in the plasma such as excited molecules and radicals as well as controlling the density of the charged species. As a result, the DC bias and ion density bombarding the substrate are correlated and controlled by the same RF power source.

The desirable feature of the RIE process is its directionality which results in anisotropic etching. The directional etching (anisotropic) means that the etching in one direction is dominated over other directions which produce sharp, well-controlled features. However, three parameters can determine the degree of directionality in the RIE process which are the lower pressure and higher substrate bias that control the energy of the ions (increase) and energy distribution (reduce) [3]. There are two main designs of the plasma etch equipment which can provide appropriate parameters for etching process.

The first one is called capacitively coupled plasma (a parallel plate reactor) which is a common and simple form of etch tool used in dry etching. Figure. 2 (left) shows a schematic of this RIE plasma chamber. In general, a typical RIE tool consists of a vacuum chamber containing two electrodes which form a parallel plate configuration. A RF-power is applied between the electrodes to ignite plasma, typically this happens at a low gas pressure of dozens or hundreds mTorr. Due to higher mobility of electrons in plasma, the powered lower electrode where a sample is placed, is charged negatively creating a DC-bias voltage. This bias voltage attracts positively charged ions to provide the desired etch anisotropy. The gases used in the etch process can be supplied via a ring shower above the sample holder.

One of the major drawbacks of this configuration is relatively high bias voltages (several hundred volts) and limited possibility to control the bias independently from other etch parameters. Also, this design does not provide high plasma density at low pressures (below few mTorr). So other RIE configurations with two separate RF-generators are more commons.

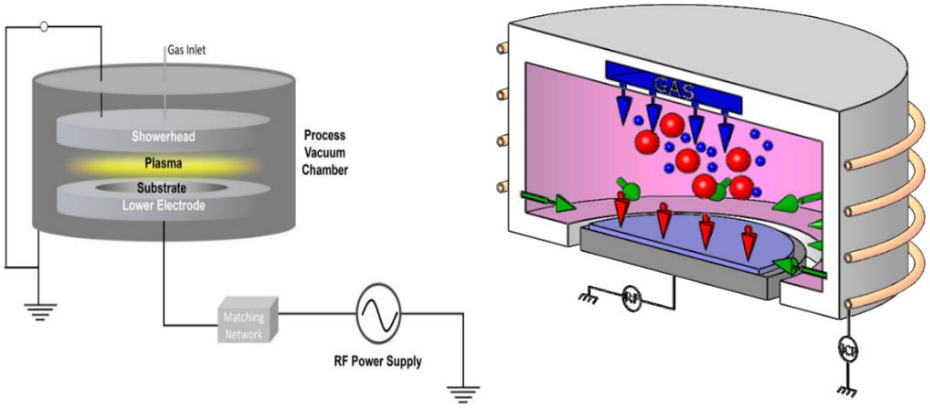


Figure 2. Capacitively coupled plasma (left) and inductive coupled plasma (ICP) (right).[4]

One of such configurations is inductively coupled plasma reactive ion etching (ICP-RIE) system, Figure 2 (right). The ICP-RIE design uses separate RF generators for plasma ignition and for DC-bias, in this case the plasma is created by inductive coils arranged around the top part of the chamber, while another generator provides energy for the bias at the sample holder. In this way, the RF-power used for the ignition of the plasma is independent of the power used for DC-bias to attract the ions toward the substrate. The ICP configuration allows also very high plasma density compared to the parallel plate design, resulting in high etch rates. Finally, the ICP plasma can be sustained at much lower pressure that makes it easy to obtain high etch anisotropy. The ICP-RIE tools are more complicated than the parallel plate etcher, but they provide high degree of flexibility and wider etch parameter space.

Both type of etch tools can be used for etching a variety of material, such as dielectrics (SiO_2, Si_3N_4), metals (W, Al), semiconductors (Si, III-Vs) and polymers (resists). Each type of material requires a dedicated plasma chemistry, for example, Si can be etched using chlorine (Cl_2) or F-containing compounds (CHF_3, CF_4). In the current project we used a mixture of Cl_2 and Ar to etch silicon using both RIE and ALE techniques.

2.2 Atomic layer etching.

As the size of features is shrinking in modern electronic devices further and further, the need for new technologies with atomic-level precision has become an urgent matter. High resolution and sharp patterns are essential for the fabrication of today's advanced nano-electronic devices. However, RIE technology couldn't keep up with the progress made in the electronics industry and the etching technology with atomic-scale fidelity became in high demand.

Atomic layer etching (ALE) technology was the solution for these challenges being an etching technique that provides an excellent etching depth control that achieves the accuracy required for producing electronic devices in sub-10 nm nodes. The principle of ALE goes back to 1989 when the first paper was published by Yoder when used ALE for crystalline diamonds and because of the similarity between atomic layer deposition (ALD) and ALE, it suggests that the ALE started in the 1980s [6].

Historically ALE is mentioned in scientific articles with different names such as plasma atomic layer etching (PALE) and layer-by-layer etching. However, the first published articles were focusing on ALE as new technology that could achieve isotropic etching which was the most interesting thing at that time and was challenging for conventional RIE technology.

First, Si and GaAs were the most studied material by ALE and especially GaAs because of their III-V direct band gap, high carrier mobility and its application in opto-electronics and high-frequency devices. [7]. In the last decade, ALE was presented at every conference on atomic layer deposition ALD and a high number of scientific articles was published due to better understanding how ALE can be used as etching process with atomic layer precision. Quasi-ALE also has been presented as a hybrid process where the etching is mixed between ALE and RIE. During the last 30 years, more than 20 materials have been studied by ALE such as Si, III-V materials, oxides, and metals. The major difference between RIE and ALE is that ALE is a non-continuous process but rather divided into cycles with four steps in each cycle. Modification, purge, etch and purge steps in sequence build one cycle which is repeated many times in order to remove a thin film from the original surface.

For activation step, it was a wide range of chemistry has been used in order to alter the binding energy of the surface atom of the etched material. Such chemistry used are halogens such as Cl (a common process gas has been used for ALE), F (fluorocarbon as source of fluorine and carbon for SiO_2 etching) and Br (has occasionally been studied).

Figure 3 shows a schematic diagram of the most common ALE process where Si is the etched material and molecular chlorine is the process gas. First, the sample surface needs to be chemically activated with chlorine (Cl_2) after that any extra amount of Cl_2 inside the chamber will pump out in the first purging step. This modification may include the formation of a monolayer of Cl_2 on top of the Si surface by the adsorption and reaction of chlorine with silicon. After purging, argon ions (Ar^+) produced by plasma react with the modified surface in order to etch a certain thickness of the material. Finally, another purging step follows to pump out the reaction products which is $SiCl_x$ in our case.

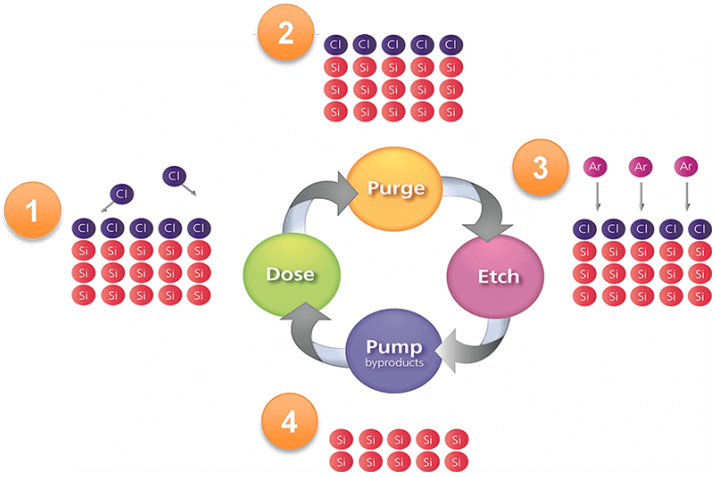


Figure 3. Typical ALE four steps configuration.[9]

The reason behind separation in the ALE process is that it allows the decoupling of generation and transport of reactive species thus making it possible to control what species are needed. The separate process steps in ALE make it easier to identify those steps that are responsible for each damage generation as compared to the continuous RIE. The next part will review how the ALE process works and explain the purpose of having cycles of different steps.

2.2.1 Activation step (Step 1)

This activation step can also be alternatively called a modification or dosing step. During the activation step, the surface of the etched material (e.g. Si) is covered by a monolayer of a reactive gas, for example, chlorine. The chlorine atoms bind chemically with the Si atoms to form volatile chlorides that are subsequently removed easily from the surface.
The activation step is realized by exposure of the etched material to either molecular chlorine Cl_2 or to plasma-generated atomic chlorine Cl. A plasma discharge can be used for the dissociation of the Cl_2 molecules by electron impact. Adsorption of molecular chlorine is relatively slow, but the atomic chlorine reacts with Si much faster due to its high reactivity. In both cases, the top chlorine layer forms silicon chlorides that are removed during the etching step according to the following reaction: **Si(s)+Cl(g)-> SiCl(g)**.

Adsorbed chlorine on the Si surface weakens the underlying Si bonds making them easier to break compared to the pristine silicon lattice in the bulk material. The Si-Cl bonds have a binding energy of 4.2 eV, which is much stronger than the Si-Si binding energy, which is 3.4 eV [5]. Park et. al explained the weakness of the Si bond under the chlorinated layer by a charge transfer just underneath the $SiCl_x$ layer (electrons transfer from Si–Si to Si–Cl bonds makes the bonding strength between the underlayer Si weak compared to the pristine Si) [10]. This in turn lowers the binding energy of $SiCl_x$ as the Si bonds underneath reduce from 3.4 eV to about 2.3 eV. However, ALE based on molecular chlorine can be performed at room temperature and the process does not need any cooling process because 20 ^{0}C is enough to suppress the thermal desorption of Si-Cl, which is known to occur at 650 ^{0}C.

2.2.2 Purging step (step 2)

After the modification step, the excess amount of Cl_2 is purged from the reaction chamber in order to prevent any modification to the etched surface during the etching step. This is critical as cross-contamination due to the unwanted Cl_2 may lead to a loss of atomic-scale precision due to parasitic contribution from RIE where both activation and etching process occur at the same time [16]. The purging time should be as short as possible in order to reduce the cycle time, but sufficient to remove all excess Cl_2.

2.2.3 Etching Step (Step3)

The etching or removal step comes immediately after modification and the first purging step. The purpose of this step is to take away the modified layer ($SiCl_x$) while keeping the unmodified layer (Si) intact. The total amount of etched material (etching depth) is determined by the number of cycles while etch per cycle (EPC) is estimated by dividing the total etching depth by the number of cycles.

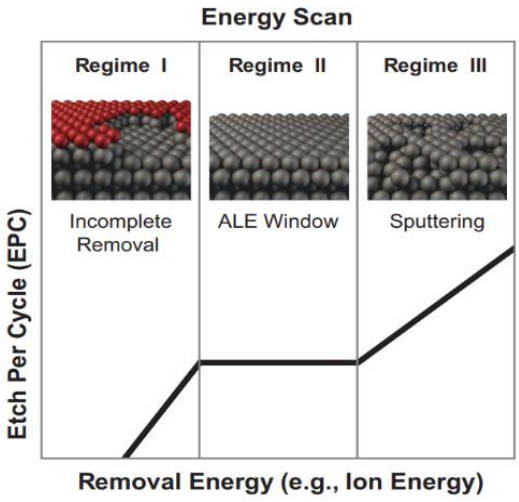


Figure 4. The ALE window indicates in Regime II [5].

The etching step includes material removal from the surface that can be implemented by three different approaches: (a) thermal (sublimation), (b) chemical, and (c) using ion collisions (bombardment). The etching process can be performed thermally by raising the wafer temperature above 650 ^{0}C which is the threshold temperature for removing SiCl and keeping it below 1500 ^{0}C to keep the unmodified Si layer intact [17]. Thermal etching is not a desirable technique due to its isotropic etching and can not be used for temperature-sensitive structures. However, chemistry is also another method that can be used as an etching technique where the chemical reaction can form species that are more loosely bound and thus more easily removed from, the surface. In order to speed up the chemical reaction, the plasma can be used to dissociate reactive gases into highly reactive radicals which are adsorbed by the surface and convert to volatile species.

In ALE two material removal techniques are commonly used: plasma or ion beam ALE (collisions) and thermal ALE (chemistry). Alternatively, plasma etching using the accelerated ions toward the surface (Ar^+ in this project) is efficient in order to provide directionality and a lower temperature process [18]. ALE process has a specific energy range of incident ions, it calls ALE window, Figure 4, where ions should have energy higher than the binding energy of the modified layer and lower than the binding energy of bulk material. In the case of etching Si by using Cl_2 as process gas, the energy of incident ions (Ar^+) should be between 2.3 eV (the binding energy of the modified Si layer) and 3.4eV (the binding energy of bulk Si). In fact, the

energy of incident ions must be greater than this energy which is about 50 eV due to inefficiency in transferring ion energy to the target bond [19]. However, the calculated yield of the incident ion (Ar^+) is about 0.1 which means, it needs ten ions with 50 eV energy to eject one SiCl during the etching process [20].

2.2.4 Purging step (Step 4)

Etch purge is the step after etching is done and it is the last step on one completed cycle when the by-products formed after removing the modified layer are purged out in order to clean the chamber. The purging time should be long enough to take out desorption products such as SiCl and $SiCl_3$ otherwise if the time purging is not long enough, some of the by-products will remain inside the chamber and may affect the sequential cycle and lead to extra etching which alters the etching resolution of the whole process.

2.3 Damage formation

ALE and RIE processes containing plasma might change the surface quality of the etched material which means these factors might cause damage formation that can be classified into different types. The introduced damage can be structural, chemical, optical, or electrical. The crystalline structure of etched material can be changed due to ion bombardment which creates defects, interstitial, ion implantation, or results in surface roughness [35].

Chemical damage is a common issue faced by compound semiconductors like GaAs. When a compound is removed from the material, it alters the chemical composition of the surface. Consequently, materials possessing a direct band gap may experience optical damage, leading to a decrease in luminescence intensity. This damage occurs due to the formation of non-radiative combination centers within the band gap, resulting from structural damage. Additionally, plasma-assisted etching of semiconductor materials can lead to electrical damage by introducing levels within the semiconductor's band gap. These additional levels hinder the flow of current by impeding the movement of charged carriers [36].

2.3.1 The possible source of damage during RIE

The RIE can be described as a continuous and simultaneous process in which the modification, etching, and purging steps occur at the same time. Basically, the positive ions pull out from plasma and accelerate by RF bias toward the target wafer surface and in synergy with neutral chemical species from the plasma, a desirable thickness of the wafer will be removed.

A continuous process is helpful to get high etch rates but also presents some limitations such as poor control of etching rate due to continuous process which makes RIE not applicable to achieve atomic layer resolution. Also, at the end of etching process the formation of a thick mixed damage layer on the top surface will increase the roughness of the surface. This layer is including a mix of reactant and the pristine surface atoms, dangling bonds, and structural defects such as atoms displacement. This type of defects will cause reducing the surface quality and affect the optical and electronic performance of the fabricated device.

In fact, the limitations of the RIE depends on the process parameters such as ions bombardment, UV light from the plasma and contamination inside the chamber. Actually, the ion energy represents the main source of damage during RIE process because it can be hundreds of electron

volts and high ion energy means high possibility for damage generation. Also, current density and mass of the ions might affect the damage formation where higher ions mass correspond to high kinetic energy of ions and it results ion implantation defect.

A damage from UV-light can be another type of damage produced by plasma discharge when high-energy photons can enhance unwanted etching for etched material. In the case of silicon, the damage results by plasma containing chlorine, especially at low ion energy. Photo-assisted etching originates from the charge transfer process, thus in plasma containing chlorine Cl, the photoelectrons are collected by Cl then the photo-generated hole causes the breaking Si-Si bonds. However, this phenomenon is observed obviously at low ion energies process, especially for wavelength less than 1700 Å [13]. In the case of Si-Si bonds, the incident photon enhanced the physical spurting of Si surface by breaking the Si-Si bonds which in turn degrades the surface quality by increasing surface roughness.

Poor control of etching rate is one of the limitations which attributed to the fact that etching rate is proportional to density of ions and radicals which supplied to the etched material surface [5]. RIE as etching process containing plasma, the generation of reactive and non-reactive species (ions and neutrals) are coupled to the same electron energy distribution. As a result, all reactants continuously bombard the surface having almost the same energy causing degrading of the surface quality by forming the thick mixed layer or increasing the surface roughness. The mixed layer and surface roughness are counted as structural damage also might affect the electrical and optical properties of the fabricated device. The thickness of the mixed layer could be reduced by reducing the energy of incoming ions, but it will reduce the etch rate at the same time which makes the damage formation and etching process coupled in such a continuous process.

Figure 5 shows the measurement of atomic force microscopy AFM on the Si surface before and after plasma treatment. As described before, the plasma is quasi-neutral, i.e., does not have an excess electric charge, containing high energy ions and UV light that might affect the quality of the surface by introducing structural damage in form of roughness. The roughness of the Si surface before plasma treatment was 0.5 nm and increased to 2.5 nm after plasma processing which means that the plasma has introduced physical damage as increasing the roughness of the surface [31].

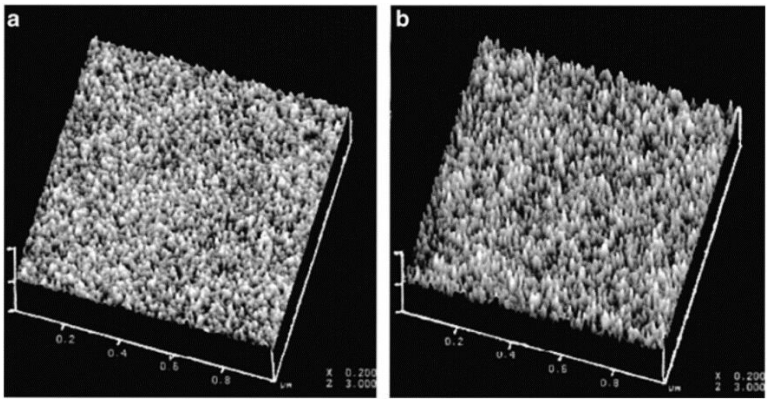


Figure 5 Atomic force microscopy image for the Si samples before and after plasma treatment [31].

Taking silicon as the case of this project, the high energy ions hitting the Si surface might generate structural damage due to the physical sputtering of Si atoms. The structural damage presents as vacancies, atoms displacement, interstitials, and dangling bonds Si^{+2} and Si^{+3}. In

another material such as SiO_2, the structural damage takes the form of breaking of the Si-O bond resulting in the formation of dangling bonds. In some cases, the structural damage is correlated with electrical and optical damage when the defects create an additional density of state in the energy bandgap which can affect badly the electrical and optical properties of the devices [23].

2.3.2 The possible source of damage during ALE

Atomic layer etching as described before is a cyclic process and each cycle is based on four steps modification, first purging, etching, and second purging. Basically, ALE is a similar technique to RIE while the main difference is that RIE is a simultaneous and continuous process. The damage can be introduced during ALE due to plasma used at the etching step which opens the door for damage formation for the same reason as in RIE. As shown in previous studies [5], [16], the final expected damage caused by ALE is much lower compared to RIE treatment due to the cyclic nature of the ALE process. This part will discuss how the damage during the ALE process forms and explain how it could be minimized or eliminated.

2.3.2.1 Modification step (1)

In the case of Si as etched material, the modification process is essentially performed either by molecular or atomic chlorine. In the case of molecular Cl_2, the gas will inject inside the chamber and thermally transported to the surface substrate and interact with Si to form the Si-Cl layer. This process typically takes 10s seconds up to minutes and it is not an extremely fast process and required some exposure to Cl_2 in order to create a monolayer of Cl on the top surface. In order to speed up the chemical reaction, plasma chlorination can be used to dissociate the molecular Cl_2 to provide radicals $Cl^{\bullet}$. Plasma activation will also generate ions Cl^{+}, Cl^{2+}, and photons which might be a source of damage during the modification step.

The worst scenario that can be taken place during this step is an etching of bulk Si or incomplete covering of the Si surface by Cl_2 gas. These imperfections might lead to form structural damage in form of surface roughness. How perfect the modification process is depends on a number of parameters, such as surface temperature, uniformity of Cl ion flux (plasma chlorination), ion energy (plasma chlorination), and exposure time.

The temperature inside the chamber is considered important due to the possibility of thermal desorption of the modified layer. In case of high temperature, it will result in an insufficient concentration of species on the surface and as a consequence incomplete removal of the top layer during the etching step. High temperature is not really desirable for the ALE process and alternatively low temperature depending on the gas process is desirable to make sure that the adsorption is completed. However, in the case of the Si-Cl bond, it needs up to 650 ^{0}C to be broken therefore the room temperature will suppress any spontaneous etching during this step and is suitable for the complete adsorption process to avoid forming surface roughness [5].
The modification process as mentioned before can be achieved by molecular or atomic gas process.

However, in the case of Si and plasma chlorination, the uniformity of the flux (Cl^{+}, Cl^{2+}, $Cl^{\bullet}$) is important to ensure that the Si surface is uniformly passivated by the active species and has the same etching rate during the etching step otherwise, a layer of nonuniform thickness will build up and results in surface roughness in subsequent steps [12].

In this project, only molecular Cl_2 has been used for the activation step that is why no damage can be considered by the energy of molecules. However, in case of plasma activation, the unwanted ions (Cl^+, Cl^{2+}) can be extracted and can reach the surface resulting in premature etching if their energy exceeds the binding energy of the Si-Si bonds. However, the threshold energy of the incident ion is lowered to 16 eV for chlorinated Si to be etched [13].
If the energies increase beyond the threshold energy, additional ion-enhanced etching will occur during the activation step by physical sputtering. One site can be passivated many times rapidly leading to producing roughness with an average greater than 1 ML (monolayer). Figure 6 shows these effects are enhanced at the edge of the feature which possibly sees higher fluxes than flat surfaces due to the larger view angle [12].

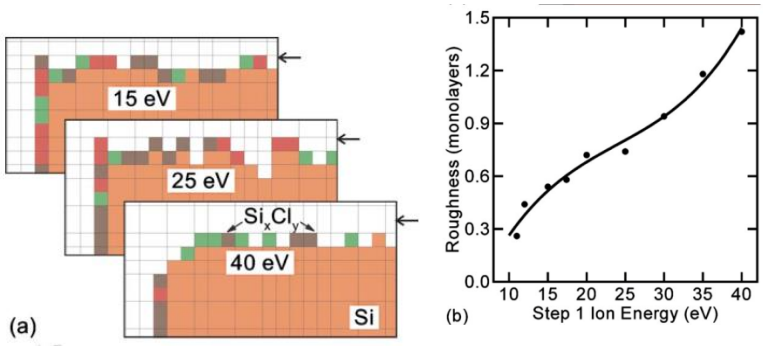


Figure 6. Surface roughness as a function of ion energy during activation process of plasma ALE. (a) Etching profile of Si-FinFET for modification step using 15, 25 and 40 eV ions energy. (b) Surface roughness as function of ion energy during modification step [12].

In addition to surface temperature, flux, and ion energy, the exposure time of the gas process has a crucial effect on damage formation during the activation process. Therefore, short exposure time will not be enough to cover all the Si surface and result in physical sputtering occurring on un-covered sites during the etching step, and this, in turn, will introduce roughness on the surface. While long chlorination time causes full covering of the Si surface, and it is not desirable because the excess amount of chlorine needs more time to pump out and it will make the whole process take a long time.

On the other side, when the plasma activation (atomic chlorine) is used, the longer exposure time with high ion energy can lead to stochastic etching as a result of etching and re-passivating of etched sites, and that in turn introduce roughness [12]. Using plasma activation will speed up the chlorination process compared to thermal activation from 10s to 1ms for for formation of one monolayer.

Ultimately, in order to form an activated layer with the proper thickness, there is a need to control the length of the exposure time and the energies of the incident ions of the gas process. Brichon et al. could achieve a chlorinated layer thickness of 0.5 nm by applying ion energy <10 eV and using a weakly dissociated plasma [14]. However, the thickness of this layer is less than that obtained in the continuous plasma process which is estimated at 4 nm at 50 eV and thicker than 20 nm at higher ion energy [15].

2.3.2.2 First purging step

Purging time should be long enough to pump out the extra chlorine and make the chamber clean and ready for the etching step. The remaining chlorine can adhere to the chamber wall; therefore, insufficient pumping time will result in an additional contribution of RIE and that might deviate the ALE regime with physical spurting which is not desirable during the etching process.

2.3.2.3 Etching step

In a perfect ALE situation after activation and purging steps, it would have adsorbed chlorine on the sample surface with no extra chlorine on the chamber wall or in a gas phase. The damage can be introduced during the etching step as a result of ions energy and UV-light generated by the plasma. The relation between the ion energy and surface atom binding energy is important in order to understand how the damage can be formed during the etching step. The relation is identified by what is called ALE window.

The optimal ALE process window requires ion energy to be sufficiently high to desorb the silicon chlorinated layer and not too high which could lead to uncontrollable sputtering. Typically, 50 eV for Ar ions are directed toward the wafer surface, as this energy is within the ALE window [5]. Even if the ion energy is within the ALE window, it is still a possibility to form damage because the energy required for desorption is higher than the binding energy of atoms underneath the modified layer [12]. Therefore, a physical sputtering will occur decreasing in etching resolution and that is in turn can cause structural damage to the surface in a form of roughness.

In the case of Si and Cl_2 as a gas process, argon ions Ar^+ of tens of eVs are used to bombard the Si surface in order to remove the modified layer Si-Cl. Chlorine adsorbed on the Si substrate will decrease the binding energy of Si-Si bonds from 4,7 eV to 2,3 eV. Ions with incident energy higher than 2.3 eV and lower than 4.7 eV (ALE window) will remove the chlorinated layer and leave the pristine Si intact.

Experimentally, the energy of incident ions is tens of eV and might be greater than 4.7eV the binding energy of pristine silicon and modified layer of 2.3 eV but it is still required due to insufficient energy transferring to the Si-Cl bond. Basically, the high energy of incident ions is deposited and leads to a collision cascade of the surface atom until a removed molecular $SiCl_x$ gets enough energy to escape in an upward direction from the surface [5]. In case the Ar^+ ions energy exceeded the ALE window, it might result in the physical sputtering of Si atoms and create damage in form of roughness. Comparing the degree of damage formed by RIE and ALE, we assume that damage formed by ALE is less than RIE because the ion energy is in the range of 10s eV compared with 100s of eV used in RIE. On the other side, the cyclic process in ALE allowed the separation between the modification and etching step while in RIE the surface is simultaneously and continuously bombard with active species.

As mentioned before, ALE is a cyclic process with steps that are correlated in the way that any deviation can occur at one step, it will affect the subsequence steps and result in damage or decrease the atomic etching resolution. Therefore, in case of imperfections in surface temperature, species flux, or ions energy during the activation step, it might result in incomplete coverage of the sample surface during the activation step. Incomplete covering means that some places on the surface will bombard directly with ions and that results in physical sputtering of the surface and increase the roughness. On the other hand, if the purging time is not long enough

during purging step 1, the gas process will adsorb again and the principle of a cyclic process of ALE will not be implemented because of the partial contribution of the RIE process.

Using plasma as source of ions, it could be problematic in term of generate a monoenergetic ions (the ions have same energy). Practically, ions generated by plasma can not be separated as high and low ions but instead there is something is called ion energy distribution (IED). IEDs represent how the ion energy spread and deviate from to be a monoenergetic ion. Consequently, when utilizing a wider range of ion energy that is not confined to the Atomic Layer Etching (ALE) window, there is a possibility of introducing ions with energy surpassing the binding energy of the bulk material. On the other hand, lower ion energy may not provide enough energy to remove the modified layer effectively. Figure 7 shows the ion energy distributions for different pressures under pulsed plasma conditions with a synchronous +24.4 V_{dc} bias applied on the boundary electrode in the afterglow. The plasma power modulation frequency is 10 kHz, 120 W average power, and 40 sccm argon gas flow [32]. For continuous plasma we expect have similar ion energy distribution which means a deviation in ion energy to be a monoenergetic ions. Consequently, achieving monoenergetic ions in the plasma etching process can be challenging. However, it is possible to optimize other process parameters, such as pressure, to regulate the width of the energy distribution and align it with the requirements of the etching process.

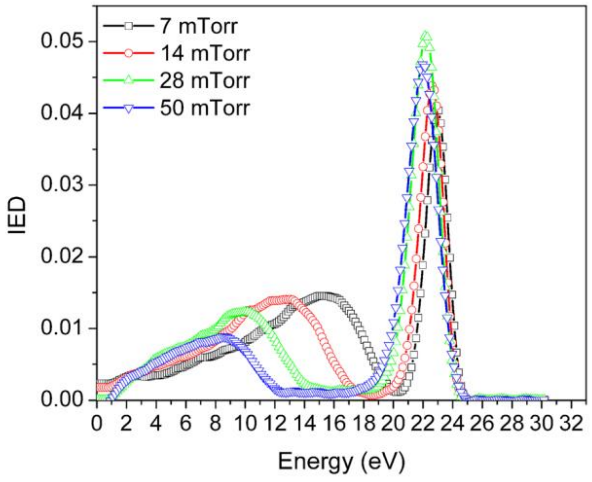


Figure 7. IEDs for different pressures under pulsed plasma [32]

2.4 Characterization methods.

As explained in the previous discussion, whatever etching process can be used, will produce damage within the surface wafer such as ion implantation, atoms displacement, voids, roughness, and other types of structural, electrical, and optical damage. However, in order to investigate surface damage, many techniques can be used in the characterization process which gives more details about the thickness of the damaged layer, surface roughness, and surface contamination that in turn improve our understanding of damage formation.

Therefore, the obtained information from characterization tools gives a perception of how the etching parameters (ion energy, etching and activation time, gas pressure, temperature, and gas flow) affect damage formation. Thus, comparing the degree of the formed damage with process parameters can lead to an optimal etching process with a lower percentage of damage. Several techniques can be used such as scanning electron microscope (SEM), atomic force microscope (AFM), transmission electron microscope (TEM), X-ray photoelectron spectroscopy (XPS),

and other techniques which can be useful. Each tool shows a specific type of damage and more tools we have means more different and important information can be obtained which in turn drives the etching techniques to an advanced level.

2.4.1 Atomic force microscopy (AFM).

Atomic force microscopy (AFM) is a type of scanning and high- resolution non-optical or electrical imaging technique for surface analyses. The principle of AFM as shown in Figure 8 is based on the measurement of forces between tip-sample. The atomic forces result in the deflection of the cantilever which can be recorded and analysed toobtain information about the scanned surface. AFM is a tool that enables topographical imaging of the sample surface and also AFM as a routing way can measure root mean square(rms) which represents the quantified value of the surface roughness.

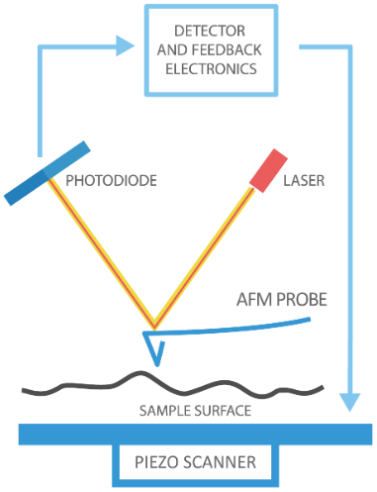


Figure 8. A schematic of atomic force microscopy tool.

Basically, AFM has three operating modes, contact, taping, and non-contact mode as shown in Figure 9. The AFM tip which is used for imaging the surface is typically a very tiny tip made of silicon or silicon nitride. Usually, tip deflects are measured by the reflection of a laser light pointed to the tip end. In the case of contact mode, the tip touches the sample surface moving over the feature of different hight which in turn causes a deflection in the cantilever. In tapping mode, also known as intermittent contact mode, the AFM probe oscillates close to the surface of the sample. The tip intermittently touches the surface during the forward oscillation, and then lifts off during the backward oscillation. On the other hand, non-contact mode, as the name suggests, operates without direct contact between the tip and the sample surface. In this mode, the AFM probe is brought close to the surface, but does not touch it.

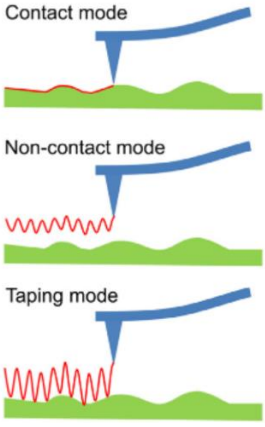


Figure 9. A schematic of three AFM modes.

As the tip scans over the sample the distance of the tip-sample changes due to attractive and repulsive forces, causing changes in oscillation amplitude and frequency. Comparing the actual measured amplitude and frequency with a reference value used as a feedback signal to generate a three-dimensional topographic image of the surface [25].

AFM is a handy tool in order to investigate the surface roughness before and after the etching process where the roughness of the selected area is calculated from the root-mean-square (rms) value of the height distribution of the surface. In this project a combination between AFM and Kelvin probe force microscopy is used for surface damage analysis where more details about KPFM will be presented next.

2.4.2 Kelvin probe force microscopy (KPFM)

Kelvin probe force microscopy (KPFM) is defined as a modified AFM tool that can measure the electrical potential of the surface. KPFM is based on a noncontact, non-destructive vibrating technique. The Coulomb force interaction between the charged surface and the tip will give additional information about the surface potential. Since its first introduction in 1991, KPFM has been used to study the electrical surface properties of materials such as metals and semiconductors and also explore the electrical properties of a wide range of nanomaterials and organic materials [26].

The working principle of KPFM is similar to that in AFM where the cantilever connected to the tip is scanned over the sample in order to measure the contact potential deference CPD between tip and the surface. The values of CPD might depend on what happens to the surface during the etching process. In other words, the values of CPD will reflect the degree of damage introduced to the surface which can be structural, electrical, or optical damage. In order to understand how the (CPD) generates, three cases of the distance between the tip and the surface should be discussed.

Figure 10a shows the case when the tip and surface are separated by sufficient distance to prevent any electrical connection where the tip and surface material have different inherent Fermi energy levels due to their structure and composition. Now if the tip is brought very close to the sample surface, in this case, the tip-sample is electrically connected through the interchange of electrons by tunnelling effect, therefore the Fermi levels of both tip and sample will be aligned and the whole system will be in equilibrium.
As a result of the equilibrium state, the vacuum level of the tip-sample will differ creating a potential difference called CPD as shown in Figure 10b where CPD is defined as follow:

$$\mathrm{CPD} = \frac{\Phi s - \Phi t}{e} \qquad (1)$$

In order to eliminate the CPD, an external bias V_{DC} has the same value of the potential difference applied as shown in Figure 10c. Consequently, if the tip work function is known, the sample work function can be calculated.

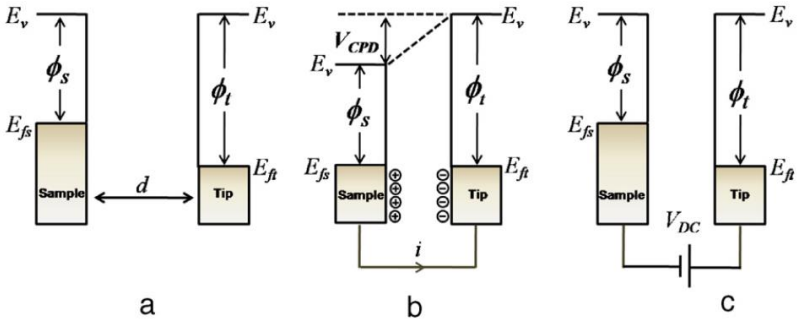


Fig. 10. Electronic energy levels of the sample and tip: (a) tip and sample are separated by distance d, (b) tip and sample are in electrical contact, (c) external bias (V_{dc}) is applied to nullify the CPD [27].

Figure 11 depicts the measuring process block diagram of the KPFM system. In order to measure the contact potential difference and thus the work function of the sample, an AC voltage with DC bias is applied between the cantilever tip and surface. V_{AC} in its turn generates an electrical force between the tip and the sample surface and V_{DC} is applied to eliminate the oscillating electric forces originating from the offset between the vacuum energy level of the tip and the sample where CPD originated.

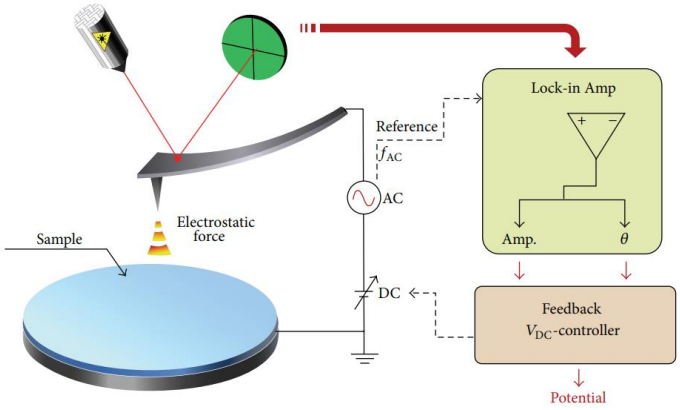


Figure 11. Block diagram of basic KPFM system [28].

By adopting the concept of the Kelvin probe method where the tip and the sample are considered as a capacitor, the electrostatic force generates between the tip and the sample is given as follows:

$$F_{el} = \frac{1}{2}\frac{\partial c}{\partial d} V^2 \qquad (2)$$

Where $\frac{\partial c}{\partial d}$ the gradient of the capacitance between tip and the sample which separated by distance (d) and (V) is the total tip-sample voltage that is given by the following equation:

$$V_{(t)} = V_{DC} - V_S + V_{AC} \sin \omega_{tip}.t \qquad (3)$$

Substituting eq.3 in eq.2 gives the equation describing the electrostatic force applied to the tip as followed:

$$F_{el}(t) = \frac{1}{2}\frac{\partial c}{\partial d} V(t)^2$$

$$= \frac{1}{2}\frac{\partial c}{\partial d}[(V_{DC} - V_s)^2 + \frac{1}{2}V^2_{AC}] \qquad (a)$$

$$+\frac{\partial c}{\partial d}(V_{DC} - V_s)(V_{AC} \sin \omega_{tip}.t) \qquad (b)$$

$$-\frac{1}{4}\frac{\partial c}{\partial d}(V^2_{AC} \cos 2\,\omega_{tip}.t) \qquad (c)$$

Both terms (a) and (c) can be described as the static deflection of the tip and capacitance microscopy respectively while the term (b) is used to measure CPD.

As a consequence of applying V_{AC} and V_{DC} to the tip, an additional oscillating originating from the electrical force will be added to the mechanical oscillation of the tip. Therefore, a lock-in amplifier is used for decoupling the AC signal from the mechanical signal in order to detect the electrostatic force between the tip and surface sample. The potential difference CPD is obtained by the V_{DC} applied to the tip when the output of the lock-in amplifier is equal to zero and in this case, the term (b) is nullified. The different values of DC bias at each scanning point are recorded to map the work function or surface potential of the scanned area [28].

As a similar work principle of AFM, KPFM has two scanning modes, amplitude AM and frequency FM where the electrostatic force will be detected. In AM mode the term (b) of static force measures from the amplitude of the cantilever oscillation at a frequency related to CPD and V_{AC}. As previously, a V_{DC} bias was applied to the tip to reduce the amplitude to zero thus, CPD can be measured. In FM mode the frequency is considered instead of the amplitude where the term (b) is detected by the frequency shift around the resonance frequency. Therefore, when the DC bias is applied to the tip, the frequency shift will be nullified thus, the CPD will be measured.

KPFM has many applications related to investigating the electric properties (work function or surface potential) of metallic and semiconductor nanostructures that are used in a variety of devices. These properties strongly affect local chemical and physical phenomena taking place at the surface and KPFM is able to discover any changes which can alter the performance of the device. Metallic nanostructures are widely used to build up devices like structures for catalyst, and chemical or biological sensors, and for these devices, the charge transfer in the interface between (metal/substrate) or (metal/chemical or biological molecules) is important to be studied due to its effect in modulating potentials on metal nanostructure such as Pt/TiO_2. KPFM has been used to investigate the surface of semiconductors such as Si, GaAs, and InSb where electrical properties like surface defects, phase state, and atomic composition have been studied [30].

Chapter 3

3. Experimental Details

All experiments in this research project were carried out at Lund Nano Lab. The project consists of three parts: 1) pre-etching process that involves sample preparation and shadow mask fabrication, 2) etching process where the samples are etched by two etching methods, reactive ion etching RIE and atomic layer etching ALE performed with the (ICP-RIE) system Apex SLR from Plasma-Therm LLC and 3) post-etching process where the etched samples are sent to the Danish metrology institute for characterization and analysis process using Kelvin probe microscopy (KPFM). Figure 12 shows a schematic of experimental approach.

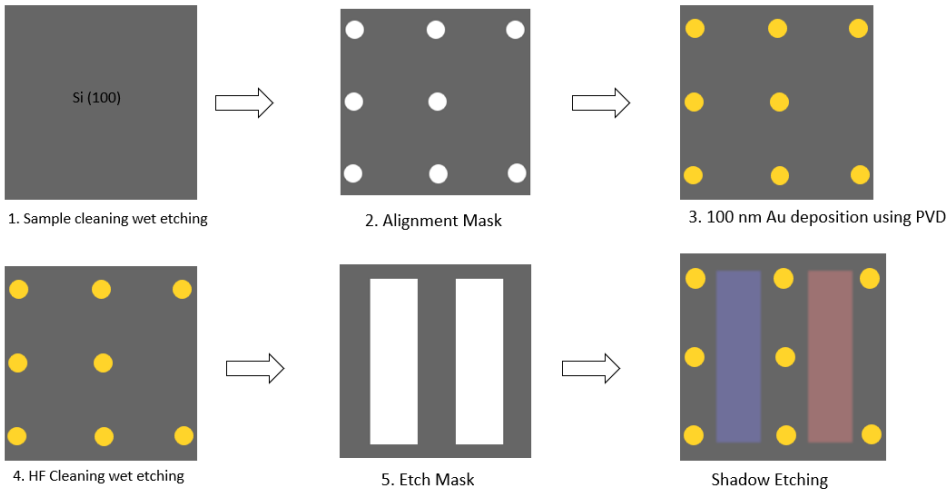


Figure 12. A schematic of experimental approach.

The samples used for this study are Si (100) and used for studying damage after etching process ALE and RIE techniques. Using the masks was introduced during this project in two steps (gold deposition and etching process). The sample has been cleaned by HF before etching process in order to remove the native oxide as shown in image 4, Figure 12. Concerning the etching process, both ALE and RIE included usage of protection shadow masks in order to protect some part of silicon to have both etched and unetched parts on the same surface. While for gold deposition the mask used for deposit gold dots in some parts of silicon surface.

3.1 Pre-Etching process

3.1.1 Sample preparation.

The samples used in this work were made from 2-inch silicon wafer Si (100) n-type, 279±25 µm thick, with a resistivity of 1-10 Ohm cm. The wafer was cut into small samples with a size of 10x10 mm^2 and then it was cleaned with acetone for 3 min in an ultrasonic bath and after that in isopropanol IPA for 3 min. Finally, the samples were dried by an N_2 drying gun.

3.1.2 Masks fabrication

Two shadow masks have been used in this project, the first mask was used for gold deposition, and the second one was used for the etching process. However, the gold deposition mask is used for depositing gold dots with 100 nm thick on top of the Si surface in order to use it as alignment marks to get good orientation for the sample. For calibration purposes, gold dots have a different surface potential than silicon, so it used as defining points where the silicon surface is located when KPFM analyses are performed. Figure 13 shows an image of the deposition mask where the mask has a size of (10x10 mm) and has seven holes (1 mm) in diameter and it separates in such a way as to make it easy to find etched surfaces.

Figure 13. Shadow mask used for gold deposition.

An additional mask is also used for the etching process in order to have both the etched and pristine Si area on the same surface. However, having an etched and unetched area on the same surface gives the possibility to study the interface position and investigate any changes in surface potential. The reason why the shadow mask is used instead of coating a photo-resist mask or any type of passivation mask is to keep the surface of the Si sample protected from any chemical reaction which could damage the surface structure and alter the surface potential of the pristine silicon.

Figure 14 shows an image of an etching mask where the mask has size 10x10 mm and has two long oval holes with (8 mm) long and (2 mm) width which identify the etched area and the rest area which is covered by the protected and define the unetched surface.

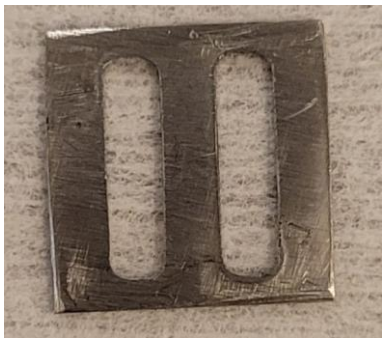


Figure 14. Shadow mask used for etching in both RIE and ALE.

The material of the masks is aluminum (Al) which is selected so that it will not react with process gases (Cl and Ar), and it is made from the same material of the chamber to keep the homogeneity of the internal environment. The masks were made at the Physics Department

mechanical workshop at Lund University and cleaned before using them inside the cleanroom by using the same recipe used for cleaning the sample but for a longer time.

3.2 Etching process

3.2.1 Etching tool.

Atomic layer etching as well as reactive ion etching process performed with Etcher APEX SLR Cl-based ICP-RIE plasma Therm LLC [22], Figure 15. The tool has the main chamber with thick aluminum walls and a load lock which can be opened in order to place the sample before transferring it into the main chamber. Having the load lock is beneficial in terms of saving the time needed for purging time with N2 in order to maintain equal chamber conditions before each etching process. Both chamber and the load-lock could be evacuated by pumping and vented by connecting them to the source of N2. The chamber and the load-lock are separated with a door that can be opened automatically when the Y-shaped arm is moves out from the chamber to bring the sample from the load-lock. When the sample moved inside the chamber, it is fixed with a mechanical clamp, and its temperature is maintained by using helium gas (He) flow out through three holes under the sample.

If the sample is placed incorrectly in its specific position, there is a risk that the sample will move, and it could be damaged and sometimes it causes chamber contamination. Therefore, a maintenance process is needed in order to take out the sample manually and this is in fact what happened during one experiment in this project. However, the process gases are transferred to the main chamber by two gas inlets, one for N2 for the venting process and another inlet for the gas mixture. The gases flow through the lines is controlled by using a mass flow controller (MFC).

Figure 15. APEX SLR Cl-based ICP-RIE plasma Therm LLC.

The plasma is generated in two ways which can be used together or separately. The first way is using electrodes where two plates in the shape of a capacitor are connected to a radio frequency (RF) source power. The plasma generates when the gas flows between the electrodes and at the same time, a negative voltage bias is built up on the wafer surface which extracts and accelerates the positive ion from the plasma toward the surface in order to etch it. Generating plasma can

be done also by using surrounding coils around the top part of the chamber where alternating current is inductively created by an RF power generator. In this case, the plasma will generate inside the space within coils. However, another gas process can be used which is BCl_3 for other applications and only a 2-inch wafer is allowed. The tool is located in the Cluster Tool room Q258, NANO-epitaxy Lab (Cleanroom Level 2), Lund Nano Lab.

3.2.2 Hydrofluoric acid cleaning

The nature of silicon exposed to air is that a layer of silicon oxide forms on its surface, which must be removed before the etching process, therefore the use of hydrofluoric acid (HF) is necessary where all the samples are dipped for 1 minute in HF bath and then cleaned by deionized water for 30 sec and finally dried for 30 sec by N_2 gun. HF is a dangerous acid therefore, protective clothing and equipment must be used when dealing with it, in particular, neoprene or thick nitrile gloves and eye protection.

3.2.3 Atomic layer etching process for Si

It has previously been shown that an ALE process includes 4 steps that are repeated a specific number of times in order to get the optimal etching depth. In this work, molecular Cl_2 gas was used for surface activation where Cl_2 reacts with the Si surface to build $SiCl_x$ which reduces the binding energy of the Si surface atoms and activates the surface for the etching step. In the first purging step, the extra amount of Cl_2 inside the chamber is pumped out to prevent the activation process by Cl during the etching step. In the etching step, the energetic Ar^+ ions bombard the activated surface to remove a very thin layer up to a Si monolayer. Finally, one more purging step is needed to remove by-products and make the chamber clean for a new cycle. Table (1) shows the parameters that have been used in the ALE process. The expecting etching depth according to this flow is almost 8 nm.

Activation	**Purge (1)**	**Etching**	**Purge (2)**
Cl_2 = 1 sccm	Cl_2 = 0 sccm	Cl_2 = 0 sccm	Cl_2 = 0 sccm
Ar = 0 sccm	Ar = 40 sccm	Ar = 10 sccm	Ar = 40 sccm
ICP = 0 W	ICP = 0 W	ICP = 0 W	ICP = 0 W
RF = 0 W	RF = 0 W	RF =15-25-50 W	RF = 0 W
Temp = 20 ^{0}C	Temp = 20 ^{0}C	Temp = 20 ^{0}C	Temp = 20 ^{0}C
Time = 2 sec	Time = 40 sec	Time = 10 sec	Time = 2 sec
Pressure = 3 mTorr	Pressure = 3 mTorr	Pressure = 3 mTorr	Pressure = 3 mTorr
He pressure = 5mTorr	He pressure = 5mTorr	He pressure = 5mTorr	He pressure = 5mTorr
He flow = 5 sccm	He flow = 5 sccm	He flow = 5 sccm	He flow = 5 sccm

Table 1. The selected parameters for ALE process include 4 steps.

3.2.4 Reactive Ion Etching process for Si

As described previously RIE process is a continuous and simultaneous process where activation and etching occur at the same time. In this work, molecular Cl_2 is used as reactive species to modify the Si surface, and Ar ions can physically etch material simultaneously with the reactive removal species. Table (2) shows the process parameters used for RIE process. The expecting

etching depth according to the parameters shown in Table 2 is about 40 nm and it is higher compared to ALE since RIE has faster and higher etching depth profile.

Cl_2	Ar	ICP	RF	Temp	Pre	Time	He Pre	He flow
20sccm	5sccm	0	35 W	20 C^0	5 mTorr	2 min	5 mTorr	2 sccm

Table 2. The selected parameters for RIE process.

3.3 Post etching process

After the Si sample has been etched by both techniques, RIE and ALE, the etched sample is scanned by KPFM in order to analyze the possible formed damage and obtain a topographical image of the sample surface. Park NX 20 and Bruker multiple systems are used in KPFM measurement, and the data collection is done under normal pressure conditions. Figure 16 shows the schematic measurement of surface potential and surface topographical image using KPFM.

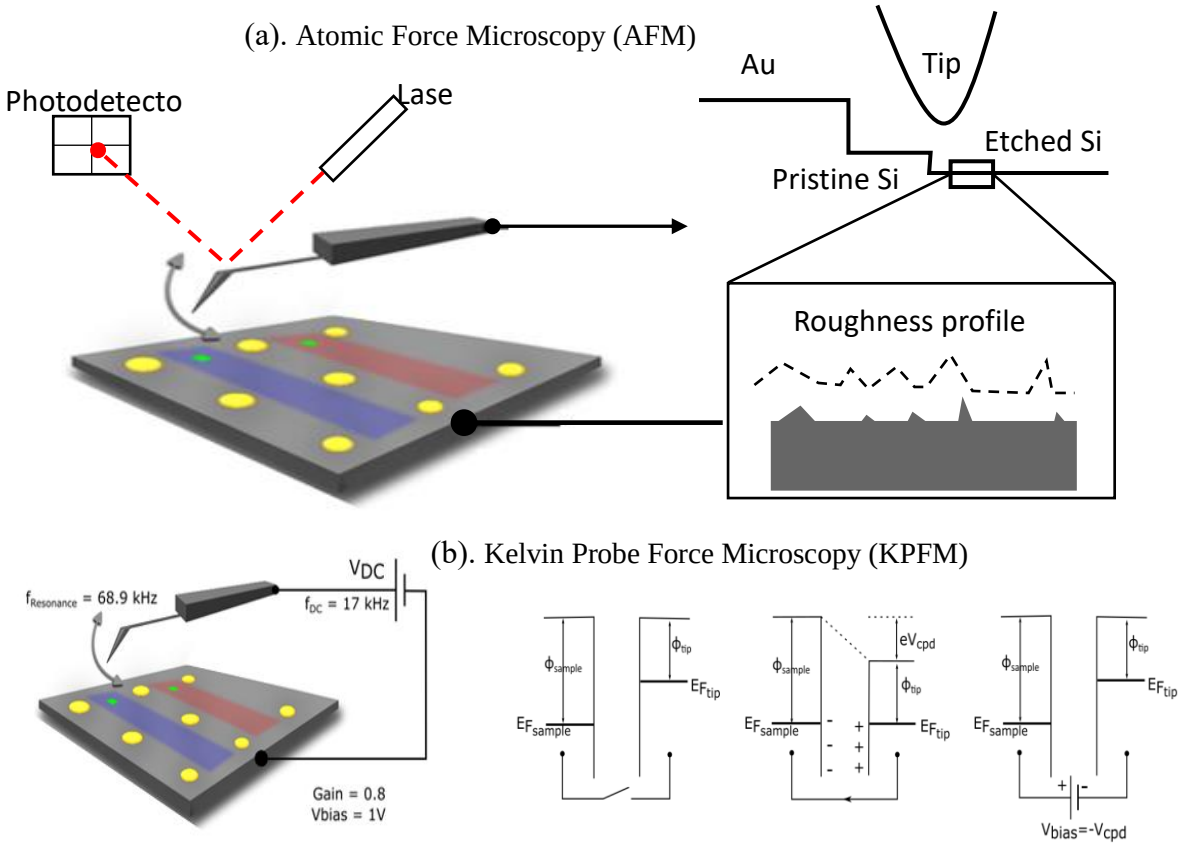


Figure 16. A schematic of (a) Atomic force microscope AFM and (b) Kelvin prob force microscopy KPFM measurement.

Chapter 4

4. Results and discussion

In order to evaluate the surface damage introduced by etching, three ALE samples with three different RF power levels and one RIE sample have been investigated. In both processes, the same chemistry has been used which is molecular chlorine Cl_2 and argon Ar in the gas phase. In this project, KPFM was used to measure contact potential deference and the roughness of the etched Si samples. The obtained CPD and rms values in its turn will reflect the degree of the produced damage.

In RIE both Cl_2 and Ar continuously and simultaneously bombard the Si surface with typical ion energy of hundreds of electron volts. While ALE is a cyclic process that uses Cl_2 chemisorption to modify the Si surface and Ar ions with energy of tens of electron volts to remove the modified layer. As the energy of reactive species (Cl_2 and Ar ions) and the nature of RIE differ from ALE, therefore, the expected damage in RIE might be significantly higher than the damage produced by ALE.

KPFM calibration method: Initially, a calibration process was performed to calculate the tip work function which is needed later to identify the correct value of the work function of the etched and unetched Si surface. The calibration process is based on the region shown in Figure 17 which is the top right gold dot corner because this position was covered by the mask. Therefore, this region is not etched and is considered as a reference Si.

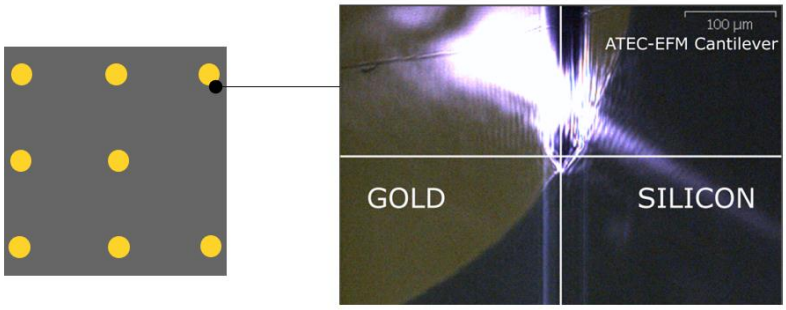


Figure 17. The position where the calibration process was done.

Figure 18a shows the 3D map acquired after scanning the interface area between the gold dot and Si surface by using AFM. This 3D map is based on four color scales; in our case, the brighter color corresponds to a larger height. Therefore, the left bright part corresponds to the larger in height which is gold (100 nm thick), and the darker right part refers to the Si surface which is lower than gold. Figure 18b is the 2D projection of the 3D map which shows the different heights of different positions going from Au to Si.

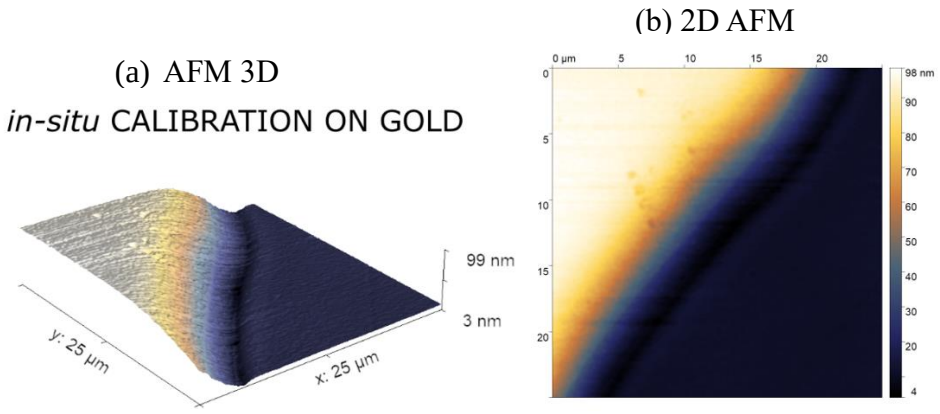


Figure 18. (a) A 3D AFM map shows different hight between Au and Si. (b) 2D projection of the 3D map.

After AFM measurement is done, KPFM has been used to measure the contact potential difference which means the difference between tip and surface Fermi energy levels. As the tip approaches the surface the Fermi energy levels of the tip and the surface start to match and then V_{dc} is applied to compensate for that difference in vacuum energy levels. Then the obtained CPD values are used to calculate the work function of scanned materials as shown in Figure 19.

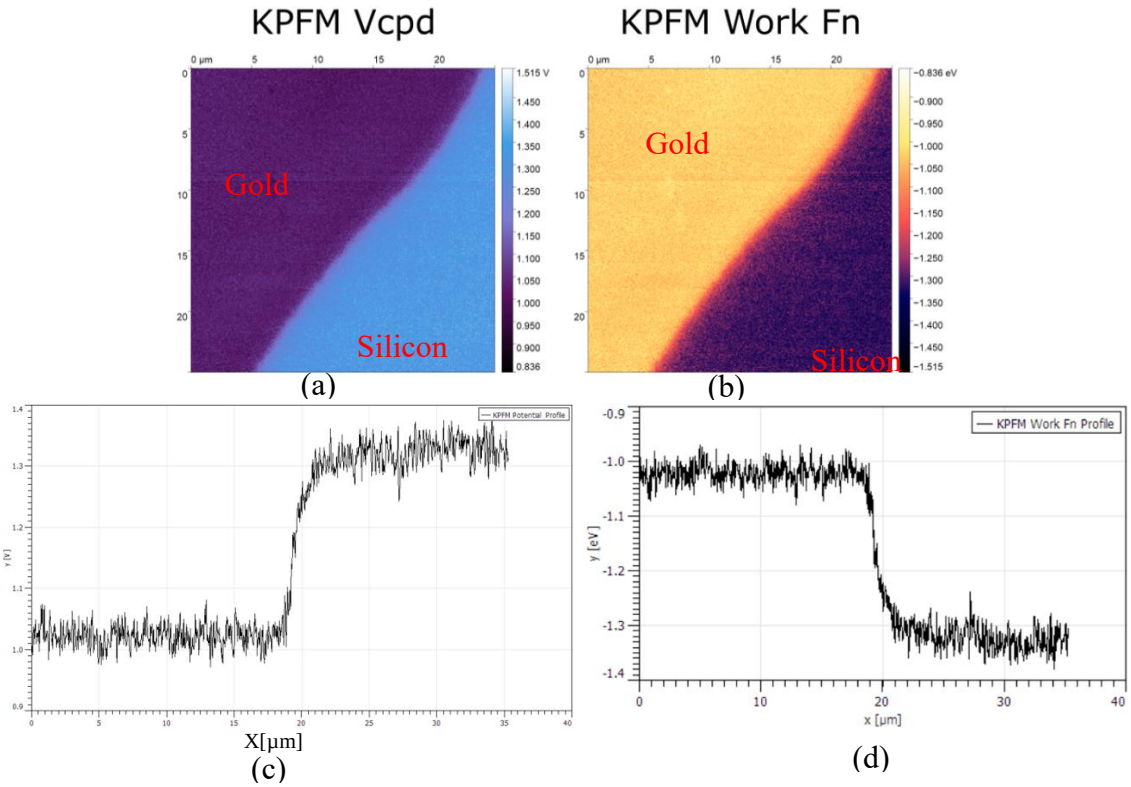


Figure 19. KPFM measurement of CPD and calculated work function of Au and Si.

Figure 19c and 19d show the corresponding change in CPD and work function profiles starting only after a very sudden step indicating the transition from gold to the silicon. This means that there is no surface contribution or artifacts generated to change the morphology which might affect the measured work function.

Usually, in KPFM, gold is used for the calibration process. After data analysis, the mean work function of the gold region was (- 1.032 eV) and the literature value is (5.1 eV) [33]. The difference between the measured and literature value is calculated as follows and added as an offset to all measurement for the calibration traceability to the literature.

$$[\Phi_{Au}]_{lit} - [\Phi_{Au}]_{mesu} = 6.132 \text{ eV}$$

By moving down to the Si region, the Si measured work function is (-1.311 eV) and by adding the offset value to the measured value, the real value of Si work function can be calculated as follow.

$$[\Phi_{Si}]_{mesu} + \text{offset} = 4.821 \pm 0.038 \text{ eV}$$

this measured value is very close to the $[\Phi_{Si}]_{lit}$ value which is (4.85 eV) indicaying that the pristine Si sample is a Si (100) [33].

AFM and KPFM measurement of RIE sample: AFM measurement of the interface between etched and the unetched surface is shown in Figure 20 where the sample has been etched under conditions reviewed in Table 2. Figure 20a shows the AFM data of the intermediate zone between etched and unetched surface. The corresponding surface potential and work function data of the partially etched areas are shown in Figure 20 b, c.

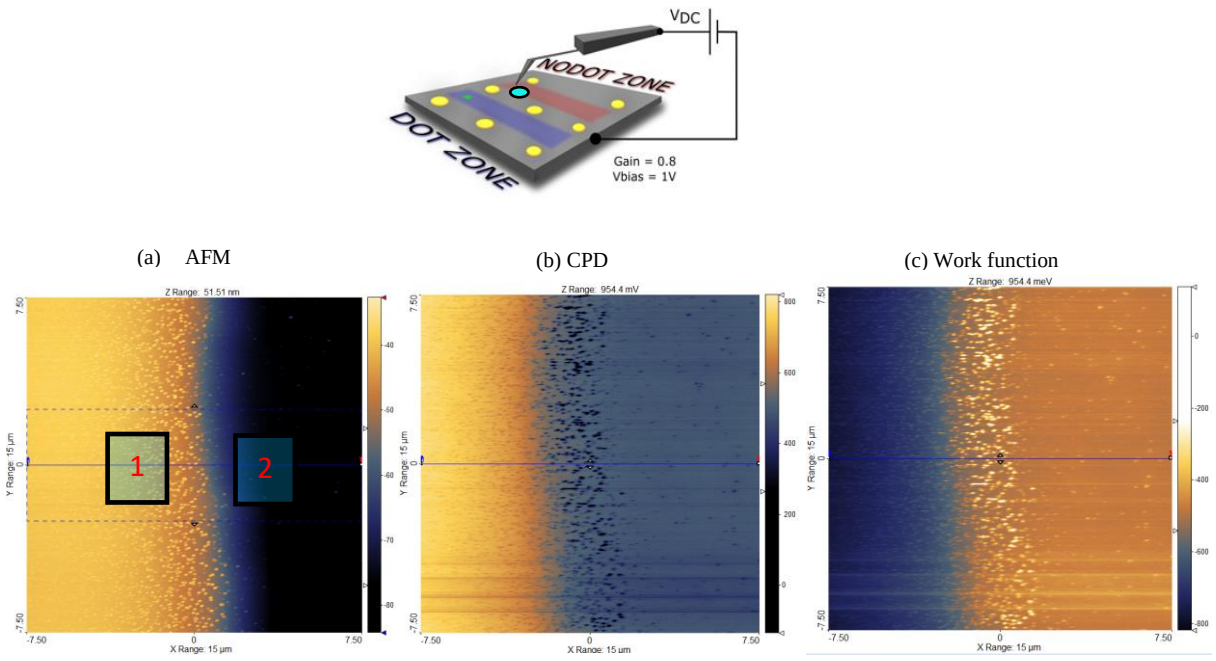


Figure 20. AFM and KPFM measurement of the interface between (1) covered and (2) uncovered Si surface. (a) AFM, (b) CPD and (c) work function.

Zone 1: By selecting the zone (1) in Figure 20a which represents the covered Si surface exactly beside the opening where the etching process is occurring. The measured data of AFM, CPD, and work function for this area is shown in Figure 22 a, b, and c respectively. By looking at the AFM data, the covered area still has partially etched areas due to ions penetration under the mask which causes a surface roughness of (0.3851 nm). The high roughness value reflects the incomplete etching process under the mask due to the change in ion density which interacts with the Si surface. The difference in ions density is due to the gap between the shadow mask

and the Si surface which results in a gradual transition between etched and unetched areas as shown in Figure 21.

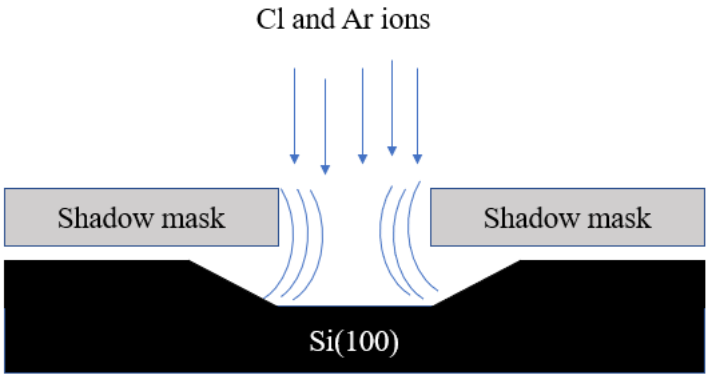
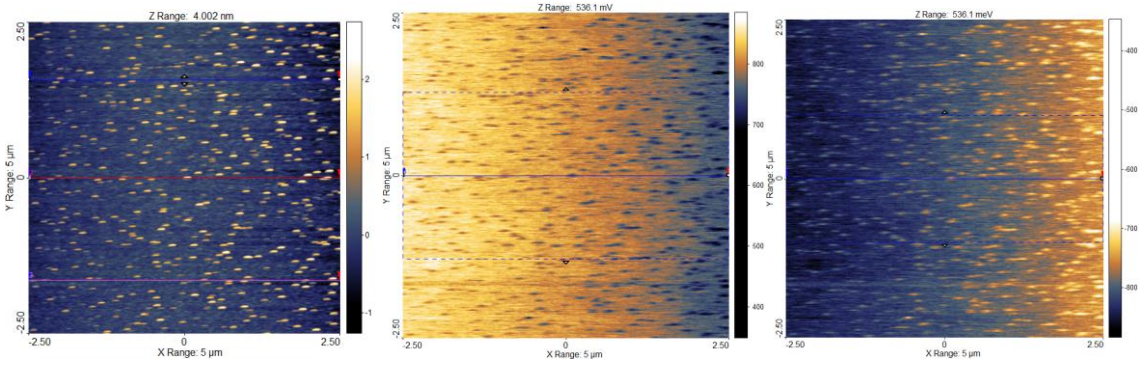


Figure 21. A schematic cross section of shadow mask effect on the Si surface.

The damage introduced in this area is translated to observed changes in the CPD. Thus, the measured work function (4.067 eV) of this area is much lower than the work function of the reference Si sample (4.821 eV) which means that the surface has been damaged.

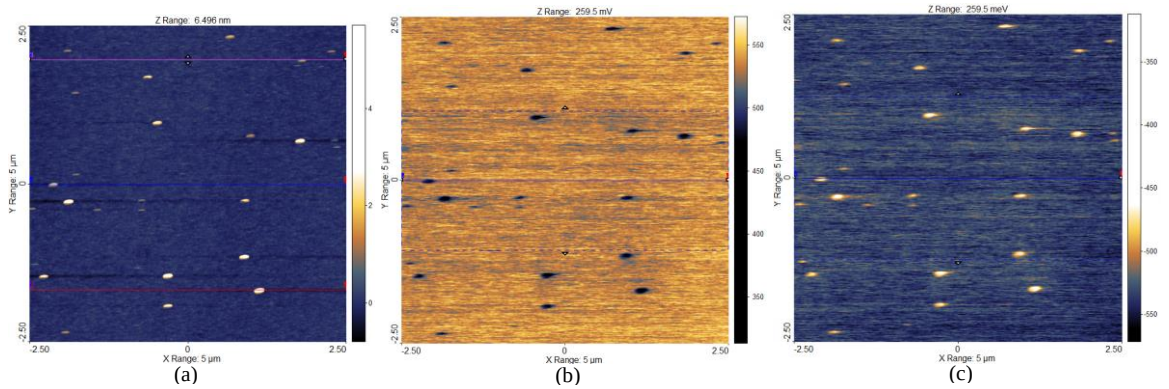


(a) (b) (c)

Figure 22. AFM, KPFM measurement for the zone (1) covered silicon. (a) AFM, (b) CPD and (c) work function.

Zone 2: Moving to the area which is indicated by (2) in Figure 20a which represents the partially etched area where the surface has not been covered by the mask. The measured data of AFM, CPD, and work function for this area is shown in Figure 23 a, b, and c respectively.

The AFM data of zone 2 is different from that of zone 1, the etched area still has partially etched places, but it looks better than zone 1. The partially etched area causes a surface roughness of 0.2059 nm. The lower roughness value reflects the improvement in the etching process in the open area, but the damage still exists. The damage formed within this area is due to change of ion density which interacts with the Si surface because of the shadowing effect of the mask edge where the ions can deflect. The damage introduced in this area is translated to changes in the CPD. Thus, the measured work function (4.33 eV) of this zone is higher than the work function of zone 1 (4.067 eV) but it is still less than the reference value (4.821 eV) which means that the surface has been damaged.

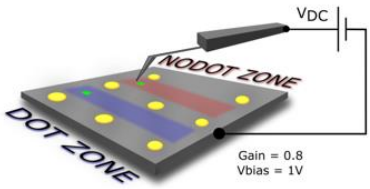


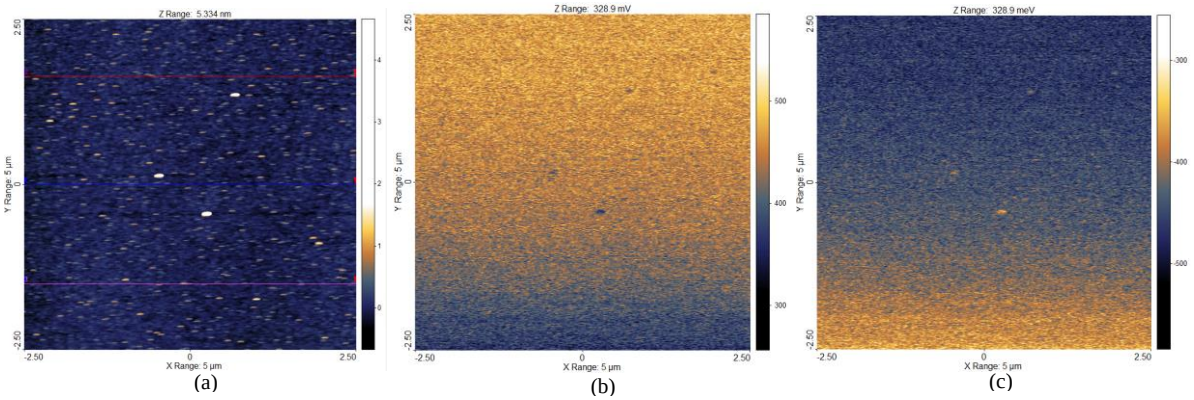
(a) (b) (c)

Figure 23. AFM, KPFM measurement for the zone (2) partially etched silicon. (a) AFM, (b) CPD and (c) work function.

RIE of open area: Now moving further away from the interface area to the middle of the etched place where a complete RIE process is applied to the Si surface and not covered by the mask. The measured data of AFM, CPD, and work function for this area is shown in Figure 24 a, b, and c respectively. The RIE etched area looks good and improved compared to the interface area but still has spots that have different heights in AFM measurements. The pure RIE on the etched surface led to a decrease in the surface roughness down to (0.1754 nm).

The measured work function is (4.321 eV) which is about the same as the work function of the zone 2 (4.33 eV) but it is still less than the reference value (4.821 eV) which means that the surface has been damaged.





(a) (b) (c)

Figure 24. AFM, KPFM measurement for the zone (2) pure RIE area. (a) AFM, (b) CPD and (c) work function.

Comparison of the AFM and KPFM data of zone 1, zone 2, and pure RIE leads to a conclusion that the partial RIE region in the interface demonstrates much greater damage both on the surface morphology (roughness) and work function of the Si compared to the complete RIE area.

KPFM measurement of ALE sample: In the second part of this project, three Si samples were etched by ALE under three different RF power as shown in Table 1.

ALE 50 W sample: Figure 25 shows the KPFM measurement of the Si sample etched by ALE for 100 cycles and 50 W of RF power. The sample has two etched areas, indicated as blue and red, both areas etched at the same time with the same conditions. Figure 25a shows the CPD and calculated work function of the area selected from the red zone where the measured CPD (1.281 V) which corresponds to the work function of 4.851 ± 0.017 eV. Figure 25b shows the measurements in the blue zone, with the CPD of 1.370 V and the corresponding work function of 4.762 ± 0.025 eV. Both etched zones have a homogenous distribution of CPD and this, in turn, will reflect in the perfect distribution of the work function which means no defect has been detected. By comparing the measured CPD and corresponding work function, we observe that both etched areas have values of work function that are close to the theoretical value of the Si work function. As a conclusion, ALE as a cyclic process has not caused any structural or electrical damage to the etched surface, thus there is no defect generated and the band gap of the Si has not been changed by the etching process. This is very important for electronic device based on Si such as integrated circuits, transistors, diodes, and many other applications.

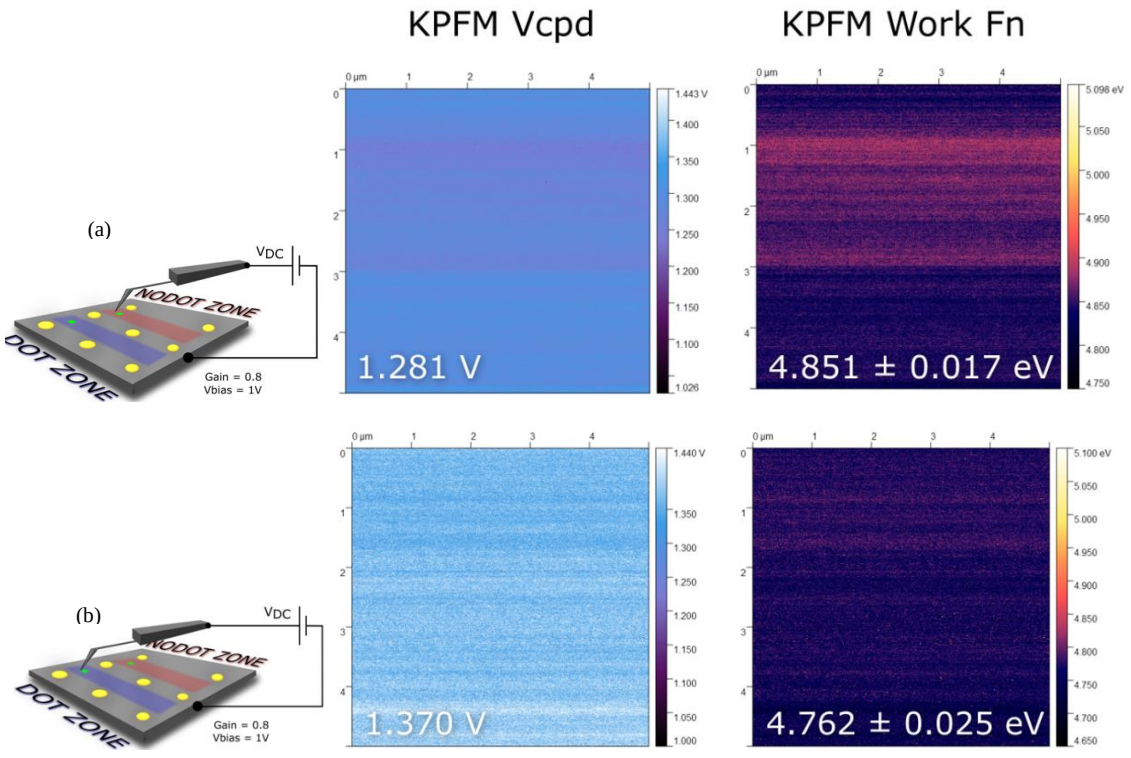


Figure 25. KPFM measurement CPD and work function for ALE sample (RF=50W). (a)Red zone, (b)Blue zone.

ALE 25 W sample: The next step was to scan the Si sample etched by ALE at 100 cycles and 25 W of RF power. Figure 26 shows the KPFM measurement of the etched sample where the mean work function has been calculated from the measured CPD of two areas marked blue and red on the schematic. The mean work function of the red zone is 4.321±0.013 eV and on the other side, the work function of the blue zone is 4.419±0.018 eV.

What can be concluded from CPD data is that both etched areas have slightly lower work function than the previous 50 W sample and lower by 0.4 eV than the theoretical value of 4.821 eV of the reference sample. The black dots in CPD data on Figure 26 refer to the measured potential of defects which could be surface contamination or structural damage. The contribution of areas with lower potential to the mean work function may explain the smaller work function values for both red and blue areas.

The most likely possibility of a decrease in the surface work function is a handling of the Si sample because the surface was not clean enough due to a glue substance used to adhere the mask on the top of the Si surfaces. Therefore, the dirt particle contributes to CPD measurements and shifts the work function of the sample toward a lower value. Also, the chamber is a multi-user tool that uses other gases that might contaminate the chamber from a previous process. In this case the contamination may affect the ALE process. Excluding the ALE process as a main reason for damage came from the fact that the same ALE conditions has been used with higher RF power in the previous 50 W sample and does not cause any damage.

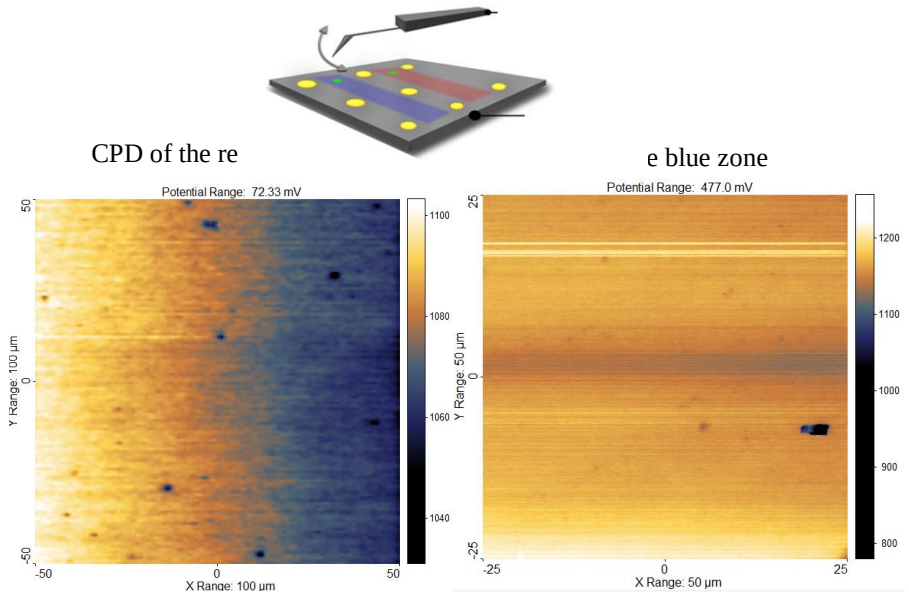


Figure 26. KPFM measurement CPD for ALE sample (RF=25W) of the red zone and blue zones.

ALE 15 W sample: The third scanned Si sample was the sample etched by ALE for 100 cycles and 15 W in RF power. Figure 27 shows the KPFM data of the CPD and the corresponding calculated work function of the two etched zones red and blue.

The CPD values of red and blue zones are 1.446 V and 1.338 V, respectively which correspond to work functions of 4.647±0.019 eV for red and 4.755±0.024 for blue zones. The CPD data of both etched zones looks very homogeneous which means that no contribution from contamination or defect can deviate the value of the work function to be close to the reference one. The work function of both etched zones is very close to the work function of the Si theoretical value which means that the ALE process does not cause any damage to the Si surface.

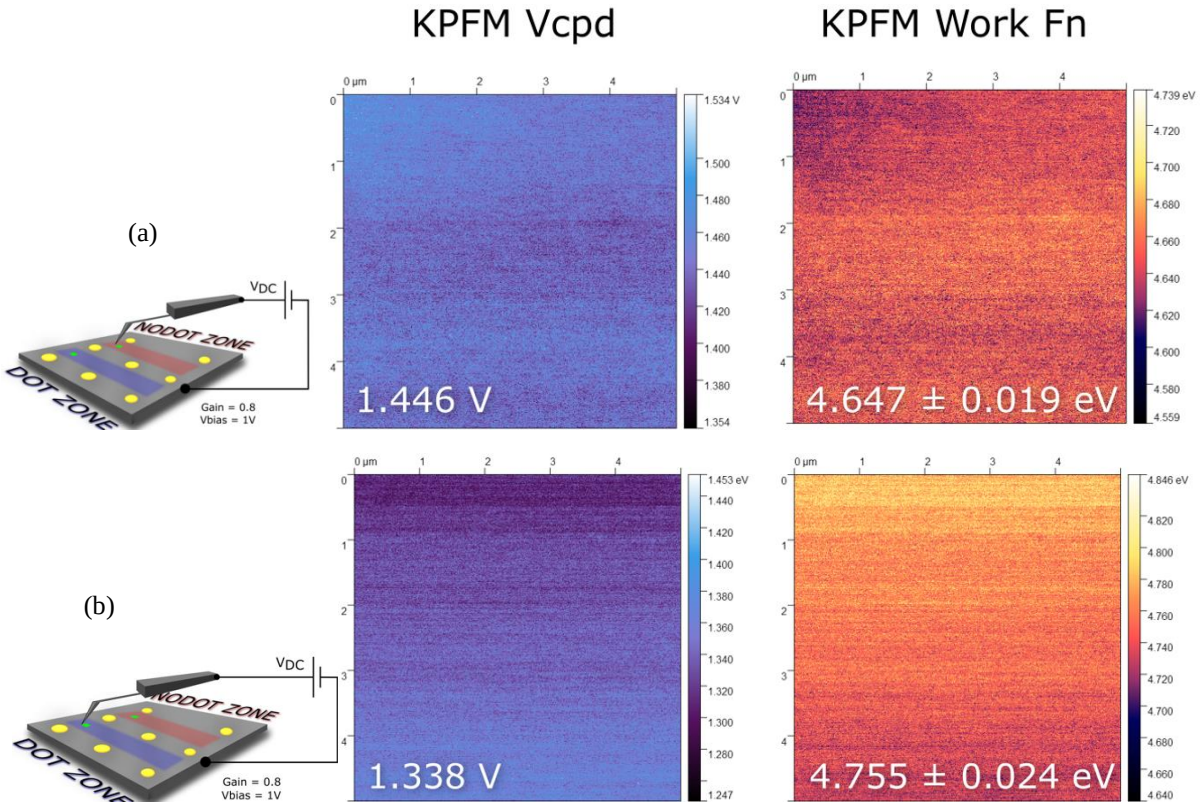


Figure 27. KPFM measurement CPD for ALE sample (RF=15W). (a) Red and (b) blue zone.

Figure 28 shows the CPD of ALE sample as a function of RF power. By comparing the results obtained from samples 50 and 15 W we conclude that ALE demonstrates smooth surface morphology and work function values higher comparing to RIE sample. Also, the energy of ions in the case of 50 W is higher than 15 W but both conditions result in very close CPD values. Thus, as long as the ion energy locating within the ALE window, the possibility of radiation damage is very low. What confirms the validity of these results is the values of work function that remain within the measured work function of Si (100). While the ALE 25 W etched sample demonstrates higher damage than the 15 and 50 W etched samples. Possibly due to the existing damage originating from the ALE process itself or contamination on the Si surface which decreases the ALE performance.

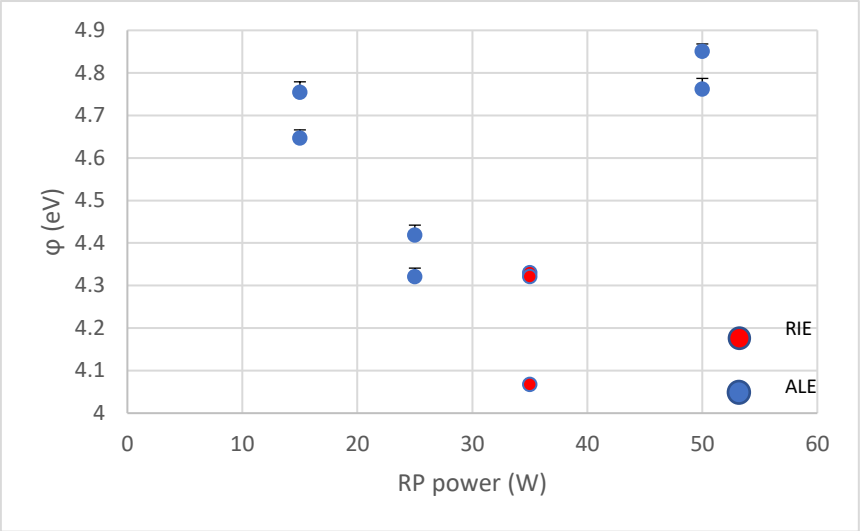


Figure 28. Surface work function ϕ as function of RF power. ALE (blue dots) and RIE (red dots) data points are plotted together.

AFM measurement of ALE etched sample: Figure 29 (blue dots) shows the roughness values of ALE and RIE etched samples as function of the RF power. The measured roughness of ALE with 15, 25 and 50 W RF-power are 0.1 nm, 0.55 nm and 0.09 nm, respectively. The lower surface roughness of 15 and 50 W samples is agreed with measured CPD and surface work function which was close to the reference value. On the other side the high surface roughness of the 25 W sample is in agreement with the measured CPD and surface work function that was lower than the reference value. Since the surface potential refers to electrical potential that exists at the surface of a material therefore, the surface roughness can have a significant effect on the surface potential of etched material. In the case of 25 W sample the surface contamination is considered as a surface roughness which lead to variations in the measured CPD. Therefore, when the tip is brought into contact with contaminated area which has different potential than the Si surface, the actual contact area can vary due to the irregularities, resulting in variations in CPD. As a result, the overall surface potential of the Si surface has been shifted from the reference value. On the contrary, in the case of 15 and 50 W the Si surface was almost flat and the roughness is very low and has no effect on the measured CPD. That means the ALE has less damage effect on the Si surface due to a cyclic process where the modification and etching step are separated.

Figure 29 (red dots) shows a roughness value for RIE process in three different places on the Si surface. The three red dots from the bottom to top indicates the RIE middle etched area, zone 2 and zone 1 respectively (see Figure 20). The measured roughness of zone 1 and 2 is 0.385 nm and 0.205 nm respectively which is higher than the roughness of RIE open area which is 0.175 nm. The higher roughness value of zone 1 is due to the incomplete etching process under the mask where some ions with high energy travel under the mask and sputtering the Si atoms. On the other side, zone 2 shows less roughness than zone 1 but still high enough to consider as a damage due to the shadowing effect of the mask edge where incomplete etching process is happen. Moving to the middle of RIE area, the roughness is much less than zone 1 and 2 but still higher than the roughness of ALE etched sample, 15 and 50 W, respectively. The higher roughness values of three RIE places is in agreement with the lower CPD values, and the corresponding work function compared to the reference Si value. The reason behind CPD value deviation is that the surface roughness leads to an increase in the effective surface area of the

Si surface. As a result, there are more surface sites available for adsorption or charge accumulation. This can result in shifting in surface potential, as more charges are accumulated on the rough surface compared to a smooth surface. Also, the surface roughness can provide additional sites for charge trapping, where charges can be localized or trapped due to irregularities or surface defects. These trapped charges can affect the surface potential, as they can modify the local electric field and alter the surface potential distribution.

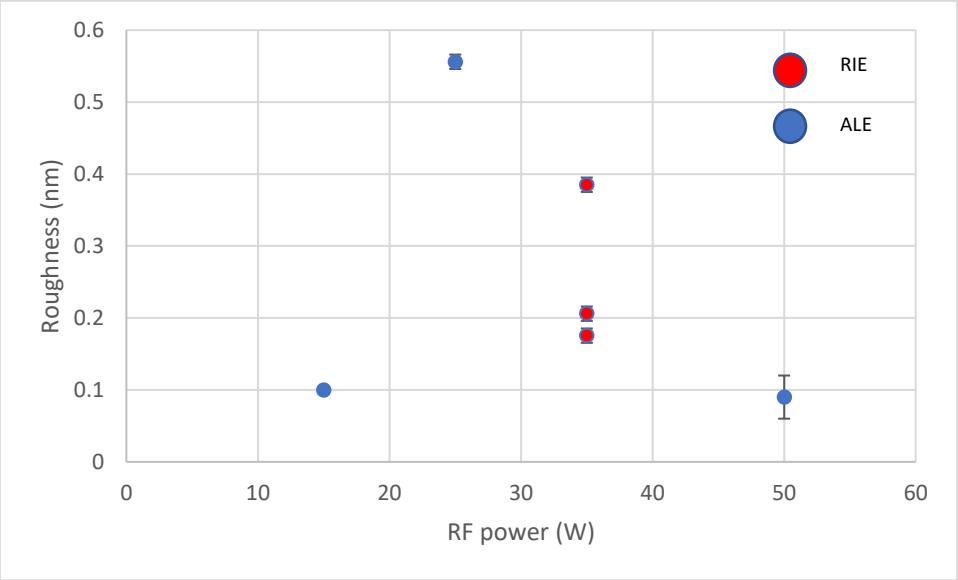


Figure 29. Surface roughness as function of RF power. ALE (blue dots) and RIE (red dots) data are plotter together.

Chapter 5

Conclusion

The damage formation in Si using RIE and ALE techniques has been investigated and a comparative study on the Si surface was successfully performed in this research project. KPFM and AFM characterisation methods have been used to evaluate the surface damage after the etching process by measuring CPD and roughness of the etched samples. The work function of the Reactive Ion Etching (RIE) sample was found to be lower in comparison to the pristine Si and Atomic Layer Etching (ALE) samples. This can be attributed to the Contact Potential Difference (CPD) values of the damaged surface, which cause a shift in the surface work function towards lower values. The damage inflicted during the RIE process alters the surface properties, resulting in a decreased work function compared to the original, undamaged Si and ALE samples While ALE samples showed very close values of CPD and work function to that of pristine Si indicating no or very small surface damage except the 25 W sample that had a contaminated surface which shifted the CPD to lower value. On the other side, a correlation between KPFM data and AFM measured roughness was observed since RIE sample had a higher roughness value compared to ALE samples. The results obtained show complete agreement with what was previously expected. Unfortunately, the observed limitation in this work was achieving the high etching depth by using ALE. The estimated etching depth in this project was about 8 nm after 100 cycles for 90 min and achieving deeper etching depth takes very long time.

To our best knowledge, this is the first time that the shadow mask has been used in damage comparison between ALE and RIE processes whereas in some works the mask is used for something else such as protecting the Si surface from UV light. Reviewing the results discussed in the RIE sample, one concludes that using a metal shadow mask for the pattern transfer process is limited due to the partially etched areas at the edge of the mask. All these findings have the potential to guide future investigation of damage formation by KPFM on ALE etched samples in different conditions than it used in this project. Moreover, in the future studies it might be possible to identify the type of damage depending on the value of CPD and work function of the sample surface. KPFM as a non-contact and non-destructive analyse method opens the door to characterize defects and impurities that affect the surface electronic structure of nanofabricated devices based on the ALE process and analyse new materials.

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