Flashlamp Annealing for Improved Ferroelectric Junctions

Theodor Blom
nat13tbl@student.lu.se

Department of Electrical and Information Technology
Lund University

Supervisor: Mattias Borg

Co-Supervisor: Rainer Timm

Examiner: Mathieu Gisselbrecht

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Abstract

The effects of flashlamp annealing (FLA) on the quality of ferroelectric $Hf_xZr_{1-x}O_2$ (HZO) interfaces, integrated on InAs substrates, are evaluated. For the integration of ferroelectric HZO on III-V semiconductors the crystallization via rapid thermal processing (RTP) can severely degrade the HZO/III-V interface. Thermal annealing in the millisecond duration were used in the efforts of reducing diffusion through the HZO film and increase device performance. Electrical characterization showed a lower defect density and improved endurance of the FLA samples compared to the RTP counterparts. The use of multiple low-energy flashes and pre-crystallization during ALD growth was also investigated for further improvement on device performance. Overall, this work provides valuable insight into low thermal budget integration of HZO on III-V semiconductors.

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Chapter 1

Introduction

The integration of electronic devices in our daily lives hardly goes unnoticed. Chances are that you are reading this very paper on an electronic device; either your phone, your computer or even your watch. To keep up with demand a lot of research is being conducted on designing faster, smaller and more energy efficient devices. A step in this direction is improving upon the basic building block of all devices, the transistor.

The transistor is the physical component which is toggled between ones (on) and zeroes (off) in order to store and process digital information. A common design of the transistor is the so called metal-oxide-semiconductor field-effect-transistor (MOSFET) where the application of a voltage to a metal gate electrode is used to control the current through the semiconductor channel of the transistor. This classic design has been steadily improved for decades but has in recent years reached a performance plateau primarily due to scaling difficulties [5].

As the MOSFET decreases in size, the effects of electron tunneling increase and eventually the difference in current between the on and off state becomes indistinguishable rendering the device useless. In 1971 it was theorized and proposed that one could develop a transistor which uses the tunneling characteristics of the electron as the source of the switching current. The concept was dubbed Ferroelectric Tunneling Junctions (FTJs) but was dismissed and forgotten as ferroelectric materials was not believed to work on smaller structures. From there the use of ferroelectric materials in transistor development was kept to a very small niche of specific applications where scalability of the devices were not an issue and can be found on the market today as FeRAMs and FeFETs with a junction length of $>100\,\mathrm{nm}$ [2, 6].

This was all changed in 2011 when Böscke et.al. published a paper revealing the successful creation of a 10 nm ferroelectric tunneling junction [7]. They used lightly doped hafnium oxide (HfO_2) which was crystallized to a ferroelectric phase. A truly remarkable discovery which reignited a lot of interest in ferroelectric materials for transistor design. Ferroelectric transistors have the advantage of being non-volatile which means they can be read without having to restore the state of the transistor (rewrite). This reduces the energy consumption dramatically

and could be a key factor in reducing the overall energy consumption of all digital devices. Additionally, the discovery of ferroelectric hafnium oxide is of great importance as HfO_2 already is a common material in modern transistor manufacturing. This allows for a simplified integration of ferroelectric transistors in current device designs [6].

Ferroelectric tunneling junctions using hafnium oxide has previously been demonstrated. In 2020 a 1 nm ferroelectric thin-film was integrated on Si and in 2021 a 10 nm junction was integrated on InAs [8, 9]. However, a common denominator of these devices is a limited endurance. A modern MOSFET should be able to perform at least 10^{12} cycles before degradation but FTJs of today are usually only cycled roughly 10^6 cycles before breakdown. This can be amended with techniques such as junction bilayers and reduced cycling voltage but one crucial limiting factor is the thermal stresses endured by the device in the crystallization process.

To reduce the thermal stresses one would need to minimize the time and temperature of the crystallization process, also known as the thermal budget. In 2018 it was demonstrated that it was possible to achieve similar performing FTJs using the fast crystallization technique of Flashlamp Annealing (FLA) to the commonly used crystallization technique of Rapid Thermal Processing (RTP) [10]. The reduction of the thermal budget on the devices is not only preferred for the performance of the individual transistor but also crucial for the successful integration into current device designs. Using nanosecond laser annealing, the integration of a FTJ in a production environment was demonstrated in 2020. Their devices showed significantly improved endurance over previous efforts [11].

These efforts show the capability of FTJs as integrated on Si and metal electrodes. Integration of FTJs on III-V semiconductors have not been studied in as much detail. Specifically, the integration of FTJs on InAs provide new challenges due to the diffusion and oxygen affinity of both In and As [12]. This paper demonstrates the improved performance of FTJs as integrated on InAs using the FLA technique compared to RTP.

Chapter 2

Ferroelectric Junctions

2.1 Ferroelectricity

Ferroelectric materials have the property of retaining an internal electric field even after an external electric field is removed [13]. The ferroelectric nature of the material is not uniform but rather comprised of many small-scale fields that can be aligned from an external source in order to propagate and strengthen the field throughout the material. In the case of ferroelectric materials the small-scale fields are referred to as domains where each domain has its own electric field strength and direction in 3D-space. The domains are separated by domain walls of varying thickness where the field is rapidly and repeatedly changing between the domain field directions. The domain boundaries can arise from electrical and thermal treatment of the samples but are mostly determined by the spontaneously oriented fields of the domains [14].

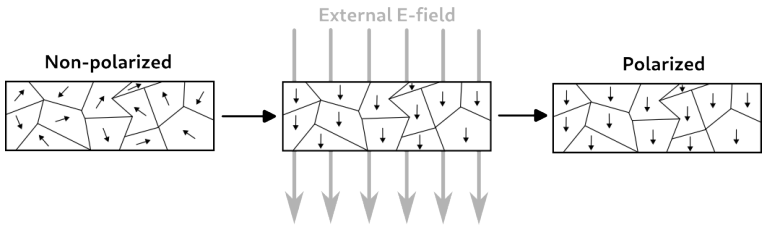


Figure 2.1: Schematic figure of the process of domain alignment to an external electric field. Initially the domains are spontaneously polarized to different polarization directions but with the application of an external electric field the domains are aligned and the ferroelectric material is polarized.

The amount of alignment between domains of a ferroelectric material is denoted its polarization and is often measured in $\mu C\,cm^{-2}$. As a ferroelectric material is created the spontaneously polarized domains are unaligned and the ferroelectric nature of the material is obscured. However, by applying an external electric field over the material the domains rotate to align with the external source. As the

external source is removed the aligned domains remain and hence also the built-in electric field. The polarization remaining after the removal of the external electric field is called the remnant polarization. The sequence of polarizing is illustrated in figure 2.1.

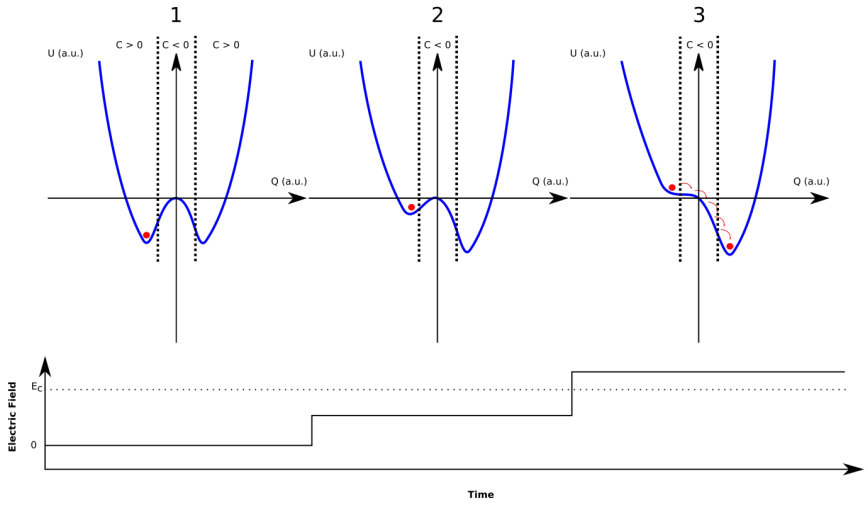


Figure 2.2: Energy landscape of a ferroelectric material through the polarization event. In the absence of an external electric field the polarization state is bound to its current trough. But with the application of a small electric field the potential between the barriers are lowered until the field if eventually greater than the coercive field E_c and the polarization of the material is switched. Figure taken from R. Athle [1].

The domains are typically not uniform and may require different external field strength in order to "wakeup" and align themselves with the external field. The required external field strength to polarize a ferroelectric sample is referred to as the coercive field and is often measured in $\mathrm{MV\,cm^{-1}}$. The quantitative definition of the coercive field is described in figure 2.3 but is commonly illustrated using the energy landscape as in figure 2.2. Here the polarization of the ferroelectric sample is in a binary system where the application of an external electric field allows for the polarization to "topple over" to the other polarization direction when the external electric field is stronger than the coercive field of the sample.

These two properties, remnant polarization (P_r) and coercive field (E_c), form the basis of how ferroelectric materials are characterized. These properties are best illustrated through a P-E curve which relates the polarization of a ferroelectric film with the electric field strength applied over the film. For a non-ferroelectric material the P-E curve would show a linear relationship between the two. However, for a ferroelectric material clear hysteresis is observed as the polarization remains with electric field strength approaching zero. An illustration of a P-E curve is

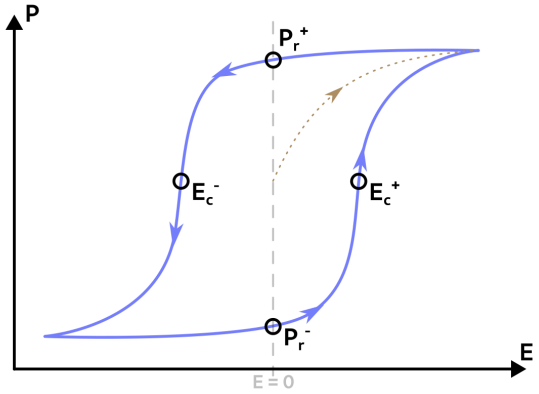


Figure 2.3: Schematic graph of a P-E curve showing the two properties of a ferroelectric material; the remnant polarization (P_r) and the coercive field (E_c).

shown in figure 2.3. The polarization is initially set to applying an external electric field (E) following the green dotted line. However, as the external field is reduced to zero the hysteresis of the ferroelectric material is revealed. Once polarized, the polarization remains without the influence of an external field (P_r^+). In order to switch the polarization, an opposite external electric field stronger than the coercive field of the material (E_c^-) must be applied. Removing the external field again shows that the polarization indeed has been switched. Important to note is that it is not possible to measure the absolute polarization of the ferroelectric materials, only the change of it as the polarization is measured through the current in the switching event.

2.1.1 $HfZrO_2$

Ferroelectric materials were first conceptualized in the 1950s along with the boom of the computing era. However, one quickly encountered integration and scalability issues with the ferroelectric materials of the time and the concept was soon forgotten to the well known MOSFET architecture [6]. In 2011 the field of ferroelectrics was revived with the discovery of ferroelectric hafnium oxide (HfO_2). Hafnium oxide was and is a commonly used oxide in integrated circuits today and could hence overcome the previous integration issues [7]. An intermediary orthorhombic phase (O) was theorized between the then known stable, non-ferroelectric amorphous (A) and monoclinic phases (M). The orthorhombic phase is non-centrosymmetric enabling the ferroelectric polarization behaviour to be retained by the material. With the addition of ZrO_2 of varying composition ranges the ferroelectric, orthorhombic phase of HfO_2 was more easily stabilized and was later proved to be scalable overcoming even the second hurdle 60 years prior [15, 8].

The orthorhombic phase of $Hf_{1-x}Zr_xO_2$ (HZO) is reached through annealing and is highly dependant on both film composition as well as time and temperature of the annealing step. The equal composition of $Hf_{0.5}Zr_{0.5}O_2$, where every other Hf

atom is replaced by Zr, is known to be the optimal choice for both stability and ferroelectric response [15]. A thorough investigation of the phase transformations of HZO in 2019 showed the transformation from the orthorhombic to the monoclinic phase requires a volume expansion. Capping the amorphous film before annealing is hence a big step in suppressing the $O \rightarrow M$ transformation [16]. Despite our best efforts, HZO grains of both the amorphous and monoclinic phases will most likely remain in the sample but maximizing the volume fraction of the orthorhombic phase is possible.

2.2 The FTJ Structure and Operation

The concept of the Ferroelectric Tunnel Junction (FTJ) was first proposed in 1971 but as the integration and scalability issues of ferroelectric materials of the time was not solved the concept was forgotten as thin films was essential for the functionality. The FTJ concept is based on using the polarization state to control the tunneling of electrons through the ferroelectric barrier. Because of the ferroelectric charges, the electrostatic potential of the barriers (Φ) is altered and is different depending on the polarization direction. Figure 2.4 shows a band diagram of a metal-insulator-metal (MIM) junction. Since the tunnel transmission depends exponentially on the square root of the barrier height, the current through the barrier will be dependant on the direction of the polarization [2].

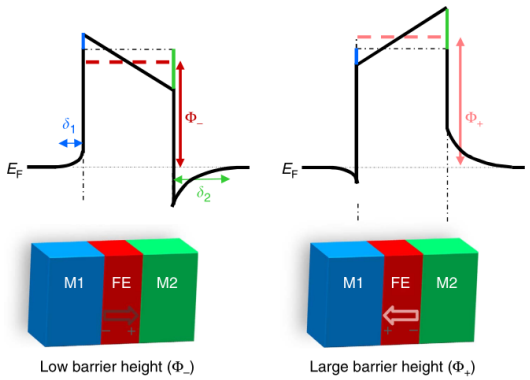


Figure 2.4: Band structure of a MIM FTJ. The asymmetry between the two electrodes allows for different electrostatic potential (Φ) depending on the polarization direction. The difference in potential allows for accurate control over the tunneling current through the barrier. Image taken from Garcia et.al. [2]

For the electrostatic potential to be different between the two polarization states the asymmetry between the two interfaces is essential. One way of introducing asymmetry is integrating the ferroelectric onto a semiconductor with a limited density of states. The use of ferroelectrics in integrated circuits is limited but the FTJ concept was proven to work in 2020 using 1 nm HZO integrated onto Si [8, 6]. However, FTJ devices are yet to prove sufficiently good to be considered for

practical applications and thus further research is required in improved annealing and integration on III-V semiconductors to fully realize their potential.

2.2.1 Leakage Mechanics and Defects

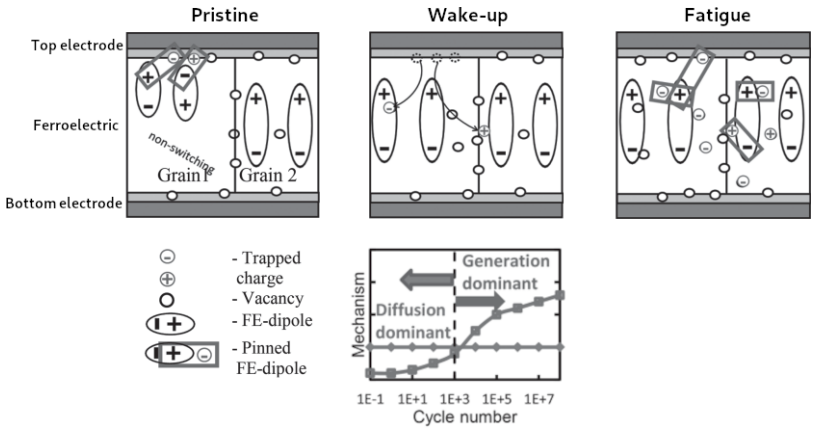


Figure 2.5: Illustration of the (de-)pinning behavior throughout cycling and how the dominant defect mechanism changes from diffusion to generation for the device to enter the fatigue cycling phase. Image adapted from Pesic et.al. [3]

A looming issue of the HZO-based ferroelectric tunnel junctions (FTJ) of today is the increase of leakage current through the device with continued polarization switching (cycling). This can be attributed to the generally higher coercive field of HZO which causes high electrical field stress on the devices, limiting endurance [6]. The high stresses of cycling causes charge injection into existing vacancies which can either facilitate or impede the ferroelectric response. This effect is known as depinning and pinning of the domains respectively. In the pristine state, some existing charge injected vacancies pin certain domains/grains from participating in the switching event. Initial cycling allows for the redistribution of these vacancies, depinning the domains and creating a more uniform field which allow for more domains to contribute to the polarization. This is known as the wake-up-phase. However, further cycling generates additional vacancies at the interfaces which screens the bulk of the ferroelectric and makes it more difficult to reach the coercive field of all domains. The generated vacancies can subsequently diffuse into the bulk trapping charges which pins the domains from participating in the switching. This is known as the fatigue phase of the ferroelectric. Further vacancy generation collects at the grain boundaries of the HZO significantly increasing the leakage current until breakdown of the device [3]. Figure 2.5 shows an illustration of the pinning and depinning of domains throughout cycling. Furthermore, a paper investigating the structural properties of the integration of ferroelectric HZO on InAs in 2016 showed the diffusion of both In and As atoms through the HZO layer during annealing which significantly affects performance of the device [12].

Both of these effects are induced by the diffusion of defects throughout the HZO.

Diffusion is both temperature and time dependant so reducing the time the sample is at an elevated temperature is paramount to reducing the effects of these defects. This is known as the thermal budget of the sample. A common fabrication technique of ferroelectric HZO is to crystallize the oxide in the order of minutes called Rapid Thermal Annealing (RTP). By using other techniques such as Flashlamp Annealing (FLA) or Pulsed-Laser Annealing (PLA) are known techniques for reducing the thermal budget the samples are exposed to [10, 11, 17].

Chapter 3

Fabrication

Metal-Ferroelectric-Semiconductor capacitors with are to be fabricated using traditional techniques. The MFS-caps were fabricated in a stack of InAs/HZO/TiN with an Au contact on top. All fabrication was done at Lund NanoLab (LNL) and is outlined in section 3.1. After fabrication the resulting capacitors have the parameters as stated in table 3.1 and look like the picture in figure 3.1.

Table 3.1: Relevant fabrication parameters of the samples. Growth and annealing parameters of each sample is stated in Chapter 5.

Layer	Thickness	Doping
Au	200 nm	-
TiN	10 nm	-
$HfZrO_2$	10 nm	1:1 (Hf/Zr)
InAs	280 µm	$1 \times 10^{16}\,\mathrm{cm}^{-3}$

Figure 3.1: Picture of fabricated capacitor rings. The numbering refers to the diameter of the inner capacitor circle in µm.

3.1 Sample Fabrication Process

3.1.1 InAs Wafer Preparation

The initial substrate was a low doped InAs 4 wafer with a layer of native oxides on top. Since the wafer is to be used as bottom contact of our capacitors a wet etch was required before any film deposition was possible. The wafer was etched in 10:1 HCl acid for 30 s and rinsed in deionized H_2O to remove any oxides. The samples were dried using a nitrogen gun and promptly advanced to the next step to reduce reoxidation. This process is schematically showed in figure 3.2. Before etching the wafers were cut into squares with a side length of roughly 10 mm to simplify processing.

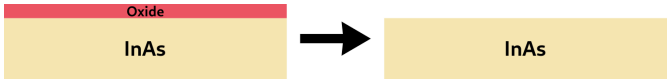


Figure 3.2: Schematic figure of the sample oxide etching process.

3.1.2 $HfZrO_2$ Deposition

With the native InAs oxides removed the deposition of $Hf_xZr_{1-x}O_2$ was done using atomic layer deposition (ALD) in a Picosun Sunale R-100 system. Samples were grown using alternating cycles (1:1) of TEMA(Hf) and TEMA(Zr) precursors to achieve equal distribution of Hf and Zr ($x = 0.5$) in the resulting ∼10 nm oxide. Depending on the sample series both chamber temperature and the number of cycles were altered. The specific growth parameters for each samples is specified in Appendix B. Figure 3.3 shows a schematic of the samples at this fabrication stage.

Figure 3.3: Schematic figure of the sample after atomic layer deposition.

3.1.3 Top Electrode Deposition

After deposition of the $HfZrO_2$ film, a ∼10 nm top contact of TiN was deposited through sputtering using an AJA Orion 5 sputter machine. Pumping the chamber to <2.7 mTorr and pre-cleaning the source for 5 min the samples were sputtered at a power of 150 W. Sputtering for ∼11 min at a deposition rate of 0.15 nm s^{-1} resulted in the desired layer thickness. Figure 3.4 shows a schematic of the samples at this stage of fabrication.

Figure 3.4: Schematic figure of the sample after top contact sputtering.

3.1.4 Annealing Process

With the amorphous oxide contained between the bottom- and the top contact annealing could take place. Depending on the sample annealing was either done through rapid thermal processing (RTP) or flash lamp annealing (FLA). The reference RTP sample were annealed at 600 °C for 30 s in a RTP-1200-100 system from UniTemp GmbH while all other samples were annealed in the FLA system by 5 ms pulses of varying energy and number. See figure 5.1 and Appendix B for a detailed overview of the number of flashes per sample and their energies. For the interested reader an in-depth review of the FLA technique is available through L. Rebohle et.al. [18].

3.1.5 Metal Contacting

In order to electrically characterize the samples, individual devices would have to be defined as well as covered in thicker highly conductive Au to not damage the underlying structure using the probe techniques described in Chapter 4. The devices were defined using optical lithography and the Au was deposited using electron-beam evaporation. Figure 3.5 shows a schematic of the samples at this stage of fabrication.

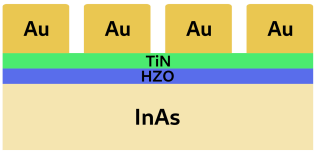


Figure 3.5: Schematic figure of the sample after device definition and Au deposition.

3.1.6 Etching of Top Contact

To further define the devices the TiN top contact was etched away in order to avoid short circuiting. Using a wet-etch in NH_4OH:H_2O_2:H_2O at the ratio of 1:2:5 at 60 °C the TiN was selectively etched away over a duration of 30 s. Maintaining

the samples still in the wet-etch hindered over-etching and ensured that there was no residue TiN short circuiting the capacitors. Figure 3.6 shows a schematic of the finished samples. See figure 3.1 for a picture of one of the samples.

Figure 3.6: Schematic figure of the sample after top contact etching. This is the finished sample.

To summarize the chapter a step by step schematic of the entire fabrication process can be seen in figure 3.7.

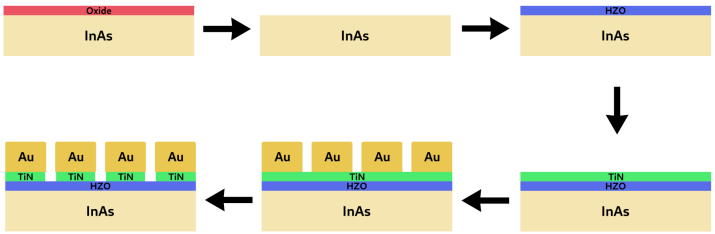


Figure 3.7: Schematic figure of the entire fabrication process.

3.2 Fabricated Sample Series

Table 3.2: Description of the fabricated samples in each series.

Series	Samples description
1	Five samples annealed with varied flash energy density from $15\,\mathrm{J\,cm^{-2}}$ to $32.5\,\mathrm{J\,cm^{-2}}$. Oxide is grown at an ALD chamber temperature of 200 °C. This series also contains one additional sample annealed with rapid thermal processing (RTP).
2	Four samples annealed with varied number of flashes from 1 to 8. All flashes have an energy density of $25\,\mathrm{J\,cm^{-2}}$. Oxide is grown at an ALD chamber temperature of 200 °C.
3	Three samples annealed with varied number of flashes from 2 to 8. All flashes have an energy density of $20\,\mathrm{J\,cm^{-2}}$. Oxide is grown at an ALD chamber temperature of 200 °C.
4	Three samples annealed with varied flash energy density from $20\,\mathrm{J\,cm^{-2}}$ to $30\,\mathrm{J\,cm^{-2}}$. Oxide is grown at an elevated ALD chamber temperature of 270 °C.
5	Three samples annealed with varied number of flashes from 1 to 4. All flashes have an energy density of $20\,\mathrm{J\,cm^{-2}}$. Oxide is grown at an elevated ALD chamber temperature of 270 °C.

Using the process described in section 3.1, five series of different samples were fabricated. Each sample in the series was annealed differently depending on the series and some series contain oxides grown at an elevated ALD chamber temperature. See table 3.2 for a summary of each series. See Appendix B for detailed processing conditions for each sample. Each fabricated sample has multiple ferroelectric capacitors (devices) as shown in figure 3.1.

Chapter 4

Electrical Characterization

To characterize the fabricated samples three different techniques were used; Positive-Up-Negative-Down (PUND), endurance pulsing and a Capacitance-Voltage scheme to quantitatively estimate the defect density of ferroelectric films integrated on semiconductors. [4] All characterization was done at the Department of Electrical and Information Technology at Lund University. The equipment used is only able to probe the devices from the top electrodes. To access the InAs substrate (bottom electrode) a short-circuit was created by breaking the oxide of one device and use that device as ground while probing other devices with intact oxides. This way we know there is no potential difference between the InAs substrate and the probing electrode with a broken oxide.

4.1 PUND and Endurance

The PUND and endurance measurements of the samples were done simultaneously by endurance pulsing up to 10^4 cycles before conducting the PUND measurements to later continue the endurance pulsing until breakdown of the sample. The two methods are described individually in the following two sections. Both methods werre performed using a Keysight B1500A parameter analyser equipped with a B1530A waveform generator.

4.1.1 PUND

The Positive-Up-Negative-Down (PUND) method is used to quantitatively measure the remnant polarization (P_r) and the coercive field (E_c) of a ferroelectric device. These properties of ferroelectric films are explained in Section 2.1. The main goal of the technique is to remove the influence of leakage current in the total current in order to determine the amount of polarization current in the switching event.

Figure 4.1 illustrates the applied voltage and the current response of the ferroelectric device. Four voltage spikes in the shape of up-up-down-down are applied over the film. The first spike polarizes the film towards the positive and gives a current

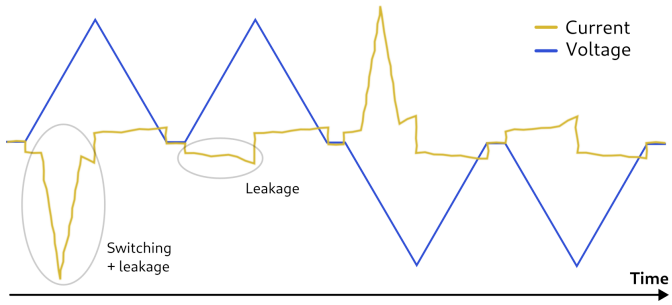


Figure 4.1: Schematic figure of a PUND measurement. The two consecutive voltage spikes only causes a ferroelectric switching event during the first spike which allows for the removal of the leakage current from the total current through integration.

response containing both the polarization current as well as any leakage current. Since the polarization field is already positive for the second spike only the leakage current is measured. By removing the response of the second spike from the first one can isolate the polarization current in the switching event. Repeating the same idea for the negative-down pulses gives us the full name; Positive-Up-Negative-Down.

Isolating the polarization current allows for better visualization of the ferroelectric properties through the P-E curve described in Section 2.1. To achieve a graph as illustrated in Figure 2.3, the applied voltage is scaled with the film thickness to achieve a unit of electric field in $\mathrm{MV\,cm^{-1}}$ and the polarization current is time-integrated to obtain the accumulated polarization charge at each electric field strength and scaled to the area of the device resulting in a unit of $\mu\mathrm{C\,cm^{-2}}$. From these data the remnant polarization (P_r) and coercive field (E_c) of each device is extracted.

4.1.2 Endurance

The endurance of a device is a measurement of how many cycles the device can endure before polarization switching no longer can be measured. Polarization switching induces more leakage through the device which eventually causes breakdown as described in section 2.2.1. By applying a voltage in a sawtooth pattern over the ferroelectric film the device is rapidly switched between the two polarization directions. Throughout cycling the electrical response of the device is observed and cycling is stopped when breakdown occurs. The number of cycles before breakdown is noted and assigned as the endurance of the device.

4.2 Capacitance-Voltage

Capacitance-Voltage (CV) measurements can be used to measure a multitude of different properties. In this paper a specific CV measurement schema described

by A. E. Persson et.al. in 2020 was used to quantitatively estimate the amount of defects in the ferroelectric films. [4] The method is based on the hysteresis of the CV curves induced by defects before the coercive field is reached and the hysteresis is exaggerated by the switching current. When the voltage on the device is swept up and down the band structure across the film changes as illustrated in Figure 4.2a and b respectively. Sweeping towards the positive allows for electrons to flow from the InAs substrate into the oxide leading to a negative charge buildup at the defect states of the oxide while the opposite is true for a bias sweep towards the negative. This effect creates a shift of the bias voltage in the CV measurement as shown by Figure 4.2c. By Gauss' law, the voltage shift ΔV_{th} and the charge density $Q_t q$ can be related by equation 4.1 where C_{ox} is the oxide capacitance density, d is the oxide thickness and $\rho(x)$ is the defect charge density. For each measured device, C_{ox} is scaled to the area of the top electrode as seen in figure 3.1.

$$\Delta V_{th} = -\frac{1}{C_{ox} d} \int_0^d x\rho(x)\, \mathrm{d}x \Longrightarrow Q_t = \frac{\Delta V_{th} C_{ox}}{q} \tag{4.1}$$

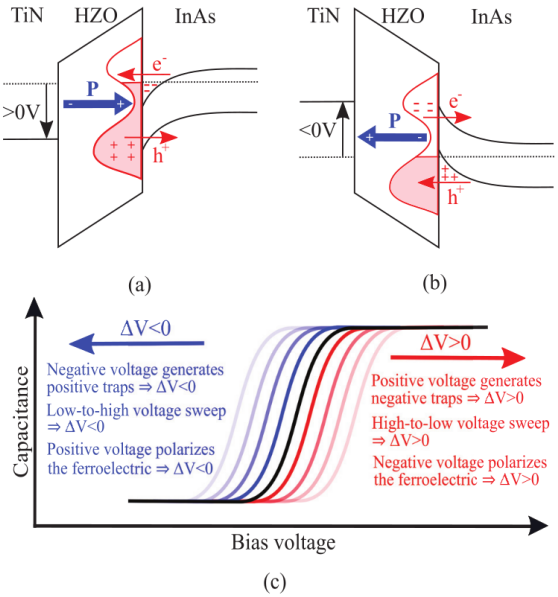


Figure 4.2: The used CV method is based on charge trapping in the voltage sweeps. Figure a and b shows negative and positive charge buildup at the defect states in the oxide at a positive and negative voltage sweep respectively. The charge buildup in each case shifts the bias voltage towards the negative and positive respectively as described in figure c. The figure is borrowed from A. E. Persson et.al. [4]

Equation 4.1 allows for a quantization of the amount of detected traps in the oxide Q_t depending on the voltage shift ΔV_{th} between the up and down voltage sweep. Figure 4.3 illustrates the measurement schema used to obtain ΔV_{th} and C_{ox} for each device to calculate the defect density Q_t. Our measurements were performed using a Agilent 4294A Impedence Analyser at a temperature of 13 K and a oscillation frequency and AC amplitude of 1 MHz and 50 mV respectively.

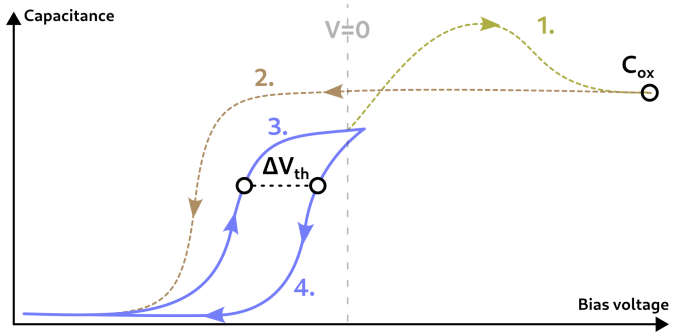


Figure 4.3: Schematic illustration of the CV measurement schema with the desired values of C_{ox} and ΔV_{th} clearly labeled. The schema is divided into 4 separate sweeps done in series where the device is initially polarized with a positive sweep to the maximum bias voltage (1) in order to find C_{ox} followed by a negative sweep to polarize the device the opposite direction (2). To find ΔV_{th} two consecutive sweeps in opposite directions are done (3 and 4). A target voltage above $V = 0$ but well below the coercive field is selected to induce the charge buildup without triggering the switching event. With these parameters measured one can calculate the defect density using equation 4.1.

Chapter 5

Results and Analysis

5.1 Flashlamp Energy Density and Film Temperature

Crystallization of the hafnia films using the flash lamp annealing (FLA) technique does not immediately reveal the temperature achieved in the films. Due to the short time frames and the geometry of the FLA setup, one must simulate the achieved temperature in the film from the structure of the samples and the flash parameters. Flash duration and preheating temperature were set to 5 ms and 250 °C respectively in order to be below the critical crystallization temperature before the FLA flash [16]. Other simulation parameters are tabulated in table A.1 and produce figure 5.1 showing the resulting back and front peak temperature for different pulse energies. The figure also includes pyrometer measurements of the back temperature during annealing (green). The discrepancies on the order of 20 K between simulated back peak temperature (black) and the measured values are attributed to a lower reflectivity of the TiN capping layer compared to the ideal values of the simulation. Therefore, the model is deemed to be in reasonable agreement with the experimental data and gives an estimate of the achieved surface peak temperature.

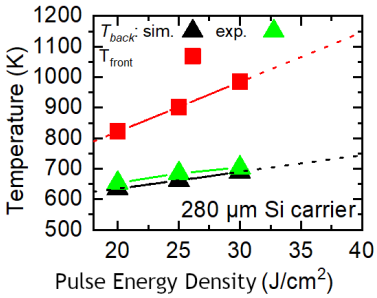


Figure 5.1: Simulated back and front peak temperatures of our samples using the simulation parameters tabulated in A.1. Pyrometer measurements of the back temperature measured during annealing (green) confirm the accuracy of these simulations.

Figure 5.1 reveal a linear relationship between the pulse energy density (E_{pulse}) and the peak HZO film temperature (T_{peak}) for our sample and FLA parameters (eq A.1). This gives a more convenient reference going forward using the achieved film temperature rather than the pulse energy density when describing different samples. The usually reported crystallization temperature required to form the ferroelectric orthorhombic phase of HZO is in the range of 400-600 °C [15, 19]. The simulated peak surface temperatures in the 20-30 J cm^{-2} pulse energy range are significantly above this critical temperature and should therefore yield a sufficiently high peak temperature to achieve ferroelectric properties in the HZO.

5.2 Sample Specifications and Characterization

As a reference point, a sample was processed using rapid thermal processing (RTP) as the annealing method in parallel to other FLA samples. This sample proves as a point of comparison for the characterization of the FLA samples throughout the work. The RTP sample was annealed at a temperature of 600 °C for 30 seconds. The electrical characterization of this sample, as described in Chapter 4, was measured and tabulated in table 5.1. Measurements were done on approximately 10-15 devices per sample to show statistical significance. The remnant polarization and coercive field are measured after a wakeup of 10^4 cycles at a pulsing voltage of 3 V.

Table 5.1: Electrical characteristics for the RTP reference sample over 10-15 devices.

PUND, Endurance and Defect Density			
Remnant Polarization	P_r	29.03 ± 0.21	µC cm^{-2}
Coercive Field	E_c	1.23 ± 0.18	MV cm^{-1}
Endurance		23 ± 11	10^3 cycles
Defect Density	D_d	9.7 ± 0.6	10^{12} cm^{-2}

The processing of the FLA samples are outlined in Section 3.1 and the different sample series are outlined in table 3.2. For the first FLA series, hereby denoted series 1, the flash energy density was varied between 15-32.5 J cm^{-2} to reach different peak temperatures in the film. The film deposition and annealing conditions for these samples are summarized in table B.1.

Resulting electrical characterization from series 1 are shown in figure 5.2. As seen in figure 5.2a and 5.2b the PUND characteristics show ferroelectric behaviour with a strong dependence on peak film temperature. The onset of ferroelectricity for these flashlamp annealed samples seem to be at a flash energy density between 20-25 J cm^{-2} (peak temperature between 550-630 °C). Therefore samples annealed with an energy density less than 25 J cm^{-2} are omitted from some of the figures. The remnant polarization and the coercive fields of the samples in this series follow a similar pattern reaching a peak of 20.12 ± 0.59 µC cm^{-2} and a minimum of 1.46 ± 0.14 MV cm^{-1} respectively at a flash energy density of 30 J cm^{-2} (peak annealing

temperature of 711 °C). Higher temperature annealing shows a degradation of these ferroelectric properties. The degradation could be the effect of multiple factors such as thermal damage to the contacts or further crystallization to the non-ferroelectric monoclinic phase but further studies are needed to confirm this hypothesis.

Figures 5.2a and 5.2b shows that the described experimental process in Chapter 3 is indeed a valid process for fabricating ferroelectric capacitors of this caliber with comparable remnant polarization and coercive fields to that of samples annealed through RTP.

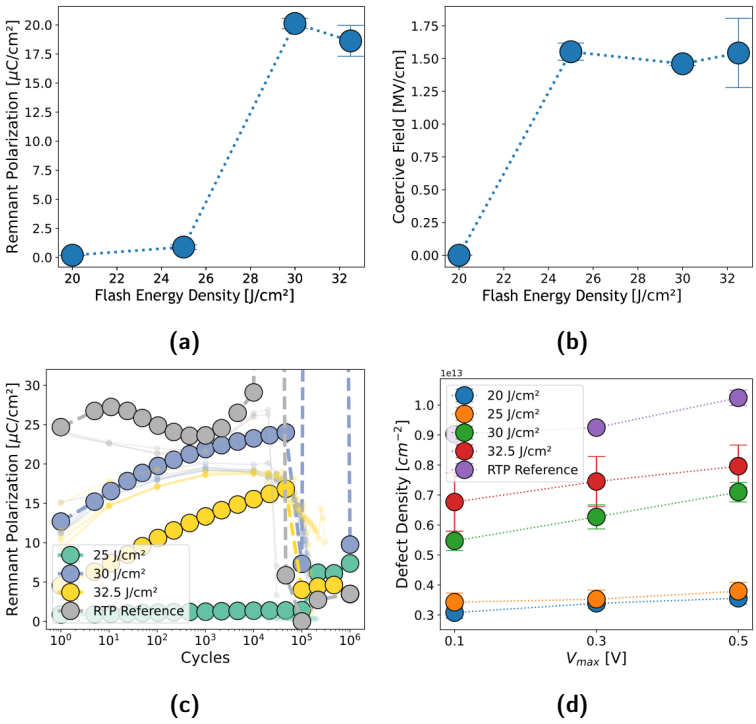


Figure 5.2: Plotted data from series 1. Figures a and b show the ferroelectric response of the samples at varying peak annealing temperature indicating comparable ferroelectric response to the RTP annealed sample presented in table 5.1. Figure c show improved endurance of one highlighted device for each sample. See table 5.2 for an aggregated value for multiple devices. Figure d show reduced defect density for all samples annealed through FLA compared to the RTP sample.

Furthermore, figure 5.2c show an increased endurance for all samples in series 1 compared to the RTP reference. The figure highlight one device from each sample but an aggregate value can be found in table 5.2. The most comparable sample flashed with $30\,\mathrm{J\,cm^{-2}}$ had an endurance roughly 6 times greater at values in the

range $(127 \pm 13)\ \cdot 10^3$ cycles. The barely ferroelectric sample flashed at $25\,\mathrm{J\,cm^{-2}}$ did not breakdown before the measurements ended at $200\ \cdot 10^3$ cycles and the endurance of these capacitors should be investigated further to reach a conclusion for their viability for use in certain gate stacks [13]. Similarly to P_r and E_c, annealing at a higher peak temperature results in degraded endurance to a value of $(82 \pm 46)\ \cdot 10^3$ cycles. These values however are still an improvement compared to the RTP sample.

The improved endurance could be a result of the reduced defect density of the flashlamp annealed films as shown in figure 5.2d using the method described in section 4.2. The measurements reveal a defect reduction of up to a factor of 3 for samples with a low ferroelectric response and close to a factor of 2 for samples showing comparable P_r and E_c to the RTP sample. This is likely due to the reduced thermal budget for the FLA samples which generates less initial defects during the annealing step. However, after sufficiently many cycles the generated defects (vacancies) start to collect at the HZO grain boundaries increasing the leakage through the oxide and causes the breakdown. However, the data studied here is not enough to rigorously conclude this hypothesis [3, 19]. See table 5.2 for a summary of the attained values for the sample annealed at a flash energy density of $30\,\mathrm{J\,cm^{-2}}$ (peak annealing temperature of 711 °C).

Table 5.2: Electrical characteristics for the sample annealed at $30\,\mathrm{J\,cm^{-2}}$ in series 1. The data is measured from 10-15 devices on the sample. See table B.1 for detailed processing conditions.

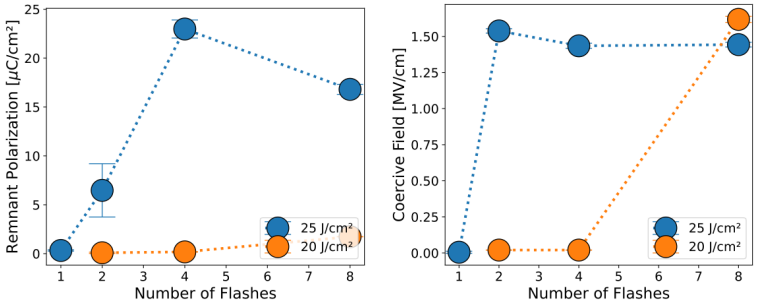
PUND, Endurance and Defect Density			
Remnant Polarization	P_r	20.12 ± 0.59	$\mu\mathrm{C\,cm^{-2}}$
Coercive Field	E_c	1.46 ± 0.14	$\mathrm{MV\,cm^{-1}}$
Endurance		127 ± 13	10^3 cycles
Defect Density	D_d	6.1 ± 0.7	$10^{12}\ \mathrm{cm^{-2}}$

Although series 1 resulted in improved endurance and lower defect density along with comparable PUND data to the RTP samples, the peak annealing temperature is still to high in order to significantly reduce the amount of defects in the film. A closer look at figure 5.2d and the barely ferroelectric sample annealed at a flash energy density of $25\,\mathrm{J\,cm^{-2}}$ reveal a further reduction of the defect density at the cost of ferroelectric response (figure 5.2a). Maintaining that low peak annealing temperature over multiple flashes could result in improved PUND data while not inducing additional defects.

For series 2 and 3 the number of flashes were varied up to a maximum of 8 flashes for two different flash energy densities, $25\,\mathrm{J\,cm^{-2}}$ and $20\,\mathrm{J\,cm^{-2}}$ respectively. See table B.2 and B.3 for detailed processing conditions. The flashes were manually timed at an interval of approximately 200 s.

Resulting electrical characteristics of series 2 and 3 are shown in figures 5.3 and 5.4. Figure 5.3a reveal an increased ferroelectric response with additional flashes up to a maximum of $22.98 \pm 1.02\ \mu\mathrm{C\,cm^{-2}}$ for series 2. Series 3 on the other hand,

annealed with a peak temperature of 550 °C, is not annealed to a significantly high peak temperature to achieve ferroelectricity until 8 flashes; but even then not to a significant degree. Series 2 show a similar degradation of the ferroelectric response when flashing up to 8 times as with the increased flash energy density in figure 5.2a where again further studies are needed to confirm its causes. The achieved coercive field as shown in figure 5.3b is comparable with both series 1 and the RTP sample.



(a) **(b)**

Figure 5.3: Plotted PUND data from series 2 and 3 ($25\,\mathrm{J\,cm^{-2}}$ and $20\,\mathrm{J\,cm^{-2}}$ respectively). Figure a and b show the evolution of the remnant polarization and the coercive field respectively over varying number of flashes for the two different flash energy densities. Increasing the number of flashes with reduced peak annealing temperature compared to series 1 results in comparable ferroelectric response to the RTP sample as tabulated in table 5.1.

Similarly to series 1, figure 5.4 show increased endurance as well as a lower defect density compared to the RTP sample. The sample flashed 4 times with an energy density of $25\,\mathrm{J\,cm^{-2}}$ (peak annealing temperature of 630 °C) which has the most similar ferroelectric response to the RTP sample had an endurance in the range $(53 \pm 11) \cdot 10^3$ cycles; an improvement of a factor of 2. Other samples in the same series showed longer endurances but at the cost of remnant polarization. More interestingly, the defect density of series 2 shown in figure 5.4b does increase with multiple flashes reaching a saturated value at 4 flashes and beyond. This gives indication for the peak annealing temperature of 630 °C still being too high in order to avoid the diffusion of defects in the sample. After 4 flashes the defect density reaches a saturated value where additional flashes only affects the already generated defects and assists in the pinning of the domains lowering P_r as shown in figure 5.3a.

Series 3, annealed with an energy density of $20\,\mathrm{J\,cm^{-2}}$ (peak temperature of 550 °C), does not give any ferroelectric response until the 8th flash as shown in figure 5.3a. This is likely due to the low total thermal impact of the 5 ms pulses at this peak annealing temperature. However, as indicated by figure 5.4d, the defect density of these samples also increase with additional flashes, reaching approxi-

mately the same value as for series 2 but showing a significantly lower ferroelectric response. This implies the total energy deposited in the samples during flashing is enough to induce additional defects but barely enough to crystallize the HZO to the orthorhombic phase. See table 5.3 for a summary of the attained values for the sample flashed 4 times at an energy density of $25\,\mathrm{J\,cm^{-2}}$ (peak annealing temperature of 630 °C) of series 2.

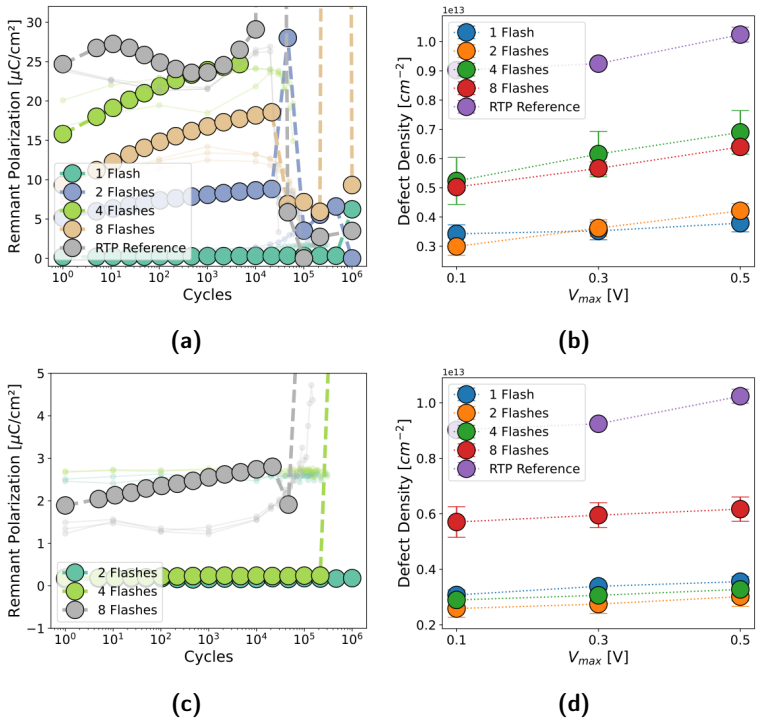


Figure 5.4: Plotted endurance and defect density from series 2 and 3. Figures a and b show the data from series 2 while figures c and d show the data from series 3. Figures a and c show the endurance of all devices of the sample with one device highlighted. See table 5.3 for an aggregated value for multiple devices. Increasing the number of flashes with reduced peak annealing temperature affects the defect density up to a point where additional flashes only assists in pinning the ferroelectric domains. The measured endurance of these samples are greater compared to the RTP samples.

Series 1 through 3 show only slight performance improvements to the RTP samples due to the flash energy density being to high to facilitate additional crystallization before inducing other effects or the time required for multiple flashes attributing to an increased defect density without further crystallization. Both these effects contribute to increased domain pinning and eventually the breakdown of the individual capacitors. In an effort to minimize the energy needed during annealing, the

Table 5.3: Electrical characteristics for the sample flashed 4 times at an energy density of $25\,\mathrm{J\,cm^{-2}}$ in series 2. The data is measured from 10-15 devices on the sample. See table B.2 for processing conditions.

PUND, Endurance and Defect Density			
Remnant Polarization	P_r	22.98 ± 1.02	$\mu\mathrm{C\,cm^{-2}}$
Coercive Field	E_c	1.44 ± 0.36	$\mathrm{MV\,cm^{-1}}$
Endurance		53 ± 11	10^3 cycles
Defect Density	D_d	5.9 ± 1.1	$10^{12}\ \mathrm{cm^{-2}}$

ALD temperature could be increased to potentially pre-crystallize the HZO during growth, hopefully resulting in a lower thermal budget needed in the annealing step.

For series 4 and 5 the growth temperature during ALD was increased from 200 °C to 270 °C. The HZO growth per cycle at this elevated temperature is reduced by roughly 20 % in our equipment. To compensate for the lower growth per cycle the amount of cycles was increased to 60:60 to maintain the same HZO thickness as previous samples.

The plotted data from series 4 is shown in figure 5.5. The increased growth temperature does indeed reduce the peak annealing temperature required to reach the onset of ferroelectricity as shown in figure 5.5a. With the increased growth temperature the window in which a significant ferroelectric response is achieved is widened and a reduced coercive field is noted in figure 5.5b. However, with our selected flash energy densities it is not clear whether we have surpassed or yet to have reached the saturation point as noted at a growth temperature of 200 °C. It would be interesting to increase the flash energy density above $30\,\mathrm{J\,cm^{-2}}$ to see the effects of a higher peak temperature anneal on the ferroelectric response.

The endurance of these samples show similar improvement as earlier FLA treated samples, as seen in figure 5.5c. With improvements up to a factor of five with comparable P_r while samples without significant ferroelectric response do not reach breakdown $\leq 300 \cdot 10^3$ cycles. The increased endurance shows in figure 5.5d as well through the reduced defect density of these samples. Interestingly, for these samples an overall increase in defect density is seen even for samples which do not show any ferroelectric response. Increasing the peak annealing temperature seem to have a reduced impact on defect generation and is ultimately comparable with previous FLA treated samples at a flash energy density of $30\,\mathrm{J\,cm^{-2}}$ (peak annealing temperature of 711 °C). This revelation seem to show that the defect generation is energy dependant and that defects that would be generated by the one $30\,\mathrm{J\,cm^{-2}}$ are being generated during growth instead. With many defects already generated during growth, the peak annealing temperature is not high enough to induce additional defects. See table 5.4 for a summary of the measured values.

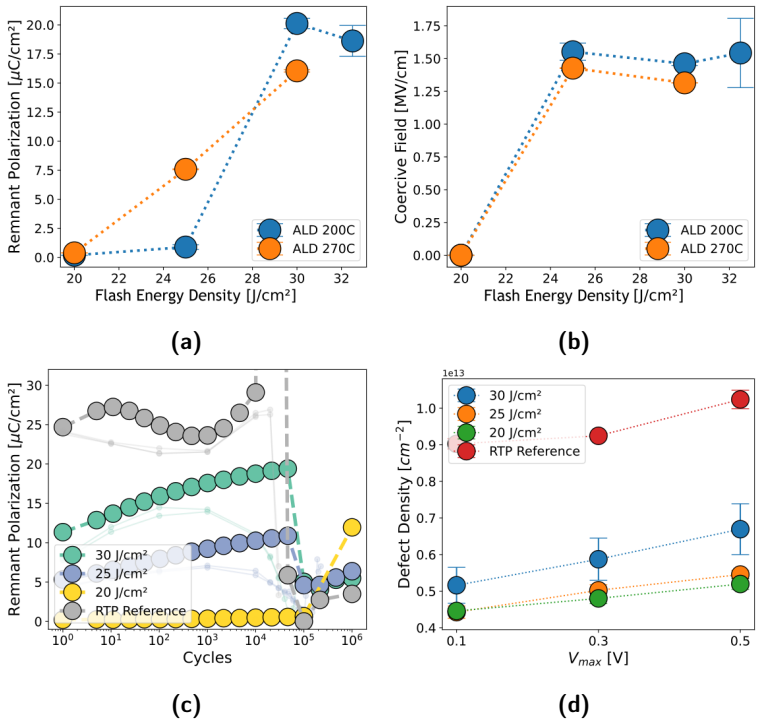


Figure 5.5: Plotted data from series 1 and 4 (ALD chamber temperature of $200\,^{\circ}\mathrm{C}$ and $270\,^{\circ}\mathrm{C}$ respectively). Figures a and b show the ferroelectric response of samples grown at different ALD temperatures for varying peak annealing temperatures indicating that increasing growth temperature assists in lowering the required temperature to reach the onset of ferroelectricity. Figures c and d show only data from series 4. Figure c show the endurance of all devices of the samples with one device highlighted per sample. See table 5.4 for an aggregated value for multiple devices showing improved endurance compared to the RTP sample. Figure d shows an overall increase in defect density for samples grown at elevated temperature but also a reduced impact of the annealing step on defect generation.

Table 5.4: Electrical characteristics for the sample annealed at $30\,\mathrm{J\,cm^{-2}}$ with oxide grown at a chamber temperature of $270\,^{\circ}\mathrm{C}$ in series 4. The data is measured from 10-15 devices on the sample. See table B.4 for processing conditions.

PUND, Endurance and Defect Density			
Remnant Polarization	P_r	16.05 ± 0.63	$\mu\mathrm{C\,cm^{-2}}$
Coercive Field	E_c	1.32 ± 0.13	$\mathrm{MV\,cm^{-1}}$
Endurance		50 ± 28	10^3 cycles
Defect Density	D_d	5.8 ± 0.7	$10^{12}\ \mathrm{cm^{-2}}$

Series 4 showed that increasing growth temperature assisted in lowering the required peak annealing temperature to reach the onset of ferroelectricity in addition to a reduced impact on defect generation during annealing. However, to reach significant values of remnant polarization a high peak annealing temperature is still required. Using the knowledge from series 2 and 3 it might be possible to reduce the impact of annealing on defect generation even further.

The plotted data from series 5 is shown in figure 5.6. The peak annealing temperature for these samples are $548\,^{\circ}\mathrm{C}$ in the attempt to incrementally reach the onset of ferroelectricity with additional flashes. Figures 5.6a and 5.6b show P_r and E_c respectively and reveal that the flash energy density of $20\,\mathrm{J\,cm^{-2}}$ (peak annealing temperature of $548\,^{\circ}\mathrm{C}$) is not sufficient to reach the onset of ferroelectricity for up to 4 flashes. Although some response is measured for all samples, this is attributed to the noisiness of non-ferroelectric samples. Since the samples are not ferroelectric, the endurance in figure 5.6c show only an increasing remnant polarization response due to increased leakage current during cycling. Figure 5.6d show the same elevated defect density as in figure 5.5d which stay consistent throughout annealing.

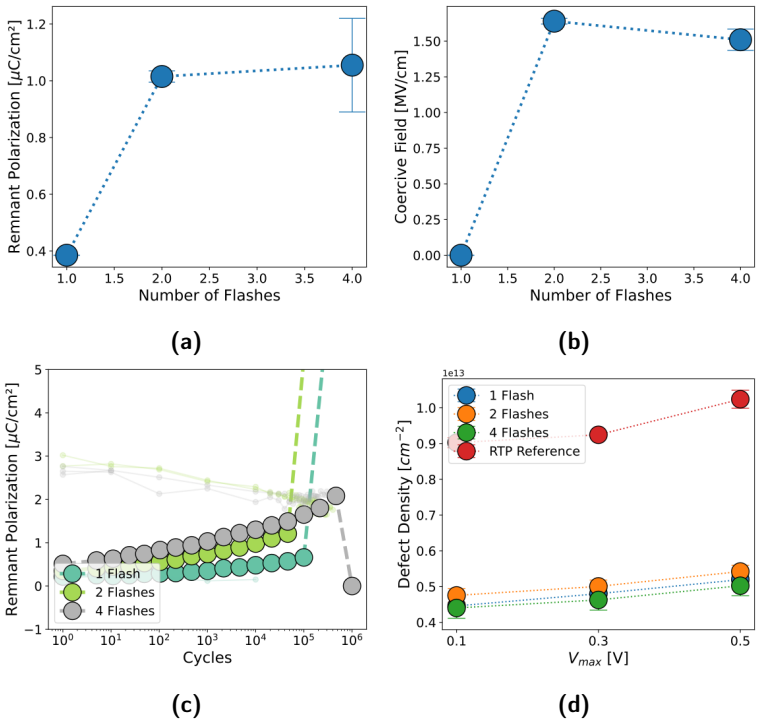


Figure 5.6: Plotted data from series 5. Figures a and b show the ferroelectric response of the samples annealed at a peak annealing temperature of $548\,^{\circ}\mathrm{C}$ over varying number of flashes. The figures reveal that the temperature is not high enough to reach the onset of ferroelectricity despite having been grown at an elevated ALD temperature. Figure c show the endurance of all devices of the samples with one device highlighted per sample. But due to the low ferroelectric response the readout is only affected by the increasing leakage current during cycling. Figure d affirms the higher defect density of samples grown at the elevated growth temperature and shown no effect on defect generation throughout the annealing steps.

Chapter 6

Conclussion

This report shows successful integration of ferroelectric HZO into a InAs/HZO/TiN stack using a flash lamp annealing (FLA) technique. The resulting capacitors show comparable ferroelectric response with capacitors annealed through rapid thermal processing (RTP) with an improved endurance up to a factor 5. The improved endurance is attributed to the reduced defect density of the films processed using FLA. This in part due to the reduced thermal budget of the FLA technique which reduces the diffusion of oxygen vacancies as well as the formation of As and In oxides from the substrate [12]. The reduced defect density allows for additional endurance cycling before breakdown of the ferroelectric capacitor.

In our efforts of further reducing the defect density, both multiple flashes at a lower peak annealing temperature and pre-crystallization during growth was examined. However, these efforts showed varied success. Additional flashes showed only marginal improvements up to the amount of flashes tested during these experiments. Using a flash lamp annealer which can produce multiple flashes at a higher repetition rate could prove fruitful. Pre-crystallization of the HZO during growth showed marginal success in lowering the required peak annealing temperature to reach the onset of ferroelectricity but did in itself prove detrimental to the defect density of the samples.

In order to better understand the material effects of these efforts this data could be combined with studies of the oxide bulk and surface to identify defects and their properties. In a complementary study by R. Athle et al the data from this study is combined with XPS data to better understand the defects of the samples [19].

References

[1] R. Athle, "Development of ferroelectric hafnium oxide for negative capacitance field effect transistors," *LUP Student Papers*, 2019.

[2] V. Garcia and M. Bibes, "Ferroelectric tunnel junctions for information storage and processing," *Nature communications*, vol. 5, no. 1, pp. 1–12, 2014.

[3] M. Pešić, F. P. G. Fengler, L. Larcher, A. Padovani, T. Schenk, E. D. Grimley, X. Sang, J. M. LeBeau, S. Slesazeck, U. Schroeder, and T. Mikolajick, "Physical mechanisms behind the field-cycling behavior of HfO_2 -based ferroelectric capacitors," *Advanced Functional Materials*, vol. 26, no. 25, pp. 4601–4612, 2016.

[4] A. E. Persson, R. Athle, J. Svensson, M. Borg, and L.-E. Wernersson, "A method for estimating defects in ferroelectric thin film moscaps," *Applied Physics Letters*, vol. 117, no. 24, p. 242902, 2020.

[5] R. Ratnesh, A. Goel, G. Kaushik, H. Garg, Chandan, M. Singh, and B. Prasad, "Advancement and challenges in mosfet scaling," *Materials Science in Semiconductor Processing*, vol. 134, p. 106002, 2021.

[6] T. Mikolajick, U. Schroeder, and S. Slesazeck, "The past, the present, and the future of ferroelectric memories," *IEEE Transactions on Electron Devices*, vol. 67, no. 4, pp. 1434–1443, 2020.

[7] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, "Ferroelectricity in hafnium oxide thin films," *Applied Physics Letters*, vol. 99, no. 10, p. 102903, 2011.

[8] S. S. Cheema, N. Shanker, C.-H. Hsu, A. Datar, J. Bae, D. Kwon, and S. Salahuddin, "One nanometer HfO_2-based ferroelectric tunnel junctions on silicon," *arXiv preprint arXiv:2007.06182*, 2020.

[9] R. Athle, A. E. O. Persson, A. Irish, H. Menon, R. Timm, and M. Borg, "Effects of TiN top electrode texturing on ferroelectricity in $Hf_{1-x}Zr_xO_2$," *ACS Applied Materials & Interfaces*, vol. 13, no. 9, pp. 11089–11095, 2021. PMID: 33625827.

[10] É. O'Connor, M. Halter, F. Eltes, M. Sousa, A. Kellock, S. Abel, and J. Fompeyrine, "Stabilization of ferroelectric $Hf_xZr_{1-x}O_2$ films using a millisecond flash lamp annealing technique," *Apl Materials*, vol. 6, no. 12, p. 121103, 2018.

[11] L. Grenouillet, T. Francois, J. Coignus, S. Kerdilès, N. Vaxelaire, C. Carabasse, F. Mehmood, S. Chevalliez, C. Pellissier, F. Triozon, *et al.*, "Nanosecond laser anneal (nla) for Si-implanted HfO_2 ferroelectric memories integrated in back-end of line (beol)," in *2020 IEEE Symposium on VLSI Technology*, pp. 1–2, IEEE, 2020.

[12] Y.-S. Kang, H.-K. Kang, D.-K. Kim, K.-S. Jeong, M. Baik, Y. An, H. Kim, J.-D. Song, and M.-H. Cho, "Structural and electrical properties of eot HfO_2 (< 1 nm) grown on inas by atomic layer deposition and its thermal stability," *ACS applied materials & interfaces*, vol. 8, no. 11, pp. 7489–7498, 2016.

[13] M. Dawber, K. M. Rabe, and J. F. Scott, "Physics of thin-film ferroelectric oxides," *Rev. Mod. Phys.*, vol. 77, pp. 1083–1130, Oct 2005.

[14] D. Damjanovic, *Hysteresis in piezoelectric and ferroelectric materials.*, vol. 3. Ceramics Laboratory, Materials Science and Engineering Institute, School of Engineering, Swiss Federal Institute of Technology - EPFL: Elsevier Ltd, 2006.

[15] J. Muller, T. S. Boscke, U. Schroder, S. Mueller, D. Brauhaus, U. Bottger, L. Frey, and T. Mikolajick, "Ferroelectricity in simple binary ZrO_2 and HfO_2," *Nano letters*, vol. 12, no. 8, pp. 4318–4323, 2012.

[16] S. Migita, H. Ota, K. Shibuya, H. Yamada, A. Sawa, T. Matsukawa, and A. Toriumi, "Phase transformation behavior of ultrathin $Hf_{0.5}Zr_{0.5}O_2$ films investigated through wide range annealing experiments," *Japanese Journal of Applied Physics*, vol. 58, no. SB, p. SBBA07, 2019.

[17] N. Volodina, A. Dmitriyeva, A. Chouprik, E. Gatskevich, and A. Zenkevich, "Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ thin films crystallized by pulsed laser annealing," *physica status solidi (RRL)–Rapid Research Letters*, vol. 15, no. 5, p. 2100082, 2021.

[18] L. Rebohle, S. Prucnal, and W. Skorupa, "A review of thermal processing in the subsecond range: semiconductors and beyond," *Semiconductor Science and Technology*, vol. 31, no. 10, p. 103001, 2016.

[19] R. Athle, T. Blom, A. Irish, A. E. O. Persson, L.-E. Wernersson, R. Timm, and M. Borg, "Improved endurance of ferroelectric $Hf_xZr_{1-x}O_2$ integrated on InAs using millisecond annealing," *Advanced Materials Interfaces*, p. 2201038, 2022.

Appendix A

Extra Material

Table A.1: Relevant simulation parameters used in COMSOL to achieve figure 5.1. The InAs/HZO/TiN is part of the sample while Si is a carrier wafer part of the FLA experimental setup.

Layer	Thickness	Doping	Reflectivity
TiN	10 nm	-	0.41
HZO	10 nm	1:1 (Hf/Zr)	-
InAs	280 µm	$1 \times 10^{16}\,\mathrm{cm}^{-3}$	-
Si	280 µm	-	-

$$T_{peak}[\mathrm{K}] = 495.5 + 16.3 \cdot E_{pulse}[\mathrm{J\,cm}^{-2}] \tag{A.1}$$

Appendix B

Processing Parameters

Table B.1: Selected sample processing conditions for series 1.

Sample Number		1	2	3	4	5
HZO						
Growth Temperature	[°C]	200	200	200	200	200
Deposition Cycles	[Hf:Zr]	50:50	50:50	50:50	50:50	50:50
FLA						
Preheat Temperature	[°C]	250	250	250	250	250
Peak Temperature	[°C]	**467**	**548**	**630**	**711**	**752**
Number of Flashes		1	1	1	1	1

Table B.2: Selected sample processing conditions for series 2.

Sample Number		1	2	3	4
HZO					
Growth Temperature	[°C]	200	200	200	200
Deposition Cycles	[Hf:Zr]	50:50	50:50	50:50	50:50
FLA					
Preheat Temperature	[°C]	250	250	250	250
Peak Temperature	[°C]	630	630	630	630
Number of Flashes		**1**	**2**	**4**	**8**

Table B.3: Selected sample processing conditions for series 3.

Sample Number		1	2	3
HZO				
Growth Temperature	[°C]	200	200	200
Deposition Cycles	[Hf:Zr]	50:50	50:50	50:50
FLA				
Preheat Temperature	[°C]	250	250	250
Peak Temperature	[°C]	548	548	548
Number of Flashes		**2**	**4**	**8**

Table B.4: Selected sample processing conditions for series 4.

Sample Number		1	2	3
HZO				
Growth Temperature	[°C]	270	270	270
Deposition Cycles	[Hf:Zr]	60:60	60:60	60:60
FLA				
Preheat Temperature	[°C]	250	250	250
Peak Temperature	[°C]	**548**	**630**	**711**
Number of Flashes		1	1	1

Table B.5: Selected sample processing conditions for series 5.

Sample Number		1	2	3
HZO				
Growth Temperature	[°C]	270	270	270
Deposition Cycles	[Hf:Zr]	60:60	60:60	60:60
FLA				
Preheat Temperature	[°C]	250	250	250
Peak Temperature	[°C]	548	548	548
Number of Flashes		**1**	**2**	**4**