Design of a 13-Bit SAR ADC with kT/C noise cancellation technique

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Popular Summary

With advancements in technology and integrated circuits, communication has evolved from telegraphs and landlines to video calls spanning the globe. There is a huge transition from large desktop computers to palm-sized mobile phones and tablets , emphasizing the pursuit of faster, more power-efficient devices with increased memory capacity. At the core of all electronic devices is a processor, often called the brain of the computer operate using binary code (zeros and ones). But, the real world communicates in analog signals. To bridge this gap, ADCs are crucial, and present in nearly every electronic device. For instance, in a mobile phone, our voice, as an analog signal, is converted by the ADC into a digital signal, enabling the device to recognize and utilize it for various functions and applications.

The thesis focuses on the design and implementation of a 13-bit Successive Approximation Register (SAR) ADC. Additionally, it aims to prove the effectiveness of the kT/C noise cancellation technique in reducing noise introduced during sampling. In this project, a 40 MHz sampling rate is employed for the 13-bit SAR ADC with kT/C noise cancellation. The resolution of the ADC set at 13 bits, indicates its accuracy, dividing analog signals into 8096 different levels, each corresponding to a binary code.

Designing a SAR ADC for higher bits requires a larger input capacitance. The challenge is to reduce this input capacitance while cancelling the resultant in kT/C noise generated, which would otherwise reduce the Signal-to-Noise Ratio (SNR) of the system. The implementation of the kT/C noise cancellation technique aims to address this challenge, allowing for the use of a smaller input capacitance while maintaining or improving the SNR.

Abstract

One of the main limitations of a Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) is the large input capacitance needed to achieve the desired performance. This large input capacitance increases the total area of the ADC and it imposes the use of a powerful buffer to drive it. Since the input capacitance is inversely proportional to the kT/C noise, reducing it, generates more noise. To reduce the input capacitance, there is a need to deal with the extra noise generated.

In this thesis, a 13-bit SAR ADC at 40MS/s using kT/C noise cancellation has been designed in 65nm technology node. This technique allows for a considerable decrease in the size of the ADC input capacitor without reducing the ADC's performance, it also reduces the requirements for the input buffers.

The designed SAR ADC uses a total input capacitance of 172.8 fF and it achieves an SNR of 67.64 dB before noise cancellation and 74.173 dB after noise cancellation. To achieve similar results without implementing the noise cancellation technique one has to increase the input capacitance by at least 10 times. Hence, there is a need to implement noise cancellation techniques, as using large input capacitance to designs SAR ADC increasing the overall area of the design.

Acknowledgements

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Abbreviations

- ADC : Analog to Digital Converter
- ASAR : Asynchronous Successive Approximation Register
- DAC : Digital to Analog Converter
- DNL : Differential Non-Linearity
- ENOB : Effective Number Of Bits
- FFT : Fast Fourier Transform
- INL : Integral Non-Linearity
- LSB : Least Significant Bit
- MOS : Metal Oxide Semiconductor
- MSB : Most Significant Bit
- NC : Noise Cancellation
- SSAR : Synchronous Successive Approximation Register
- SNR : Signal to Noise Ratio
- SNDR : Signal to Noise and Distortion Ratio
- SQNR : Signal to Quantization Noise Ratio

Contents

Chapter 1

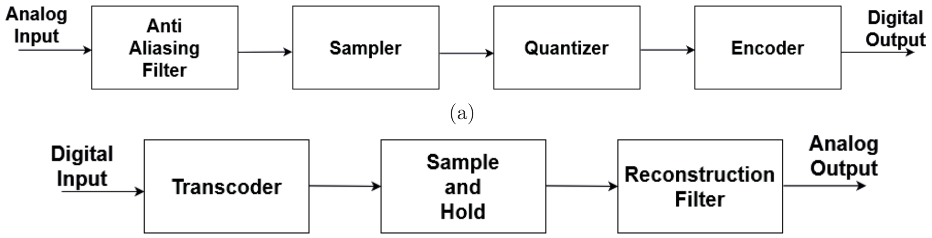
Introduction

1.1 Background

Analog electronics has always maintained its significance across various applications. Even though digital electronics has made huge progress, analog electronics still holds its head high because the real world mostly works with analog. There is a need to convert these analog quantities into digital logic levels and vice versa based on requirements of the applications and data converters achieves this task [6].

Data converters are pivotal components in bridging the gap between continuous analog signals and discrete digital signals. These devices come in two main types: Analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). ADCs capture the analog signals and convert them to digital. DACs perform the exact opposite by transforming digital data into analog, enabling devices to interact with the analog world. A basic block diagram of the ADC and DAC is shown in Fig 1.1 below [2].

Noise in a system effects the overall performance of the system. In context of analog to digital converters which is the main focus of this thesis, several types of noise can be seen. kT/C noise and quantization noise dominate the ADC noise floor and these are used to approximate the ADCs effective noise figure. It is crucial to understand these different types of noise for designing and optimizing SAR ADCs.



(a)

(b)

Figure 1.1: Basic Block Diagram a) Analog to digital and b) Digital to analog conversion

1.2 Objective

In this thesis work, an effort has been made to cancel the kT/C noise which is associated with thermal agitation of charge carriers in resistors and capacitors within electronic circuits. It is important to cancel this noise as it introduces fluctuations in the analog signal during the comparison, leading to uncertainty in the decision making process for comparators. This causes comparators to erroneously interpret small signal variations affecting the accuracy of ADCs.

Implementing a CDAC for SAR ADC with very small capacitance increases the kT/C noise. It is important to cancel this noise to obtain better performance. The noise cancellation technique shown in this thesis not only cancels the kT/C noise but also helps us in using small capacitance there by reducing the overall area of the SAR ADC.

Chapter 2

Basic principles of Analog to Digital converter

2.1 Introduction to Analog to Digital converters

Based on the sampling frequency, ADCs can be broadly classified into two major categories.

Nyquist rate ADCs operate at the Nyquist sampling rate, which is twice the maximum frequency present in the analog input signal. They ensure that the input signal is sampled adequately to avoid aliasing, which is the distortion caused by undersampling. Nyquist rate ADCs typically have a lower sampling frequency and require anti-aliasing filters to remove unwanted frequencies prior to sampling.

Oversampled ADCs operate at a higher sampling frequency compared to the Nyquist rate. Oversampling allows for more accurate and higher-resolution conversion by capturing additional information about the input signal. These ADCs utilize techniques such as oversampling, noise shaping, and digital filtering to improve the overall performance and achieve higher resolution.

2.2 Nyquist A/D converter

Nyquist A/D converters, are a type of analog-to-digital converters that operate at the Nyquist sampling rate. The Nyquist rate is defined as twice the maximum frequency present in the analog input signal. These converters are designed to ensure that the input signal is adequately sampled without causing aliasing, which is a distortion caused by undersampling. This theorem also states that, to accurately reconstruct an analog signal from its digital representation, the sampling rate must be at least twice the highest frequency present in the analog signal. Nyquist ADCs must adhere to this principle to ensure they sample the input signal at a rate that captures all relevant information.

Sampling theory: The Nyquist-Shannon Sampling theorem is one of the most important concepts in signal processing. It states that a continuous analog signal can be perfectly reconstructed from its samples if and only if the sampling frequency f_s is greater than or equal to twice the maximum frequency f_{max} present in the signal.

$$f_s \geq 2.f_{max} \tag{2.1}$$

This theorem ensures that aliasing is neglected, which is the phenomenon where high-frequency components in the analog signal are erroneously folded into lower frequencies during the sampling process [2].

Anti-Aliasing filter: Before the analog signal is sampled it is often passed through an anti-aliasing filter to remove the high-frequency components from the signal that could cause aliasing when sampled.

ADC Core: The core of a Nyquist ADC consists of the actual analog-to-digital converter which converts the sampled signal into a digital code. This core can use various architectures like Successive Approximation Register, flash ADC, pipeline ADC, or delta-sigma ADC which are discussed further.

Trade-offs: Though Nyquist ADCs are widely used, they come with trade-offs such as speed, power consumption, and cost. Faster ADCs consume more power and may be more expensive. Designers must balance these factors to meet the specific requirements of their application.

2.2.1 Flash ADC

A Flash ADC also known as a parallel ADC or direct ADC, is a high-speed analog-to-digital converter that employs a bank of comparators for rapid conversion. Its name "Flash" reflects its ability to generate digital output almost instantly in a single clock cycle.

The basic idea of a Flash ADC is to compare the input voltage to a set of reference voltages in binary-weighted manner and produce a digital code representing the comparison results. A block diagram of N-bit Flash ADC is given below in Fig 2.1.

Reference Voltage: The ADC uses a reference voltage network that generates a series of reference voltages, each representing a different weight. These reference voltages are equally spaced and cover the full input voltage range.

Comparator Array: the heart of the Flash ADC is an array of high-speed voltage comparators. Each comparator compares the input voltage to one of the reference voltages.

Encoder: The output of each comparator is a binary '1' or '0' depending on whether the input voltage is greater or less than the reference voltage. These binary outputs are then fed into the encoder circuit.

Encoder Operation: The encoder examines the binary outputs from the comparators and generates a digital code representing the highest reference voltage that the input voltage exceeds. This digital code is the output of the Flash ADC and represents the analog input voltage.
Pros: Speed, Low latency (entire conversion process takes place within a single clock cycle)
Cons: Power consumption and cost.

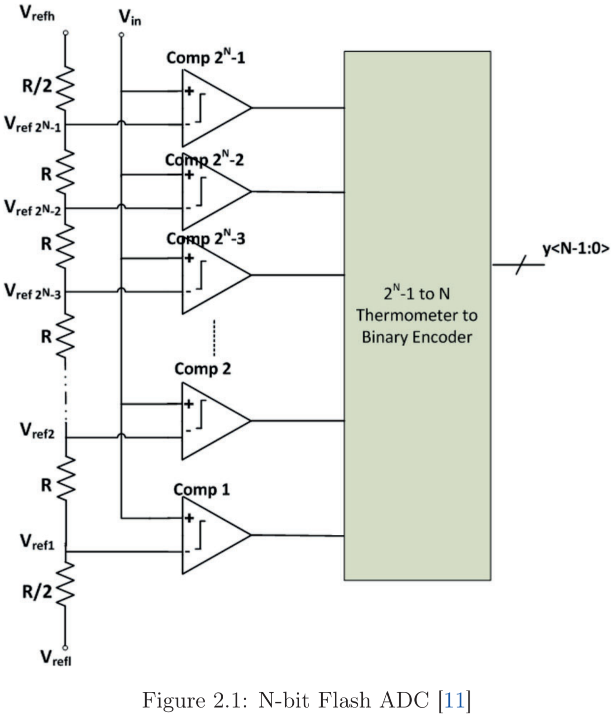


Figure 2.1: N-bit Flash ADC [11]

2.2.2 Dual slope ADC

Dual slope ADC is a type of analog-to-digital converter that uses two integration slopes to convert an analog input voltage into digital output.

Key components

Integrator (Ramp Generator): It is the heart of dual slope ADC. The integrator generates a linear ramp waveform. The slope of this ramp is controlled by the input voltage to be measured.

Comparator: A comparator is used to measure the ramp voltage with the reference voltage. The comparator generates a signal indicating when the ramp voltage crosses the reference voltage.

Counters: This ADC employs two counters up and down counter. The up counter counts the time taken for the integrator output voltage to reach the reference voltage. The down counter counts the time taken for the integrator to discharge from the reference voltage back to zero.

Working principle

The integrator is allowed to integrate in positive slop until the ramp voltage equals the input voltage. Up counter keeps track of the time taken during this integration. When the ramp voltage reaches the input voltage the comparator triggers a switch to change the slope of the ramp. The integrator now integrates in a negative slope until the ramp voltage returns to zero. During the negative slope, the down counter keeps track of the time taken for the integrator to discharge. The digital output is determined based on the counts recorded by the up and down counter. A typical block diagram of Dual slope is shown below in Fig 2.2.

Pros: High noise rejection, low cost, Improved linearity.

Cons: Slower conversion speed, large size, power consumption.

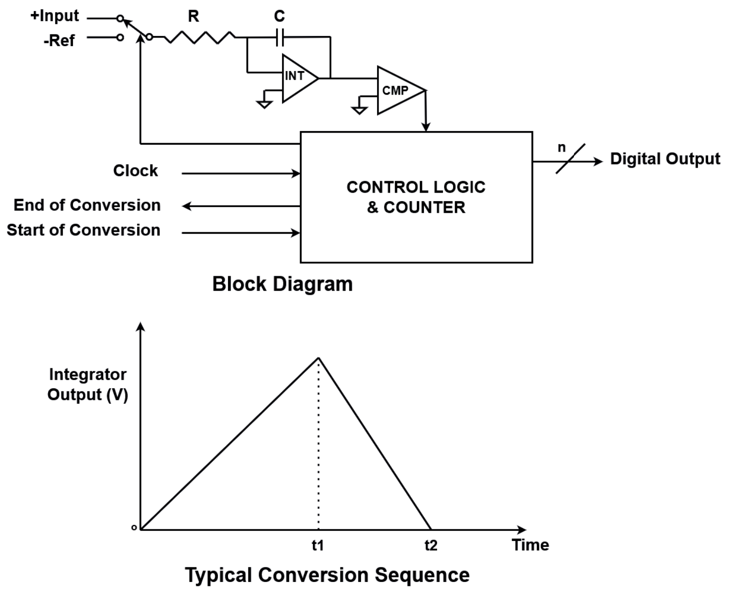


Figure 2.2: Dual Slope ADC block diagram and its output waveform [12]

2.2.3 Pipeline ADC

A pipeline ADC is a high-speed and high-resolution ADC architecture commonly employed in various applications, including telecommunication, medical imaging, and multimedia processing. It achieves its performance by breaking down the analog-to-digital conversion process into several stages or pipelines. Each stage is responsible for processing a fraction of the input signal's dynamic range, and the results are combined to generate the final digital output. The pipeline can achieve high-speed conversion with reasonable accuracy, making it suitable for high-frequency and high-resolution applications. The block diagram of a pipeline ADC is shown below in Fig 2.3.

Working principle

Input Sampling: The analog input signal is sampled at the beginning of the pipeline. This sampled signal is then processed through a series of identical stages.

Stages: A pipeline ADC consists of multiple identical stages depending on the resolution. Stage 1: This stage processes the input signal and provides coarse quantization. It typically divides the input range into 2^N segments, where N is the number of bits assigned to this stage. The quantized output from this stage is often referred to as the stage 1 output or intermediate output.

Inter-stage Sample and Hold: After each stage, the output is sampled and held for a brief period. This allows the next stage to process the data while maintaining the same input signal value.

Subsequent Stages: The following stages continue to refine the quantization by dividing the remaining dynamic range into smaller segments. Each stage operates on the residual error from the previous stage, narrowing it down further. The output of each stage is sampled and held for the next stage.

Digital Combining Logic: After the last stage, the digital outputs from all stages are combined into a single digital word that represents the final digital output. This combining logic aligns the outputs from each stage to create the complete digital code.

Pros: High-speed Conversion, high resolution.

Cons: of Pipeline ADC: Complex design, Latency, Lower accuracy at high frequencies.

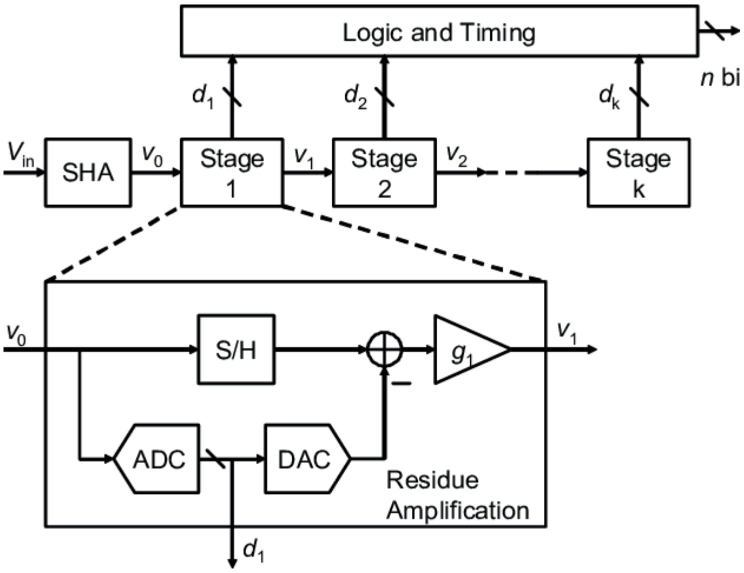


Figure 2.3: Block diagram of an N-bit Pipeline ADC [13].

2.3 Over-sampled A/D converter

2.3.1 Delta Sigma ADC

Delta-sigma ADC is a type of analog-to-digital convert that achieves high resolution by oversampling the input signal and using a feedback loop to quantize the difference between the actual and predicted signals. The block diagram of Delta Sigma ADC is given below in Fig 2.4.

Key components

Modulator : The modulator is the core component of a delta sigma ADC. It consists of an integrator and a comparator. The integrator continuously accumulates the difference between the input signal and its digital representation. The comparator compares the integrated signal with reference voltage and generates a 1 bit quantized output.

Feedback loop: The quantized output is fed back to adjust the integrator's input. The feedback loop helps in continuously refining the accuracy of the representation.

Digital Filter: A digital filter is employed to filter the high-frequency noise introduced by oversampling. The noise-shaping property of the delta-sigma modulator pushes quantization noise to higher frequencies.

Decimator: The filtered and over-sampled bitstream is then passed through a decimator. The decimator reduces the data rate by averaging or selecting specific samples.

Working principle

Delta sigma ADCs sample the input at a rate much higher than Nyquist rate. If the Nyquist rate is $f_{nyquist}$, a delta-sigma ADC might sample at N*$f_{nyquist}$ where n is a high oversampling ratio. The modulator integrates the difference between the input signal and the digital representation. The result is a 1-bit quantized signal. The 1-bit quantized signal is fed back to adjust the integrator's input, reducing the error between the actual and quantized signals. The feedback loop inherently performs noise shaping, pushing quantization noise to higher frequencies. This allows the use of a simple digital filter to remove the higher-frequency noise. The filtered and over-sampled bitstream is processed by a digital filter. The digital filter suppresses high-frequency noise and provides a high-resolution output.

The decimator reduces the data rate by selecting or averaging specific samples. The final output is a digital representation of the input signal with significantly enhanced resolution.

Pros: High Resolution, Simplicity of analog circuitry, Flexible architecture.
Cons: High power consumption, Complex digital circuitry.

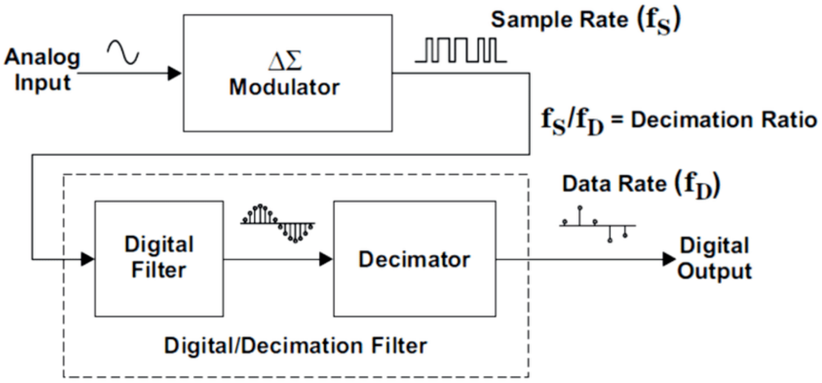


Figure 2.4: Block diagram of a Delta-Sigma ADC [14].

2.4 Performance metrics

Performance metrics are essential for evaluating the quality of Analog to digital converters. These metrics can be broadly divided into two main categories.

2.4.1 Static characteristics

The Static characteristics of an ADC reveal the discrepancies between the ADC's transfer characteristics and the ideal characteristics.

Offset error

Offset Error is the difference between the beginning of the first actual code transition point and the ideal code transition point present in the ideal characteristics. This offset can result from imperfections in the ADCs circuitry, such as component mismatches or DC voltage offsets.

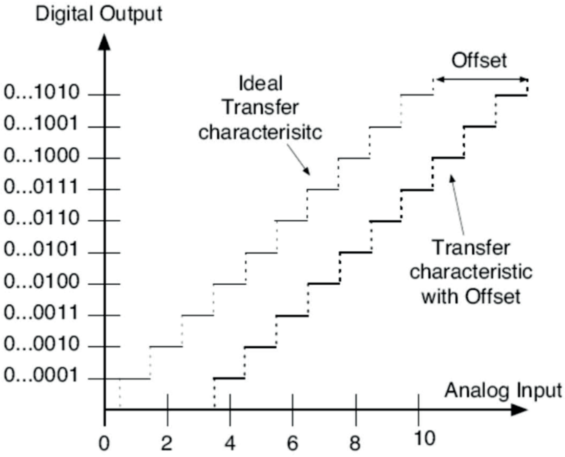


Figure 2.5: Offset error in SAR ADC [3].

Gain error

The gain error depicts the difference between the last actual code transition point and the ideal one considering that the offset error has been removed.

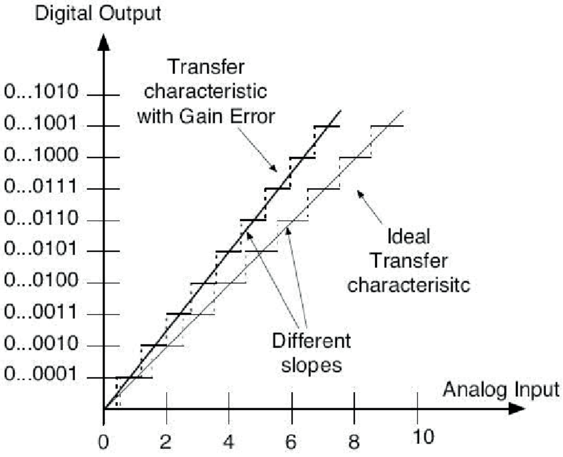


Figure 2.6: Gain error in SAR ADC [3].

Differential Non-Linearity(DNL)

Differential Non-Linearity (DNL) stands out as a crucial performance metric in static characteristics, showcasing the variance in code width at the 1 Least Significant Bit (LSB) level compared to the ideal width of 1 LSB. DNL is typically expressed in LSB units. A positive DNL signifies that the transition point is higher than expected, indicating a greater voltage difference than 1 LSB. Conversely, a negative DNL suggests that the transition point is lower than expected, with a voltage difference of less than 1 LSB. To ensure precise conversions, particularly in high-precision applications, it is crucial to choose an Analog-to-Digital Converter (ADC) with low DNL. An example illustrating the DNL characteristics of a Successive Approximation Register (SAR) ADC is presented below in Fig 2.7.

1LSB step: Refers to the change in the digital output code when the analog input voltage crosses one of these thresholds or reference points. In a perfect ADC, this change should be exactly 1 LSB. In other words, when you increment the analog input voltage by the smallest possible amount that the ADC can resolve, the digital output code should increase by 1.

$$1 \text{ LSB} = FullScaleRange/2^{resolution} \tag{2.2}$$

Example: For a 13-bit ADC with a full-scale range of 0 to 5V, 1 LSB is 122μ V.

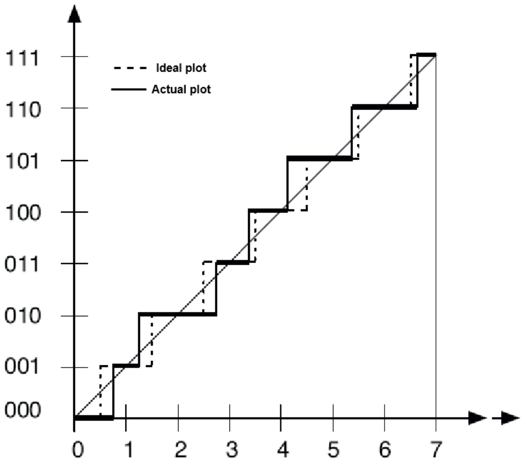


Figure 2.7: DNL characteristics in SAR ADC [3].

Integral Non-Linearity(INL)

INL is a critical performance parameter used to characterize the linearity of an ADC. INL measures the deviation of the actual transfer function of the ADC from an ideal straight line. INL is also expressed in terms of LSBs, where one LSB represents. In an ideal ADC, the digital output codes are perfectly linearly spaced concerning the analog input voltage. This means that for each increment in the digital code, the input voltage increases by exactly one LSB. In such a case, the INL would be zero [6].

In real-world ADCs, imperfections such as capacitor mismatches, non-idealities in switches, offset errors and gain errors can introduce nonlinearity into the conversion process. This nonlinearity results in deviations between the actual and ideal codes, giving rise to an INL value greater than zero.

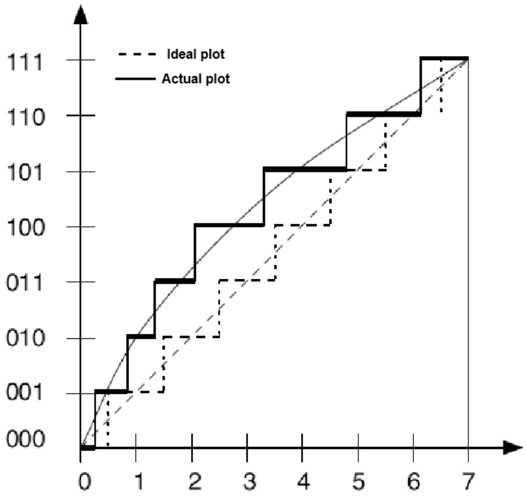


Figure 2.8: INL characteristics in SAR ADC.

2.4.2 Dynamic characteristics

The dynamic characteristics are obtained by the response of the ADC for a sinusoidal input. It is used to calculate the frequency response of the system. This analysis is used to learn more information about noise and also about other high-frequency effects. These performance metrics are exhibited by parameters like SNR, SNDR, SFDR, and ENOB.

Signal to noise ratio (SNR)

SNR is defined as the ratio of the power of the signal and the total noise power generated by the quantization process. This property accounts for the whole noise present in the entire Nyquist range. Its value depends on the magnitude of the input signal and it decreases with the decrease in the signal amplitude. SNR is given by:

$$SNR_{(dBFS)} = 10.log_{10}(P_{signal}/P_{noise}) \tag{2.3}$$

$$SQNR = (6.02 * resolution + 1.76) \tag{2.4}$$

P_{signal} represents the power of the desired input signal that the ADC is intended to measure and digitize.

P_{noise} represents the power of all unwanted noise sources present in ADCs output noise sources can include quantization noise, thermal noise, electromagnetic interference and other sources of interference. Quantization noise is a significant contributor, arising from the discrete nature of digital representation in ADCs. A higher SNR indicates better ADC performance.

Signal to noise distortion ratio (SNDR)

SNDR provides a comprehensive measure of the ADCs ability to capture the desired signal while considering both noise and harmonic distortion components in the ADCs output. SNDR is a critical metric for assessing ADC performance because it provides a more detailed view than SAR. While SNR focuses solely on the comparison between the desired signal and overall noise, SNDR accounts for both noise and harmonic distortion. SNDR is given by:

$$SNDR_{(dBFS)} = 10.log_{10}(P_{signal}/P_{noise+distortion}) \tag{2.5}$$

Spurious free dynamic range(SFDR)

SFDR is one of the critical metrics for ADCs. It quantifies the ADCs ability to capture the weak input signals in the presence of undesired noise and interference such as harmonics and spurious signals. A high SFDR indicates that the ADC can effectively distinguish between the desired signal and unwanted spurious components. It also reflects the ADCs linearity and ability to maintain accuracy even when strong undesired signals are present in the input.

Understanding the spurious signals: In real-world analog signals and electronics systems, there are often unwanted components known as 'spurious signals or spurs'.

SFDR measures the range between the strongest spurious signal (unwanted harmonic or distortion) and the ADCs fundamental signal. The dynamic range is the difference in power between the strongest spurious signal and the power of the fundamental signal.

Effective number of bits (ENOB)

Effective Number of Bits (ENOB), is a key performance metric used to evaluate the accuracy or precision of an analog-to-digital converter (ADC). ENOB quantifies the actual resolution of an ADC system, accounting for the effects of noise and distortion. It provides a measure of how closely the ADC approximates an ideal ADC with the same resolution. ENOB takes into account both quantization noise and any other noise or distortion sources.

$$ENOB = (SINAD_{(dB)} - 1.76_{(dB)})/(6.02_{(dB/bit)}) \tag{2.6}$$

SNDR (SINAD) represents the ratio of the amplitude of the analog input signal to the RMS value of the quantization noise, other noises, and distortion. The factor 1.76 accounts for the inherent noise sources in an ideal ADC and 6.02 is a conversion factor for translating SINAD to ENOB. Higher ENOB values indicate better overall performance, meaning that the ADC effectively utilizes more bits for representing the signal and has less noise or distortion.

2.5 Successive Approximation Register(SAR) converters

SAR ADC is a type of nyquist ADC with an attractive architecture that is suitable for various modern applications. It is a digital-friendly architecture. The term digital friendly means that the ADC is partially built with many digital blocks. The whole system can be divided into four main subsystems namely a Sample and hold circuit, a Capacitive DAC, a Comparator, and a SAR logic block. SAR works on a binary search algorithm which is used to convert the analog input signal to an equivalent digital output. Most of the SAR ADCs also incorporate the charge redistribution technique described in [5] using a binary weighted capacitor array to perform high-speed conversion. SAR ADC falls under the Nyquist rate ADC. Compared with other Nyquist rate ADCs, the SAR ADC has a lot of positives in terms of power efficiency, minimized design complexity, low chip area, and high-speed operation.

SAR ADC is a type of analog-to-digital converter that operates by successively approximating the analog input to a digital code. It utilizes a binary search algorithm to determine the digital representation of the input signal.

Key components

DAC: SAR ADCs have an internal DAC that generates an analog voltage based on the digital code being tested.
Comparator: The comparator compares the generated DAC voltage which is present at the input of the two terminals of the comparator.
SAR Logic and register: The SAR logic controls the successive approximation process. A shift register, known as the SAR register holds the intermediate digital approximation.

Working

The process starts by setting the internal registers of the ADC. The digital output initially contains all zeros. The input of all the switches is turned on initially. If the Vp+ is greater than Vn-. Then the comparator digital output is set to 1. Based on this comparison result (1 or 0) the MSB is set to 1 or 0 and then based on MSB the next bit MSB-1 is set to 1 or 0 and this continues for the complete 13-bit comparison. When every switch is switched on or off the DAC will convert the digital value into analog which is compared. After all 13bits have been determined through successive approximation processes, the ADC generates a final 13-bit digital code that represents the analog input value. The logic block used here has been designed by using Verilog-A code. Based on the comparator output the control signals for the CDAC which is necessary for the conversion process are generated by the logic block. This is how an SAR ADC works in brief and going further we can discuss in deep about each stage, their implementation, and results.

SAR ADC can be distinguished into two types based on the way clocking schemes are used. They are Synchronous SAR and Asynchronous SAR.

Synchronous SAR (SSAR) It is clocked by a high-speed external clock signal. This clock is distributed to all the internal blocks, providing synchronization of internal blocks. The block diagram of the SSAR is shown below in Fig 2.9.

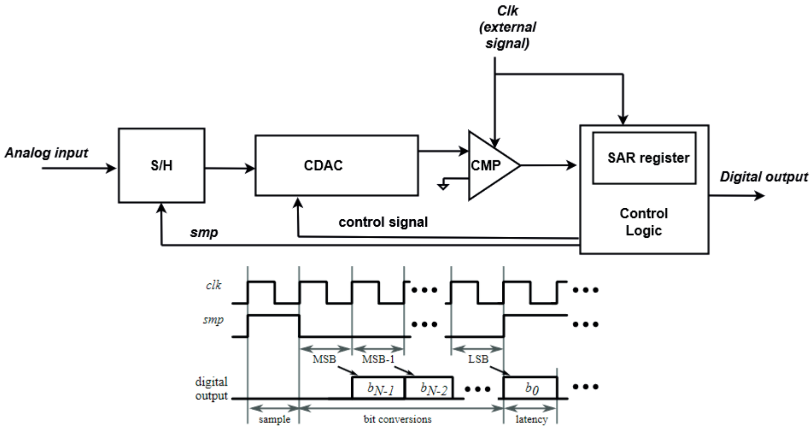


Figure 2.9: Block diagram and timing diagram of Synchronous SAR ADC [5]

Asynchronous SAR (ASAR) In ASAR the clock signals are generated by the logic block and are given to the comparator but also have an external sampling clock which is fed to the sample and hold block and the logic block. Block diagram of ASAR is shown below in Fig 2.10.

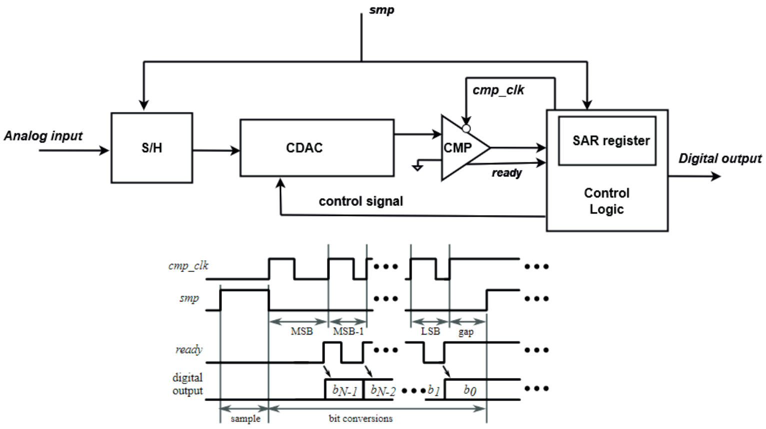


Figure 2.10: Block diagram and timing diagram of Asynchronous SAR ADC [5]

Chapter 3

SAR ADC with noise cancellation - Theory

3.1 Switches

Switches are necessary for the sampling and conversion process as they control the flow of signals to the circuit. In the design, two kinds of switches, transmission gate, and bootstrap are used. In general, switches can be designed by a single NMOS, parallel connection of both NMOS and PMOS and bootstrapped switches.

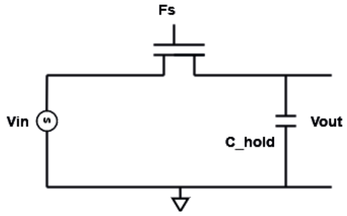


Figure 3.1: S/H circuit using NMOS switch

3.1.1 MOS Switch

A simple MOS switch can either be an NMOS or PMOS where the input is connected to the source and the gate of the transistors acts as the control switch to turn on or off the transistors. For an NMOS to turn on, the gate-source voltage must be high (V_{dd}) i.e. greater than threshold voltage V_{th}, and for a PMOS to turn on the gate-source voltage must be low (0) i.e. less than threshold voltage V_{th}. When the NMOS gate is high the transistor will turn on and the output equals input. Similarly, when the PMOS gate is low the transistor will turn on and the output equals input.

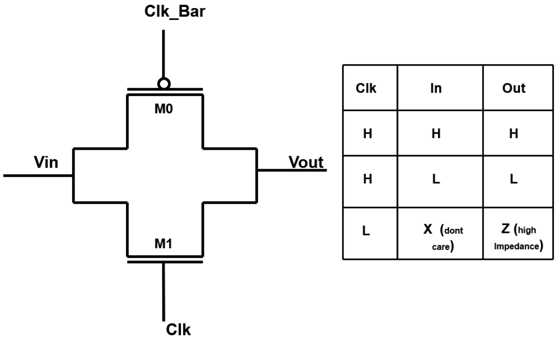
As shown in the figure below fs acts as the control signal and the input is given to the source of the transistor. Sampling output is taken across V_{out}. Typical sample and hold circuit using NMOS switch is shown above in Fig 3.1.

Transmission gate

A transmission gate is a fundamental electronics component used in both digital and analog circuits. It serves as a bidirectional switch that can used to control the flow of signals in a circuit. A transmission gate typically consists of two complementary metal oxide semiconductor (CMOS), one NMOS (N-channel MOS), and one PMOS (P-channel MOS).

On State: When a control signal is set to logic high both NMOS and PMOS transistors turn on simultaneously. In this state, the transmission gate effectively connects the input signal to the output without much resistance allowing the signal to pass through.

Off State: When the control signal is set to logic low both transistors turn off. In this state, the transmission gate acts as an open switch, effectively disconnecting the input and output, preventing the signal from passing through. designed by a single NMOS, parallel connection of both NMOS and PMOS and bootstrapped switches.



Clk	In	Out
H	H	H
H	L	L
L	X (dont care)	Z (high Impedance)

Figure 3.2: Transmission gate

Bootstrapped

The bootstrapped circuit technique minimizes the switch-on resistance variation in the presence of large input and output voltage swings. The basic structure is given in the figure below. Switches S_3 and and S_4 are controlled by the $\bar{Clk}$ signal and switches S_1, S_2, and S_5 are controlled by the Clk signal. When Clk is high Switches S_2 charges the cap C (Node A) to V_{dd}. When the $\bar{Clk}$ is high Switches S_1, S_5, and S_2 are closed and S_3 and S_4 are open. Now Node B will have the voltage to turn on the transistor there by maintaining a constant gate voltage. The transistor acts as a switch and because of the constant gate voltage at, it minimizes the variation in the switch on resistance.

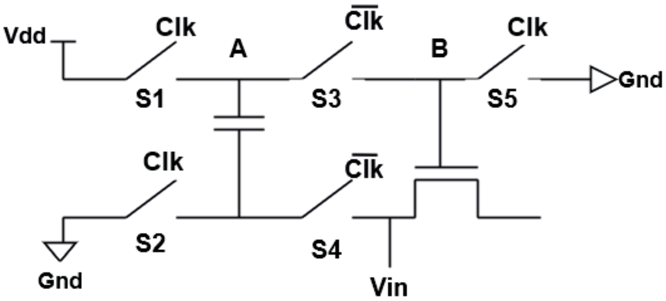


Figure 3.3: Basic model of bootstrapp

3.2 Sampling

The sampling process is one of the most crucial steps in an analog-to-digital converter which helps convert the continuous analog signals into discrete digital representations. Overview of the Sampling process:

1) Signal Acquisition: The first step is to get the analog signal that you want to convert. This signal can be from various sources like sensors, microphones, or any continuous waveform with varying voltage levels.

2) Sampling rate: the sampling rate, also known as the sampling frequency is a critical parameter in the sampling process. It determines how often the ADC takes samples of the analog signal per unit of time. The sampling rate is measured in Samples per second (Sps) or hertz (Hz). According to the Nyquist Theorem, "the sampling rate must be at least twice the frequency of the input signal" to accurately represent it in a digital form. This ensures that no information is lost during the conversion.

3) Sample and Hold (S/H) circuit: Before converting the analog signal

into a digital value, it needs to be "sampled" at specific intervals. A sample and hold circuit is used for this purpose. It captures the instantaneous value of the analog signal at predefined sampling points and holds it constant during the conversion process.

4) Quantization: After sampling, the ADC quantizes the sampled analog values. Quantization involves assigning discrete digital values to each sampled point. The resolution of the ADC determines how finely the analog range is divided into digital values. For example, a 10-bit resolution can represent the analog signal using 1024 different digital values.

3.2.1 Ideal Sampling

In an ideal world, zero resistance sampling switches. When the switch is closed V_{out} tracks the input V_{in} till the switch is open. When the switch is open it holds the value at that instant.

3.3 Switching Schemes

In capacitive SAR ADCs the switching and capacitor arrangements play an important role. The sequence in which the switches are turned on and off and the nodes to which these switches connect the capacitors etc. The switching scheme dictates the energy efficiency, DAC size, and other critical performance metrics of the ADC.

Charge redistribution and charge sharing are the two operation modes used in SAR ADC designs.

3.3.1 Charge Redistribution

In the charge redistribution (CR) scheme, the output of DAC is set by varying the voltage on the bottom plate of the capacitor while maintaining total capacitance unchanged.

Conventional Switching

Initially, the input is sampled on the bottom plate of the capacitors. Once the sampling is finished, these capacitors are disconnected from the input. Then in the top array, the MSB is connected to V_{ref} while the remaining are connected to the ground. On the bottom array, the opposite is done. This operation results in an energy consumption of $4CV^2$. For more information on switching schemes and comparison, check the plot below in Fig 3.4 [4].

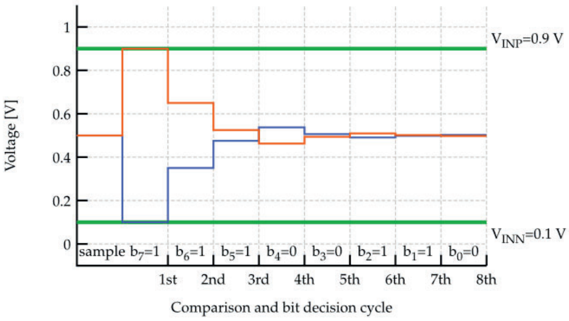


Figure 3.4: Conventional switching charge sharing plot [4]

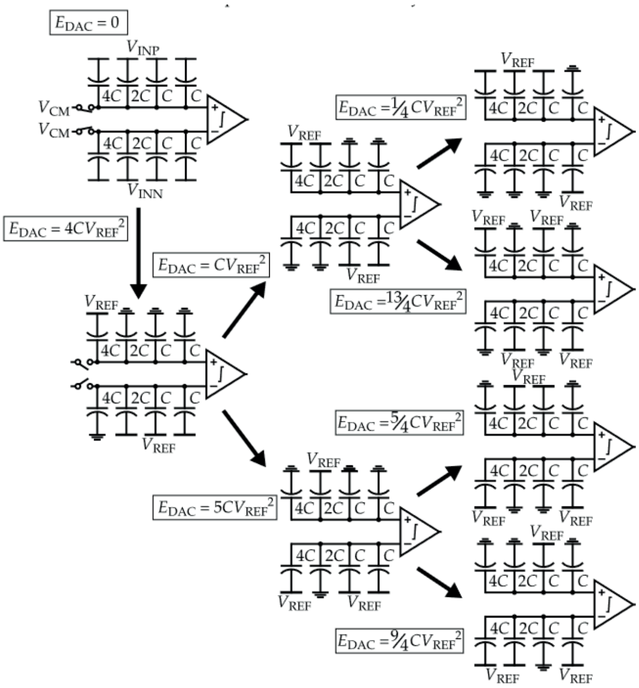


Figure 3.5: Conventional switching scheme

Monotonic Switching

The monotonic switching method was introduced to improve the efficiency of conventional switching. Requires only 2^{n-1} capacitors instead of 2^n. In the first phase, the input is sampled on the top plates of the capacitive arrays, while the bottom plates are connected to the reference voltage. The MSB is obtained by the comparator. Depending on whether the MSB is "0" or "1", the MSB capacitor of the bottom array or from the top array is connected to the ground. The same procedure is carried out for the remaining bits and the output bits are extracted from the comparator output. The switching and conversion cycle is shown in the figures below. For more information on switching schemes and comparison, check the plot below in Fig 3.6 [4].

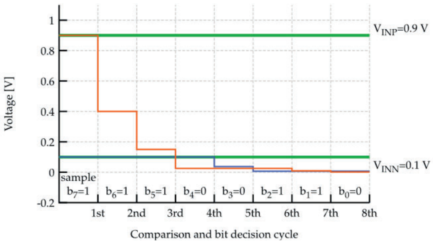
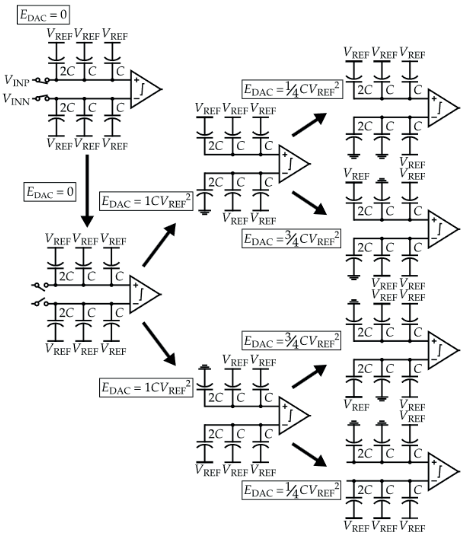


Figure 3.6: Monotonic switching charge sharing plot



$E_{DAC} = 0$
V_{REF} V_{REF} V_{REF}
2C C C
V_{INP}
V_{INN}
2C C C
V_{REF} V_{REF} V_{REF}
$E_{DAC} = 0$
$E_{DAC} = 1CV_{REF}^2$
$E_{DAC} = 1CV_{REF}^2$
$E_{DAC} = \frac{1}{4}CV_{REF}^2$
$E_{DAC} = \frac{3}{4}CV_{REF}^2$
$E_{DAC} = \frac{3}{4}CV_{REF}^2$
$E_{DAC} = \frac{1}{4}CV_{REF}^2$
+
−

Figure 3.7: Monotonic switching scheme

V_{cm} based switching Switching

V_{cm} based SAR ADC is also called merged capacitor switching. This switching scheme also employs top plate sampling, so that in the first cycle the inputs are connected to top plates, and bottom plates are connected to V_{cm}. Depending on the comparator result "0" or "1" the largest cap is discharged to the ground or charged to V_{ref}. A similar process is followed for all the other bits. For more information on switching schemes and comparison plot check the plot below in Fig 3.8 [4].

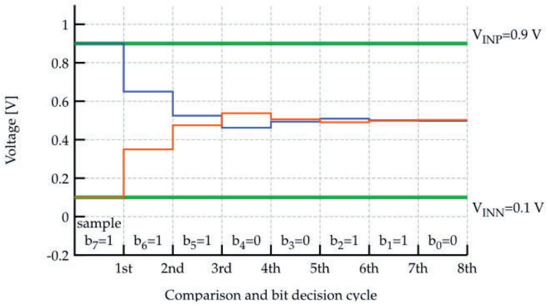


Figure 3.8: V_{cm} based switching charge sharing

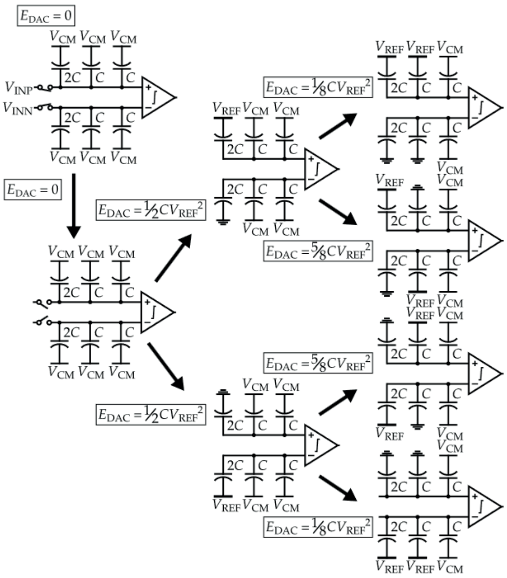


Figure 3.9: V_{cm} based switching scheme

3.4 Switched Capacitive DAC

In this thesis, a conventional switching scheme has been implemented. In a SAR ADC, the CDAC is an important part and it can be designed in both binary weighted and split capacitor CDAC architectures. The operation of the DAC can be divided into three sections:

1) Reset Mode: All the capacitors in the DAC are reset so that there are no pre-stored charges. If the capacitors are not reset they may add a lot of nonlinearities leading to improper charge sharing which ultimately results in wrong digital data. This step can be accomplished by connecting all capacitors to the ground.

2) Sampling Mode: In the sampling mode, the top plate of the capacitors is connected to V_{cm}(0.6 V), and all the bottom plates of the capacitors are connected to the input voltage level. The bottom plate is charged to input voltage and V_{cm} respectively. The input sampling switch is turned off first and connected to the ground. Now the top plate has V_{cm} - V_{in} voltage at the positive input and negative input of the comparator. Both are compared and based on the decision obtained, the MSB switching is determined.

3) Redistribution mode: The charge gets redistributed among different capacitors at different stages of the conversion cycle based on the switching. Based on the decision of the comparator in the sampling mode the MSB switch is connected to V_{ref} or Gnd. If the comparator decision was 1 then the Voltage at the positive input of the comparator would be [(V_{cm}-V_{in})+$V_{ref}/2$] and this continues till all the bits are resolved.

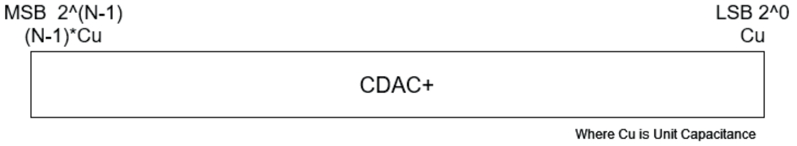


Figure 3.10: CDAC binary weighted design

3.4.1 Sample Mode

As mentioned before we are implementing both binary Weighted CDAC and the Split CDAC. Lets us discuss the binary-weighted structure first. To implement a 13-bit SAR ADC we have to have 8192 * C_u (unit capacitance). MSB will have the capacitance value 4096 * C_u and so on. All the 13 Capacitors in the positive array are connected to Vip which represents the positive input voltage. We have to follow the same for the negative array which is connected to V_{in}. In this mode, the sampling process is carried out and the values of input voltage and V_{cm} are stored in the top and bottom plates respectively. At the end of this mode the top plate in all the positive array capacitors will have V_{cm}-V_{in} value and all the negative array capacitors will have V_{cm}+V_{in}.

3.4.2 Redistribution Mode

In this mode, the voltage division operation happens among the capacitor arrays by connecting the MSB ($4096 * C_u$) to the positive reference voltage (V_{refp}). The same manner is followed in the negative array too by connecting the MSB $4096 * C_u$ to the negative reference voltage (V_{refn}). This operation leads to the situation of having a voltage equivalent of V_{cm}-V_{in}+($V_{ref}/2$) at the positive input of the comparator and a voltage equivalent of V_{cm}+V_{in}-($V_{ref}/2$) at the negative input port of the comparator. The same operation is continued for the other stages of the capacitors in the DAC array till the LSB is reached. The comparator gives out a high logic if the positive V_{DAC} is greater than the negative V_{DAC} level. High logic of 1.2 V and low logic of 0 are maintained in the project.

One of the main advantages of using the binary-weighted architecture is just because of the simplicity of the design and is also very efficient in performance. But because of a total of $8192 * C_u$ capacitance which increases the area and simulation time binary weight architecture is not preferred for higher resolution. In binary weighted CDAC design, the total capacitances grow exponentially with the increase in ADC resolution. An efficient way of reducing the total capacitance is implementing a split CDAC.

3.5 Split capacitor CDAC

In this architecture, a small bridge capacitor C_b is placed between the main-DAC (mDAC) and sub-DAC (sDAC) as an attenuation capacitance. It reduces the total capacitance by approximately half compared to the binary-weighted CDAC. Since the total capacitance is reduced, the Split capacitor CDAC architecture shows a decreased ADC power consumption and reduced chip area than the binary-weighted CDAC.

Total capacitance drops from

$$[2^N * C_u] - - - - > [2 * 2^{0.5N} * C_u]\ , \tag{3.1}$$

The bridge capacitance Cb can be calculated by

$$C_b = [(2^{0.5N}) * C_u/(2^{0.5N} - 1)] \tag{3.2}$$

The value of the bridge capacitance C_b is found by considering that C_b in series with the left side array must be equal to C_u.

$$C_u = (C_b * 2^{N/2} * C_u)/(C_b + 2^{N/2}C_u), \tag{3.3}$$

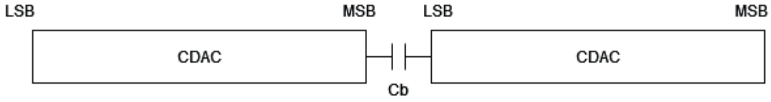


Figure 3.11: CDAC binary weighted design

3.6 Amplifier

Amplifiers are important electronic circuits that increase the strength or amplitude of the signals. They play a vital role in various applications including audio systems, communication devices, and instrumentation. Gain is a fundamental parameter of amplifiers and represents the ratio of the output signal amplitude to the input signal amplitude. It quantifies how much an amplifier multiplies the input signal. Gain is usually expressed in decibels (dB). The gain of the amplifier can be calculated using the following formula.

$$Gain(A) = V_{out}/V_{in} \tag{3.4}$$

Gain in dB is given by

$$Gain(dB) = 20 * log_{10}(V_{out}/V_{in}) \tag{3.5}$$

3.6.1 Differential Amplifier

An amplifier with differential input and differential output is a fundamental circuit in electronics used for amplifying the voltage difference between the two input signals while rejecting any common mode signals (signals that are common to both inputs). It is a critical component in applications where accurate signal processing, noise rejection, and precision are essential. Let's try to understand how to calculate its gain and understand the concept of feedback in differential amplifiers.

The gain of a differential amplifier is typically expressed in terms of the differential voltage gain(A_{dm}) and the common mode voltage gain (A_{cm}). The differential voltage gain represents how much the amplifier amplifies the difference between the two input voltages, while the common mode voltage gain represents how much it amplifies any voltage that is common to both inputs.

Differential mode gain

The differential gain of the amplifier quantifies how much the amplifier amplifies the voltage difference between two input signals, typically called the non-inverting input and the inverting input.

$$A_{dm} = V_o/V_d = -gmR_D, V_d = V_1 - V_2 \tag{3.6}$$

Common mode gain

An average of the two input signals is called a common mode signal denoted by V_c.

$$V_c = (V_1 + V_2)/2 \tag{3.7}$$

$$A_{cm} = V_o/V_c = -gmR_D/(1 + 2gmR_{ss} + R_D/r_o) \tag{3.8}$$

Common mode rejection ratio(CMRR)

The ability of a differential amplifier to reject a common mode signal is defined by a ratio called 'Common mode rejection ratio' denoted as CMRR. CMRR is defined as the ratio of the differential voltage gain A_{dm} to common mode gain A_{cm} and is expressed in dB.

$$CMRR = A_{dm}/A_{cm} \tag{3.9}$$

The major goal in circuit design is to minimize the noise level. Noise comes from many sources(thermal, EM, etc). A regular amplifier amplifies both signal and noise.

$$v_1 = v_{sig} + v_{noise} \tag{3.10}$$

$$v_o = A.v_1 = A.v_{sig} + A.v_{noise}. \tag{3.11}$$

If the signal is applied between two inputs and we use a difference amplifier with a large CMRR, the signal is amplified a lot more than the noise which improves the signal-to-noise ratio. So CMRR is important.

Inverter Based Amplifier with Common mode feedback

The designed amplifier achieves a high gain when the common mode voltage is close to the trip-point voltage (where the PMOS and NMOS have the same strength). This design as mentioned has CM feedback. The two resistors enable sensing the output common mode voltage. This voltage is used to bias the two tail transistors. When the common mode increases, the P-side transistor strengths are reduced, and the CM is reduced. Here the amplifier is used to amplify the analog CDAC output before it is compared by the comparator. Amplifiers are also used for any offset or gain errors in the signal before the analog signal is digitized. The amplifier design implemented is shown in the Fig 3.13 below. The design implementation with data is shown in Fig 4.11.

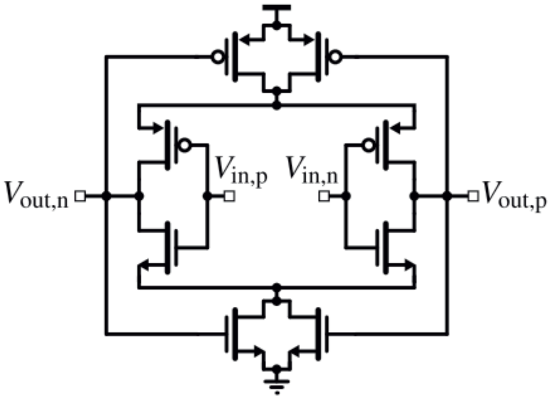


Figure 3.12: Designed amplifier schematic from the paper [7]

3.7 Comparator

The comparator is a crucial part of the SAR ADC design. It compares the instantaneous value of two analog inputs and generates a digital output. A simple approach to designing a comparator is to design a high-gain amplifier with differential analog input and single-ended large swing output. These are also called 'open-loop comparators'. The minimum voltage difference is decided by the converter's resolution. A high resolution in a very small $V\_\delta(min)$, thus a high gain amplifier is required. However, a higher gain amplifier leads to a smaller cutoff frequency. As the cut-off frequency decides the setting time of the comparator, the converter will be slower due to the smaller cut-off frequency. To overcome this lower gain stages are cascaded to broaden the operation frequency but at the same time larger input-referred offsets are introduced. A more common way is to design a latched comparator.

3.7.1 Latch-only comparator

Latched comparators make use of the combination of amplification and positive feedback. They work in a discrete-time domain rather than a continuous-time domain. In the reset phase (latch is low) the comparator tracks the inputs; in the regeneration phase (latch is high) the positive feedback starts work and the comparator generates a digital output based on the sign of the input difference.

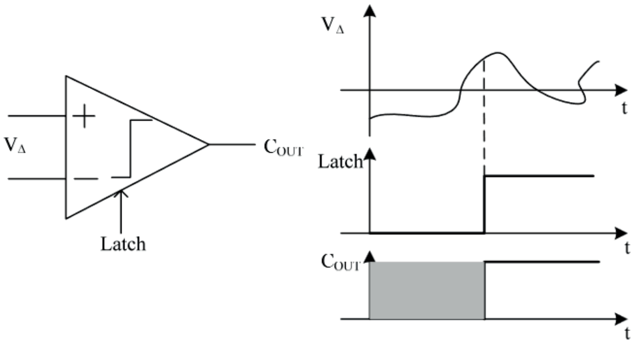


Figure 3.13: Operation of latch [24]

The figure below shows the circuit schematic of a latch comparator. During the reset phase(RST low), nodes V_{o+} and V_{o-} are pre-charged to V_{dd} by M5/M6. When RST goes high, the comparison starts V_{o+} and V_{o-} discharge the output capacitance with unequal rates due to the different input voltages. When one of the nodes is lower than V_{dd}-V_{thp}, the cross coupled PMOS transistors M3/M4 are activated, allowing V_{dd} to fully charge one of the output capacitances. The output inverters are for signal recovery. It is important to note that M7 works as a bias transistor. It consumes power during the whole comparison. Due to the mismatch of the transistors, high input referred offset voltage directly adds to the total ADC offset. A more power efficient approach is to design a dynamic latched comparator, which only consumes the power during the regeneration phase.

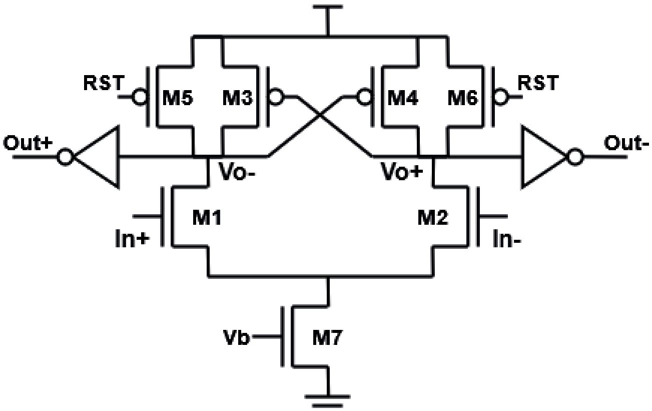


Figure 3.14: Design of latch comparator

3.7.2 Combining Pre-Amplifier and Latch

Though the latch comparators provide fast speed and low power they suffer from high input offset error which makes them unattractive to designs requiring small input differences. An optimal solution combining a pre-amplifier and a latch is employed to compromise the situation. The offset is attenuated by the gain of the pre-amplifier as shown in the below equation.

$$\sigma_{os\_total} = \sqrt{\sigma^2_{os\_amp} + (\sigma^2_{os\_latch}/A^2_{v\_amp})} \qquad (3.12)$$

The pre-amplifier can be a conventional one stage differential amplifier with NMOS input pair and PMOS resistive load. This provides sufficient gain to attenuate the error. The implemented latch comparator design in discussed in coming chapters.

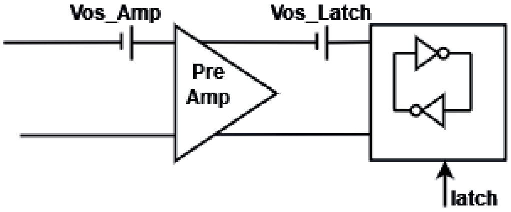


Figure 3.15: PreAmp with latch

3.8 SAR Logic Block

The SAR Logic Block is the brain of the design. It controls the entire conversion process. The block stores the output digital value of the analog input equivalent value and also generates the switching signals required for the DAC at the correct intervals to get the conversion done at the right time for the right level of values. In the thesis, the whole block of the SAR logic is realized in Verilog-A.

The design of the logic block can be divided into four stages.

Initialization: Here we will be resetting all the registers and counters.

Sampling: Here signals for the sampling process are generated and the top plate of the capacitor is charged to analog input voltage and the bottom plate is charged to V_{cm}.

Bit-by-bit conversion: The logic block controls this process starting with the most significant bit (MSB) and proceeding to the least significant bit (LSB). For a 13-bit SAR ADC, this process involves 13 iterations where each iteration determines whether the current bit has to be set to 1 or 0 based on the sampled voltage levels which are compared using a comparator.

Final digital code: After all 13 bits have been determined through the successive approximation process, the logic block assembles them into the final digital output code.

Detail explanation

The clock has been divided into 16 clock cycles. Where the thirteen-bit conversion and the top and bottom plate sampling are carried out at each clock cycle.

The SAR Logic block designed from the Verilog-A code is shown below. During the first clock cycle top and bottom sampling are done signals (*cont_sample*) and (*cont_bottom_sample*) are turned on. During the second clock cycle the bottom sampling signal (*cont_bottom_sample*) is of the difference of the voltage of the top plate and the bottom plate appears at the bottom plate of the capacitor or the input to the comparator. During the third clock cycle, top sampling (*cont_sample*) is off and a conversion start signal (*cont_conv_start*) is generated. The MSB bit code [12] is set to 1. During the fourth clock cycle, based on the comparator decision the code [12] is set to "0" or "1". If the voltage at the positive input of the comparator (compp) is greater than the voltage at the negative input of the comparator (compn) then the comparator decision is 1 (high). Once the MSB decision is made the next bit code [11] is set to one. This continues till the fifteenth clock cycle. In the sixteenth clock cycle, the last bit is set to "1" to "0". After which a ready signal is generated and then the digital data is stored in the registers.

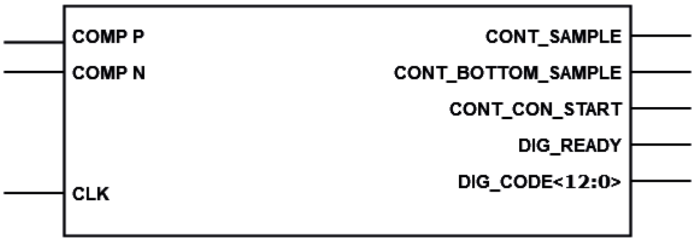


Figure 3.16: Logic block designed from Verilog code

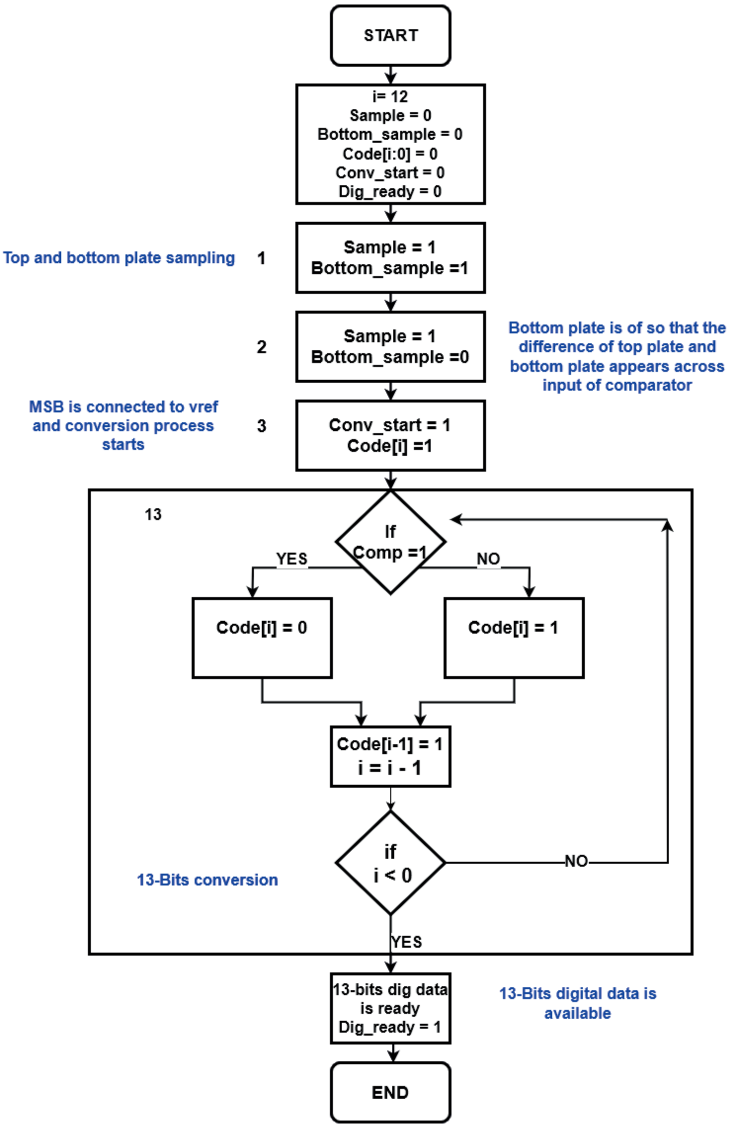


Figure 3.17: Flow chart of SAR Logic block

3.9 Noise Cancellation

As discussed initially SAR ADC consists of a capacitor array, a comparator, and a SAR logic. The capacitor array serves as the sample and hold circuit and also the DAC forms the input capacitor of an SAR ADC. SAR ADC achieves superior energy efficiency and is highly compatible with technology scaling.

ADCs suffer from a fundamental SNR challenge: it's the sampling kT/C noise. To satisfy the SNR requirement, the kT/C noise is typically suppressed by increasing the input capacitor size. Large input capacitors make it very costly to design the ADC input driver. To ease the ADC input driver requirements many researchers have proposed several solutions like embedding a buffer inside the SAR ADC loop [15]-[23]. In this way, the sample and hold circuit is separated from the feedback DAC and shielded from the input by the buffer. The input capacitance of the ADC is the only input capacitance to the buffer and thus is substantially reduced, leading to a relaxed burden for the ADC input driver. Since the buffer resides inside the SAR loop its nonlinear distortions during the sampling and conversion phases cancel each other. A simple source follower can be used as a buffer. However, the buffer still needs to drive large sampling capacitors limited by kT/C noise which consumes extra power and degrades the ADC power efficiency. Using current steering DACs to feedback the conversion results is also a solution but they consume large static power. CDACs are also used to reduce the power but using the large DAC size is a huge burden to the buffer. Since the root cause of the problem is the large input capacitor. There is a need to find ways to reduce the capacitor size without incurring large kT/C noise. In the paper [1] published an effort has been made to find a way to cancel the kT/C noise. It allows us to use a much smaller input capacitor without the usual downsides of increased noise.

In the paper [1] published a tiny 240 fF input capacitor has been used. It takes up a small space. It works fast operating at a 40 MS/s. In terms of performance, the ADC design is good as it achieves a 69 dB signal-to-noise and distortion ratio. To conclude, the SAR ADC with noise cancellation technique not only solves a common noise problem but also does it in a way that makes the design simpler, smaller, and more power-efficient.

In this thesis, we are implementing this technique for our SAR ADC design to prove if this technique works and also to see if we are getting better results by using even smaller input capacitances. A typical design and its impact are shown in Fig 3.18 below.

3.9.1 How the noise cancelation work?

When signal ϕ_1 is high input voltage V_{in} is tracked on C_1. The preamp offset is amplified and stored on C_2. When ϕ_1 falls the C_1 sampling phase finishes and C_1 stores the sampled input and the kT/C_1 noise. The voltage across the capacitor during the remaining time of the operation cycle can be expressed as $V_{C1} = V_{in}(t_1) + v_{ns1}$.

When ϕ_1 falls ϕ_2 is still high. Thus the input signal sampling continues on C_2 after the preamp. The C_2 sampling finishes with a fall of ϕ_2. The voltage now at preamp input is $V_{in}(t_2)$ - $V_{in}(t_1)$ - vns_1- vos. This voltage is amplified by A times and stored on C_2. When ϕ_2 falls kT/C_2 noise vns_2 is introduced on C_2. The voltage on C_2 after falling of ϕ_2 is $V_{C2} =$ A[$V_{in}(t_2)$ - $V_{in}(t_1)$ - v_{ns1}- v_{os}] $+ v_{ns2}$.

After ϕ_2 falls, the SAR conversion starts the digital codes are fed to the bottom plate of the DAC(i.e. the left-hand side of C_1) and the SAR logic attempts to bring the right-hand side of C_2 to zero. Ignoring other circuit non-idealities the final digital output can be found to be $D_{out} = V_{in}(t_2) + v_{ns2}/A$. We can see that the kT/C_1 noise v_{ns1} is canceled and does not exist in D_{out}. Thus C_1 can be made arbitrarily small but without incurring kT/C_1 noise penalty. The kT/C_2 noise v_{ns2} is suppressed thus permitting the use of small C_2.

Generalising noise cancelation

After ϕ_1 falls, the input of amplifier A is

$$V_{in,Amp}(t_2) = V_{in}(t_2) - V_{in}(t_1) - v_{ns1} - V_{os} \tag{3.13}$$

When ϕ_2 falls $V_{in,Amp}(t_2)$ is multiplied by A and stored on C_2 together with kt/C_2.

At the comparator input, during the conversion phase

$$V_{comp,in} = A[V_{DAC} - [(V_{in}(t_1) + v_{ns1}) + V_{os}]] - A[[V_{in}(t_2) - V_{in}(t_1) - v_{ns1} - V_{os}] + v_{ns2}] \tag{3.14}$$

$$V_{comp,in} = AV_{DAC} - AV_{in}(t_1) - v_{ns2} \tag{3.15}$$

$$V_{comp,in} = A[V_{DAC} - V_{in}(t_2) - (v_{ns2}/A)] \tag{3.16}$$

v_{ns1} disappears. This means we can have a small C_1, which can be driven by a power-efficient buffer. C_2 can be small too, since its noise is suppressed by the amplifier gain.

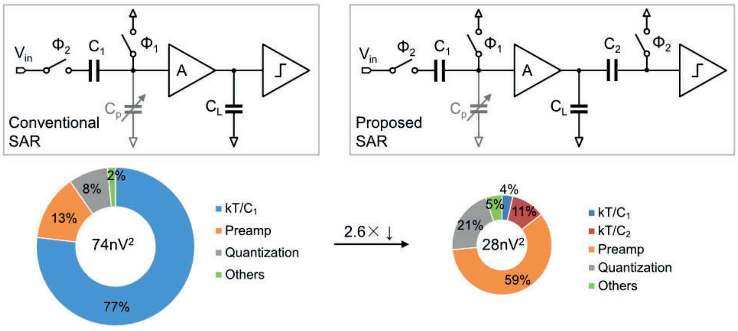


Figure 3.18: Noise summary and design comparison of SAR ADCs with and without kT/C noise cancellation [1]

Chapter 4

Implementation

4.1 SAR ADC Block Diagram of the Design

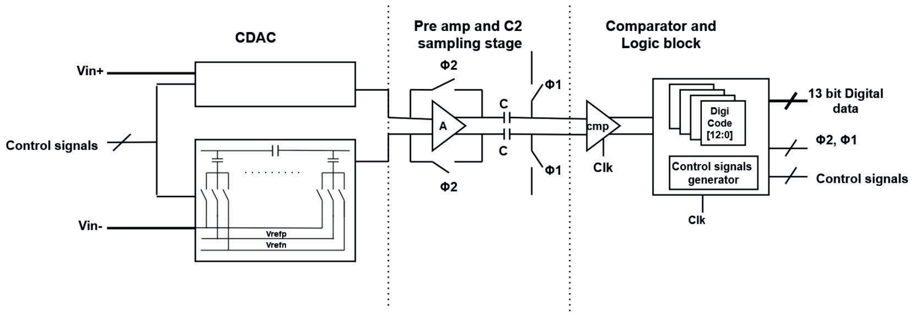


Figure 4.1: SAR ADC Block Diagram.

A basic block diagram of the SAR ADC designed for the thesis is shown in above Fig 4.1. A typical SAR ADC should have a CDAC, comparator and logic block. The only change to the architecture is the addition of the noise cancellation block shown in figure above. The logic block has been designed from verilog-A code. The CDAC has been implemented in split capacitor architecture. The comparator designed is a latched comparator with pre-amp. A separate CMFB amplifier has been designed which is part of the noise cancellation block. Tnasmission gate switches are used to control vrefp, vrefn, feedback of the amplifier and also for the sampling stage in the noise cancellation block as shown in block diagram. Bootstrapped switch is used to control the input signal. External clock of 640 MHz is used for the comparator and logic block. All the control signals for the switches are generated by the logic block. Going further in the section we will study and learn in detail about every block in the block diagram.

4.2 CDAC

Two CDACs have been designed where one is connected to the positive terminal of the pre-amp and the other to the negative terminal of the pre-amp. The inputs to CDAC are Vin, vrefn, vrefp, Vcm and control signals. The output of the CDAC is connected to the input of the pre-amp. All control signals like $\phi 1(control\_bottom\_sample)$, $\phi 2$ $(control\_sample)$ and other control signals shown in Fig 4.4 below are all generated from the logic block. Control signals code and code_b which control the switches for vrefp and vrefn are generated as shown in Fig 4.3. Once the $control\_sample$ signal is low the conversion process starts and the $cont\_conv\_start$ is high. The signal then along with the digital output is used to generate the signals to control the switches for vrefp and vrefn.

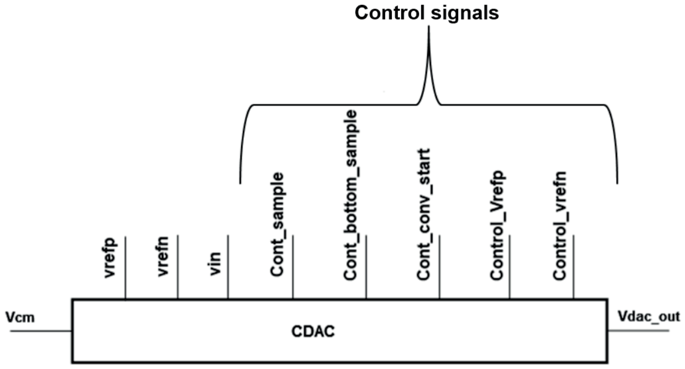


Figure 4.2: CDAC cell

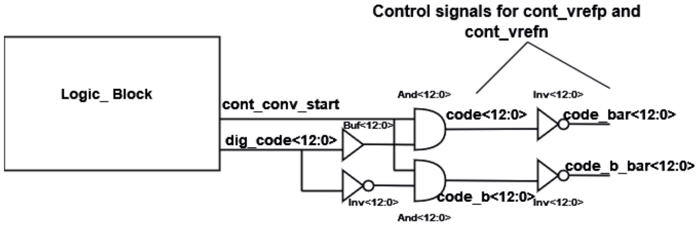


Figure 4.3: Control switches for reference voltage switches

The designed CDAC has been converted to a CDAC cell as shown in Fig 4.2 to which all the control signals are connected to control the sampling and conversion process.

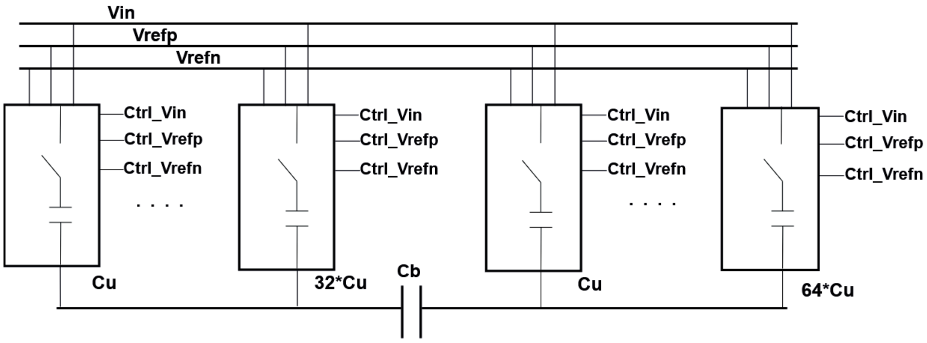


Figure 4.4: CDAC split arrangement

The split CDAC design was introduced to reduce the area of the SAR ADC. The binary-weighted DAC is converted into two sub-DACs with a total capacitance of $2^7$and 2^6 which are connected by a bridge capacitor C_b. Using the split capacitance method the total capacitance can be reduced from $2^N * C_u$ to $(2.2^{N/2} * C_u)$

To calculate the bridge capacitance $C_b = [(2^{0.5N}){*}C_u/(2^{0.5N}{-}1)]$ formula is used. Substituting $N = 13$ and $C_u(unitcapacitance) = 5fF$ we get $C_b = 5fF$. The schematic of the structure is shown in Fig 4.4 above.

4.3 Switch Cell and Switches

The rectangular blocks we see in the split CDAC is shown below in Fig 4.5. As one can clearly see we have pins for the control signals of the three signals vin, vrefn and vrefp. Vtop and Vbottom pins are just used to analyze the voltage levels at the top and bottom plate of the capacitor and the Vbottom is connected to the input of pre-amp. For pins ctrl_vrefp and ctrl_vrefn control signals code and code_b signals are connected for the DAC connected to the positive input of the comparator and the control signals code and code_b are reversed for the DAC connected to the negative input of the comparator.

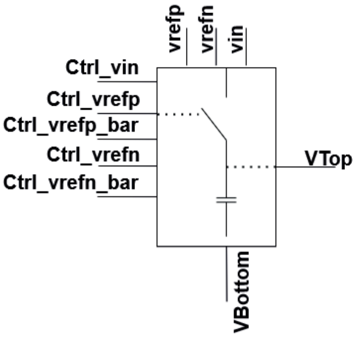


Figure 4.5: Cell.

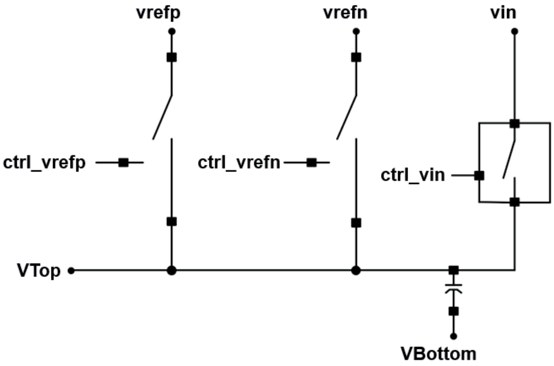


Figure 4.6: Switch connection in a cell.

Each cell block contains a switch arrangement as shown in the Fig 4.6 above. CDAC is one of the main blocks in a SAR ADC. In the design a transmission gate switch as shown in Fig 4.7 has been used which is sized accordingly such that the DC voltage applied at the input is equal to the DC voltage at the output. The transmission gate switches are used for vrefp and vrefn. The control signals used to control the flow of vrefp and vrefn are connected in place of the clk and clk_bar as shown below. A bootstrapped switch shown in Fig 4.8 is used for the input as it reduces the loss during switching. It uses a capacitor to supply additional voltage to the gate and also achieves a low ON resistance. The bootstrapped is used for input sampling because the input is varying and the bootstrapped switch provides better stability when compared to the transmission gate. The output of all three switches is connected to the top plate of the capacitor and the bottom plate is connected to the input of the capacitor.

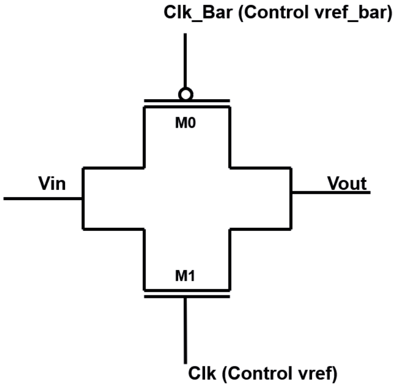


Figure 4.7: Switch connection in a cell.

name	Type	value	unit
M0	width	3	μm
	length	60	nm
M1	width	1	μm
	length	60	nm

Table 4.1: Design data of Transmission gate

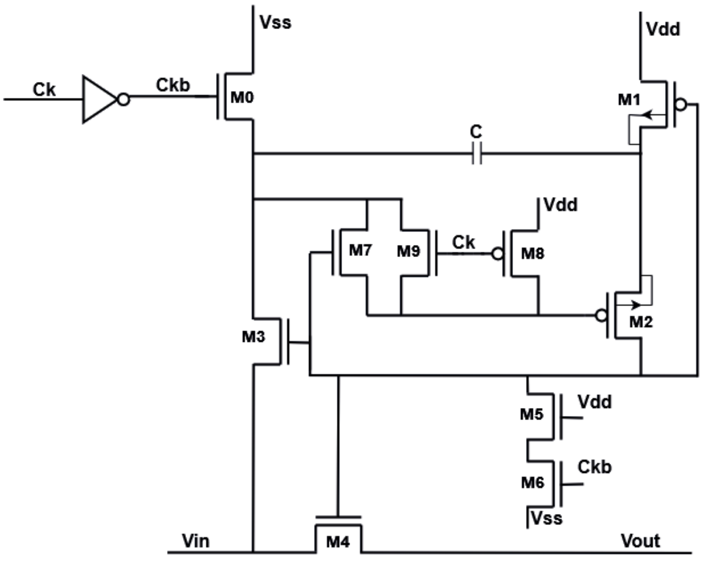


Figure 4.8: Bootstrapped switch designed in Thesis

name	Type	value	unit
M1/M2/M3/M0/M7/M8/M9/M6/M5/M11	width	0.4	μm
	length	60	nm
M10	width	0.8	μm
	length	60	nm
M4	width	4	μm
	length	60	nm
C0	value	19.47	fF

Table 4.2: Design data of Bootstrapped circuit

4.4 Comparator

As discussed initially comparator plays an important role in comparing the voltage levels of both the DAC outputs. The following configuration of the dynamic comparator is chosen because it gives the lowest offset voltage and high output drive load capability. This architecture of the comparator consists of a regenerative latch and a couple of inverters. The inverters help in keeping the rise time and fall time sharper which leads to making the comparator being used at higher speeds. The comparator's input stage and the output latch stage are separated from each other so that they can be able to work at a lower supply voltage and have stable offset voltage. This design also has two additional inverters apart from the general conventional architecture to strengthen the regenerative nodes so that the comparison speed is relatively much faster than the conventional one.

When the clock signal is low the PMOS transistors connected to the input stage get turned on and it leads to the charging of the drain nodes to V_{dd} which in turn leads to the activation of the PMOS transistors present at the regenerative latch leading to pre-charging the transistors to the supply voltage level. But at the same time, the NMOS transistors get pre-charged to ground level.

During the regenerative phase, the decision of the comparator's result is made. In this mode, the clock signal gets high and the nodes that got precharged to the V_{dd} level during the reset phase get discharged at the rate of the input voltages according to its input level. If the input voltage level to the PMOS at the input stage gets reduced below V_{dd}-p, then the PMOS present between the input stage and the regenerative stage gets switched on this leads to the turning on of the NMOS transistors at the regenerative latch which helps regenerate the input difference to the full-scale voltage level. The designed comparator is shown below in Fig 4.9.

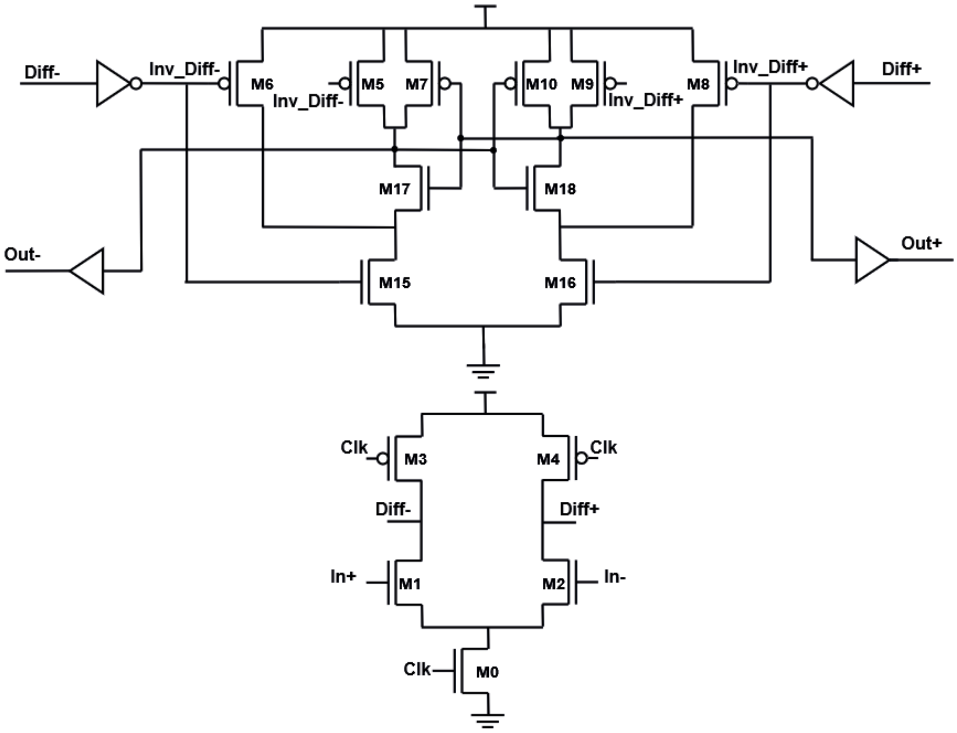


Figure 4.9: Comparator designed in thesis

name	Type	value	unit
M5/M7/M10/M19	width	7	μm
	length	60	nm
M6/M8	width	0.135	μm
	length	60	nm
M12/M11/M1/M2	width	10	μm
	length	60	nm
M14/M13	width	5	μm
	length	60	nm
M17/M18/M15/M16	width	2	μm
	length	60	nm
M1/M2	width	3	μm
	length	60	nm
M3/M4	width	1	μm
	length	60	nm

Table 4.3: Design data of Comparator circuit

4.5 Amplifier

name	Type	value	unit
M1/M4	width	15	μm
	length	60	nm
M2/M3	width	25	μm
	length	60	nm
M0/M7	width	40	μm
	length	60	nm
M5/M6	width	10	μm
	length	60	nm
C$_L$	Value	100	fF

Table 4.4: Design data of Amplifier

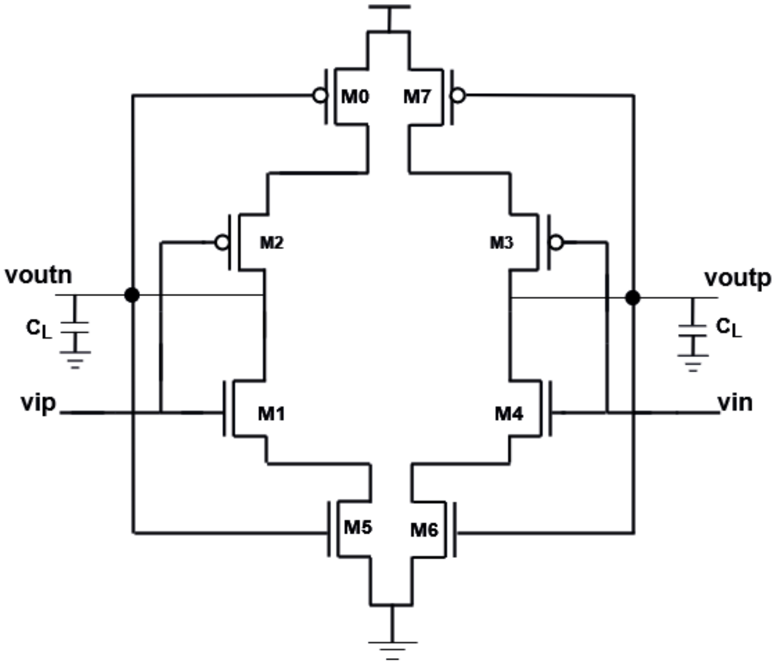


Figure 4.10: Pre Amplifier designed in thesis

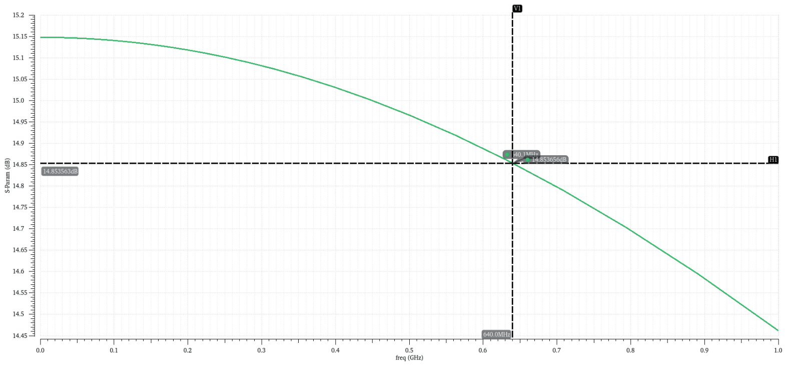


Figure 4.11: Gain of the Amplifier

Inverter-based common mode feedback amplifier has been designed for a gain of around 15 dB in the Thesis.

Chapter 5

Verification of SAR ADC noise cancellation technique

An efficient FFT analysis is crucial for the entire system and for achieving this, one must adhere to coherent sampling. Failing to follow this process introduces a significant challenge of spectral leakage, impacting the overall SNR of the system. Coherent sampling mitigates spectral leakage, which occurs when the energy from a signal spreads into adjacent frequency bins. By maintaining coherence, the FFT analysis is more accurate, and spectral components remain well-defined. Ensuring the sampled waveform is coherent preserves the integrity of the original signal. It is crucial in applications where precision and accuracy are paramount. Coherent sampling contributes to improved frequency resolution in FFT analysis. The uniform distribution of samples allows for a more detailed examination of the frequency content of the signal. Following coherent sampling helps avoid aliasing issues. Aliasing occurs when higher-frequency components are incorrectly interpreted as lower frequencies, leading to inaccuracies in the analysis.

Coherent sampling can be explained as shown $F_{in} = (M * F_s)/N$ where Fin is input frequency, M is a prime number which indicates the chosen number of periods of input signal for the computation of FFT, N is number of FFT points chosen and F_s is the sampling frequency. In this section, we will be discussing the simulations we undertook on Cadence Virtuoso and also discuss in detail their outcomes. The below table depicts the data used for the simulations.

Name	Value	Unit	Variable
Sampling Frequency	40M	Hz	**fsamp**
Sample points	128/256/512/**[1024]**		**nsamp**
Frequency resolution	39.06 K	Hz	**fres**=(fsamp/nsamp)
Clock Frequency	640 M	Hz	**fclk** = (fsamp*16)
Input Siganl Frequency	0.117 M	Hz	**fsig** = (fres* 3)
Amplitude	1.2	V	**Vin**
Common mode voltage	0.6	V	**Vcm**

Table 5.1: Data used for simulations

5.1 13 bit SAR ADC

Without Noise Cancellation

The thesis was designed initially from ideal blocks. Started designing an ideal SAR ADC with an ideal CDAC, ideal comparator, and logic block. Once the ideal SAR ADC was working fine the ideal blocks were replaced with non-ideal blocks one at a time to make sure they worked properly. They were replaced with the circuits shown in the previous section. For a sampling frequency(F_s) 40MS/s, input frequency (F_{in}) 117.1875 KHz, and unit capacitance (C_u) 12 fF the dynamic characteristics of SAR ADC are measured. SNDR = 70.55 dB, SFDR = 89.37 dBc, and ENOB = 11.42 are obtained. Noise contributions from all the blocks are considered.

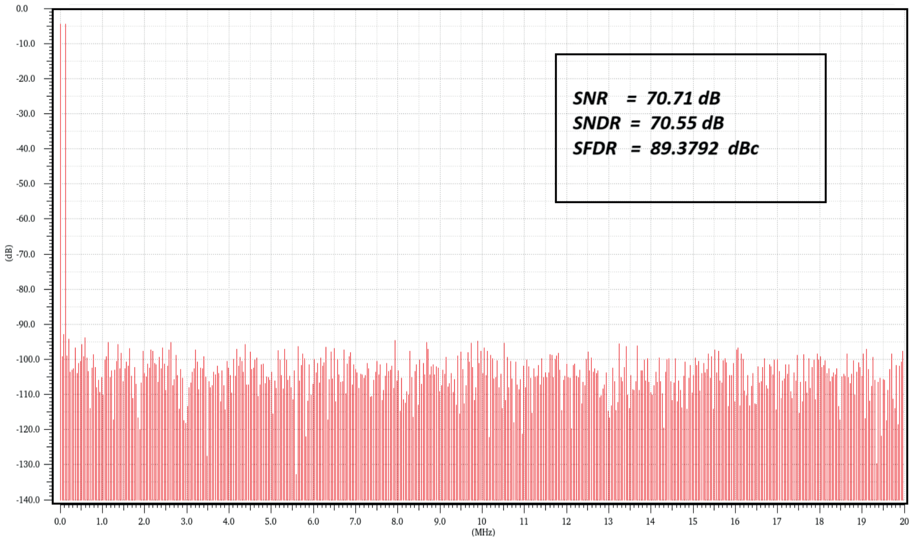


Figure 5.1: 13-Bit SAR ADC without NC

With Noise Cancellation

The whole point of conducting the thesis is to implement the kT/C noise cancellation technique. The pre-amplifier and the C_2 sampling stage were designed (shown in Fig 4.1) and introduced to the design between the CDAC and comparator to cancel the kT/C noise. After the noise cancellation block was introduced, there was some improvement in the dynamic characteristics for the same configuration. SNDR = 75.36 dB, SFDR = 92.0 dBc and ENOB = 12.22. Noise contributions from all the blocks are considered.

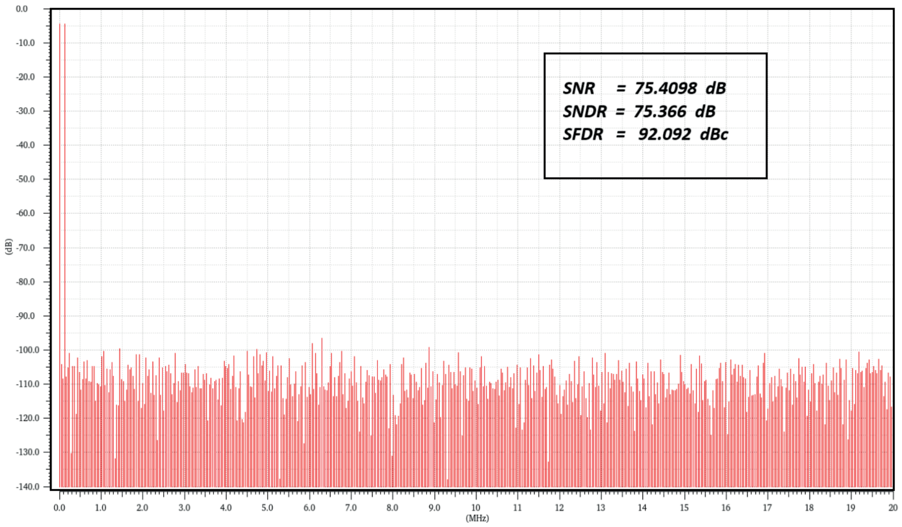


Figure 5.2: 13-bit SAR ADC with NC

5.2 13-Bit SAR ADC for C$_u < 1fF$

As mentioned in previous sections. The purpose of implementing noise cancellation is that one can use a small unit capacitance and expect better performance (improvement in SNR/ SNDR). When the unit capacitance is very low, the only problem is the increase in kT/C noise as they are inversely proportional. This increase in kT/C decreases the overall performance (SNR) of the SAR ADC. Hence the kT/C noise cancellation has been introduced to remove the excess kT/C noise and also hopefully achieve better performance (SNR) for small unit capacitances. Using smaller capacitances also decreases the overall area of the design. Keeping this in mind, multiple simulations have been done for different unit capacitance values between 0.5 fF and 1 fF, and the results have been discussed below.

Fig 5.3 shows SNR and SNDR variation for different values of capacitance before adding the noise cancellation block. The SNR and SNDR must gradually increase with the increase in the unit capacitance but in the given figure the SNR and SNDR are higher for 0.75 fF it could be because of the C_2 (shown in Block diagram Fig 4.1) is set high. Generally, the load capacitance of the amplifier and the C_2 capacitor must be 150 fF combined.
In Fig 5.4 SNR and SNDR variation for different values of capacitance after the addition of a noise cancellation block. As expected the SNR and SNDR increase with the increase in unit capacitance. There is approximately 4 dB gain in SNR when we compare the data given in both plots. This shows that from the implemented noise cancellation there is some improvement in the ADCs performance, SNR in this case.

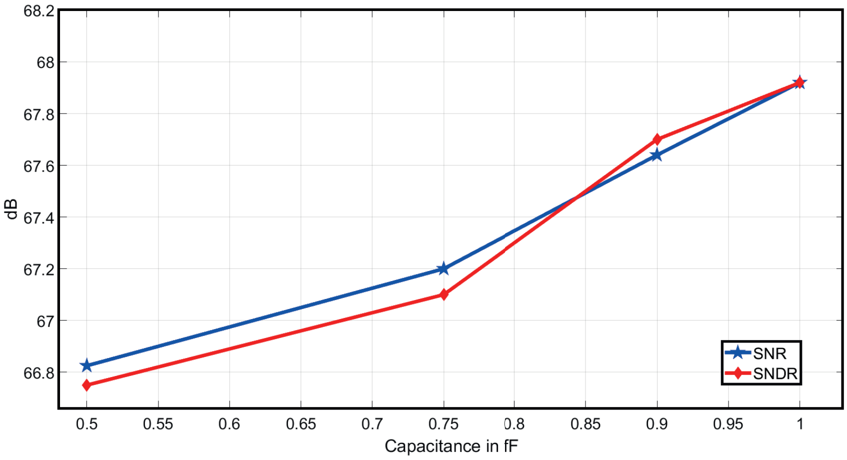


Figure 5.3: SNR, SNDR vs Capacitance without noise cancellation

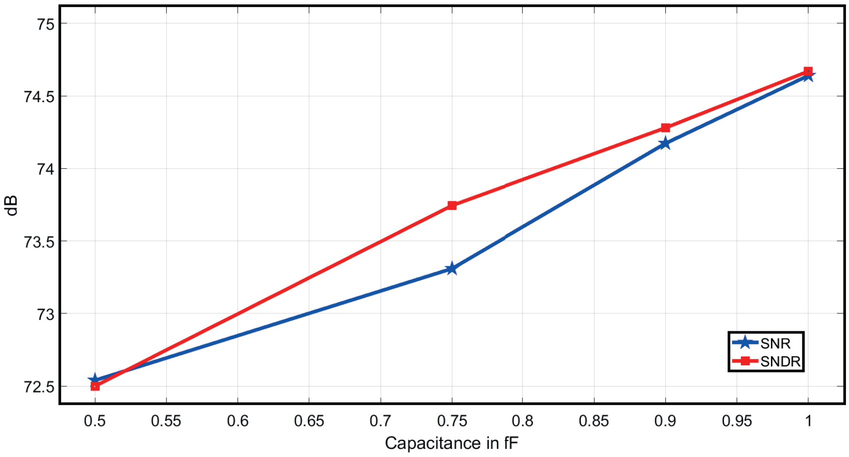


Figure 5.4: SNR, SNDR vs Capacitance with noise cancellation

Fig 5.4 given below depicts the variation in ENOB for different values of capacitance. From the plot, it is clear that the ENOB is better after the noise cancellation block is added to the SAR ADC. In some cases, there is a gain of close to a bit in ENOB.

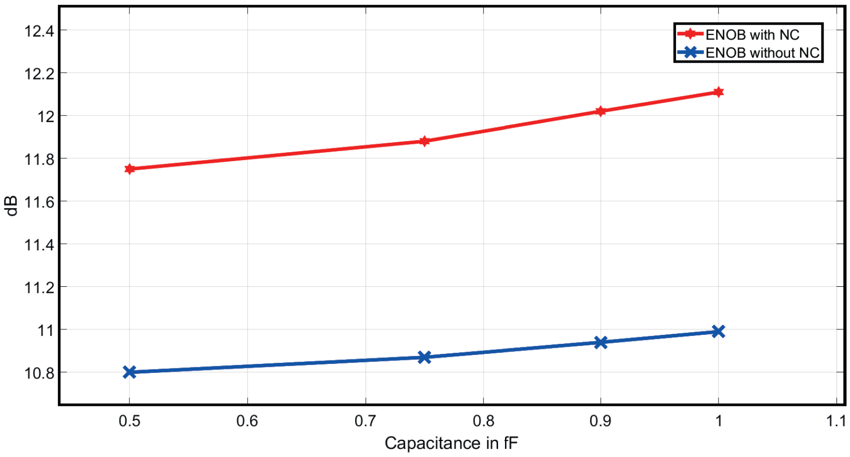
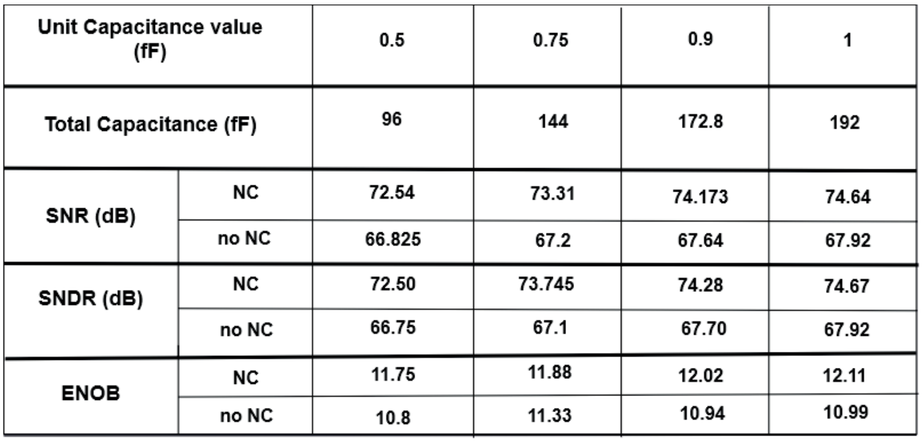


Figure 5.5: ENOB with and without noise cancellation

5.2.1 Summary



Unit Capacitance value (fF)		0.5	0.75	0.9	1
Total Capacitance (fF)		96	144	172.8	192
SNR (dB)	NC	72.54	73.31	74.173	74.64
	no NC	66.825	67.2	67.64	67.92
SNDR (dB)	NC	72.50	73.745	74.28	74.67
	no NC	66.75	67.1	67.70	67.92
ENOB	NC	11.75	11.88	12.02	12.11
	no NC	10.8	11.33	10.94	10.99

Figure 5.6: Summary of all the simulations conducted

5.3 13-bit SAR ADC with no noise contributions from the comparator

This simulation was conducted to see how much contribution other blocks contribute other than the CDAC. So the noise contributions from the comparator were turned off to see the difference in SNR in both cases i.e. with and without a noise cancellation block. The results are as shown below in table 5.3. There is not much of a difference in SNR for the noise cancellation technique with and without noise contribution from the comparator. Whereas we can see a 2 dB difference in SNR for SAR ADC with no noise cancellation technique. From this, one can conclude that implementing the noise cancellation technique also reduces the noise from the comparator.

Capacitance value	SNR (dB)	SNDR (dB)
0.9 no NC and with contribution from comparator	67.6400	67.70
0.9 no NC and no contribution from comparator	70.19	70.099
0.9 NC and with contribution from comparator	74.1732	74.2874
0.9 NC and no contribution from comparator	74.6300	74.8500

Table 5.2: SNR variations with no contribution from comparator

5.4 With and without noise contribution from CDAC

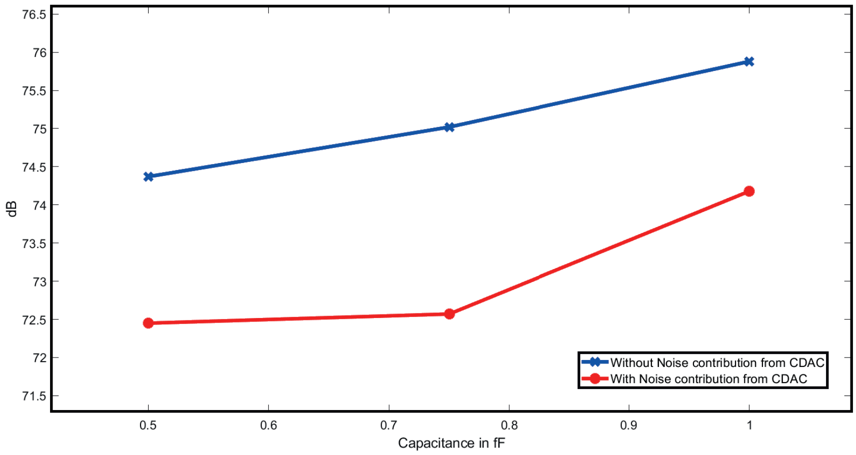


Figure 5.7: With and without noise contribution from CDAC

From these simulations we can know what should be SAR ADC in ideal scenario. By not considering the noise contributions from CDAC we can say that the kT/C noise is absent as CDAC is the main source for the kT/C. A comparison table has been given below SNR with considering noise from CDAC and without considering noise from CDAC.

Capacitance value	SNDR without Noise from CDAC (dB)	SNDR with Noise from CDAC (dB)
0.5	74.37	72.45
0.75	75.02	72.57
1	75.88	74.1799

Table 5.3: SNR variations with no contribution from comparator

From the results it is very clear that though we are not completely cancelling the kT/C noise there is definitely some improvement in SNR with noise cancellation technique architecture when compared with without noise cancellation technique from previous section.

5.5 Performance at Nyquist i.e F$_{in}\approx$ F$_s/2$

When $F_{in} \approx F_s/2$ the SAR ADC architecture without noise cancellation performs as expected giving an SNDR = 67.62 dB and ENOB = 10.93 and for the SAR ADC architecture with noise cancellation technique a decline in performance can be seen. The SNDR = 52.45 dB and ENOB = 8.42. The input frequency (F_{in}) is set to 18.67 MHz which is approximately half of the sampling frequency (F_s).

The fact that the SAR ADC architecture works fine without the noise cancellation block make us believe that the designed noise cancellation block must be the reason for the decrease in performance. After investigating we could see that there is attenuation of the signal between the comparator and the C_2 sampling stage.

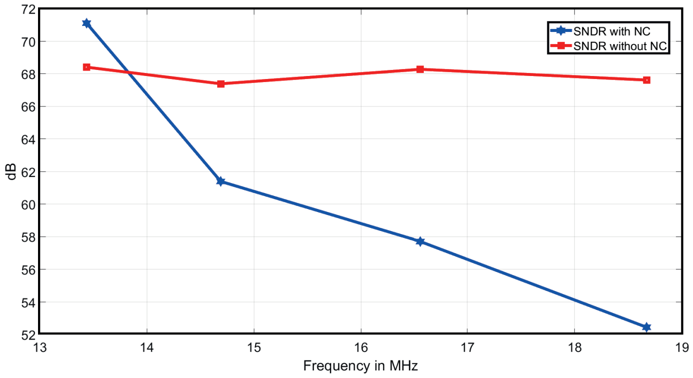


Figure 5.8: SNDR vs Input frequency (F$_{in}$)

Input frequency (MHz)	SNDR (dB)	SNR (dB)	ENOB
13.4375 (NC)	71.1068	72.29	11.51
13.4375 (no NC)	68.41	68.41	11.07
14.69 (NC)	61.399	67.91	9.90
14.69 (no NC)	67.39	67.37	10.90
16.56 (NC)	57.71	64	9.29
16.56 (no NC)	68.28	68.48	11.04
18.67 (NC)	52.45	58.91	8.42
18.67 (no NC)	67.62	67.58	10.93

Table 5.4: SNR and SNDR for different values of input frequency

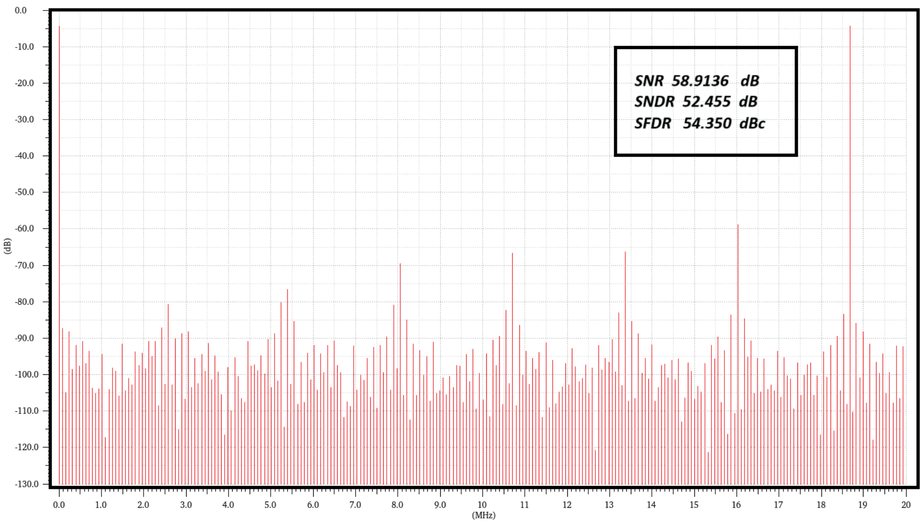


Figure 5.9: Spectrum of F_{in} ≈F_s with NC technique

Fig 5.8 depicts a lot of distortions in the spectrum which is causing the decrease in performance. Increasing the capacitance C shown in Fig 4.1 between the comparator and pre amplifier will reduce the attenuation of the signal after amplification. But there are chances that this might degrade the kT/C noise cancellation and it might not work. As shown below Fig 5.9 there is improvement in the performance although there is a lot of distortion that is still affecting the performance of the system as the SNDR is very low. The performance improvement was seen after increasing the capacitance value from 100 fF to 350-400 fF.

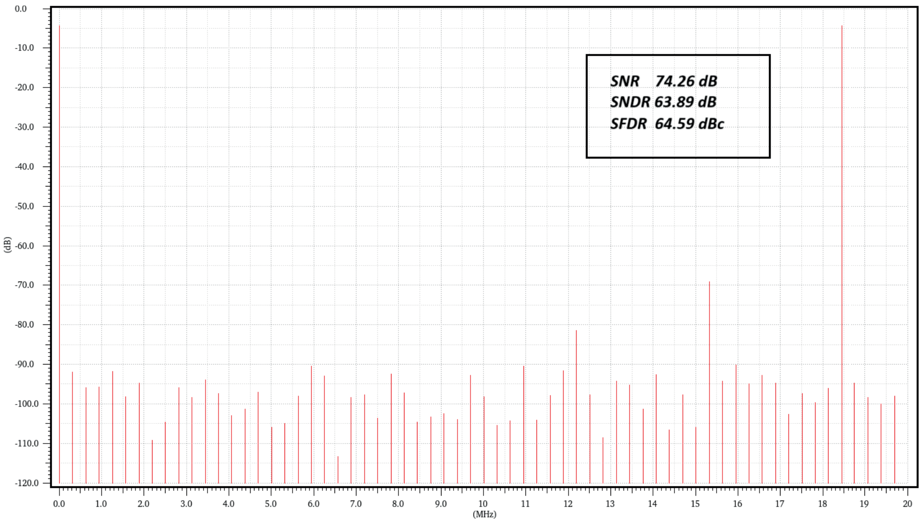


Figure 5.10: Spectrum of F_{in} ≈F$_s$ after increasing the Cap in noise cancellation block

5.6 Variation of SNDR for different sampling frequencies

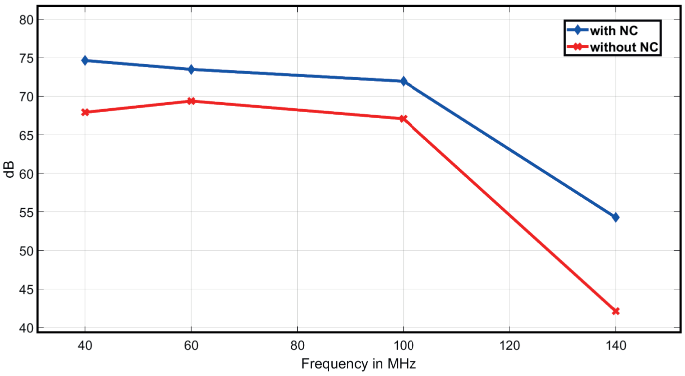


Figure 5.11: SNDR vs sampling frequency (f$_s$)

For frequencies less than 100 MHz the SNDR has no huge variations. The unit capacitance is 1 fF. There is also improvement seen in SNDR with the noise cancellation technique shown blue graph. Using a 100 MHz sampling frequency forces us to use a 1.6 GHz clock which is very fast. But the fact that the SAR ADC designed is working fine for a clock frequency of 1.6 GHz is a good sign. The performance starts depleting after the sampling frequency crosses 100 MHz. The designed SAR ADC with noise cancellation can be used for higher sampling rates up to 100MHz successfully.

Sampling Frequency (MHz)	SNDR (dB)	SNR (dB)	ENOB
40 (NC)	74.67	74.64	12.11
40 (no NC)	67.92	67.92	10.99
60 (NC)	73.49	73.37	11.91
60 (no NC)	69.07	69.38	11.18
100 (NC)	71.95	72.11	11.65
100 (no NC)	67.08	67.45	10.84
140 (NC)	54.27	54.78	8.72
140 (no NC)	42.106	44.318	6.70

Table 5.5: SNR and SNDR for different values of sampling frequency

5.7 Power consumption

Although designing the SAR ADC for a low power was not our main objective. It is important to calculate the power consumption as a new noise cancellation block has been added to the SAR ADC architecture that has an amplifier. Wanted to see how much power the SAR ADC design consumes with and without the noise cancellation block. After running simulations for SAR ADC with and without noise cancellation it is observed that the SAR ADC without noise cancellation consumes approximately 1.5 mW power whereas the SAR ADC with noise cancellation consumes approximately 2.425 mW power. This is for the overall design which includes switches, comparator, pre-amplifier, input, and reference. The FOM for those with noise cancellation is 13.7 fJ/conversion step and for those without noise cancellation is 18.4 fJ/conversion step. This shows that the power is spent well in the SAR ADC with noise cancellation technique. The formula to calculate FOM is given below

$$FOM = Power/2^{ENOB} * F_s \tag{5.1}$$

	with NC	without NC
Power (mW)	≈ 2.42	≈ 1.5
FOM (fJ/conversion-step)	13.7	18.4

Table 5.6: Power and FOM for the designed SAR ADC with and without NC

Chapter 6

Conclusion

In this thesis project, a 13 bit 40 MS/s SAR ADC architecture is successfully implemented with and without the noise cancellation technique. Every blocks have been individually studied and have been successfully implemented. As defined in objective the noise cancellation has been successfully implemented and has been verified for low input capacitance.

The comparator plays a crucial role in data conversion system. A dynamic latch comparator is chosen for its low power consumption, though it generates a lot of kick back noise which deteriorates the input. The noise cancellation technique also plays an important role in cancelling this kick back noise as shown in section 5.3. The designed comparator also works well for high clock frequencies up to 2.2 GHz and may be even higher.

Switches are also a main concern when we started. For an NMOS or PMOS switch the on resistance is changed as a function of reference voltage. The transmission gate is valued for its consistently stable on-resistance and effective cancellation of charge injection and also the bootstrap switches are preferred for input as they maintain constant voltage across gate and hence maintaining constant on resistance. A performance degradation can be seen for frequencies close to Nyquist. As a future work the bootstrap can also be designed efficiently for higher frequencies.

If the challenge is to implement the noise cancellation technique for low power and also lower area replacing the conventional switching scheme with merged capacitor switching (Vcm based switching will reduce the area and also power consumption. Have implemented both binary weighted and split capacitor CDAC architecture. The SAR logic is also successfully implemented using verilog-A in Cadence.

The kT/C noise cancellation block seems to be successfully working as we are getting a better SNR after implementing the noise cancellation block. Also managed to get decent results for a total unit capacitance of 172.8 fF which is very less input capacitance. Since we are getting better results and improvement in SNR after implementing the noise cancellation technique, we can conclude that the noise cancellation technique works fine and it can be a huge developement in this domain considering one can implement higher bits using less input capacitance and also obtain decent SNR.

Future work , as discussed in previous paragraphs designing the SAR ADC with other switching schemes to reduce the power consumption. Improving the design of the pre-amp which is part of the noise cancellation block. There is also scope for improving the comparator designed.

Chapter 7

Appendix

7.1 SAR LOGIC BLOCK CODE

```

// VerilogA for SAR_ADC, sar_logic, veriloga

`include "constants.vams"
`include "disciplines.vams"

module sar_logic_13bit_2input(clk, compp,compn,cont_sample, cont_bottom_sample, ...
    cont_conv_start,  dig_code, dig_ready);

inout clk;
electrical clk;
inout compp;
electrical compp ;
inout compn;
electrical compn ;
inout cont_sample ;
electrical cont_sample ;
inout cont_bottom_sample ;
electrical cont_bottom_sample ;
inout cont_conv_start;
electrical cont_conv_start ;
inout [12:0] dig_code ;
electrical [12:0] dig_code ;
inout dig_ready ;
electrical dig_ready ;

parameter real vh = 1.2 ;
parameter real vl = 0 ;
parameter real tr = 10p ;
parameter real tf = 10p ;

integer state ;
integer i ;
integer comp_decision ;
integer code[12:0];
integer sample ;
integer bottom_sample ;
integer conv_start ;
integer ready ;
analog begin
@(initial_step) begin
state = 0 ;
sample = 0 ;
bottom_sample = 0 ;
```

```
ready = 0 ;
conv_start = 0 ;
for(i=12; i≥0; i=i-1) begin
code[i] = 0 ;
end
end
@(cross(V(clk)-(vh + vl)/2, +1))begin
comp_decision = (V(compp) > V(compn)) ? 1 : 0 ;
end

@(cross(V(clk)-(vh+vl)/2,+1)) begin
state = state + 1 ;
if(state > 16) begin
state = 1 ;
end
case(state)
1 : begin
sample = 1 ;
bottom_sample = 1 ;
conv_start = 0 ;
ready= 0 ;
end
2 : begin
sample = 1 ;
bottom_sample = 0 ;
conv_start = 0 ;
end
3 : begin
sample = 0 ;
conv_start = 1 ;
code[12] = 1 ;
for(i=11; i ≥ 0; i= i-1 ) begin
code[i] = 0 ;
end
end
4 : begin
code[12] = (comp_decision == 1 ) ? 0 : 1 ;
code[11] = 1 ;
end
5 : begin
code[11] = (comp_decision == 1 ) ? 0 : 1 ;
code[10] = 1 ;
end
6 : begin
code[10] = (comp_decision == 1 ) ? 0 : 1 ;
code[9] = 1 ;
end
7 : begin
code[9] = (comp_decision == 1 ) ? 0 : 1 ;
code[8] = 1 ;
end
8 : begin
code[8] = (comp_decision == 1 ) ? 0 : 1 ;
code[7] = 1 ;
end
9 : begin
code[7] = (comp_decision == 1 ) ? 0 : 1 ;
code[6] = 1 ;
end
   10 : begin
code[6] = (comp_decision == 1 ) ? 0 : 1 ;
code[5] = 1 ;
end
11 : begin
code[5] = (comp_decision == 1 ) ? 0 : 1 ;
code[4] = 1 ;
end
12 : begin
```

```
code[4] = (comp_decision == 1 ) ? 0 : 1 ;
code[3] = 1 ;
end
13 : begin
code[3] = (comp_decision == 1 ) ? 0 : 1 ;
code[2] = 1 ;
end
14 : begin
code[2] = (comp_decision == 1 ) ? 0 : 1 ;
code[1] = 1 ;
end
15 : begin
code[1] = (comp_decision == 1 ) ? 0 : 1 ;
code[0] = 1 ;
end

16 : begin
code[0] = (comp_decision == 1 ) ? 0 : 1 ;
ready = 1 ;
end
endcase
end
V(cont_sample) <+ transition(sample*vh, 0, tr, tf);
V(cont_bottom_sample) <+ transition(bottom_sample*vh, 0, tr, tf);
V(cont_conv_start) <+ transition(conv_start*vh, 0, tr, tf);

V(dig_code[12]) <+ transition(code[12]*vh, 0, tr, tf);
V(dig_code[11]) <+ transition(code[11]*vh, 0, tr, tf);
V(dig_code[10]) <+ transition(code[10]*vh, 0, tr, tf);
V(dig_code[9]) <+ transition(code[9]*vh, 0, tr, tf);
V(dig_code[8]) <+ transition(code[8]*vh, 0, tr, tf);
V(dig_code[7]) <+ transition(code[7]*vh, 0, tr, tf);
V(dig_code[6]) <+ transition(code[6]*vh, 0, tr, tf);
V(dig_code[5]) <+ transition(code[5]*vh, 0, tr, tf);
V(dig_code[4]) <+ transition(code[4]*vh, 0, tr, tf);
V(dig_code[3]) <+ transition(code[3]*vh, 0, tr, tf);
V(dig_code[2]) <+ transition(code[2]*vh, 0, tr, tf);
V(dig_code[1]) <+ transition(code[1]*vh, 0, tr, tf);
V(dig_code[0]) <+ transition(code[0]*vh, 0, tr, tf);
V(dig_ready) <+ transition(ready*vh, 0, tr, tf);
end

endmodule
```

7.2 Multiplexer(MUX)

```
/ VerilogA for SAR_ADC, mux, veriloga

`include "constants.vams"
`include "disciplines.vams"

module mux(in1, in0, sel, out);
inout in1, in0, sel, out ;
electrical in1, in0, sel, out ;

parameter real vh = 1.2 ;
parameter real vl = 0 ;
parameter real tr = 10p ;
parameter real tf = 10p ;

analog begin
V(out) <+ (V(sel) > (vh + vl)/2) ? V(in1) : V(in0) ;
end

```

```

endmodule
```

7.3 D Flipflop

```
// VerilogA for SAR_ADC, dff, veriloga

`include "constants.vams"
`include "disciplines.vams"

module dff(D, clk, Q);
inout D, clk, Q ;
electrical D, clk, Q ;

parameter real vh = 1.2 ;
parameter real vl = 0 ;
parameter real tr = 10p ;
parameter real tf = 10p ;

integer data_D ;
integer data_Q ;
analog begin
@(initial_step) begin
data_D = 0 ;
data_Q = 0 ;
end
@(cross(V(clk)- (vh+vl)/2, +1)) begin
data_D = (V(D) > (vh+vl)/2 ) ? 1 : 0 ;
data_Q = data_D ;
end
V(Q) <+ transition(data_Q*vh, 0, tr, tf) ;
end


endmodule
```

7.4 DAC 13bit

```
// VerilogA for SpectreVerilog_VerA, DAC13Bit, veriloga

`include "constants.vams"
`include "disciplines.vams"
module DAC10Bit(DACOUT, RN, RP, b0, b1, b2, b3, b4, b5, b6, b7, b8, b9,b10,b11,b12, ...
    clk);
inout DACOUT;
electrical DACOUT;
inout RN,RP;
electrical RN,RP;
inout b0, b1,b2,b3,b4,b5,b6,b7, b8, b9, b10,b11,b12 ;
electrical b0,b1,b2,b3,b4,b5,b6,b7 , b8, b9, b10,b11,b12;
inout clk;
electrical clk;

real out,code,vrn,vrp;
real delay, rise,fall,thresh;

analog begin

@(initial_step) begin
delay = 10p;
```

```
rise = 5p;
fall = 5p;
thresh = 0.6;
code = 0;
end

   @(cross( V(clk) - thresh, +1 )) begin
code = 0;
    if (V(b12) > thresh) code = code + 4096;
if (V(b11) > thresh) code = code + 2048;
if (V(b10) > thresh) code = code + 1024;
if (V(b9) > thresh) code = code + 512;
if (V(b8) > thresh) code = code + 256;
if (V(b7) > thresh) code = code + 128;
if (V(b6) > thresh) code = code + 64;
if (V(b5) > thresh) code = code + 32;
if (V(b4) > thresh) code = code + 16;
if (V(b3) > thresh) code = code + 8;
if (V(b2) > thresh) code = code + 4;
if (V(b1) > thresh) code = code + 2;
if (V(b0) > thresh) code = code + 1;
   end

out = (V(RN) + ((V(RP)-V(RN))/8096)*code);

V(DACOUT) <+ transition( out, delay, rise, fall );

end



endmodule
```

7.5 Calculations

```

SNR |dB = 10 Log  (Psign/Pnoise)

P_noise = P_Q + P_(kT/C)

Psign and Pnoise are the power of the signal and the power of the noise
in the band of interest\\

P_sin = X^2 Fs /8 = (D*2^13)^2/8

P_Q = D^2 /12$\\

D = X_FS / 2^13 \\

P_(kT/C) = (k*T)/(192*Cu)

Where
k = 1.38 * 10^-^2^3 (Boltzmann constant)
T = 300K
Cu = Unit capacitance

From the data used for simulations
D = 1.46 * 10^-4
P_sin = 0.18
P_Q= 1.8*10^-9

Considering only P_Q i.e P_(kT/C) is absent

SNR = 80dB
```

```

For
Cu = 12fF
P_(kT/C) = 1.8*10^-9

SNR = 77dB

A 3dB difference can be seen in ideal case when P_kT/C is equal to P_Q.

For
Cu = 0.75fF
P_(kT/C) = 28.75*10^-9

SNR = 67.7 dB


For
Cu = 0.5fF
P_(kT/C) = 43.125*10^-9

SNR = 66.02 dB


For
Cu = 0.9fF
P_(kT/C) = 23.9*10^-9

SNR = 68.44 dB
```

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