Cost-Effective Design Solution for GAIM Shooting Trigger PCB & Improving the Power Distribution Network

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Master's Thesis

By

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Abstract

Virtual Reality (VR) shooting simulators have gained popularity as effective training and entertainment tools. GAIM is a Swedish company specializing in VR shooting simulators, offering VR headsets with physical dummy guns and rifles. These dummy weapons contain complex electronics that are prone to compilations, especially because the Printed Circuit Board (PCB) is fitted in very compact spaces inside the weapons. Small PCB size constraints will affect various aspects such as design complexity, Radio Frequency (RF) performance, Power Integrity (PI), cost etc.

This report investigates the process of replacing an RF module (ANNA-B112) with an RF chipset (nRF52832) & discrete components (crystals, chip antenna, decoupling components etc), on the already existing PCBs inside the guns/rifles, with the basis of maintaining optimal RF performance, and significantly decrease the cost (depending on the production quantity). Power integrity analysis and simulations will be conducted for both the old and new design, with a focus on enhancing the impedance characteristics of the power distribution network (PDN).

To achieve this, various processes will be tackled. Starting with the design process, which consists of symbol/footprint creation, schematic and PCB layout design. Simulations of the PCB to optimize the power integrity (PI) with PDN impedance analysis. Once the design process is finished we move on to the manufacturing and assembly process. After the assembly we have a finished PCB with mounted components, which will be ready for RF/antenna measurements and functionality verification.

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List of acronyms

BOM   Bill Of Materials

BLE   Bluetooth Low Energy

CF   Carrier Frequency

CPU   Central Processing Unit

DUT   Device Under Test

DRC   Design Rule Check

e-CAD   Electronic Computer-Aided Design

EMC   Electromagnetic Compatibility

EMI   Electromagnetic Interference

ESD   Electro-Static Discharge

ESL   Equivalent Series Inductance

ESR   Equivalent Series Resistance

GND   Ground

GPIO   General Purpose I/O

HF   High-frequency

HFCLK   High Frequency Clock

I/O   Input/Output

LFCLK   Low Frequency Clock

LO   Local Oscillator

L1   Layer 1

L2   Layer 2

L3   Layer 3

L4   Layer 4

PCB   Printed Circuit Board

PDN   Power Distribution Network

PI   Power Integrity

PWR   Power

Rev   Revision

RF   Radio Frequency

SMD   Surface-Mounted Device

SoC   System-On-Chip

TRP   Total Radiated Power

VCO   Voltage Controlled Oscillator

VR   Virtual Reality

Popular Science Summary

Virtual Reality (VR) has transformed various industries and had a significant impact in the training arena [23]. Industries such as shooting simulators have gained popularity as training and entertainment tools. Everything from effective training for law-enforcement and military, to having a fun night with some friends in the living room hunting animals in a simulated VR world. Virtual reality aims to replicate an environment that stimulates the senses, primarily sight and sound, to create an artificial world that feels real [23].

Dummy guns and rifles with complex electronics that connect via bluetooth to the VR headset, are prone to complications with the rapid development of technology and the miniaturization of the printed circuit board (PCB). Complications such as design complexity and expensive components.

This thesis project aims to investigate a more cost-effective solution for an already existing electronics trigger device, situated in a dummy gun that is used for shooting simulations. The goal is to reduce the component cost and upgrade some electrical properties for the new PCB, while still maintaining the desired bluetooth connection with the VR headset. To achieve this, various processes will be tackled. Processes such as a full re-design of the PCB, therefore decreasing the component cost and upgrading the electrical properties. Various simulations, verifications and measurements will be systematically performed on the manufactured PCB to ensure proper functionality, and desired bluetooth connection is maintained.

1. Introduction

Virtual Reality (VR) shooting simulators have gained popularity as effective training and entertainment tools. GAIM is a Swedish company specializing in VR shooting simulators, offering VR headsets with physical dummy guns and rifles.

Figure 1.1: GAIM product, dummy gun and the trigger unit [1].

These dummy weapons contain a trigger unit with complex electronics that are prone to compilations, especially because the Printed Circuit Board (PCB) is fitted in very compact space. Small PCB size constraints will affect various aspects such as design complexity, Radio Frequency (RF) performance, power consumption, cost etc.

In order for the simulations to be operating as smoothly as possible the communication between the electronics in the trigger unit and the VR headset needs to be optimal. The communication protocol between the electronics and the VR headset are done through an RF module using Bluetooth. These RF modules are usually very expensive, and are major components that affect the profit margins, especially when the production quantity is very high. Replacing the RF module with an RF chipset and discrete components is a solution for the cost aspect, and can decrease the component cost upwards to 30%.

1.1 Project aims and challenges

The goal of this master's thesis is to re-design the PCB, by replacing the currently used RF module (ANNA-B112 [3]) with an RF chipset (nRF52832 [4]) and some discrete components. Discrete components such as, crystals (32.768kHz & 32MHz), chip antenna (2450AT18A0100001E [5]) which is a 2.4GHz surface-mounted device (SMD), matching network for the antenna that consists of capacitors and high-frequency (HF) inductors, and a bunch of decoupling components such as capacitors, inductors and resistors, making a fully functional trigger PCB for the VR shooting simulation.

1.1.1 Fitting the nRF chip & discrete components

Swapping the RF module with an RF chipset presents a major challenge in the design process. Fitting the nRF chipset and discrete components on the same PCB outline that is currently used with the ANNA module. The reason GAIM does not want to change the PCB outline is because they want to use the same mechanical parts for the trigger that are currently used in their weapons. A major goal is to find a suitable floorplan for the components to make sure all the new components fit on the same board, while following design and RF rules. A floorplan is essentially the most ideal component placement considering the board outline.

1.1.2 Cost considerations

As mentioned in the first section of the introduction, RF modules can be very expensive. Swapping the modules with discrete components might reduce the component cost upwards to 30%, which on a large production scale can have a large impact on the profit margins. However, having discrete components introduces another cost aspect. Certifications. Usually when dealing with RF modules you only need to undertake one certification ,which measures radiated emissions. However, dealing with discrete components there are two certifications that need to be done. Certification for radiated emissions (just like the RF module), and conducted emissions.

In this report we will investigate the cost aspect. Depending on the production quantity, what will be less costly? Using an RF module or using the RF chipset with discrete components? Small quantities will result in the certification costs for the chipset with discrete components being much more expensive than the certification cost for the RF module. Very large quantities will result in the certification costs being negligible for both the

module and chipset, thus the cost factor will mostly be defined by the component cost.

1.1.3 Implementing ESD protection

On the previous PCB design there were no electro-static discharge (ESD) protection design techniques implemented. Electrostatic discharge is the sudden release of built-up charge between objects, causing electricity to flow between them. Electrostatic discharge is enough to damage many semiconductor parts including MOSFETs, diodes and CMOS IC chips such as CPUs and graphic ICs.

In this report we will implement various ESD protection circuitry and ESD design techniques.

1.1.4 Power Integrity (PI) optimization

As electronic circuits have been scaled down, so have their absolute voltage margins. It is therefore getting increasingly important to be able to control that the supply voltage is steadily kept at the right level. Alternating currents in the power delivery network (PDN) will cause the voltage to vary outside the margins if the power network impedance is not correctly adjusted. This means that there could be induced voltages in the power distribution network in the circuit, causing components on the PCB to get lower reference voltages. In this report we will investigate such adjustments in the power distribution network (PDN) of our design, by simulating and incorporating different design techniques such as bypassing for better impedance control on the PDN.

2. Theory

In order to understand the discoveries of this project we will go through some theoretical aspects, such as PCB design, techniques, and standards used in the 21th century. We will also dive into the realm of Radio Frequency (RF), and discuss the basics of RF communication systems and their central building blocks (which is implemented in both the RF module and the RF chipset). Lastly we will discuss the importance of power integrity optimization and how it is done in the power distribution network of the design.

2.1 PCB design

The basic building blocks of modern electronics are printed circuit boards (PCBs), which link and interconnect different components to create working systems. PCB design is a crucial stage of the product development cycle, enabling us to convert theoretical concepts of electronic circuits to physical devices.

The quality of the PCB design plays a major role in determining the performance, reliability, and manufacturability for the final product. It is your job as an electronics engineer to design the PCB such that it follows all desired specifications for the application it is intended for, while adhering to all the design rules in order for the PCB to be manufacturable.

The rapid development of modern electronics has been pushing PCBs towards miniaturization, high speed, better functionality, reliability, and longer lifetime, resulting in the popularity of multilayer boards. Using a semi-solid adhesive called prepreg to combine two or more single and/or double-sided PCBs, creating multilayer PCBs, with a solid and thick core in the middle. With the increase of complexity and densities, it is plausible for issues to arise, such as noise, stray capacitance, and crosstalk when layer arrangement is inefficiently designed [6].

Optimal arrangement for a multilayer stack-up is one of the crucial elements in determining the electromagnetic compatibility (EMC) performance of a device. A correctly defined stack-up can minimize the radiation, but also protect the circuit board from external noise interference. However a poorly designed stack-up may encounter electromagnetic interference (EMI) radiation. In the next section we will discuss and define a PCB stack-up.

2.1.1 Defining the stack-up

Stack-up illustrates the arrangement of copper and insulating layers that construct the printed circuit board. There are many advantages of having a well-defined multilayer stack-up.

Firstly a multilayer stack-up allows you to get more circuitry on a single board through the various layers inside the PCB.

Secondly the PCB stack-up can help minimize circuit vulnerability, such as external noise, minimize radiation, and help with impedance mismatch [20].

Lastly a well-defined stack-up can minimize for low-cost, staying well above the minimum manufacturing capabilities will decrease the manufacturing cost.

General layers for a well-designed stack-up may include ground planes (GND), power planes (PWR), and signal layers. Here is an example of an 8-layer PCB stack-up.
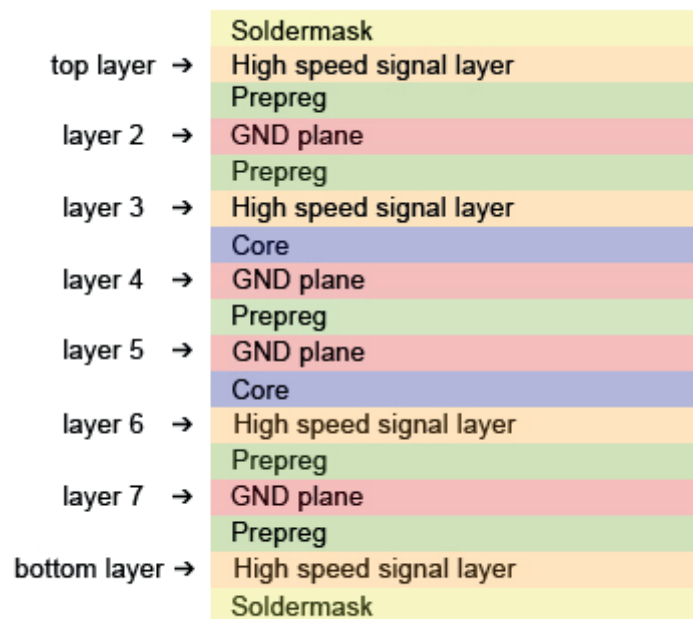
Figure 2.1: Layer stack-up for an 8-layer PCB [6].

2.1.2 What are vias?

As mentioned in section 2.1.1, multilayer stack-ups allow us to fit more circuitry in the various layers inside the PCB. This raises some questions. How are the layers inside connected to each other? Can the same signal be on every layer? Introducing vias, vias are small drilled holes that go through two or more adjacent layers. It allows signals to move between layers, which means the same signal can be on every layer. Vias are commonly categorized into three types—blind via, buried via and through-hole via. In this project only through-hole vias are used, and are the least expensive to drill during the manufacturing process.

Through-hole vias span from one outer layer (top layer) all the way to the other outer layer (bottom layer), and is the most commonly used type of via. While spanning from one outer layer to the other, it connects all the inner layers [7] [19].
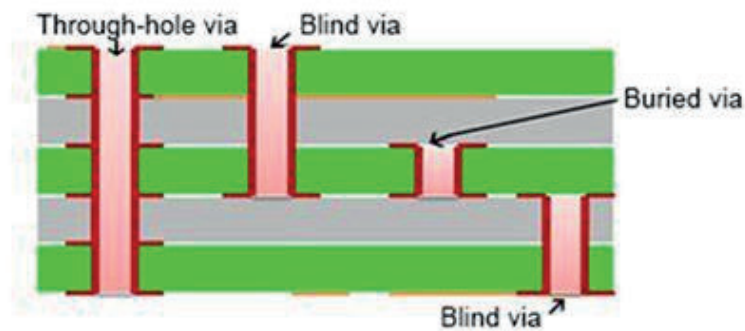
Figure 2.2: Types of vias [7].

Figure (2.2) demonstrates the different types of vias on a 6-layer PCB stack-up. The through-hole via goes through the entire board, connecting each and every of the six layers.

2.1.3 ESD protection design techniques

During a lifetime of a PCB there is a high likelihood of encountering electrostatic discharge, especially circuits that are meant to interface with the physical environment [8]. The design for this project will be enclosed in a trigger unit as mentioned in section 1.1.1. However that does not mean it is not prone for electrostatic discharge, since there are connectors on the PCB intended for external communication. ESD protection is an important aspect when it comes to design techniques, and is intended to protect sensitive components from blowing during an ESD event. Commonly, static charge accumulates during the operation of a PCB, which causes the electrostatic discharge to occur. By strategically placing ESD protection in the design, it will protect sensitive circuitry [8] [17].

There are various ESD protection techniques, but in this project I will only discuss the ESD protection that will be implemented in the GAIM PCB.

First ESD protection design technique implemented is ESD diodes on every external connector. Regarding the placement of ESD diodes on the PCB, it is important to keep the diodes as close as possible to the external connectors. Keeping the diodes close to the connectors will make the travel path for the static electricity miniscule, and protect the circuitry that comes after the diode [18].
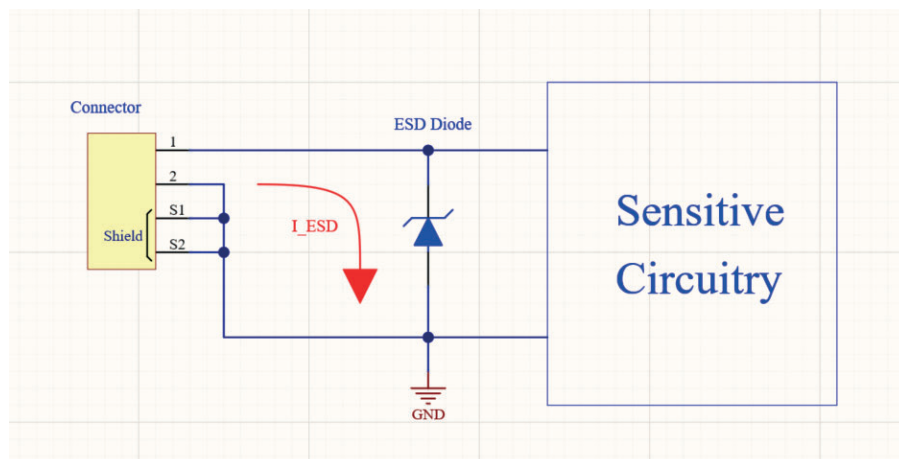
Figure 2.3: Schematic representation of the ESD diode.

Figure (2.3) illustrates the intended use of an ESD protection diode. Where *I_ESD* is the electrostatic discharge current, going from the connector through the ESD diode.

The second ESD protection technique implemented in this design is solely done in the layout design, where no extra components are needed. As we know from section 2.1.1, the top and bottom of the stack-up are covered in a non-conductive insulating thin layer called solder mask, which gives a circuit board the green color. By removing the solder mask on the edges of the board, we expose the copper ground plane. During an ESD event the discharge will go directly to ground from the edges and protect sensitive components.
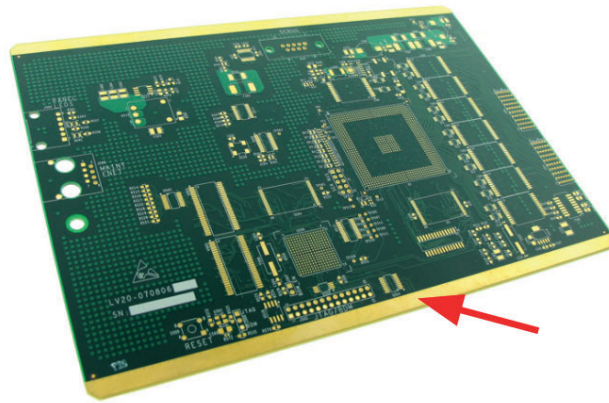
Figure 2.4: PCB with exposed copper ground on the edges [9].

Figure (2.4) illustrates the exposed copper ground on a PCB. This ESD protection design technique will be implemented on the GAIM PCB.

2.2 RF & Antenna theory

Since this master's thesis is not extensively about RF communication, I will not go into great details about this topic. Only the most basic principles and equations will be discussed.

2.2.1 Basic building blocks of an RF system

The basic building blocks of a wireless communication system is shown in figure (2.5):
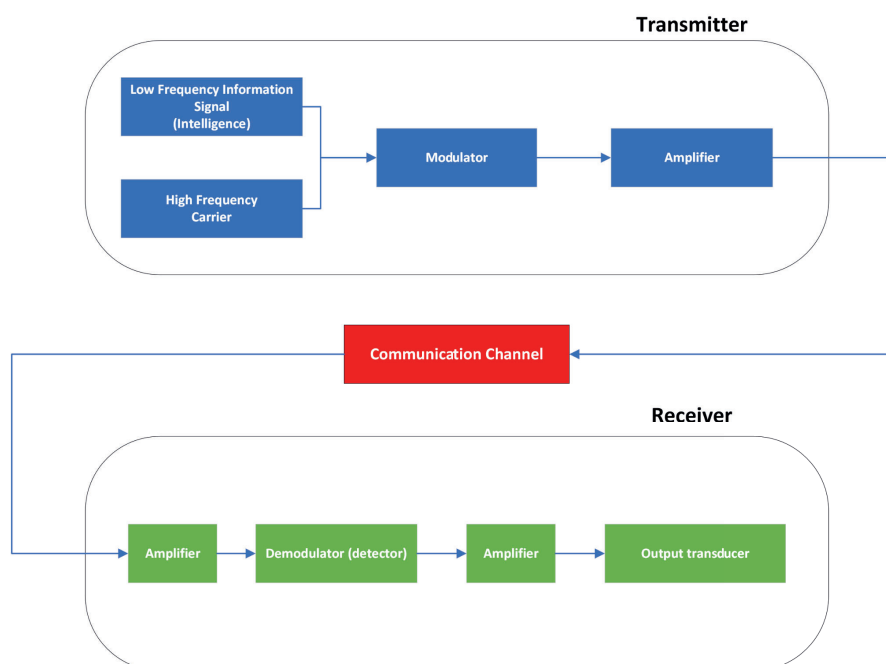
Figure 2.5: Basic building blocks of a wireless communication system [22].

There are three major aspects in a wireless communication system, the transmitter, a communication channel, and the receiver. To simplify the theory, a transmitter transformers information into signals, and sends it through a communication channel (such as power lines, cables, air etc). The receiver then converts those signals back into the same information.
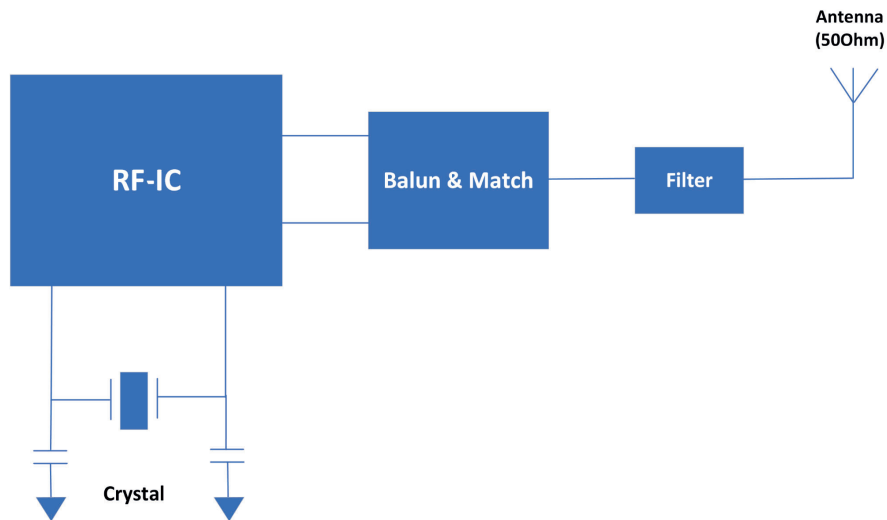
Figure 2.6: Basic building blocks of an RF system [22].

Figure (2.6) illustrates the basic building blocks for a typical RF system. It consists of a central processing unit (CPU), such as a transmitter, receiver, transceiver, or a system-on-chip (SoC) with an integrated microcontroller.

There is a crystal, which is typically used for the reference frequency for the local oscillator (LO) and the carrier frequency (CF).

The balun circuitry converts a differential signal to a single-ended signal, or vice versa.

A matching network for the antenna, which is used for impedance matching. In electronics, impedance matching is the practice of designing or adjusting the input impedance or output impedance of an electrical device for a desired value. Often, the desired value is selected to maximize power transfer or minimize signal reflection.

Filters are used to improve selectivity, which means filtering un-desired frequencies such as high frequency noise.

Lastly there is an antenna with 50 OHM impedance, intended for correct impedance matching.
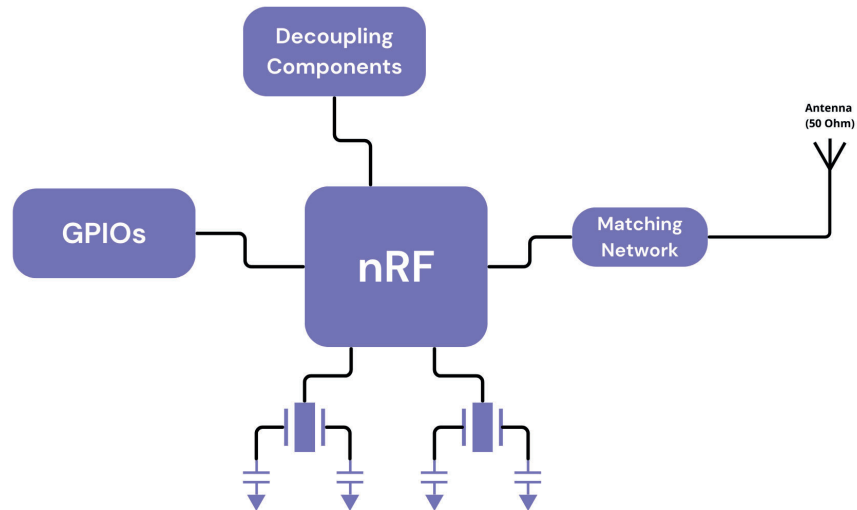
Figure 2.7: Simplified building blocks for the GAIM PCB.

Figure (2.7) illustrates a simplified RF block diagram for the new GAIM PCB. It consists of two crystal oscillators, one for the high frequency clock (HFCLK), and the other one for the low frequency clock (LFCLK). The HFCLK is for the CPU and requires a 64MHz clock signal for optimal operation. The LFCLK is distributed to different peripherals, and requires a 32.768kHz clock signal.

For this project only two general purpose I/Os (GPIOs) will be used. A button (will be used for reset, and other tasks), and a connector (that will be connected to the mechanical trigger unit, refer to figure (1.1)).

The matching network, used for 50 OHM impedance matching with the 2.4 GHz antenna. Which is an industry standard frequency for bluetooth.

A cluster of decoupling components will be used for supplying power for the nRF chip, and controlling the impedance on the power distribution network.

2.2.2 Power ratios & levels

When dealing with RF most voltages and powers are referred to in dB. Here are some relevant power ratios and power levels [13]:

$$P = 10 * log(\frac{P_1}{P_2}) \qquad [P] = dB \qquad (2.2.1)$$

$$P' = 10 * log(\frac{P_3}{1mW}) \qquad [P'] = dBm \qquad (2.2.2)$$

Where P is the power represented in dB, P' is the power represented in dBm and is referenced with 1mW. P_1, P_2, and P_3 are in watts.

2.2.3 Antenna power gain

Antennas are made with conductors with finite conductivity, which makes them susceptible to ohmic power loss [13]. The total input power is:

$$P_{in} = P_l + P_{rad} \qquad (2.2.3)$$

Where P_{in} is the power accepted by the antenna at its terminals during the radiation process, P_{rad} is the power radiated by the antenna, and P_l the power dissipated within the antenna [13].

To calculate the efficiency we use:

$$\eta_r = \frac{P_{rad}}{P_{in}} \qquad (2.2.4)$$

Where η_r is the radiation efficiency of the antenna.

2.2.4 ITU indoor propagation model & Sensitivity

This section will provide a brief overview of sensitivity and the ITU indoor propagation model.

The ITU indoor propagation model is a radio propagation model that estimates the path loss in a closed area, such as a building with any form of walls. This model is suitable for appliances designed for indoor applications that use the lower microwave bands, such as 2.4GHz [24] [25].

The ITU model is formally expressed like this:

$$L = 20log_{10}(f) + Nlog_{10}(d) + P_f(n) - 28 \qquad (2.2.5)$$

$$L = |S - P_{out}|$$
(2.2.6)

Where L is the path loss expressed in dB, f is the frequency of transmission in MHz, N is the distance power loss coefficient, d is the distance in meter, P_f is the floor loss penetration factor, which will be zero in this case, n is number of floors between the transmitter and receiver, also zero. S is the sensitivity after the antenna, P_{out} is the total radiated power, also called P_{rad}.

For this project we are interested in solving for the distance d, on both the old and new PCB. Comparing the distances we can figure out which PCB has better RF performance.

Sensitivity serves as an indicator, reflecting a device's ability to receive and decode a signal within a specified 'satisfactory error rate,' which is typically defined by the specifications of each application. The measurement of sensitivity is expressed in power levels, such as -100 dBm [26].

2.3 Power Integrity (PI)

The circuitry on a modern PCB requires the voltages and currents to be maintained at necessary levels within the power delivery networks (PDN), with minimal fluctuation. Variations in the PDN can cause performance degradation of the signals and cause false responses [11].

2.3.1 Power Distribution Network (PDN) bypassing

As electronic circuits have been scaled down, so have their drive voltages. This means that the absolute voltage margins are decreasing and it is getting increasingly important to be able to control that the drive voltage is steadily kept at the right level [12]. If the voltage ends up outside the margins, the digital logic might run slow or even malfunction [11].

The power distribution system connects the power domains of the chip to a voltage regulator that supplies the drive voltage (in this project the supply voltage comes from a cell battery). There are two aspects to consider when keeping the drive voltage controlled: the impedance of the PDN and the characteristics of the current flowing in the PDN. Combined they cause a total voltage drop [13]:

$$\Delta V = IR + L\frac{di}{dt} \qquad\qquad (2.3.1)$$

There is a quasi static part called the IR drop, and a dynamic part. The focus will be on lowering the resistances related to the power grid of the chip, the bondwires, and the planes and traces of the package and the PCB.

The next section will deal with dynamic voltage drop. However, it will be shown that it is important to manage the PDN impedance over a wide frequency range including DC.

2.3.2 Dynamic voltage drop

Most of the modern digital circuits are based on CMOS technology (including the nRF chip used in this project). To illustrate the dynamic voltage drop we will use complementary MOSFET transistors that are connected in series between power and ground, as shown in figure (2.8). The inductances of the power and ground conductors, connecting the circuit to the voltage regulator, are represented by L_{DD} and L_{SS}, while the capacitive load is shown as C_L. For simplicity the model C_L includes the output capacitance of the circuit, pad, package, and trace capacitances.
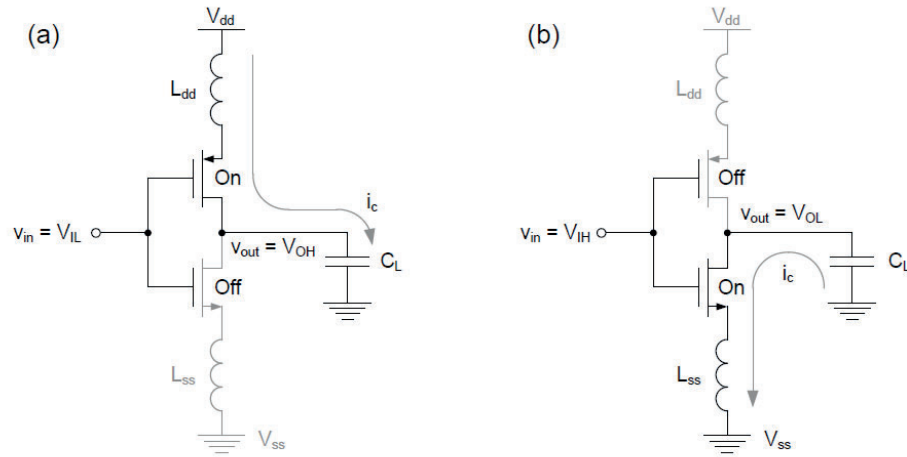
Figure 2.8: (a) Charging of the load capacitance when switching from low to high on the output and (b) discharging of the load when switching from high to low on the output [10].

During a switch when the MOSFETs change states, the current will either charge or discharge the load capacitance. This means that there will be a current flowing through the inductances [14]:

$$i_c = C_L \frac{v_c}{dt} \tag{2.3.2}$$

From Faraday's law of induction we know that variations in current flow will induce a voltage drop across inductive circuitry [13]:

$$V_L = L \frac{di}{dt} \tag{2.3.3}$$

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Where L is the inductance, V_L is the voltage across the inductor, and di is the current variations. The rapid charging / discharging will therefore change the power / ground potential at the circuit relative to the *Vdd* / *Vss* regulator reference. The potential difference ΔV is proportional to the inductances L_{dd} / L_{ss} of the PDN.

A way to decrease these voltage variations is to lower the inductance of the PDN current loop. For instance, the inductance scales linearly with the length of the conductors, which hence should be kept as short as possible. It is also affected by a number of other parameters related to the routing and PCB layer dimensions, such as the thickness of the dielectric layers between planes and traces. Another method for decreasing the effective inductance is bypassing. The impedance is then decreased by shortening the current loops with capacitors.

2.3.3 Bypassing of the Power Distribution Network

There are three stages of a PDN: chip, package, and PCB [15]. The power and ground rails on the chip are connected to the power and ground conductors on the package, which in turn are connected to the power and ground planes on the PCB where the regulator is situated. The simplified model of a PDN can be seen in figure (2.9). The indices describe what net the element belongs to. The *p* stands for power, *g* ground, *r* regulator, *b* board, *p* package, and *c* chip. Meaning *pb* would represent the power on the board net.
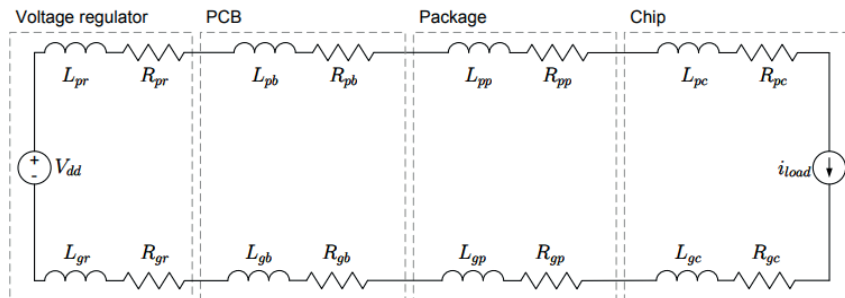
Figure 2.9: Simplified model of the PDN divided into three levels (PCB, package, and chip) [10].

From figure (2.9) we see that the PDN can be represented as a RL network. The impedance, as a function of frequency, becomes:

$$Z(\omega) = R_{tot} + j\omega L_{tot} \qquad (2.3.4)$$

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Where R_{tot} and L_{tot} are the total power and ground conductor resistances and inductances. This means that the distance between the chip and the regulator can be a couple of centimeters depending on how long the traces/planes are on the PCB, thereby making this current loop very inductive.

The supply current is in general composed of frequency components covering a broad spectrum starting at DC. The overall aim is to assure that the magnitude of the output impedance of the PDN is low for the whole bandwidth of the current waveform. This is illustrated in figure (2.10), where the cut-off frequency defines the current bandwidth, while the target impedance defines the impedance to meet or reach below. In our applications, where we only control the board level PDN, the cut-off frequency is often set to a value defining the frequency beyond which the package and chip are designed to handle the bypassing.
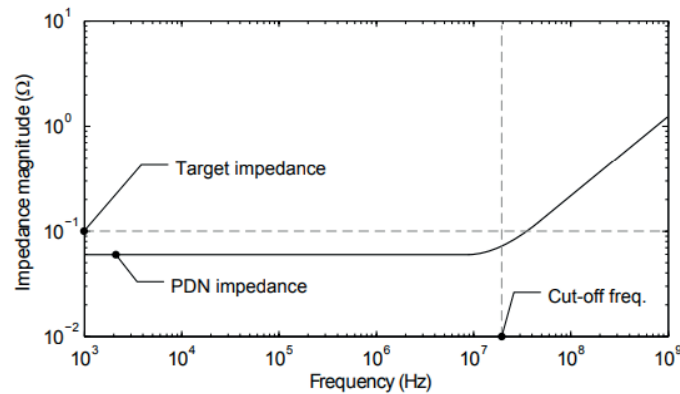
Figure 2.10: Ideal output impedance of a passive PDN as a function of frequency. The cut-off frequency defines the current bandwidth, while the target impedance defines the impedance to meet or stay below [10].

2.3.4 Defining cut-off frequency and target impedance

The target impedance is calculated by Ohms law:

$$Z_{target} = \frac{\Delta V}{\Delta I_{MAX}} \tag{2.3.5}$$

ΔV is the maximum allowed voltage fluctuation for the components (IC), ΔI_{MAX} is the maximum current variations, meaning it is not the maximum current drawn at any specific moment, but instead the change in

rate of the current. As an example, let us assume that a chip will step the current from 700mA to 1500mA in 25ns. If the voltage drop across the PDN is estimated to be 50mV, the target impedance would then be according to (2.3.5):

$$Z_{target} = \frac{50mV}{(1500-700)mA} = 62.5m\Omega$$

When optimizing the PDN impedance it is relevant to have a decent estimation of the current bandwidth, meaning the highest frequency component of the current waveform during normal operation of the chip. Which will represent the cut-off frequency:

$$f_{co} = \frac{1}{\pi \cdot t_r} \tag{2.3.6}$$

Where t_r is the rise-time of the waveform, and f_{co} is the cut-off frequency/bandwidth [16].

Next section will discuss the actual impedance of the PDN, in the frequency range that needs to be addressed by the PCB and packaging bypass capacitors.

2.3.5 Selecting the correct capacitor

As shown in figure (2.9) the PDN can be described as an RL network. Plotting the magnitude of the impedance will give us the figure (2.11).
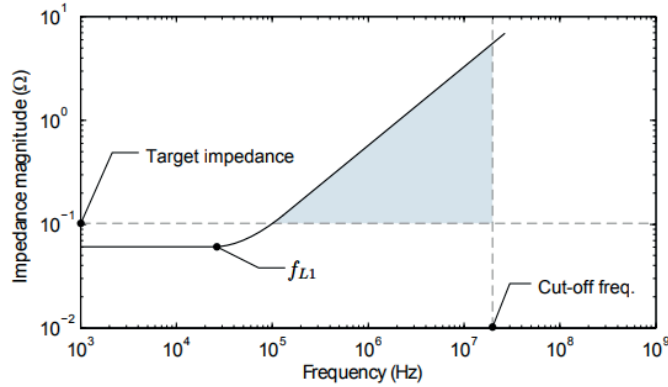
Figure 2.11: Typical impedance magnitude as a function of frequency for a PDN without bypassing capacitors. The shaded area indicates a violation of the impedance requirement.

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The total impedance is mostly determined by the resistance up to the frequency f_{L1}, which is determined by [16]:

$$f_{L1} = \frac{R_{tot}}{2\pi L_{tot}} \qquad (2.3.7)$$

Above f_{L1} the inductance L_{tot} will be the main contributor for the impedance of the PDN according to (2.3.4).

In order to keep the impedance low on the PDN, we need to create new current loops when the impedance exceeds the target impedance:

$$f = \frac{Z_{target}}{2\pi L_{tot}} \qquad (2.3.8)$$

To create new current loops that decouples the high inductances on the regulator, is done by placing one or more capacitors on the PCB between power and ground. As shown in figure (2.12), there will be two current loops.
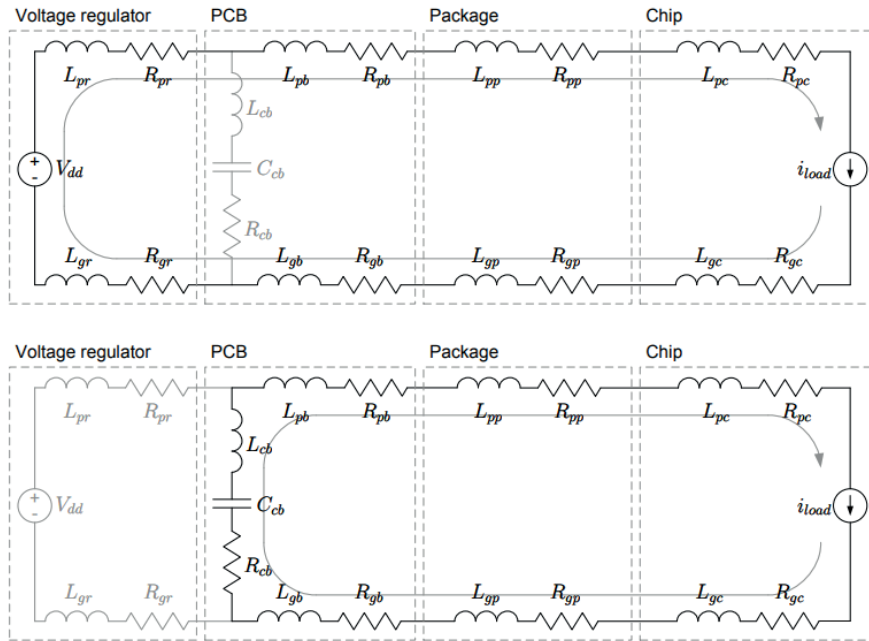
Figure 2.12: Bypassing capacitors will form new current loops in the PDN, here shown as a new loop created by a capacitor on the PCB.

The capacitor is placed in parallel to the voltage regulator, and the impedance seen from the load will therefore be:

$$Z(\omega) = (R_{cb} + \frac{1}{j\omega C_{cb}} + j\omega L_{cb}) || (R_{pr} + R_{gr} + j\omega(L_{pr} + L_{gr}))$$

Which can be simplified to:

$$R_{reg} = R_{pr} + R_{gr}$$

$$L_{reg} = L_{pr} + L_{gr}$$

$$Z(\omega) = (R_{cb} + j(\omega L_{cb} - \frac{1}{\omega C_{cb}})) || (R_{reg} + j\omega L_{reg}) \qquad (2.3.9)$$

The bypassing capacitance and the regulator inductance will form a parallel resonant circuit damped by the resistances of the regulator and the capacitor.
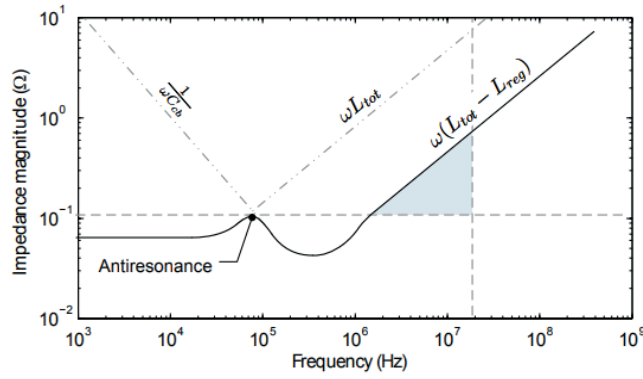
Figure 2.13: Typical impedance magnitude, as a function of frequency, for a PDN with a single set of bypassing capacitors.

The parallel resonance, also called antiresonance will cause the impedance to peak, as seen on figure (2.13). The peak impedance can be calculated using the quality factor Q and the characteristic impedance Z_0 of the resonance circuit [10][16]:

$$Z_{peak} = QZ_0 = \frac{\omega_0 L_{reg}}{R_{reg} + R_{cb}} \sqrt{\frac{L_{reg}}{C_{cb}}} = \frac{L_{reg}}{(R_{reg} + R_{cb})C_{cb}} \qquad (2.3.10)$$

Given that the peak impedance Z_{peak} should not exceed the target impedance Z_{target} we get:

$$Z_{peak} < Z_{target} \iff C_{cb} > \frac{L_{reg}}{(R_{reg} + R_{cb})Z_{target}} \qquad (2.3.11)$$

This will give a minimal requirement on the bypass capacitance C_{cb}. We see from (2.3.11) that the series resistances of the capacitor R_{cb} (ESR) can lower the capacitor requirement by damping the resonance. The best results will be obtained with both R_{reg} and R_{cb} being equal to the characteristic impedance since the system then is critically damped [16].

For frequencies above the anti-resonance the PDN impedance will decrease and mainly depend on the bypass capacitance, as seen in figure (2.13). Moving up in frequency the first series resonance is found, the resonance between the capacitance from the bypass capacitor and the inductance of the new loop. This is approximated by:

$$f_{res} = \frac{1}{2\pi\sqrt{L_{reg}C_{cb}}} \qquad (2.3.12)$$

Contrary to the parallel resonance which has a peak, the series resonance has a minimum, thereby the PDN impedance will be mostly resistive. Even higher frequencies the PDN impedance will yet again depend on the RL network, and needs to be decoupled once again, not to exceed the target impedance at:

$$f = \frac{Z_{target}}{2\pi(L_{tot} - L_{reg})} \qquad (2.3.13)$$

The same procedure will hence be repeated until the target impedance is met for the whole bandwidth, putting new bypassing capacitors on the PCB, closer and closer to the IC chip. A way to keep the resistive and inductive parts low on a capacitor, while increasing the capacitance, is to put several capacitors in parallel at each level of bypassing. How the impedance is affected by putting capacitors in parallel or altering their capacitance, equivalent series resistance (ESR), or inductance (ESL), is shown in figures (2.14),(2.15),(2.16), and (2.17).
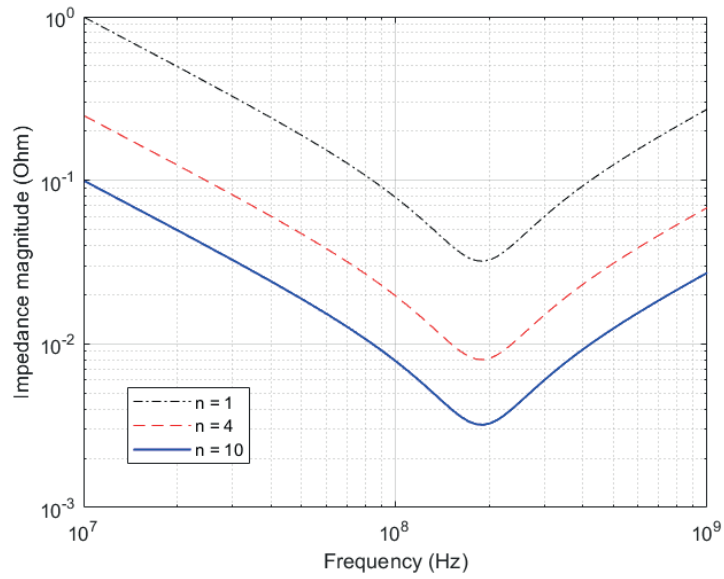
Figure 2.14: Impedance when varying the number of capacitors in parallel, where n is the number of capacitors.
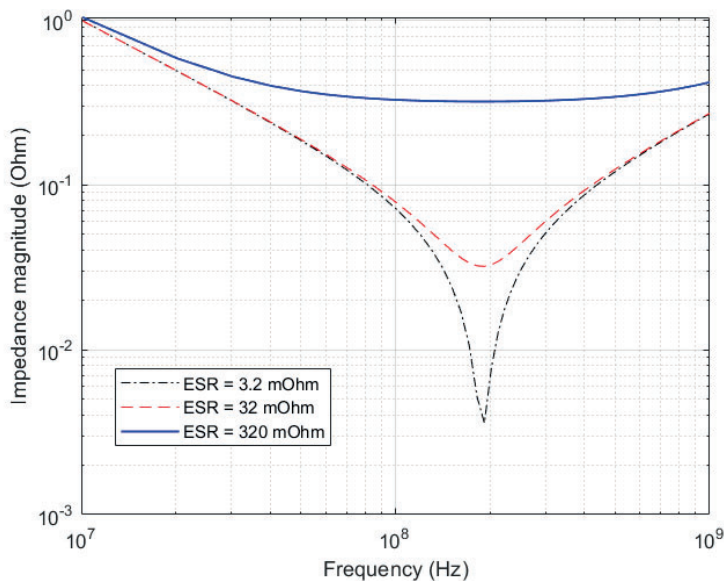
Figure 2.15: Impedance when varying the ESR.

35
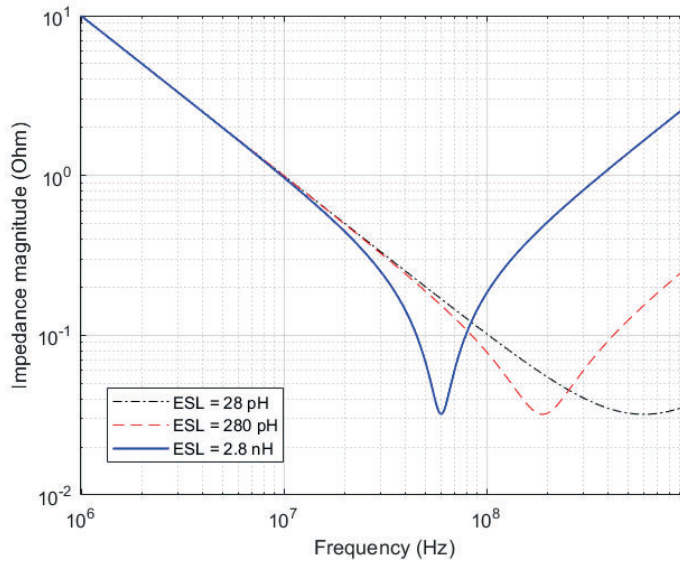
Figure 2.16: Impedance when varying the ESL.
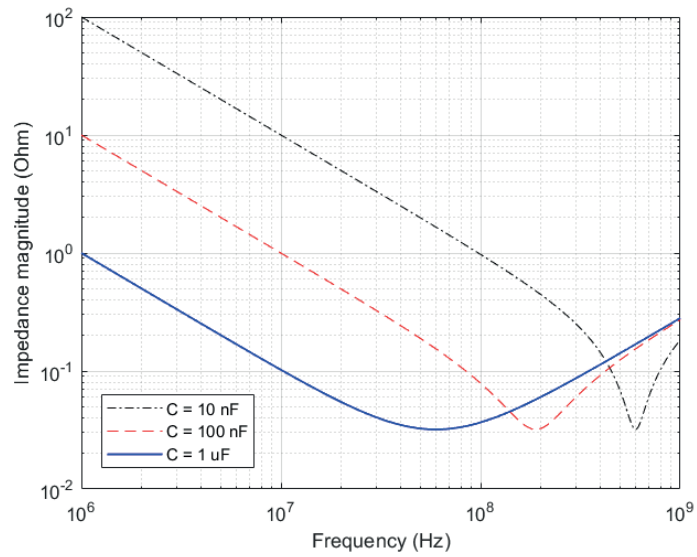
Figure 2.17: Impedance when varying the capacitance value.

3. Methodology

The following chapter explains what hardware and software were used in the design, assembly and testing process of the GAIM PCB.

3.1 Design process of the PCB

Software used for the design of this PCB was Altium Designer.

3.1.1 Component library & Component creation

For this project the existing library from the previous revision of GAIM was used. The nRF chipset and discrete component symbols and footprints were made by me using the design tool inside the library.
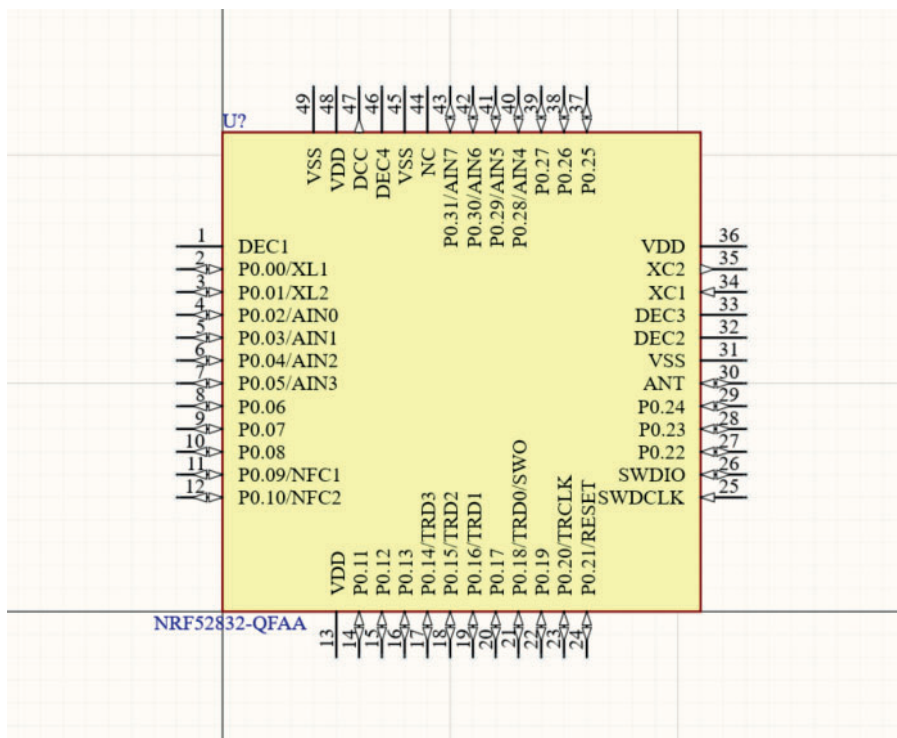
Figure 3.1: Schematic symbol of the nRF chip made by me.
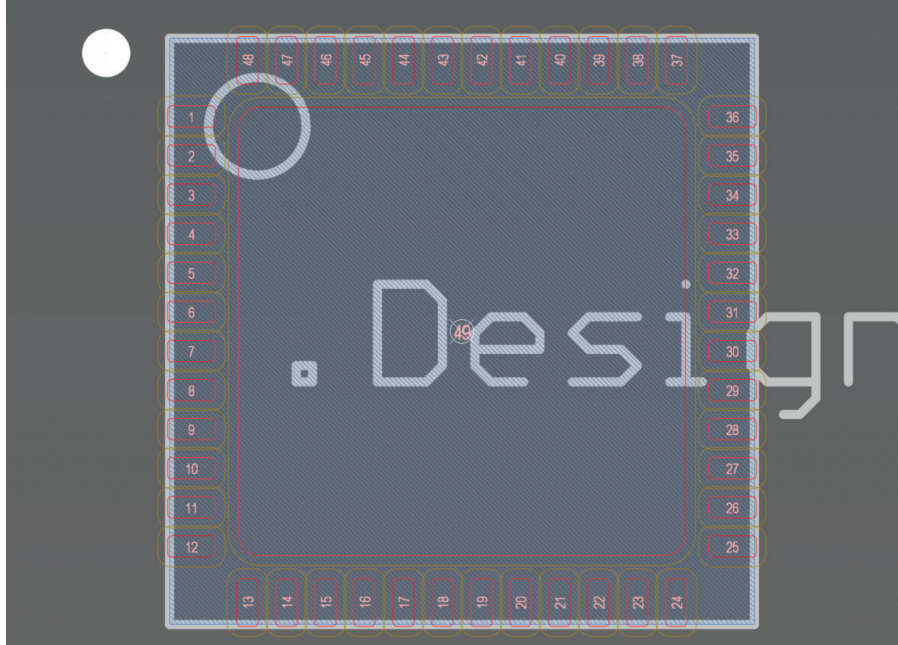
Figure 3.2: Footprint for the nRF chip made by me.

The same thing is done for the rest of the discrete components that are not already in the library.

Once the symbol and footprint is created for all the necessary components, they are linked and ready for use.

3.1.2 Schematic design

Drawing the schematic is done by placing all the necessary components, section it out by the specific circuitry and connecting everything.

Once every component has been connected properly, with correct net-labels etc, the schematic is done, and we have a finished canvas.
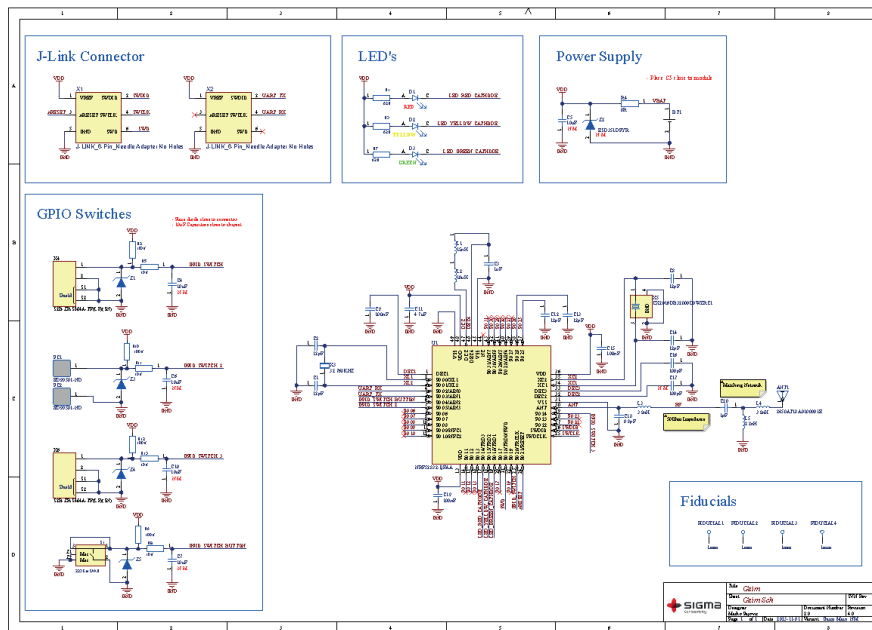
Figure 3.3: GAIM Schematic.

Fig (3.3) illustrates the finished schematic, where we can clearly see each different section with specific circuitry, annotated components, and all net-names that were manually placed. For a better view of the schematic refer to Appendix A section A.1.

3.1.3 Bill Of Materials (BOM)

The bill of materials (BOM) is essentially a list with all the components needed for the PCB to be assembled. The BOM is divided into columns and rows. Each row represents a component. Each column represents different information about that specific component, such as a description, the designator (used for identification of a component on the board), manufacturing part number etc, as shown in figure (3.4) below.

| Designator	Quantity	Comment	Description	Value	Manufacturer	Manufacturer Part N	Supplier 1	Supplier Part Number 1	Rating	Fitted
ANT1	1	2450AT18A0100001E	Antenna RF ANT 2.4GHZ CHIP SOLDER SMD M3216	2.4GHz	Johanson Technolo	2450AT18B100E	Digi-Key	712-1006-1-ND		
BT1	1	SMTU2032-LF	BATTERY HOLDER Renata Battery Holder		Renata	SMTU2032-lf	farnell	1216354		
C1, C2, C8, C12, C13	6	12pF	CAP CER 12pF 25V COG, NP0 1% M0603	12pF	Murata	GJM0335C1E120FB0	Digi-Key	490-GJM0335C1E120FB01D	25V	
C3	1	1uF	CAP CER 1uF 10% X7R M1608	1uF	Murata	GCM188R71C105KA	Digi-Key	490-5241-1-ND	16V	
C9, C15, C19	3	100nF	CAP CER 100nF 16V X7R 10% M0603	100nF	Murata	GRM033Z71C104KE	DigiKey	490-GRM033Z71C104KE14DTR-ND		
C11	1	4.7uF	CAP CER 4.7uF 10V X5R 10% M1005	4.7uF	Samsung Electro-M	CL05A475KP5NRNC	Digi-key	1276-1480-2-ND		
C16	1	100pF	CAP CER 100pF 25V COG 5% M0603	100pF	Murata	GRM0335C1E101JA	Digi-key	490-3160-2-ND	25V	
C18	1	0.8pF	CAP CER 0.8pF ±0.05pF 25V COG, NP0, M0603	0.8pF	Murata	GJM0335C1ER80WB	Digi-key	490-14788-2-ND	25V	
C20	1	1pF	1 pF ±0.1pF 50V Ceramic Capacitor C0G, NP0 M0603	1pF	Murata	GJM0335C1H1R0BB0	DigiKey	490-GJM0335C1H1R0BB01	50V	
D1	1	APHHS1005LSECK/J3-PF	LED RED Colour M1005	RED	Kingbright	APHHS1005LSECK/J	Digi-key	754-2123-2-ND	2mA, 1.85V	
D2	1	APHHS1005LSYCK/J3-PF	LED Yellow Colour M1005	Yellow	Kingbright	APHHS1005LSYCK/J	Digi-key	754-2125-2-ND	2mA, 1.85V	
D3	1	APHHS1005LCGCK	LED Green Colour M1005	Green	Kingbright	APHHS1005LCGCK	Digi-key	754-2121-2-ND	2mA, 1.9V	
L1	1	15nH	IND CER 15nH 560mA ±10% M1005 172 mOHM	15nH	Delta Electronics/C	0402HS-150EKTS	Digi-Key	2035-0402HS-150EKTSTR-N	560mA	
L2	1	10uH	IND CER 10uH 300mA ±20% M1608 1.37 OHM	10uH	Murata	LQM18DZ100M70L	Mouser	81-LQM18DZ100M70L	300mA	
L3, L4	2	3.9nH	IND CER 3.9nH High Frequency Inductor, 500 mA, .17	3.9nH	Murata	LQP03HQ3N9C02D	Mouser	81-LQP03HQ3N9C02D	500mA	
L5	1	2.2nH	IND CER 2.2nH High Frequency Inductor, 600 mA, .12	2.2nH	Murata	LQP03HQ2N2C02D	Mouser	81-LQP03HQ2N2C02D	600mA	
PC1, PC2	2	ED90501-ND	CONN PC PIN GOLD	7937	Mill-Max Manufactu	ED90501-ND		7937-0-00-15-00-00-03-0		
R1, R3, R7	3	62R	RES 62R 1% 1/16W M1005	62R	Yageo	311-62.0LRCT-ND		311-1.00LRCT-ND	1/16W	
R2, R6, R10, R12	4	100K	RES 100K 1% 1/20W M0603	10K	Yageo	RC0201FR-07100KL	Digi-Key	311-100KMCT-ND	1/20W	
R4	1	0R	RES 0R 1/10W M1005	0R	Panasonic	ERJ-2GE0R00X	Digi-key	P0.0JCT-ND	1/10W	
R5, R8, R11, R13	4	10K	RES 10K 1% 1/20W M0603	10K	Stackpole	RMCF0201FT10K0	Digi-Key	RMCF0201FT10K0CT-ND	1/20W	
S1	1	223GMSAAR	SWITCH TACTILE Right Angle 160gf	160gf	CTS Electrocompon	223GMSAAR	Digi-key	223GMSAAR-ND		
U1	1	NRF52832-QFAA	IC RF TXRX+MCU BLUETOOTH 48-VFQFN		Nordic	NRF52832-QFAA-R	Digi-key	4823-NRF52832-QFAA-RCT-ND		
X1, X2	2	J-LINK_6-Pin_Needle Ada	J-LINK_6-Pin, Needle Adapter without holes	J-LINK_6-Pin_Needl						
X3	1	32.768KHZ	XTAL 32.768kHz, 9pF, ±20ppm	32.768kHz	Micro Crystal AG	CM7V-T1A-32.768KH	Digi-key	2195-CM7V-T1A-32.768KHZ-9PF-20PPM-TA-QCCT-ND		
X4, X6	2	S2B-ZR-SM4A-TF(LF)(SN)	CON 4 Positions Header 0.100" (1.5mm)		JST Sales America I	S2B-ZR-SM4A-TF(LF)	Digi-key	455-1693-1-ND	1.5mm	
X5	1	CX2016DB32000D0WZR	32MHz ±25ppm Crystal 8pF 60 Ohms 4-SMD, No Lea	32MHz	KYOCERA AVX	CX2016DB32000D0	Digi-key	478-CX2016DB32000D0WZRC1TR-ND		
Z1, Z3, Z4, Z5	4	ESD351DPYR	Diode TVS 6.5V 16A M1006	6.5V Clamp 16A Ipp	Texas Instruments	ESD351DPYR	Digi-key	296-51109-1-ND		

Figure 3.4: GAIM BOM.

BOM is sent off to the assembler who will order the components, and start the assembly process once the components and the PCB arrives from the manufacturer. For a more detailed view of the BOM refer to Appendix A section A.3.

3.1.4 Setting design rules & Layout design

Once the schematic is done and approved it is time to import that schematic to the PCB editor.

This will import all the component footprints and nets that are linked with each symbol on the schematic to the PCB Editor.

Before we start placing components on the board we need to set the stack-up and design rules. That is done in the stack-up manager and design rules settings. The rules can vary from project to project and from manufacturer to manufacturer. In this project the manufacturing company is called Brandner. The manufacturing company capabilities is what will set our design rules and stack-up, meaning the minimum clearance/width between components, traces, holes etc.

#	Name	Material	Type	Weight	Thickness	Dk	Copp
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.025mm	4.2	
1	Top Layer	CF-004	Signal	1oz	0.047mm		Above
	Dielectric 2	PP-006	Prepreg		0.18mm	4.1	
2	2		Signal	1oz	0.035mm		Above
	Dielectric 1	Core-025	Core		1.08mm	4.6	
3	3		Signal	1oz	0.035mm		Below
	Dielectric 3	PP-006	Prepreg		0.18mm	4.1	
4	Bottom Layer	CF-004	Signal	1oz	0.047mm		Below
	Bottom Solder	Solder Resist	Solder Mask		0.025mm	4.2	
	Bottom Overlay		Overlay				

Figure 3.5: Layer stack-up for the GAIM PCB.

The stack-up for this project is shown in figure (3.5). It is a 4 layer board and where we can see the different copper pours, dielectric materials and thicknesses etc. The stack-up contains all the information about what materials will be used to manufacture the PCB.

Since there is an RF section in the design, we need to consider impedance matching as discussed in RF theory. This means that the RF trace on the board needs to be 50 OHMS. Setting impedance on traces in Altium is done by a built-in tool that will set the clearance and width on the RF traces to achieve 50 OHM impedance.
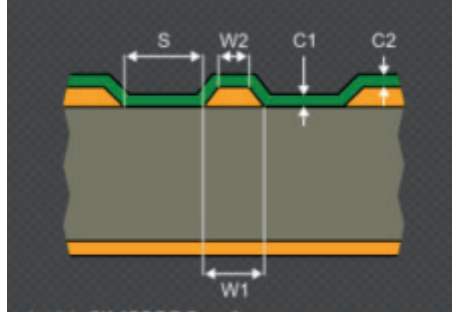
Figure 3.6: 50Ω impedance profile for GAIM PCB.

Where:

$$S = 0.3mm$$
$$W1 = 0.28mm$$
$$W2 = 0.27mm$$
$$C1 = 0.025mm$$
$$C2 = 0.025mm$$
$$Z_0 = 50.41\Omega$$
$$\gamma = 0.82\%$$
$$\tau_p = 5.96ns/m$$
$$L = 300.28nH/m$$
$$C = 118.17pF/m$$

S is the clearance between the trace and the planes, $W1$ and $W2$ is the width of the trace, $C1$ and $C2$ is the solder mask thickness, Z_0 is the impedance , γ is the deviation, τ_p is the delay per meter, L is the inductance per meter, and C is the capacitance per meter.

After viewing the manufacturing capabilities from the Brandner website, it is time to set the design rules. In tables (3.1), (3.2), (3.3), (3.4), and (3.5) we see the clearances and widths that are used for this board.

(mm)	Track	SMD Pad	TH Pad	Via	Copper	Text
Track	0.15					
SMD Pad	0.15	0.15				
TH Pad	0.15	0.15	0.15			
Via	0.15	0.15	0.15	0.15		
Copper	0.15	0.15	0.15	0.15	0.15	
Text	0.15	0.15	0.15	0.15	0.15	0.15
Hole	0	0	0	0	0	0

Tabel 3.1: Clearances for different nets.

(mm)	Track	SMD Pad	TH Pad	Via	Copper	Text
Track	0.3					
SMD Pad	0.3	0.3				
TH Pad	0.3	0.3	0.3			
Via	0.3	0.3	0.3	0.3		
Copper	0.3	0.3	0.3	0.3	0.3	
Text	0.3	0.3	0.3	0.3	0.3	0.3
Hole	0	0	0	0	0	0

Tabel 3.2: Clearances with 50 OHM impedance characteristics. Taken from the impedance profile in **figure 3.6**.

(mm)/Layer	L1 (Top)	L2	L3	L4 (Bottom)
Min	0.125	0.125	0.125	0.125
Preferred	0.15	0.15	0.15	0.15
Max	1	1	1	1

Tabel 3.3: Trace width for any arbitrary signal. Shows the minimum, preferred and maximum width on each layer

(mm)/Layer	L1 (Top)	L2	L3	L4 (Bottom)
Min	0.15	0.15	0.15	0.15
Preferred	0.3	0.3	0.3	0.3
Max	5	5	5	5

Table 3.4: Trace width for power signals.

(mm)/Layer	L1 (Top)	L4 (Bottom)
Min	0.28	0.28
Preferred	0.28	0.28
Max	0.28	0.28

Table 3.5: Trace width for a 50 OHM impedance trace. Taken from the impedance profile in **figure 3.6**.

Upon the establishment of all design rules, the layout design phase can start.

Firstly, the floorplan is devised, determining the most optimal and logically sound placement for all components. Some components have a fixed placement from a mechanical perspective, such as the battery holder,

connectors and button. This makes the placement for the nRF chip and the discrete components limited. Given GAIM's requirements to maintain identical mechanical functionalities, it is imperative to position the nRF chip in a location approximating the placement of the ANNA RF module in the previous design.
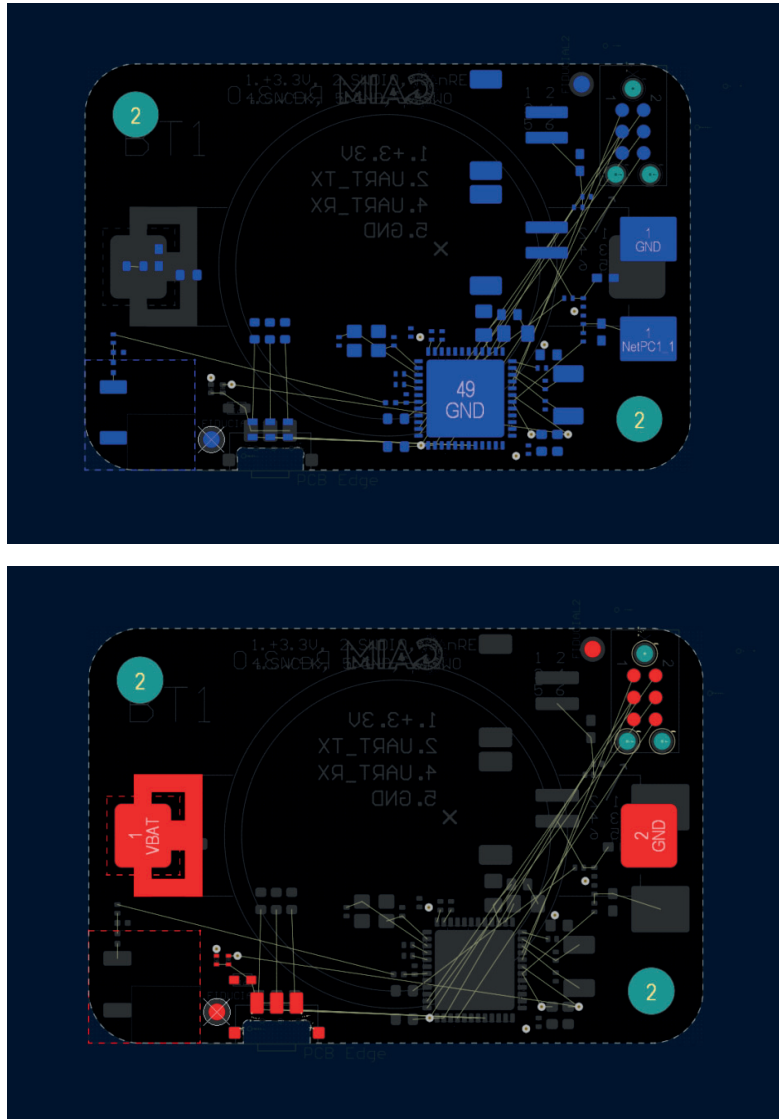
Figure 3.7: Floorplan for GAIM 4.0.

Once the floorplan is set, I can start the routing process. I start routing the most important and sensitive traces/components. In this case the most sensitive aspect is the RF impedance controlled trace. When routing these types of traces we want to keep ground all the way around the trace, including ground vias. This is shown in figure (3.11). In the lower left corner the RF trace goes from the nRF chip to the matching network and the antenna.

For the antenna it is important to follow the datasheet [5]. To address the challenge of degradation and alteration in the antenna radiation pattern caused by the presence of ground underneath on the PCB, a solution involves removing a 6.5mm*6.5mm section from the ground planes on each layer, seen in the left corner of figures (3.8), (3.9), (3.10), and (3.11).

Another sensitive component in this design are the crystals. For crystals it is important to keep ground directly below, on layer 3 (since the crystals are placed on the bottom layer (L4)). Routing traces below the crystals may generate crosstalk, since crystals are considered high-speed signals. Crosstalk is avoided by having ground planes below the crystals. In fact as shown in figure (3.10) (L3), the entire plane is GND with no other signals routed. I purposefully avoided routing any signals on layer 3 to keep the entire plane GND, for the reason to not accidentally create crosstalk or degrade the impedance controlled RF trace below on layer 4.

Leveraging creative routing techniques, I successfully directed the remaining arbitrary signals across the top layer, layer two, and layer four. Finishing off with the power network on the top layer shown in figure (3.8). This is called a power tree, since the power traces look like branches with a big stem.

Upon completion of all routing, we have a finished PCB, shown in figure (3.12), and ready for review. The reviewing process is done by the RF team to check the RF routing and antenna placement, and also done by another PCB designer to make sure all the routing is done correctly. Running the built-in tool DRC in Altium will display all design errors.

Once the review process is done and approved, we are ready to send the board for manufacturing, which will be discussed in the next section.
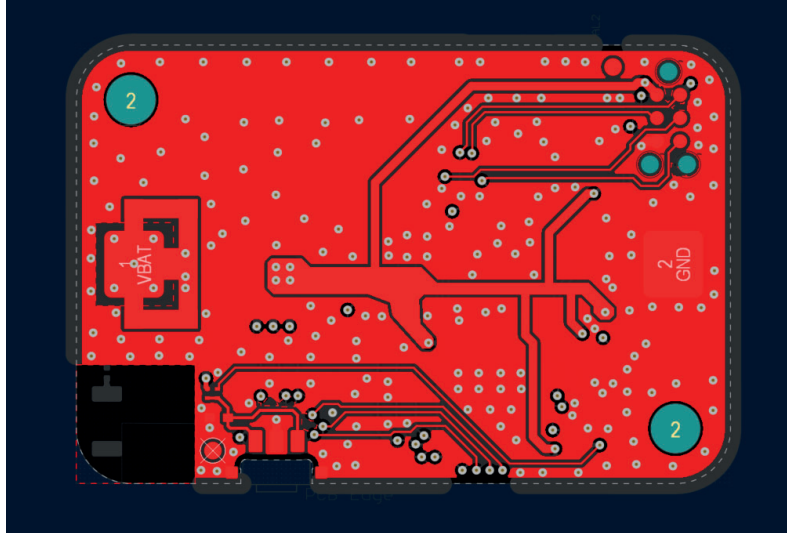
Figure 3.8: Top Layer (Signal/Power)
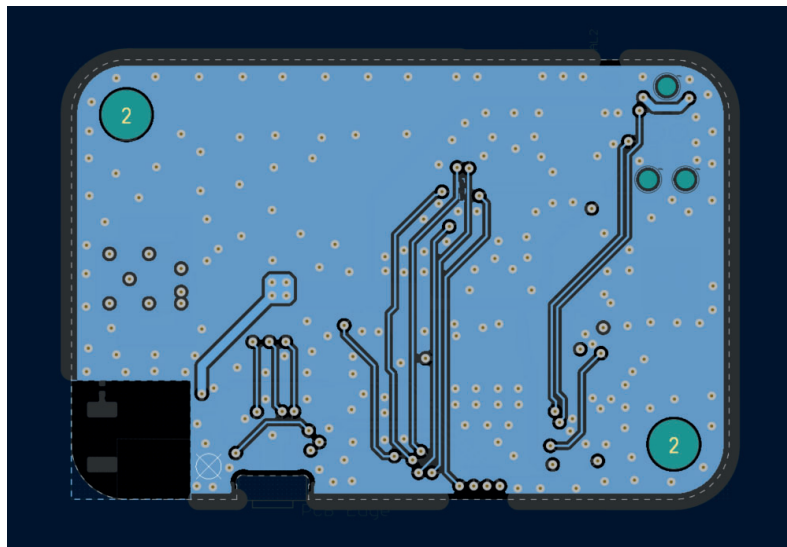
Figure 3.9: Layer 2 (Signal)
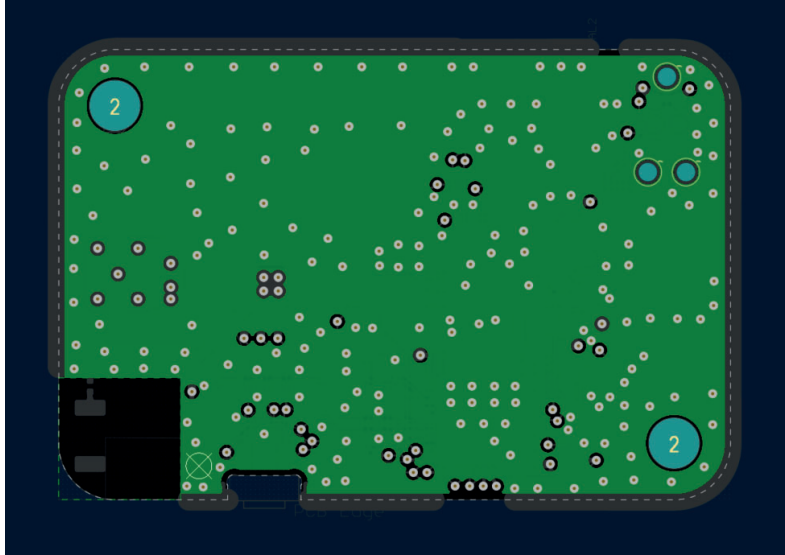
Figure 3.10: Layer 3 (GND)
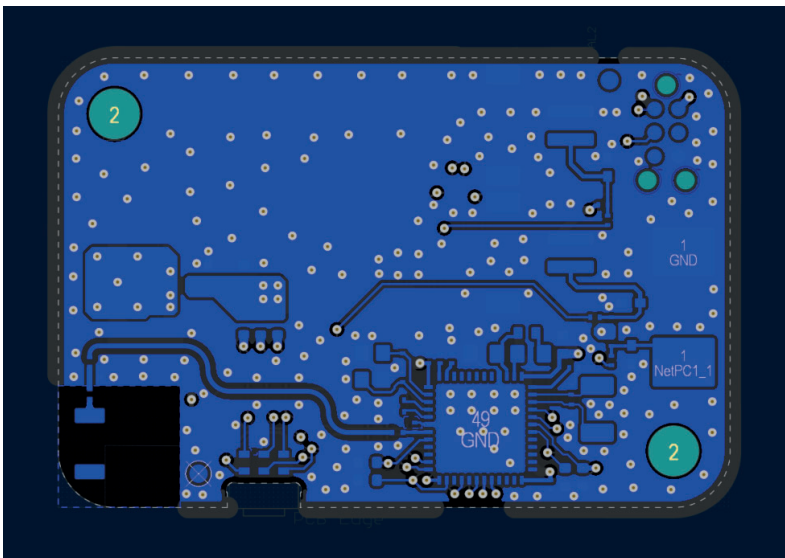
Figure 3.11: Bottom Layer (Signal)
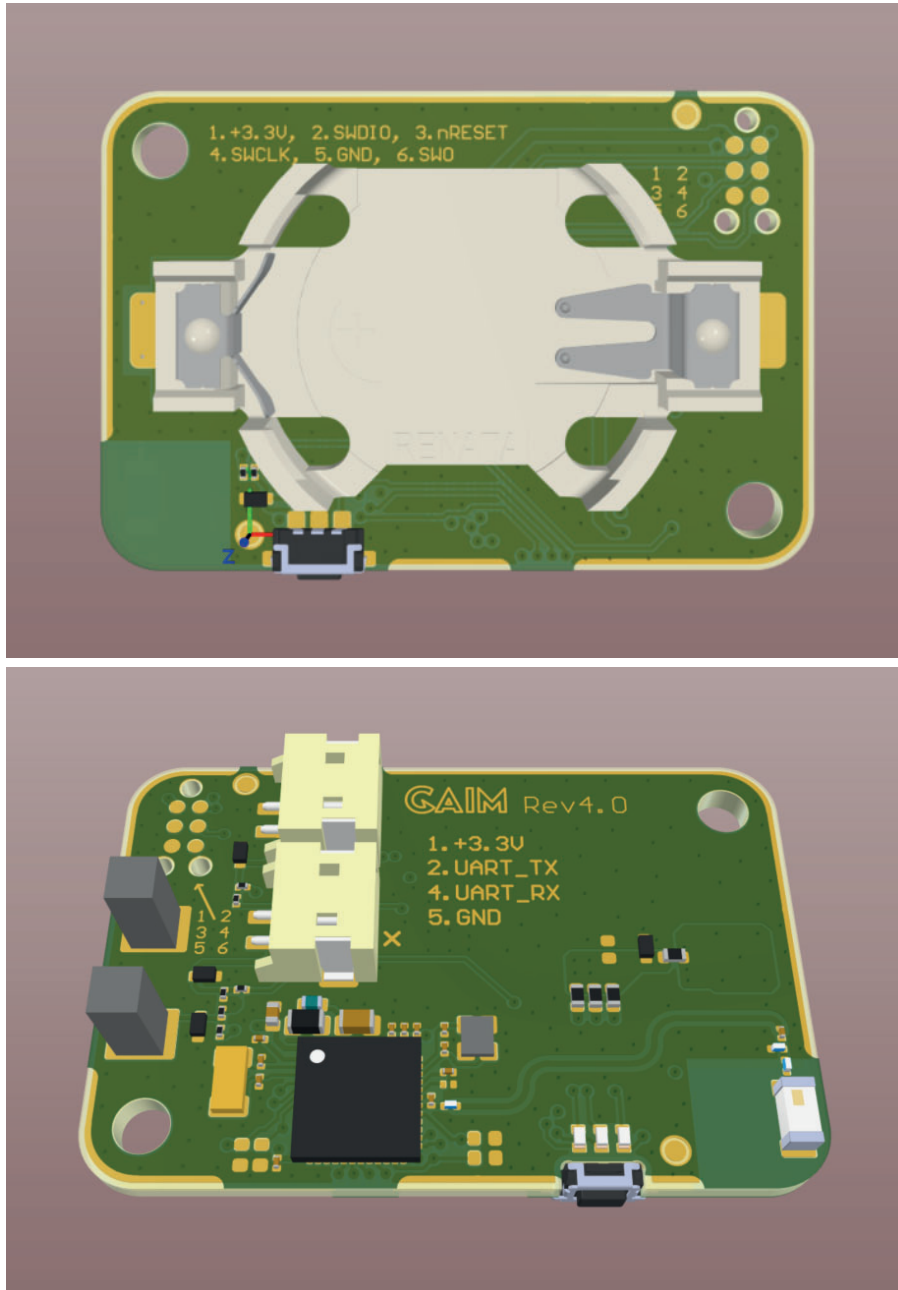
Figure 3.12: GAIM 4.0 PCB.

3.1.5 Output manufacturing files

Once the design process is finished it is time to order and manufacture the boards. Within Altium you can export manufacturing files. The manufacturing files consist of gerber, ODB++, and P&P. Gerber and ODB++ are files for creating the PCB, using either a drill for vias or laser for small traces/vias. P&P files stands for pick and place, which is a file for all component placements.

Other manufacturing files are schematic, BOM and assembly drawing. Schematic and BOM are discussed in section 3.1.2 and 3.1.3, assembly drawing is essentially a schematic for the assembler that displays the position and orientation for each component. For a more detailed view of the assembly drawing check section A.2 in Appendix A.

3.2 Analysis of the PDN

Using SPICE on Altium I modeled the GAIM PCB using an RLC network, with typical capacitance, resistance and inductance for a 4-layer board.
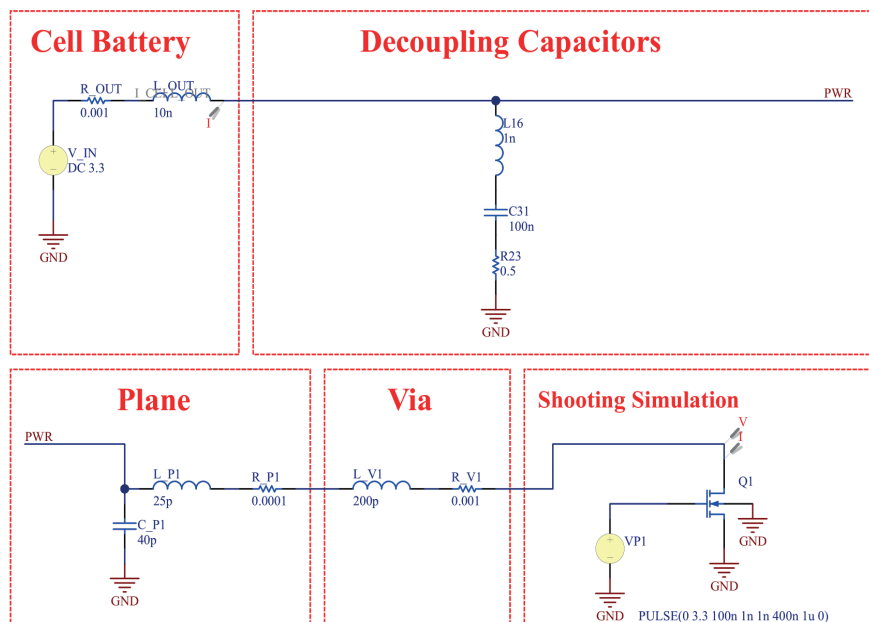
Figure 3.13: Modeled GAIM PCB using an RLC network.

From figure (3.13) we see all the different sections of the PCB, where the shooting simulation will model when the trigger is pulled. The *VP1* voltage source will generate rapid pulses with a 1us period and a rise/fall time of 1ns. In reality the period, and rise/fall time are much slower which will give more stable results. But we want to simulate in the more extreme zones.

The plane section is a simplification of the power distribution network of the PCB.

Current probes are placed at the output of the cell battery and at the drain of the MOSFET, and a voltage probe is placed at the drain of the MOSFET.

The first simulations were transient simulations that ran for three periods, with 25 points per period. There were in total nine transient simulations, varying the ESR, ESL, capacitance value, and the number of decoupling capacitors in parallel for each simulation. The effects on varying different values are presented in section 4.3.1 of the results.

3.2.1 Impedance of the modeled RLC network

Let us now investigate the impedance magnitude proportional to the frequency. By modeling the impedance network that is equivalent to figure (3.13), we get:
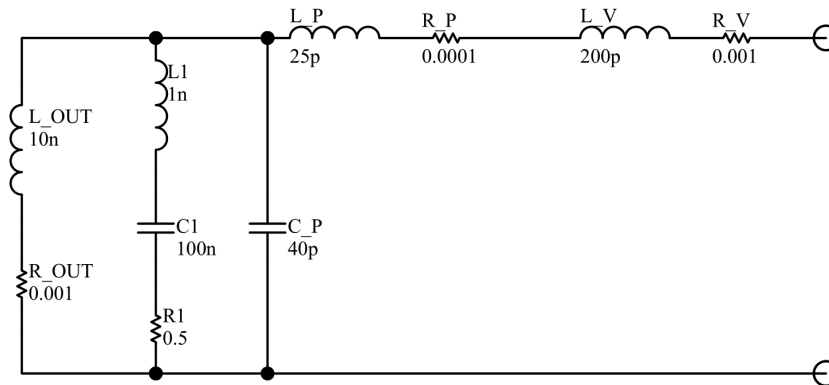
Figure 3.14: Impedance network, including the decoupling capacitor.
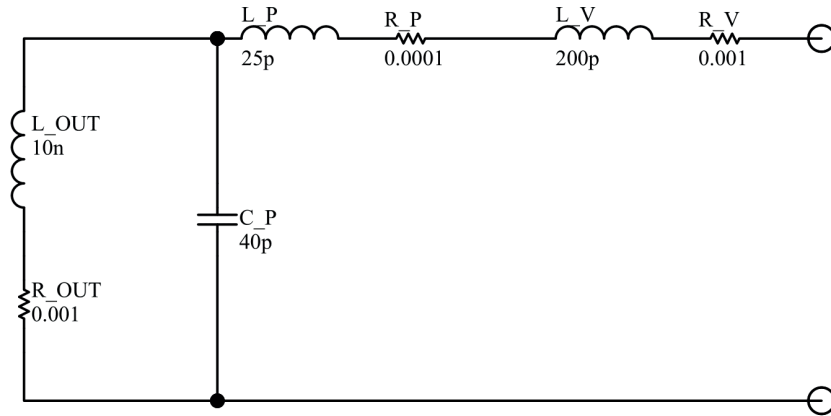
Figure 3.15: Impedance network, excluding the decoupling capacitor.

Calculations of the impedance magnitude with respect to the frequency for figure (3.14) and (3.15) are shown in section 4.3.2 of the results.

3.2.2 Impedance measurements of the PDN on the PCB

To perform real AC impedance simulations for the power delivery network (PDN) on GAIM PCB, the software SIWave was used. ODB++ output files from Altium were used to import the real PCB layout into the simulation program. Running AC impedance simulations will tell us what decoupling capacitors are most optimal to use, and the overall impedance of our power network. Determining the target impedance is very difficult, judging by the substantially allowed voltage margins for the nRF chip, my guess is that the target impedance is in the 10s of ohms. However for simplicity and more extreme zones I will approximate the target impedance to be 0.1 ohm. The cut-off frequency is defined when the PDN impedance magnitude is equal to the target impedance.

The AC simulations of the GAIM PCB are presented in section 4.3.3 of the results.

3.3 Manufacturing & Assembly

3.3.1 Manufactured PCB before assembly
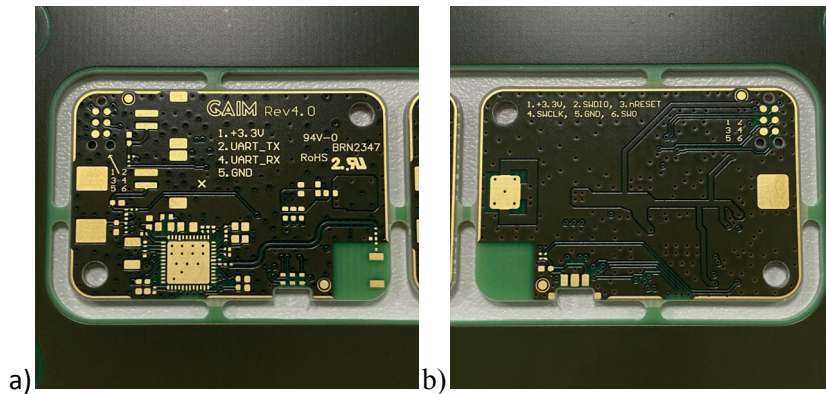
Figure 3.16: (a) Top side of the manufactured PCB (b) Bottom side of the PCB.

3.3.2 Manufactured PCB after assembly
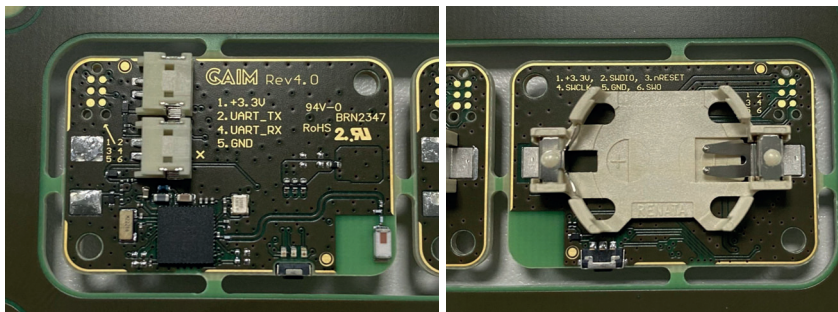
Figure 3.17: Top and bottom side of the assembled GAIM PCB.

In figures (3.16) and (3.17), we have manufactured and assembled boards. The assembly process was done in the lab using a soldering station, microscope and various different tools.

3.4 Flashing & Functionality verification

3.4.1 Flashing the PCB with software

Figure 3.18: Flashing the PCB using J-Link.

Figure (3.18) elucidates the procedure of programming the nRF chip and instilling vitality into the board.

For functionality verification there was a protocol I followed. The protocol is a standard protocol used by SIGMA, for testing PCBs and verifying their functionality.

3.4.2 Functionality verification protocol

The verification protocol follows:

"Bring-up DUT main battery (Vbat) Power:

- Note the DUT power consumption in off mode, check that it does not draw excessive power i.e. is internally shorted.
- Probe all Vbat test & service points to confirm that the voltage is as expected in all nodes i.e. all nodes are physically connected to Vbat.

Bring-up DUT Switch ON:

- Note the DUT total power consumption during power on, check that it does not draw excessive power i.e. is internally shorted. Note max value and value after stabilizing (i.e. boot up is finished)
- Probe all power nodes during startup and verify that they reach correct values (as per product or component specification), note the values. It is common that some power nodes are set to incorrect voltages if SW has not finished, usually then to the power management ICs default values. This is not critical but should be noted and reported. What is critical is if voltages are incorrect due to leakage to other power nodes or ground.

For all GPIO signals, Interrupt, etc., read the component specification to confirm how the pin should be configured, active high / low etc. Measure the voltage level to confirm. Any intermediate voltage level at any time (also measured at startup / shutdown and during operation) is a sign that something is wrongly configured and there is a current leakage.

CPU power up and down:

- Measure Start-up and shut-down sequence of inputs to the CPU, especially the supply voltages. Look at timing and levels, look out for glitches. Verify according to the CPU or platform specification."

Using a switching power supply connected to the GAIM PCB, and an oscilloscope, some measurements were taken by following the protocol above. The measurements are presented in section 4.4 of the results.

3.5 RF/Antenna measurements

Once the PCB is assembled and tested with functionality, I move on to RF and antenna measurements. There are two types of measurements done on the PCB, radiated and conducted.

3.5.1 Total Radiated Power (TRP) measurements

Radiated measurements were done in an antenna chamber that measures total radiated power (TRP) in dBm. As seen below in figure (3.19), the PCB was placed inside the chamber.
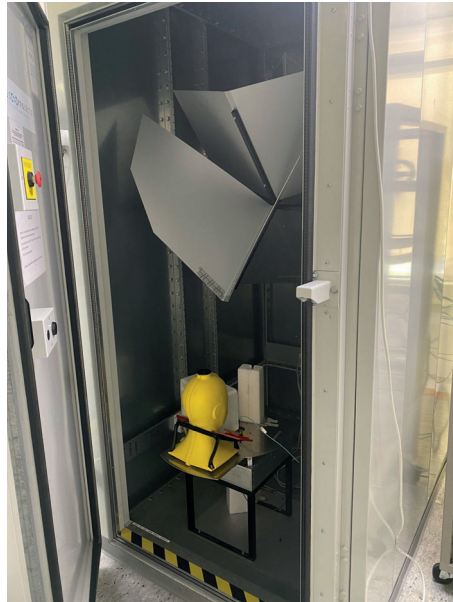
Figure 3.19: RF chamber for radiated measurements.

The new PCB (GAIM 4.0) is flashed with a special test program that emits at three different frequencies (not at the same time, but by pressing the button it will switch between the frequencies). The frequencies are 2402MHz, 2440MHz, and 2480MHz, and thus measuring the trp for each frequency. The flashed program on the chip is set to have a conducted power (power that goes into the antenna, also called input power) of 0 dBm. By referring to the theory in section 2.2.3, we can calculate the antenna efficiency by using equations (2.2.3) and (2.2.4). We measure the total

radiated power, and use the 0 dBm input power to calculate the antenna efficiency.

The measurements were done in three different scenarios. Firstly done with just the GAIM 4.0 PCB, secondly GAIM 4.0 PCB placed in the trigger mechanical unit (refer to figure 1.1), and lastly done with the old design, GAIM 3.0 PCB also placed in the trigger mechanical unit. The results are presented in section 4.5.

3.5.2 Conducted power measurements on the RF trace

Conducted measurements are directly measured on the RF trace on the PCB. By scratching the solder mask (green color) to expose the copper, both on the RF trace and ground plane, I soldered an SMP connector as illustrated in figure (3.20) below.
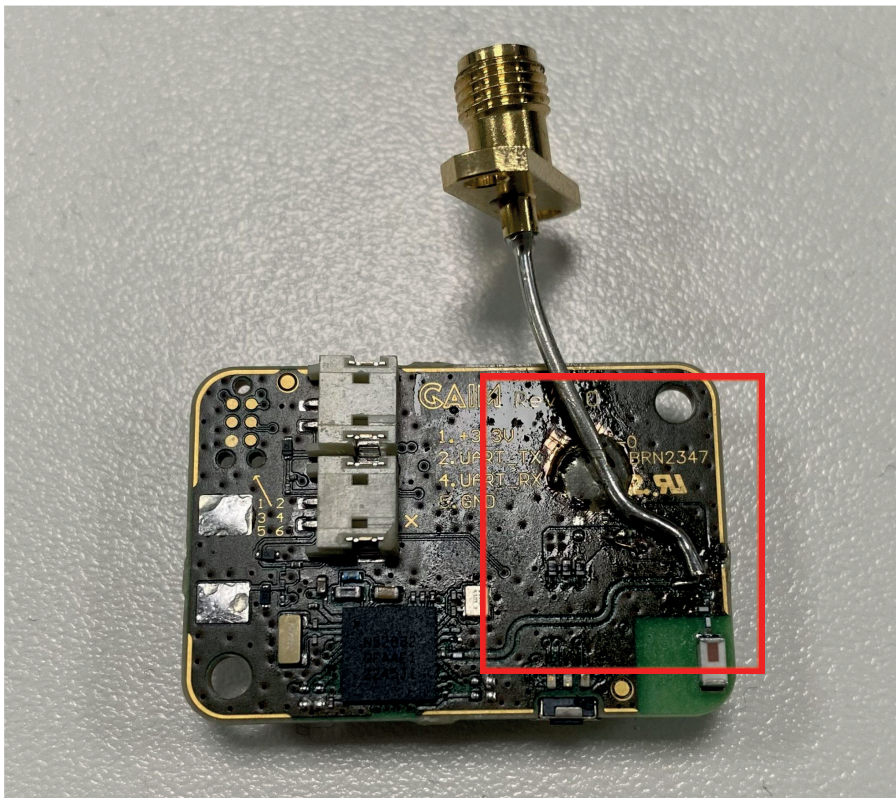
Figure 3.20: GAIM 4.0 PCB with smp connector, soldered to the RF trace.

The smp connector will be directly connected to a spectrum analyzer, to measure the total conducted power, using a different program that will have a conducted power of 4 dBm. The program will allow me to manually sweep through all channels on the bluetooth low energy (BLE) frequency spectrum, and measure the output power on the RF trace, as seen in figure (3.21).
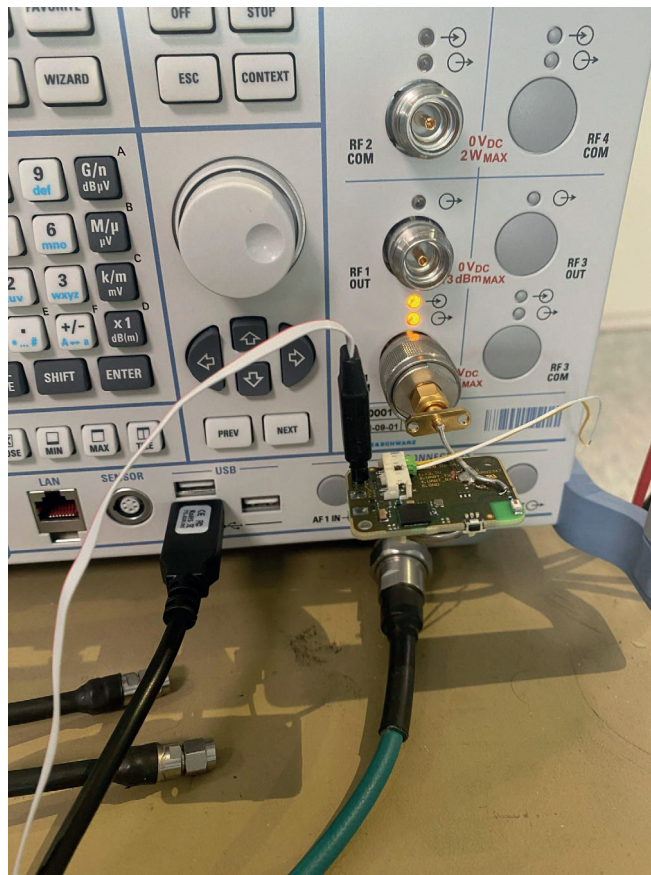
Figure 3.21: Conducted measurements, by manually sweeping through all channels.

The main reason for conducted power measurements is to see the power loss on the RF trace throughout the entire frequency spectrum. For ideal situations the measured conducted power should be 4 dBm on the entire spectrum, however nothing is ideal. The conducted power measurements are presented in section 4.5.2.

3.5.3 Sensitivity measurements on the RF trace

The same setup is used as in figure (3.21) to measure the conducted sensitivity of the new PCB (GAIM 4.0). It is done by starting with a conducted power of -85dBm and sending 300 data packages each time, with a specified checksum. This checksum is used to calculate bit errors. On each iteration the conducted power is lowered by 0.1dBm. The power is lowered all the way until the measured error rate is more than 30%. The lowest conducted power that gives us an error rate less than 30% will be the conducted sensitivity of the chip.

The conducted sensitivity for the RF module on the old PCB can be seen in the ANNA module datasheet [3].

4. Results

4.1 PCB design

This section presents the solution and complexity of swapping out the ANNA-B112 RF module, and fitting the nRF chip with discrete components, which are shown in figures (4.1) and (4.2). Additionally some optimizations from an ESD protection aspect were made to the new revision.

4.1.1 Fitting the nRF and discrete components
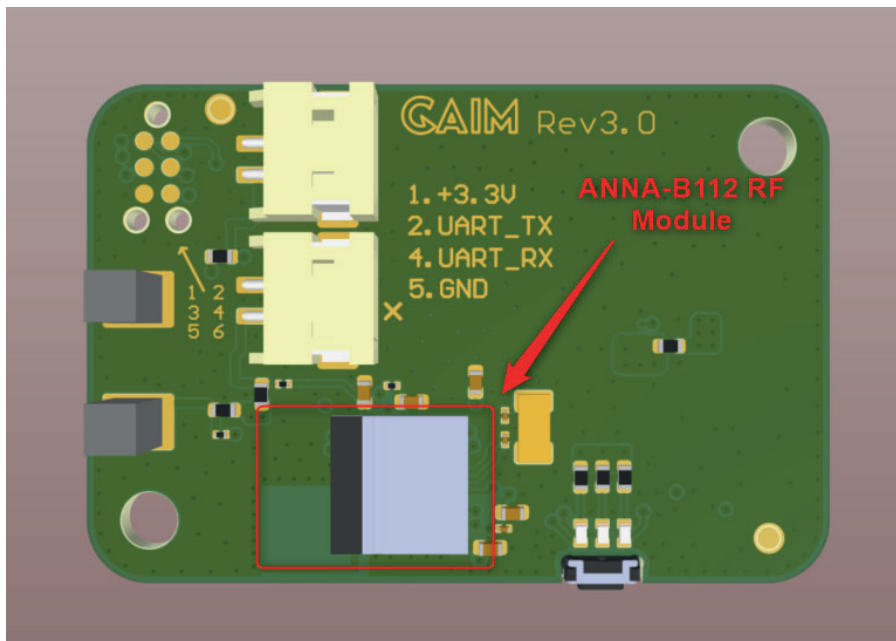
Figure 4.1: PCB from the previous design of GAIM (Rev3.0), with the ANNA-B112 RF module.
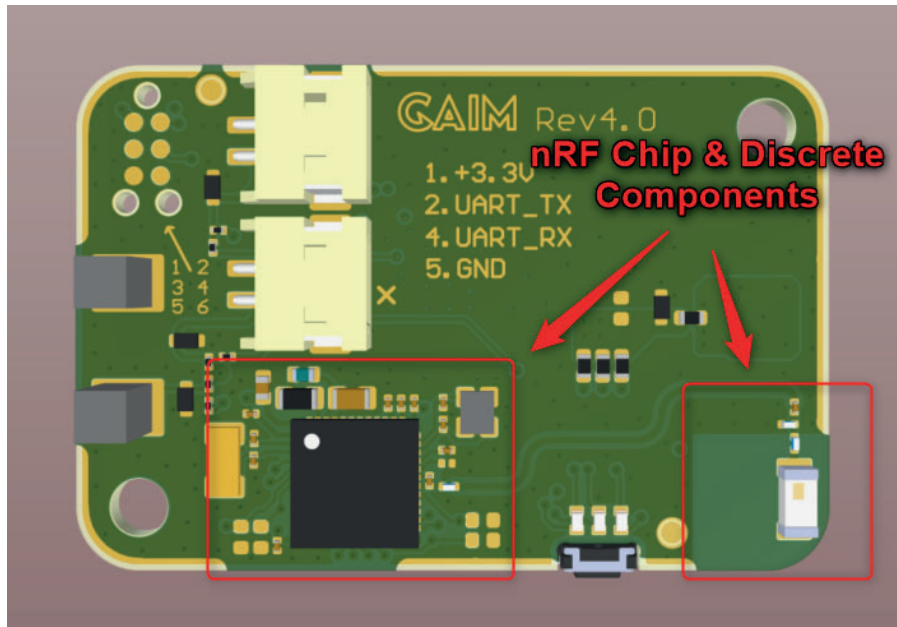
Figure 4.2: New revision of the GAIM PCB, fitted with nRF chip and discrete components (Rev4.0).

4.1.2 ESD protection optimization

From figures (4.2) and (3.16), we see the ESD protection design technique implemented. The soldermask has been removed on the edges of the PCB exposing the GND copper plane, and various ESD diodes were placed near each external connector (including the two big connectors and the button).

4.2 Cost aspect

In this section the cost considerations are presented. We will look at the reduction of component cost and the cost for certification of the boards.

4.2.1 Component cost reduction

Manufacturer Part No	Quantity	Supplier 1	Average Component Price	Total Unit Cost
ERJ-2GE0R00X	1	Digi-Key	0,2305833333	168,114177
RMCF0201FT10K0	4	Digi-Key	0,2469657143	
CBR02C120F3GAC	2	Digi-Key	1,874705	
RC0402FR-0762RL	3	Digi-Key	0,2213214286	
RC0402FR-07100KL	4	Digi-Key	0,2213214286	
0201X104K6R3CT	1	Mouser	0,26122625	
223GMSAAR	1	Digi-key	2,54895	
ANNA-B112	1	Digi-key	93,485196	
APHHS1005LCGCK	1	Digi-key	2,413238	
APHHS1005LSECK/J3-PF	1	Digi-key	3,4724775	
APHHS1005LSYCK/J3-PF	1	Digi-key	3,580445	
CM7V-T1A-32.768KHZ-9PF-20PPM-TA-QC	1	Digi-Key	6,38402	
ED90501-ND	2	Digi-Key	3,222883333	
ESD351DPYR	4	Digi-Key	2,220622857	
S2B-ZR-SM4A-TF(LF)(SN)	2	Digi-key	5,19463	
SMTU2032-lf	1	farnell	23,734	

Table 4.1: Total component cost of the old revision of GAIM (SEK).

Manufacturer Part No	Quantity	Supplier 1	Average Component Price	Total Unit Cost
2450AT18B100E	1	Digi-Key	4,667524286	125,6248603
SMTU2032-lf	1	farnell	23,734	
GJM0335C1E120FB01D	6	Digi-Key	0,523075	
GCM188R71C105KA64D	1	Digi-Key	0,8541416667	
GRM155R71E104KE14J	3	DigiKey	0,228205	
GRM188R61A475KAAJD	1	Digi-Key	1,963081667	
GRM0335C1E101JA01D	1	Digi-Key	0,1786925	
GJM0335C1ER80WB01D	1	Digi-Key	0,6979825	
GJM0335C1H1R0BB01D	1	DigiKey	0,36437625	
APHHS1005LSECK/J3-PF	1	Digi-key	3,4724775	
APHHS1005LSYCK/J3-PF	1	Digi-key	3,580445	
APHHS1005LCGCK	1	Digi-key	2,413238	
0402HS-150EKTS	1	Digi-Key	1,70962625	
LQM18DZ100M70L	1	Mouser	1,6441925	
LQP03HQ3N9C02D	2	Mouser	0,9289155556	
LQP03HQ2N2C02D	1	Mouser	0,9289155556	
ED90501-ND	2	Digi-Key	3,222883333	
RC0402FR-0762RL	3	Digi-Key	0,2213214286	
RC0402FR-07100KL	4	Digi-Key	0,2213214286	
ERJ-2GE0R00X	1	Digi-Key	0,2305833333	
RMCF0201FT10K0	4	Digi-Key	0,2469657143	
223GMSAAR	1	Digi-key	2,54895	
NRF52832-QFAA-R	1	Digi-key	41,02303286	
CM7V-T1A-32.768KHZ-9PF-20PP	1	Digi-Key	6,38402	
CX2016DB32000D0WZRC1	1	Digi-Key	5,683313333	
ESD351DPYR	4	Digi-Key	2,220622857	

Table 4.2: Component cost for the new revision of the board (SEK).

To calculate the cost saved in percentage I use (4.2.1).

$$1 - \frac{New\ Component\ Cost}{Old\ Component\ Cost} = 1 - \frac{125.6}{168.1} = 1 - 0.74 = 0.26 \qquad (4.2.1)$$

$$C_{Saved} = 168.1 - 125.6 = 42.5 \qquad (4.2.2)$$

Where C_{Saved} is the cost saved per unit. Since the PCB outline, stack-up, and the design technology are the same for both the old and new revision, the cost for manufacturing the boards will be the same.

The overall component cost from a production perspective can be calculated using (4.2.3) and (4.2.4).

$$C_{ANNA} = 168.1 * n \qquad (4.2.3)$$

$$C_{nRF} = 125.6 * n \qquad (4.2.4)$$

Where C_{ANNA} is the total component cost with n units produced using revision 3.0, C_{nRF} is the total component cost with n units produced using revision 4.0.

4.2.2 Certification cost

The certification cost is classified, therefore I will approximate the cost to be around 100000 SEK (which was a reasonable cost when discussing with the engineers at Sigma). Let's investigate what the certification cost is proportional to the production quantity for the previous design.

Production Quantity	10	100	1000	10000	50000
Certification Cost per unit (SEK)	10000	1000	100	10	2
Total Cost Per Board (SEK)	10168	1168	268	178	170

Table 4.3: The certification cost per unit, proportional to the production quantity (GAIM 3.0).

Since the nRF chip requires two certifications, let us estimate the cost for simplicity to be 200000 SEK. The cost proportional to the production quantity would be:

Production Quantity	10	100	1000	10000	50000
Certification Cost per unit (SEK)	20000	2000	200	20	4
Total Cost Per Board (SEK)	20126	2126	326	146	130

Table 4.4: The certification cost per unit, proportional to the production quantity (GAIM 4.0).
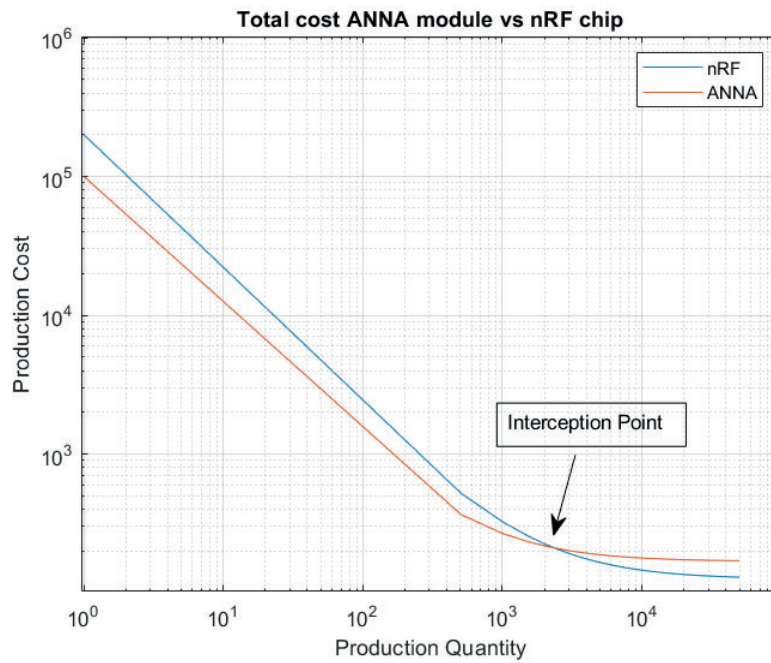
Figure 4.3: The total production cost per board, proportional to the production quantity. The cost includes the component cost and the certification cost (in SEK).
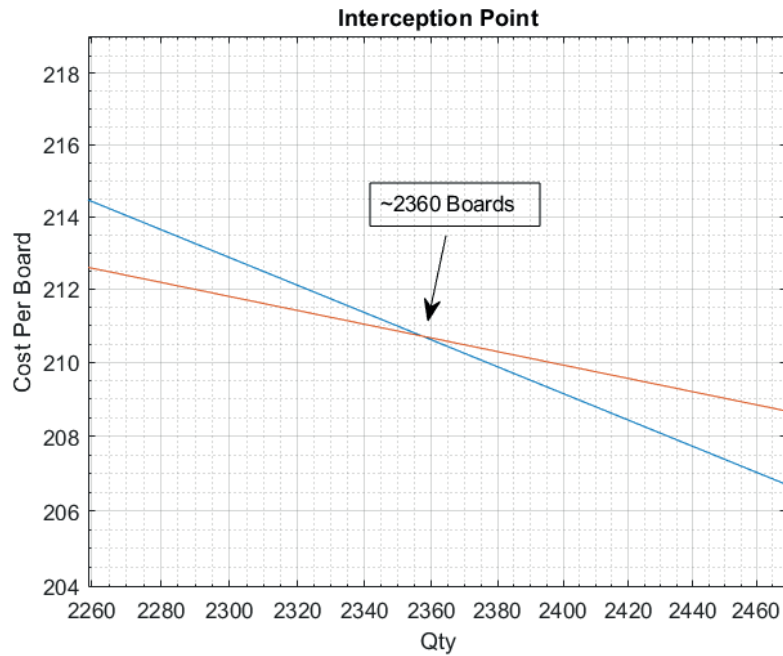
Figure 4.4: Interception point between the ANNA module and nRF chip.

The interception point is the production quantity where the cost for the ANNA module is the same as the nRF chip (including the certification costs). The quantity above the interception point means the nRF is cheaper to produce, and vice versa when the quantity is below the interception point.

4.3 PDN impedance simulations/measurements

4.3.1 Transient simulations on the modeled RLC network

Firstly presenting the transient simulations from the modeled RLC network, as seen in figure (3.13).

4.3.1.1 Varying the capacitance

The results when varying the capacitance value of the decoupling capacitor:
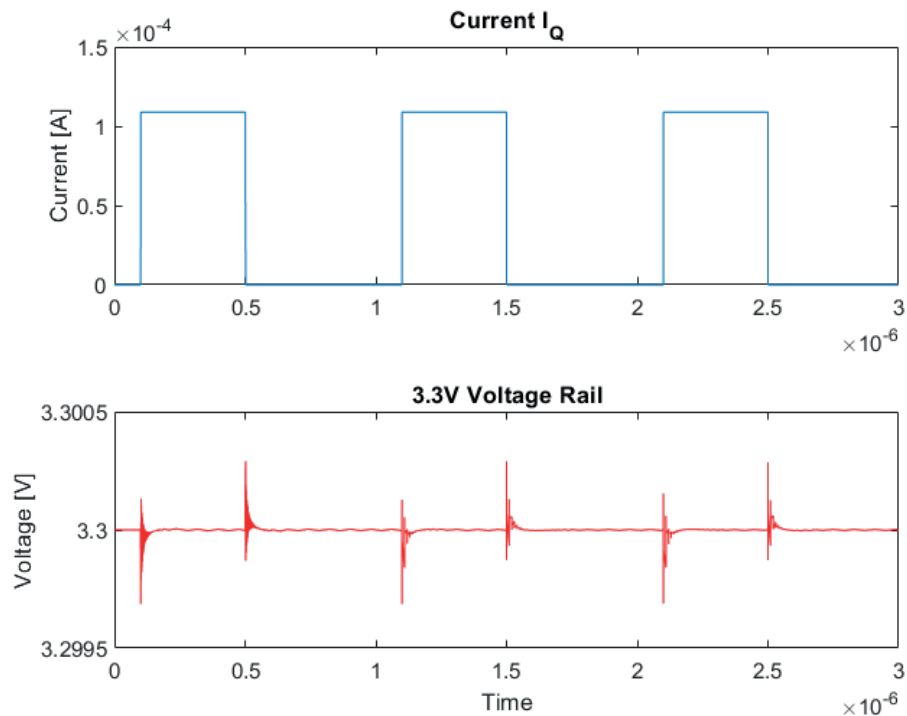
Figure 4.5: Transient simulation, C=100nF, ESR=0.5Ohm, ESL=1nH. This will be the reference figure.
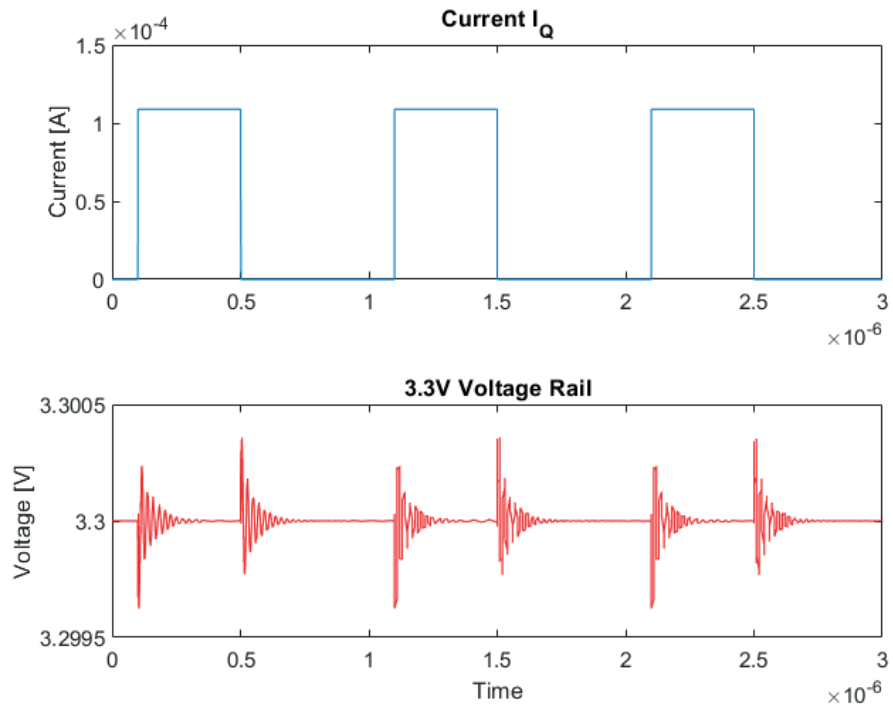
Figure 4.6: Transient response on the supply voltage with C=1nF, ESR=0.5Ohm, ESL=1nH.
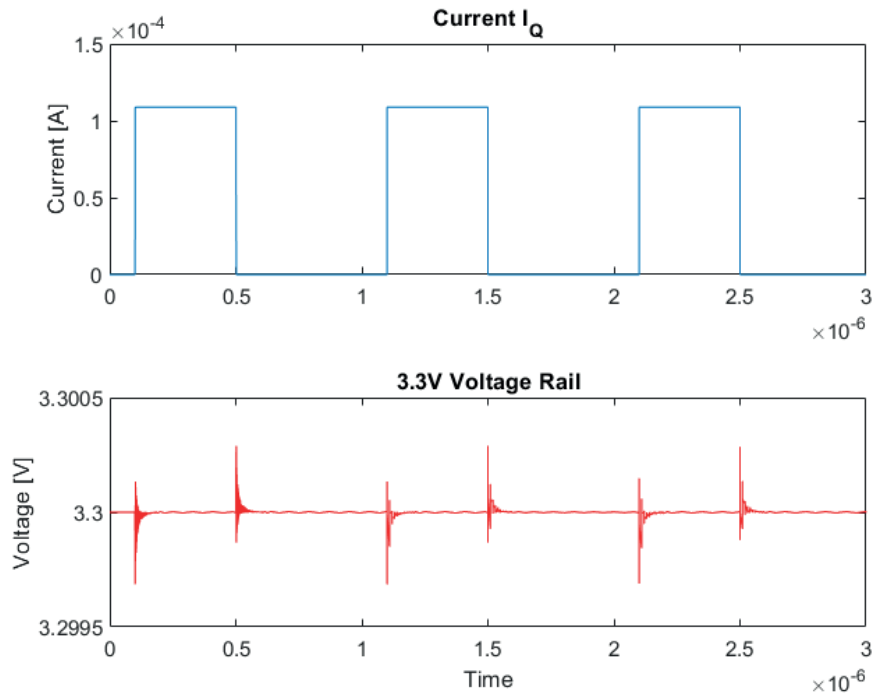
Figure 4.7: Transient response on the supply voltage with C=1000nF, ESR=0.5Ohm, ESL=1nH.

In figure (4.5-4.7) the capacitance of the decoupling capacitor varies from 1nF to 1000nF. The top plot of each figure displays the current I_Q, which is the trigger shooting simulation. The bottom plot illustrates what happens to the 3.3V supply voltage, which is the power distribution network. As shown, there are some voltage variations and ringing depending on the capacitance value. Lower capacitance will give significantly more ringing, however there seems to be minimal difference between 100nF and 1000nF.

4.3.1.2 Varying the ESR
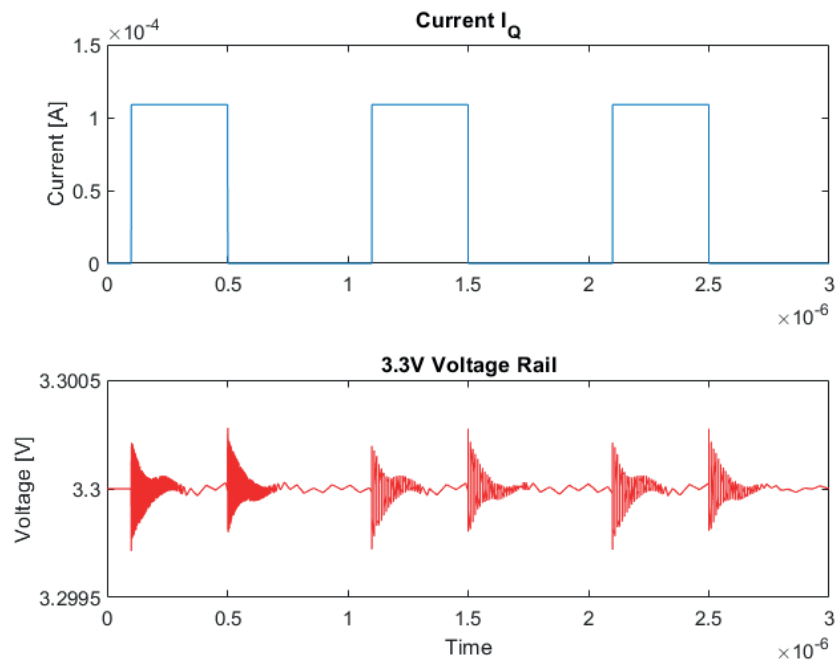
Figure 4.8: Transient response on the supply voltage with C=100nF, ESR=0.05Ohm, ESL=1nH.
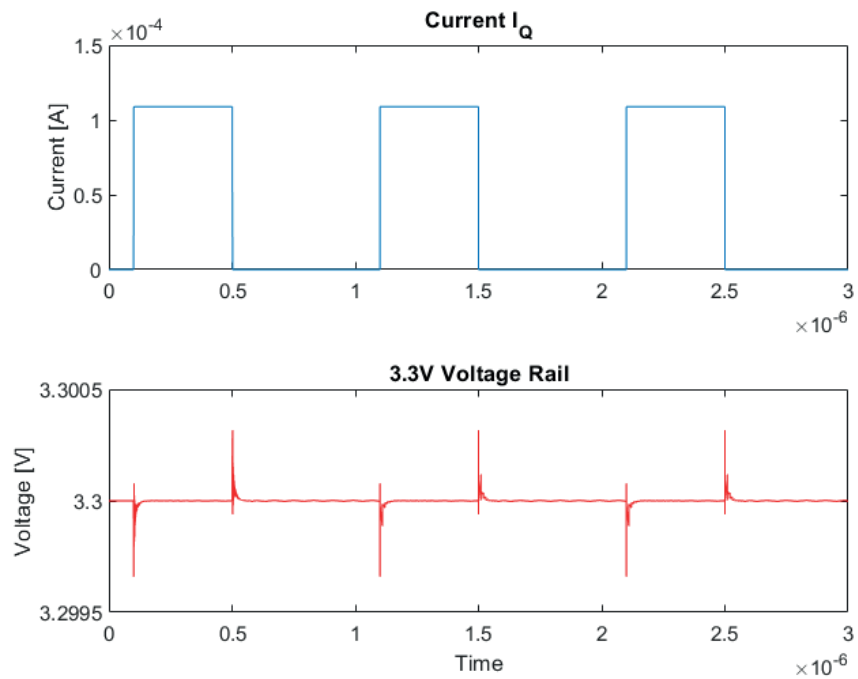
Figure 4.9: Transient response on the supply voltage with C=100nH, ESR=1 Ohm, ESL=1nH.

Figures (4.8-4.9) illustrate voltage variations on the 3.3V supply voltage depending on the ESR of the capacitor. Higher ESR will give less ringing variations on the supply voltage.

4.3.1.3 Varying the ESL
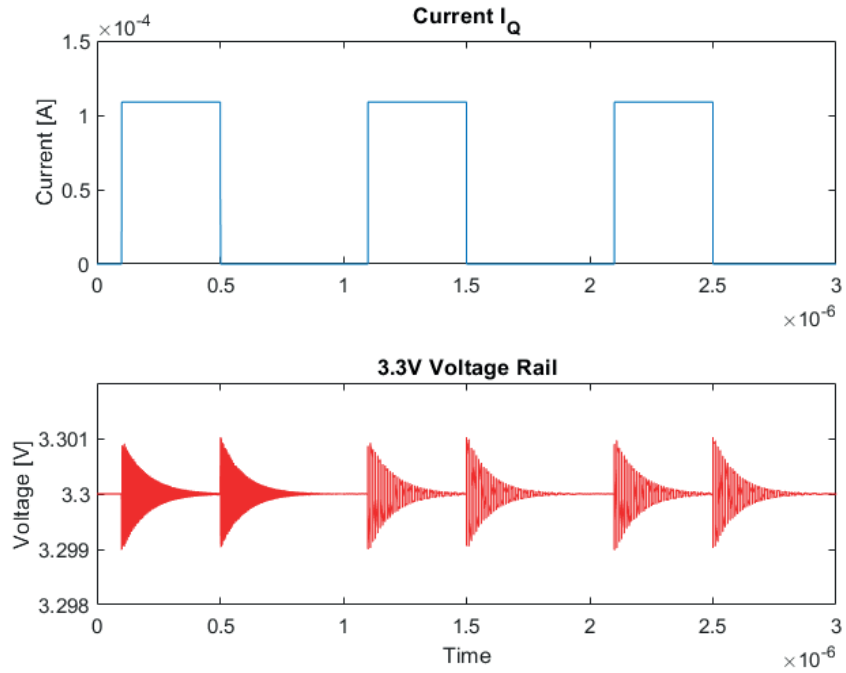
Figure 4.10: Transient response on the supply voltage with C=100nF, ESR=0.5Ohm, ESL=10nH.
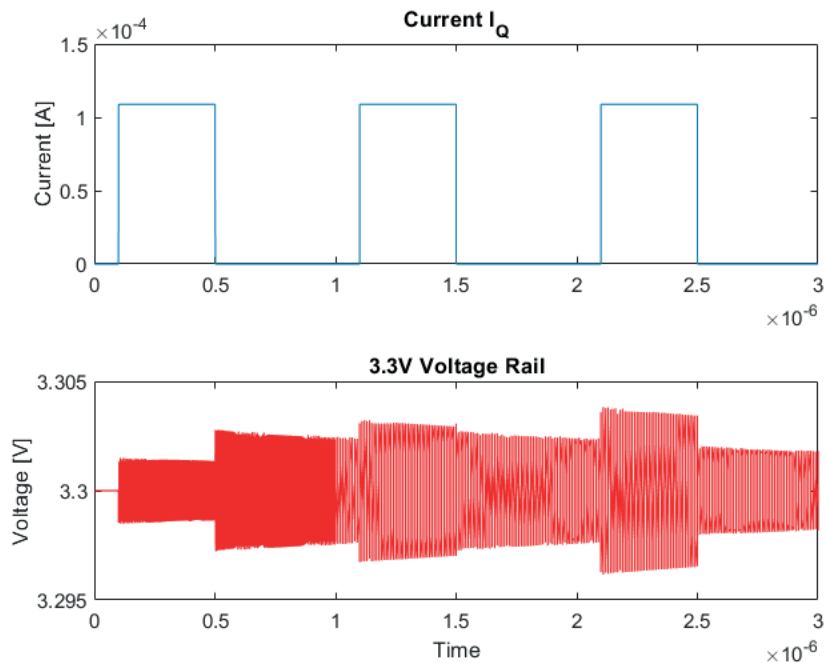
Figure 4.11: Transient response on the supply voltage with C=100nF, ESR=0.5Ohm, ESL=100nH.

From figures (4.10-4.11) we see that there are extreme ringing variations on the supply voltage when increasing the ESL value on the decoupling capacitor.

As seen in figures (4.5-4.11) there are unwanted oscillations on the supply voltage, when varying capacitance, ESR, and ESL for the decoupling capacitor, due to inductances and capacitances on the PDN and the decoupling capacitor. Ideally we want a capacitor with medium to higher capacitance, higher ESR and lower ESL for best results.

4.3.1.4 Decoupling caps in parallel & no decoupling caps

Let me also include when having multiple decoupling capacitors in parallel, and having no decoupling capacitors at all.
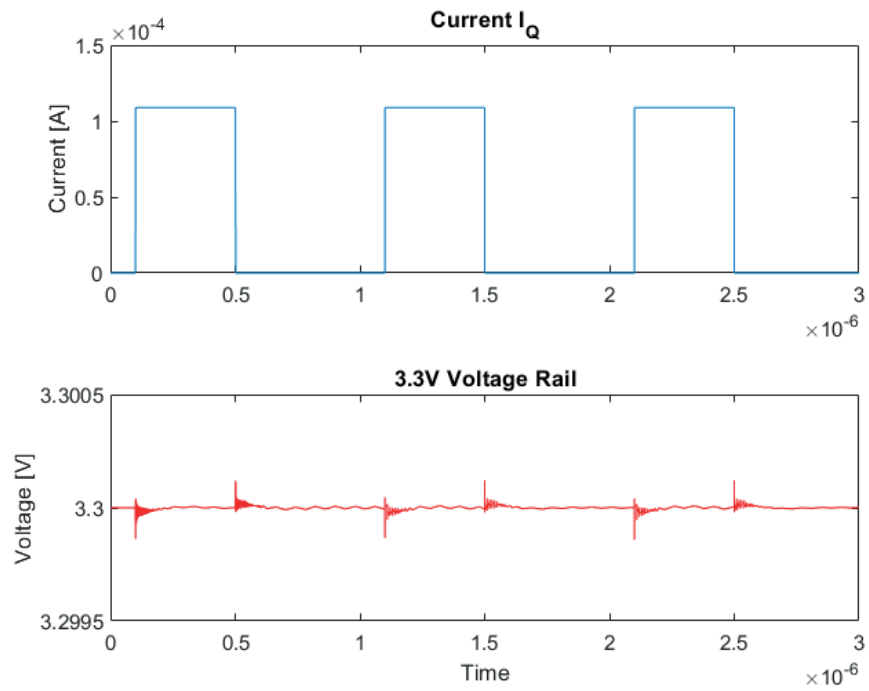
Figure 4.12: Transient response on the supply voltage with C=100nF, ESR=0.5Ohm, ESL=1nH, with multiple decoupling capacitors.
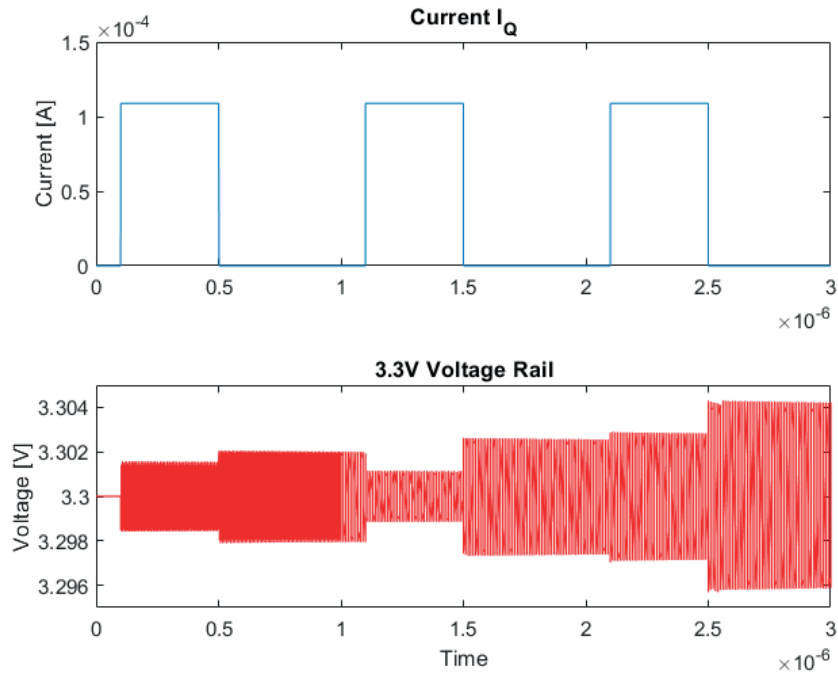
Figure 4.13: Transient response on the supply voltage with no decoupling capacitors.

As seen from figures (4.12-4.13), having multiple decoupling capacitors in parallel is very desirable for reducing both ringing and voltage spikes on the supply voltage. Having no decoupling capacitors is however very undesirable.

4.3.2 Impedance simulations on the modeled RLC network

Secondly we move on to the impedance calculations of the RLC network from figure (3.14) and (3.15). From figure (3.14) we get:

$$Z_{With}(\omega) = ((R_{out} + j\omega L_{out}) \,||\, (R_1 + j(\omega L_1 - \frac{1}{\omega C_1})) \,||\, \frac{1}{j\omega C_p} +$$

$$+ ((R_p + R_v) + j\omega(L_p + L_v)) \tag{4.3.1}$$

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From figure (3.15) we get:

$$Z_{Without}(\omega) = ((R_{out} + j\omega L_{out}) \mathbin{\|} \tfrac{1}{j\omega C_p}) +$$

$$+ ((R_p + R_v) + j\omega(L_p + L_v)) \qquad (4.3.2)$$

Where R_{out} is the internal battery resistance, L_{out} is the inductance of the battery, R_1 is the ESR of the decoupling capacitor, L_1 is the ESL of the decoupling capacitor, C_1 is the capacitance of the decoupling capacitor, C_p is the capacitance of the power distribution plane, R_p is the plane resistance, L_p is the plane inductance, R_v is the via resistance, and L_v is the via inductance.

Using (4.3.1) and (4.3.2) I plot the impedance magnitude with respect to frequency, including when increasing the number of decoupling capacitors in parallel.
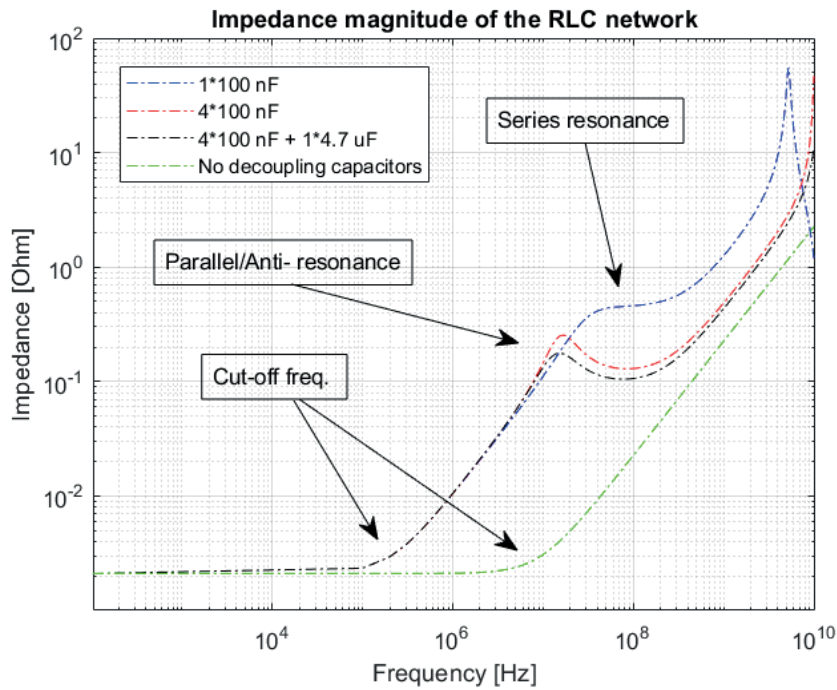
Figure 4.14: Impedance simulations of the modeled GAIM RLC network.

Figure (4.14) yields a very interesting result that is not fully concurrent with the theory. This will further be discussed in section 5.3 in the conclusion.

4.3.3 Impedance measurements on the PDN of GAIM 3.0 & 4.0 PCBs

The results above have only been from the modeled RLC network using figure (3.13). The figures in this section present the real AC impedance measurements on the PDN using the GAIM 3.0 and GAIM 4.0 PCBs.

Firstly, all simulations below are done on the upgraded PCB (GAIM 4.0):
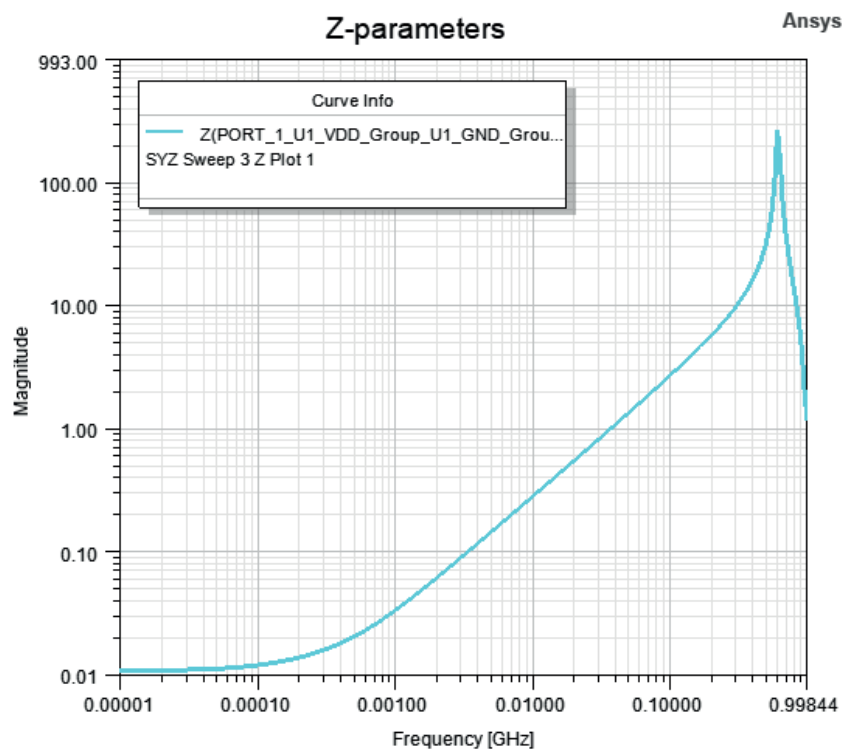
Figure 4.15: AC impedance simulation, with no decoupling capacitors.

In figure (4.15) we see that the impedance magnitude frequency response on the PDN is concurrent with the theory. We have a cut-off frequency of about 3.5MHz, since the target impedance is approximated to be about 0.1 Ohms.

The next few measurements were done with different decoupling capacitors.
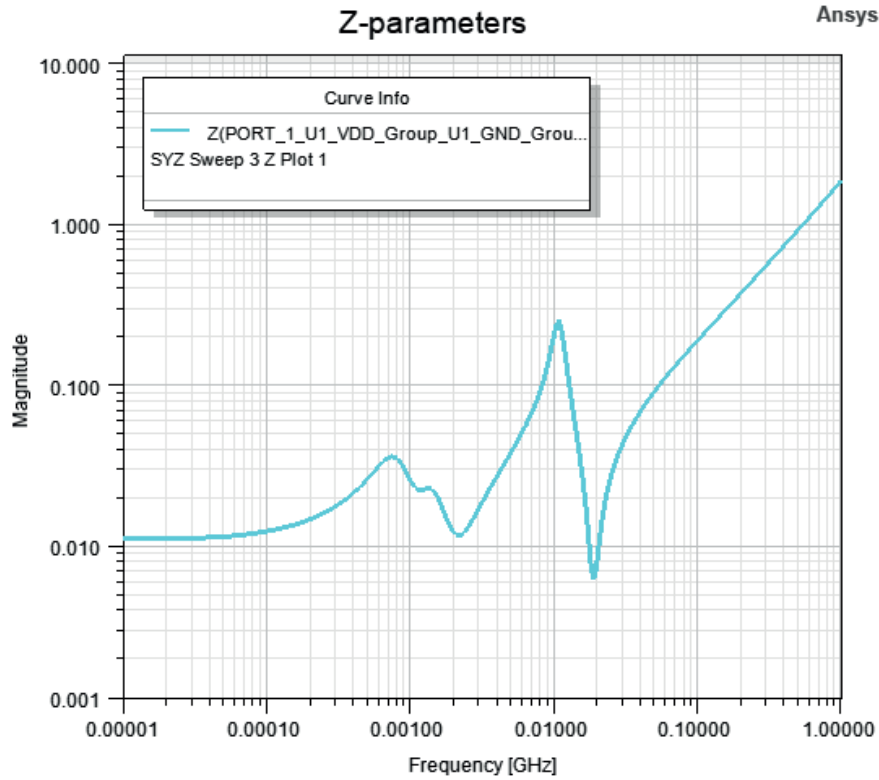
Figure 4.16: AC impedance simulations, all decoupling capacitors are C=100nF.

In figure (4.16) we see parallel resonant peaks at around 70kHz, 105kHz and 10MHz, due to all the decoupling capacitors, which is expected according to the theory. However the peak at 10MHz goes above the target impedance, making the cut-off frequency 30MHz.
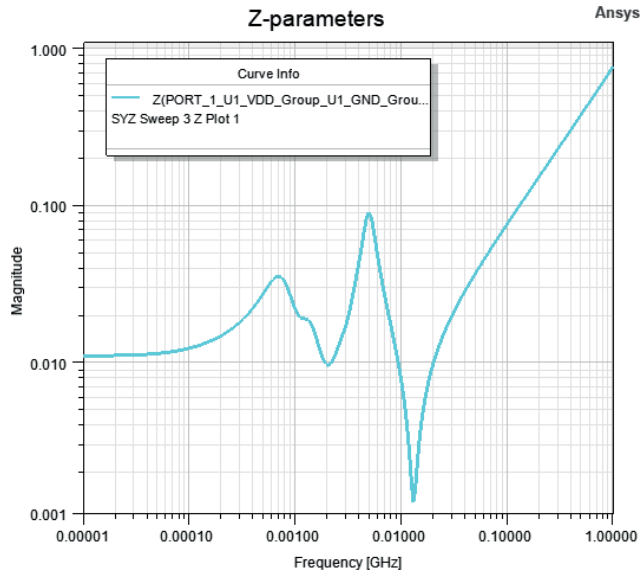
Figure 4.17: AC impedance simulations, all decoupling capacitors are
C=1uF.
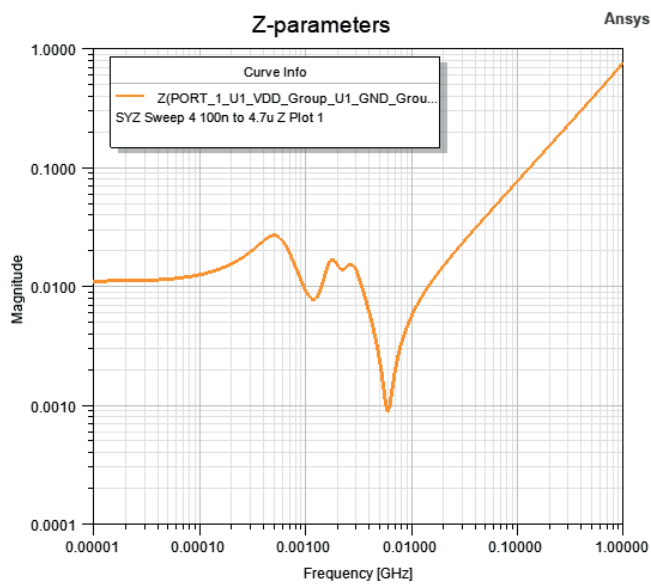
Figure 4.18: AC impedance simulations, all decoupling capacitors are
C=4.7uF.

Figures (4.17-4.18) are both good enough, since the resonant peaks are less than the target impedance. According to theory in section 2.3.3 equation (2.3.10), larger capacitors will give smaller peaks, which is congruent with the measurements. The cut-off frequencies are now at 105MHz. However having larger capacitance will lead to physically larger capacitors, which will make the design process more complex, due to having constraint size of the PCB outline.
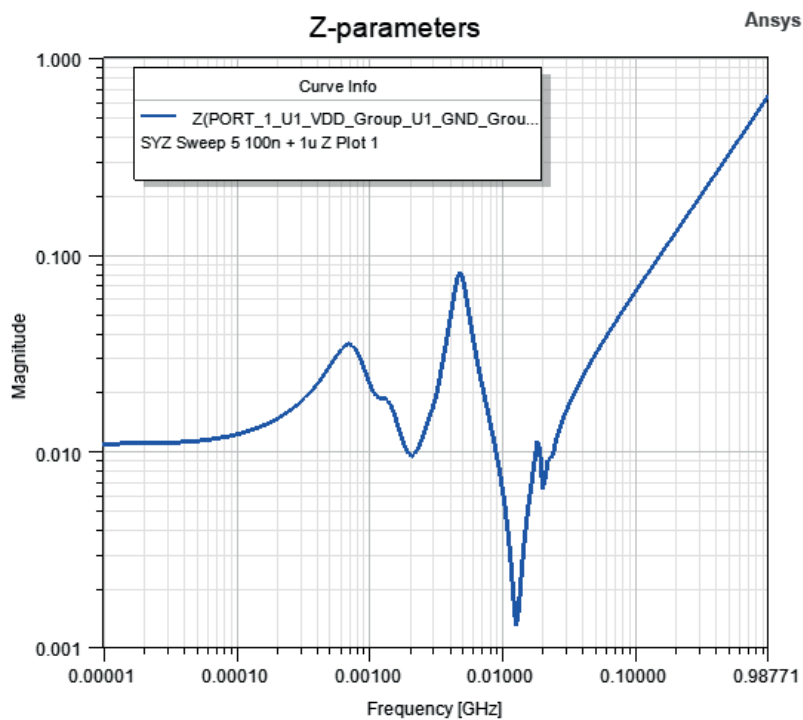
Figure 4.19: AC impedance simulations, all decoupling capacitors are C=100nF in parallel with C=1uF.
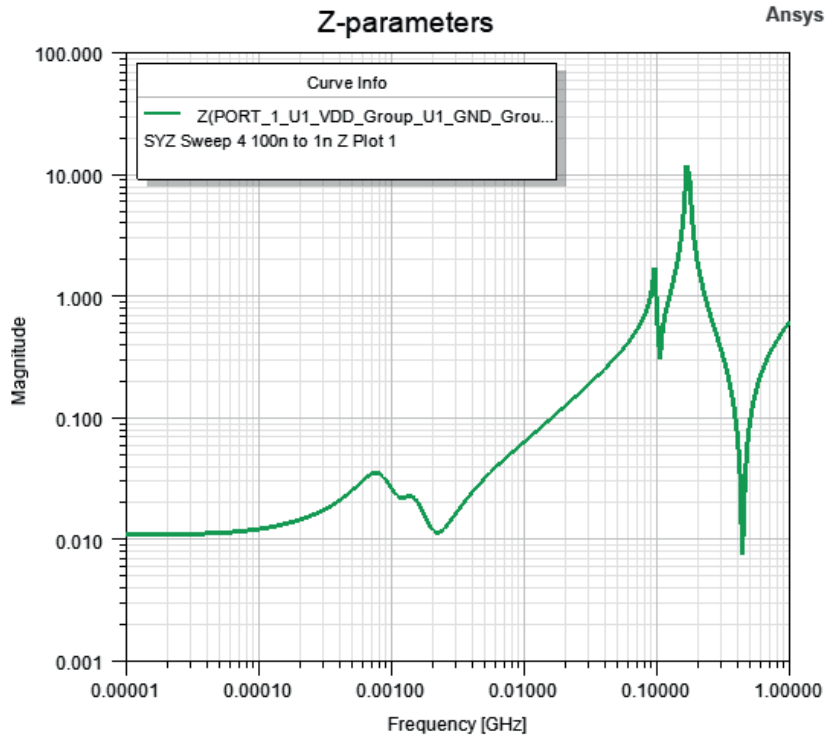
Figure 4.20: AC impedance simulations, all decoupling capacitors are C=1nF.

Figures (4.19-4.20) are more simulations with different capacitance values, which are also good enough.

The simulation below was done on the old version of the PCB (GAIM 3.0):
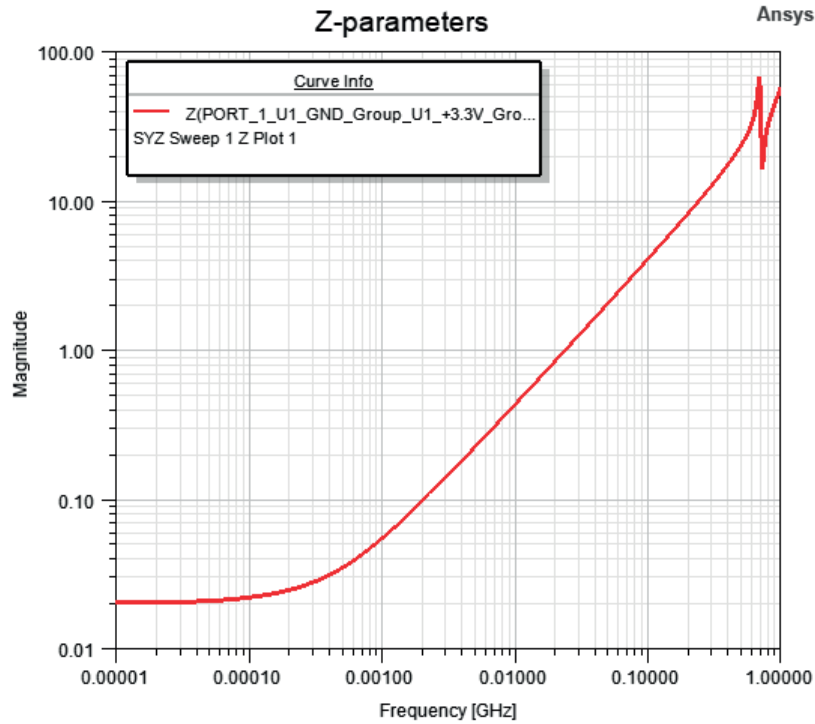
Figure 4.21: AC impedance simulation, no decoupling capacitors.

Comparing figure (4.15) and (4.21) we see an improvement of the power distribution network impedance with a factor of 2 in the DC range on the upgraded GAIM 4.0 PCB. The improvement is due to having larger power planes on the PDN, compared to the old version, using no planes, but instead traces on the PDN. The cut-off frequency had a minuscule improvement of 3.5MHz in figure (4.15), and 2MHz on the old PCB according to figure (4.21), resulting in an improvement of 1.5MHz.

4.4 Functionality verification

The figures below present the results from the verification protocol when testing the GAIM PCB. The testing was done with an oscilloscope and setting the trigger on both rising and falling edges to measure different nodes and their behaviors during power on and off. We want to see if the power nodes on the PCB reach the desired voltage, provided by a switching power supply.

4.4.1 VBAT PWR measurements (GAIM 4.0)
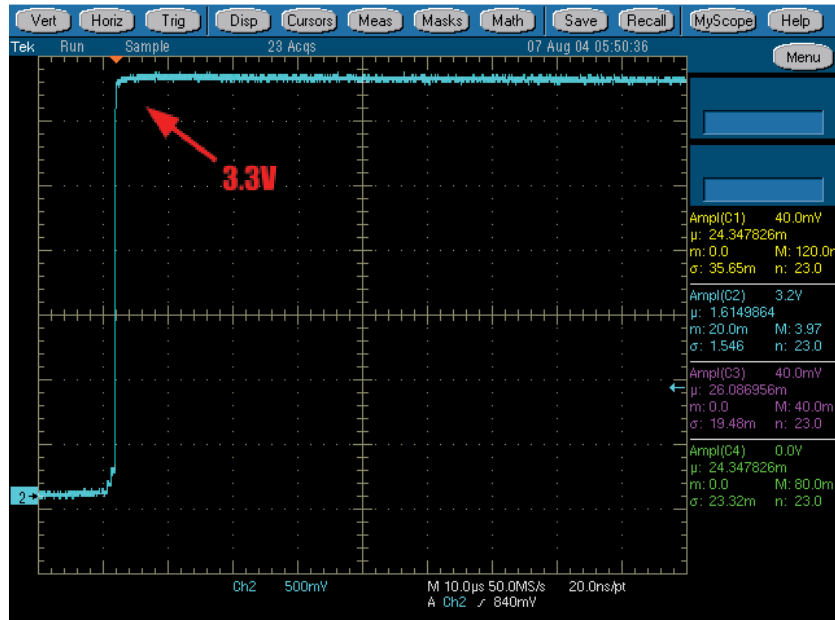
Figure 4.22: Measurements on the main VBAT power node.

Figure (4.22) displays the battery voltage measured on the pad where the battery holder is soldered. As we see from the figure, VBAT node reaches the desired voltage of 3.3V during turn-on of the switching power supply.

Figure 4.23: Measurements on the first (and only) VBAT power plane.

From figure (4.23) we see the measurements done on the VBAT power plane that is connected to the pad measured in figure (4.22). As expected this power plane reaches the desired voltage of 3.3V during turn-on.

4.4.2 VDD measurements
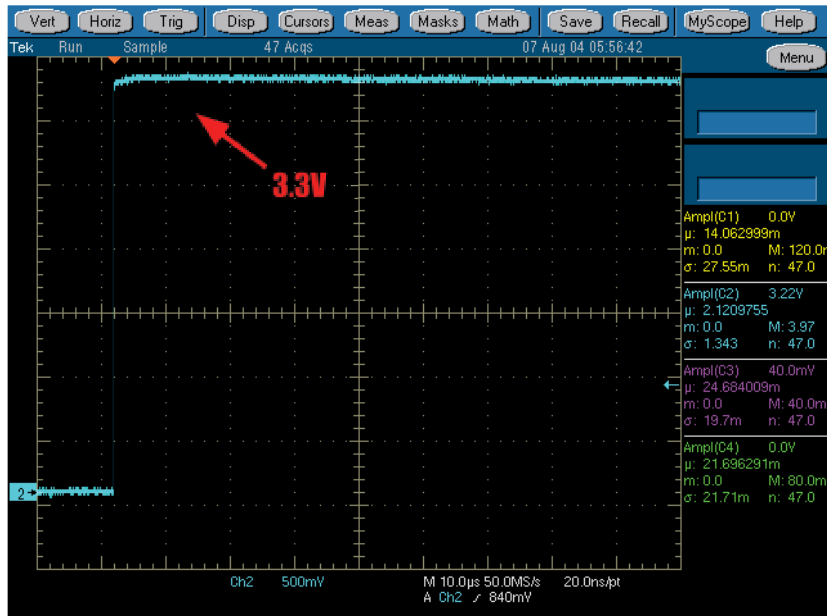
Figure 4.24: VDD measurements on the LED resistors.

The VDD power network is connected to the VBAT power plane through a 0R resistor, which technically means that the entire VDD network should have the same voltage as VBAT. The VDD measurements in figure (4.24) were taken on the resistors that connect to the LEDs. As expected the VDD on the resistors reach the desired voltage of 3.3V. It is important to check that the VDD reaches the desired voltage on all the VDD nodes across the PCB, which will indicate that all sections of the board have access to the supply power.
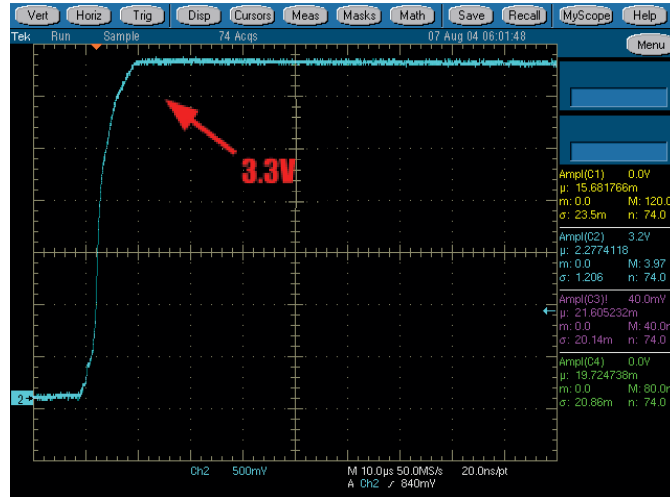
Figure 4.25: VDD measurements on the big capacitor near nRF.

Figure 4.26: VDD measurements on the small capacitor near nRF.

Same VDD measurements are done on the larger and smaller decoupling capacitors near the nRF chip, illustrated in figure (4.25-4.26). This means that the chip is getting the correct power. However the desired voltage takes longer to achieve as seen in figure (4.25). This is due to the initial charging of the large capacitor.
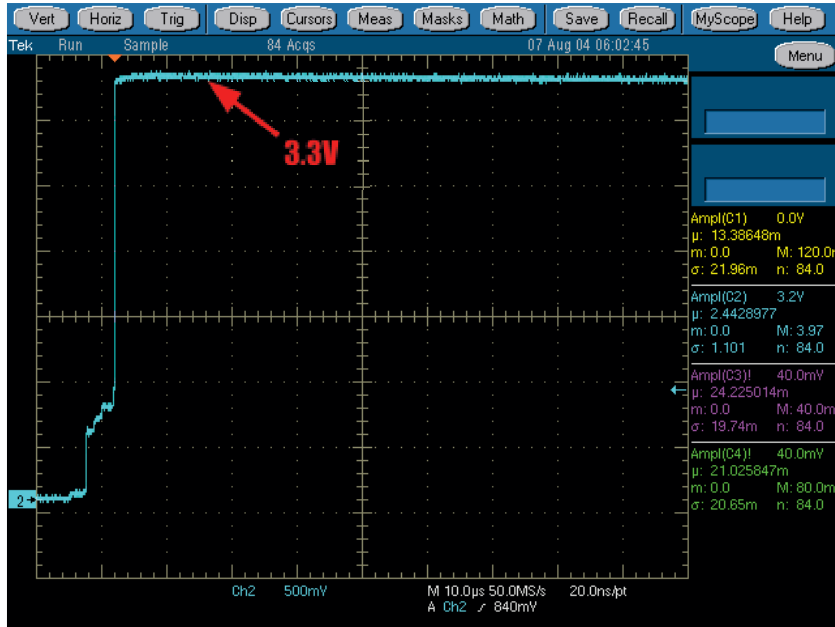
Figure 4.27: VDD measurements after the PU resistor on connector 1.
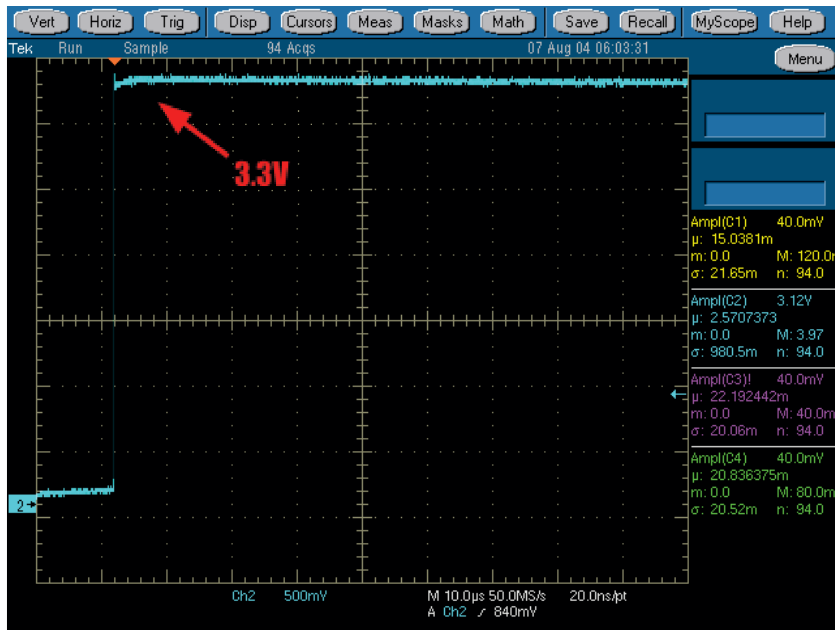
Figure 4.28: VDD measurements after the PU resistor on connector 2.
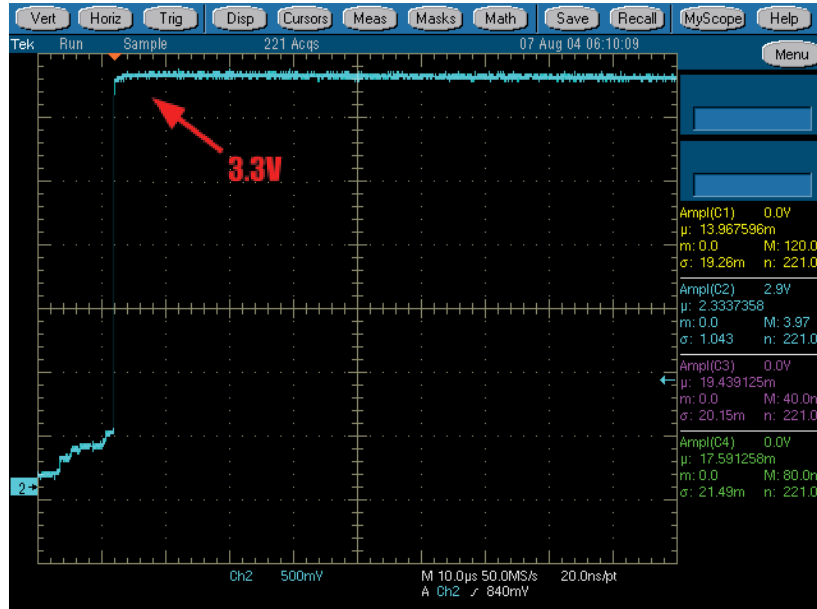
Figure 4.29: VDD measurements after the PU resistor on the button.

From figures (4.27-4.29) the VDD measurement is done after the pull-up resistor on each external connector/switch. As seen from the figures all the nodes are pulled up to the desired voltage by the resistor. This is important due to the fact that each GPIO in use connecting to the nRF chipset needs to be recognized as a logic high, otherwise we would not be able to detect triggers and button presses etc.
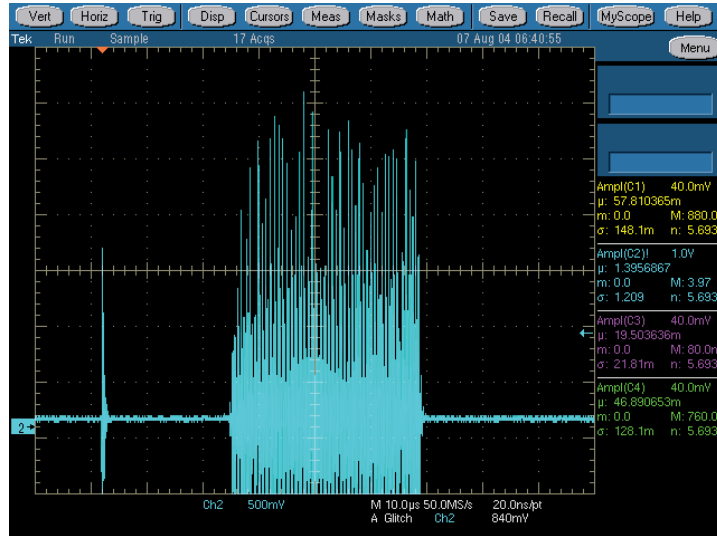
Figure 4.30: VDD on big capacitor near nRF during switch-on.

Changing the trig on the oscilloscope to detect glitches on the VDD. Figure (4.30) displays some glitches on the 3.3V rail voltage, due to high frequency components coming from the switching power supply. However during ideal operation the PCB will use a cell battery, and these high frequency components will not be present.

4.4.3 GPIO measurements during triggering (GAIM 4.0)
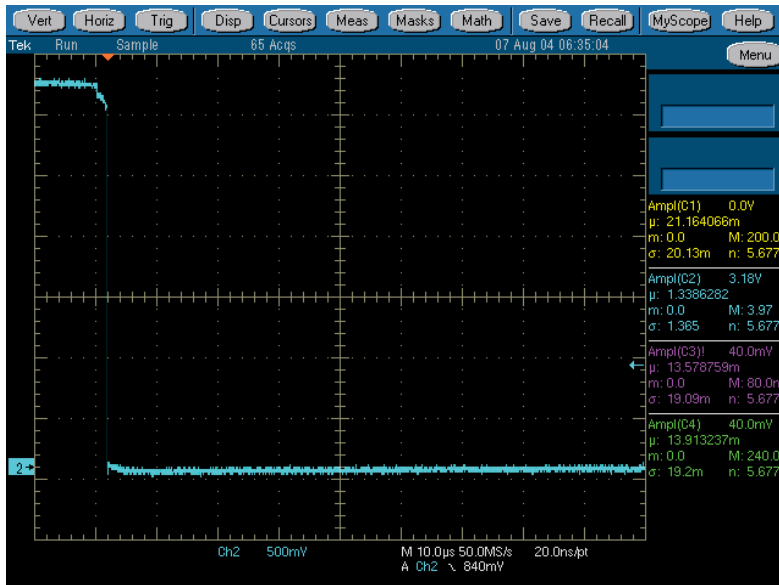
Figure 4.31: Measurements on connector 1, falling edge during a trigger switch.
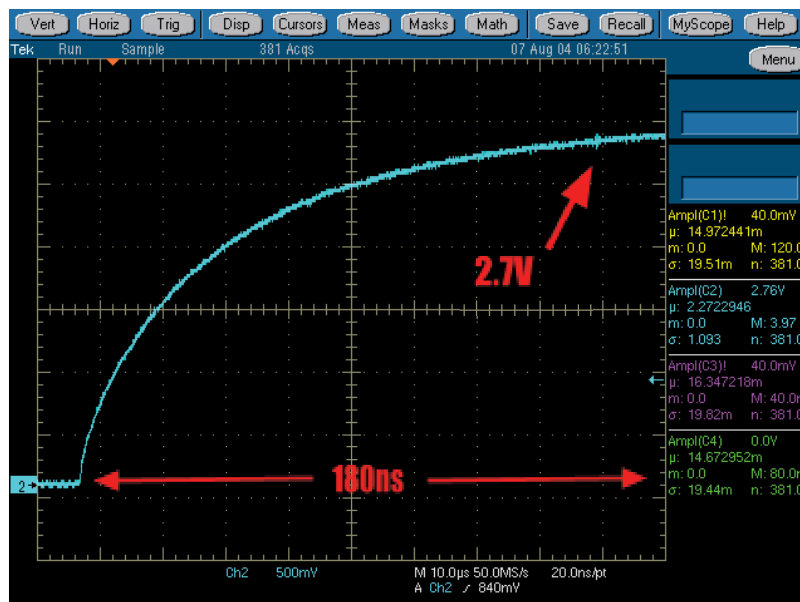
Figure 4.32: Connector 1, rising edge during a trigger switch.
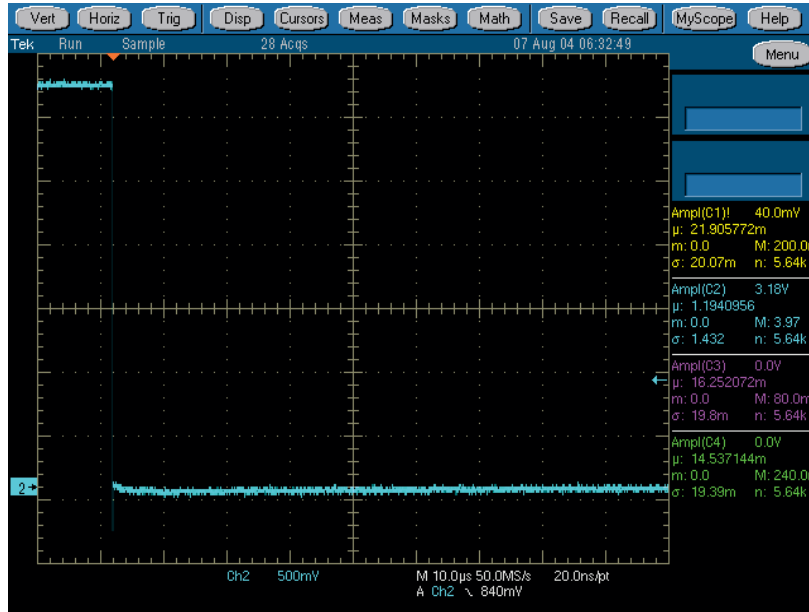
Figure 4.33: Button switch, falling edge.
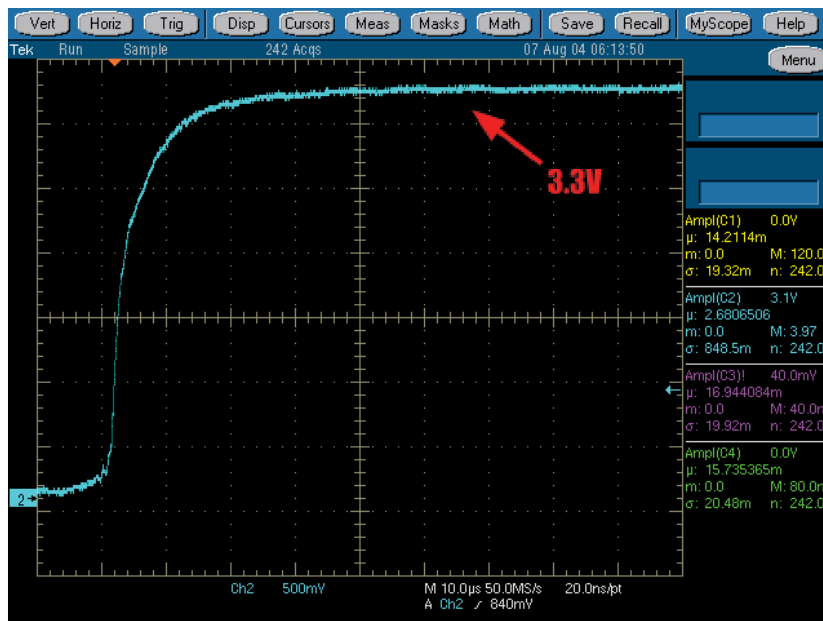
Figure 4.34: Button switch, rising edge.

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For this project only one of the connectors on the board will be in use, as well as the button. The connector will be linked to the trigger mechanism on the gun. This means when the trigger is pulled on the gun, the connector will be pulled to ground, and when the trigger is released, the connector will rise again to VDD. The button will be for reset and bluetooth connection. The connector and the button are assigned as general purpose inputs, and are triggered when pulled down to ground. Figures (4.31-4.32) illustrates when the connector for the gun trigger is activated and pulled down to ground. When released, the pull-up resistor will pull that node up to VDD again. The time it takes for the node to be pulled up will be the time limit for a shooting cycle, in this case it will be 180ns. From figures (4.31-4.34) we see that all the desired voltages are achieved.

4.4.4 GPIO measurement during triggering (GAIM 3.0)
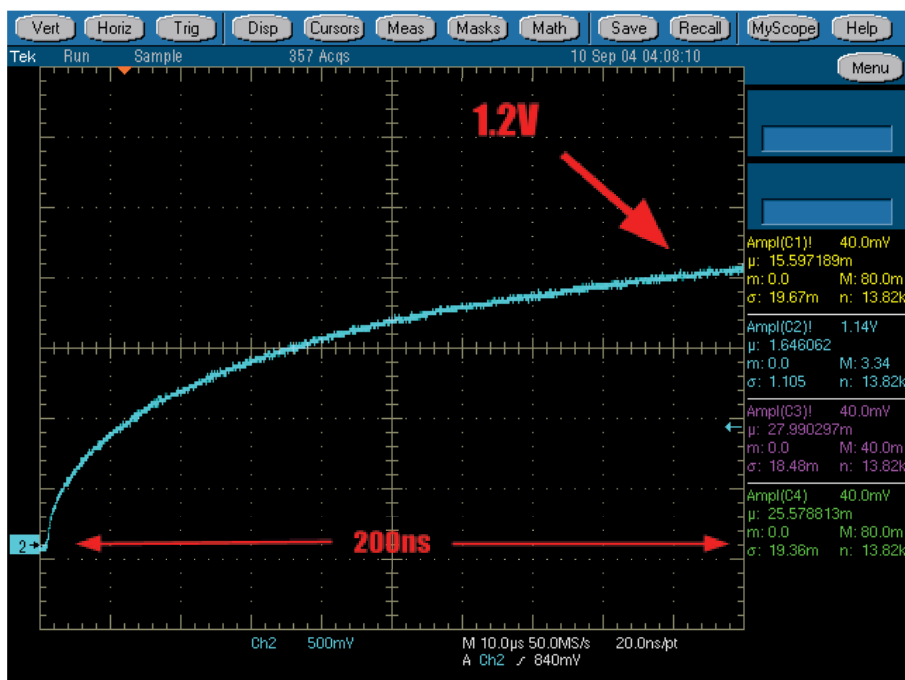
Figure 4.35: Connector 1, rising edge during a trigger switch on GAIM 3.0.

Both versions of the GAIM PCB have same valued pull-up resistors on the GPIO pins, however on the new design I chose to go down in size for the resistors to decrease the design complexity. The old design had a resistor package size of M1006 (1mm*0.6mm footprint), and the new design has a

package size of M0603 (0.6mm*0.3mm footprint). Comparing figures (4.32) and (4.35) we see that there is an improvement in time for the GPIO pin to reach VDD on new design. This improvement can depend on various things, which will be almost impossible to verify. One speculation is that there is less stray capacitances on the new design, since the footprints and packages of the pull-up resistors are much smaller, however that is very unlikely since stray capacitances are in the picofarads, which will have almost zero effects on signals that are this low in frequency.

Another speculation is that choosing smaller sized resistors somehow sped up the charging process of the GPIO pin, which is also unlikely since the same values on the pull-up resistors were used on both the old and new design.

The third speculation is that the slower charging process on the old design is linked to the ANNA RF module. Possibly some internal systems and processes linked to the GPIO pins that are controlling the speed of the pull-up.

However both the designs are fast enough for a trigger to be detected when using the gun, since the average reaction time for a person is in the hundreds of milliseconds, while the charging time of the GPIO pins are in the hundreds of nanoseconds for both the old and new design.

4.5 RF/Antenna measurements

The following sections display the results obtained during RF and antenna measurements.

4.5.1 Conducted power measurements for one channel

As mentioned in section 3.5, the PCB was flashed with a test program that emits at frequencies 2402MHz, 2440MHz, 2480MHz, with the conducted power of 0 dBm. In this section I will present what measurements on one frequency looks like. We will focus on the frequency 2402MHz. However in the next section we will look at the results when measuring all channels between 2402-2480MHz to see the power loss on the RF trace (without the antenna).
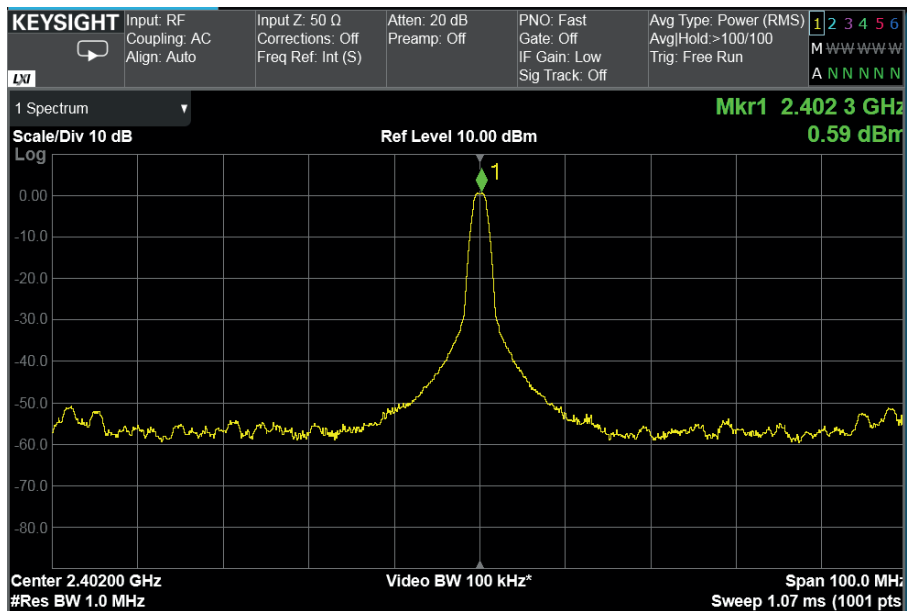
Figure 4.36: Signal on the RF trace in the frequency domain.
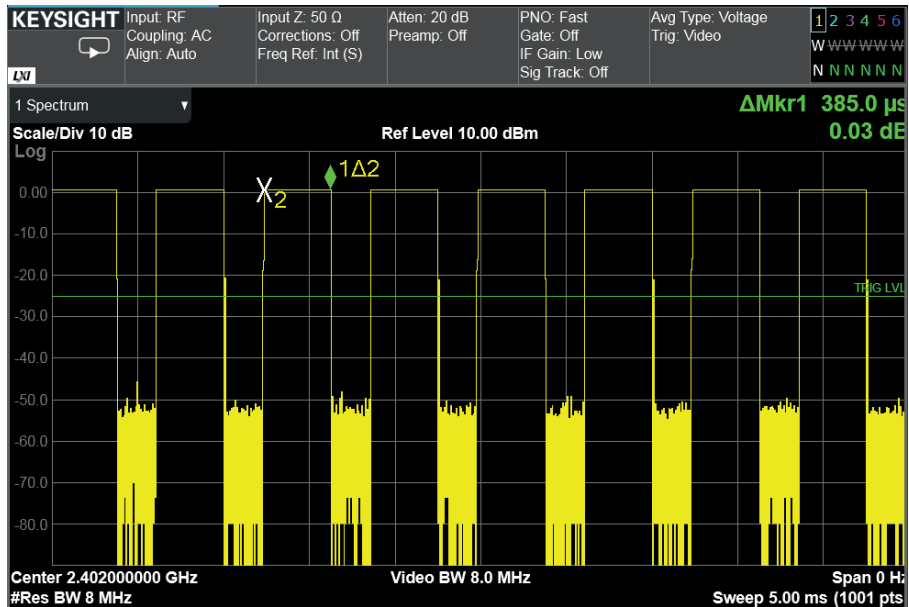
Figure 4.37: Signal on the RF trace in the time domain.

From figure (4.36) and (4.37) we see the signal measured on the RF trace of the new PCB. The signal itself is irrelevant, but we can see the conducted power (power into the antenna) to be around 0 dBm. This conducted power will be used when calculating the antenna efficiency, since the same program will be running when doing TRP measurements in the RF chamber.

4.5.2 Conducted power measurements for all channels

The same set-up for power measurements will be done here, but on all channels, using a different program with a conducted power of 4 dBm.
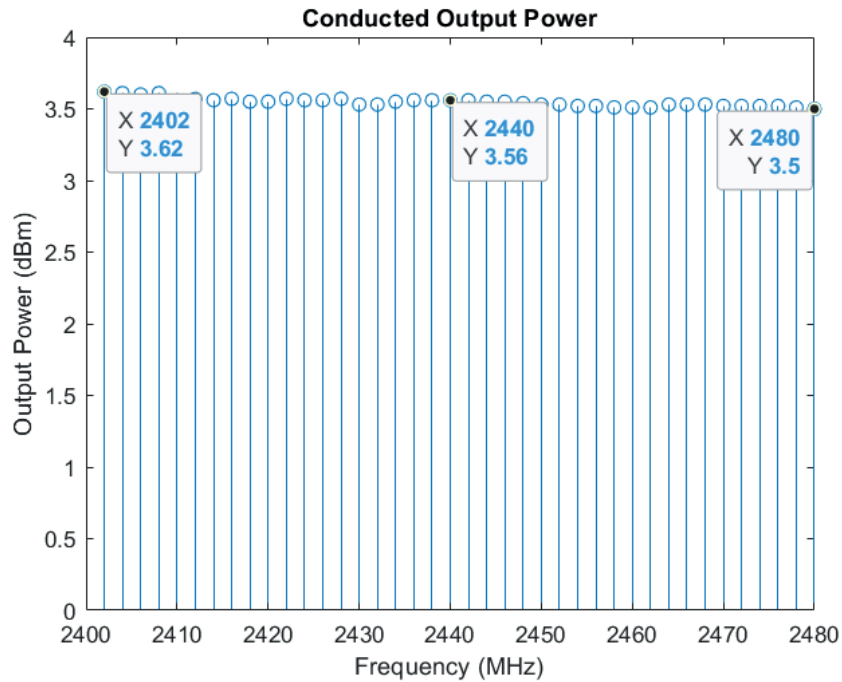
Figure 4.38: Output power on the RF trace, for all channels on the BLE band.

From figure (4.38) we can see the power loss of 0.38-0.5 dB throughout the entire BLE frequency spectrum, which is expected. The loss occurs in the chipset and RF trace. The output power in this case is just another word for the conducted power (power that goes into the antenna, also called input power). All conducted power measurements were only done on the new PCB (GAIM 4.0), since we have a visible RF trace on the PCB. However on the old design, the antenna is integrated in the RF module, making it impossible to measure conducted power.

4.5.3 Total Radiated Power (TRP) measurements & Antenna efficiency

The following tables contain the results of the total radiated power measurement and the efficiency of the antenna, on both the old and new PCB.

GAIM 4.0 PCB				
Freq (MHz)	Conducted (dBm)	TRP (dBm)	Efficiency (dB)	Efficiency (%)
2402	0	-3.7	-3.7	42.7%
2440	0	-4.9	-4.9	32.4%
2480	0	-7	-7	20.0%

Table 4.5: TRP measurements and antenna efficiency on the new PCB.

GAIM 4.0 PCB (Placed inside the trigger mech unit)				
Freq (MHz)	Conducted (dBm)	TRP (dBm)	Efficiency (dB)	Efficiency (%)
2402	0	-11.4	-11.4	7.2%
2440	0	-11.6	-11.6	6.9%
2480	0	-10.9	-10.9	8.1%

Table 4.6: TRP measurements and antenna efficiency on the new PCB placed inside the trigger unit.

Tables (4.5) and (4.6) display the results of the total radiated power measurements, done on the new PCB (GAIM 4.0). Table (4.5) are the measurements done on just the PCB, while table (4.6) are the measurements when the PCB is placed in the mechanical trigger unit from figure (1.1). The conducted power will be the same for all measurements (due to the program on the chip). As we see from the tables the efficiency of the antenna decreases when placed in the mechanical trigger unit. This is expected since

we are enclosing the antenna, therefore decreasing the radiated power. The material of the enclosure will absorb some of the electromagnetic radiation. However this efficiency is still very good considering the maximum distance for the intended application is around 1 meter.

GAIM 3.0 PCB (Placed inside the trigger mech unit)				
Freq (MHz)	Conducted (dBm)	TRP (dBm)	Efficiency (dB)	Efficiency (%)
2402	0	-11.3	-11.3	7.4%
2440	0	-10.9	-10.9	8.1%
2480	0	-9.5	-9.5	11.2%

Table 4.7: TRP measurements and antenna efficiency on the old PCB placed inside the trigger unit.

Table (4.6) are the total radiated power measurements on the old PCB enclosed in the mechanical trigger unit. The RF module is flashed with the same program as before, setting the conducted power to 0 dBm. Comparing tables (4.6) and (4.7), it is observed that the former design (GAIM 3.0) exhibited slightly superior antenna efficiency, which was expected for obvious reasons. These reasons will be discussed in section 5.5. However I succeeded with maintaining decent antenna efficiency with the new design (GAIM 4.0).

4.5.4 Sensitivity & Distance measurements

The measurements in section 3.5.3 were taken three times on the new PCB (GAIM 4.0), with different frequencies. An average of the results give us a conducted sensitivity of -94dBm. For the old PCB (GAIM 3.0), we see from the datasheet that the conducted sensitivity is -91dBm. This gives us a drastic improvement of sensitivity in the new design. Using equation (2.2.5) and (2.2.6) in section 2.2.4, we calculate the distance to be:

GAIM 4.0 PCB				
Conducted Sensitivity (dBm)	Average TRP (dBm)	Sensitivity (dBm)	Path Loss (dB)	Distance (m)
-94	-11.3	-82.7	71.4	11.35

Table 4.8: RF performance for GAIM 4.0 PCB.

GAIM 3.0 PCB				
Conducted Sensitivity (dBm)	Average TRP (dBm)	Sensitivity (dBm)	Path Loss (dB)	Distance (m)
-91	-10.6	-80.4	69.8	10.03

Table 4.9: RF performance for GAIM 3.0 PCB.

From table (4.8) and (4.9) we can see the conducted sensitivity for both the old and new PCB. However this value is before the antenna, to get the real sensitivity of the chip and module we need to subtract the radiated power. I took the average TRP for both designs, by averaging the TRP values from table (4.6) and (4.7). With the real sensitivity we can calculate the maximum distance before data-transfer degradation. As observed from table (4.8) and (4.9), we can see an improved distance of 1.32m with the new PCB configuration, using discrete components. However since the maximum distance for the application of the trigger unit will be at most about 1m, both designs are more than good enough to get a stable communication with the VR headset.

Conclusion

In this section, the results are discussed, along with potential improvements to consider.

5.1 PCB design

In figures (3.17), (4.1) and (4.2) we see the complexity of fitting the nRF chipset with the discrete components compared to the previous revision of GAIM using the ANNA module. Going from an RF module to discrete components meant an increase in approximately 20 components. The size constraint for fitting all these components on the board are shown in figure (4.2) highlighted with the red box. It is similar to solving a puzzle where all pieces need to fit perfectly while still achieving the attended application of the component and following the design rules. Sometimes the pieces will not fit, and a full reconstruction of the mechanical part (board outline) is the only viable solution. Fortunately for this project I managed to fit all the necessary components.

In section A.1 of the Appendix, from the schematic (in the group GPIO Switches) we see that ESD diodes were incorporated into the design on each switch, similar to the configuration of figure (2.3) from section 2.1.3. As mentioned in section 2.1.3 the diodes were placed as close as possible to all the external connectors and buttons. This was done for the shortest current path to ground during an ESD event. ESD testing was done using an ESD gun, shooting high voltage at the PCB. This was done a couple of times and the board survived, which means that the diodes were working. When choosing diodes it is important to consider the capacitance of the diode. We do not want to add unnecessary load capacitance to the system, especially when dealing with high-speed and HF signals. Fortunately the GPIOs on the GAIM PCB are only up to 10kHz, so the added capacitance will not affect the signals as much.

The second ESD protection design technique implemented can be seen in figure (3.16) and (3.17) of section 3.3. This is something I would consider to improve for future work, since the width of the exposed copper on the sides is only 0.3 mm, which is very small. The width of the exposed copper ground should at least be 0.5 mm, but unfortunately 0.5 mm was not possible on this design due to signal traces routed on the top and bottom layer were 0.5mm for the edge. Quantifying the results of this technique was not possible due to the small width of the exposed ground.

5.2 Cost aspect

In section 4.2.1 we start off by comparing the component cost for the different configurations. The previous configuration using the ANNA module, gives us a component cost of ~168 SEK per PCB. When using the new configuration with the nRF chip and discrete components the component cost decreases to ~126 SEK. Even though we incorporated twenty more components in the new configuration, the component cost has decreased by ~42 SEK per PCB. This is a 26% decrease. On a small production scale this reduction in cost might not be as notable compared with a large production scale. Especially when incorporating the certification cost.

Continuing to the next section 4.2.2, we include the certification cost of the PCB. As stated in section 1.1.2 of the introduction, when dealing with RF modules there is only one certification to tackle. However when dealing with discrete components there are two certifications. Depending on the production quantity one configuration is less expensive than the other. We see from tables (4.3), (4.4) and figures (4.3), (4.4), which configuration will be less expensive proportional to the quantity produced. The figures illustrate the interception point, which means the production quantity where the cost per PCB is exactly the same for both configurations. This point has been approximated to be about 2360 boards. This means when producing more than 2360 PCBs the nRF configuration is less expensive, however when producing less than 2360 boards the ANNA configuration is less expensive.

The overall market and audience for GAIM will decide what configuration will be most suitable from a cost perspective. If GAIM knows that their product will be sold to over 2360 custommers, then nRF configuration is the way to go, if not then ANNA configuration is more optimal.

5.3 PDN analysis

Starting with the transient simulation using the modeled RLC network for the GAIM PCB (figure 3.13), we see from figures (4.5), (4.6), (4.7), (4.8), (4.9), (4.10), (4.11), (4.12), and (4.13) the different responses by varying parameters such as capacitance values, ESR, and ESL. From figures (4.5), (4.6) and (4.7) we see there are more fluctuations on the voltage rail when decreasing the capacitance on the decoupling capacitors. When removing all the decoupling capacitors we see there are extreme voltage variations and noise in figure (4.13). We also observe from the figures that increasing the ESR, decreasing the ESL, and having multiple capacitors in parallel will give less voltage fluctuations. In theory, this means we should choose a decoupling capacitor with higher capacitance, higher ESR, lower ESL, and place multiple capacitors in parallel.

Secondly, looking at the impedance calculations for the modeled RLC network (figure 3.14 with decoupling capacitors, and 3.15 without decoupling capacitors), we see that these models are more simplified compared to figure (2.12) in the theory section. Comparing those figures, we observe that all ground RL components are neglected on the modeled PDN in figures (3.14) and (3.15). Using these figures I calculated the impedance for both, using equation (4.3.1) and (4.3.2), and in matlab I plotted the impedance with respect to frequency using different decoupling capacitor values, and multiple capacitors in parallel. This gave an interesting result in figure (4.14). When using no decoupling capacitors we get a higher cut-off frequency compared to using decoupling capacitors. This is not concurrent with the theory, because according to the theory we should get an increase in cut-off frequency when introducing decoupling capacitors. The reason it is not consistent with the theory might be because the modeled RLC network for the GAIM PCB is too simplified and the missing ground RL components on the PDN will reduce the cut-off frequency when not using any decoupling capacitors. However when observing the antiresonance and series resonance on figure (4.14), we recognize that the simulations are concurrent with the theory. When increasing the decoupling capacitance the peak should decrease according to equation (2.3.10) in the theory section. This is observed from the simulation in figure (4.14), where the antiresonance peak is decreasing when increasing capacitance.

Lastly, we will discuss the real AC impedance simulations done on the GAIM PCB. Starting with figure (4.15) illustrating the PDN impedance magnitude without any decoupling capacitors. From the figure we can see the cut-off frequency to be roughly about 3.5MHz. Since the nRF chip has a

clock frequency of 64MHz, we want the cut-off frequency to be well above that. Figures (4.15), (4.16), (4.17), (4.18), (4.19), and (4.20) illustrate the impedance measurements on the GAIM PCB using different decoupling capacitor values. From these results we can see that using higher capacitance values will give less parallel resonance peaks and give better cut-off frequencies. These results are consistent with the theory. Ideally using 4.7uF capacitors will give the best results on the PDN impedance as seen in figure (4.18). However using larger capacitance values will mean physically larger capacitors on the PCB. This is not possible since the component placement for all the discrete components is limited, including the decoupling capacitors. Therefore using 1uF as decoupling capacitors will be most optimal for this PCB.

Figure (4.21) displays the impedance measurement without any decoupling capacitors on the previous version of the PCB (GAIM 3.0). In comparison with figure (4.15), we see the DC impedance magnitude was improved and decreased by a factor of 2 with the new version of the PCB (GAIM 4.0). The improvement is due to larger power planes on the PDN on the new design, compared with the old version where only power tracks were used. Using equation 2.3.1 and 2.3.4 in section 2.3, we see that larger impedances on the PDN will cause larger voltage drops on the PDN. Having large voltage drops is detrimental for proper chip operations, due to a decrease in the supply voltage seen from the chip. Decreasing the impedance on the PDN by a factor of 2 will inherently decrease the linear *IR* voltage drop on the PDN with the same factor.

However, greater improvements on the impedance could be done by increasing the size of the power planes, even making a dedicated power layer, which means the entire layer will be filled with a copper power plane. Introducing dedicated power layers however will have a negative effect on both the design complexity and cost aspect. This is due to adding two new layers to the stack-up. What was four layers will now become six layers when introducing dedicated power layers. The trade-off for making dedicated power layers will therefore be increasing the PCB manufacturing cost.

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5.4 Functionality verification

From figure (4.22) and (4.23) we see the measurements taken on each node that is directly connected to the battery node during start up. The behaviors are normal, and it reaches the desired VBAT voltage of 3.3V.

Figures (4.24), (4.25), (4.26), (4.27), (4.28), (4.29), and (4.30) illustrate the measurements taken on the supply voltage nodes. Starting with (4.24) the measurements are taken on the VDD node from the LEDs. As we see the behavior is normal during operation, and desired voltage is reached. On (4.25) we measure the voltage on the big decoupling capacitor near the nRF chip, and the voltage reaches the desired supply voltage. We also see from the figure the behavior of the voltage, typical for charging a capacitor. Figure (4.26) shows the voltage behavior on the small decoupling capacitor near the nRF chip, the charging of that capacitor is much faster (since it is a much smaller capacitance compared with the big capacitor). Figures (4.27), (4.28), and (4.29) show the voltage behavior of the supply voltage on each connector measured after the pull-up resistors. As we see, all have normal behaviors and reach the desired voltage of 3.3V. On figure (4.30) however there are some glitches on the supply voltage on the big capacitor when switching on/off the switching power supply. These glitches are up to 1V, which is not good for the chip if there are big voltage spikes. This is caused by the high frequency components in the switching power supply, and can be solved by having filtering components on the board, such as filtering capacitors or ferrite beads. This PCB is not intended to have a supply voltage from a switching power supply, therefore the filtering components are not necessary, since the supply will come from a cell battery which does not contain the high frequency components.

Figures (4.31), (4.32), (4.33), and (4.34) display the voltage behaviors when triggering the connectors on the board (top connector and button). Figure (4.31) shows when triggering connector 1, by pulling it down to ground. Releasing the connector will cause the pull-up resistor to conduct and charge the supply capacitor, we see that in figure (4.32). It takes 180ns to recharge the node, this could be a problem since this connector is used for the trigger on the gun. This limits each shot cycle to be every 180ns, which is very fast considering the reaction time of a normal person is 250ms [21]. The same behaviors can be observed in figures (4.33) and (4.34). However this is the reset button, which means the timing is not a problem since the reset sequence takes a couple of seconds to complete.

Figure (4.35) illustrates when connector 1 is triggered on the old design (GAIM 3.0). As mentioned at the end of section 4.4 in the results,

comparing the time delay between the new design and old design we have a significant improvement. However both are fast enough considering the intended application and the reaction time of an average person.

5.5 RF/Antenna measurements

Starting with section 4.5.1 and 4.5.2, where I conducted power measurements on the RF trace. Both the RF module on the old PCB and nRF chip on the new PCB were flashed with software to have a conducted power of 0 dBm. Conducted power measurements are impossible to do on the module, since the antenna is integrated. For simplicity I will assume the conducted measurements done on the new PCB will be the same for the old PCB, since both PCBs are flashed with the same program. Figures (4.36) and (4.37) illustrate the RF signal measured on the RF trace, for the frequency 2402MHz. The signal itself is irrelevant, however as seen in the figures the conducted power is 0 dBm. In section 4.5.2 we want to measure the conducted power on the entire frequency band for BLE. I flashed the chip with a different software, setting the conducted power to 4dBm and using the UART connection on the PCB I can scan through the entire band and measure the conducted power for each channel. As seen in figure (4.38), the conducted power remains virtually the same with miniscule ohmic power loss of 0.38-0.5 dBm.

In section 4.5.3 we observe the results from the total radiated power measurements done in the RF chamber. In this section we are using the software with a conducting power of 0dBm. Table (4.5) presents TRP measurements done on just the PCB (GAIM 4.0), and table (4.6) are the same measurements done on the PCB enclosed in the trigger mechanical unit from figure (1.1). Comparing the results we can see that antenna efficiency degrades by a large amount. This is due to the enclosure absorbing a significant amount of electromagnetic radiation. This could be solved by using different materials for the enclosure, however the efficiency in table (4.6) is more than good enough to give a stable connection. Doing the same measurements on the old PCB (GAIM 3.0) with the RF module we see from table (4.7) that the antenna efficiency is slightly superior compared to the new PCB. This is due to RF modules having a fully optimized RF system, and more calibrated antennas integrated in the modules [27].

However, antenna efficiency is not the only aspect that dominates RF performance. In section 4.5.4 we measure the sensitivity of the RF module and nRF chip. With sensitivity I can then get the maximum distance before there is data-transfer degradation. By examining the data presented in table

(4.8) and (4.9), the conducted sensitivity of both the old and new PCB configurations becomes apparent. It is important to note that this sensitivity value is recorded prior to the antenna, necessitating the deduction of radiated power for an accurate assessment of the chip and module sensitivity. The average total radiated power (TRP) was calculated for each design by averaging the TRP values documented in table (4.6) and (4.7). Utilizing the actual sensitivity values, the maximum distance before data-transfer degradation can be computed. The results, as indicated in table (4.8) and (4.9), reveal an enhanced distance of 1.32m with the implementation of the new PCB configuration, integrating discrete components. However, given that the application range of the trigger unit is anticipated to be a maximum of approximately 1m, it is evident that both designs surpass the requisite criteria for maintaining stable communication with the VR headset.

5. Future Work

This project was successful in achieving the desired goals of designing a functional electronics trigger device for the dummy guns used in the shooting simulations. There is definitely room for improvement when it comes to user experience and making the simulations feel even more realistic.

One improvement for better user experience is developing a recoil mechanism for the dummy guns when shooting. This will simulate a more realistic feeling when pulling the trigger, which will be very beneficial for especially law-enforcement and military training. One possible way to simulate recoil in the dummy guns is to incorporate carbon dioxide cartridges. Designing a mechanism that will rapidly release gas from the cartridge rotated in the opposite direction, when the trigger is pulled. That could possibly be a master's thesis project from a mechanical engineering perspective.

6. Appendix A: Extended material

In this section there are more visible and detailed figures that were difficult to understand in the report.

A.1 Schematic

A.2 Assembly Drawing

Top side

View from Top side (Scale 7:1)

X1

FIDUCIAL2

RENATA

BT1

+

R8
R6

Z5

FIDUCIAL1

S1

PCB Edge

sigma
Connectivity

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| Scale: | Units: | Sheet size: |
| | Millimeters | A3 |

Prepared (Also Subject Responsible if Other):
Marko Pojovic
Doc Responsible / Approved:
Marko Pojovic

Date:
2023-11-5

Rev:
4.0

Product Name:
GAIM

Document No/Name:
Placement Drawing

SHEET 2 OF 3

Bottom side

View from Bottom side (Scale 7:1)

ANT1

C20 L4
L5

FIDUCIAL3

D1 D3 D2

C10 C4

C19

C6 C7

R1 R7 R3

X5

C17 L3
C16
C14 C18

U1

C8

C15
C12
C13

C3

L2

C9 C2 C1

X3

L1

C11

R10 R11

Z3

PC1

R4 Z2

C5

R13
R12

Z4

X6

X4

Z1

R2 R5

PC2

FIDUCIAL4

X2

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A.3 Bill of Materials (BOM)

Designator	Quantity	Description	Value	Manufacturer	Manufacturer Part No	Rating
ANT1	1	Antenna RF ANT 2.4GHZ CHIP SOLDER SMD M3216	2.4GHz	Johanson Technology	2450AT18B100E	
BT1	1	BATTERY HOLDER Renata Battery Holder		Renata	SMTU2032-lf	
C1, C2, C8, C12, C13, C14	6	CAP CER 12pF 25V COG, NP0 1% M0603	12pF	Murata	GJM0335C1E120FB01D	25V
C3	1	CAP CER 1uF 10% 16V X7R M1608	1uF	Murata	GCM188R71C105KA64D	16V
C9, C15, C19	3	CAP CER 100nF 16V X7R 10% M0603	100nF	Murata	GRM033271C104KE14D	
C11	1	CAP CER 4.7uF 10V X5R 10% M1005	4.7uF	Samsung Electro-Mech	CL05A475KP5NRNC	
C16	1	CAP CER 100pF 25V COG 5% M0603	100pF	Murata	GRM0335C1E101JA01D	25V
C18	1	CAP CER 0.8pF ±0.05pF 25V COG, NP0, M0603	0.8pF	Murata	GJM0335C1ER80WB01D	25V
C20	1	1 pF ±0.1pF 50V Ceramic Capacitor COG, NP0 M0603	1pF	Murata	GJM0335C1H1R0BB01D	50V
D1	1	LED RED Colour M1005	RED	Kingbright	APHHS1005LSECK/J3-PF	2mA, 1.85V
D2	1	LED Yellow Colour M1005	Yellow	Kingbright	APHHS1005LSYCK/J3-PF	2mA, 1.85V
D3	1	LED Green Colour M1005	Green	Kingbright	APHHS1005LCGCK	2mA, 1.9V
L1	1	IND CER 15nH 560mA ±10% M1005 172 mOHM	15nH	Delta Electronics/Comp	0402HS-150EKTS	560mA
L2	1	IND CER 10uH 300mA ±20% M1608 1.37 OHM	10µH	Murata	LQM18DZ100M70L	300mA
L3, L4	2	IND CER 3.9nH High Frequency Inductor, 500 mA, .17	3.9nH	Murata	LQP03HQ3N9C02D	500mA
L5	1	IND CER 2.2nH High Frequency Inductor, 600 mA, .12	2.2nH	Murata	LQP03HQ2N2C02D	600mA
PC1, PC2	2	CONN PC PIN GOLD	7937	Mill-Max Manufacturin	ED90501-ND	
R1, R3, R7	3	RES 62R 1% 1/16W M1005	62R	Yageo	311-62.0LRCT-ND	1/16W
R2, R6, R10, R12	4	RES 100K 1% 1/20W M0603	100K	Yageo	RC0201FR-07100KL	1/20W
R4	1	RES 0R 1/10W M1005	0R	Panasonic	ERJ-2GE0R00X	1/10W
R5, R8, R11, R13	4	RES 10K 1% 1/20W M0603	10K	Stackpole	RMCF0201FT10K0	1/20W
S1	1	SWITCH TACTILE Right Angle 160gf	160gf	CTS Electrocomponents	223GMSAAR	
U1	1	IC RF TXRX+MCU BLUETOOTH 48-VFQFN		Nordic	NRF52832-QFAA-R	
X1, X2	2	J-LINK_6-Pin_Needle Adapter without holes	J-LINK_6-Pin_N			
X3	1	XTAL 32.768kHz, 9pF, ±20ppm	32.768kHz	Micro Crystal AG	CM7V-T1A-32.768KHZ-9PF-20PPM-TA-QC	
X4, X6	2	CON 4 Positions Header 0.100" (1.5mm)		JST Sales America Inc.	S2B-ZR-SM4A-TF(LF)(SN)	1.5mm
X5	1	32MHz ±25ppm Crystal 8pF 60 Ohms 4-SMD, No Lea	32MHz	KYOCERA AVX	CX2016DB32000D0WZRC1	
Z1, Z3, Z4, Z5	4	Diode TVS 6.5V 16A M1006	6.5V Clamp 16A	Texas Instruments	ESD351DPYR	

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