# Popular Science Summary

Nowadays, people are quite getting used to hear about "4G" or "5G". It actually means 4th or 5th generation of wireless communication. The revolution from 4th to 5th is basically high carrier frequency and larger bandwidth. People may wonder what carrier frequency and bandwidth mean. If we take logistics as an example, the information we transfer is the good. Higher carrier frequency is equal to faster speed of the train, it will reduce the time used. Larger bandwidth is equal to having more train carriages, it can transfer more information each time. Then the analog to digital converter(ADC) we discussed in the thesis is like loading and unloading along this good supply chain. It plays a role of interaction between transferring and destination.

In reality, the function of ADC is to convert the analog signal into digital code. It needs to be fast to keep up with speed of transferring as we mimicked above. Another consideration is the linearity, which requires the converter output to be as linear to the input as possible. We find that this linearity performance can be impacted by some "fixed" errors. The mentioned "fixed" error is to distinguish with "random" one. How to handle these errors is one of the key theory parts in this thesis. Finally, we come up with the goal to design a high speed and high linear ADC.

How to boost the speed is the first problem. Intuitively, we believe that simple circuit form can have rather fast speed. The problem accompanied with high speed benefit is the inaccuracy. This inaccuracy we encountered here is mainly for gain factors inside the system, which is one major "fixed" error as we mentioned above. To deal with this error it comes with the idea of "correction". The basic strategy is that we try to "estimate" this error, and use the estimation value to recover the correct data. Here how to estimate is a mature algorithm referred as least square error.

Another finding is the hidden bandwidth limitation inside the ADC analog circuit when the system runs at quite high speed. This limitation acts as a low pass filtering and degrades the linearity performance. Intuitively, this low pass filtering in the analog side can be compensated by having another high pass digital filter in the digital part. The coefficients of digital filter can be estimated the same way as gain error mentioned above.