Comparator Design for High Speed ADC

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MASTER´S THESIS
DEPARTMENT OF ELECTRICAL AND INFORMATION TECHNOLOGY
FACULTY OF ENGINEERING | LTH | LUND UNIVERSITY

Comparator Design for High Speed ADC

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June 14, 2024

Printed in Sweden
Tryckeriet i E-huset, Lund

Abstract

High-speed Analog-to-Digital Converters (ADCs) play an important role in modern electronic systems, especially those systems that require high data rates and low power consumption. These converters are essential components in various applications, including telecommunications, medical imaging, radar systems, and wireless communication.

This thesis explores four different dynamic comparators to enhance the speed and efficiency for a 10-bit SAR-Pipeline ADC which is applied as 6 + 5 bits with one redundant bit. It encounters critical challenges such as optimizing speed, minimizing input referred noise, and reducing power consumption. By using a 22nm Fully-Depleted Silicon-On-Insulator (FDSOI) technology, this thesis involves detailed pre-layout and post-layout simulations to ensure the robustness and reliability of the comparator designs.

In pre-layout simulations, the triple-tail comparator with a feedforward path shows the fastest decision time of 60pS, compared to 100pS for the strong-arm latch and 80pS for the double-tail comparator. All the comparators in this thesis could meet the requirements of input referred noise and kickback noise, both smaller than half of LSB (Least Significant Bit). The post-layout results show that, while it introduces some parasitics like capacitances and resistances that deteriorate speed and kickback noise, it has a minimal impact on noise performance and power consumption. The exploration for comparators provides valuable insights into the design of high-speed ADCs. Future research directions include further reducing noise and power consumption and integrating these comparators into more complex systems for real-world applications.

Acknowledgments

I wish to express my profound gratitude to my industrial supervisors, Sunny Sharma and Hamidreza Ameri, for their exceptional guidance, expertise, and providing me with the invaluable opportunity to undertake this thesis under their mentorship.

I also want to express my sincere thanks to Acconeer in Malmö for their approvement of the chosen thesis topic and for generously providing the necessary tools for the successful execution of this project.

Furthermore, I am deeply grateful to all the esteemed professors at the Faculty of Engineering (LTH), Department of Electrical and Information Technology, at Lund University, whose dedication to teaching and mentorship has equipped me with the requisite knowledge and skills to conduct this thesis effectively.

Finally, I also extend my sincerest appreciation to my family, partner, and friends for their support, encouragement, and companionship all of the time.

Popular Science Summary

There are continuous analog signals and discrete digital signals in our life. For example, physical quantities in nature such as sound, temperature, and voltage are usually analog signals. These signals are continuously changing and have no discrete points in time. Digital signals are discrete signals whose amplitude can only take on specific discrete values. The most common digital signals are binary signals that can only take on the values 0 and 1. For example, the information processed within a computer is a digital signal, and all data is stored and processed in binary form.

An analog-to-digital converter (ADC) is a device that converts an analog signal to a digital signal. ADCs are used in a wide variety of applications, including but not limited to:

Audio and video equipment: Analog signals captured by microphones, video cameras, and other devices are converted to digital signals by ADCs for digital audio and video processing and storage.

Radar: Radar systems receive analog signals from the target through the antenna, and the ADC is responsible for converting these analog signals into digital form. This digitization allows the signal to be processed by digital systems, such as computers, digital signal processors, etc.

And the role of the comparator is to determine whether something is big or small. In an ADC, the job of the comparator is to compare the input analog signal with a reference voltage. If the input signal is larger than the reference voltage, the comparator outputs a high level, and if the input signal is smaller than the reference voltage, the comparator outputs a low level. This output is what is used to help the ADC determine the size of the input signal and then convert it to digital form.

Comparators have many key properties that need to be investigated and continually improved, such as speed and noise. Speed refers to how fast the comparator can complete a comparison operation. In some applications, especially in high-speed radar or communication systems, signals change very quickly, so the comparator needs to be able to react at a very high speed or it will miss an important part of the signal. So the speed performance of the comparator is studied to ensure that it can perform the comparison operation in a very short time. Noise refers to random fluctuations in the output of the comparator that introduce uncertainty and affect the accuracy of the ADC. For instance, if the noise in the

comparator output is too large, it will make the input signal not stable enough, leading to errors in the conversion results. Therefore, the study of the noise performance of the comparator is to ensure that its output is as accurate as possible and is not disturbed by noise.

In this thesis, we investigated several different structures of comparators to improve their performance for use in high-speed ADCs. During the investigation, we encountered some challenges such as trade-off between speed and noise, difficulty in establishing the correct test-bench circuit. Eventually, we successfully designed four different comparators that meet the requirements of the system ADC and compared their performance in a variety of ways.

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List of Acronyms

ADC Analog-to-Digital Converter

CDAC Capacitor-Digital-to-Analogue Converter

CDF Cumulative Distribution Function

DAC Digital-to-Analog Converter

DT Double-tail Structure Comparator

IRN Input Referred Noise

MSB Most Significant Bit

LSB Least Significant Bit

SA Strong-Arm Latch

SAR Successive-Approximation-Register

TT1 Triple-tail structure Comparator

TT2 Triple-tail structure Comparator With a Feedforward Path

Vth Threshold Voltage

Chapter 1

Introduction

1.1 Motivation

Nowadays, in various technological fields such as telecommunications, digital signal processing and consumer electronics have significantly increased the demand for high-speed Analog-to-Digital Converters (ADCs). It is a crucial component which is responsible for converting continuous analog signals into discrete digital signals that can be processed by digital systems. The performance and efficiency of these ADCs are significant in determining the overall capabilities of modern electronic devices.

High-speed ADCs are essential in applications where fast and accurate signal conversion is critical. For instance, in radar systems, the speed of signal processing directly affects the ability of this system to detect and respond to fast-moving objects.

Within high-speed ADCs, comparators are one of the most critical components. The primary function of a comparator is to compare the input signal with a reference level and decide whether the input is higher or lower than this reference. This decision-making process must be executed with high speed and gigh accuracy. In high-resolution ADCs without redundancy and error correction capabilities, even some tiny inaccuracies in the comparator can lead to significant errors. In conclusion, it is quite necessary to dive into and explore various comparators to find out the most suitable and efficient one for specific application.

The primary challenges of designing comparators contain improving speed and accuracy, reducing power consumption, noise reduction and mitigating offset. By improving comparator design, this work aims to contribute to the development of faster, more accurate, and more energy-efficient ADCs. The outcomes of this thesis have the potential to enhance the performance of various electronic systems, leading to more advanced and reliable applications in telecommunications, consumer electronics and so on.

In summary, this thesis is driven by the critical role that high-speed ADCs play in modern technology and the challenges associated with comparator design.

1.2 Background Knowledge

1.2.1 ADC theory

ADC(Analog-to-Digital Converter) is a type of circuit that convert analog signal to digital signal. In this thesis, the comparator will be implemented for SAR ADC.

SAR ADCs(Successive-approximation-register analog-to-digital converters) are usually applied for high-speed and low-power application. Resolution for SAR ADCs most commonly ranges from 8 to 16 bits. They employ a binary search method across all potential quantization levels until ultimately determining a digital output for each conversion [1]. The conceptual block diagram for single ended analog input signal is shown in Figure 1.1.

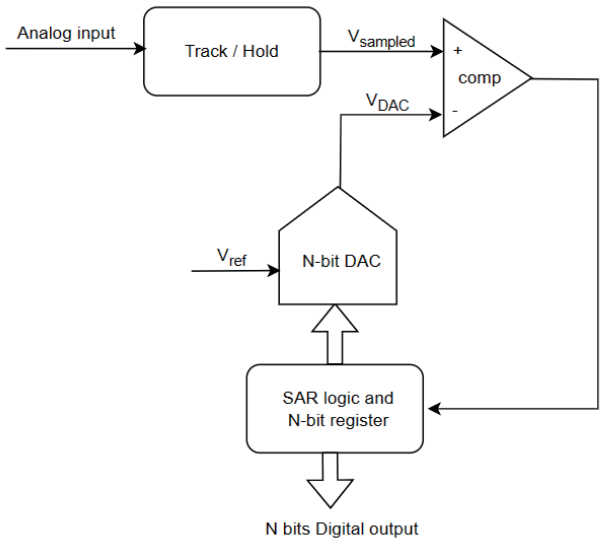

Figure 1.1: SAR ADC block diagram.

Here is a detailed explanation of the theory behind SAR ADC:

The analog input signal is sampled and held constant by a Sample-and-Hold (S/H) circuit. This step ensures that the input voltage keeps stable during the conversion process.

The ADC starts the conversion process by resetting the Successive Approximation Register (SAR) and initializing the Most Significant Bit (MSB) of the register to 1, while all other bits are set to 0.

The digital code in the SAR is converted to an analog voltage by a Digital-to-Analog Converter (DAC). Initially, only the MSB is set, so the DAC output is half of the reference voltage.

The output of the DAC is compared with the input voltage through a comparator. If the DAC output is less than the input voltage, the MSB remains set; otherwise, it is cleared.

The SAR proceeds to the next bit which is set to 1, and the new digital code

is again converted by the DAC to an analog voltage. This new DAC output is compared with the input voltage. The process repeats for each bit from the MSB to the Least Significant Bit (LSB), setting or clearing each bit based on the output of the comparator.

After all bits have been tested and set appropriately, the SAR holds the final digital code which is the digital representation of the input analog voltage.

As illustrated in Figure 1.2, higher bits give more accurate results. In other word, the final output will be closer to the Vin with more bits.

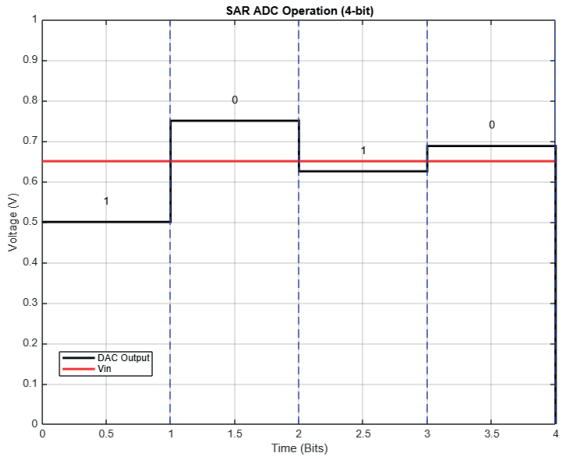

Figure 1.2: 4-bit SAR ADC operation of binary search

1.2.2 Comparator theory

Comparator is a device that compares two voltages or currents and produce a digital signal for the outputs indicating which one is larger. There are two main types of comparators, static comparator and dynamic comparator. For higher linearity system, static comparator is suitable. While the dynamic one is usually implemented for those high-speed and low-power system which coincidently match the requirements of our system specification. Therefore, this thesis will only explore the dynamic comparators.

Figure 1.3 shows a simple symbol of comparator. After the comparator is triggered by clock signal, it will start comparing the difference between V+ and V-. If V+ is larger than V-, they output a logic '1', otherwise they output a logic '0'. We also call comparator as a 1-bit ADC.

1.3 System Specification

To achieve a higher sampling rate, the SAR ADC will be splited into two stages and connects them with an amplifier. In this case, a 10-bit ADC is applied as 6 + 5 bits with one redundant bit. The first 6 bits are delivered to the first stage

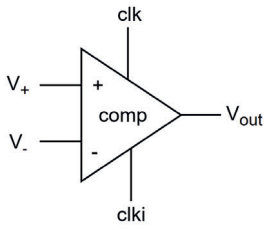

Figure 1.3: symbol of comparator

CDAC for generating the residue bits. The redundant bit is to absorb some errors from CDAC and other noise sources that may flip the bit cycle output incorrectly. The maximum total capacitance of CDAC that has 2fF unit capacitance is 2 + 2 + 4 + 8 + ... + 64 = 128fF. And the clock frequency for comparator would be 300M * 6 = 1.8GHz. An example of redundancy and error correcting ADC is available in reference [2].

Table 1.1: System specification.

Parameters	Requirements
Sampling Rate	300MSps
Resolution	10bits
Reference Voltage	900mV
LSB	$\frac{0.9}{2^{10}} = 878.9$uV
Input-referred Noise	$< 1/2$LSB
Kickback Noise	$< 1/2$LSB

1.4 Technology

This thesis is based on the 22nm FDSOI technology with flip-well and body biasing architecture. The filp-well for NMOS and PMOS modifies the transistor Vth by lightly p-dope or n-dope channel implant respectively. There are no more parasitic diode between source/drain and substrate. It can also be run at much higher voltage. Body bias is more effective as the channel is fully depleted compared to bulk technologies where the channel is heavily doped. P-well could connect to 0V to -2V and N-well could connect to 0V to 2V. Therefore, transistors could be switched on much faster than conventional well structure.

Chapter 2
Architectures of Comparator

This chapter will elaborate how four different architechtures of comparators work that we investigated in this thesis.

2.1 Strong-Arm Latch

The Strong-Arm Latch [10] is a simple and robust latch with high sensitivity that was proposed by Behzad Razavi. The schematic is depicted in Figure 2.1.

During the reset phase, the comparator clock is logic zero. M5, M6, M9, M10 turn on so that two output nodes (OUTP and OUTN) are pulled up to logic high.

During the regeneration phase, the comparator clock is logic high which turns on the tail NMOS transistor. Then the output nodes could start discharging to the ground. Their discharging rates are determined by the differential input voltage and the latch will gradually enlarge the voltage difference. Finally, the decision can be made.

2.2 Improved Double-Tail Comparator

To achieve a higher speed, double-tail comparator was proposed. In this thesis, we will explore one improved double-tail structure as shown in Figure 2.2 [11].

During the reset phase, the comparator clock is logic zero. M9, M10 turn on so that fp and fn are reset to VDD. Then, S5 and S6 can be switched on to pull down the output nodes to the ground.

During the regeneration phase, the comparator clock is logic high. M1 and M2 are on. In the first stage, fp and fn start discharging. As soon as one of them achieve to a voltage that could switch on one of M7 and M8, the other node will be pulled up immediately. This is how the first stage get a higher gain. However, this cross-coupled structure will cause a worse power consumption since there is a current path from VDD to the ground through input transistor and tail transistor. Therefore, M3 and M4 were introduced to overcome this issue. But this will bring more kickback to the input. In the second stage, the latch could continue enlarging the voltage difference of the first stage output and make a final decision.

C1 can be applied to filter some noise from the tail current source.

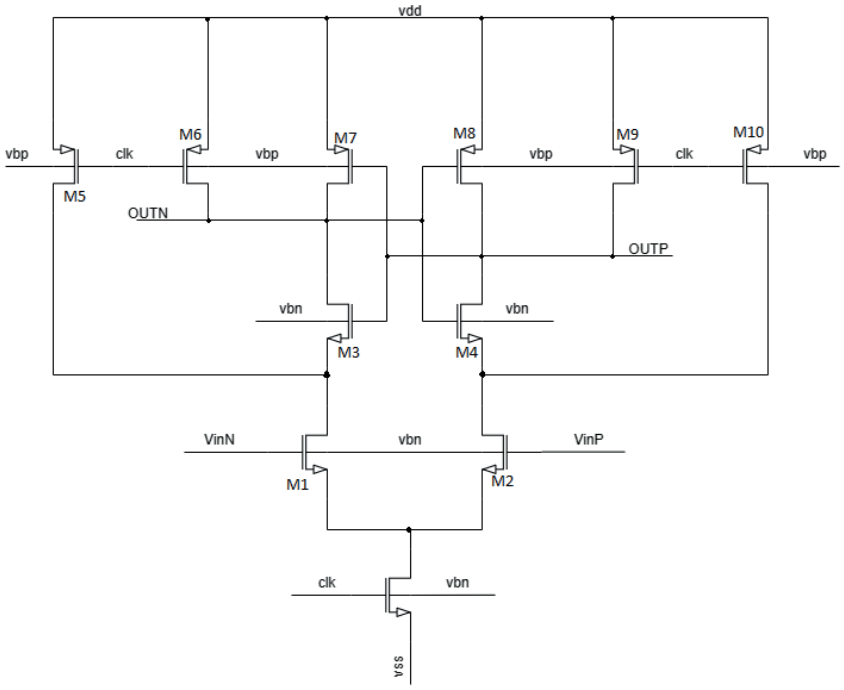

Figure 2.1: Schematic of Strong-Arm Latch.

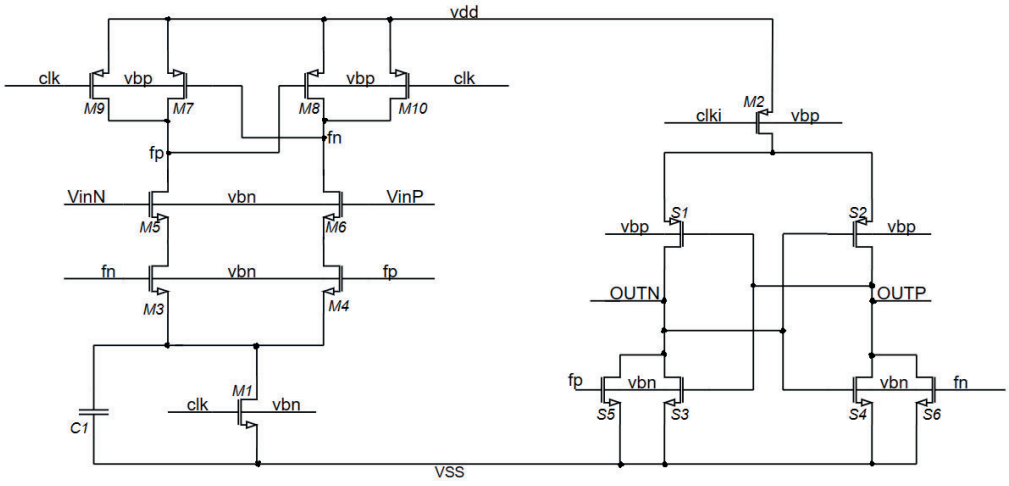

Figure 2.2: Schematic of improved double-tail comparator.

2.3 Triple-Tail Comparator

Since the improved double-tail comparator shows an insurmountable tradeoff between kickback noise and power consumption, a triple-tail comparator were proposed as shown in Figure 2.3 [12].

The multi-stage architechture allows us to do the optimization independently on each stage. The first stage can be designed for high gain, low noise, low offset. The second stage can suppress the output noise and provide some extra gain. The third latch stage is optimized to achieve the shortest possible regeneration time according to its load.

During the reset phase, clk is logic low so M5 and M6 are on. Then xn and xp nodes can be pulled up to VDD so that M7 and M8 are on to pulled down yn and yp to VSS. Then S3 and S6 in the third stage will be switched on to reset two output nodes to VDD. For a faster reset time, we introduced S1 and S2 which represent our original contributions compared to the reference paper.

During the regenaration phase, clk is logic high so T1, T2 and T3 are on to make the comparator start comparison. The differential input voltage will be enlarged until it could activate the third stage latch to make a decision.

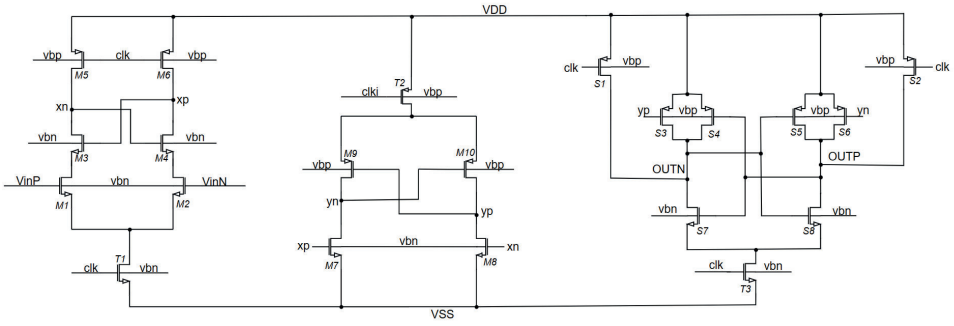

Figure 2.3: Schematic of triple-tail comparator.

2.4 Triple-Tail Comparator with a Feedforward Path

This structure works similarly with the triple-tail comparator in 3.3, except for a feedforward path which connects the first stage and the third stage directly [13].

As illustrated in Figure 2.4, the transistors that are enclosed by the dash lines could input the differential signals after the first amplification without the amplification of the second stage. In this way, when the differential voltage is large enough to activate the third latch making decision, the comparator could save some decision time due to discarding the second stage.

The delay of this structure can be quantified as:

$$\tau_1 \approx \frac{C_X}{g_{m3,4}} \tag{2.1}$$

$$\tau_2 \approx \frac{C_Y}{g_{m9,10}} \tag{2.2}$$

$$\tau_3 \approx \frac{C_{out}}{g_{s7,8}} \tag{2.3}$$

$$\tau_{\text{comp}} \approx \tau_1 + \tau_{\text{FF}} \tag{2.4}$$

$$\tau_{\text{FF}} \approx \begin{cases} \tau_2(1+\frac{g_{m7,8}}{g_{m9,10}}) + \tau_3(1+\frac{g_{s3,6}}{g_{s7,8}}) & \text{small Vin} \\ \tau_3(1+\frac{g_{s9,10}}{g_{s7,8}}) & \text{large Vin} \end{cases} \tag{2.5}$$

where g_m are the transconductances of corresponding transistor. τ_1, τ_2 and τ_3 are the time constants of stage-1, stage-2 and latch stage, respectively. C_x, C_y, and C_{out} represent the output node capacitance of each stage.

Hence, in both the direct and feedforward paths, minimizing stacking allows to overcome just a single transistor threshold, enabling a small delay.

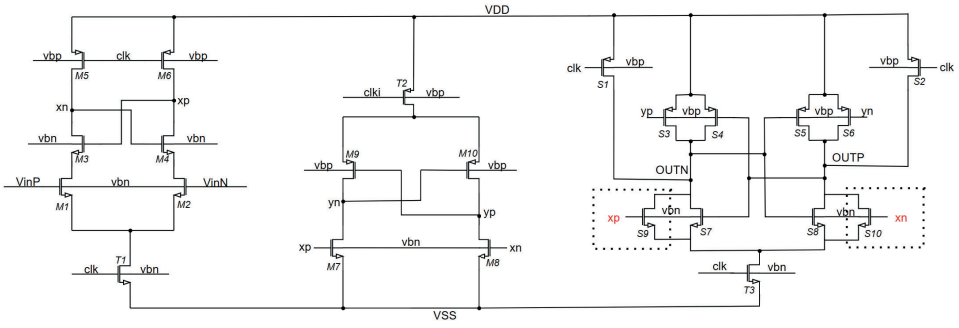

Figure 2.4: Schematic of triple-tail comparator with a feedforward path.

Chapter 3
Design Considerations

3.1 Decision Time and Reset Time

Speed is one of the most essential parameters of comparators because it would define how fast the ADC system could work. We determine the speed of comparators by finding out the decision time and reset time. For instance, the decision time of Strong-Arm Latch is measured from the 50% of the rising/falling edge of sampling clock to the point where the voltage difference of two outputs achieve to 90% of the reference voltage, as shown in Figure 3.1. The reset time is measured similarly, as shown in Figure 3.2. The measurement of reset time is taken close to the reference voltage that is comparator positive supply voltage so that the comparator does not have memory of the previous sample.

The design objective is to make the comparator finish making decision and resetting within one clock cycle. In conclusion, we could have a higher sampling rate if we consume less decision time and reset time [3].

3.2 Input-Referred Noise

For an ADC, IRN(input-referred noise) is the noise that is generated by the transistor itself. It is generally more meaningful to measure it rather than other type of noise because it relates directly to the unaltered signal. Input-referred noise is measured by dividing the measured output noise by the gain of the pre-amplifier. Therefore, it is more effective to analyze noisy circuits in this way [4].

In this thesis, PSS + Pnoise simulation is applied to measure the IRN [6]. The noise can be measured at the single point defined by the threshold value. The threshold value is referring to the results of the transient noise simulation. Then the total output noise can be presented.

$$\text{Total Integrated Noise} = \sqrt{\int_1^{f_{\text{nyquist}}} S_V(f)\, df} \tag{3.1}$$

$S_V(f)$ is the noise voltage spectral density, typically in units of V^2/Hz.

The gain can be calculated from the design variables. The following equation shows how to get the final input referred noise.

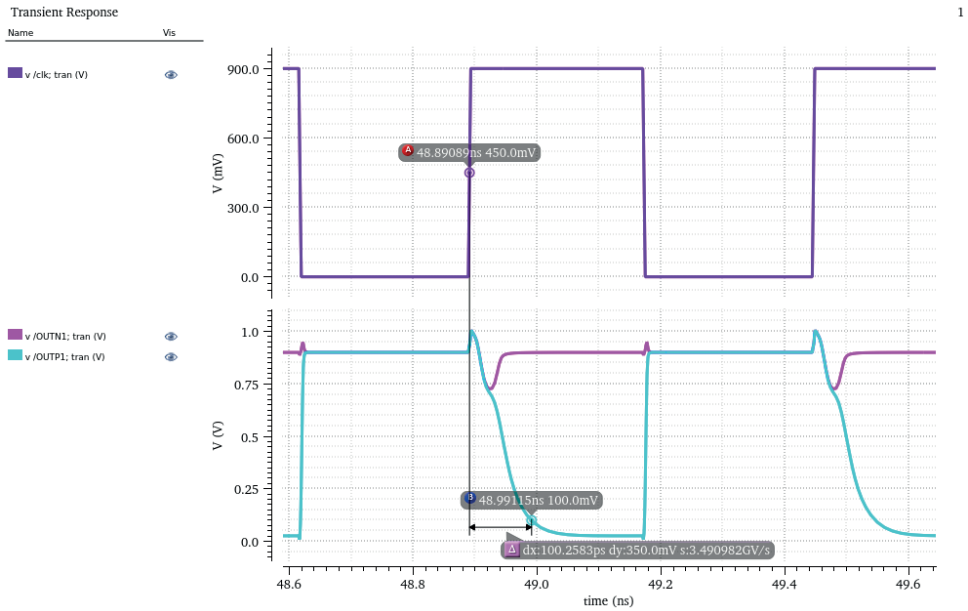

Figure 3.1: Decision time.

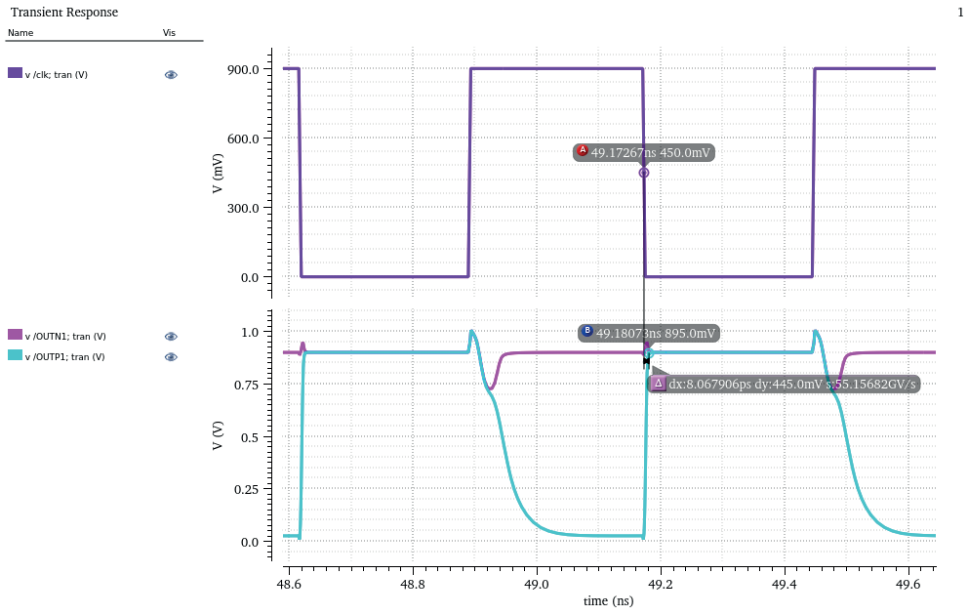

Figure 3.2: Reset time.

$$\overline{V_{n,\text{in}}^2} = \frac{\overline{V_{n,\text{out}}^2}(\text{total})}{A_v^2} \tag{3.2}$$

In the result display window, noise contribution of each transistor will be presented. Input transistors should contribute most of the noise. Otherwise, we can adjust the size of transistors to improve the noise performance.

However, using PSS + Pnoise simulation directly is not suitable for post-layout simulation. Since it could be affected by offset. It is common to determine the offset and then use the offset correction circuit to re-obtain the center point, then use PSS and Pnoise to do the analysis.

Another way can also be to find out what the offset is and then add a dc source in series to one of the input of the comparator (with the right polarity to cancel the offset) and get the right center point to do a PSS and Pnoise simulation.

The most precise method of measuring IRN is to do the transient noise simulation. That is why we set the threshold value of Pnoise according to it. A DC input is provided to the comparator input with the signal amplitude within expected noise amplitude. After the comparator works a large number (e.g. 1000) of times, the number of logic '1', and the number of logic '0' out of the comparator could be counted, as shown in Figure 3.3. Then we could get the probability of the correct cycles [5].

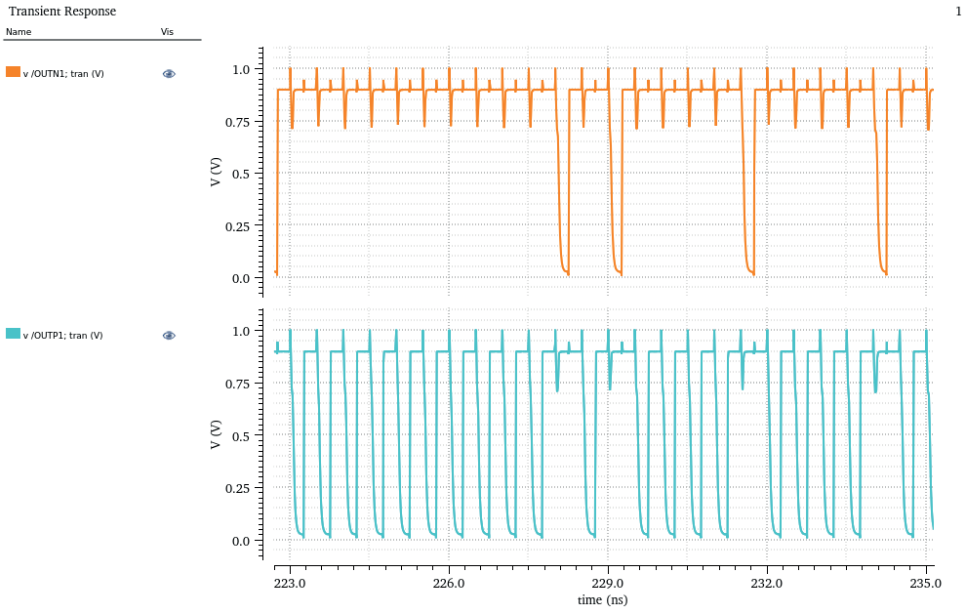

Figure 3.3: Waveform of correct cycles and incorrect cycles.

The inverse CDF (Cumulative Distribution Function) of the standard normal distribution is calculated for the given probabilities through MATLAB. This gives "std_x" which are the z-scores corresponding to the given probabilities. According

to the linear relationship, σ and µ can be found by fitting between the values and the corresponding inverse CDF values of the standard normal distribution.

$$\text{std\_x} = \frac{\text{input} - \mu}{\sigma} \tag{3.3}$$

Finally, we can get the input referred noise which is the value of σ. µ represents the offset. An example of the fitted image and calculated results for Strong-Arm Latch are shown in Figure 3.4 and Figure 3.5.

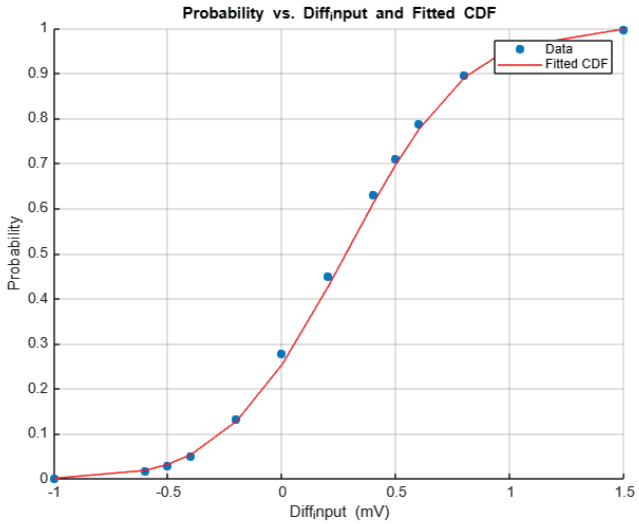

Figure 3.4: Example of fitted distribution.

Name	Value	Size	Class
Diff_input	*1x13 double*	1x13	double
cdf_values	*1x13 double*	1x13	double
intercept	-0.6608	1x1	double
mu	0.2791	1x1	double
p	[2.3674,-0.6608]	1x2	double
point	1000	1x1	double
probability	*1x13 double*	1x13	double
sigma	0.4224	1x1	double
slope	2.3674	1x1	double
std_x	*1x13 double*	1x13	double

Figure 3.5: Calculated results by MATLAB.

In terms of the value of the input, for pre-simulation, we should try some value around Vcm (450mV) because there is no offset. For instance, we set the positive input to Vcm + 0.5LSB and set the negative input to Vcm - 0.5LSB. So their differential input is LSB which is the assumed noise amplitude to sweep. For post-simulation, we should try a large range of values to locate a center point which might move due to offset. Then narrow it down around the center point for a more precise fit.

However, transient noise simulation requires quite long simulation time for enough accuracy and shows little insight into sources of noise.

In conclusion, PSS + Pnoise simulation has higher efficiency while transient noise simulation should be used as the final reference. These two methods should be validated against each other.

3.3 Kickback Noise

Kickback noise is not a physically existing property like input-referred noise. For each transistor, there is parasitic capacitance between the gate and the drain nodes. When the comparator start comparison, the large and fast voltage variation on the output nodes will be coupled back to the input nodes through that parasitic capacitance. Then the input voltage of the comparator that is connected to a charge redistribution based CDAC will be disturbed and this may result in incorrect ADC converted output [7].

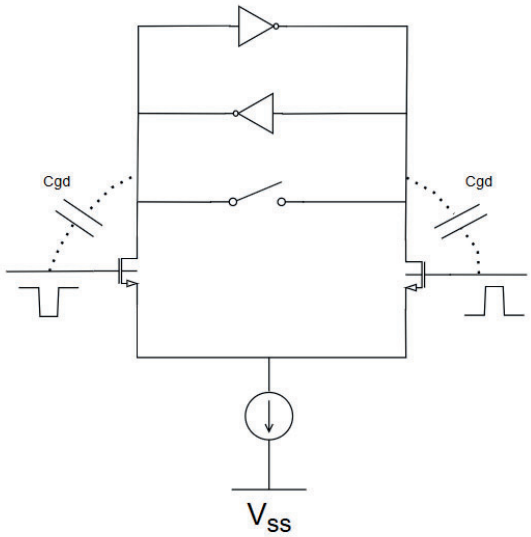

Figure 3.6: Kickback path.

For measuring this parameter, we introduced a structure as testbench which shows in Figure 3.7.

Two switches play an important role in this testbench. We separate the signal flow to three phases. During the first phase, S1 is connected and S2 is disconnected. The top plate of C_CDAC is pre-charged to a voltage of the source. The total capacitance of CDAC is 128fF and it is elaborated in 1.3. During the second phase, S1 is disconnected and S2 is connected. So the cap voltage can be connected to the input transistor. During the third phase, the comparator is clocked and start comparison. Then we can observe the voltage variation of VC node. To avoid some overlapping issue, the clocks are designed in Figure 3.8. They clock the S1, S2 switches and comparator, respectively.

The kickback for each input node would be found. Then we could calculate the differential value of VCP and VCN which is the final kickback noise. The common part of them will be counteracted during the comparison. However, the common mode component of kickback changes the common mode input voltage. It would make the offset dynamic and change the input-referred noise of the comparator as the thermal noise component changes with common mode of the comparator.

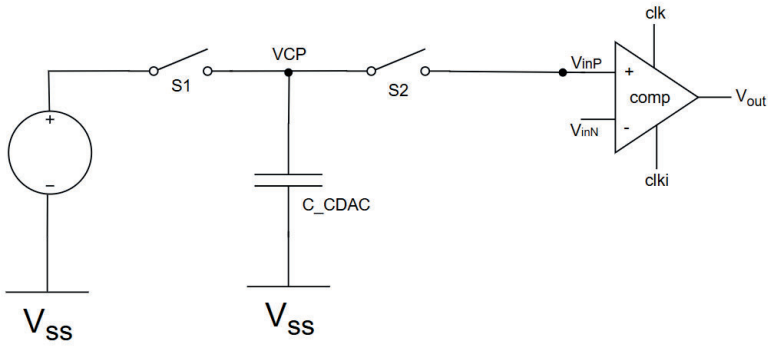

Figure 3.7: Test circuit of measuring kickback noise.

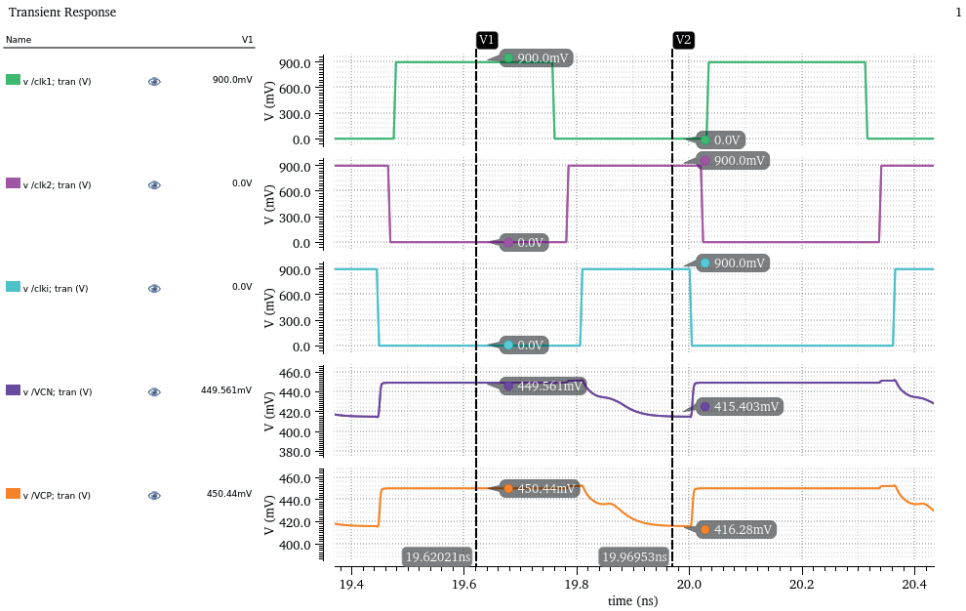

Figure 3.8: Example result of kickback noise.

3.4 Offset

Due to the layout asymmetry and mismatch in the manufacturing process of the transistors, the circuits exhibit a dc offset. It can limit the performance of comparator [8].

When measuring offset, we usually applied the ramp as input signal. The simulation time should be long enough to achieve good accuracy. In Figure 3.9, the waveform shows a transient response of Strong-Arm Latch under normal TT corner. The flip point of outputs could align with the intersection of inputs. Therefore, it dose not present any offset.

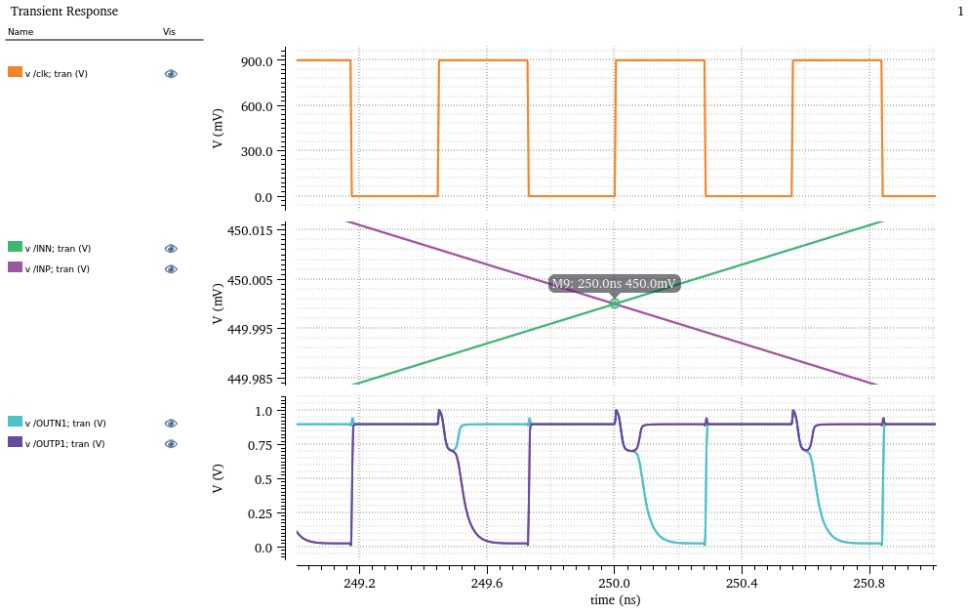

Figure 3.9: Example result of measuring offset.

To find out the influence of mismatch and process, Monte Carlo simulation should be implemented. Then the mean value and standard deviation can be found.

In Monte Carlo simulations, mean and standard deviation are key statistical metrics used to summarize and understand the results of the simulation [9].

The mean value is the average of all the outcomes generated by the Monte Carlo simulation. It is a measure of the central tendency of the data and gives an indication of where the bulk of the results lie. The mean provides an estimate of the expected value of the variable that are interested.

Mathematically, if x_i represents the individual result and N is the number of results, The mean μ is given by:

$$\mu = \frac{1}{N}\sum_{i=1}^{N} x_i \tag{3.4}$$

The standard deviation is a measure of the dispersion or variability of the results around the mean. It quantifies the amount of variation or spread in the results.

The standard deviation σ is calculated as the square root of the variance. The variance is the average of the squared differences between each outcome and the mean. Mathematically, if μ is the mean, the variance σ^2 and standard deviation σ are given by:

$$\sigma^2 = \frac{1}{N}\sum_{i=1}^{N}(x_i - \mu)^2 \tag{3.5}$$

$$\sigma = \sqrt{\sigma^2} \tag{3.6}$$

We also designed a structure to calibrate the offset by appling body biasing technique as shown in Figure 3.10. The bulk of NMOS can be biased to 2V under this technology, so we pre-charge the C1 to 2V during the first phase. When the calibration start, VC will gradually discharge so that we can find out the flip point of the comparator outputs. In other words, the calibration time can be found. The sensitivity is determined by the value of R1 and C1.

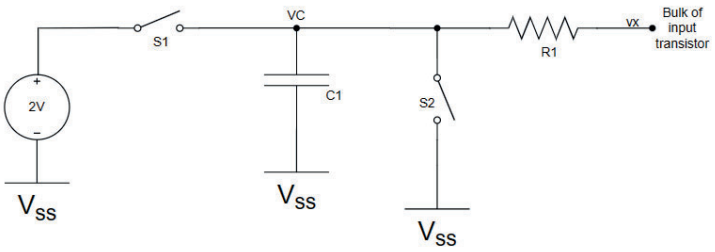

Figure 3.10: Conceptual offset calibration method.

Chapter 4

Simulation Results

4.1 Body Biasing Architecture

Usually, the bulk of NMOSs will be connected to the ground and the bulk of PMOSs will be connected to the power supply (i.e., not flip-well devices). While under the 22nm-FDSOI technology, we can apply a bias voltage to the substrate to lower the threshold voltage of the transistors, enabling them to turn on very quickly. In this thesis, we connect 2V to the bulk of NMOS transistors and -2V to the bulk of PMOS transistors which is the limited value of biasing. The figures below show the difference in terms of all of the structures over TT corner and 25°C. The first color in the list on the left side of the image corresponds to the normal architecture, the second color corresponds to 22nm-FDSOI. The starting point of the waveform is the LSB.

Each one of the architectures performs a great speed improvement after implementing the body biasing architecture except for the double-tail structure.

After careful inspection and consideration, we found that a better approach for the body biasing technique in this structure is to allow the input pair transistors and the cross-coupled pair transistors to achieve self-biasing [14]. It makes the input transistors as high-Vth devices for faster off which is different with other low-Vth biasing technique. However, it results in worse power dissipation and unbalanced input transistor pair. Since the kickback effect of the double-tail structure has influenced by the switching transistors below the input transistors, we will maintain the original design.

Table 4.1: Comparison of decision time between normal technology and body-biasing technique, Vin = LSB.

Structures	Normal	22FDX	Improvement
SA (pS)	128.1	101.3	26.8
DT (pS)	74.4	82.1	-7.7
TT1 (pS)	85.9	66.2	19.3
TT2 (pS)	79.3	60.8	18.5

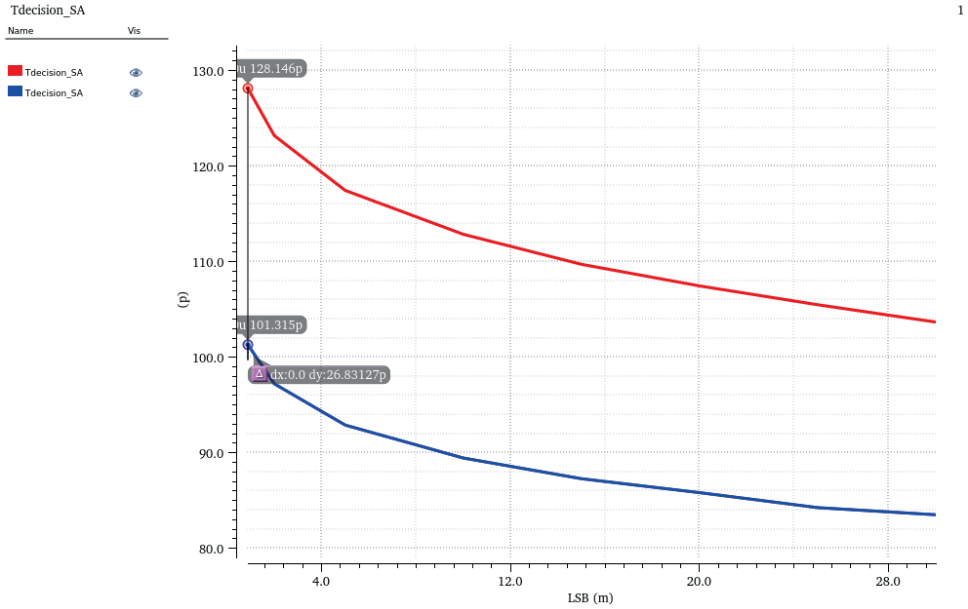

Figure 4.1: Comparison between normal architecture and body biasing architecture for Strong-Arm Latch, starting from LSB.

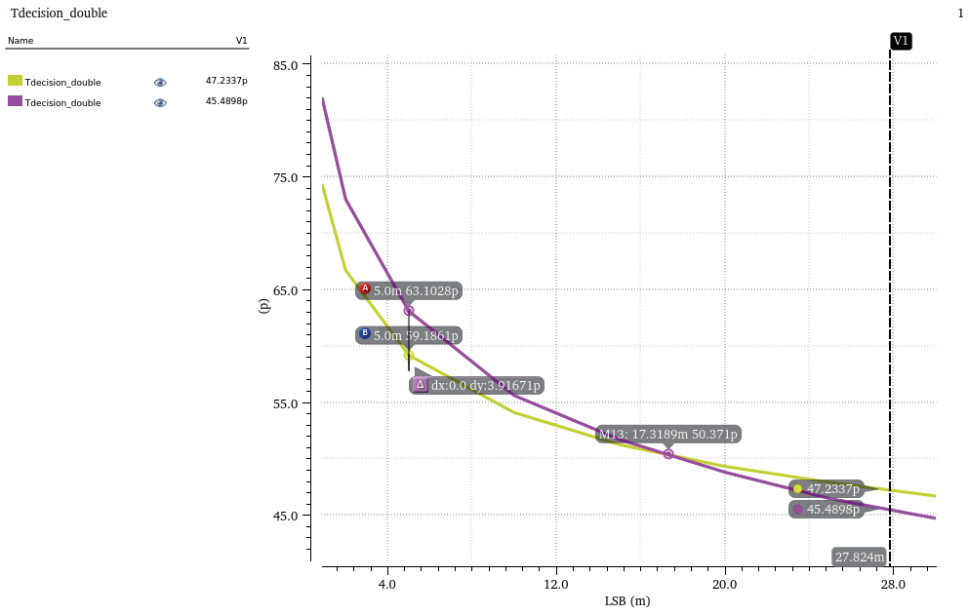

Figure 4.2: Comparison between normal architecture and body biasing architecture for Improved Double-Tail Comparator, starting from LSB.

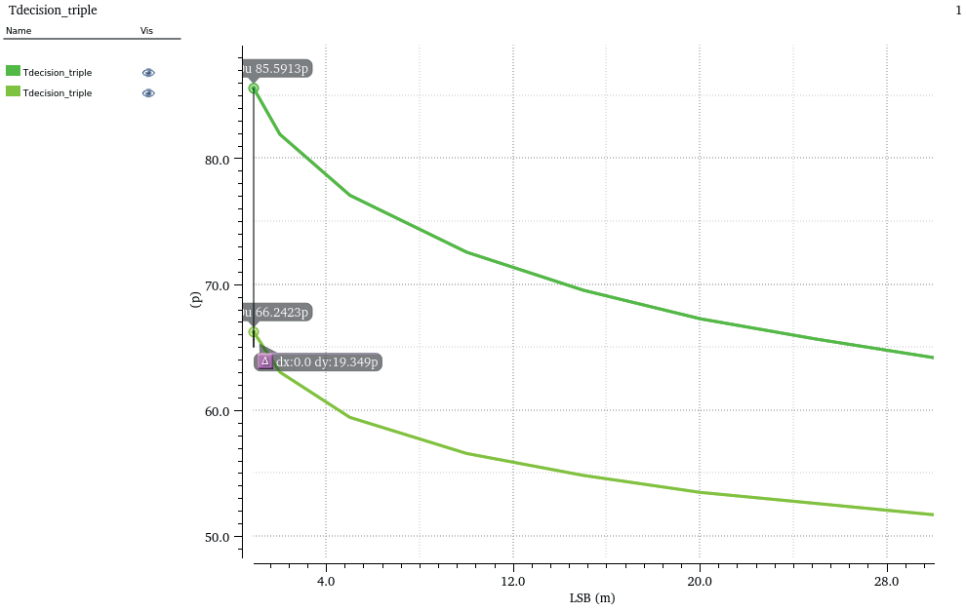

Figure 4.3: Comparison between normal architecture and body biasing architecture for triple-tail comparator, starting from LSB.

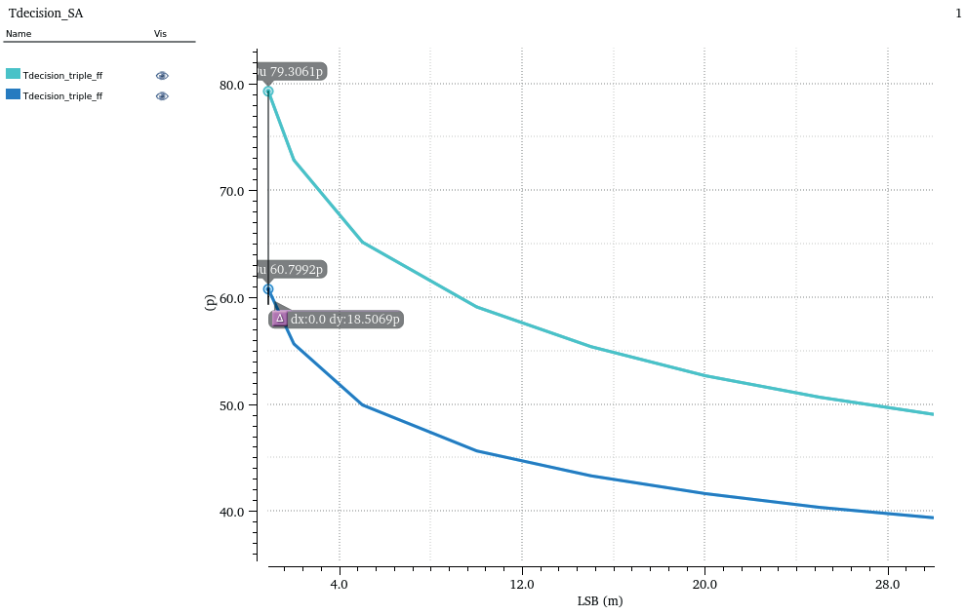

Figure 4.4: Comparison between normal architecture and body biasing architecture for triple-tail comparator with a feedforward path, starting from LSB.

4.2 Speed

The table and figures below depict the transient simulation results of speed for each structure. They clearly demonstrate the differences between the various structures.

Table 4.2: Comparison of decision time between various structures under different corners, Vin = LSB.

Structures	TT	FF	SS
SA (pS)	101.3	94.6	113.2
DT (pS)	82.0	77.2	88.8
TT1 (pS)	66.2	60.3	75.5
TT2 (pS)	60.8	55.3	68.8

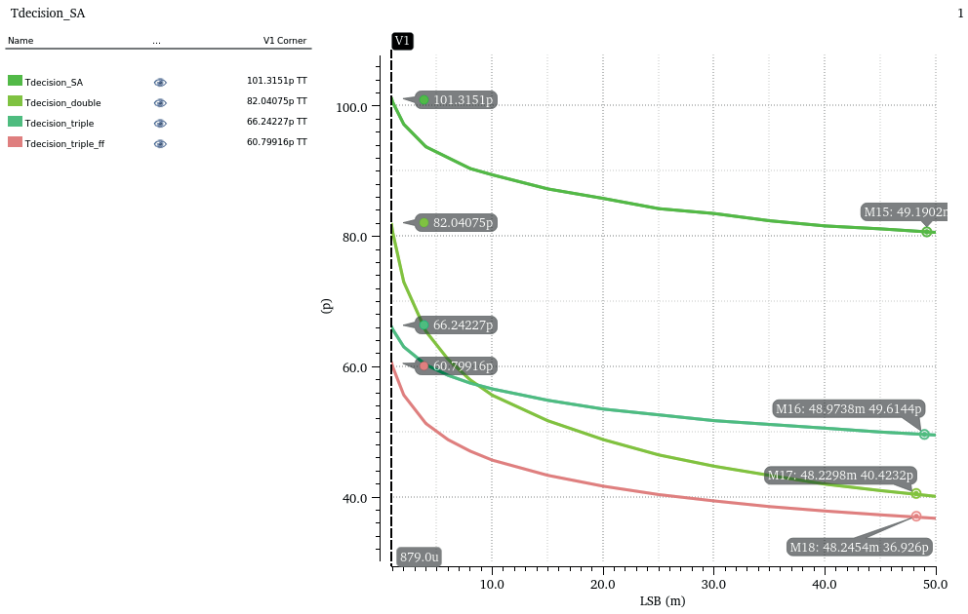

Figure 4.5: Decision time with respect to differential input voltage under TT corner.

The Strong-Arm Latch exhibits a significantly slower speed performance during the whole time. When the differential input voltage is LSB, triple-tail structures exhibit the best speed performance. However, as the differential input voltage increases, the architecture of triple-tail without a feedforward path experiences a speed limitation. Under SS corner, this speed limitation manifests even earlier. While the feedforward path shows a great performance for eliminating this limitation.

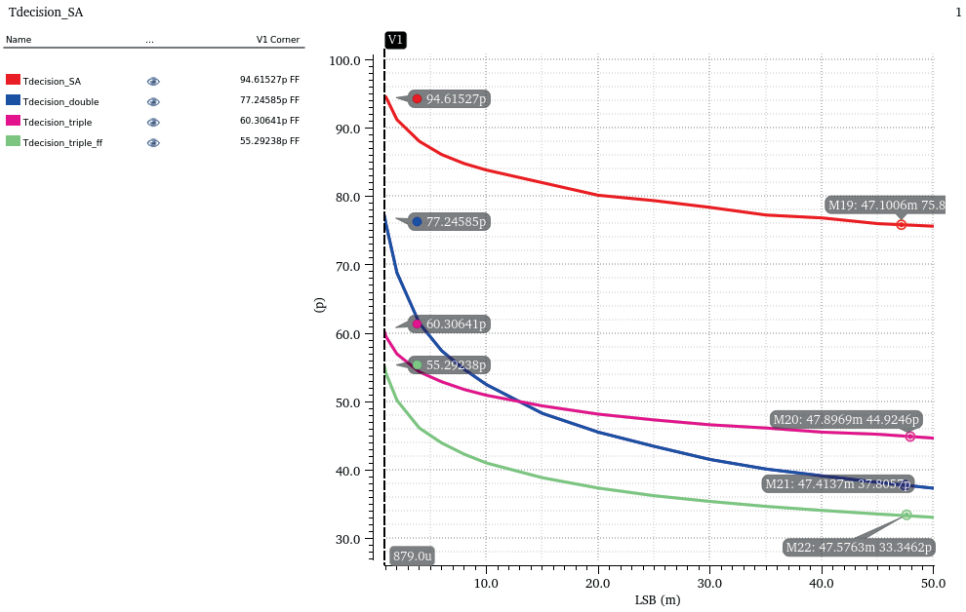

Figure 4.6: Decision time with respect to differential input voltage under FF corner.

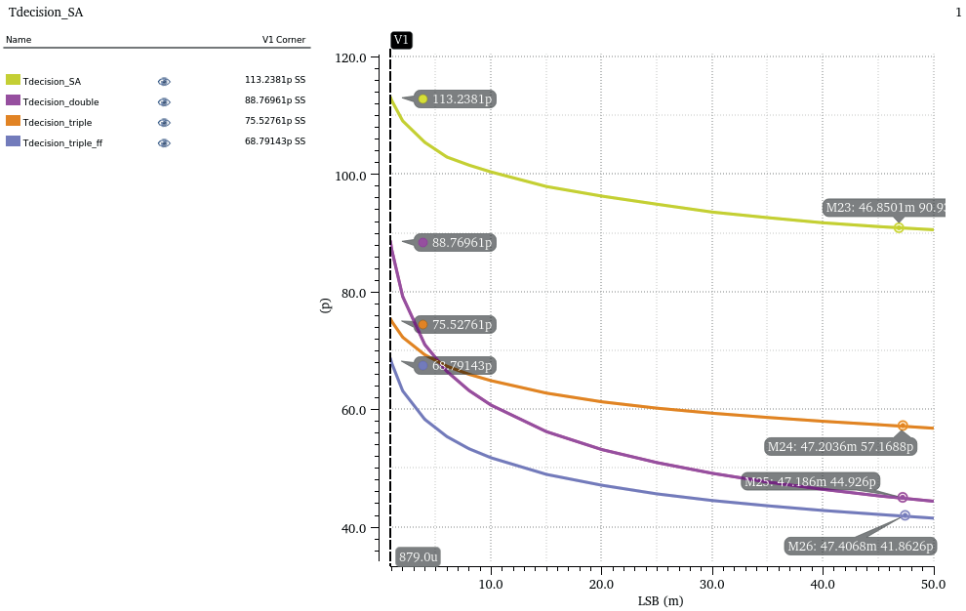

Figure 4.7: Decision time with respect to differential input voltage under SS corner.

4.3 Input-Referred Noise

For a fair comparison, all the comparators are designed to have similar input referred noise which is around half of LSB. Fitted CDF can be seen from Figure 4.8 to Figure 4.11, the calculated results for IRN and offset are also organized in Table 4.3.

Table 4.3: Results from input-referred noise simulations.

Parameters	SA	DT	TT1	TT2
Offset, μ (mV)	-0.019	-0.006	0.061	-0.028
IRN, σ (μV)	458.7	444.2	437.7	430.7

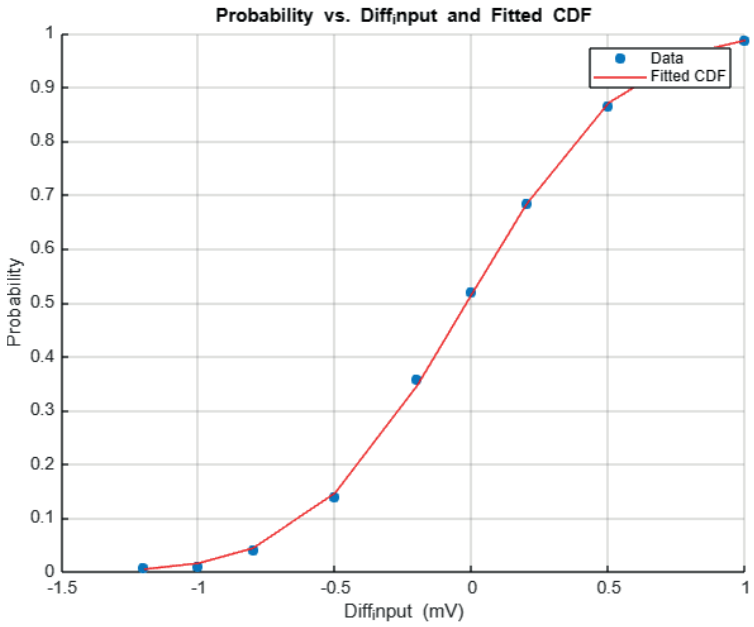

Figure 4.8: Probability vs. Diff_input and Fitted CDF for Strong-Arm Latch.

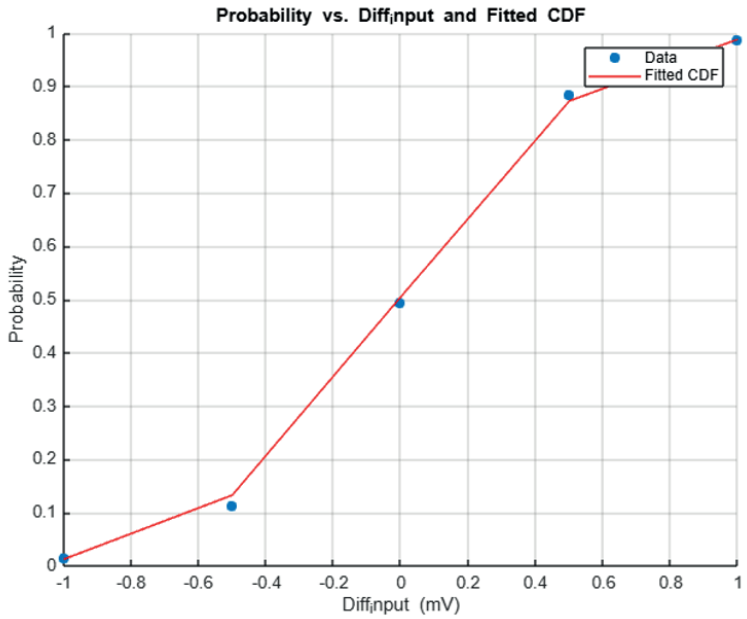

Figure 4.9: Probability vs. Diff_input and Fitted CDF for Double-tail structure comparator.

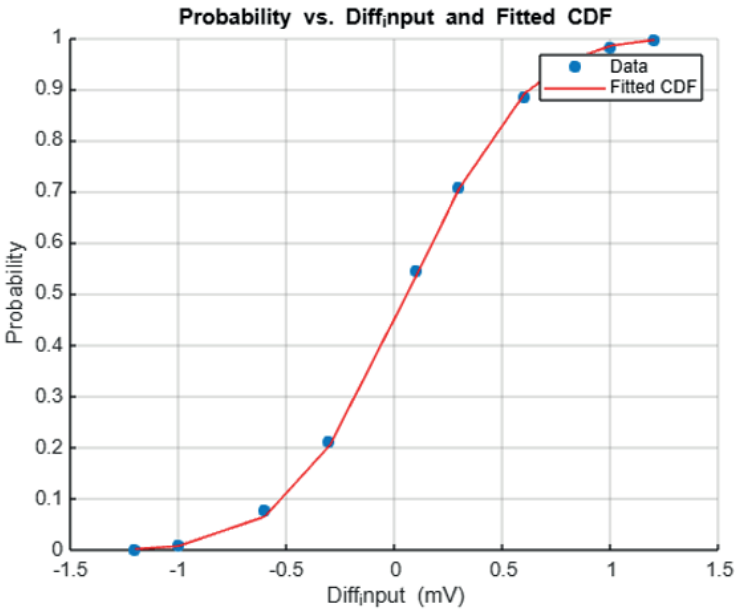

Figure 4.10: Probability vs. Diff_input and Fitted CDF for Triple-tail structure comparator.

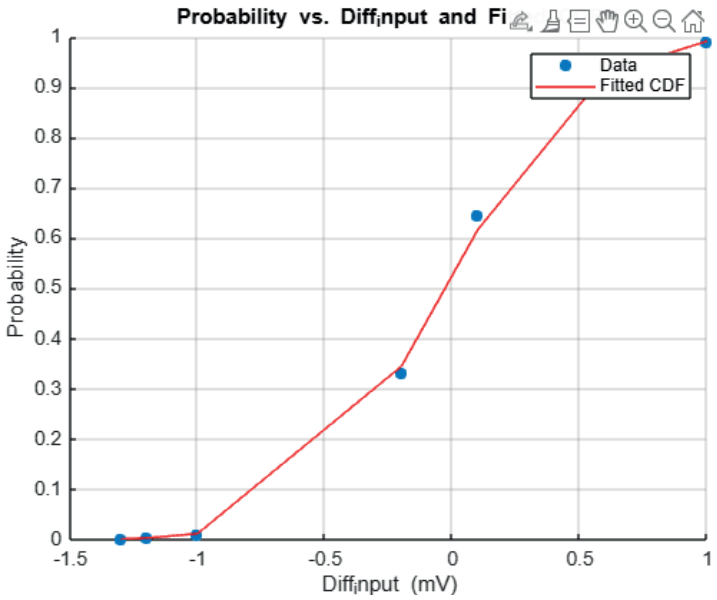

Figure 4.11: Probability vs. Diff_input and Fitted CDF for Triple-tail structure comparator with a feedforward path.

4.4 Kickback Noise

As shown in Table 4.4, double-tail structure performs the worst for kickback. The definition for VC node can be found in Figure 3.7. VCN means the negative input node and VCP means the positive input node. The differential kickback noise also be measured under Monte Carlo simulation since it could be affected by the process variations and mismatch.

In double-tail architecture, the special cross-coupling pair amplifies the gain of the first-stage amplification phase. Since the faster amplification speed results in larger voltage variations at the input node due to the existence of parasitic capacitance. Therefore, it could make sense for the larger kickback of the double-tail structure.

For double-tail structure in Figure 2.2, when fn or fp is suddenly pulled up to VDD, the gate voltage of the corresponding input transistor is seriously disturbed due to circuit asymmetricity, it can be seen in Figure 4.12. In this case, VCN is pulled up due to the sudden voltage change of fp which results in the smaller common kickback and larger differential kickback.

For a fair comparison, all the input pairs have the same size. Therefore, other structures perform similarly of this parameter.

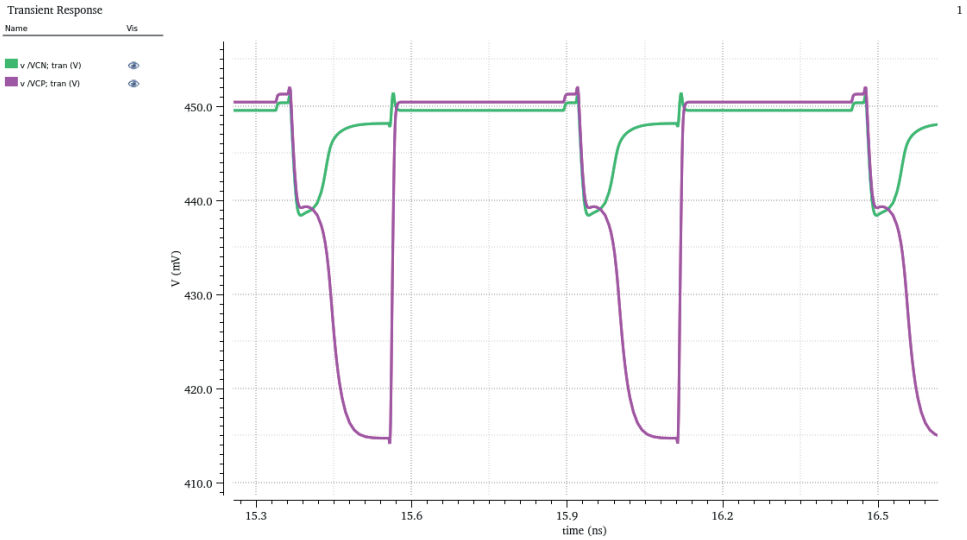

Figure 4.12: Transient simulation waveforms of VCN and VCP for double-tail structure.

Table 4.4: Kickback noise simulation results, Vin = LSB, TT corner, 25°C.

Structures	Common kickback	Differential kickback	MC_diff
SA	34.3mV	3.7µV	79.7µV
DT	18.5mV	34.3mV	33.6mV
TT1	31.3mV	10.3µV	123.6µV
TT2	31.3mV	11.4µV	129.0µV

4.5 Offset

Figures and table below show the Monte Carlo-simulated error in input voltage offset voltage due to mismatch, all at 25°C, over 400 samples per corner.

Table 4.5: Monte Carlo simulations Results for offset, temperature = 25°C.

Parameters	SA	DT	TT1	TT2
mean (µV)	145.8	-79.2	-360.6	-168.4
σ (mV)	1.97	2.11	1.99	2.11

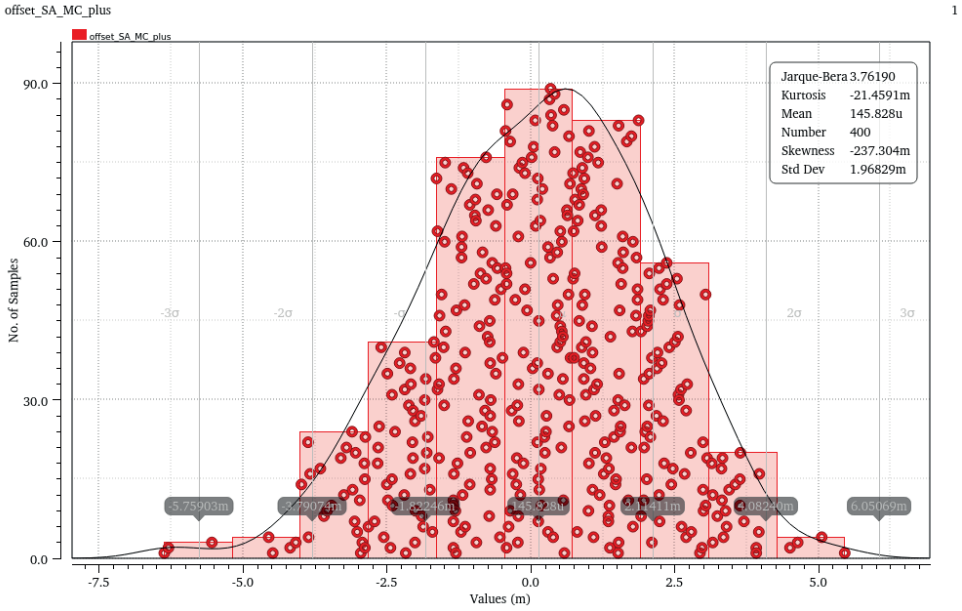

Figure 4.13: Histogram over Monte Carlo simulations for Strong-Arm Latch.

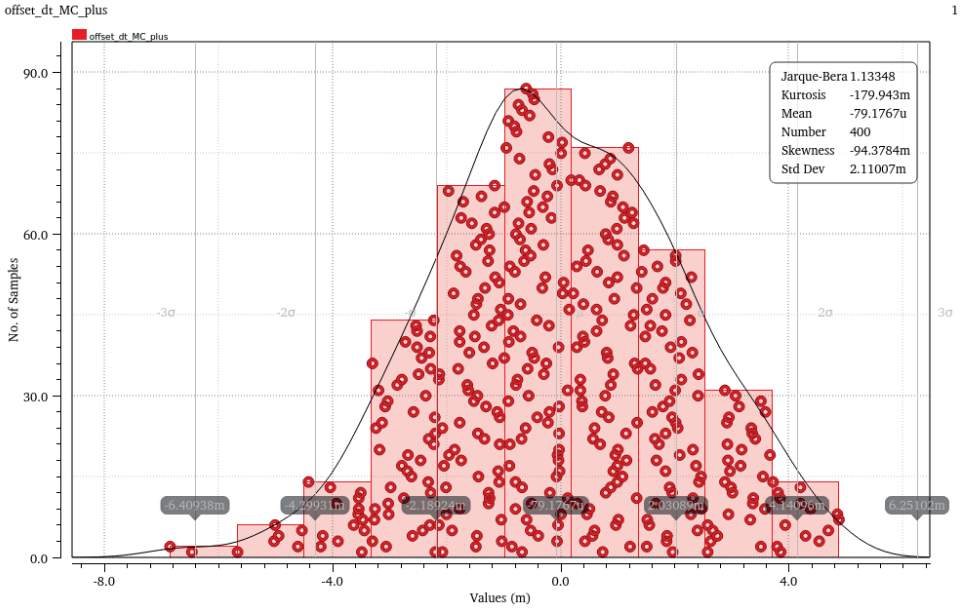

Figure 4.14: Histogram over Monte Carlo simulations for Double-tail structure comparator.

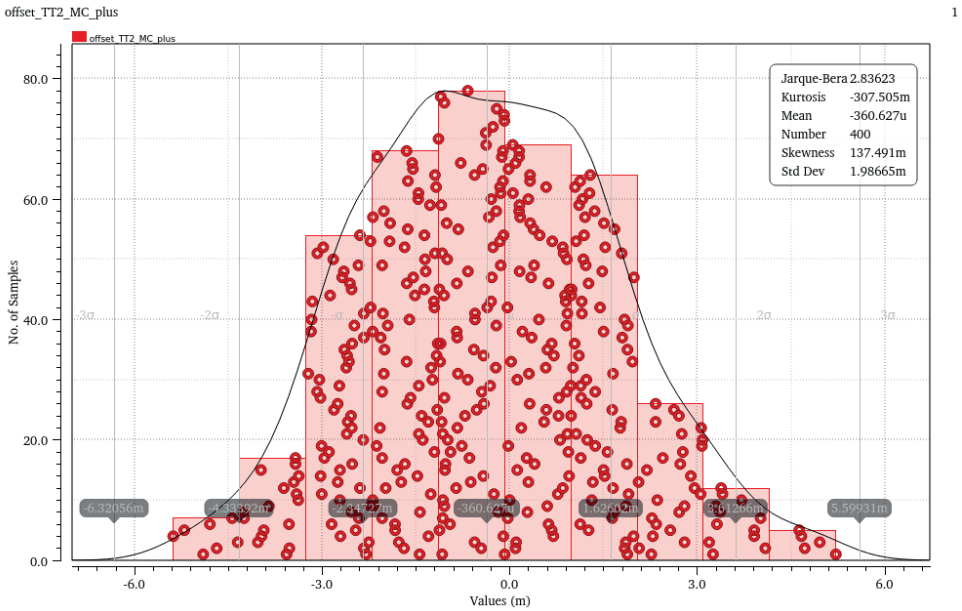

Figure 4.15: Histogram over Monte Carlo simulations for Triple-tail structure comparator.

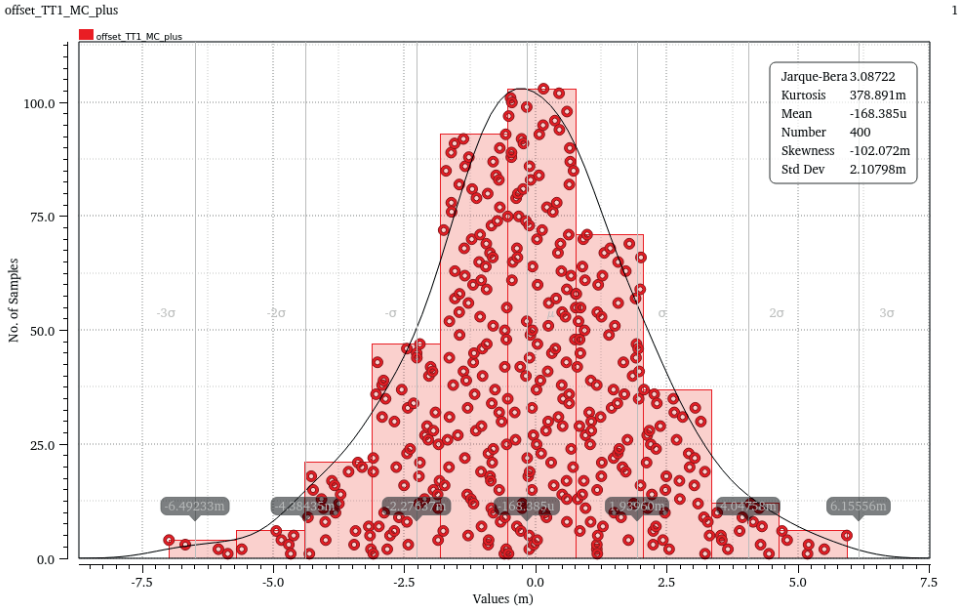

Figure 4.16: Histogram over Monte Carlo simulations for Triple-tail structure comparator with a feedforward path.

4.6 Summary

Table 4.6 illustrates a summary of results in the tests. The results of kickback noise is the differential kickback noise under Monte Carlo simulation. Obviously, all the simulation results meet the specifications except the kickback noise of double-tail structure comparator. To advance the research on DT, a kickback noise cancelling technique should be introduced.

Table 4.6: Summary of Results.

Parameters	SA	DT	TT1	TT2
Decision time (pS)	101.3	82.0	66.2	60.8
Reset time (pS)	7.32	19.81	5.97	6.08
IRN (µVrms)	458.7	444.2	437.7	430.7
Kickback Noise (µV)	79.7	33.6mV	123.6	129.0
Offset (mV)	1.97	2.11	1.99	2.11
Power consumption (µW)	66.4	159.0	99.7	144.4

Chapter 5

Layout and Post-layout Simulation

5.1 Analysis of Technology

Double Patterning Technology

Due to the small spacing of metal layers, DPT (double patterning technology) splits these layers into two masks to enable reliable printing and higher density chip design using current optical lithography.

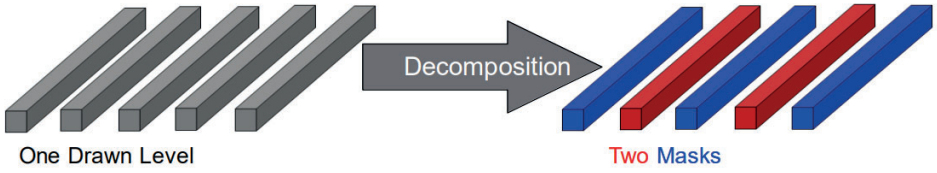

Figure 5.1: Decomposition of metal layers.

Flip-Well Body Bias Architecture

It is possible to enable the flip-well architecture (NMOSs are over NWELL, PMOSs are over PWELL). Since all the comparators are applied body biasing architecture, deep N-well is also implemented. The deep n-well can create isolation between two layers of p-well regions, allowing one of the p-wells to be biased separately while the p-substrate is connected to ground.

Consideration

Good layout design is essential for the performance of the comparators. In layout design, attention should be paid to avoiding cluttered wiring, minimizing circuit area, and reducing interconnect capacitance. Additionally, proper placement and connection of devices should be considered to minimize signal delay and power consumption [15].

5.2 Layout

Figure 5.2 to Figure 5.5 show the layout diagram of each comparator topology. The active areas of them are $9.2\,\mu\text{m} \times 8.7\,\mu\text{m}$, $7.8\,\mu\text{m} \times 8.6\,\mu\text{m}$, $8.9\,\mu\text{m} \times 9.1\,\mu\text{m}$, and $8.9\,\mu\text{m} \times 9.1\,\mu\text{m}$, respectively. They are all designed to be as symmetrical as possible. The body biasing connections and flip-well structure are done carefully.

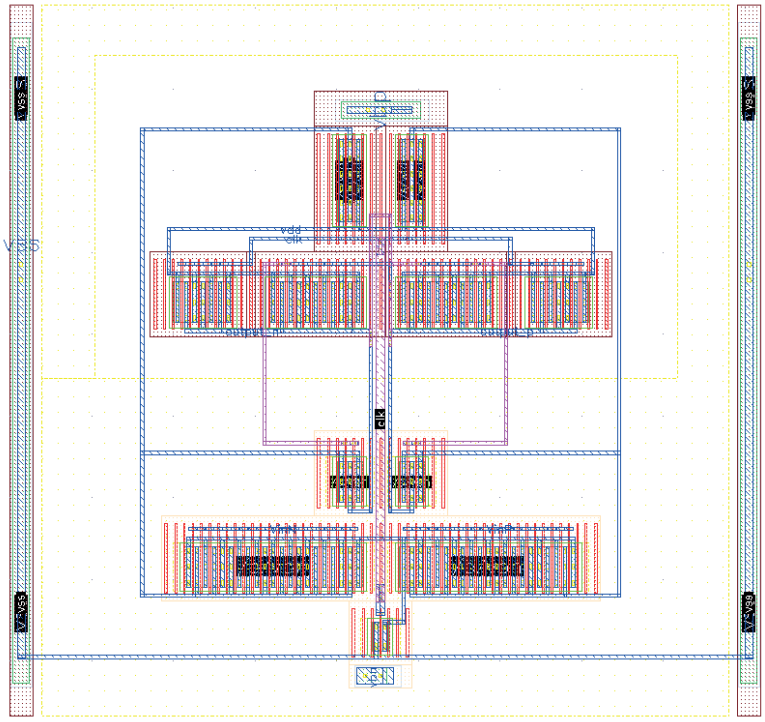

Figure 5.2: Layout of Strong-Arm Latch.

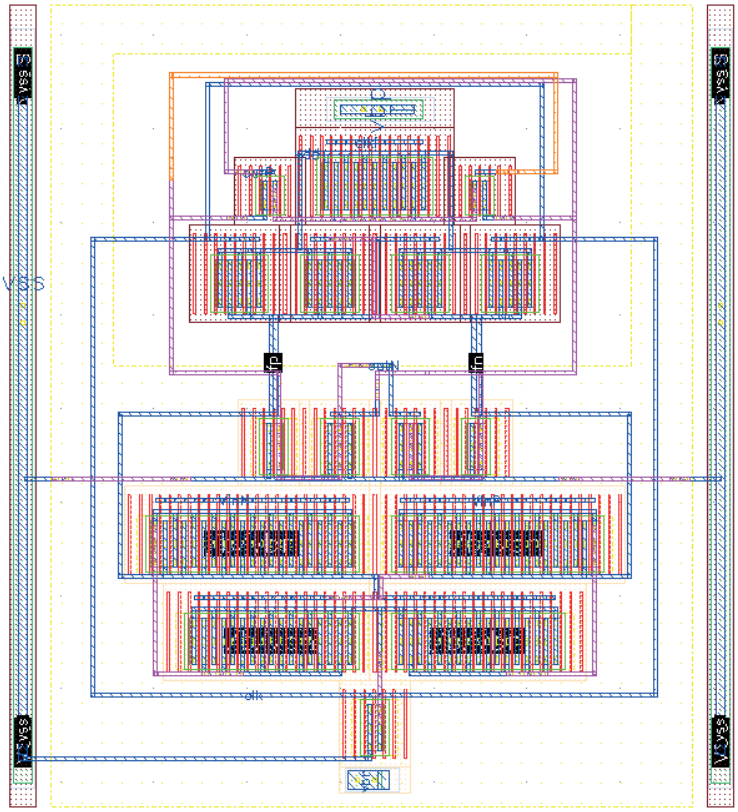

Figure 5.3: Layout of Double-tail structure comparator.

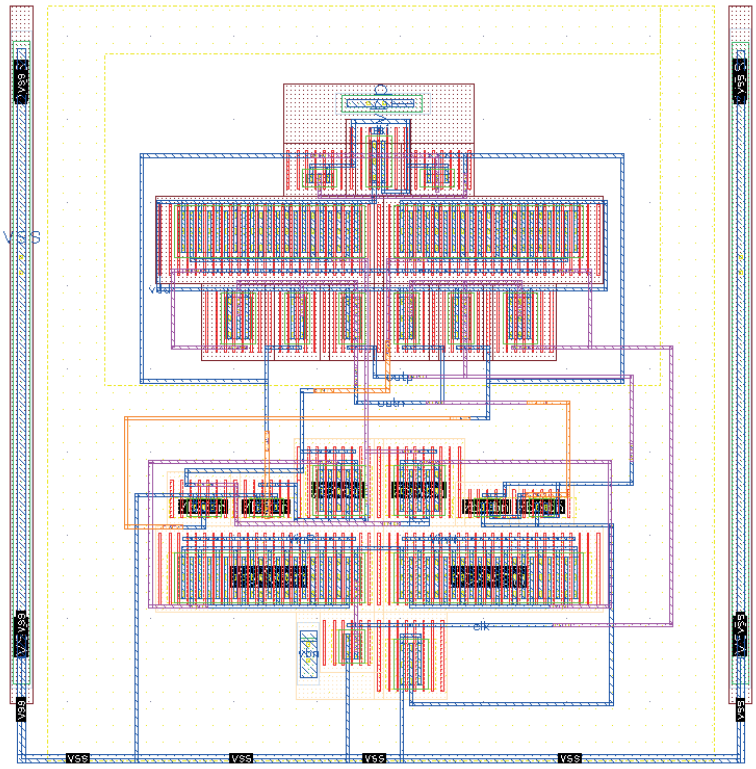

Figure 5.4: Layout of Triple-tail structure comparator.

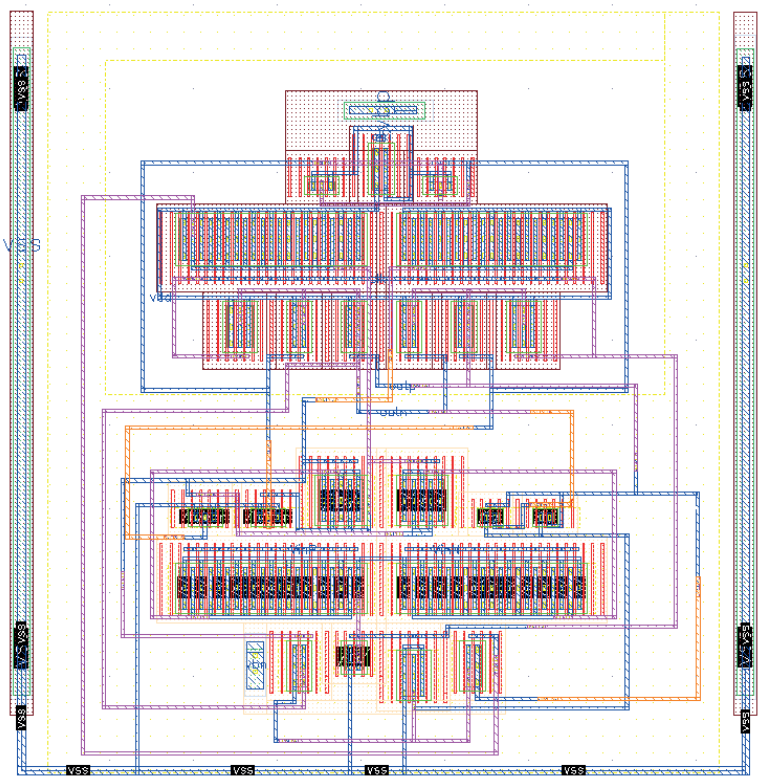

Figure 5.5: Layout of Triple-tail structure comparator with a feed-forward path.

5.3 Post-Layout Simulation

Figure 5.6 and Figure 5.7 the deterioration of speed after post-simulation, especially the triple-tail structure. Because there are more complex relations between these transistors, floorplan and alignments are also more complicated. Therefore, due to the introduction of parasitic parameters, interconnect delays and some other issues, the comparators show a worse performance on speed.

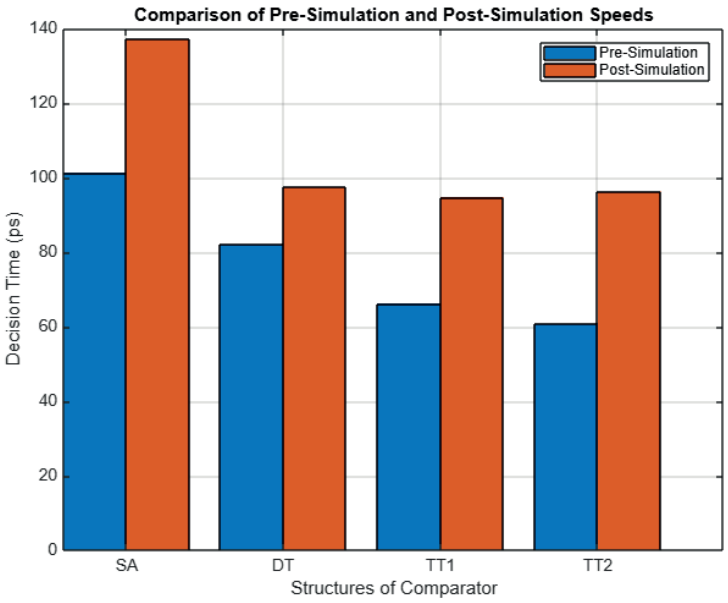

Figure 5.6: Comparison of Pre-Simulation and Post-Simulation of Decision Time.

Figure 5.8 illustrates the difference of input referred noise. Some are better and some are worse. But the variations are all within 20%. There are some reasons below:

The intrinsic noise sources (such as thermal noise and flicker noise) are inherent to the devices (transistors, resistors, etc.) themselves and are modeled accurately in both pre-layout and post-layout simulations. These intrinsic noise characteristics do not change significantly between the two stages [16].

Although post-layout simulations include parasitic elements , these parasitics generally have a limited impact on the noise performance compared to their impact on signal propagation delay and speed. Parasitics can slightly alter the frequency response, but their effects on overall noise is far less.

The underlying circuit topology does not change from pre-layout to post-layout simulations. The noise performance is almost solely determined by the circuit design, which will remain unchanged. The layout does introduce further parasitic elements, but it doesn't change essential noise characteristics of the devices and of the circuit topology.

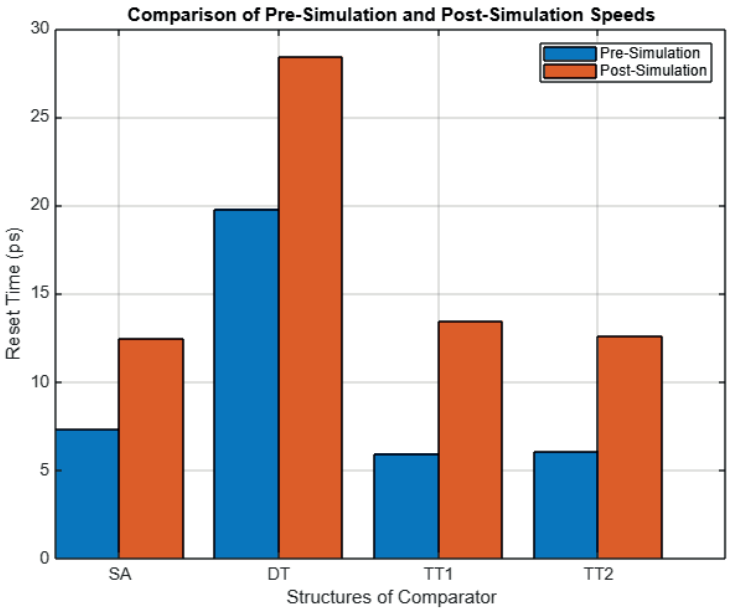

Figure 5.7: Comparison of Pre-Simulation and Post-Simulation of Reset Time.

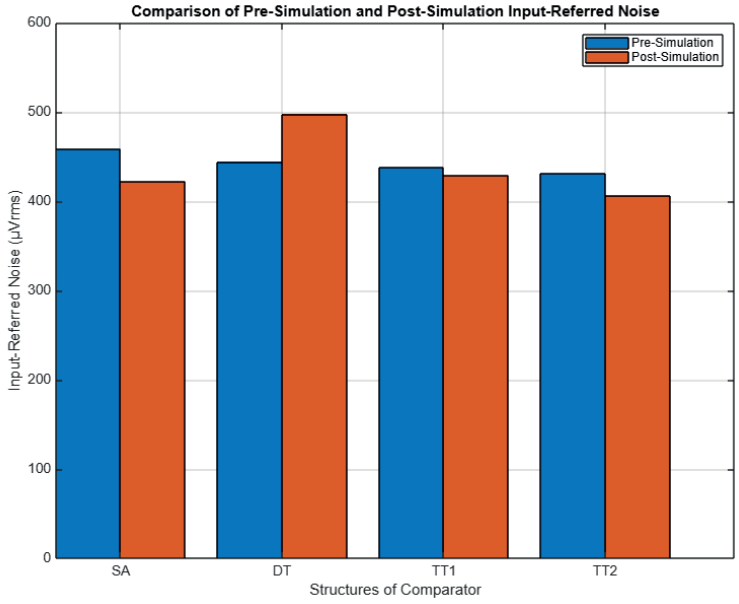

Figure 5.8: Comparison of Pre-Simulation and Post-Simulation of IRN.

Figure 5.9 depicts the change of the differential kickback noise under Monte Carlo simulation. Here we disgard the double-tail structure since it can not meet the system specification. Once the layout is complete, the process variations introduce the physical mismatches of the transistors with other elements. It may cause asymmetries in the corresponding circuit, which enhances the probability of suffering from the kickback noise.

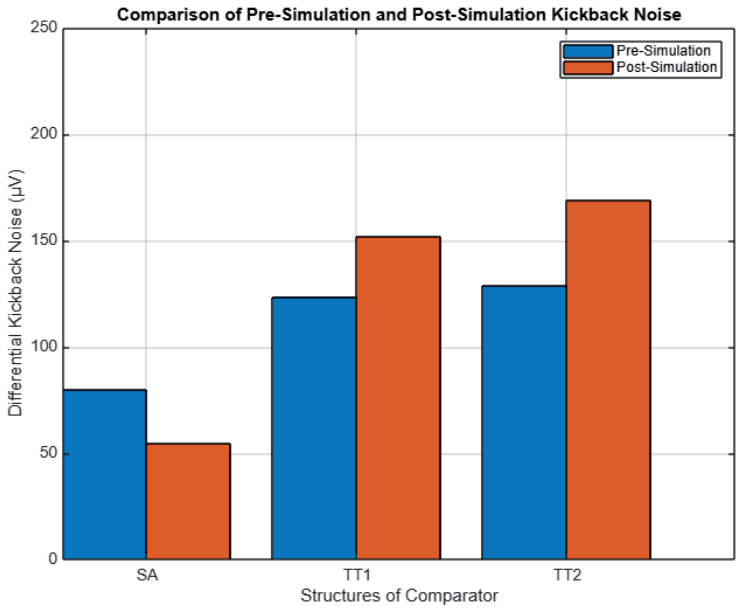

Figure 5.9: Comparison of Pre-Simulation and Post-Simulation of Kickback Noise.

Figure 5.9 illustrates a slight change in power consumption. Although parasitic capacitances and resistances can affect signal propagation delays, they have less of an effect on dynamic power consumption because an increase in parasitic capacitance only slightly increases the energy consumption for charging and discharging.

The temperature is a factor that is included in post-simulation to view its effect on the performance of the circuit. Some circuits operating at elevated temperatures might automatically avoid overheating, hence showing less power consumption in the post-simulation.

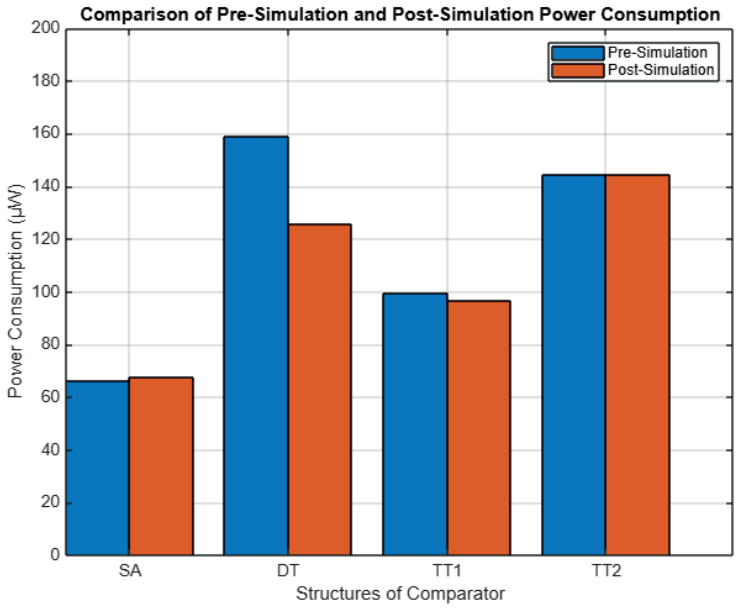

Figure 5.10: Comparison of Pre-Simulation and Post-Simulation of Power Consumption.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

This thesis has successfully designed and validated four high-speed comparator architectures capable of meeting specific performance requirements concerning speed, input-referred noise, and kickback noise.

The workflow followed the steps from a theoretical study and literature review to identifying goals, schematic design, pre-layout simulation, layout design, and post-layout simulation.

The designs of the comparators will thus be characterized by a high speed, becoming suitable for our specific ADC systems. The introduction of structures and optimal choice of sizes of transistors help reduce delay and noise. It is also significant to test methods of parameter measurements and implement achievable test-benches. 22nm-FDSOI was very crucial in providing better speed performance. Post-layout simulations confirmed the robustness of the designs, with a bit deviations in performance metrics compared to pre-layout simulations. The trustworthy result also shows how the structure is continuously perfected.

Finally, the fastest speed is around 95pS, and the most significant power consumption is less than 150µW for post-layout simulation.

6.2 Future Work

This thesis research is general and open to many possible efforts based on this work. Some directions for the future work of the thesis are summarized below:

Better layout design. The lack of good layout design makes the speed and kickback performance not good enough.

Integrate the designed comparators into a complete ADC system and perform lots of testing of the system at the system level. It will provide a practical insight into the performance of these comparators in real-time applications and help to identify unforeseen problems that need fixing.

Nowadays, with the increase in the demand of the market for higher resolution ADCs, it is meaningful to explore and design newer techniques or architectures for higher-bit ADCs in the pursuit of high-speed performance.

Power savings without loss of speed and accuracy can be achieved by exploring techniques such as sub-threshold and near-threshold operation [17].

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Appendix A

Some extra material

A.1 Matlab Code for Fitting

Here is the MATLAB code for fitting σ and μ:

Listing A.1: MATLAB Code for Fitting

```
Diff_input = [-1.6 -1.4 -1.2 -1 -0.8 -0.6 -0.4 0.1];
% example input, mV

point = 1000;
probability = [12 46 112 247 404 585 752 978] / point;

% Calculate the inverse cumulative distribution function
% values of the standard normal distribution
std_x = norminv(probability);

% Fit a linear relationship between std_x and offset
p = polyfit(Diff_input, std_x, 1);

% p contains the fitting coefficients
% p(1) is the slope, p(2) is the intercept
slope = p(1);
intercept = p(2);
sigma = 1 / slope;
mu = -intercept * sigma;

% Generate the fitted CDF values
cdf_values = normcdf(Diff_input, mu, sigma);

% Plot the scatter plot and the fitted CDF curve
figure;
scatter(Diff_input, probability, 'filled');

% Use scatter plot to show actual probability values
hold on;
```

```
plot(Diff_input, cdf_values, 'r-');

% Use line plot to show fitted CDF
hold off;
xlabel('Diff\_input(mV)');
ylabel('Probability');
legend('Data', 'Fitted CDF');
title('Probability vs. Diff\_input and Fitted CDF');
grid on;
```

Printed by Tryckeriet i E-huset, Lund 2024

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