Wideband Matching Network and Antenna Switch Design in mmWave Transceivers for Transition from FR2 to FR3 Band

Gayathri Krishnasamy
`ga7771kr-s@student.lu.se`

Department of Electrical and Information Technology
Lund University

Academic Supervisor: Baktash Behmanesh

Industrial Supervisors: Per-Olof Brandt

and

Meshach Milon Paul Pears Pradeep Kumar

Examiner: Pietro Andreani

September 16, 2024

Abstract

6G technology is set to revolutionize wireless communication, advancing far beyond speed enhancements to reshape how we interact with technology. A key factor in this evolution is the efficient use of the radio spectrum, particularly in the centimeter-wave (FR3) bands, ranging from 7 GHz to 24 GHz. This thesis investigates strategies for adapting FR2 transceivers to operate in FR3 frequencies through advanced tuning and wideband matching techniques. Additionally, it presents the design of an antenna switch optimized for this frequency range.

The research leverages 22nm Fully Depleted Silicon On Insulator (FDSOI) technology, incorporating both pre-layout and post-layout analyses to mitigate parasitic effects and unwanted coupling. This comprehensive methodology ensures optimal performance in terms of bandwidth and impedance matching. Post-layout simulations revealed that the matching networks for both the Power Amplifier (PA) and Low Noise Amplifier (LNA) achieved a wide bandwidth, thanks to careful design modifications addressing parasitics such as capacitance, resistance, and signal coupling. Moreover, the antenna switch design demonstrated excellent performance, with an isolation of 37 dB and an insertion loss of 1.19 dB, making it suitable for high-frequency applications.

Future work will aim to refine the design further by enhancing bandwidth while reducing the overall footprint. It will also explore additional circuit techniques to improve the matching network's performance, as well as finalize the layout design and post-layout simulations for the antenna switch to meet precise performance specifications.

Acknowledgements

I would like to extend my heartfelt gratitude to my industrial supervisors, Per-Olof Brandt and Meshach Milon, for their steadfast guidance, support, and insightful feedback throughout this thesis. Their expertise and encouragement have been truly invaluable.

I am also deeply appreciative of BeammWave in Lund for offering me the opportunity to collaborate on this research, as well as for providing the necessary tools and a supportive environment that were essential for its successful completion.

My sincere thanks go to my academic supervisor, Baktash Behmanesh, and my examiner, Pietro Andreani, for their unwavering support and constructive feedback. Additionally, I am grateful to the esteemed professors at the Faculty of Engineering (LTH), Department of Electrical and Information Technology at Lund University, whose mentorship has been instrumental in developing the skills and knowledge required for this research.

Finally, I am deeply grateful for the unwavering support of my family and friends, whose encouragement and belief in me have been instrumental in completing this thesis.

Popular Science Summary

Imagine your smartphone or internet connection working faster than ever before, with minimal delay and strong connectivity for all your smart devices.This is the promise of the Frequency Range 3 (FR3) band, a key player in the future of 5G and 6G technology. Operating between 7GHz and 24GHz, FR3 can offer lightning fast-data speeds and incredible support for the Internet of Things (IOT), which includes everything from smart home devices to autonomous vehicles.But there's a catch, while FR3 can deliver impressive performance, it also comes with challenges. The high frequencies used in FR3 mean that signals can't travel as far and struggle to penetrate obstacles like walls. Additionally, setting up the infrastructure fro FR3 is costly. To make the most of this technology, we need to overcome these hurdles with advanced technology, strategic planning, and supportive regulations.

One of the critical components in making this happen is the Radio Frequency (RF) transceiver. Think of it as the communication hub of wireless technology, capable of both sending and receiving signals. For FR3 to work effectively, we need to fine- tune these transceivers so they operate seamlessly at the higher frequencies of FR3. This involves adjusting their internal components to handle the new frequency ranges and ensuring that the signals are strong and clear. This achieved by a circuit called matching networks. Another essential part of this setup is the antenna switch, which directs signals to the right path or antenna. This helps ensure that communication remains clear and reliable.

During our work, we encountered challenges in making these networks perform perfectly. Parasitics (unwanted electrical effects) and coupling (interference between components) made precise tuning difficult. Overcoming these issues required careful adjustment to ensure that the technology would work as intended and deliver the fast, reliable connections we're aiming for.

In summary, while the FR3 band holds great promise for the future of wireless communication, turning that promise into reality requires overcoming technical challenges. With continued innovation and careful planning, we can unlock its full potential and pave the way for a new era of connectivity.

Table of Contents

List of Figures

List of Tables

List of Abbreviations

RF	Radio Frequency
IOT	Internet of Things
FR3	Frequency Range 3
ICs	Integrated Circuits
LNA	Low Noise Amplifier
IF	Intermediate Frequency
LO	Local Oscillator
PLL	Phase Locked Loop
ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
PA	Power Amplifier
BPF	Band Pass Filter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IP2	Second Order Intercept Point
IP3	Third Order Intercept Point
FDSOI	Fully Depleted Silicon On Insulator
PAE	Power Added Efficiency
DUT	Device Under Test
PDK	Process Design Kit
NF	Noise Figure
SNR	Signal to Noise Ratio
SPST	Single Pole Single Throw
SPDT	Single Pole Double Throw
DPDT	Double Pole Double Throw
IL	Insertion Loss

Introduction

1.1 Motivation

With the increasing demand for sophisticated services and the proliferation of connected devices, current wireless communication systems must improve to fulfill customers' expectations for quality of service, throughput, latency, connection, and security. 5G and 6G are expected to transform wireless communication networks, providing continuous connectivity and satisfying worldwide demand for accessible wireless connections. This fast shift will redefine the communication environment by bringing more sophisticated and advanced services and devices, as well as new technologies capable of operating at extremely high frequencies and wide bandwidths. FR3 ranges from 7 GHz to 24 GHz, nestled between the FR1 (Sub-6GHz) and FR2 (over 24 GHz) bands utilized in 5G. This upper mid-band frequency region has tremendous potential for 5G and 6G applications. FR3 combines the advantages of both lower and higher bands: it has broader bandwidths for high-speed data transmission, unlike FR1, and superior propagation qualities for urban areas, unlike FR2.

Matching networks are critical for enhancing performance in modern high-frequency and high-bandwidth communication systems because they offer efficient power transfer while maintaining signal integrity among antennas, transmitters, and receivers. When building wideband matching networks for Integrated Circuits (ICs), several complex difficulties must be addressed. This includes managing the sizing of passive components, accounting for parasitics from the layout, limiting signal distortion, and maintaining a constant impedance across a wide frequency range. To ensure consistent performance, designs must account for production disparities.

The motivation for this research arises from the need to overcome these challenges and develop robust wideband matching networks that ensure optimal performance of transmitter and receiver amplifier paths in the FR3 band. This study aims to contribute to the advancement of high-frequency communication technologies, thereby supporting the development of next-generation wireless systems.

1.2   Background Knowledge

1.2.1   Transceivers

An RF transceiver is a device that can transmit and receive radio frequency signals, enabling wireless communication. It integrates both a transmitter and a receiver into a single unit. A basic RF transceiver block diagram is shown in figure 1.1.
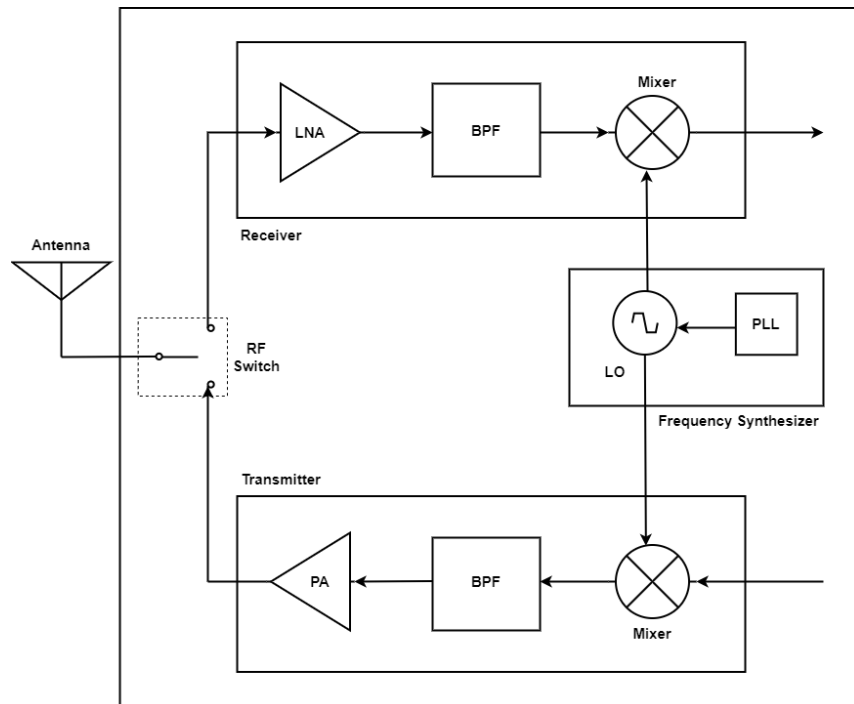
Figure 1.1: Transceiver Block Diagram.

The receiver module begins by capturing a RF signal from the antenna, routed via an RF switch to the receiver [1]. This weak signal is amplified by a LNA, which enhances its strength while minimizing noise. The amplified RF signal is down-converted to Intermediate Frequency (IF) using a mixer that combines it with a frequency from a local oscillator. Down-converted signals are essential because, at very high frequencies, active devices like transistors struggle to provide signal amplification. By converting a high frequency signal to a lower IF, signal processing becomes more convenient. Additionally, down-conversion improves frequency selectivity, allowing for more precise filtering and better overall performance. The Local Oscillator (LO) frequency, generated by a frequency synthesizer incorporating a Phase Locked Loop (PLL), ensures synchronized and stable frequencies across the system. The down-converted IF signal undergoes further processing tailored to the receiver's design, such as filtering and amplification. Finally, an Analog to Digital Converter (ADC) converts the processed analog IF signal into a digital format for further digital signal processing or analysis.

In the transmitter end of an RF transceiver, digital data is initially converted into an analog base-band signal by a Digital to Analog Converter (DAC). This analog signal is then modulated to encode the data onto a carrier frequency. The modulated base-band signal is up-converted to a RF signal using a mixer, which shifts it to the desired RF frequency. The RF signal is subsequently amplified by a PA, which increases the signal power to ensure it can be transmitted over long distances with minimal loss. It is then routed to the antenna through an RF switch. Finally, the antenna radiates the amplified RF signal into the air, completing the transmission process and allowing the signal to be received by a corresponding receiver. This sequence ensures that the original digital data is effectively transmitted as an analog RF signal.

1.2.2 Frequency Range 3

FR3, spanning from 7 GHz to 24 GHz, is gaining prominence in the development of 6G technology due to its balanced propagation and bandwidth characteristics, which offer both broad coverage and high data rates. This spectrum strikes a middle ground between the extensive range of sub-6 GHz frequencies and the high-speed capabilities of mmWave bands, making it suitable for diverse applications from urban to rural settings. Its enhanced outdoor-to-indoor coverage improves signal penetration in densely populated areas and supports advanced applications [2]. Additionally, FR3 facilitates the deployment of Massive MIMO technology, boosting system performance through larger antenna arrays, and aligns with radar technologies to enable multi-functional systems. The future prospects for FR3 include effective spectrum management and regulatory frameworks to prevent interference, as well as advances in signal processing and antenna design. Overall, FR3's distinct characteristics make it an important component in the advancement of 6G, driving innovations and enhancing wireless communication capabilities.
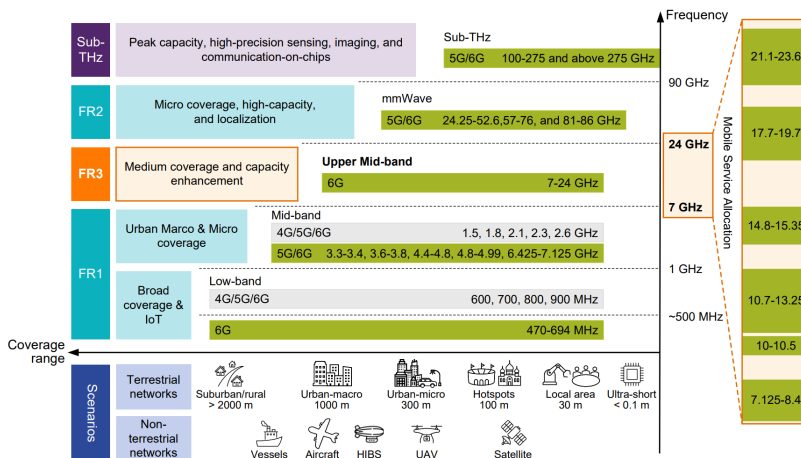
Figure 1.2: Overview of Frequency Spectrum [2].

1.2.3   Matching Network

Impedance matching is a fundamental design requirement in RF circuits, crucial for ensuring efficient power transfer. The circuit illustrated in figure 1.3 features incident and reflected waves. The reflected waves are due to the fact that they are not completely absorbed by the load due to impedance mismatch.
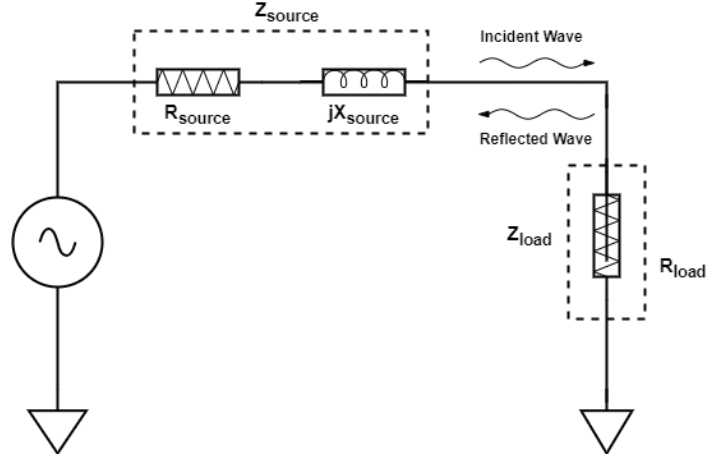
Figure 1.3: Time Varying Signal Source Terminated with a Load.

Reflection coefficient is defined as the ratio of amplitude of the reflected wave to that of the incident wave. Mathematically, it is expressed as:

$$\Gamma = \frac{Z_{load} - Z_o}{Z_{load} + Z_o}$$

where Z_o is the characteristic impedance of the transmission medium. When the reflection coefficient is zero ($\Gamma = 0$), there are no reflected waves, ensuring maximum power transfer. This is achieved when the load impedance (Z_{load}) is equal to the complex conjugate of the source impedance Z_{source}.

$$Z_{load} = Z_{source}^*$$

For purely resistive impedances, the equation simplifies to

$$R_{load} = R_{source}$$

Assuming that $R_{source} = R_{load}$ in figure 1.3, maximum power transfer can be achieved by adding a matching component $-jX_{match}$, where $jX_{source} = -jX_{match}$. This is depicted in figure 1.4. The additional circuitry used to maximize power transfer and minimize reflections is known as a matching network.
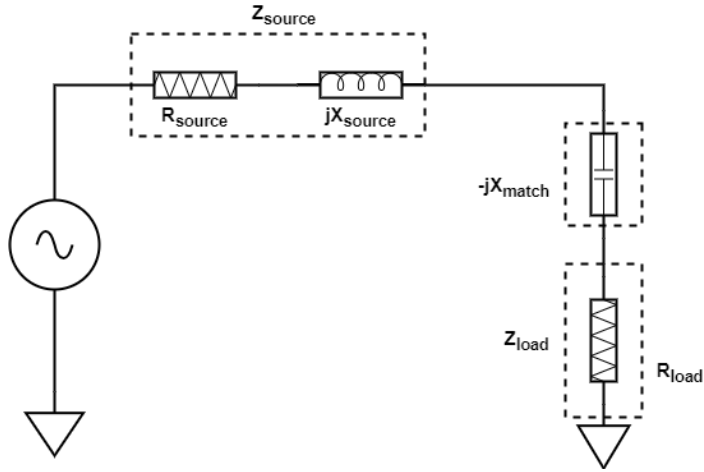
Figure 1.4: Impedance Transformation by Adding a Complex Conjugate Component.

Impedance matching is crucial in various stages of RF systems, such as between the antenna and the PA output, between the PA and the Band Pass Filter (BPF) on the transmitter side, and between the antenna and the LNA input, between the LNA output and the BPF on the receiver side. This matching reduces losses due to impedance mismatches and enhances overall system performance.

In power amplifiers, the focus of impedance matching is on maximizing the output power for the given load. This approach ensures that active devices, like transistors, operate at their full capacity. Techniques like load-line matching and load-pull are commonly used in these applications. Load-pull simulations involve plotting power contours on a Smith chart for various loads in tools like Cadence Virtuoso or Keysight ADS, allowing engineers to select the optimal load impedance to maximize the PA's power output and performance.

Conversely, in receivers, impedance matching adheres to the maximum power transfer theorem due to the need to handle weak and attenuated signals that have traveled long distances. Any mismatch at the antenna or receiver front-end can significantly degrade signal quality by causing reflections and reducing received signal strength. Conjugate matching is a key technique used to enhance overall system performance as it is also used in inter-stage matching in transmitter and receivers.

1.2.4 Bandwidth and Quality Factor

Quality factor Q, represents the ratio of energy stored in a network to the average power dissipated per unit time[4]. Mathematically, it is defined as:

$$Q = 2\pi \cdot \frac{maximum\ instantaneous\ energy\ stored\ in\ the\ network}{energy\ dissipated\ per\ cycle}$$

For a parallel RLC tank, the quality factor is,

$$Q = \frac{R_p}{\omega_0 L_p} = \frac{R_p}{\sqrt{L_p/C_p}}$$

where ω_0 is the resonant frequency of the tank.

The 3dB bandwidth, or half-power bandwidth, is the frequency range over which the power of the signal drops to half of its peak value. For a parallel RLC tank circuit, the 3dB bandwidth is given by [4],

$$B_{3dB} = 2\pi f = \frac{1}{RC}$$

The fractional bandwidth, which is the 3dB bandwidth normalized to the resonant frequency, is simply the inverse of the quality factor [4].

$$\frac{B_{3dB}}{\omega_0} = \frac{1}{R\omega_0 C} = \frac{1}{Q}$$

From this relationship, we can infer that for a given resonant frequency, higher Q results in a narrower bandwidth, while a lower Q leads to a wider bandwidth. Therefore, when designing matching networks, it is crucial to minimize the quality factor to achieve a broader bandwidth.

1.2.5   1-dB Compression Point and Third Order Intercept Point

Linearity in RF systems is a critical characteristic that ensures the output signal of a component is directly proportional to its input. This feature is especially important in components such as LNAs, PAs, mixers and switches, which are integral to both transmitters and receivers. Non-linearity in these systems leads to signal degradation and distortion, which is especially problematic in semiconductor components like Metal Oxide Semiconductor Field Effect Transistor (MOSFET)s, known for their inherent non-linear behaviour under high power levels or in saturation [5]. This issue becomes more pronounced with multi-tone signals, causing inter-modulation distortion. Balancing linearity and efficiency poses a significant challenge, as MOSFETs are most efficient near their saturation region but also exhibit increased non-linearity. Key performance metrics used to assess the linearity of RF systems and their components include the 1dB compression point, the Second Order Intercept Point (IP2) and the IP3.

In a plot of input power versus output power, the 1-dB compression point is where the output power falls by 1dB in comparison to the ideal linear output curve [4]. This is shown in figure 1.5. This deviation marks the beginning of non-linear operation, indicating that the amplifier or RF component is starting to saturate and cannot maintain a proportional increase in output power with respect to the input power. Hence, higher the value of 1dB compression point, higher is the linearity of the device.

As illustrated in figure 1.5, the IP3 is where the extrapolated lines of the fundamental signal and the third-order inter-modulation products intersect. This intersection represents the theoretical input power level at which the power of
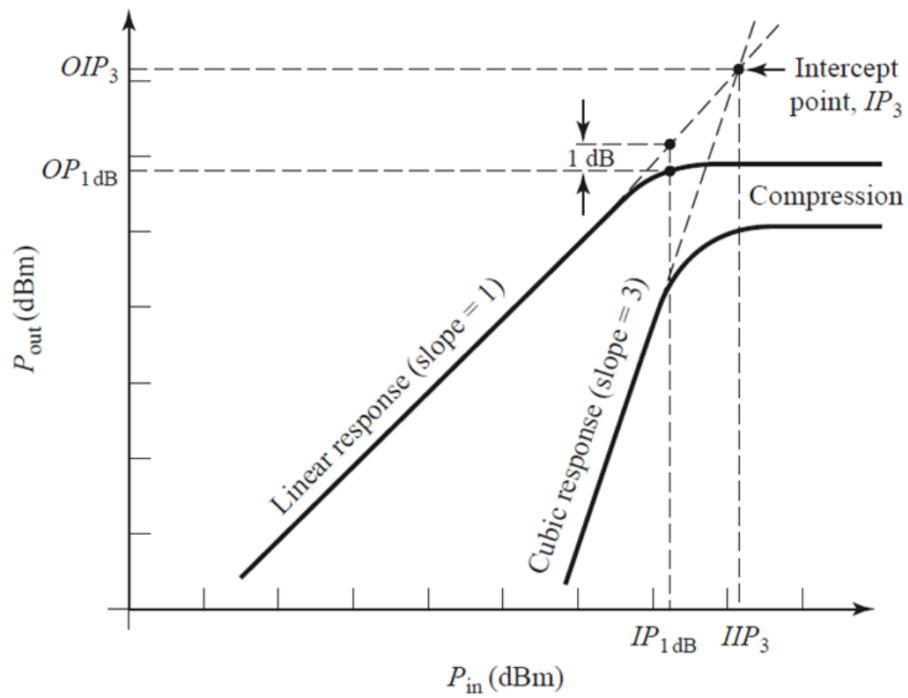
Figure 1.5: Plot illustrating the 1-dB compression point and IP3.

the third order distortion products equals the power of the fundamental signals. Since, third-order products are the closest to the fundamental signal in terms of frequency, the IP3 indicates the point beyond which inter-modulation distortion starts to significantly affect the signal [4]. Therefore, a higher IP3 value reflects better linearity.

1.3   Technology

This thesis is designed using 22nm FDSOI technology, which offers significant advantages in low power logic and RF/mmWave performance, owing to its unique architectural features. This technology is characterized by its low operating voltage range (0.4V - 0.8V) and enhanced electrostatic control, resulting in a steep sub-threshold slope [6]. FDSOI transistors provide high transconductance and self-gain, which are crucial for analog and RF applications. With a reduced parasitic capacitance to the substrate, the technology ensures high cutoff frequencies and maximum oscillation frequencies. The metal stacks within the technology are optimized to support dense digital designs and mmWave circuits, with simulations demonstrating lower insertion loss and higher power saturation.

Wideband Output Matching Network for Power Amplifier

This chapter provides the foundation for designing output matching networks for power amplifiers, providing an in-depth look at fundamental concepts and performance metrics such as output power, gain and efficiency. We explore different matching techniques and gain an understanding of how loadline matching is utilized in power amplifiers. Additionally, we delve into transformer-coupled matching and its effectiveness in achieving wideband matching. The discussion then shifts to circuit design and simulations, highlighting the transformation of theoretical concepts into practical designs. We conclude with an exploration of layout and post-layout simulations, focusing on the challenges of implementing designs into physical layouts and verifying their performance.

2.1 Power Amplifier Fundamentals

Power amplifiers are engineered to amplify the power of an input signal, while ensuring that the output signal maintains the original waveform without distortion. They are critical in designs where maximizing output power and efficiency is of prime importance. The upcoming subsections will detail the key performance metrics of power amplifiers.

2.1.1 Output Power

In the circuit shown in figure 2.1, for an input sinusoidal signal at a fundamental frequency, the instantaneous output power $P_{out,inst}$ is given by,

$$P_{out,inst} = v_{out}(t) \times i_{out}(t)$$

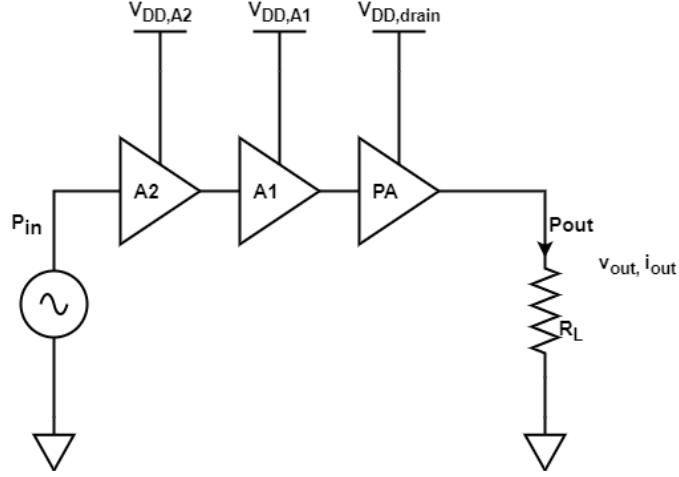The average power $P_{out,av}$ is calculated as,

$$P_{out,av} = \lim_{x \to \infty} \frac{1}{T} \int_{-T/2}^{T/2} P_{out,inst}(t) \, dt$$

Hence, the output power P_{out} is,

$$P_{out} = \frac{V_{out,max}^2}{2R_L} = \frac{V_{out,rms}^2}{R_L}$$

where $V_{out,max}$ is the sinusoidal voltage at fundamental frequency and $V_{out,rms}$ is the corresponding RMS value.

Figure 2.1: PA with two driver stages (A_1 and A_2) connected to an antenna represented by its load [7].

2.1.2 Power Gain

Power gain is described as the ratio of output power to input power. The gain in dB is expressed as,

$$G_{dB} = 10 \log_{10} \frac{P_{out}}{P_{in}}$$

2.1.3 Power Added Efficiency

Power amplifiers are able to boost an input signal's strength by utilizing additional power from a DC source. There are two primary efficiency metrics for PA : drain efficiency and Power Added Efficiency (PAE). Drain efficiency measures the ratio of output power to the DC power, but overlooks the input power of the amplifier. For a more accurate assessment, PAE is used. It is defined as the ratio of effective power (the difference between output power and the input power) to the DC power.

$$PAE = \frac{P_{out} - P_{in}}{P_{DC,tot}} = \frac{P_{out} - P_{in}}{P_{DC,drain} + P_{DC,A}}$$

The DC power is the total DC power consumed by the chain in figure 2.1, and hence includes the DC power used by the drain of the PA and the combined DC power of all other amplifier stages (driver stages) [7].

2.2   Load-Pull Measurements

The antenna connected to the PA is commonly assumed to present a standard load impedance of 50Ω. However, to optimize the output power of the PA, the antenna's impedance often needs to be transformed to a lower value [7]. This impedance transformation is critical in maximizing the efficiency and power delivery of the PA. To achieve the desire load impedance for the PA, we employ a technique called loadline or load-pull matching.

In load-pull measurements, the load impedance presented to the Device Under Test (DUT) is varied systematically. The PA's performance is recorded for each variation. This data is then used to plot contours of constant output power and power-added efficiency on a Smith chart as shown in figure 2.2.
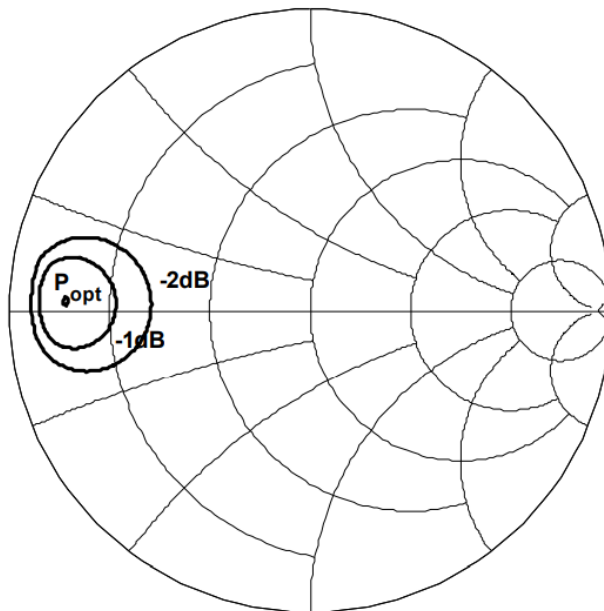

Figure 2.2: Load-pull contour for a PA [7].

Once the desired load impedance is identified from the load-pull measurements, impedance matching networks can be designed and implemented to transform the antenna's impedance to this optimal value.

2.3   Transformers

RF transformers are essential passive electronic components that play a crucial role in converting a given impedance, voltage or current to another desired value. Transformers consist of two magnetically coupled coils as shown in figure 2.3. When an alternating current is applied to the primary winding, it generates a time-varying magnetic flux, which in turn induces a voltage in the secondary winding.
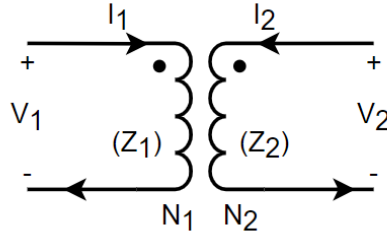
Figure 2.3: Transformer Circuit.

RF transformers are used for

- Impedance matching to ensure maximum power transfer and minimal signal reflections in circuits

- Stepping voltage/current up or down.

- DC isolation between circuits while allowing AC signals to pass through.

- Facilitating the conversion between balanced and unbalanced signals.

- Common mode rejection in balanced architectures.

In figure 2.3, the transformer circuit is depicted with its primary and secondary components. The primary winding has current I_1, voltage V_1, impedance Z_1, and number of turns N_1. Correspondingly, the secondary winding has current I_2, voltage V_2, impedance Z_2, and number of turns N_2.

The turns ratio (n) of the transformer is defined as the ratio of the number of turns in the secondary coil to the number of turns in the primary coil.

$$n = \frac{N_2}{N_1}$$

The relationship between voltage, current and impedance between the primary and secondary winding of the transformer is given by the following equations,

$$V_2 = \frac{N_2}{N_1}V_1$$

$$V_2 = nV_1$$

$$I_1 = \frac{N_2}{N_1} I_2$$

$$I_2 = \frac{I_1}{n}$$

$$Z_2 = n^2 Z_1$$

The mutual inductance M of the transformer shown in figure 2.4 can be calculated as [8]:

$$M = k\sqrt{L_1 L_2}$$

where L_1 and L_2 are the inductances of the primary and secondary windings, respectively, and k is the coupling coefficient. Coupling coefficient is a measure of how effectively the magnetic flux from one winding couples with the secondary winding. The value of k ranges from 0 to 1. If $k = 0$, there is no magnetic coupling between the two coils and if $k = 1$, the two coils are perfectly coupled.

The relationship between the turns ratio and the primary and secondary inductances of a transformer is given by
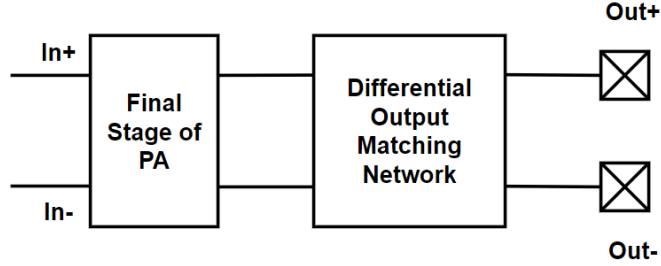
$$n = \sqrt{\frac{L_2}{L_1}}$$
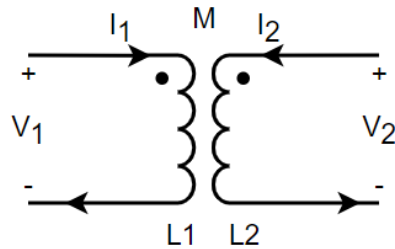
Figure 2.4: Self Inductance and Mutual Inductance of a Transformer.

2.4   Design Considerations and Simulation Results

Transformer-coupled matching networks are widely used to design wideband power
amplifiers [9][10]. Figure 2.5 shows the output matching network positioned be-
tween the final stage of a class-AB power amplifier and the antenna.

Figure 2.5: Output Matching Network Between PA and Antenna.
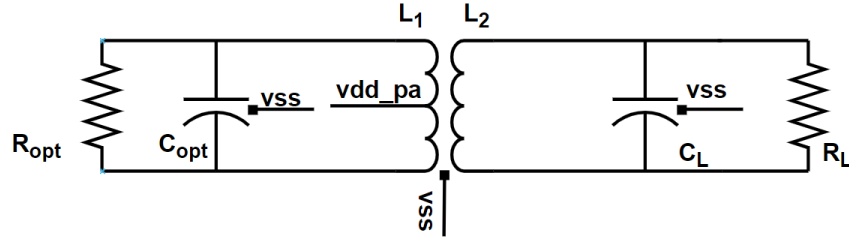
Figure 2.6: Transformer-Coupled Matching Network.

Figure 2.6 illustrates the schematic of the transformer-coupled differential
matching network, designed to transform the output impedance of the final stage
of the PA to the standard 50Ω antenna impedance. The transformer is configured
with a centre tap to provide DC biasing for the PA, ensuring that the transistors
operate within the saturation region.

Through load-pull simulations, the optimal output impedance for the Class-
AB PA was identified as 20Ω, along with a capacitive impedance of 300fF. To
achieve the required impedance transformation, the coupling factor of the Process
Design Kit (PDK) transformer was set to be 0.86. Using standard impedance
transformation formulae, initial values of the primary and secondary inductances of
the transformer were calculated. The load capacitance C_L, which accounts for the
pad capacitance and additional output matching capacitance, was also considered
in these calculations. After determining these initial values, further fine-tuning of
the transformer inductances and capacitances was performed through simulations.
The final values after post-layout simulations of the complete layout are presented
in table 2.1. This refinement ensures better matching between the PA and the
antenna, resulting in efficient power transfer.

The impedance transformation formulae are given bellow[10].

$$\frac{C_{opt}}{C_L} = \frac{R_L}{R_{opt}}$$

$$\frac{L_1}{L_{2'}} = \frac{R_{opt}}{R_L}$$

where L_1 is the primary inductance, $L_{2'}$ and K' are the equivalent secondary inductor and coupling factor, which can be calculated as follows:

$$L_{2'} = L_2 + L_{leak}$$

$$k' = k\sqrt{\frac{L_2}{L_{2'}}}$$

The frequency complex poles can be calculated as:

$$f_L = \frac{1}{2\pi\sqrt{L_{2'}C_L(1-k')}} = \frac{1}{2\pi\sqrt{L_1 C_{opt}(1-k')}}$$

$$f_H = \frac{1}{2\pi\sqrt{L_{2'}C_L(1+k')}} = \frac{1}{2\pi\sqrt{L_1 C_{opt}(1+k')}}$$

Component	Value
k'	0.86
R_{opt}	20Ω
R_L	50Ω
C_{opt}	$300fF$
C_L	$600fF$
L_1	$0.759nH$
$L_{2'}$	$0.797nH$

Table 2.1: Values of Components in the Transformer-Coupled Matching Network.

The S11 parameters, also known as the reflection coefficient, is used to assess the matching quality of the circuit. The S11 parameter is plotted on a Smith chart in figure 2.7, and the reflection coefficient is also plotted in dB versus frequency in figure 2.8. In the Smith chart, good matching is typically indicated when the plot is near the centre of the chart, corresponding to the 50Ω impedance point, which signifies minimal reflection. A common design requirement for acceptable performance is that the S11 value must be below -10dB across the desired frequency range.

For our design, we have achieved an S11 value below -11dB over the frequency range from 9GHz to 21GHz. This result indicates good matching within the FR3 band for the circuit schematic designed with PDK components.
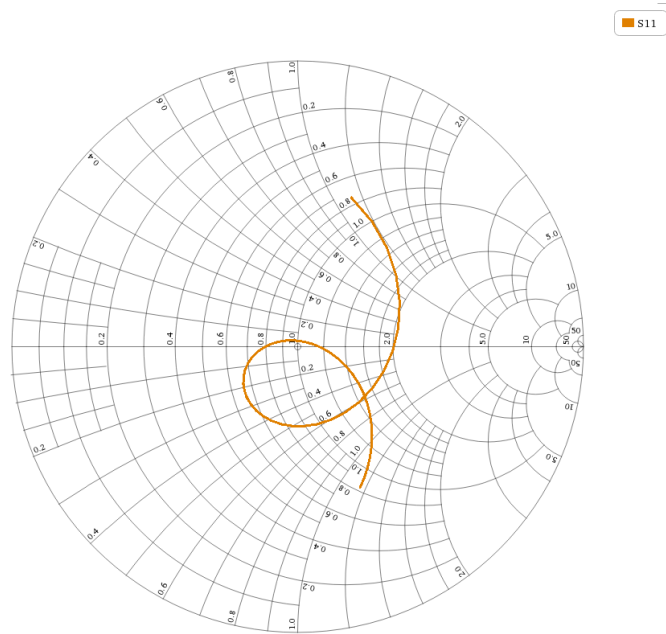
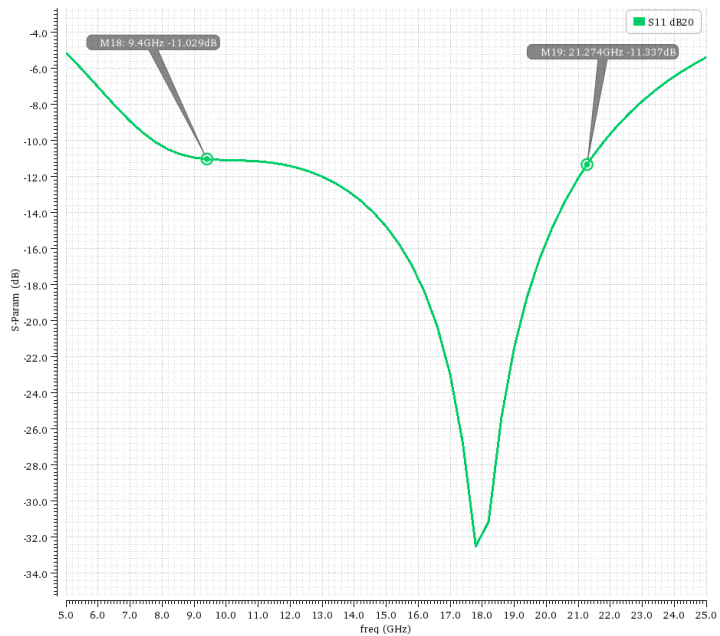**Figure 2.7:** Smith Chart Plot of the S11 Parameter.

**Figure 2.8:** Plot of S11 Parameter in dB versus Frequency.

2.5   Layout

A stacked balun was used for the transformer due to its area efficiency. The stacked design allows for primary and secondary windings to be placed on different metal layers, reducing the horizontal footprint on the chip. The transformer was designed with an inner diameter of 70μm, a turn width of 6.5μm, and a turn spacing of 2.6μm, with both the primary and secondary windings comprising two turns each. To realize the required capacitances of 300fF and 600fF, a 1.8V alternative polarity MOM capacitor was employed. The layout is shown in figure 2.9
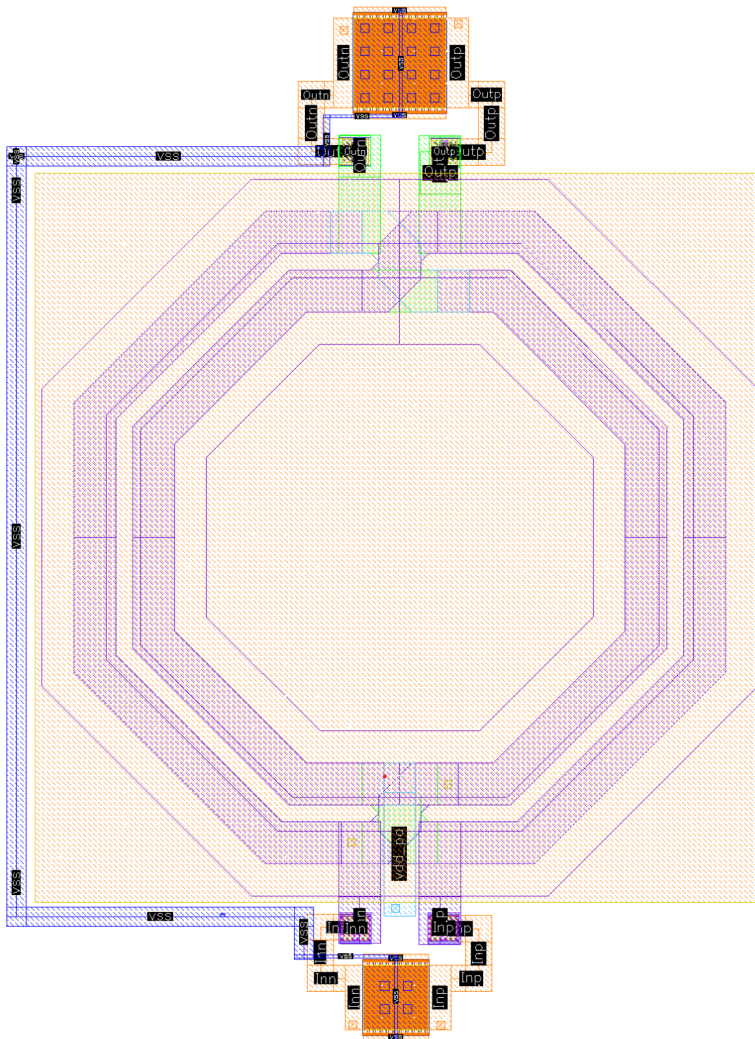
**Figure 2.9:** Layout of the Transformer-Coupled Matching Network.

To evaluate the performance of the design with the layout, parasitic extraction (PEX) using Quantus and electromagnetic simulations using EMX in Cadence were carried out. PEX was used to identify and model parasitics introduced by the physical layout, such as resistances, capacitances, and inductances that can affect circuit performance. On the other hand, EMX simulations were conducted to capture the electromagnetic effects of the nets and the devices, particularly at high frequencies.

The parasitic extraction and EM simulations revealed that the matching performance was not satisfactory. To create a more comprehensive and realistic model, RF pads were introduced into the design, as detailed in subsection 2.5.1. Further simulations were performed to account for the effects of the RF pads and address the observed impedance mismatch in the circuit. This process led to the design and integration of 35pH inductive nets at 14GHz at the differential input end of the matching network as shown in figure 2.10, enhancing both matching and overall circuit performance.
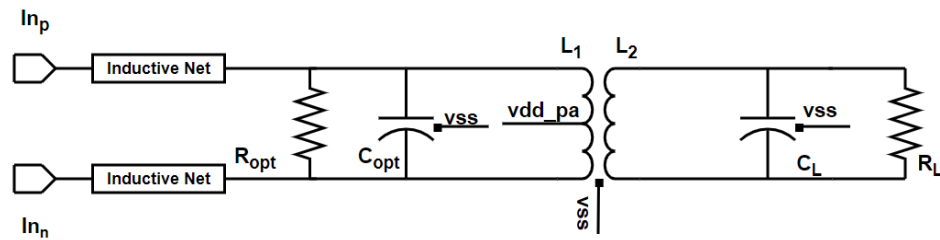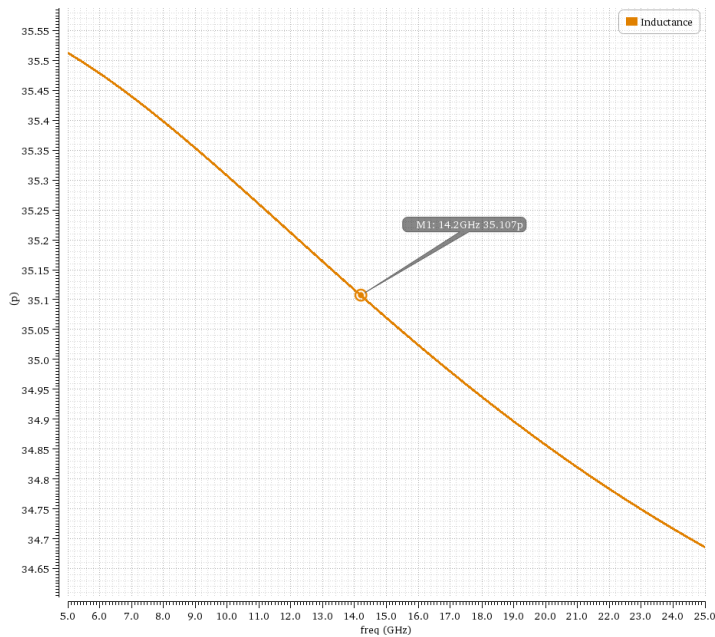

Figure 2.10: Final Schematic of the Transformer-Coupled Matching Network

The layout of the individual net is shown in figure 2.11. EM simulations were performed to assess the inductive net's performance across a range of frequencies. The results, shown in figure 2.12, present a plot of inductance versus frequency.
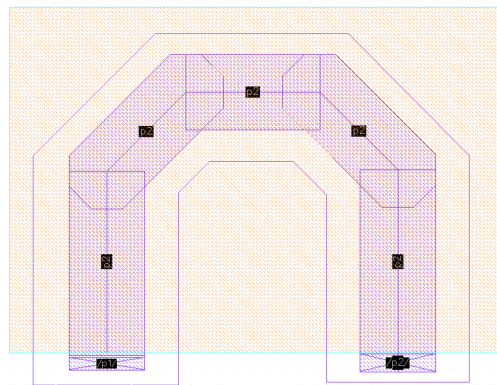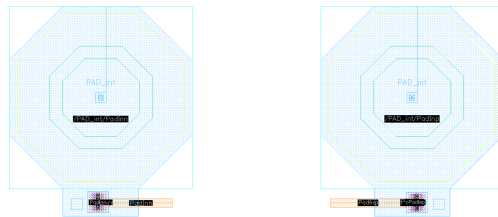

Figure 2.11: Layout of the Inductive Net

Figure 2.12: Plot of Inductance versus Frequency for the Inductive
            Net, as Simulated by EMX

2.5.1 RF Pads

RF pads of the type Bump Pads are utilized in the layout. These RF pads serve
as a critical interface points for connecting the integrated circuit to the external
points in the PCB. They are designed in the LB metal layer and are octagonal in
shape. The layout of the RF pads, including their design and connection nets to
the matching network, is depicted in figure 2.13

Figure 2.13: Layout of RF Pads

The complete layout of the output matching network, including the inductive nets and RF pads, is illustrated in figure 2.14.
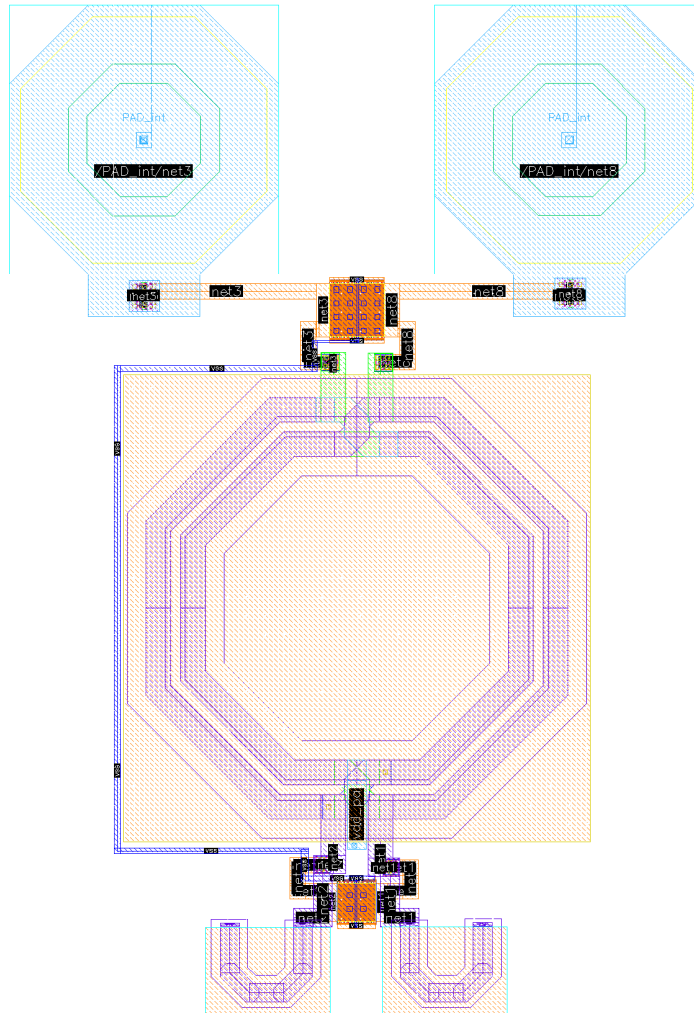
Figure 2.14: Output Matching Network Layout with Inductive Nets and RF Pads

2.6   Post-Layout Simulations

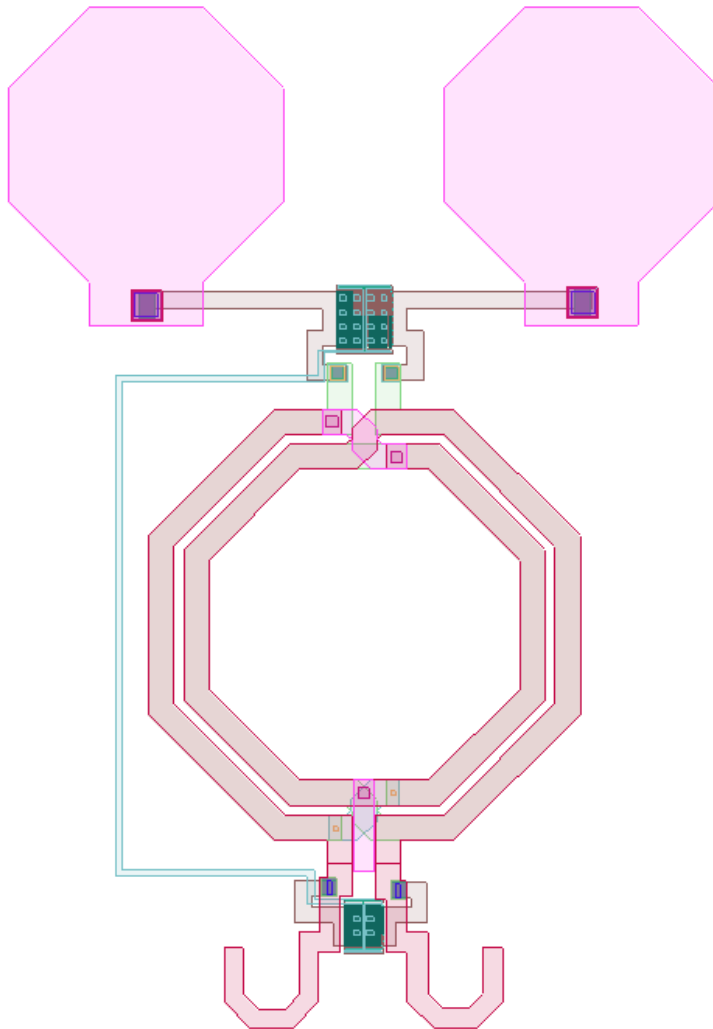The EMX extracted view of the output matching network is depicted in figure 2.15.


Figure 2.15: EMX Extracted View of the Output Matching Network
with Inductive Nets and RF Pads

Figure 2.16 shows the S11 parameters for both the initial schematic and EM simulation results of the complete layout on the Smith chart. Figure 2.17 compares the initial schematic design and EM simulation of the complete layout design for S11 versus frequency. From figure 2.17, we observe improved matching after layout design changes, with the EM simulation results showing good matching between 8 GHz and 24 GHz, with S11 values consistently below the -11 dB threshold.

In terms of performance, the post-layout design achieves a voltage gain of 11.5 dB with the final stage of the PA, closely matching the gain in the schematic design, as shown in figure 2.18. Additionally, figure 2.19 demonstrates that both the schematic and EM simulations achieve an output power of -8.16 dBm for an input power of -20 dBm. The saturated power for the EM simulation is 20.58 dBm, compared to 21.86 dBm in the schematic design.

To evaluate the linearity of the device, the 1dB compression point and third-order inter-modulation points were measured, with the results plotted in figures 2.20 and 2.21, respectively.
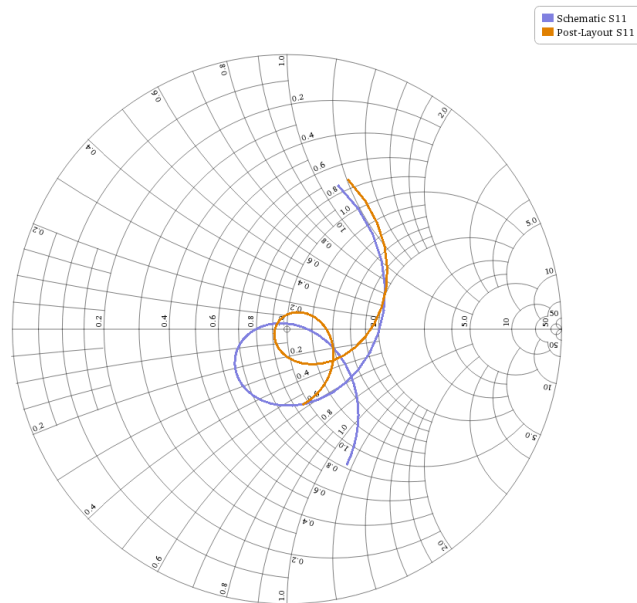
Figure 2.16: S11 Parameter on Smith Chart for Initial Schematic and EM Simulation of Complete Layout
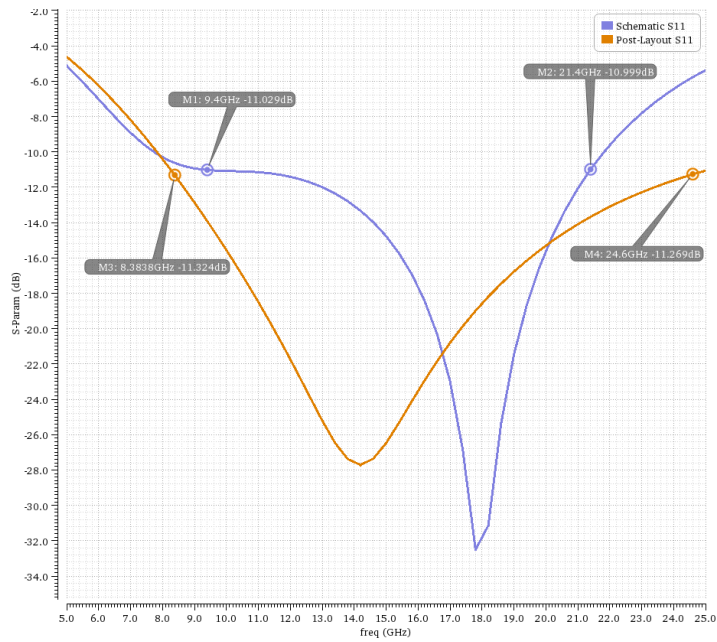
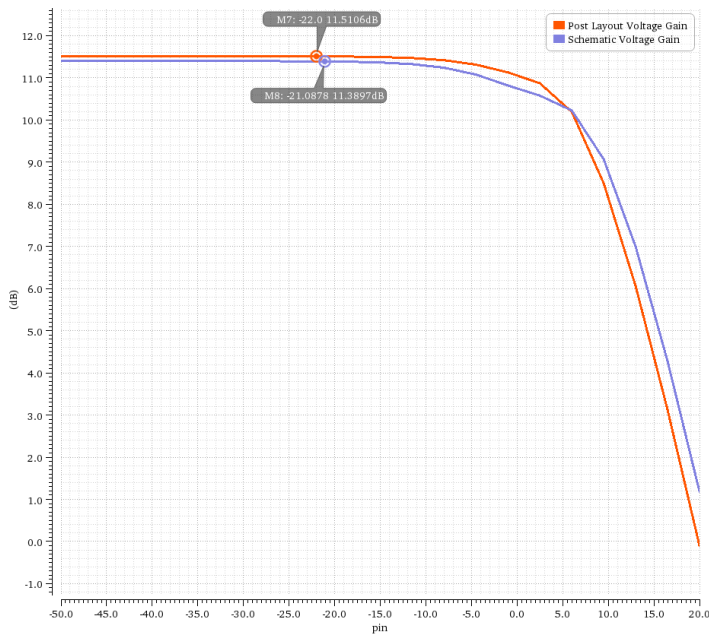**Figure 2.17:** S11 versus Frequency for Initial Schematic and EM Simulations of Complete Layout

Figure 2.18: Gain Plot for Initial Schematic and EM Simulations of Complete Layout
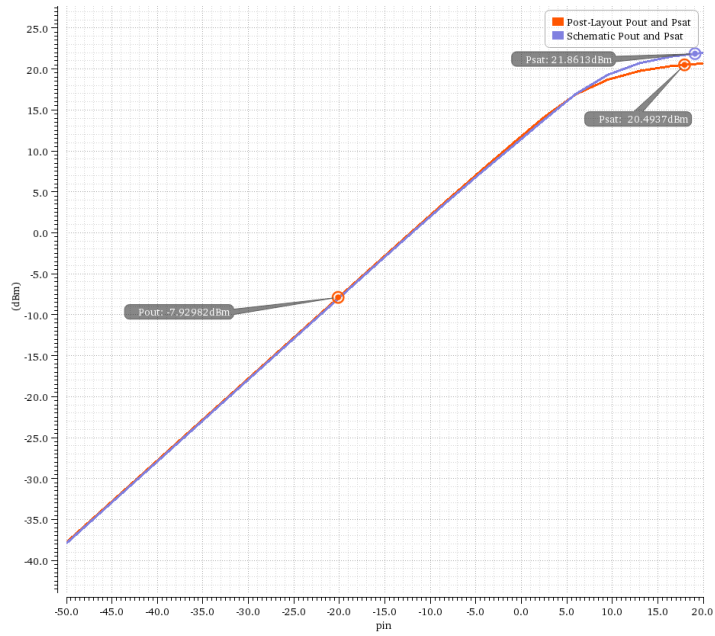
Figure 2.19: Plot for Output Power and Saturated Power
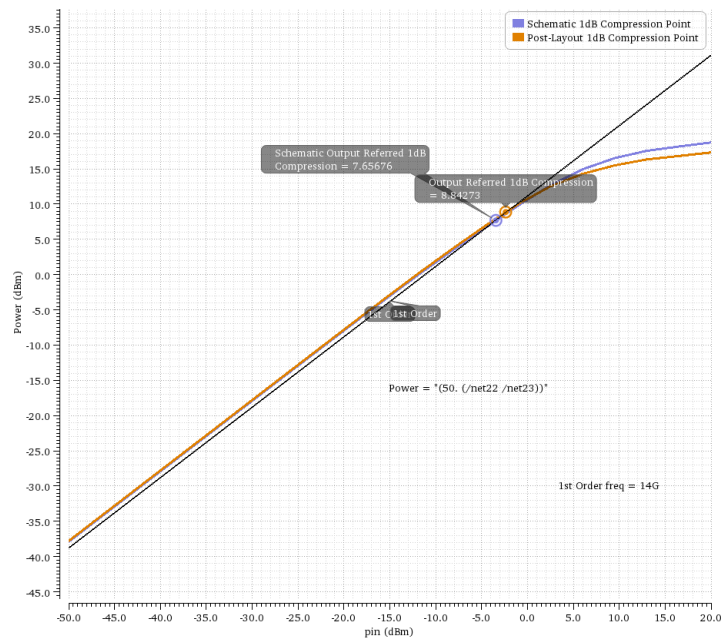
Figure 2.20: 1dB Compression Point
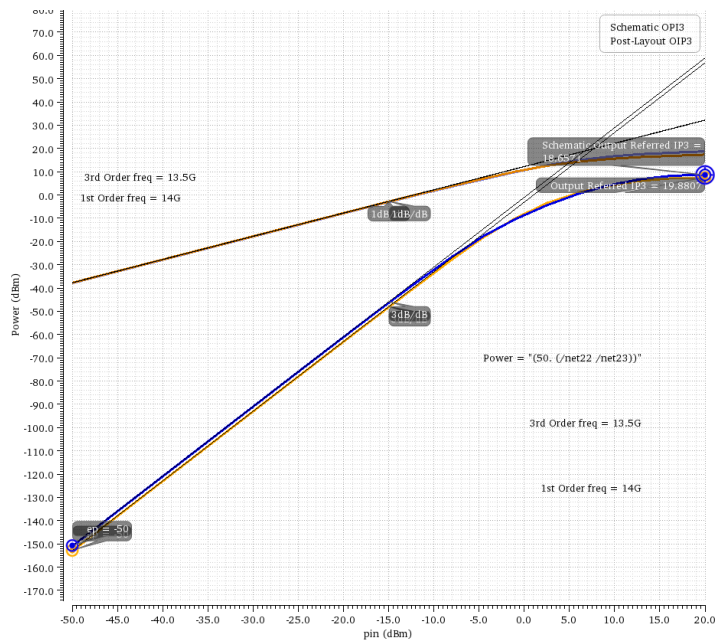
Figure 2.21: Third-Order Intermodulation Point

2.7   Summary

Table 2.2 summarizes the design results, highlighting the comparison between the initial schematic and the final post-layout design. This comparison helps to assess the effectiveness of the design optimizations made during the layout process.

Parameters	Schematic Results	EM Simulation Results
Freq BW (GHz)	9 - 21	8 - 24
Gain (dB)	11.3	11.5
Psat (dBm)	21.86	20.58
P_{1dB} (dBm)	7.656	8.842
OIP3 (dBm)	18.657	19.88
Area (mm^2)	-	0.0244

Table 2.2: Summary of Results

Wideband Input Matching Network for LNA

This chapter begins by explaining the significance of input matching for LNA, emphasizing why proper matching is essential for optimal performance. It then delves into key LNA design concepts such as noise figure, gain, bandwidth, and noise matching techniques. Following this, the chapter explores the use of resistive feedback in common-source amplifiers and their effectiveness in designing wideband input matching networks for LNA. The chapter proceeds to cover design considerations and presents simulation results, concluding with the layout design and post-layout simulation results.

3.1   Fundamental Concepts in LNA Design

The overall performance of a receiver is largely determined by the first stage LNA, making it crucial to design the LNA with low Noise Figure (NF). A low NF is essential because it sets the noise baseline for the entire receiver chain. Any noise introduced by the LNA is amplified by subsequent stages, degrading the Signal to Noise Ratio (SNR) and reducing the receiver's ability to distinguish weak signals from noise. However, achieving a low NF often involves trade-offs, particularly with input matching [11].

Input matching is vital for maximizing power transfer, especially with low-power signals, as in the case of LNA, and for reducing reflections that can degrade performance. Even when no significant impedance transformation is needed, a matching network is necessary due to the frequency dependent nature of the real-world component impedances, such as antennas and LNAs. Moreover, it stabilizes performance by accounting for variations in input impedances due to factors like biasing and temperature, ensuring efficient signal transfer. The upcoming subsections details some of the target specifications of an LNA.

3.1.1   Gain

Gain of a device refers to its ability to amplify the amplitude or power of an input signal. It is typically expressed as the ratio of the output signal to the input signal.

The voltage gain in dB is given by the formula:

$$Voltage\ Gain = 10\log(\frac{\frac{V_{out}^2}{R_{out}}}{\frac{V_{in}^2}{R_{in}}}) = 20\log(\frac{V_{out}}{V_{in}})$$

3.1.2   Noise Performance

The noise performance of a system is characterized by Noise Factor (F). The Noise Factor quantifies how much noise a device adds to the input signal with respect to an ideal noiseless device. It is defined as:

$$F = \frac{Signal\ to\ Noise\ Ratio\ at\ Input}{Signal\ to\ Noise\ Ratio\ at\ Output}$$

The noise factor expressed in decibels(dB) is referred to as Noise Figure (NF), and it is given by the formula:

$$NF = 10\log_{10}(F)$$

The overall Noise Factor of a multi-stage system can be calculated using Frii's Formula. The total noise factor is calculated as:

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 \times G_2} + ...$$

where $F_1.F_2,...$ are the Noise Factors of each stage, and G_1, G_2,... are the gains of each stage.

Another key parameter in assessing noise performance is the SNR, which is the ratio of the signal power to the noise power. It is typically expressed as:

$$SNR = \frac{P_{signal}}{P_{noise}}$$

3.1.3   Centre Frequency and Bandwidth

The centre frequency of an LNA is the specific frequency at which the amplifier is designed to operate most efficiently, typically at the midpoint of its intended frequency range. Bandwidth refers to the range of frequencies over which the LNA maintains acceptable performance, including gain, noise figure and impedance matching.

3.2   Noise Matching Techniques

Designing LNA involves balancing NF, gain, linearity, impedance matching, and power dissipation, with a common goal of achieving simultaneous noise and input matching at a given power level. The classical Noise Matching (CNM) technique focuses on minimizing NF by matching the input to the optimum noise impedance, often leading to gain mismatches [12]. The Simultaneous Noise and Input Matching (SNIM) technique uses feedback, to achieve both noise and gain matching.

Power Constrained Noise Optimization (PCNO) adjusts transistor size and source inductance to minimize the NF, but this results in a higher NF than the minimum possible. Finally, the Power-Constrained Simultaneous Noise and Input Matching (PCSNIM) technique introduces additional matching components to achieve simultaneous matching at low power, though it may increase noise resistance and reduce bandwidth [12].

3.3 Design Considerations

The input matching network is designed to ensure that the 50Ω impedance of the antenna is matched to the 50Ω input impedance of the LNA as shown in figure 3.1.

Our design employs a resistive feedback common-source amplifier to achieve this matching [11]. The feedback network is illustrated in figure 3.2. The choice of a resistive feedback common-source amplifier is beneficial because it improves gain and bandwidth while mitigating the impact of subsequent stages on the overall noise figure of the LNA [11]. Figure 3.3 presents the small-signal circuit of the input matching network. The passive balun in the circuit, represented by R_L and C_L, is used for biasing the MOSFET in the input matching network and the subsequent LNA stage, ensuring proper operation in the desired saturation region. Additionally, considering the Miller Effect, the gate-drain parasitic capacitance C_{gd} of the MOSFET can be approximated as $A \cdot C_{gd}$ at the gate, where A is the voltage gain between the MOSFET's gate and drain. The input impedance $Z_{in-core}$ is expressed as [11]:

$$Z_{in\_core} = \frac{Z_{temp}}{g_m + sC_{gs} + \left(\frac{Z_{temp}}{R_f} - g_m\right) \cdot \frac{R_f}{R_{f+} + R_L // C_L}}$$
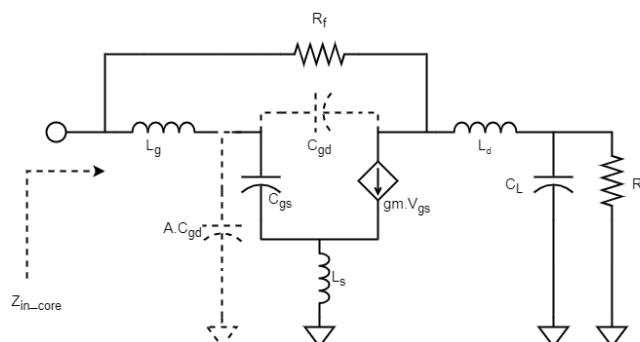
$$Z_{temp} = [sL_s(g_m + sC_{gs}) + 1] \times (1 + s^2 \cdot AC_{gd} \cdot L_g) + s^2 \cdot C_{gs} \cdot L_g$$
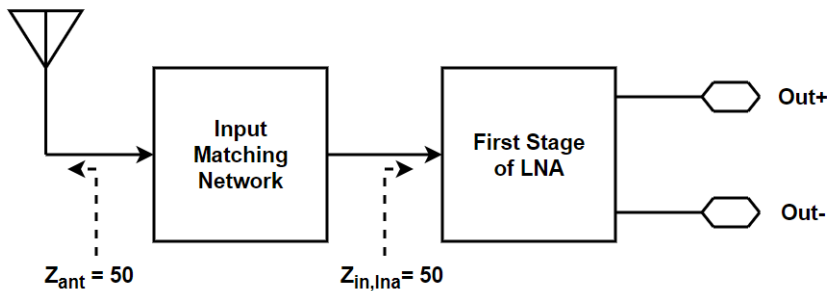
Figure 3.1: Input Matching Network Between Antenna and LNA
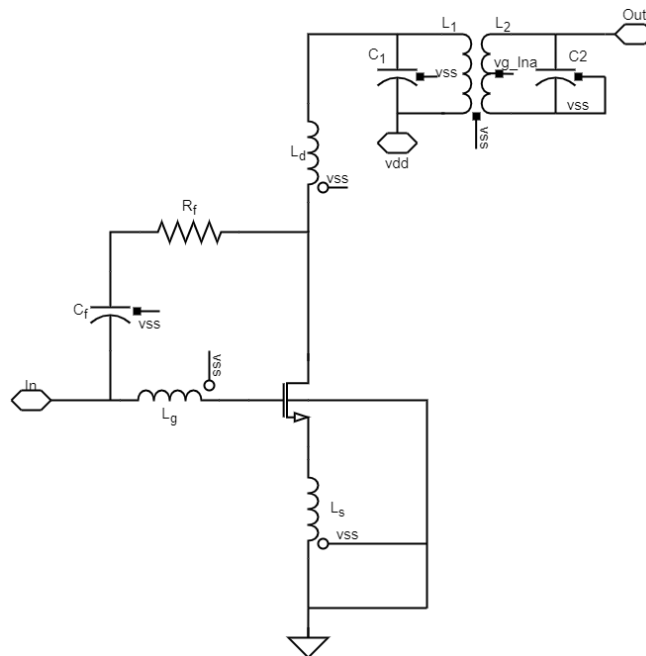
Figure 3.2: Schematic of the Resistive Feedback Common-Source Amplifier

Figure 3.3: Small Signal Circuit of the Input Matching Network

At low operating frequencies, the input impedance $Z_{in-core}$ is primarily influenced by the feedback resistor R_f and the MOSFET's transconductance g_m. It is crucial to note that the NF decreases as transconductance increases. Therefore, when designing R_f and g_m to meet the 50Ω input matching requirement, these considerations are essential. The MOSFET was designed with a width of 7μm and a length of 20nm, resulting in a transconductance of 178mS. Accordingly, the feedback resistance was calculated to be 445.25Ω. At higher frequencies, parasitic capacitance effects become more significant. To address this and achieve high-frequency input matching, inductors L_g, L_d and L_s are introduced into the design. Inductors L_g and L_d provide inductive peaking, while L_s provides resonance with capacitance C_{gs}. The values for L_d, L_g and L_s are 310pH, 400pH and 170pH, respectively. The passive balun is designed for operation at 14GHz with a coupling coefficient of 0.88, featuring primary and secondary inductances of 804pH and 851pH, respectively. Additionally, the capacitors C_1 and C_2 are set at 103.9fF and 398.2fF. These values were achieved after post-layout simulations and recurring fine tuning of the components to achieve wideband matching with good performance in terms of gain and noise figure. The component values are documented in table 3.1.

Component	Value
g_m	178mS
R_f	445.25Ω
C_f	99fF
L_g	400pH
L_d	310pH
L_s	170pH
L_1	804pH
L_2	851pH
k	0.88
C_1	103.9fF
C_2	398.2fF

**Table 3.1:** Component Values for the Input Matching Network

3.4   Simulation Results

The results of the matching network, represented by the S_{11} parameters, are plotted on the Smith chart in figure 3.4. Figure 3.5 shows the S_{11} values versus frequency, demonstrating that good matching is achieved from 10GHz to 19GHz, where the S_{11} values are below -11dB threshold.

The gain for the design, including the first stage of the LNA, is plotted in figure 3.6, where it reaches 21.66 dB at 15 GHz. The noise figure of the design with the first stage of LNA was simulated and found to be 2.103 dB, indicating a low noise performance, as depicted in figure 3.7 and 3.8.
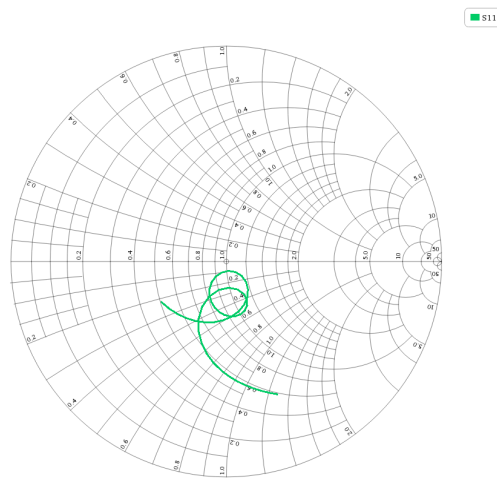
Figure 3.4: Smith Chart of S_{11} Parameters for the Input Matching Network
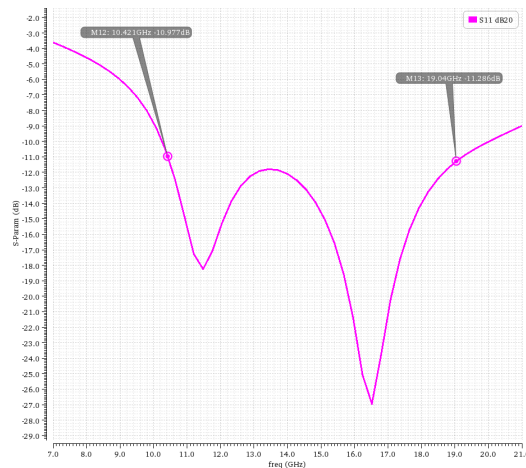
Figure 3.5: S_{11} versus Frequency for the Input Matching Network
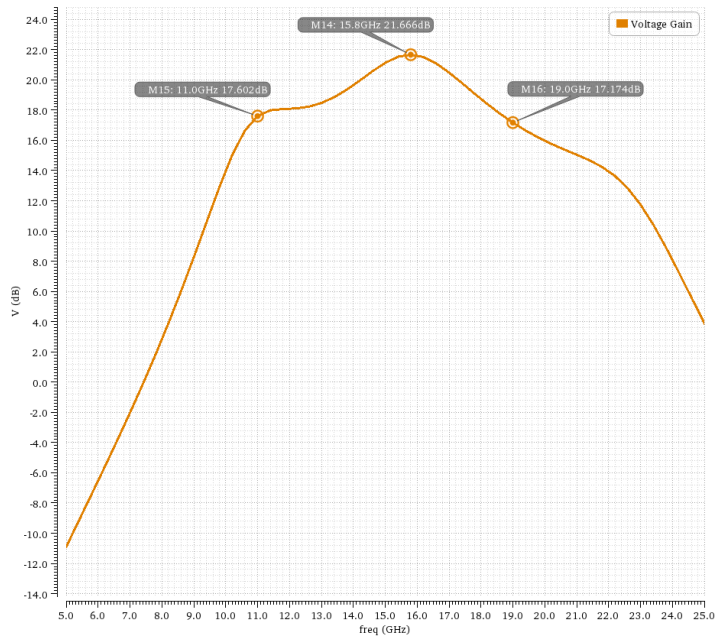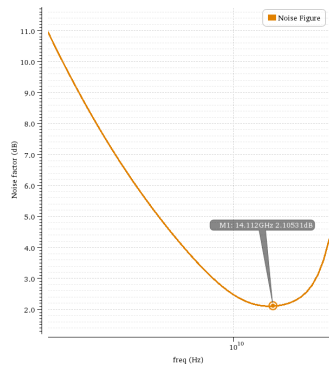
Figure 3.6: Gain plot
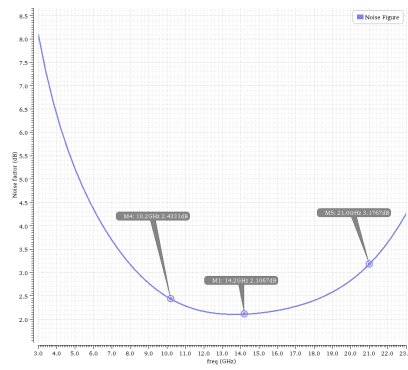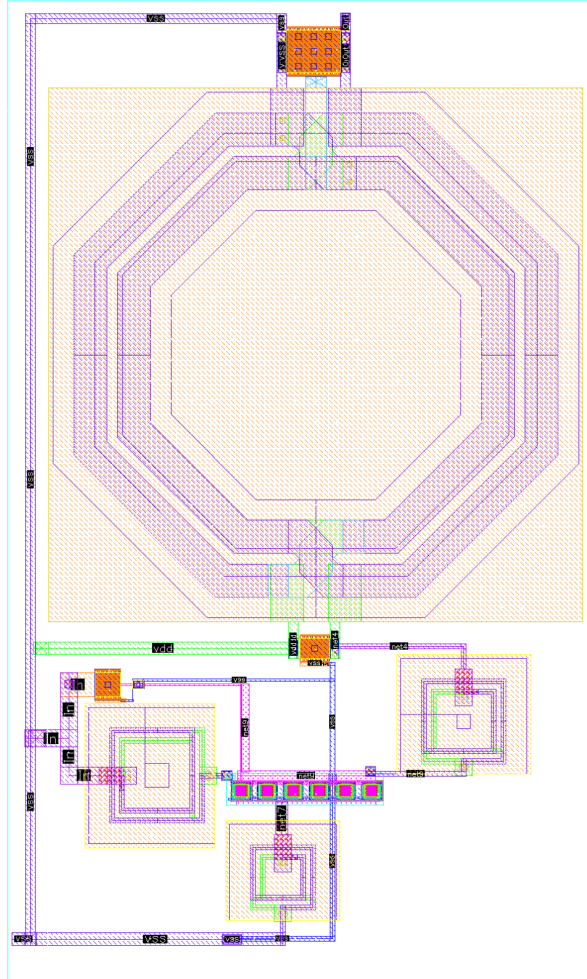

Figure 3.7: Noise Figure Plot

Figure 3.8: Zoomed-In View of the Noise Figure Plot

3.5   Layout

Figure 3.9: Layout of the Input Matching Network

The layout of the input matching network is shown in figure 3.9. The design incorporates a Super-Low Threshold Voltage FET (SLVT-NFET) with a flip-well configuration, featuring a total width of 7μm, a length of 20 nm, and 10 gate fingers. For the inductors, vertically oriented peaking inductors were used, with the first, second, and third spirals placed in the QB, QA, and JA layers. The feedback resistor is implemented using an N+OP SOI diffusion resistor. Additionally, the design includes an RF stacked balun with an 80μm inner diameter and an 8μm turn width. Capacitors C_1, C_2 and C_f were designed using 1.8V alternative polarity MOM capacitors.

3.6   Post-Layout Simulations

The EMX extracted view of the input matching network is depicted in figure 3.10.
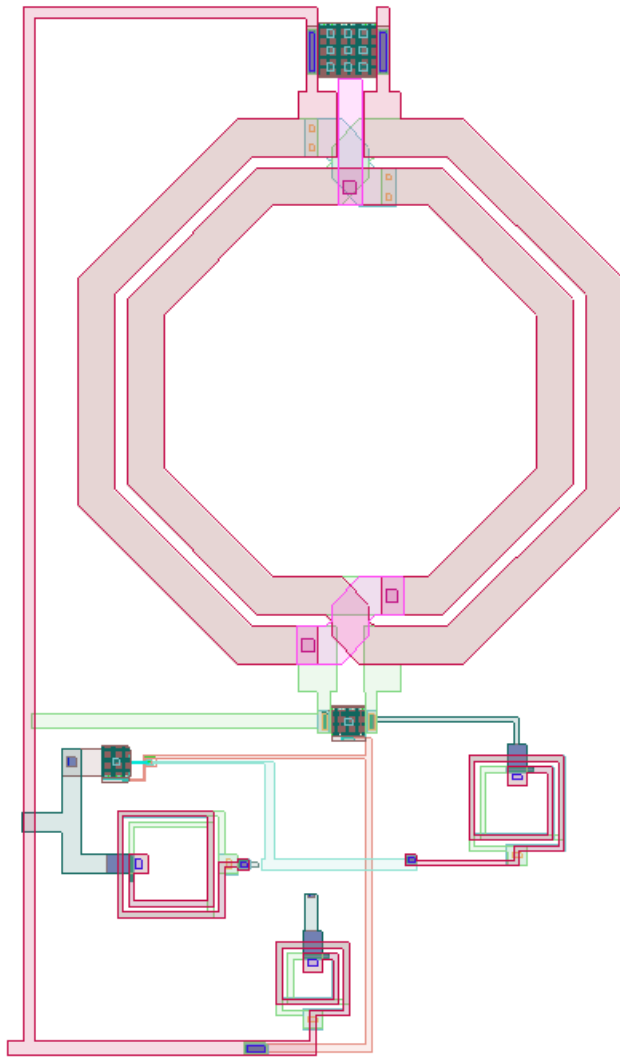

Figure 3.10: EMX Extracted View of the Input Matching Network

The S_{11} parameters, comparing the matching achieved after EM simulation of the final layout with the initial schematic design, are plotted on the Smith chart in figure 3.11. Additionally, the S_{11} parameters versus frequency are shown in figure 3.12. From figure 3.12, it is observed that good matching is achieved between 8GHz and 24GHz, with S_{11} value remaining below -11dB across this frequency range. Furthermore, figure 3.12 demonstrates that optimizing the layout design has improved the matching bandwidth.
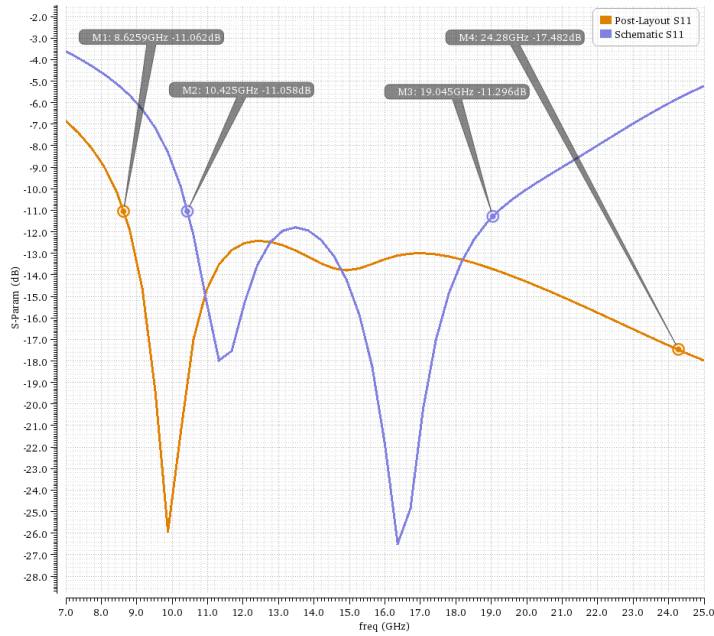
The noise figure plot for the initial schematic and EM simulations of the final layout is shown in figure 3.13. It is observed that the noise figure in the post-layout simulation has increased by 0.8dB compared to the schematic design. The post-layout design achieves a NF of 2.9dB at 14GHz, which meets the design specifications.

Figure 3.14 presents the voltage gain plot for both the initial schematic and EM simulation of the final layout design. The maximum gain in the EM simulation is 19.85 dB at 15 GHz, compared to 21.6 dB in the schematic design. The EM simulation gain plot shows that the design achieves a bandwidth from 10 GHz to 20 GHz.

To assess the linearity of the design, post-layout simulations were conducted for both the 1 dB compression point and third-order intermodulation distortion. The results are illustrated in figures 3.15 and 3.16, respectively. The output 1 dB compression point was measured at -3.17 dBm, while the IIP3 was found to be -9.646 dBm.
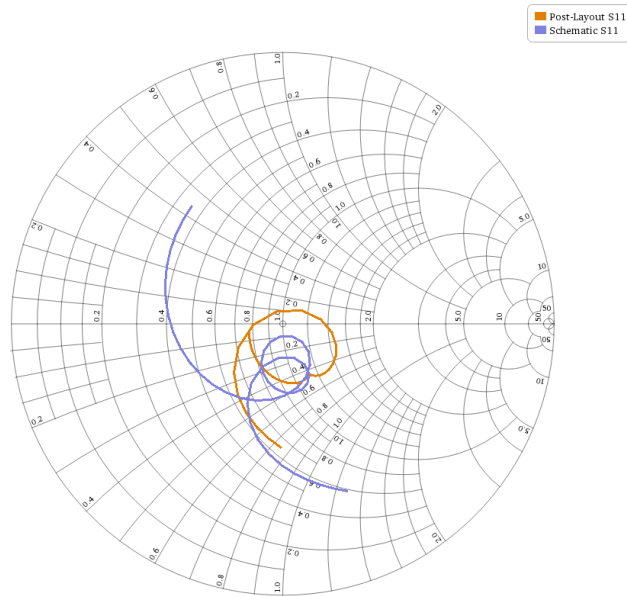
Figure 3.11: S11 Parameter on Smith Chart for Initial Schematic and EM Simulation of the Final Layout

Figure 3.12: S_{11} Parameters versus Frequency, Comparing the Initial Schematic Design and EM Simulation for the Final Layout
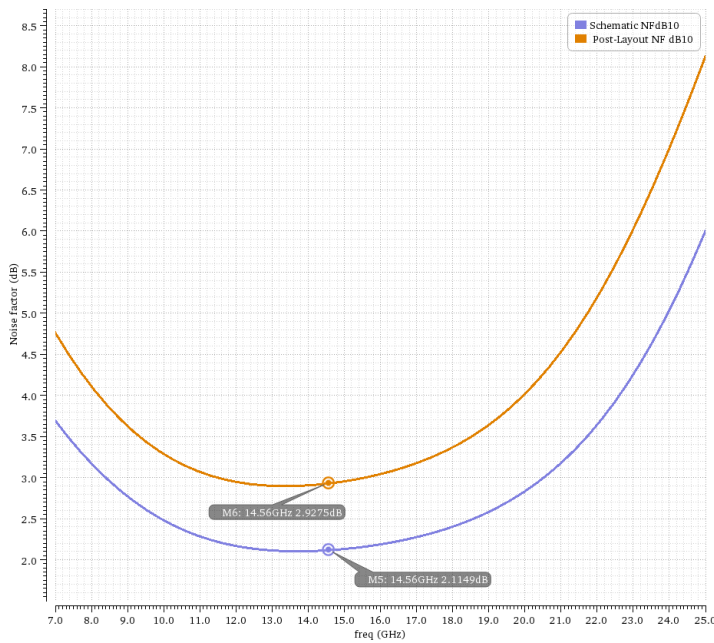
Figure 3.13: Noise Figure Comparison Between Initial Schematic and Final Layout EM Simulation
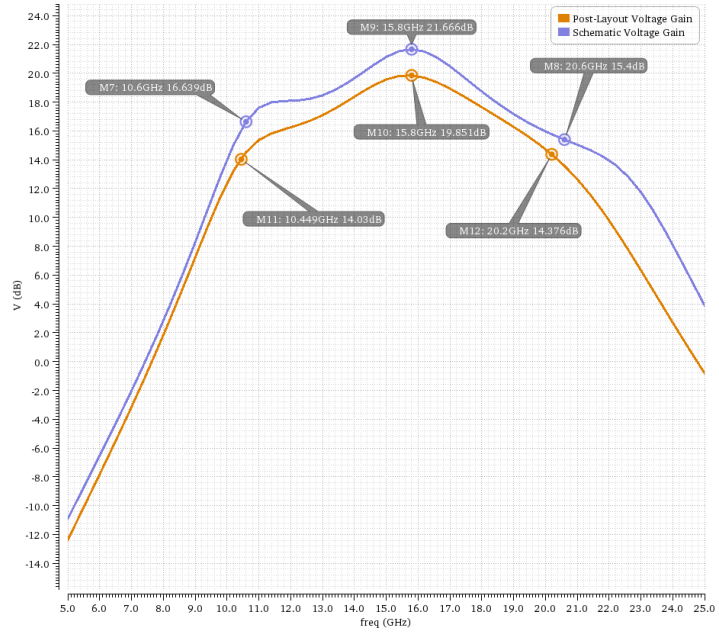
Figure 3.14: Voltage Gain Plot for Initial Schematic and Final Layout EM simulation
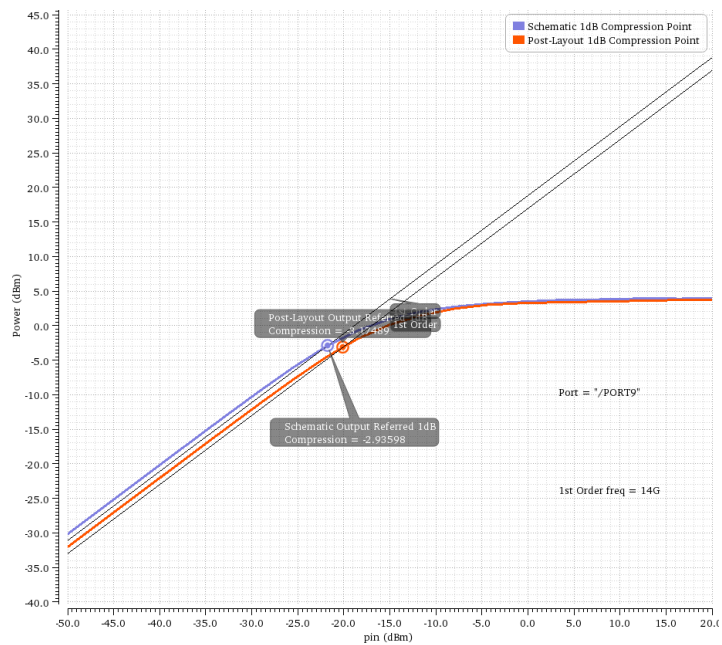
Figure 3.15: 1 dB Compression Point Measurement for the Design.
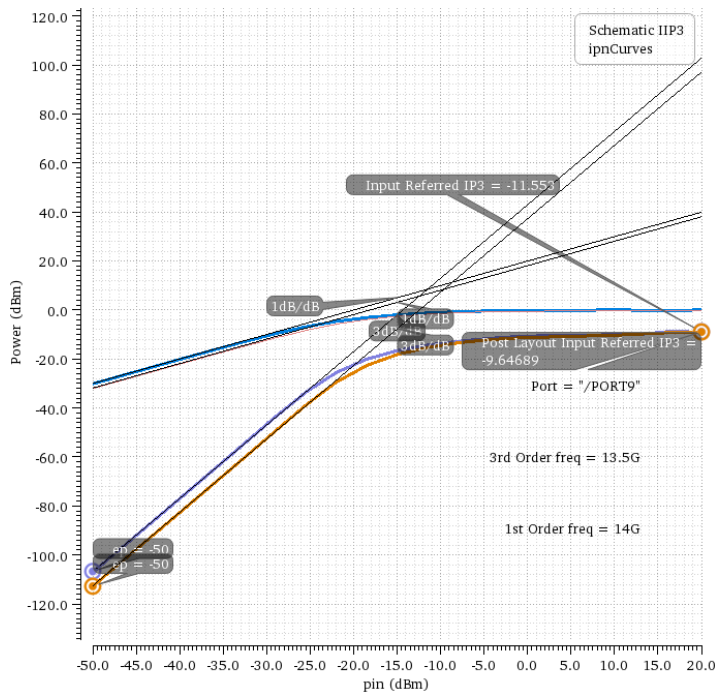
Figure 3.16: Third-Order Intermodulation Point for the Design

3.7   Summary

Table 3.2 presents a summary of the design's key performance metrics, offering a clear snapshot of how the design meets its performance objectives.

Parameters	Schematic Results	EM Simulation Results
Freq BW (GHz)	10.6 - 20.6	10 - 20
Gain (dB)	21.66	19.85
NF (dB)	2.114	2.927
OP_{1dB} (dBm)	-2.93	-3.17
IIP3 (dBm)	-11.55	-9.64
Area (mm^2)	-	0.0304

Table 3.2: Summary of Results

Antenna Switch

This chapter begins with an overview of antenna switches, highlighting their significance and the key performance metrics for their design. Following this, the circuit design and simulation results are presented, with a detailed analysis of how back gate bias and matching influence critical metrics such as insertion loss, return loss, and isolation.

4.1 Background Knowledge

RF switches or antenna switches, are devices used to route high-frequency signals to different transmission paths. These switches come in various configurations depending on their application, including Single Pole Single Throw (SPST) for basic on/off control, Single Pole Double Throw (SPDT) for routing between two signal paths, and Double Pole Double Throw (DPDT) for more complex switching scenarios that involve multiple inputs and outputs.

There are two main types of RF switches: electromechanical and electronics. Electromechanical switches rely on mechanical contacts to perform switching. Electronic RF switches, on the other hand, utilize semiconductor devices such as diodes or transistors to achieve fast switching. These switches are faster and more reliable, making them suitable for applications requiring high speed operation. Electronic switches can also offer lower power consumption and better integration with modern electronic systems, particularly in compact and portable devices.

We focus on the design of an electronics switch using MOSFETs in FDSOI technology. The following subsections discuss the key parameters for an antenna switch.

4.1.1 Insertion Loss

Insertion Loss (IL) is a measure of the power loss that a signal experiences as it passes through a switch in its ON state. It is typically expressed as the ratio of the output power to the input power and is given by:

$$Insertion\ Loss\ (dB) = 10\log_{10}\frac{P_{out}}{P_{in}}$$

In terms of s-parameters, IL can also be represented as:

$$Insertion\ Loss = -20\log_{10}|S_{21}|$$

The IL is influenced by the size of the MOSFET as follows [13]:

$$IL = (\frac{R_{on} + 2Z_o}{2Z_o})^2$$

where Z_o is the load impedance and R_{on} is the on-resistance, which is given by [14]:

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})}$$

4.1.2   Return Loss

Return Loss is a measure of how well the switch is impedance matched to the connected port. It is expressed as the ratio of the reflected power to the incident power, indicating how much of the signal is reflected back due to impedance mismatches.It is measured in the ON state of the switch. It is expressed in decibels as:

$$Return\ Loss = 10\log_{10}\frac{P_{reflected}}{P_{in}}$$

Return loss, calculated using the s-parameters is given by:

$$Return\ Loss = -20\log_{10}|S_{11}|$$

4.1.3   Isolation

Isolation measures an RF device's ability to confine signals to their designated paths while minimizing leakage to unintended paths. It is quantified as the power difference between the available input power and the output power when the switch is in the OFF state. It is mathematically expressed as:

$$ISO = 10\log_{10}\frac{P_{out,off}}{P_{in}}$$

As the width of the MOSFET increases, the on-resistance R_{on} decreases, leading to a reduction in insertion loss. However, this increase in width also results in higher parasitic capacitance, which negatively impacts the switch's isolation. Additionally, improving return loss enhances isolation and reduces insertion loss, but this often comes at the expense of increased area due to the additional matching circuit elements. Therefore, it is crucial for designers to strike a balance between insertion loss, isolation, switching speed, return loss, and area when designing an antenna switch.

4.1.4   Switching Time

Switching time refers to the duration it takes for an RF switch to transition between its ON and OFF states, and vice versa.

4.2 Circuit Design and Simulation Results

A SPDT switch with a series-shunt configuration, as depicted in figure 4.1, has been designed. Each series and shunt path incorporate three NMOSFET devices. We utilized an SLVT (super-low threshold voltage) NFET with a flipped-well configuration, which is regarded as the optimal choice for RF switches operating below 20GHz [15]. The shunt FETs have a width of $29.4\mu m$, while the series FETs are $72\mu m$ wide. Additionally, $9.2k\Omega$ bias resistors were used, along with $2.45k\Omega$ resistors placed in parallel with the FETs.
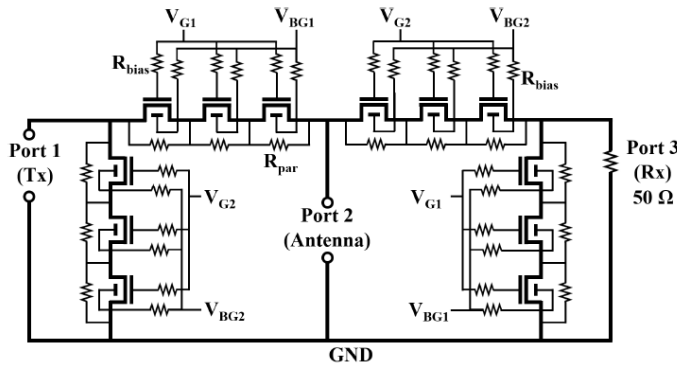

Figure 4.1: Schematic of the Antenna Switch [15]

Bias resistors are placed at the gate and substrate of MOSFETs to minimize oscillations during switching operations. These oscillations arise because the gate capacitance and inductance form an LC circuit, which can oscillate and generate electromagnetic interference (EMI) noise. Additionally, the bias resistance at the gate plays a crucial role in determining the switching time of the MOSFET. A smaller bias resistance results in faster switching times, but it can also cause ringing, leading to increased EMI. On the other hand, a larger bias resistance slows down the switching time, leading to higher switching losses and greater heat dissipation. Therefore, selecting the appropriate bias resistance is essential to balance switching speed, EMI noise, and thermal management in the design.

To transmit the RF signal from the TX port (Port 1) to the Antenna (Port 2), the gate bias voltages are configured such that $V_{g2} < V_{th}$ and $V_{g1} > V_{th}$. This setup allows the RF signal to pass through the series FETs to the antenna, while the shunt FETs remain in the OFF state. Any residual signal or noise present at the RX port (Port 3) is grounded via the shunt FETs and the series FETs on the RX side are also in the OFF state. This configuration effectively isolates the RX port, maintaining good isolation performance in the design.

4.2.1 Stacking FETs

Stacked FETs are crucial in RF switches, especially for high-power applications, as they allow the circuit to handle higher voltages while maintaining optimal performance. In our design, three FETs are stacked to evenly distribute the voltage across the devices, thereby preventing any single FET from reaching its breakdown voltage, which can be influenced by factors such as gate-oxide breakdown, punch-through, hot electron effects, and avalanche breakdown. This configuration enhances the switch's power handling capability, enabling efficient management of high-power RF signals without compromising device integrity.

A key performance factor for these stacked FETs is the voltage swing, which defines the range of voltage variation each FET experiences during operation. Proper management of the voltage swing is critical, as excessive swings can lead to signal distortion or damage.

In our SPDT series-shunt configuration, measurements of the drain-to-source voltage (V_{ds}) for the stacked FETs in the ON state, shown in figure 4.2, reveal that each FET experiences an equal voltage swing for an input power level of -20 dBm. Additionally, the gate-to-source voltage (V_{gs}) distribution, depicted in figure 4.3, remains within the required operating range for all FETs. These results confirm that the voltage is evenly distributed and that each FET operates within optimal parameters, ensuring reliable performance and compliance with design specifications.
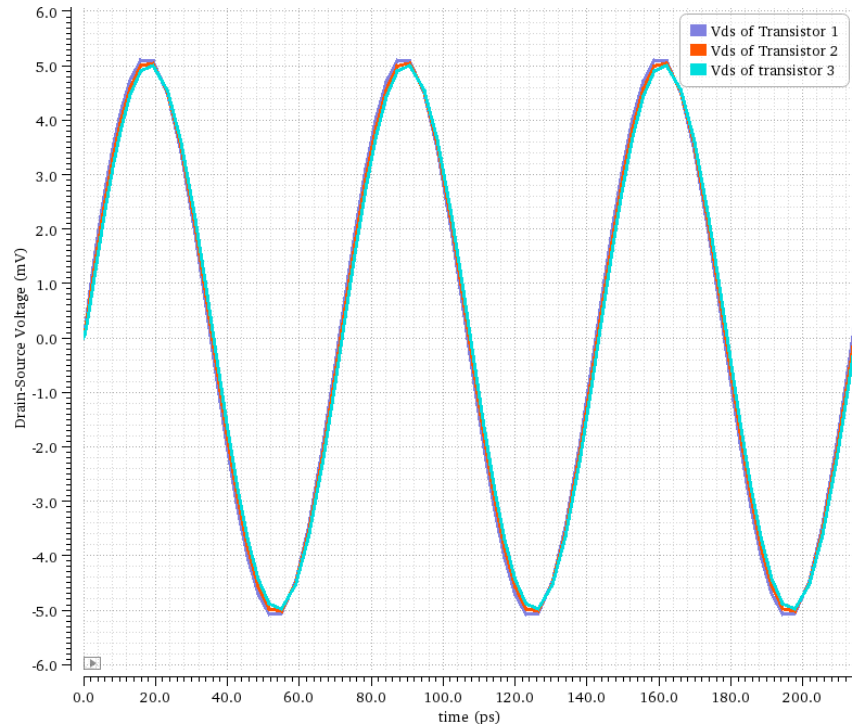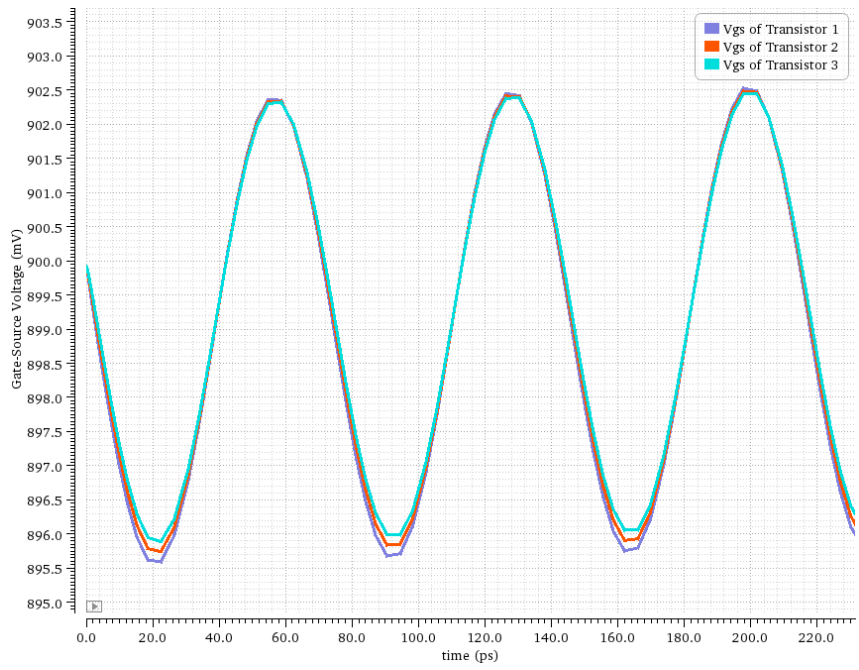

Figure 4.2: Drain-Source Voltage of FETs

Figure 4.3: Gate-Source Voltage of FETs

4.2.2   Transmitter to Antenna Path

To improve matching, a 100pH inductor was added in series to all three ports of the design. This subsection presents the simulation results for the transmitter-to-antenna path. Figure 4.4 compares the return loss for the design with and without matching. Without matching, the return loss stays below the -11dB threshold from DC to 60GHz, while the addition of matching improves the performance, particularly at 30GHz. In figure 4.5, it is shown that matching degrades the insertion loss performance. Figure 4.6 illustrates that matching has minimal impact on isolation, maintaining a value of -37dB at 14GHz. Figure 4.7 provides the 1dB compression point, yielding an OP1dB of 22.94dBm. Lastly, figure 4.8 presents the third-order intermodulation result, with an IIP3 value of 39.7dBm.
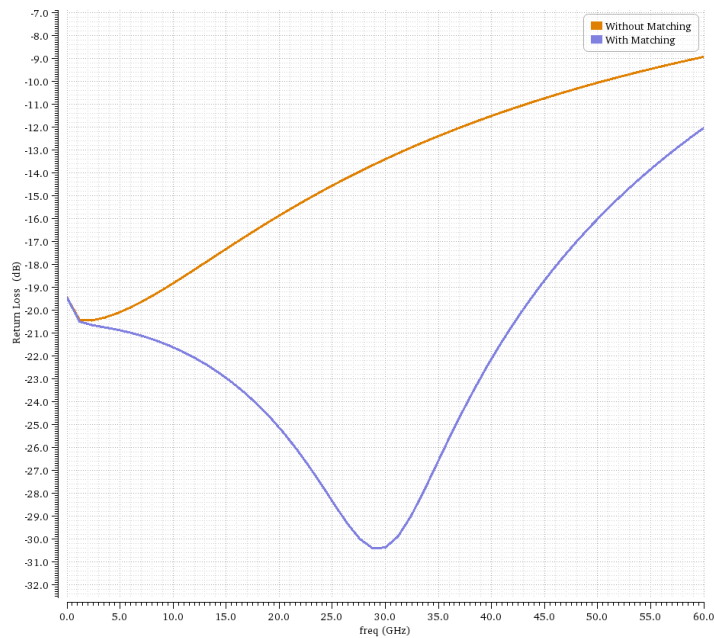

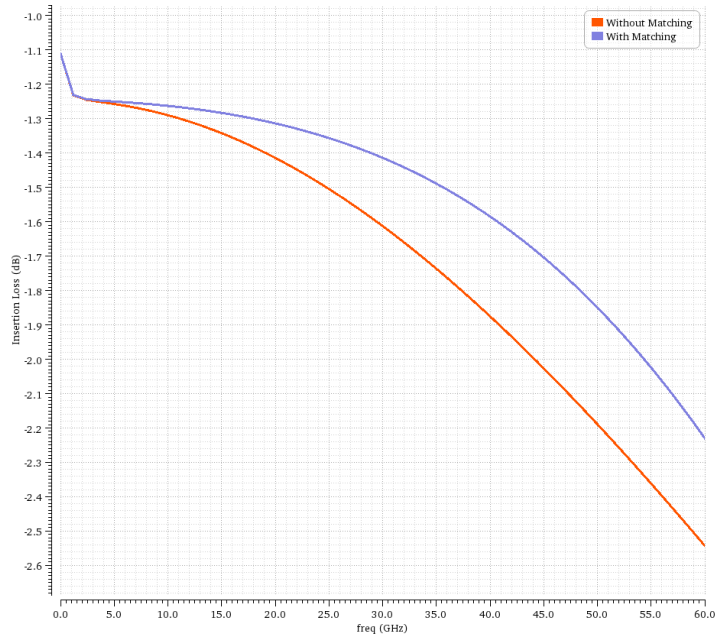**Figure 4.4:** Return Loss for Transmitter to Antenna Path

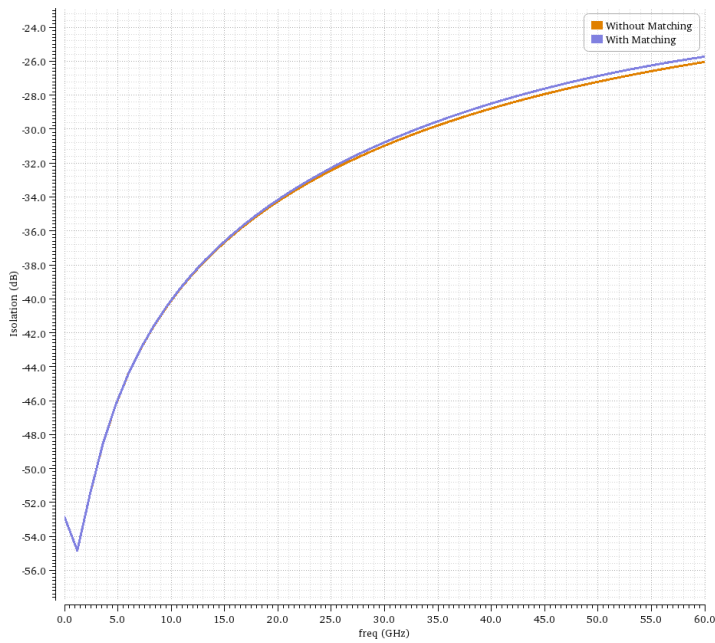**Figure 4.5:** Insertion Loss for Transmitter to Antenna Path

Figure 4.6: Isolation for Transmitter to Antenna Path
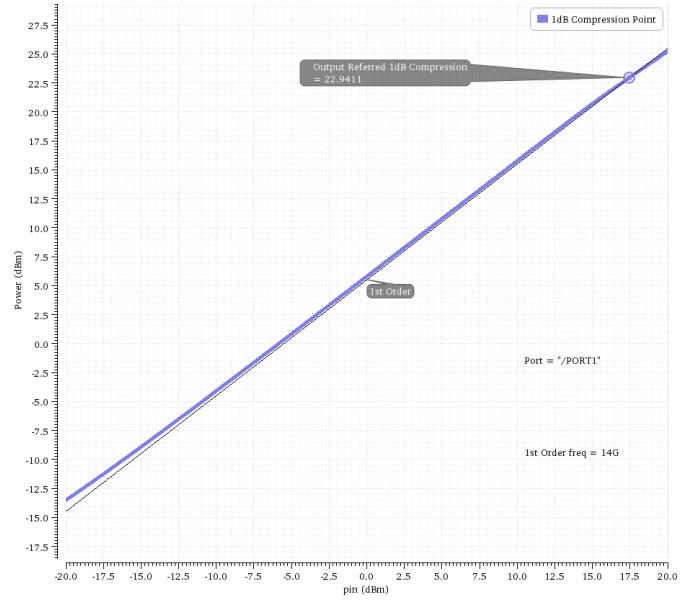
Figure 4.7: 1dB Compression Point of Antenna Switch
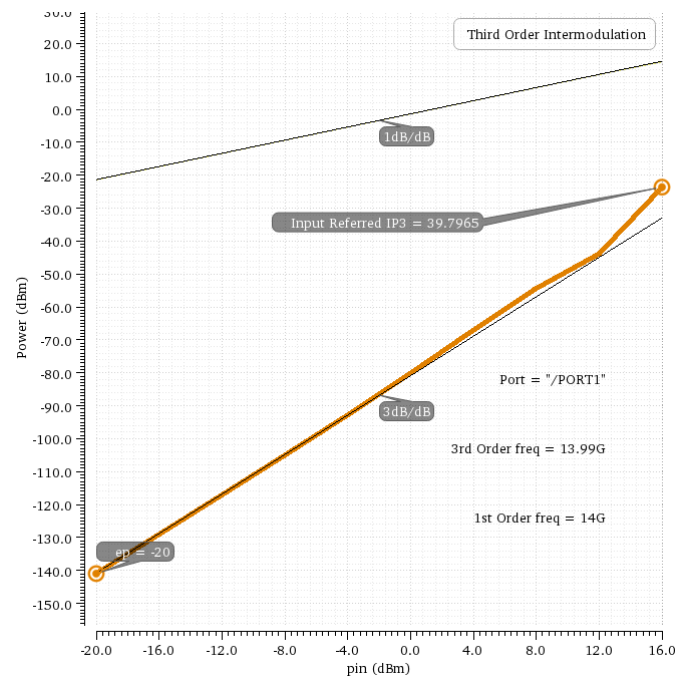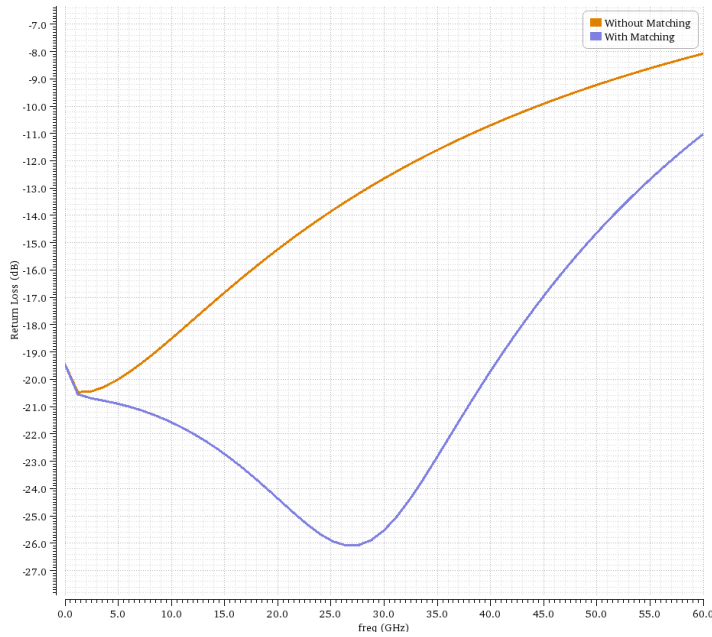

Figure 4.8: Third Order Intermodulation Plot for the Antenna Switch

4.2.3   Antenna to Receiver Path

To evaluate the performance of the antenna switch in the antenna-to-receiver path, simulations were performed, and the results are depicted in figures 4.9, 4.10, and 4.11.

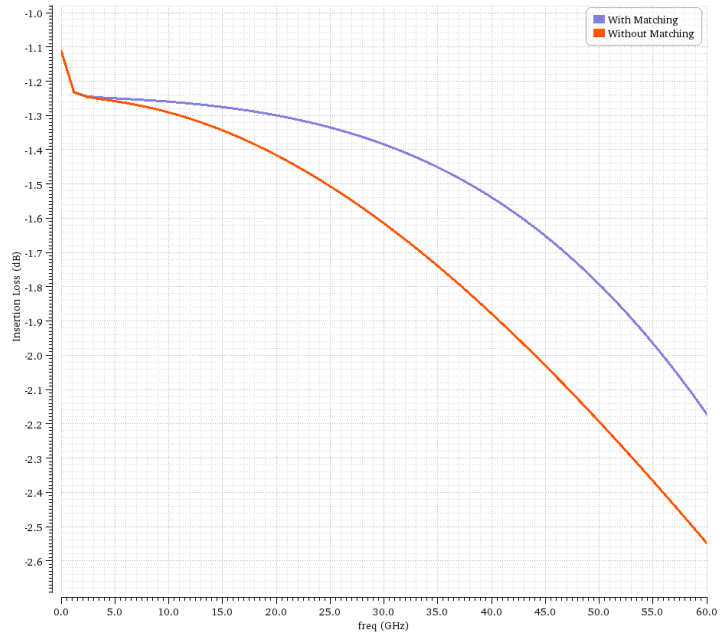**Figure 4.9:** Return Loss for Antenna to Receiver Path

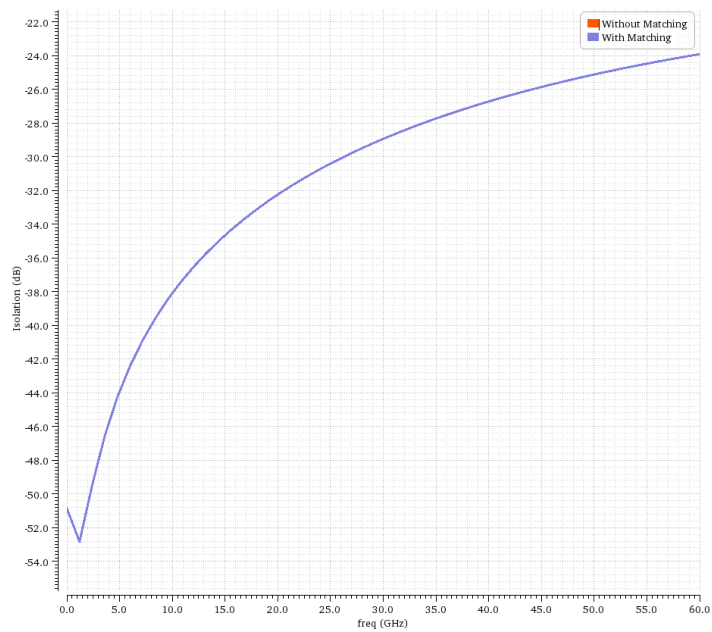**Figure 4.10:** Insertion Loss for Antenna to Receiver Path

Figure 4.11: Isolation for Antenna to Receiver Path
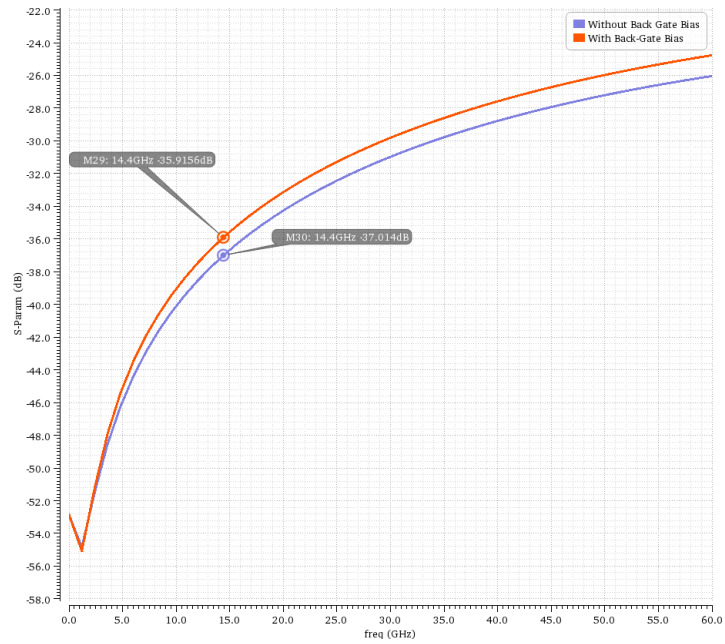
4.2.4   Back-Gate Bias

The SLVT FET devices feature a back gate terminal that allows tuning of the transistor's threshold voltage by applying a DC voltage to the substrate. We analyzed the effect of back gate bias on the isolation and insertion loss of the antenna switch.

In the switch's on state, a bias voltage V_{bg1} is applied to the NFET. When V_{bg1} is applied, the threshold voltage V_{th} increases, leading to a reduction in the FET's on-resistance. This decrease in on-resistance subsequently lowers the insertion loss of the device, as shown in figure 4.12, where an improvement of approximately 0.15dB in insertion loss is observed. V_{bg2} is maintained at zero bias, as it has little impact on insertion loss as the C_{off} elements have no dependency on V_{bg} [15].
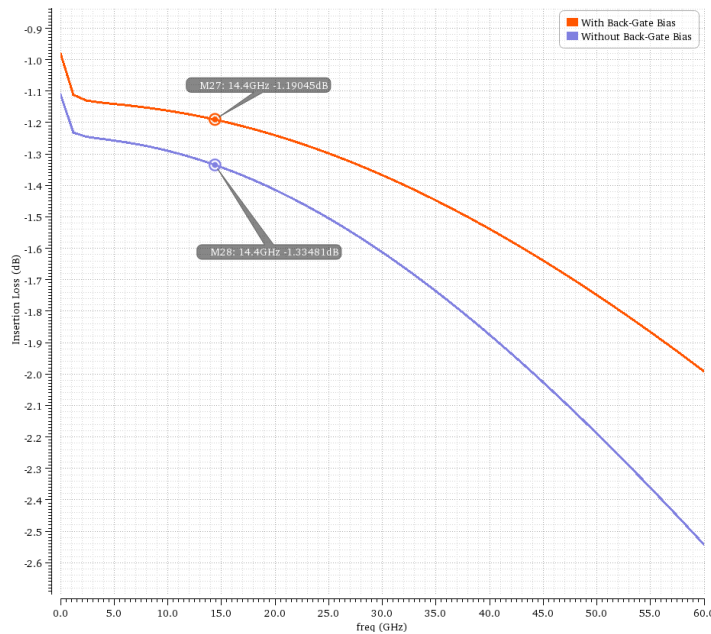
Figure 4.12: Effect of Back Gate Bias on Insertion Loss

Similarly, to analyze the effect of the back gate on the isolation of the chip, V_{bg1} is set to zero bias while V_{bg2} is applied with a DC bias. The isolation is measured when the switch is in the off state. The results, plotted in figure 4.13, show a 2 dB improvement in isolation at 14 GHz.

Figure 4.13: Effect of Back Gate Bias on Isolation

4.3   Summary

Table 4.1 presents a comprehensive summary of the key performance metrics and simulation results for the antenna switch circuit design.

Parameters	Results
Insertion Loss(14GHz) [dB]	1.19
Isolation(14GHz) [dB]	37
P1dB (dBm)	22.94
IIP3 (dBm)	39.7
Switching Time (ns)	0.25

Table 4.1: Summary of Results for Antenna Switch

4.4 Integrating LNA Input Matching Network, PA Output Matching Network, and RF Switch

The designed input matching network, which is paired with the first stage of the LNA, and the output matching network, which interfaces with the last stage of the PA, are combined with the designed antenna switch. This integration is illustrated in figure 4.14.
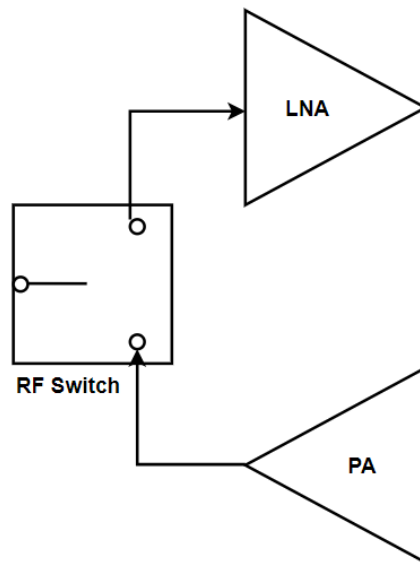
Figure 4.14: Integration of LNA Input Matching Network, PA Output Matching Network, and Antenna Switch

4.4.1 Simulation Results: PA to Antenna Path

The matching performance for the PA to antenna path is illustrated on the Smith chart in figure 4.15 and as a frequency response plot in figure 4.16. These figures show that a good matching is achieved across the frequency range from 8.2 GHz to 23.4 GHz. Figure 4.17 demonstrates that a voltage gain of 10dB is obtained. However, there is a 1.5dB reduction in gain compared to the output matching network design with the PA alone, which can be attributed to the inclusion of the antenna switch. Additionally, figure 4.18 indicates that the system achieves a saturation power of 22.23 dBm. This comprehensive analysis highlights the effectiveness of the matching network integration while also acknowledging the impact of the additional antenna switch on overall gain performance
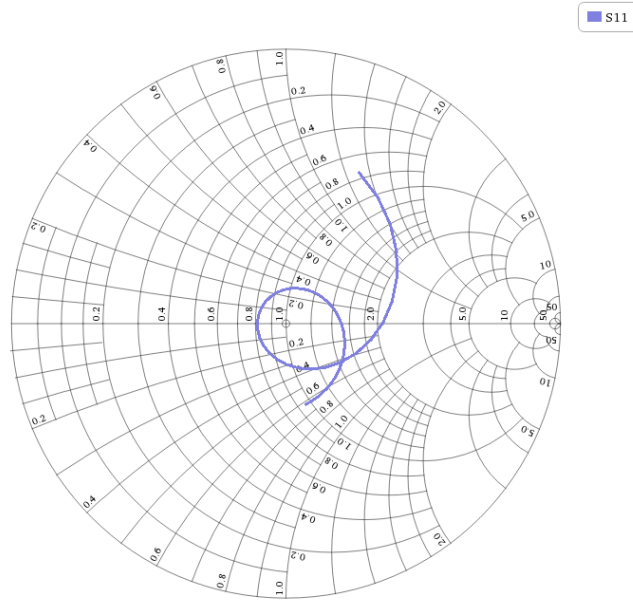
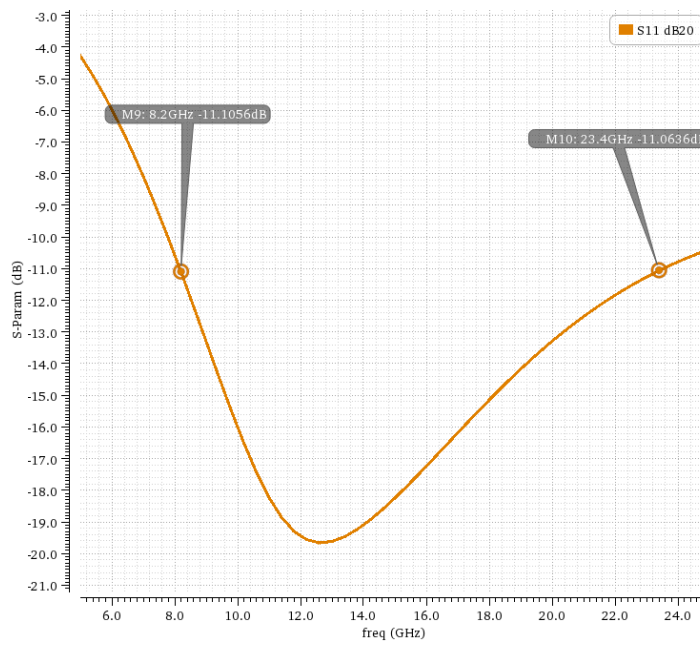**Figure 4.15:** S11 Parameter on Smith Chart
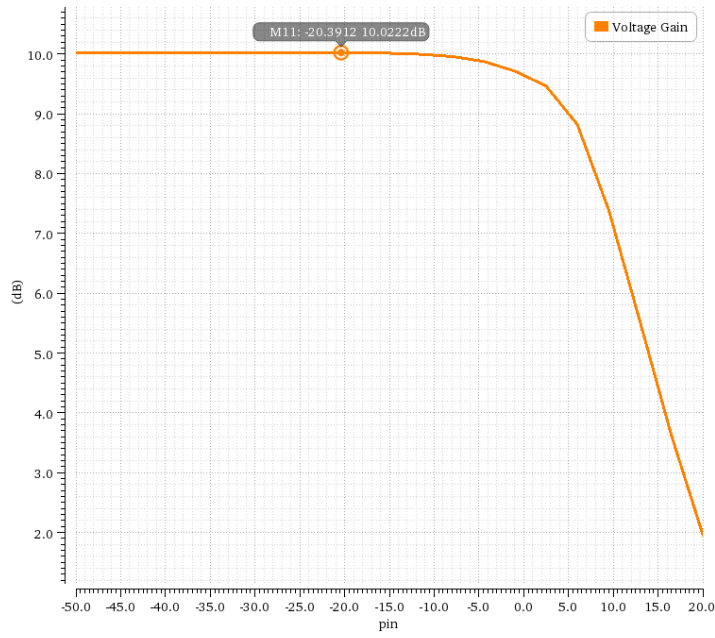

Figure 4.16: S11 versus Frequency

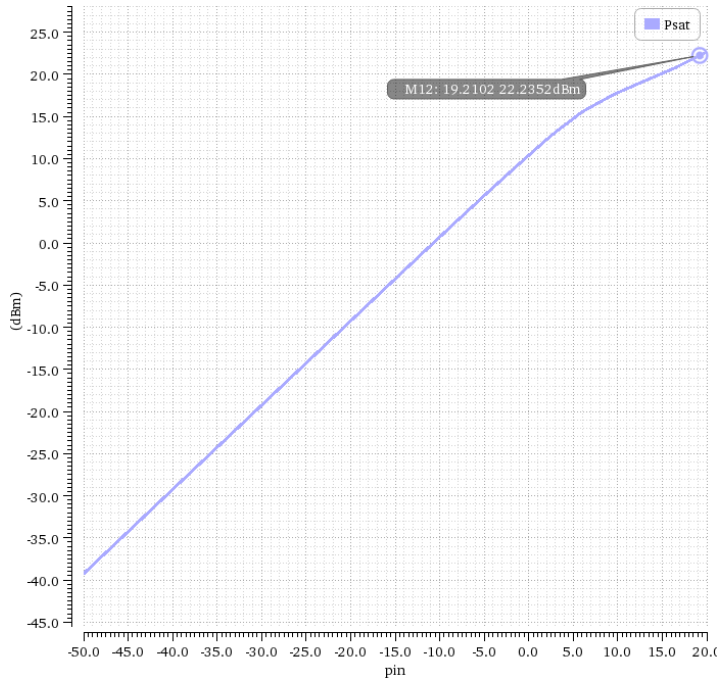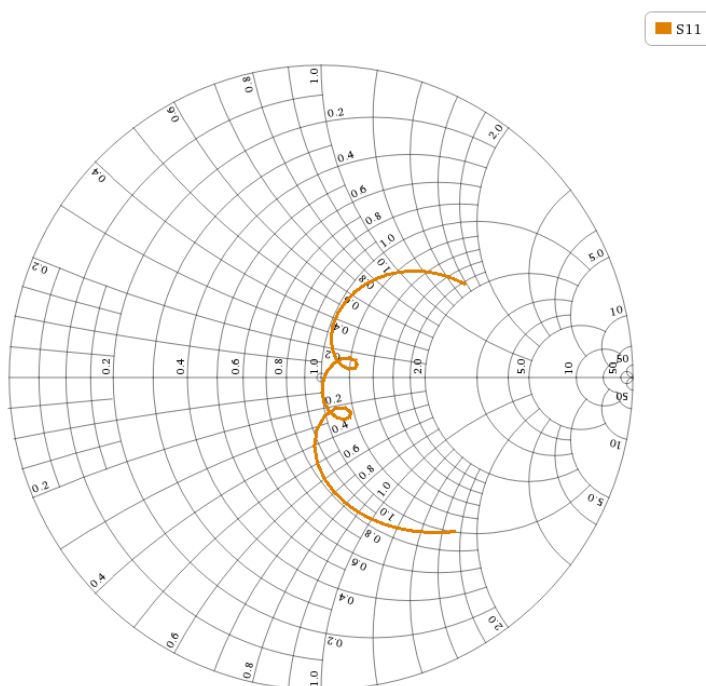**Figure 4.17:** Voltage Gain Plot

Figure 4.18: Plot for Saturated Power

4.4.2   Simulation Results: Antenna to LNA Path

The matching performance of the antenna to LNA path is demonstrated in figure 4.19 and figure 4.20. From these figures, we observe that the design achieves good matching across the frequency range from 9.4 GHz to 20.6 GHz, with the S11 value remaining below the -11 dB threshold.Additionally, figure 4.21 shows that the voltage gain of the design with the first stage of the LNA is 16.9 dB. However, there is a 3 dB reduction in gain compared to the stand-alone input matching network of LNA design, which is attributed to the inclusion of the antenna switch. Furthermore, figure 4.22 highlights a 2 dB increase in the noise figure, with the integrated design having a NF of 4.4 dB compared to the stand-alone design. This noise increase is also due to the addition of the antenna switch. Despite these trade-offs, we achieve good overall performance for both the receiver and transmitter paths, demonstrating the effectiveness of the integrated design.

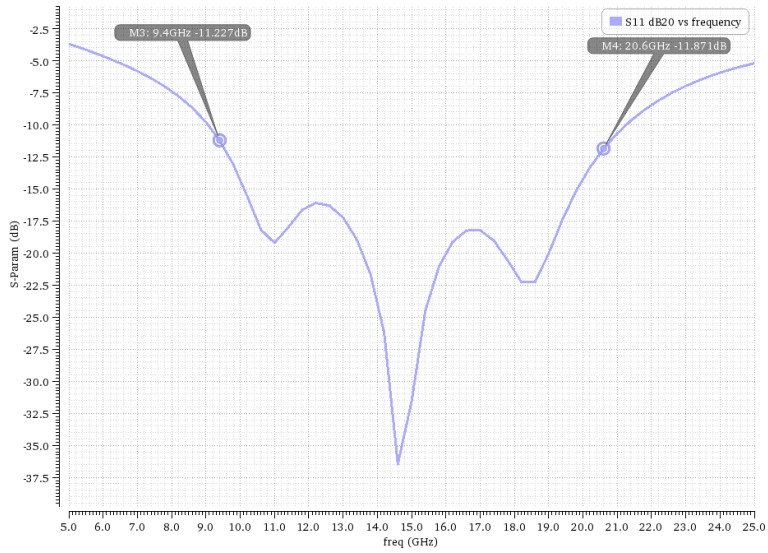**Figure 4.19:** S11 Parameter on Smith Chart
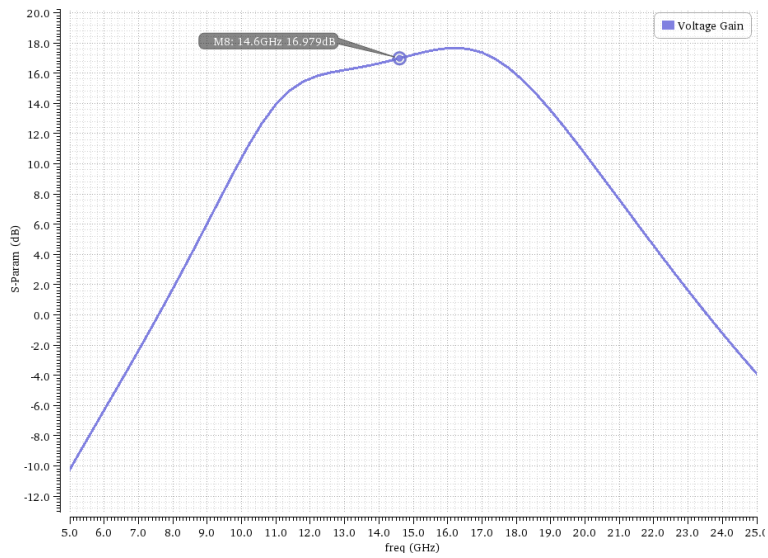
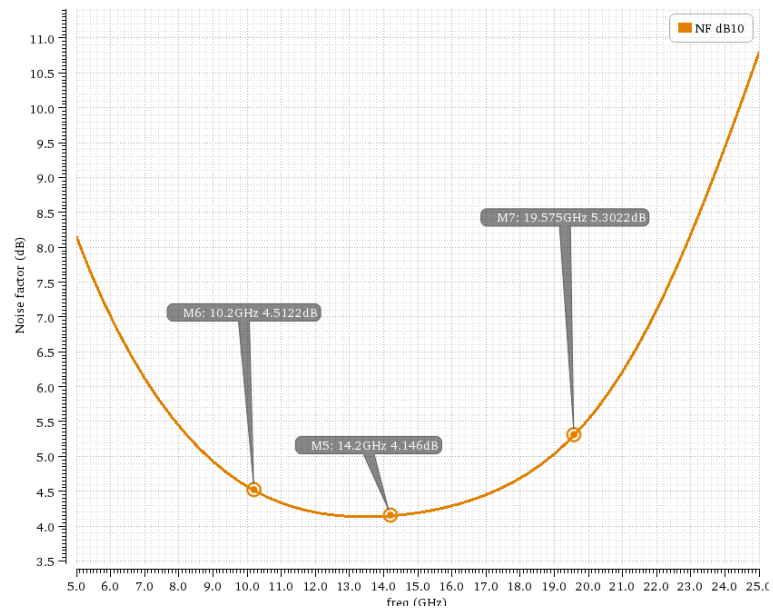**Figure 4.20:** S11 versus Frequency

Figure 4.21: Voltage Gain Plot

Figure 4.22: Noise Figure Plot

Chapter 5

Conclusion

This thesis focused on the design and optimization of key components for a wideband RF front-end module in the FR3 band using 22nm FDSOI technology. The objectives included the development of a wideband output matching network for the PA, a wideband input matching network for the LNA, and an antenna switch.

For the transmitter path, a transformer-coupled wideband output matching network was designed and simulated. Post-layout simulations confirmed that the design achieved a bandwidth of 8 to 24GHz, with a voltage gain of 11.5dB including the final stage of the PA. Importantly, the design footprint was maintained at a compact 0.024mm^2.

Similarly, a resistive feedback common-source amplifier was used to design a wideband input matching network for the LNA. After necessary layout adjustments, the post-layout simulations showed a bandwidth of 10 to 20GHz and a voltage gain of 19.85dB in the first stage of the LNA. The design also maintained a low noise figure of 2.9dB within the desired frequency range, with a layout area of 0.0304mm^2.

Additionally, an antenna SPDT switch with a series-shunt configuration was designed and analyzed. The effects of back-gate biasing and matching on insertion loss, return loss and isolation was studied. The design resulted in an isolation of 37dB, an insertion loss of 1.19dB at 14GHz, and a switching time 0.25ns.

For the integration, the designed LNA input matching network, PA output matching network, and antenna switch were successfully combined into a unified system. Post-integration performance evaluations showed that the system achieved a good matching performance from 9.4GHz to 20.6GHz in the receiver path, and from 8.2GHz to 23.4GHz in the transmitter path. The integrated design achieved a voltage gain of 10dB in the transmitter path and 16.9dB in the receiver path. A 1.5dB reduction in gain was observed due to the inclusion of the antenna switch in the transmitter path, while the noise figure in the receiver path increased by 2dB, reaching 4.4dB.

In conclusion, the designs developed in this thesis not only met the individual performance targets for wideband operation, compact size, and efficient signal handling but also demonstrated successful integration into a complete RF front-end system, optimized for operation in the FR3 band.

Future Work

The future work for this thesis involves a few key areas for improvement and expansion. One of the primary focuses will be refining the layout design of the matching networks to further enhance performance. For the LNA matching network, incorporating a bandpass filter before the resistive feedback stage could improve bandwidth [11]. However, this approach may introduce additional challenges, such as parasitics and a larger footprint, so careful design considerations will be necessary to mitigate these effects while still achieving a wide bandwidth.

In the antenna switch design, future work should prioritize completing the layout and conducting post-layout simulations to validate and optimize performance metrics like insertion loss, return loss, and isolation. Further research could also explore alternative configurations, such as employing different transistor technologies or tuning techniques to improve switching speed, reduce power consumption, and enhance overall efficiency.

While the integration of the LNA and PA matching networks has been completed at the layout level, the antenna switch is currently integrated only at the schematic level. A crucial step moving forward will be to complete the antenna switch layout and fully integrate it with the LNA and PA at the layout level. This will enable post-layout simulations of the entire RF front-end module, ensuring optimal performance and efficiency for wideband applications in the FR3 band.

References

[1] Domine Leenaerts, Johan van der Tang, Cierco Vaucher, *Circuit Design for RF Transceivers*

[2] Zhuangzhuang Cui, Peize Zhang, and Sofie Pollin, *6G Wireless Communications in 7–24 GHz Band: Opportunities, Techniques, and Challenges*, `https://arxiv.org/pdf/2310.06425`

[3] F. R. Gomez, *Design of impedance matching networks for RF applications*, Asian Journal of Engineering and Technology, vol. 6, no. 4, pp. 47-56, September 2018.

[4] L.Sundström, G.Jönsson, H.Börjeson, *Radio Electronics*, LTH, Electrical and Information Technology.

[5] Jack Browne, *Underlining the Meaning of Linearity*, `https://www.mwrf.com/technologies/components/article/21848259/microwaves-rf-underlining-the-meaning-of-linearity`

[6] S. N. Ong et al., *A 22nm FDSOI Technology Optimized for RF/mmWave Applications*, 2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Philadelphia, PA, USA, 2018, pp. 72-75,`10.1109/RFIC.2018.8429035`.

[7] Fritzin.Jonas, *Power Amplifier Circuits in CMOS Technologies*, 2009, Linköping studies in science and technology. Thesis, 0280-7971 ; 1414

[8] J.R. Long, *Monolithic transformers for silicon RF IC design*, in IEEE Journal of Solid-State Circuits, vol. 35, no. 9, pp. 1368-1382, Sept. 2000, `10.1109/4.868049`

[9] Bo Chen et al., *IEEE Microwave and Wire Comp Letters (MWCL*,vol. 27, pp. 377-379, 2017, `10.1109/LMWC.2017.2679047`

[10] J. Gong, W. Li, J. Ye, J. Hu and T. Wang, *An 8–18GHz c1ass-AB power amplifier with 16dBm output power and 23 % PAE over entire X-Ku band*,14th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), 2018, `10.1109/ICSICT.2018.8565695`

[11] S. Han, X. Wu, W. Li, Y. Wang, Y. Lin and H. Xu, *A 4.7-to-18-GHz Ultra-Wideband Variable-Gain Balun-LNA Using 3rd-Order-Band-Pass Input Matching in 40-nm CMOS*,2023 IEEE 15th International Conference on ASIC (ASICON), Nanjing, China, 2023, pp. 1-4, `10.1109/ASICON58565. 2023.10396238`

[12] T.-K. Nguyen, C.-H. Kim, G.-J. Ihm, M.-S. Yang, S.-G. Lee, *CMOS Low-Noise Amplifier Design Optimization Techniques*,IEEE Transactions on microwave theory and techniques, vol. 52, no. 5, May 2004, pp. 1433-1442, `10.1109/TMTT.2004.827014`

[13] C. Chen, X. Xu and T. Yoshimasu, *A DC-50 GHz, low insertion loss and high P1dB SPDT switch IC in 40-nm SOI CMOS*,2017 IEEE Asia Pacific Microwave Conference (APMC), Kuala Lumpur, Malaysia, 2017, pp. 5-8, `110.1109/APMC.2017.8251363`

[14] X. Chen and M. K. Raja, *A wideband 0.6dB insertion loss +20.5dBm P1dB CMOS T/R switch*,2011 International Symposium on Integrated Circuits, Singapore, 2011, pp. 184-187, `10.1109/ISICir.2011.6131908`

[15] M. Rack, L. Nyssens, S. Wane, D. Bajon and J. -P. Raskin, *DC-40 GHz SPDTs in 22 nm FD-SOI and Back-Gate Impact Study*,2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Los Angeles, CA, USA, 2020, pp. 67-70, `10.1109/RFIC49505.2020.9218317`