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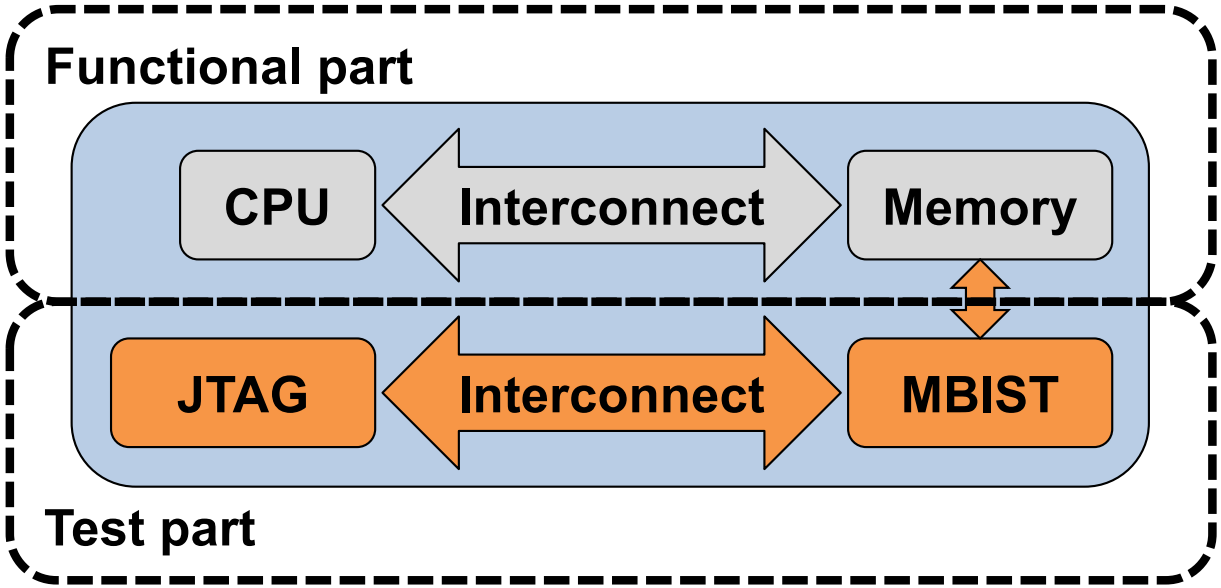
Access to on-chip test structures via functional buses

ERIK LARSSON

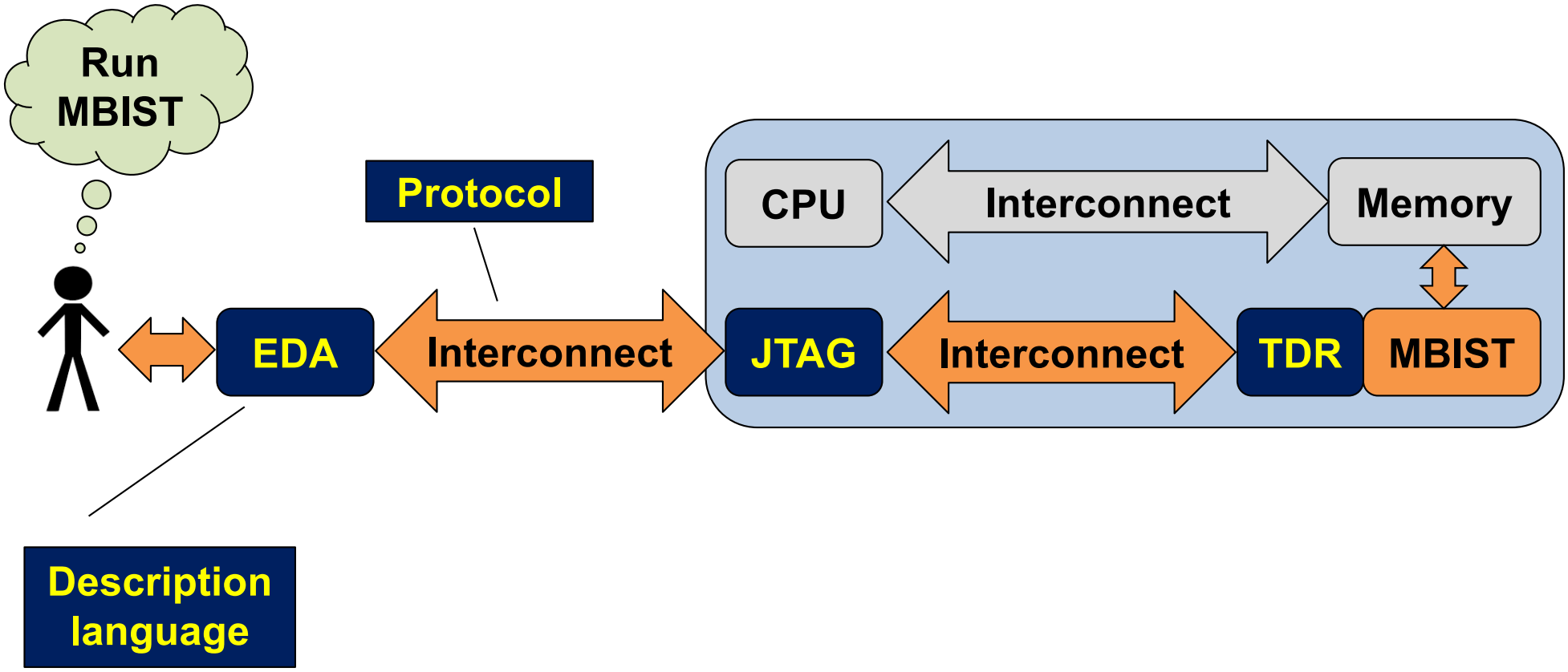
Semiconductors



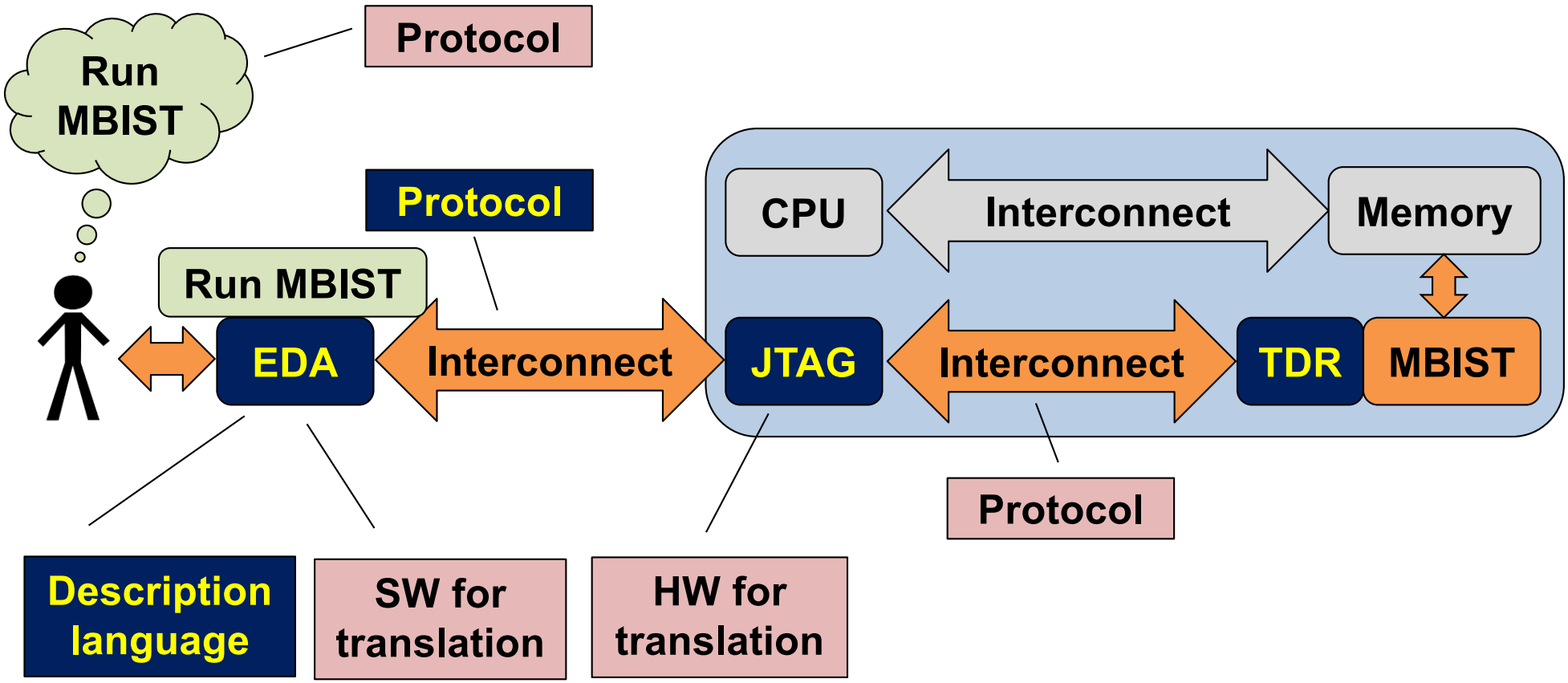
Standards

- IEEE Std. 1149.1 - Standard for Test Access Port and Boundary-Scan Architecture - (Joint Test Action Group (JTAG))

IEEE Std. 1149.1



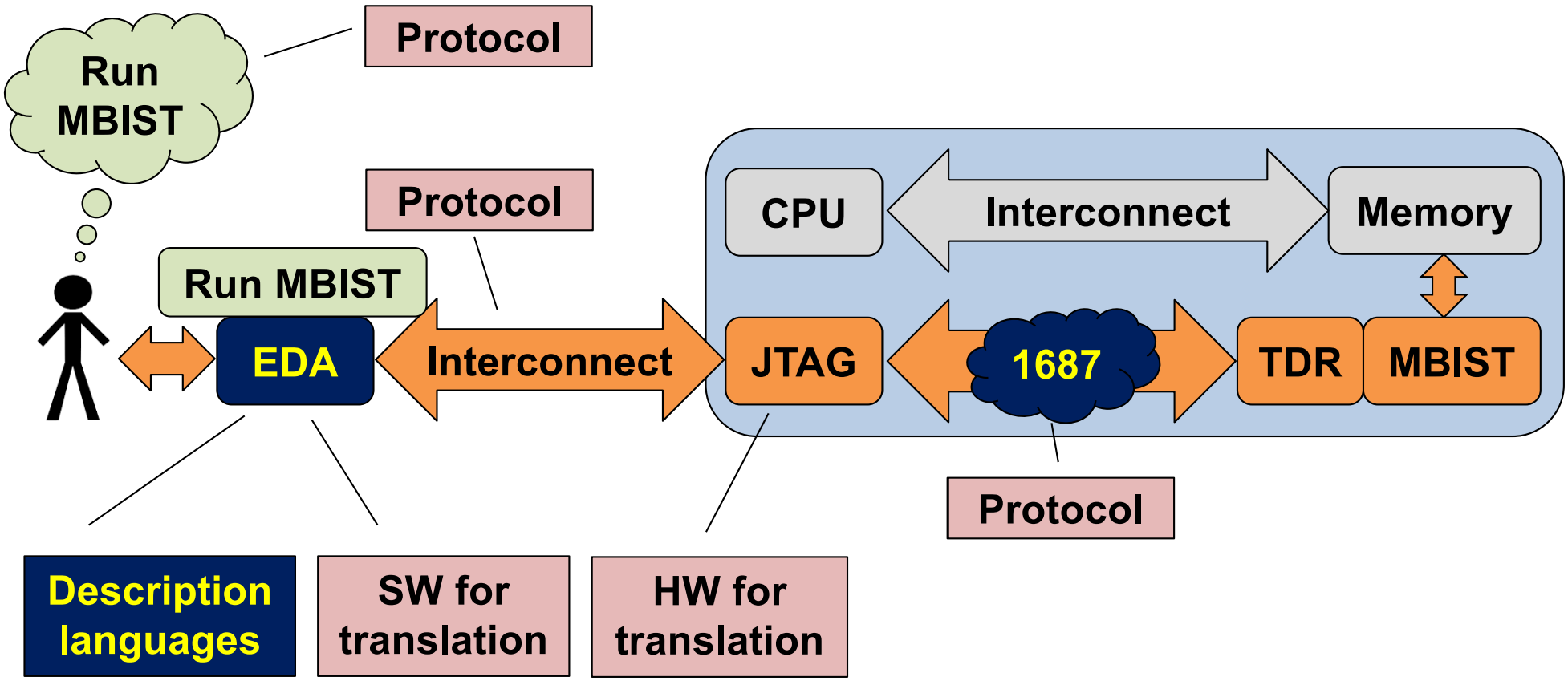
IEEE Std. 1149.1



Standards

- IEEE Std. 1149.1 - Standard for Test Access Port and Boundary-Scan Architecture - (Joint Test Action Group (JTAG))
- IEEE Std. 1687 - Standard for Access and Control of Instrumentation Embedded within a Semiconductor Device - (Internal JTAG (IJTAG))

IEEE Std. 1149.1+1687



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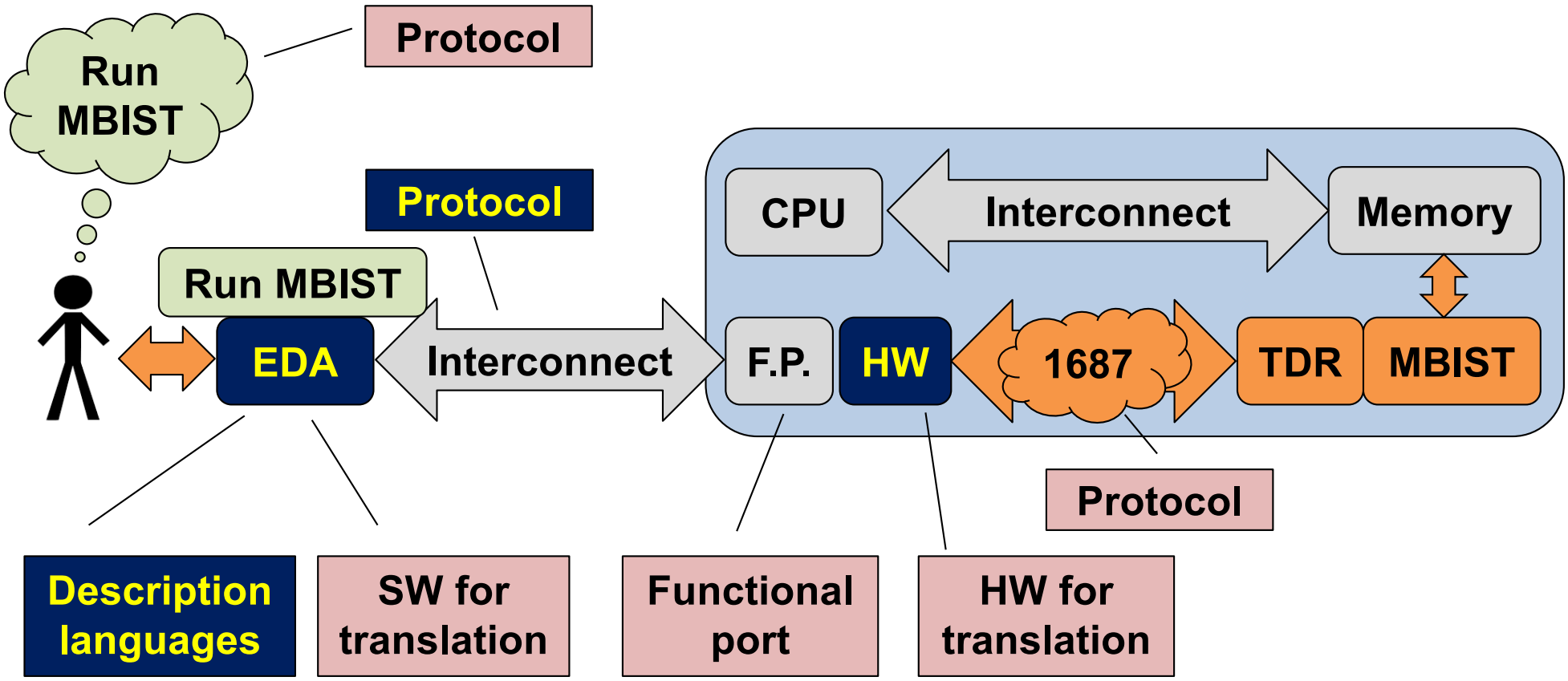
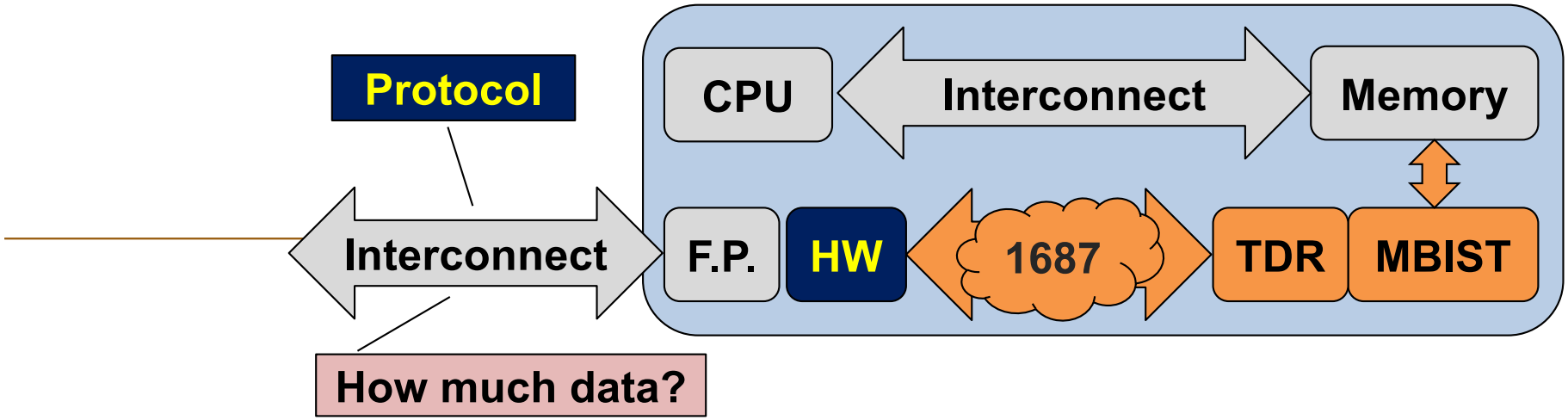
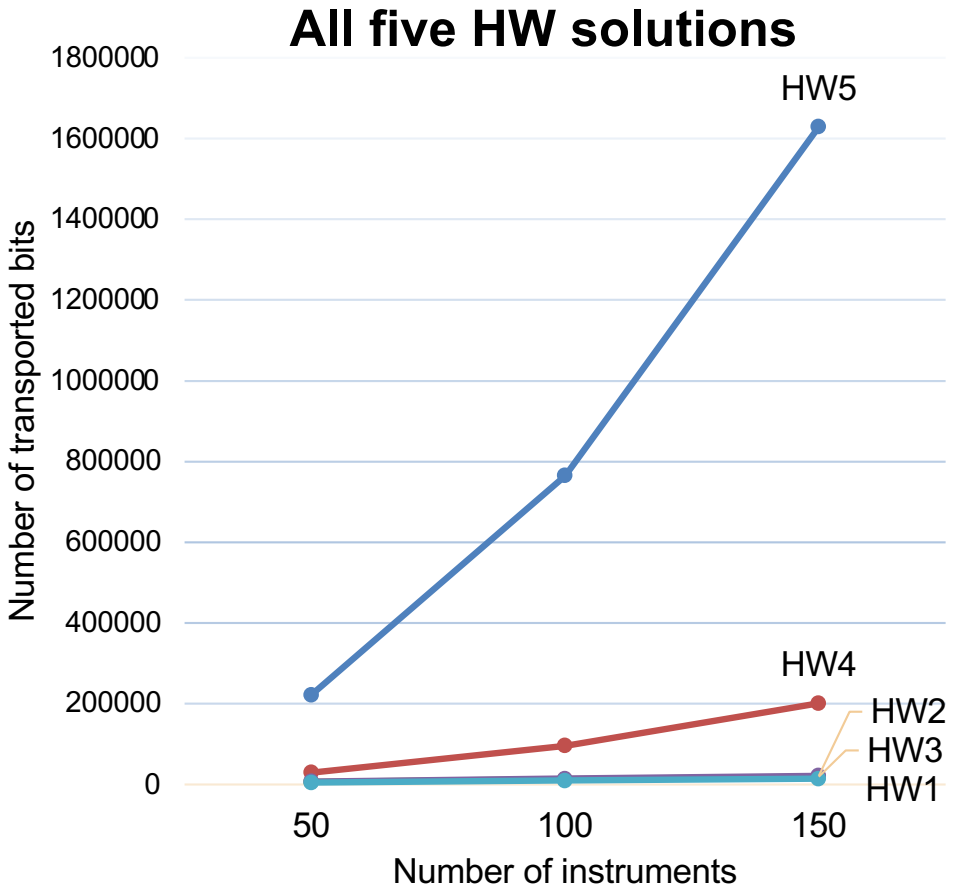
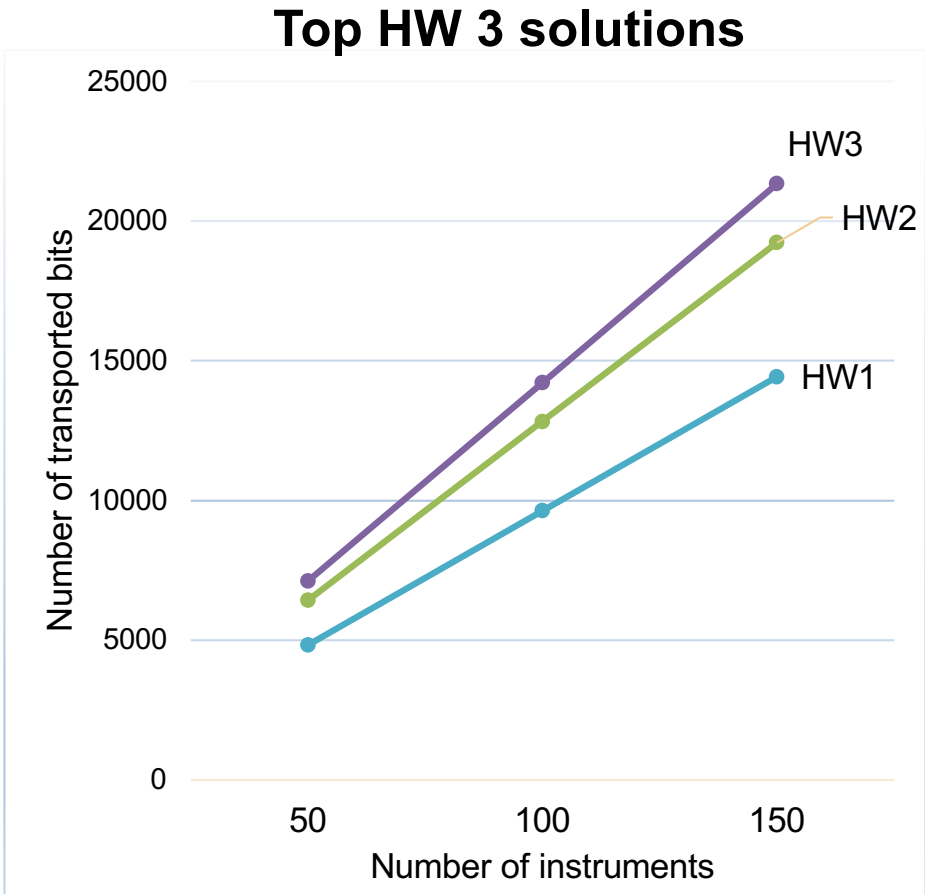
- IEEE Std. **P**1687.1 - Standard for the Application of Interfaces and Controllers to Access 1687 IJTAG Networks Embedded Within Semiconductor Devices

IEEE Std. 1149.1+1687+1687.1




Protocol
CPU
Interconnect
Memory
Interconnect
F.P.
HW
1687
TDR
MBIST
How much data?


All five HW solutions
1800000
1600000
1400000
1200000
1000000
800000
600000
400000
200000
0
Number of transported bits
HW5
HW4
HW2
HW3
HW1
50
100
150
Number of instruments


Top HW 3 solutions
25000
20000
15000
10000
5000
0
Number of transported bits
HW3
HW2
HW1
50
100
150
Number of instruments

Standards

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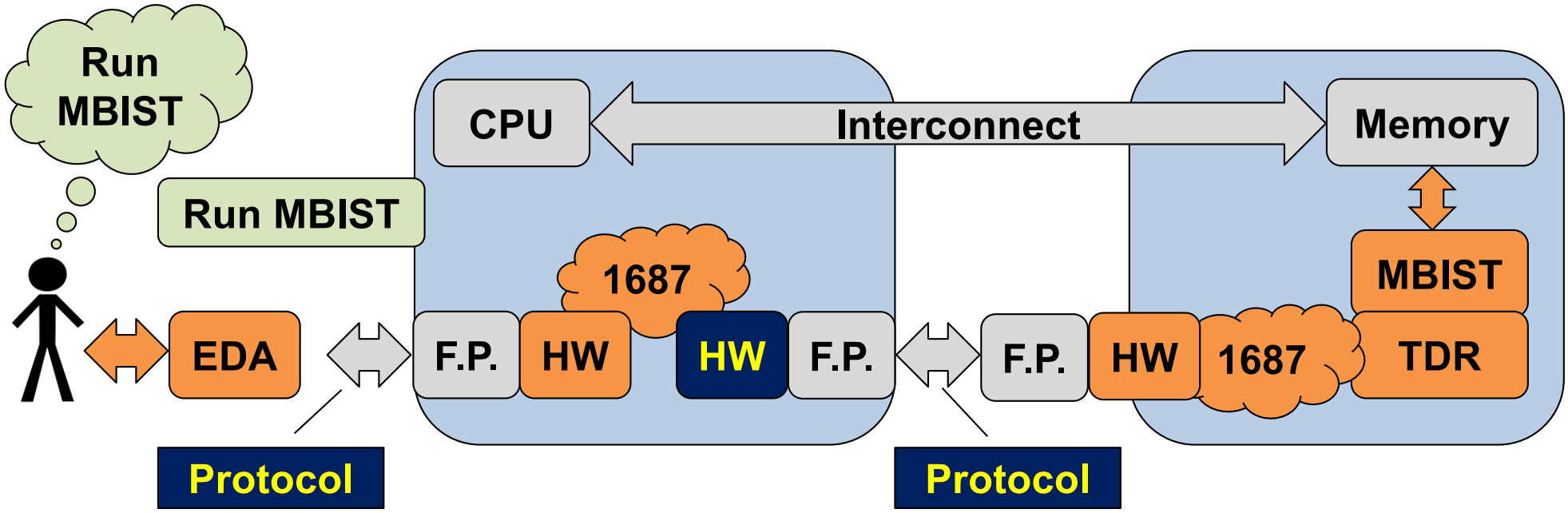
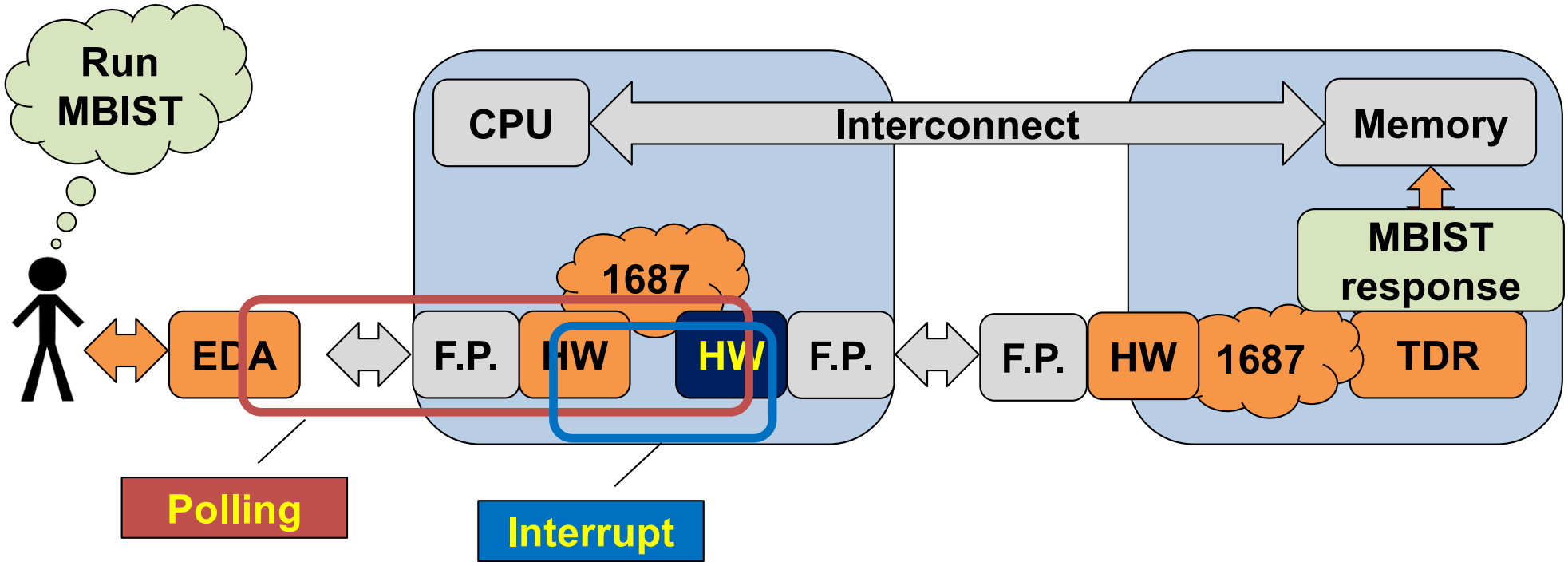
- IEEE Std. **P**2654 - Standard for System Test Access Management (STAM) to Enable Use of Sub-System Test Capabilities at Higher Architectural Levels - (System JTAG (SJTAG))

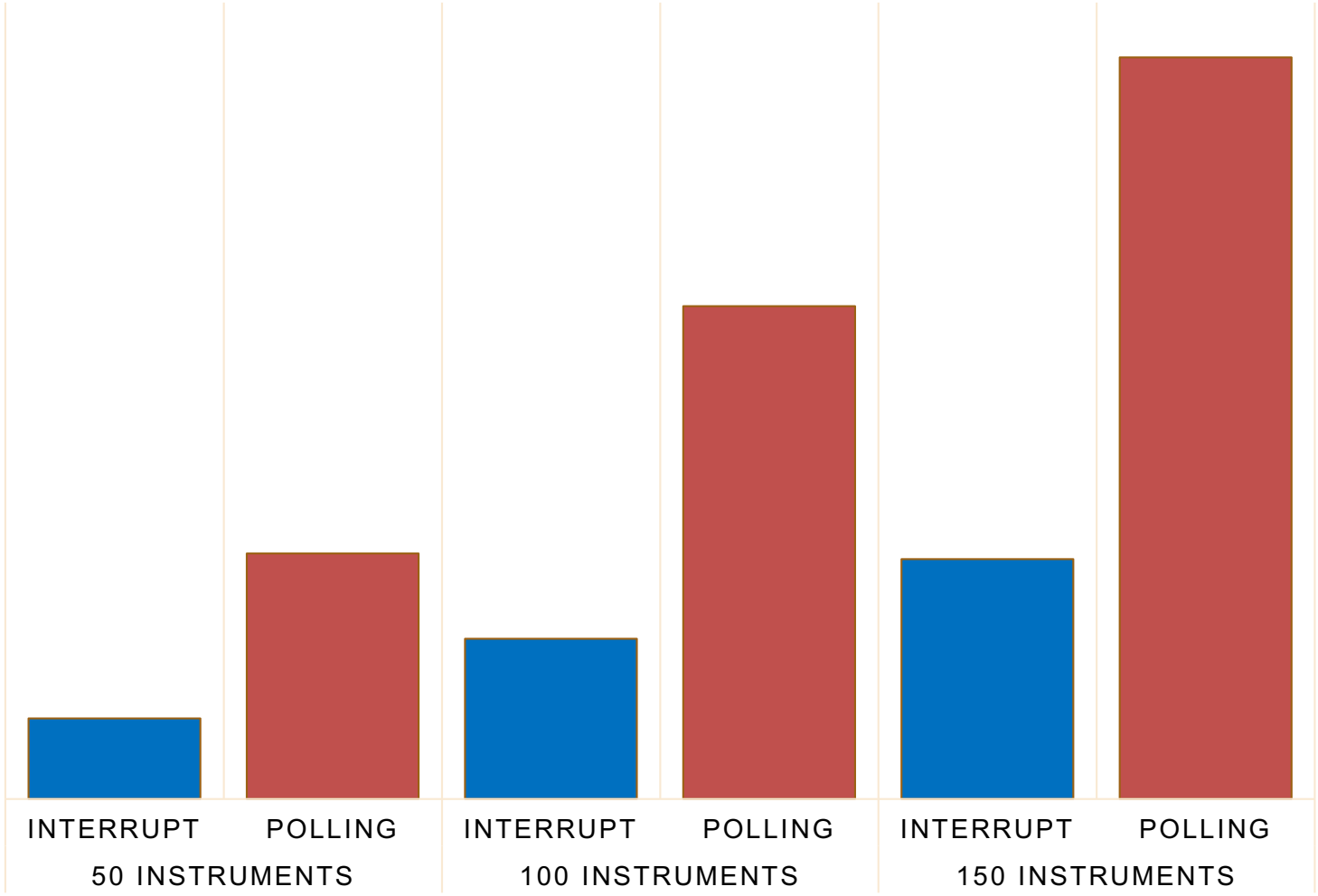
IEEE Std. 1149.1+1687+1687.1+2654



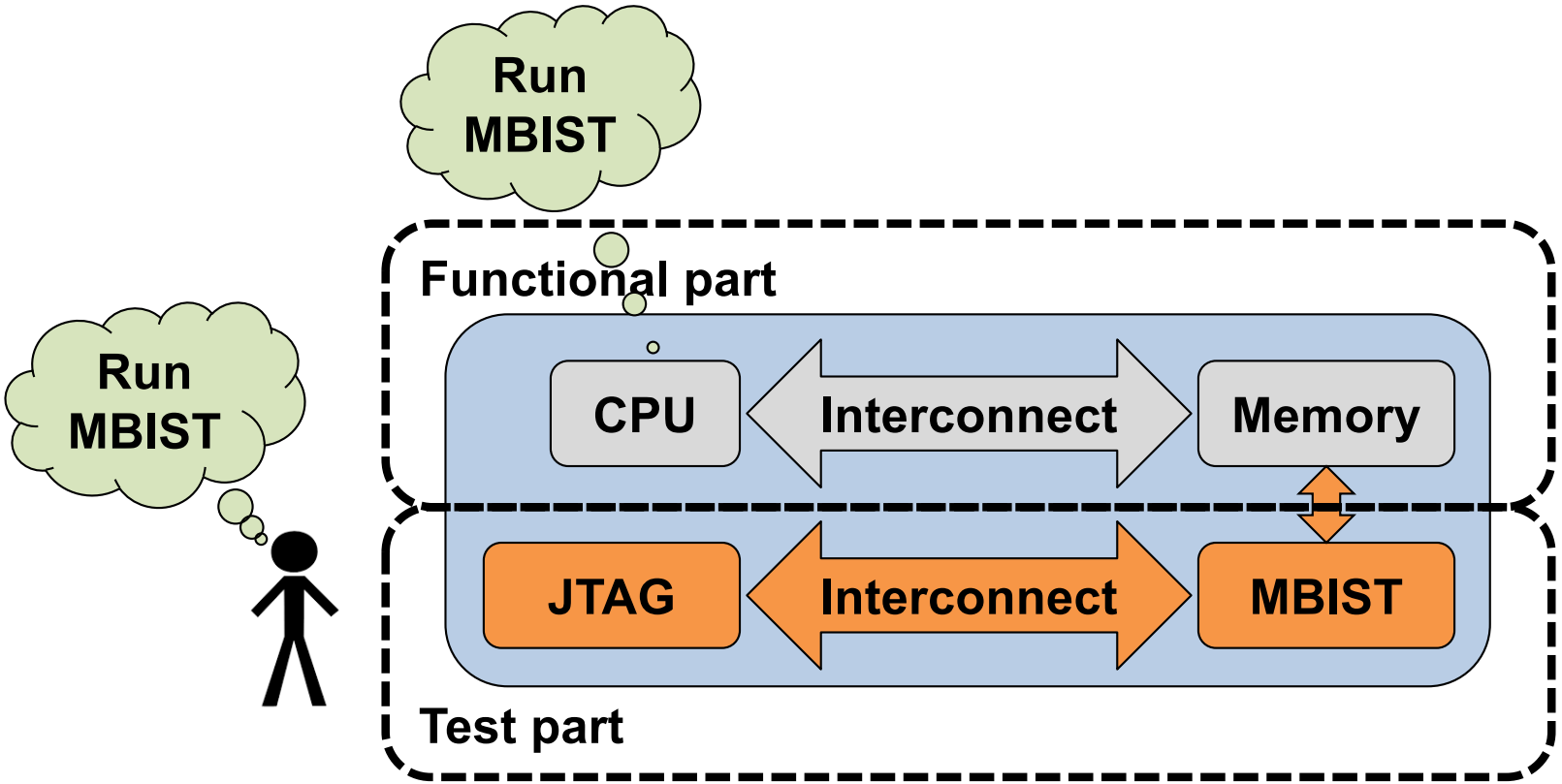
IEEE Std. 1149.1+1687+1687.1+2654



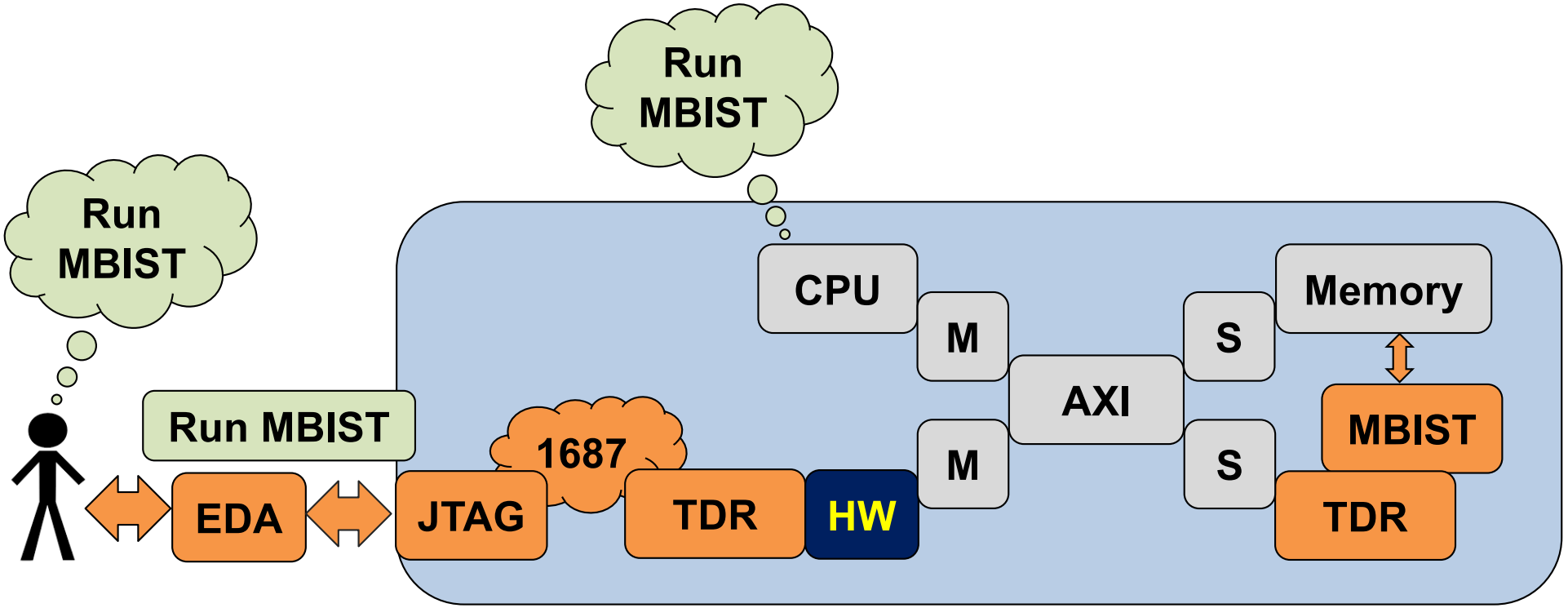
Data overhead



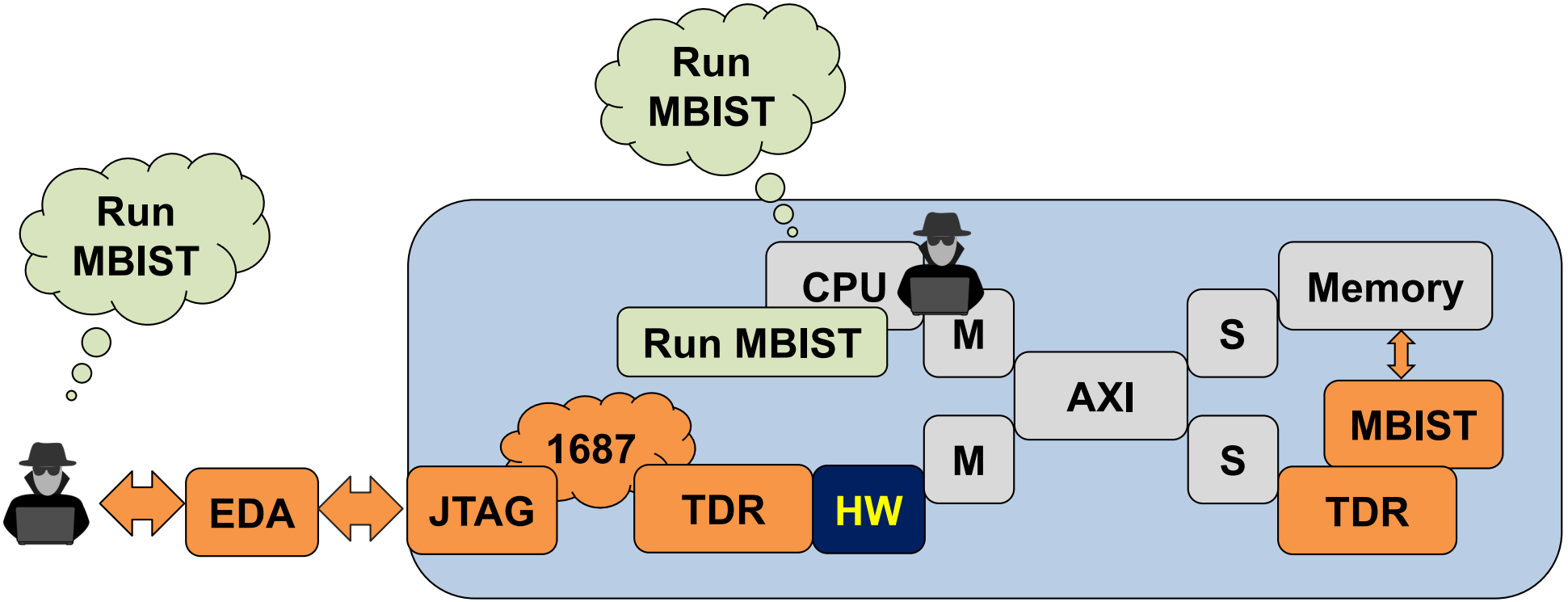
Shared access to test structures



Advanced eXtensible Interface (AXI)



Some future perspectives



Our papers

- Functional port instead of JTAG – IEEE Std. P1687.1
  - Erik Larsson, Prathamesh Murali & Gani Kumisbek, IEEE Std. P1687.1: translator and protocol, 2019, International Test Conference.(paper)(presentation)
  - Erik Larsson, Zilin Zhang & Prathamesh Murali, Accessing general IEEE Std. 1687 networks via functional ports, 2021, International Test Conference (paper)(video)
- Test and secure network of instruments
  - Erik Larsson, Zehang Xiang & Prathamesh Murali, Graceful Degradation of Reconfigurable Scan Networks, 2021 May 27, In: IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 29, 7, p. 1475-1479. (paper)(video)
- Board-level access – IEEE Std. P2654
  - Erik Larsson, Shashi Kiran Gangaraju & Prathamesh Murali, System-Level Access to On-Chip Instruments, 2021 Apr 1, IEEE European Test Symposium (ETS). p. 1-6. (paper)(video)

IEEE-SA Test Technology Standards Committee (Chair Ian McIntosh)

IEEE Std 1149.1 “Standard for Test Access Port and Boundary-Scan Architecture” expires at the end 2023.

- Contact Heiko Ehrenberg (h.ehrenberg@goepelusa.com) to join the group or for further details.

IEEE Std 1687 “Standard for Access and Control of Instrumentation Embedded within a Semiconductor Device” expires at the end of 2024.

- Contact Jeff Rearick (Jeff.Rearick@amd.com) to join the group or for further details.

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Access to on-chip test structures via functional buses

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