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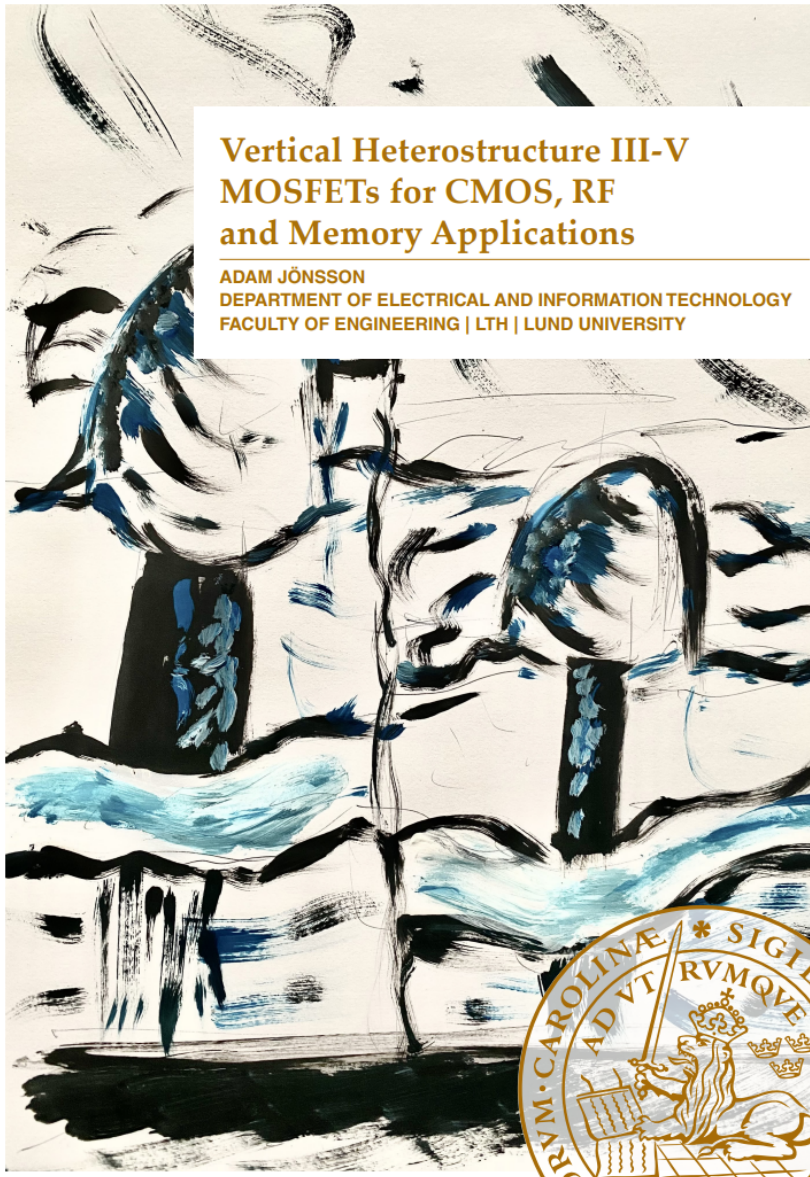

Vertical Heterostructure III-V MOSFETs for CMOS, RF and Memory Applications

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Vertical Heterostructure III-V MOSFETs for CMOS, RF and Memory Applications

Doctoral Thesis

Adam Jönsson

LUND
UNIVERSITY

Department of Electrical and
Information Technology
Lund, August 2021

Academic thesis for the degree of Doctor of Philosophy, which, by due permission of the Faculty of Engineering at Lund University, will be publicly defended on Friday, September 17, 2021, at 9:15 a.m. in lecture hall E:1406, Department of Electrical and Information Technology, Ole Römers Väg 3, 223 63 Lund, Sweden. The thesis will be defended in English.

The Faculty Opponent will be Professor Aaron Voon-Yew Thean, National University of Singapore.

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Vertical Heterostructure III-V MOSFETs for CMOS, RF and Memory Applications

Abstract:
MOSFETs on Si (Paper I & II), where MOVPE grown vertical InAs-GaSb heterostructure nanowires are used for realizing monolithically integrated and co-processed all-III-V CMOS. Utilizing a bottom-up approach based on MOVPE grown nanowires enables design flexibilities, such as in-situ doping and heterostructure formation, which serves to reduce the amount of mask steps during fabrication. By refining the fabrication techniques, using a self-aligned gate-last process, scaled 10-20 nm diameters are achieved for balanced drive currents at $I_{on} \sim 100$ μA/μm, considering I_{off} at 100 nA/μm (V_{DD} = 0.5 V). This is enabled by greatly improved p-type MOSFET performance reaching a maximum transconductance of 260 μA/μm at V_{DS} = 0.5 V. Lowered power dissipation for CMOS circuits requires good threshold voltage V_T matching of the n- and p-type device, which is also demonstrated for basic inverter circuits. The various effects contributing to V_T-shifts are also studied in detail focusing on the InAs channel devices (with highest transconductance of 2.6 mA/μm), by using Electron Holography and a novel gate position variation method (Paper V).
The advancements in all-III-V CMOS integration spawned individual studies into the strengths of the n- and p-type III-V devices, respectively. Traditionally materials such as InAs and InGaAs provide excellent electron transport properties, therefore they are frequently used in devices for high frequency RF applications. In contrast, the III-V p-type alternatives have been lacking performance mostly due to the difficult oxidation properties of Sb-based materials. Therefore, a study of the GaSb properties, in a MOSFET channel, was designed and enabled by new manufacturing techniques, which allowed gate-length scaling from 40 to 140 nm for p-type Sb-based MOSFETs (Paper III). The new fabrication method allowed for integration of devices with symmetrical contacts as compared to previous work which relied on a tunnel-contact at the source-side. By modelling based on measured data field-effect hole mobility of 70 cm^2/Vs was calculated, well in line with previously reported studies on GaSb nanowires. The oxidation properties of the GaSb gate-stack was further characterized by XPS, where high intensities of x-rays are achieved using a synchrotron source allowed for characterization of nanowires (Paper VI). Here, in-situ H_2-plasma treatment, in parallel with XPS measurements, enabled a study of the time-dependence during full removal of GaSb native oxides.
The last focus of the thesis was building on the existing strengths of vertical heterostructure III-V n-type (InAs-InGaAs graded channel) devices. Typically, these devices demonstrate high-current densities (g_m >3 mS/μm) and excellent modulation properties (off-state current down to 1nA/μm). However, minimizing the parasitic capacitances, due to various overlaps originating from a low access-resistance design, has proven difficult. Therefore, new methods for spacers in both the vertical and planar directions was developed and studied in detail. The new fabrication methods including sidewall spacers achieved gate-drain capacitance C_{GD} levels close to 0.2 fF/μm, which is the established limit by optimized high-speed devices. The vertical spacer technology, using SiO_2 on the nanowire sidewalls, is further improved in this thesis which enables new co-integration schemes for memory arrays. Namely, the refined sidewall spacer method is used to realize selective recess etching of the channel and reduced capacitance for large array memory selector devices (InAs channel) vertically integrated with Resistive Random Access Memory (RRAM) memristors. (Paper IV) The fabricated 1-transistor-1-memristor (1T1R) demonstrator cell shows excellent endurance and retention for the RRAM by maintaining constant ratio of the high and low resistive state (HRS/LRS) after 10^6 switching cycles.

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This thesis is typeset using LaTeX 2ε with the body text in Palatino and Goudy Initials, headings in Helvetica, text in figures in Arial.

Frontispiece: Oil interpretation by the author Adam Jönsson of a FIB cross-section of nanowire based III-V CMOS.

Printed by Tryckeriet i E-huset, Lund University, Lund, Sweden.

In dedication to my father, Lars Jönsson
May you rest in peace.

Abstract

This thesis focuses mainly on the co-integration of vertical nanowire n-type InAs and p-type GaSb MOSFETs on Si (Paper I & II), where MOVPE grown vertical InAs-GaSb heterostructure nanowires are used for realizing monolithically integrated and co-processed all-III-V CMOS. Utilizing a bottom-up approach based on MOVPE grown nanowires enables design flexibilities, such as in-situ doping and heterostructure formation, which serves to reduce the amount of mask steps during fabrication. By refining the fabrication techniques, using a self-aligned gate-last process, scaled 10-20 nm diameters are achieved for balanced drive currents at $I_{on} \sim 100$ μA/μm, considering I_{off} at 100 nA/μm ($V_{DD} = 0.5$ V). This is enabled by greatly improved p-type MOSFET performance reaching a maximum transconductance of 260 μA/μm at V_{DS} = 0.5 V. Lowered power dissipation for CMOS circuits requires good threshold voltage V_T matching of the n- and p-type device, which is also demonstrated for basic inverter circuits. The various effects contributing to V_T-shifts are also studied in detail focusing on the InAs channel devices (with highest transconductance of 2.6 mA/μm), by using Electron Holography and a novel gate position variation method (Paper V).

The advancements in all-III-V CMOS integration spawned individual studies into the strengths of the n- and p-type III-V devices, respectively. Traditionally materials such as InAs and InGaAs provide excellent electron transport properties, therefore they are frequently used in devices for high frequency RF applications. In contrast, the III-V p-type alternatives have been lacking performance mostly due to the difficult oxidation properties of Sb-

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The last focus of the thesis was building on the existing strengths of vertical heterostructure III-V n-type (InAs-InGaAs graded channel) devices. Typically, these devices demonstrate high-current densities (g_m >3 mS/μm) and excellent modulation properties (off-state current down to 1nA/μm). However, minimizing the parasitic capacitances, due to various overlaps originating from a low access-resistance design, has proven difficult. Therefore, new methods for spacers in both the vertical and planar directions was developed and studied in detail. The new fabrication methods including sidewall spacers achieved gate-drain capacitance C_{GD} levels close to 0.2 fF/μm, which is the established limit by optimized high-speed devices. The vertical spacer technology, using SiO_2 on the nanowire sidewalls, is further improved in this thesis which enables new co-integration schemes for memory arrays. Namely, the refined sidewall spacer method is used to realize selective recess etching of the channel and reduced capacitance for large array memory selector devices (InAs channel) vertically integrated with Resistive Random Access Memory (RRAM) memristors. (Paper IV) The fabricated 1-transistor-1-memristor (1T1R) demonstrator cell shows excellent endurance and retention for the RRAM by maintaining constant ratio of the high and low resistive state (HRS/LRS) after 10^6 switching cycles.

Populärvetenskaplig Sammanfattning

Omsättningen för den globala halvledarindustrin uppgår till 509 miljarder dollar år 2020 och under de kommande åren förväntas stadig tillväxt. Denna tillväxt har traditionellt sett drivits framåt av konsumentvaror såsom datorer och smarta mobiltelefoner. Dock förväntas behovet av mer konsumentelektronik att stagnera medan andra nya applikationer signifikant kommer expandera industrin. Bland dessa nya applikationer finner vi bland annat sakernas internet (IoT) och molnbaserade beräkningar, men framför allt produkter baserade kring AI och 5G-nätverk. Vi går därmed mot en framtid med mer specialiserad hårdvara anpassad för ett flertal olika användningsområden. Trots denna spridning inom industrin förblir den huvudsakliga inkomstkällan olika typer av processorer, vars viktigaste beståndsdel är fälteffekttransistorn. Denna utveckling har därmed bidragit till en industri som tillåter en mycket större mångfald av nya och intressanta förbättringar av fält-effekts transistorerna.

Till största delen har förbättringar för konsumentvaror inom halvledarindustrin drivits framåt med hjälp av miniatyrisering av transistorn samt förbättringar av de elektriska ledningarna som sammankopplar dessa. På grund av grundläggande fysik har det blivit mer och mer problematiskt att fortsätta med denna trend då de kritiska storlekarna hos de elektriska komponenterna närmar sig ett fåtal atomlager. Intresset för alternativa material som kan ersätta kisel på komponentnivå har därmed ökat markant. Bland dessa alternativ finns III-V halvledarna. I dessa material kan elektroner röra sig snabbare, vilket kan ge större strömmar utan ökad effektförlust. Inom analoga användningsområden såsom förstärkning av

diverse kommunikationssignaler, har det redan blivit lönsamt att använda III-V material. Denna utveckling har inte kunnat ske på samma sätt för digitala applikationsområden. För fortsatt utveckling krävs dock att analoga förstärkningar av hög-frekventa signaler sker parallell t med digitala beräkningar. Alltså behöver metoder utvecklas för att sammanföra digitala samt analoga beräkningsblock bestående av olika kretsar.

Inom detta arbete introducerar vi nya kretsar för digitala applikationer, kompatibla med framtidens högfrekvensförstärkare. Detta har möjliggjorts med hjälp av stora framsteg inom förståelsen hos antimonid-baserade material. Dessa material är en subgrupp bland III-V föreningarna, där exempelvis gallium-antimonid redan nu används flitigt inom LED-teknik samt optoelektronik. Olika metoder har alltså utvecklats för att realisera förbättrade transistorer baserade på gallium-antimonid, integrerade med andra mer traditionella III-V transistorer. Gallium-antimonid erbjuder bättre rörlighet av laddningsbärarna hål, vilket krävs för att realisera komplementära kretsar nödvändiga för digitala applikationer. Intresset för antimonider har också ökat under senaste tiden då dessa förutspås användas för att skapa robusta system för kvantdatorer.

Utvecklingen av nya integrations och tillverkningsstrategier leder till en demonstration av en ny typ av III-V baserad minnescell, som kan användas för att realisera så kallad In-Memory Computation. Traditionellt sett måste resultatet från digitala beräkningar fysiskt förflyttas för att sedan sparas i en separat minnescell. Alla dessa steg leder till ökad fördröjning vilket därmed begränsar prestanda. Dessa typiskt sett separata block kan sammanföras för att parallellisera beräkningarna, denna metod kallas för In-Memory Computation. Data kan därmed sparas i form av mönster som kan sedan åberopas för beräkningar i realtid, vilket är speciellt viktigt för exempelvis bildigenkänning.

Acknowledgments

♪*"Beneath the stains of time*
The feelings disappear
You are someone else
I'm still right here" ♪
- Johnny Cash, *Hurt*

This thesis has been produced during a turbulent and extremely eventful time of my life. To maintain bearings during a bittersweet journey a few people has acted as anchor points for safe navigation through the difficult waters that has been my life as well as my academic career. Namely *Cezar Zota*, *Olli-Pekka Kilpi*, *Fredrik Lindelöw*, *Stefan Andric*, *Saketh Ram*, *Marcus Sandberg*, *Karl-Magnus Persson* and *Martin Hjort*. My supervisor and mentor *Lars-Erik Wernersson* has showed great patience and understanding throughout this journey, and I will forever be grateful for that. *Johannes Svensson* and *Erik Lind* have been a encyclopedia of knowledge and I am happy to consider them my dear friends.

Furthermore, I want to extend my gratitude to all my wonderful colleagues who I have shared many laughs with, all of them have provided a joyful work environment. So thank you to *Zhongyunshen Zhu*, *Lars Ohlsson*, *Mattias Borg*, *Sebastian Heunich*, *Jun Wu*, *Markus Hellenbrand*, *Abinaya Krishnaraja*, *Ben Nel*, *Johan Lundgren*, *Daniel Sjöberg*, *Hannes Dahlberg*, *Gautham Rangasamy*, *Heera Menon*, *Robin Atle*, *Lasse Södergren*, and *Patrik Olausson*.

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On a closing note, I have to thank my dear family *Lars* (in spirit), *Charitha*, and my brother *Max*.

Adam Jönsson
Lund, Aug 2021

Contents

Preface

This thesis is the grand summary of about five years of work in the *Nanoelectronics Group* (now known as *Elektromagnetism & Nanoelektronik*) at Lund University. We explore various applications, within electronics, in the field of narrow gap III-V semiconductors and present a detailed studies of Vertical Nanowire Metal-Oxide-Semiconductor Field-Effect Transistors (V-NW MOSFETs). This work provides the building blocks to synthesize, and to connect, fully III-V based systems, spanning from digital applications and memory systems all the way to high-frequency analog applications. The work was supervised by Professor *Lars-Erik Wernersson*, Doctor *Johannes Svensson* and Professor *Erik Lind*.

STRUCTURE OF THE THESIS

The thesis is essentially an article compilation with an extensive introduction outlining the theory behind the work as well as an outlook by providing benchmarking. The main part of the thesis covers the topic of All-III-V CMOS that ultimately spawned separate studies into both n- and p-type based vertical III-V nanowire MOSFETs (including memory selectors). The various developed MOSFETs implement VLS-grown nanowires ranging from InAs to heterostructure based nanowires including InAs-GaSb and InAs-InGaAs nanowires.

- **INTRODUCTION**
  In addition to the introduction the majority of the thesis consists of the publications appended in the back. The Introduction provides a framework for the focused and topics-wise, scattered publications. The Introduction is intended to work as an encyclopedia for aspiring researchers focusing on semiconductor-based electrical devices.

- **APPENDICES**

  A Fabrication Recipes
  Appendix A provides a detailed process flow of III-V CMOS, p-type III-V MOSFET, RF n-type III-V MOSFET and various process modules.

- **PAPERS**
  The papers forming the main body of the thesis are reproduced in the back and listed in the following section.

INCLUDED PAPERS

The following papers form the main body of this thesis and the respective published or draft versions are appended in the back.

Paper I: A. Jönsson, J. Svensson, and L.-E. Wernersson, "A Self-Aligned Gate-Last Process Applied to All-III-V CMOS on Si", *IEEE Electorn Devices Letters*, vol. 39, no. 7, pp. 935-938, July 2018, doi: 10.1109/LED.2018.2837676.
► *I carried out processing of devices, performed measurements and analyses and wrote the paper.*

Paper II: A. Jönsson, J. Svensson, and L.-E. Wernersson, "Balanced Drive Currents in 10-20 nm Diameter Nanowire All-III-V CMOS on Si", *IEEE International Electron Devices Meeting (IEDM)*, Dec. 2018, DOI: 10.1109/IEDM.2018.8614685.
► *I carried out processing of devices, performed measurements and analyses and wrote the paper.*

Paper III: A. Jönsson, J. Svensson, E. Lind, and L.-E. Wernersson, "Gate-Length Dependence of Vertical GaSb Nanowire p-MOSFETs on Si", *IEEE Transactions on Electron Devices*, vol. 67, no. 10, pp. 4118-4122, Oct. 2020, doi: 10.1109/TED.2020.3012126.
► *I carried out processing of devices, performed measurements and analyses and wrote the paper.*

Paper IV: S. R. Mamidala, K.-M. Persson, A. Irish, A. Jönsson, R. Timm, and L.-E. Wernersson, "High Density Logic-in-Memory using Vertical III-V Nanowires on Silicon", *Nature Electronics* vol. 4, no. 12, pp. 914-920, Dec. 2021, doi: 10.1038/s41928-021-00688-5.
► *I created process modules and collaborated for hardware implementation, created 3d schematic figures, and was involved in early stages of paper writing.*

Paper V: A. Jönsson, J. Svensson, E.M. Fiordaliso, E. Lind, M. Hellenbrand, and L.-E. Wernersson, "Doping Profiles in Ultrathin Vertical VLS-Grown InAs Nanowire MOSFETs with High Performance", *ACS Applied Electronic Materials* vol. 3, no. 12, pp. 5240-5247, Nov. 2021, doi: 10.1021/acsaelm.1c00729.

► *I carried out processing of devices, performed measurements and analyses and wrote the paper.*

Paper VI: S. Yngman, G. D' Acunto, Y-P. Liu, A. Troian, A. Jönsson, J. Svensson, S. Andric, L.-E. Wernersson, A. Mikkelsen and R. Timm, "Characterization of GaSb surfaces and nanowires during oxide removal", *Manuscript in preparation*

► *I provided samples and feedback regarding plasma treatment and paper writing.*

Paper VII: Z. Zhu, J. Svensson, A. Jönsson, and L.-E. Wernersson, "Improvement of GaSB Vertical Nanowire p-type MOSFETs on Si Using Rapid Thermal Annealing", *IOPscience Nanotechnology* vol. 4, no. 7, pp. 075202, Nov. 2021, doi: 10.1088/1361-6528/AC3689.

► *I assisted in process development by providing process modules, and also involved in paper writing.*

Paper VIII: Z. Zhu, A. Jönsson, Y.-P. Liu, J. Svensson, Rainer Timm, and L.-E. Wernersson, "Improved Electrostatics in GaSb vertical nanowire p-MOSFETs by Employing Controllable Digital Etch Schemes", *Accepted in ACS Applied Electronic Materials Dec. 2021*

► *I assisted in process development by providing process modules, prepared samples for XPS-study, and also outlined the paper topic.*

RELATED WORK

The following publications are not included in the thesis, but summarise related work that I was involved in. The work is divided into peer-reviewed journal papers and conference contributions and is listed according to the thematic order of the thesis.

CONFERENCE CONTRIBUTIONS

Paper ix: A. Jönsson, J. Svensson, and L.-E. Wernersson, "Vertical, High-Performance 12 nm diameter InAs Nanowire MOSFETs on Si using an all III-V CMOS process", *Compound Semiconductor Week (CSW)*, May. 2018.

► *I was awarded Best Student Paper Award. This conference was held at Massachusetts Institute of Technology (MIT)*

Paper x: A. Jönsson, J. Svensson, and L.-E. Wernersson, "All-III-V CMOS on Si Using a Self-aligned Gate-last Process", *Swedish Microwave Days*, May. 2018.

Acronyms and Symbols

Here, important acronyms, abbreviations, and symbols are listed, which are recurring throughout the thesis. Some parameters, which only occur in a narrow context, are intentionally omitted; some parameters are used in more than one way, but the context is always explicitly clarified in the corresponding text. Some (compound) units are provided with prefixes to reflect the most commonly encountered notations in the literature.

ACRONYMS AND ABBREVIATIONS

$(NH_4)_2S$	Ammonium Sulfide
1T1R	1-Transistor-1-Memristor
AI	Artificial Intelligence
Al_2O_3	Aluminum Oxide
ALD	Atomic Layer Deposition
ASIC	Application-specific integrated circuits
C_4F_8	Octafluorocyclobutane
CMOS	Complementary Metal-Oxide-Semiconductor
DC	Direct Current
DRAM	Dynamic Random Access Memory
EOT	Equivalent Oxide Thickness
FOx-15	Flowable Oxide 15
GAA	Gate-all-around

GaSb	Gallium Antimonide
H_2	Hydrogen
HCl	Hydrogen Chloride
HEMT	High Electron Mobility Transistor
HfO_2	Hafnium Oxide
HRS	High Resistive State
HSQ	Hydrogen Silsesquioxane
ICP	INductively Coupled Plasma
IL	Interlayer
InAs	Indium Arsenide
InGaAs	Indium Gallium Arsenide
InP	Indium Phosphide
IPC	Instructions per Clock-cycle
LRS	Low Resistive State
MESFET	Metal-Semiconductor Field-Effect Transistor
Mo	Molybdenum
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MOSFET	Metalorganic Vapor Phase Epitaxy
MZMs	Majorana Zero Modes
V-NW	Vertical Nanowire
NW	Nanowire
O_2	Oxygen
PCM	Phase Change Memory
RF	Radio Freqeuncy
RIE	Reactive Ion Etcher
RRAM	Resistive Random Access Memory
SCEs	Short Channel Effects
SF_6	Sulfur Hexafluoride
Si	Silicon
SiO_2	Silicon Dioxide
SOI	Silicon-on-Insulator
SRAM	Static Random Access Memory
SOI	Spin-Transfer Torque Magnetoresistive Random Access Memory

TASE	Template Assisted Selective Epitaxy
TE	Top Electrode
TEM	Transmission Electron Microscopy
TFET	Tunnel Field-Effect Transistor
TiN	Titanium Nitride
TMAH	Tetramethylammonium Hydroxide
TMAl	Tetramethyl Aluminum
VLS	Vapor Liquid Solid
VLSI	Very Large Scale Integrated
W	Tungsten
WZ	Wurtzite
ZB	Zincblende

LATIN SYMBOLS

a_0	m	Lattice Constant
C_g	F	Gate Capacitance
C_{ox}	F	Oxide Capacitance
C_q	F	Quantum Capacitance
E_F	eV	Fermi Level Energy
E_g	eV	Band Gap
f_{max}	Hz	Maximum Oscillation Frequency
f_T	Hz	Transition Frequency
$g_{m,max}$	S/m	Maximum Transconductance
I_D	A, μA$\cdot\mu$m^{-}1	Drain Current, often normalised by the gate width
I_{DS}	A, μA$\cdot\mu$m^{-}1	Source-to-Drain Current, often normalised by the gate width
I_G	A, μA$\cdot\mu$m^{-}1	Gate Current, often normalised by the gate width
$InAs$		Indium Arsenide
I_{on}	A, μA$\cdot\mu$m^{-}1	On-Current, often normalised by the gate width

I_S	A, μA$\cdot\mu$m$^-$1	Source Current, often normalised by the gate width
k_B		$\approx 1.381 \times 10^{-23}$ kg m^2 K^{-1} s^{-1}, Boltzmann Constant
k_{Th}	W/mK	Thermal Conductivity
L_g	m	Gate Length
m_0		$\approx 9.109 \times 10^{-31}$ kg, Electron Rest Mass
m^*	m_0	Effective Mass
q		$\approx 1.602 \times 10^{-19}$ C, Elemental Charge
R_D	Ω, $\Omega \cdot \mu$m	Drain Resistance, often normalized by the gate width
R_{on}	Ω, $\Omega \cdot \mu$m	On-Resistance, often normalized by the gate width
R_S	Ω, $\Omega \cdot \mu$m	Source Resistance, often normalized by the gate width
R_{SD}	Ω, $\Omega \cdot \mu$m	Source & Drain Resistance, often normalized by the gate width
SS_{lin}	mV/dec	Minimum Linear Subthreshold Swing
SS_{sat}	mV/dec	Minimum Saturated Subthreshold Swing
T		Transmission
	s	Propagation Delay
v_{inj}	cm/s	Carrier Injection Velocity
V_{DS}	V	Drain-to-Source Voltage
V'_{DS}	V	Effective Drain-to-Source Voltage
V_{GD}	V	Gate-to-Drain Voltage
V'_{GD}	V	Effective Gate-to-Drain Voltage
V_{GS}	V	Gate-to-Source Voltage
V_T	V	Threshold Voltage
x		Generic Latin Symbol

GREEK SYMBOLS

α	eV^{-1}	Non-Parabolicity Factor

κ		Relative Permittivity
λ_0	m	Mean Free Path
λ_n	m	Natural Length Scale
μ_e	cm^2/Vs	Electron Mobility
μ_h	cm^2/Vs	Hole Mobility
ϕ	rad	Phase

FUNCTIONS AND OPERATORS

$\mathbf{ln}(\cdot)$	Natural Logarithm
$\mathbf{sin}(\cdot)$	sine

INTRODUCTION

1

Background

The global semiconductor sales revenue is upwards to 509 billion USD as of 2020 and is expected to continue to grow steadily. Soaring demands for consumer electronics, such as personal computers and lately smartphones, has traditionally pushed the industry forward. However, the need for consumer electronics is expected to saturate and instead newer applications will expand the industry. Among these emerging technologies are Internet of Things, cloud computing and most importantly products based around AI and 5G networks. The proliferation of applications thus lead to new opportunities for specialized hardware to meet the demands. Notably, the bulk of the industry's revenue originates mainly from digital logic processors, where the metal-oxide-semiconductor field-effect transistor (MOSFET) remains the most important and fundamental device. [1]

Gordon Moore published his prediction in 1975 which described a doubling of transistor density per year enabled by downscaling of the MOSFET device. This was incentivized by decreased power dissipation at greater speed when shrinking the physical dimensions of the transistor, an effect traditionally known as *Dennard* Scaling. This has led to more performance per dollar for every subsequent generation which means that *Gordon Moore's* predictions where in fact a financial observation. [2] Dennard scaling led to ever increasing clock speeds up until 2002 when Si complementary metal-oxide-semiconductor (CMOS) technology entered the era of power constricted scaling where power density reached 100 W/cm^2. [3] From this point on, clock speed increase became stagnant and performance improvements were instead pursued by introducing multi-core CPUs, first described by *Gene Amdahl* in 1967. [4]. This approach relies heavily on parallelization of tasks, which ultimately limits the applications of multi-core systems. However, massive

graphical calculations, performed in a GPU, and training of artificial neural networks (ANN) are tasks that greatly benefit from parallel computation. [5]

Typically cost of manufacturing a wafer has remained constant up until 2015, where increased complexity, due to transistor metal routing requiring more layers, could be balanced by increased wafer sizes. [6] As of 2015 every next-generation CPU, from 16 nm down to 5 nm node size, has been more expensive than its predecessor. Considering both the termination of Dennard Scaling and steeper prices for newer nodes, the marketplace for advanced processing chips has been redrawn. Namely, general purpose chips are becoming less attractive as compared to application-specific integrated circuits (ASICs). The computing premium attained with specialized chips were typically quickly erased by the performance gain caused from every next-generation CPU. In other words, the steep design costs for ASICs was previously never recouped, which is not the case anymore. [7] Therefore, we have now entered the era of specialized chips, also translating to specialized hardware. This development allows for new transistor architectures using novel materials to co-exist and to be co-integrated with traditional Si CMOS.

1.1 TRANSISTOR EVOLUTION

Improved performance in digital applications is no longer attained by increased clock speeds, which is attributed to non-scalable effects such as threshold voltage scaling, leading to a minimum supply voltage of about 1 V (down to 0.7 V) in Si CMOS technology (high-performance optimized transistors). [8] Considering stagnant clock-speeds, improved performance is instead attained by an increase in instructions per clock-cycle (IPC). This is essentially achieved by greater parallelization of tasks, thus fundamentally limited by transistor density to achieve performance gains. The performance in MOSFETs for digital applications are constricted by static power dissipation which further limits the scaling of supply voltage. However, for transistors optimized for analog radio-frequency (RF) applications, device density and static power dissipation are not key factors. Instead, current gain and lowered parasitic capacitances govern the performance for RF transistors. This gives more degrees of freedom when designing the optimal RF devices, including implementation of new channel materials such as narrow bandgap III-Vs.

1.1.1 DIGITAL APPLICATIONS

The gate-length of state-of-the-art MOSFETs is approaching few nm, leading to fundamental limitations with respect to quantum mechanics such as tunneling effects as well as diminished electrostatic control over the transistor

gate. The decreased efficiency of gate electrostatic control is referred to as Short Channel Effects (SCEs), and include e.g. drain induced barrier lowering, subthreshold slope degradation and threshold voltage roll-off. Onset of SCEs contradict the established trends, thus continued down-scaling lead to increased power dissipation. A solution to combat these modern scaling effects has been to incorporate various multi-gate structures, where the transistor has evolved from planar architecture into three-dimensional tri-gate and vertical gate-all around (GAA) channel MOSFETs, see Figure 1.1. Planar architectures have also been developed further, achieving improved electrostatics by e.g. silicon-on-insulator (SOI) adaptation (Figure 1.1-a), where ultra-thin planar semiconductor channels can be realized (<6 nm). [9, 10] The tri-gate architecture (Figure 1.1-b) was already introduced by *Intel* in 2012 for their 22 nm node technology, which demonstrated 37% improved performance at 50% lower power dissipation compared to its contemporary planar version. [11,12] However, the GAA architecture (Figure 1.1-c & d) has yet to be adopted for digital applications, even though it provides the ultimate electrostatic control. [13] The evolution from planar to tri-gate architectures (including stacked nano-sheets) has carried over many traditional 2D lithography techniques, which is not possible to the same extent when incorporating vertical GAA technologies. Namely, reliable fabrication methods must be developed to attain high-resolution lithography within the vertical direction, while enabling design flexibilities such as varied gate-length, strain-engineering and threshold voltage control.

Various technology boosters have continued the MOSFET performance improvements for very large-scale integrated (VLSI) circuits, independent of geometrical scaling. Among the main innovations are strained silicon and high-κ dielectrics that has led to circuit performance improvements. Substituting the oxide, traditionally constituted by SiO_2, at the gate-stack level using high relative permittivity (κ) dielectrics such as HfO_2 or Al_2O_3 has circumvented current leakage issues related to quantum tunneling. Thus high-κ dielectrics has allowed similar oxide capacitance when incorporating a thicker dielectric as compared to SiO_2, where a 6.4 nm thick HfO_2 film is equivalent to a 1 nm SiO_2 film (planar gate-stack). Strained channel materials have enabled improved charge carrier transport properties (mobility) within the channel, engineered to co-inside with the orientation in line with the direction of the current. For Si MOSFETs mobility enhancement factors, over bulk Si, of ~ 2 for electrons and up to ~ 10 for holes has been demonstrated, thus balancing the performance discrepancy typically found between p- and n-type digital MOSFETs. Strained channel materials can be attained by e.g. growing a thin lattice mismatched layer on top of a substrate, which is a reoccurring technique in SOI technology. [17]

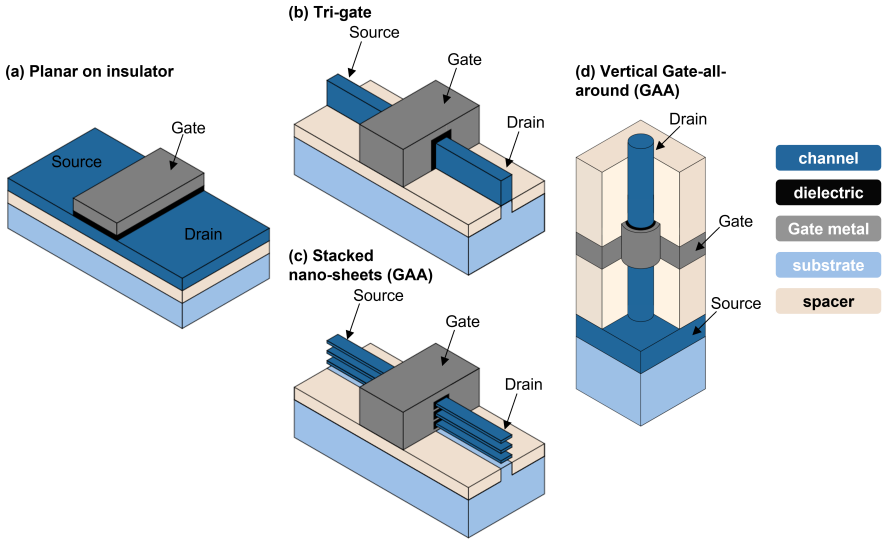

Figure 1.1: Schematic representation of modern transistor architectures varying from planar to 3d integration. (a) Planar on insulator devices are commercially available as fully depleted silicon-on-insulator (FDSOI) technology. (b) Tri-gate architecture is found in all modern Si CMOS technology nodes for digital applications. (c)-(d) Gate-all-around technology providing ultimate electrostatic control for increased scalability. Here stacked nanosheets (c) represent the evolution of the tri-gate architecture, where *IBM* has introduced commercial stacked nanosheet transistors (also coined as ribbonFET by *Intel*), with 12 nm gate-length, for use in 2 nm node logic processors. [14, 15] Vertical GAA architectures (d) are projected for future use, 2030 and beyond, according to International Roadmap for Devices & Systems (IRDS) 2020 report [16].

1.1.2 III-V MOSFETS FOR RF APPLICATIONS

Looking beyond the limitations of Si there are many promising material alternatives, especially attractive are the III-V compounds with their direct bandgap and excellent transport properties, see Table 3.3. High mobility μ of charge carriers enables ballistic transport for short channel (<100 nm) transistors, where no scattering events occur within the channel-region. Thus, the performance is governed by the carrier injection velocity v_{inj}, which ultimately boosts transistor currents further. [18] The ternary compound InGaAs has had considerable success for high frequency RF optimized transistors, due to high electron mobility μ_e as well as compatibility with well-established InP wafers. [19] Notably, InAs and GaSb provide high bulk mobility for electrons

μ_e and holes μ_h, respectively. The material combination of InAs-GaSb can also provide abrupt and crystalline heterojunctions due to matching lattice constants between the compounds. [20] Furthermore, for VLSI compatibility various buffer layers for integration on Si are typically employed, therefore self-heating effects need to be considered. Here, the ternary III-Vs typically showcase significantly lower heat conductivity k_{Th} compared to its binary counterparts and also Si (Table 3.3). [21] Also, for scaled devices optimized for logic, the transistor drive current I ultimately determine the switching speed, where I is proportional to both mobility and effective mass $I \sim m^* \cdot \mu$. A large effective mass (translating to large density of states) therefore compensates for lower mobility in scaled digital devices. However, for RF devices where a high transition frequency f_T is coveted, low capacitance are pursued. Considering intrinsic gate capacitance C_{gg} and transconductance g_m, the transition frequency can be described as $f_T \propto g_m/C_{gg} \sim \mu$ (m^* cancel out). Thus, high mobility is vital when pursuing devices optimized for high frequency RF applications. [22]

Table 1.1: Transport properties and thermal conductivity k_{Th} of various III-V materials compared to Si. Where v_{inj} is the injection velocity, m^*/m_0 effective electron mass (fraction of electron mass), a_o the lattice constant, as well as μ_e and μ_h representing the bulk electron and hole mobility, respectively. Furthermore, the lattice matched III-Vs are highlighted. ^{A}$In_0.53Ga_47As$ composition. ^{B}Heavy hole effective mass. [21,23,24]

Material	E_g [eV]	μ_e [cm^2/Vs]	μ_h [cm^2/Vs]	v_{inj} [cm/s]	m^*/m_0	a_0 [Å]	k_{Th} [W/mK]
Si	1.12	1400	400	$2.3 \cdot 10^5$	0.26	5.43	148
InAs	0.35	13000	500	$7.7 \cdot 10^5$	0.023	6.09	26.5
GaSb	0.73	3000	1000		0.4^B	6.09	33
$InGaAs^A$	0.74	12000	300	$7.7 \cdot 10^6$	0.043	5.86	∼5
InP	1.34	5400	200		0.08	5.86	68

III-V based devices have had considerable success for use in high frequency applications by commercially available high-electron-mobility transistors (HEMTs). State-of-the-art HEMTs have achieved transition frequencies (f_t) up to 710 GHz (InAs channel) [25] and maximum oscillation frequencies (f_{max}) up to 1.5 THz (InP channel) [26]. The basic principle of these devices is the high electron mobility in the remotely doped channel material (δ-doping), usually consisting of III-V compounds, to achieve low RF noise and excellent gain for high frequency operation. In contrast to MOSFET devices

the HEMTs substitute the gate-oxide with a thin high-bandgap semiconductor barrier. This method circumvents the many detrimental issues regarding the III-V/oxide interface, typically leading to reduced reliability and increased current noise. [27] Ultimately, using a semiconductor barrier means poor electrostatic control and lower intrinsic gate-capacitance, which has led to stagnated gate-length scaling limited to 20 nm for HEMTs. [22] MOSFET implementations offer further scalability, where state-of-the art III-V and Si CMOS based high frequency devices have provided f_t/f_{max} of about 400/400 GHz. [11, 28–33]

1.2 III-SB BASED ELECTRONICS - P-TYPE MOSFETS AND BEYOND

Nanoscaled III-Sb devices have experienced a surge of interest due to its usefulness in various applications, such as optolectronics, tunnel FETs and recently topological superconductors. The III-Sb group of materials share the same qualities as other III-V material, where specifically InSb has proven to be useful due to its extremely narrow bandgap (0.17 eV) as well as providing a high g-factor, which is a measurement of quantization efficiency of spin states with applied magnetic field. Thus, it has been reported that InSb is used as a platform for study of Majorana Zero Modes (MZMs) which might lead to the realization of topological quantum computations. [34]

III-V based MOSFETs in general have demonstrated strong n-type performance, however for digital applications robust p-type performance is also vital for realizing Complementary Metal-Oxide-Semiconductor (CMOS) circuits. The most promising option for p-type MOSFETs using III-V compounds are GaSb and InGaSb which demonstrate high bulk mobility for holes. The transport properties can also be further boosted by introduction of compressive strain, which is also employed to improve modern Si p-type MOSFETs. This can be done by employing external stressors or utilizing lattice mismatch between heterostructures. Induced strain in (In)GaSb promotes splitting of the valence bands corresponding to heavy- (hh) and light-holes (lh), where the mobility of the hh improve vastly. By employing a 2% compressive strain an effective hole-mobility of 1500 cm^2/Vs have been demonstrated for InGaSb thin films. [35, 36]

Various challenges for incorporating III-Sb materials remain when considering etch selectivity and oxidation properties. GaSb specifically has been reported to be etched in water [37], which adds to the complexity of fabricating nanoscale structures based on antimonides. Also, surface effects such as roughness and gate-oxide interface defects have proven to be detrimental for nanowire-based applications, where deteriorated hole transport properties for down-scaled diameters (< 40 nm) are commonly observed. [38]

However, recent advances in growth methods employing template-assisted selective epitaxy (TASE) have demonstrated hole mobility of 760 cm^2/Vs (hall measurements), remarkably close to the bulk mobility (see 3.3), for nanostructures with critical dimensions down to 20 nm.

1.3 MEMORY ARCHITECTURE – IN MEMORY COMPUTATION

Traditional computing systems are typically built based on the von Neumann architecture where memory blocks and processing units are separate entities. Computational tasks therefore require data to be transferred back and forth between the processing and memory units which introduce increased latency and energy dissipation due to power hungry metal interconnect lines/busses. For modern workloads, such as machine learning, the exchange of massive volumes of data is especially prevalent. Thus the performance is severely bottle-necked by slow read/write memory speed, which can be partly mitigated by on-chip integration of memory (near-memory computing [39]) and parallelization. However, the Processor-Memory performance disparity, represented by CPU vs Dynamic Random Access Memory (DRAM) units, has increased by 50% each year, rendering von Neumann based systems insufficient for future AI applications. [40]

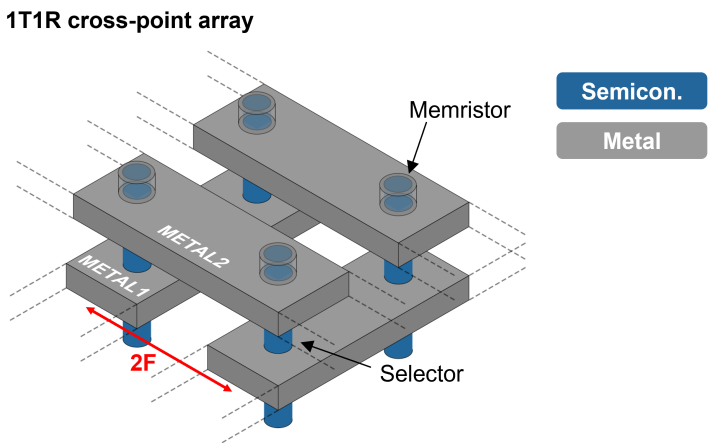

Figure 1.2: Schematic of a dense crossbar array consisting of one 1T1R memory cell at each metal line intersection. Here METAL1 and METAL2 contact the selector and memristor, respectively. The distance between metal lines (center to center) represents twice the minimum feature size 2·F, thus the unit cell area is $4F^2$.

To overcome this so-called memory wall arising from von Neumann based systems, alternative approaches such as in-memory computation have been proposed. Here, the calculation task is performed within the memory itself, thus CPU and memory units are conjoined, which is an attribute shared with the biological properties of a mammalian brain, increasing computational efficiency drastically. Therefore, new memory devices are required to properly facilitate in-memory computation, where Resistive Random Access Memory (RRAM), Spin-Transfer Torque Magnetoresistive RAM (STT-MRAM) and Phase Change Memory (PCM) are promising technologies. [41]

Dense cross-point arrays of parallel memory cells need to be incorporated to support high bandwidth data traffic necessary for modern workloads, see Figure 1.2. Incorporating memory selectors, for every memory cell, expand the maximum array size vastly due to lowered leakage currents originating from half- and unselected cells. [42] Memory selector architectures can be based on both two and three terminal devices, where the selector can e.g. consist of a diode or transistor in parallel with a memristor. Using a transistor adds routing complexity which can be greatly mitigated using a vertical architecture where contact layers are inherently separated. A vertical structure also enables a memristor to be stacked directly on top of a transistor (1T1R cell) with a mininmal footprint of $4F^2$ (Figure 1.2). Particularly, RRAM requires high drive currents and tunable compliance current level to enable stable operation. [43] State-of-the-art vertical III-V MOSFET technology enables sufficient currents (transconductance >3 mS/um) at low supply voltages [44] to drive, and form, RRAMs while maintaining low off-state leakage currents (down to 1 nA/um) [45].

1.4 MY CONTRIBUTION - MOTIVATION

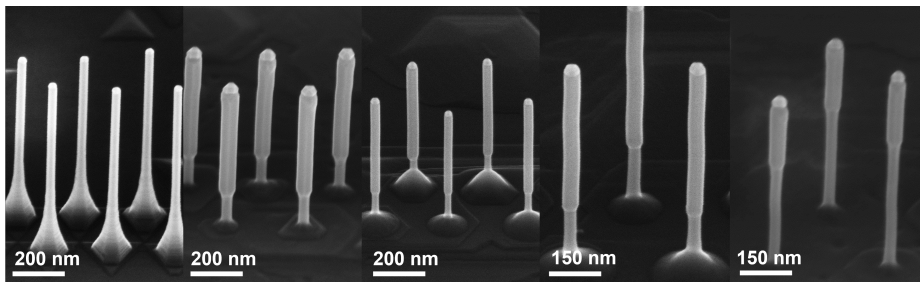

Figure 1.3: A collage of sweeping electron microscopy (SEM) pictures of various vertical nanowires, based on InAs, InGaAs and GaSb, used in this thesis. More information regarding these structures will be disclosed in later chapters.

The overarching theme of this thesis is various co-integration techniques by utilizing the inherent benefits of the vertical narrow-gap (E_g < 1 eV) III-V nanowire based architecture for MOSFETs. We employ epitaxially grown nanowires (bottom-up approach), see Figure 1.3, in our electrical devices providing the following advantages [20, 45–48]:

- III-V integration on Si
- Low thermal budget (growth < 450^o C)
- Bandgap engineering for heterostructure design to boost device performance
- Core-shell integration for δ-doping and improved contacts
- Small footprint, and nucleation point, to minimize defect propagation and various crystal defects
- *In-situ* doping, reducing mask steps associated with e.g ion implantation

Therefore, this thesis aims to utilize these benefits, adapting them towards III-V based CMOS, RF and memory applications by developing various fabrication techniques. In order to provide competitive performance and to push the envelope of III-V based MOSFETs many techniques, and standalone studies, are employed to characterize both channel, oxide and contacts.

2

Nanowire MOSFET Theory

2.1 MOSFET CHARACTERIZATION

Various performance metrics for MOSFETs are typically derived by measuring transfer and output characteristics as shown in Figure 2.1. Currents are normalized by the width of the gate which corresponds to circumference of the nanowire channel in vertical GAA nanowire MOSFETs. Essentially these measurements capture the behavior of the current I_D passing through the channel with respect to biasing conditions at steady state. The transfer characteristics are measured at a constant V_{DS} while sweeping the gate-voltage V_{GS}. Therefore, this measurement depicts the efficiency of the gate-electrode. The transfer characteristics are further divided, by the threshold volage V_T, into the subthreshold (off-state) and on-state region. Two important metrics derived from the V_{GS} sweep is subthreshold swing (SS) and transconductance, which are deduced from the subthreshold and on-state regions, respectively. The subthreshold swing SS is determined from the inverse of the slope $(\partial \log I_D/\partial V_{GS})^{-1}$, in logarithmic scale, within the off-state region and is defined as the voltage required to change the current one decade, below the threshold voltage. Similarly, the transconductance g_m is acquired as the slope $\partial I_D/\partial V_{GS}$ within the on-state (linear scale) and provides the number of amperes delivered per volt (siemens). These metrics are of great importance for digital applications which require high on-currents I_{on} delivered at low supply voltage V_{DD} for reduced propagation delay t_p according to

$$t_p = \frac{C_L V_{DD}}{2 I_{on}} \tag{2.1}$$

where C_L is the load capacitance. Here a reduced propagation delay allows for operation at increased clock-frequencies. Also, dynamic power dissipation

P_D requires a decreased V_{DD} and has a squared dependence of drive voltage ($P_D \sim V_{DD}^2$). However, the voltage operation window (Figure 2.1-a) must be designed to avoid large static power dissipation P_S when biased at the off-state. Namely, the P_S has a linear dependence on the off-state current I_{off} ($P_D \sim I_{off}$) thus requiring $I_{off} < 100$ nA/μm. Three different I_{off} limits have therefore been defined; 1, 10 and 100 nA which corresponds respectively to low-power, general purpose and high-performance applications. As shown in Figure 2.1-a the supply voltage for III-V MOSFETs can typically be scaled down to 0.5 V, as compared to about 0.7 V (Intel 14-nm node [49]) for high-performance optimized Si CMOS. Furthermore, the on-state is defined at the bias points $V_{DS} = V_{DD}$ and $V_{GS} = V_{OFF} + V_{DD}$, where V_{OFF} is defined as the voltage coinciding with the chosen I_{off} limit. [50]

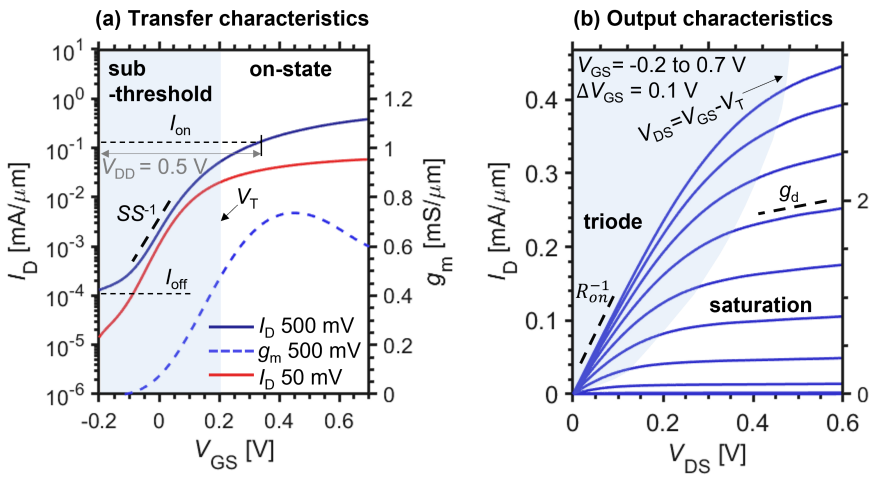

Figure 2.1: (a) Transfer and (b) output characteristics measured from a vertical nanowire III-V (InAs-InGaAs) n-type MOSFET.

The output characteristics are measured at constant V_{GS} while sweeping the gate-voltage V_{DS} as displayed in Figure 2.1-b. The I_{DS} vs V_{GS} sweep is further divided into two regions, triode and saturation. For high frequency operation, a MOSFET is operated within the saturation region where a linear and predictable behavior of the transconductance g_m can be achieved, thus operation will be independent of small variations in DC-bias. Here, the output conductance g_d is defined as the slope of the output characteristics $g_d = \partial I_D / \partial V_{GS}$. An ideal transistor demonstrates $g_d \approx 0$ in the saturation region, whereas a large g_d instead indicate short channel effects or the onset of impact ionization and/or band-to-band tunneling. [51] g_d at saturation is

especially important for RF applications where the intrinsic voltage gain A of the device scales with g_m according to $A = g_m/g_d$. The inverse output conductance at large gate-bias for $V_{DS} \rightarrow 0$ V represents the on-current R_{on}, which is constituted of access resistances R_A and channel resistance. The R_{on} metric can therefore give an approximate value of external resistances of the device.

2.2 DRIFT DIFFUSION & BALLISTIC TRANSPORT

The current passing through the MOSFET channel, considering drift-diffusion operation, can be described as

$$I_D = \frac{W}{L} C_g \mu_0 \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right) \tag{2.2}$$

within the linear operation region ($V_{DS} < V_{GS} - V_T$). Here W and L constitutes the channel width and length respectively, C_g total gate capacitance, and μ_0 mobility of the charge carriers. Gate capacitance C_g is constituted by the quantum capacitance C_q, charge centroid capacitance C_c, and oxide capacitance C_{ox} in series. Shrinking the gate-length, considering constant drain-source bias, leads to increased electric potential translating to greater drift-velocity of the charge carriers. However, at high electric fields the drift-speed tend to saturate at a certain velocity v_{sat}. This occurs by the increased scattering rate of highly energetic charge carriers, which is primarily caused by optical phonon emissions. Within the saturation regime ($V_{DS} > V_{GS} - V_T$) the current is independent of V_{DS}, and further considering velocity saturation for short-channel devices the drain-current can be described as

$$I_D = W C_g v_{sat} (V_{GS} - V_T). \tag{2.3}$$

Fundamentally, the transistor gain is governed by the intrinsic channel capacitance and the saturated drift speed. For III-V materials, the direct bandgap and high mobility serves to limit the scattering events within the channel, by greatly increased mean free path λ_0 corresponding to the distance between scattering events. Therefore, short channel III-V MOSFETs typically operate within the ballistic regime, where no scattering events occur in the channel. For ballistic transport, the drain-current can be expressed as

$$I_{D,ballistic} = W C_g v_{inj} (V_{GS} - V_T). \tag{2.4}$$

where v_{inj} is the injection velocity at the source-side and T is the channel transmission. The description of current for velocity saturated and ballistic

devices bear striking resemblance, both are limited by the velocity of the charge carriers and are independent of gate-length. However, in the case of ballistic transport the current is governed by the injection velocity at the source adjacent to the channel. The properties of channel will still influence the device properties by a transmission co-efficient T, dependent on L_G and mean free path λ_0, described as

$$T = \frac{\lambda_0}{\lambda_0 + L_G}. \tag{2.5}$$

Considering the transmission T in conjunction with ballistic transport, the MOSFET current can instead be expressed as

$$I_D = T \cdot I_{D,ballistic}. \tag{2.6}$$

This description is referred to as a quasi-ballistic because the mean free path λ_0 is ultimately governed by channel mobility. [52]

2.3 BALLISTIC MOSFET ELECTROSTATICS

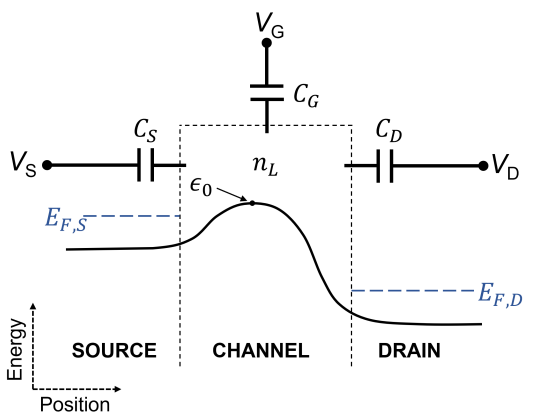

Figure 2.2: Showing the conduction band of an n-type MOSFET, modelled by three capacitors; gate C_G, source C_S and drain C_D capacitance. Namely, the gate, source and drain bias, V_G, V_S and V_D respectively, control top of the barrier ϵ_0 as well as the charge n_L in the channel via their associated capacitors. Moreover, the conduction band is depicted with applied drain-source bias V_{DS} ($V_{DS} = V_D - V_S$) influencing the source $E_{F,S}$ and drain $E_{F,D}$ Fermi-level correspondingly; $-qV_{DS} = E_{F,D} - E_{F,S}$.

In MOSFETs, the current flow is controlled by injection/thermionic emission of charge carriers over a potential barrier. In the case of ballistic transport the injection of charge carriers from the source, over the channel potential barrier and into the drain, is naturally governed by the top of the barrier ϵ_0. Mainly, ϵ_0 is controlled by the gate-voltage V_G, although it is also influenced by the bias conditions at the drain and source. To fully capture the behaviour of the top of the barrier ϵ_0 with respect to bias conditions Poisson's equation need to be solved. However, a simplified three capacitor circuit model, valid for ballistic MOSFETs, can be implemented for intuitive understanding of the electrostatics, see Figure 2.2. The top of the barrier is thus influenced by the drain C_D and source capacitance C_S in addition to the gate capacitance C_G. The potential U_1 at the cross point, when neglecting the free charge carriers n_L can be described by the various capacitance contributions added by superposition

$$U_1 = -q\left(\frac{C_G}{C_{tot}} + \frac{C_S}{C_{tot}} + \frac{C_D}{C_{tot}}\right). \tag{2.7}$$

where C_{tot} corresponds to the parallel coupling between the capacitors $(C_S + C_D + C_G)$. Adding the contributions of mobile charges n_L in the channel and short circuiting the voltage in the model the potential U_2 at the crosspoint can instead be described as

$$U_2 = \frac{q^2}{C_{tot}} n_L. \tag{2.8}$$

Observe that the mobile charges n_L are dependent of the bias conditions, however in the case of 2D density of states (valid for 2DEG devices) the charge remain constant within the channel. Finally, when considering the contributions of U_1 and U_2 as well as optimized MOSFET design ($C_G \gg C_D, C_S$) the top of the barrier can be described as

$$\epsilon_0 = U_1 + U_2 = -qV_G + \frac{q^2}{C_G} n_L. \tag{2.9}$$

Specifically for a cylindrical geometry, valid for nanowire MOSFETs, the oxide capacitance, corresponds to C_G and can be calculated as

$$C_G = \frac{2\pi\varepsilon_{ox}}{\ln \frac{t_{ox}+r_{nw}}{r_{nw}}} \tag{2.10}$$

where ε_{ox} is the oxide permittivity, r_{nw} the nanowire radius, t_{ox} oxide thickness. III-V based MOS stacks exhibit comparably low density of states, consequently when scaling the dimensions, the contribution from U_2 will

be negligible. Thus, the requirement for the quantum capacitance limit is fulfilled (QCL), which translates to all the voltage drop occurring solely over the semiconductor, meaning that the gate-bias will directly control the energy bands within the channel as $\epsilon_0 = -qV_G$ considering (2.9). Therefore, the oxide down-scaling (physical and/or permittivity) is only meaningful up until a certain point for channels with heavily scaled dimensions. [53, 54]

2.4 NANOWIRE MOSFET MODELING

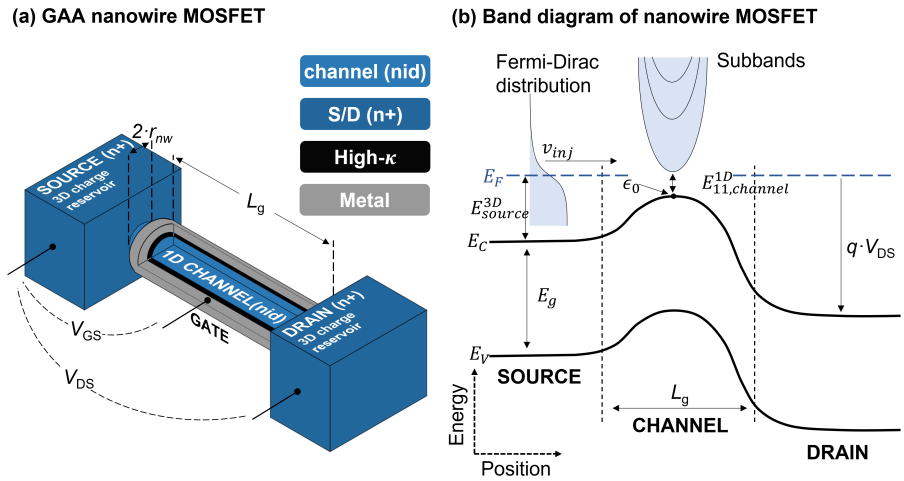

Figure 2.3: (a) Schematic representation of generic nanowire MOSFET with a gate-all-around electrode, also providing a cut-through segment to expose the nanowire channel described by 1D transport properties. Here V_{GS} and V_{DS} are the gate-source and drain-source voltages respectively, r_{nw} the nanowire radius and L_g the physical gate-length. (b) Representative energy landscape of the proposed nanowire geometry with conduction band E_C, valence band E_V and bandgap E_g represented. Here the electron populations are highlighted, where they are described by a 3D Fermi-Dirac distribution and quantized subbands in the source and gate regions, respectively. When the device is biased at the on-state, high E-field at the drain side, the source facilitates the major contribution to the current, thus the current is governed by the charge at the source-side and carrier injection velocity v_{inj}. $E^{1D}_{11,channel}$ represents the energy difference between the first subband and top of the barrier ϵ_0 within the gate. Also, the Fermi-level position at the source side is E^{3D}_{source} and is described by 3D density-of-states statistics.

When focusing on nanowire based architectures, the most reccuring geometry employs small critical dimensions within the channel region (diameter < 25 nm), with comparably large contacts acting as charge reservoirs. These assumptions are applicable to state-of-the-art MOSFETs using various gate-replacement techniques [55–59] as well as vertical nanowire transistors employing selective recess etching of the channel region [44, 46]. Figure 2.3 provides an overview of the traditional nanowire based architechture, with corresponding energy landscape across the MOSFET terminals. The device is described by charge reservoirs with an intermediate 1D channel. Thus, to fully describe the device properties, different charge carrier distributions and corresponding transmissions need to be accounted for between the various geometries. The remainder of the chapter aims to facilitate modelling and optimization of such a device by describing both intrinsic and extrinsic effects.

2.4.1 INTRINSIC TRANSPORT PROPERTIES & COMPACT MODELING

For III-V based short channel devices (< 100 nm), using e.g. InGaAs or InAs, quasi-ballistic transport describes the MOSFET properties accurately. Considering the geometry in Figure 2.3 and III-V materials, the drain current I_{DS} in a top of the barrier controlled device can be described as

$$I_{DS} = \frac{2q}{h} \int_E T(E)M(E)(f_s(E) - f_d(E))dE. \tag{2.11}$$

where $f_s(E)$ and $f_d(E)$ are the equilibrium Fermi functions in source and drain respectively, $T(E)$ is the transmission and $M(E)$ the available current-carrying subbands within the channel (all variables are dependent on energy E, q and h are physical constants). Essentially the current is constituted by the carriers injected into the channel from source and drain, respectively, $f_s(E) - f_d(E)$ where the available current-carrying energy states $M(E)$ inside the channel acts as a filter. $M(E)$ is thus constituted by the maximum supported charge within the channel and is dependent on 1D density of states $D_{1D}(E)$, gate-length L_g, and injection velocity $v_{inj}(E)$ according to

$$M(E) = L_g \frac{h}{4} v_{inj}(E) D_{1D}(E), \text{ where } D_{1D}(E) = \frac{2}{h}\sqrt{\frac{2m^*}{E - \epsilon_o}} \tag{2.12}$$

Here, D_{1D} is dependent on effective mass m^* and the top-of-the-barrier energy ϵ_0 in the electrostatically controlled channel. Assuming a perfect electrostatic gate, with small capacitance contribution from source and drain (valid for GAA structure), and operation within the QCL-limit the top of the barrier ϵ_0 will be directly controlled by the applied gate-bias V_{GS} as $\epsilon_0 = -qV_{GS}$ (see section 2.3).

In addition to equation (2.5), the transmission $T(E)$ can be more accurately described with effective channel length L_{eff} as follows

$$T = \frac{\lambda(E)}{\lambda(E) + L_{eff}}, \text{ where } L_{eff} = \begin{cases} L_g & \text{small } V_{DS} \\ \frac{k_B T}{q} \frac{1}{V_{DS}} & \text{large } V_{DS}. \end{cases} \tag{2.13}$$

Here, $(k_B T)/q$ constitutes the thermal voltage and V_{DS} the drain-source voltage. Essentially, larger V_{DS} increase the penetration of the high-field region into the channel and increases transmission $T(E)$ significantly by lowered probability of back-scattering. [60]

For device evaluation and circuit design, a compact model can be developed considering the previously discussed physics regarding ballistic transport in (2.11) [61]. This model manages to capture the essentials of ballistic transport by considering the charge at the source-side Q_{x0} and a constant injection velocity $v_{inj,VS}$ (at energy level corresponding to ϵ_0) at the source according to

$$I_D = W Q_{x0} v_{inj,VS} F_s, \tag{2.14}$$

with the addition of the device width W and a smoothing function F_s. The smoothing function F_s is used to capture all modes of operation (linear to saturation, Figure 2.1). Comparing it to (2.11) when biased at the on-state (no drain influence, neglected f_d), Q_{x0} can be described as

$$Q_{x0} = -q \int_E D_{1D}(E) f_s(E) dE \approx n C_{inv} (V_{GS} - V_T)^{\alpha} \tag{2.15}$$

where C_{inv} constitutes the on-state gate capacitance, n the subthreshold swing ideality and additionally α is a fitting factor. The described model is referred to as the virtual source model, where device behaviour is centered around the charges at the source with their corresponding injection velocity $v_{inj,VS}$. The virtual source model is semi-empirical, meaning it mainly employs physical parameters, thus can be useful for extracting physical properties of a device. [60] In Figure 2.4 Applying the virtual source model (2.14) to a vertical nanowire based InAs device gives a good fit, and yields a corresponding injection velocity of $3.5 \cdot 10^5$ m/s. Note that extrinsic source and drain resistance, R_S and R_D, has to be considered for calculation of intrinsic device properties (see section 2.4.4).

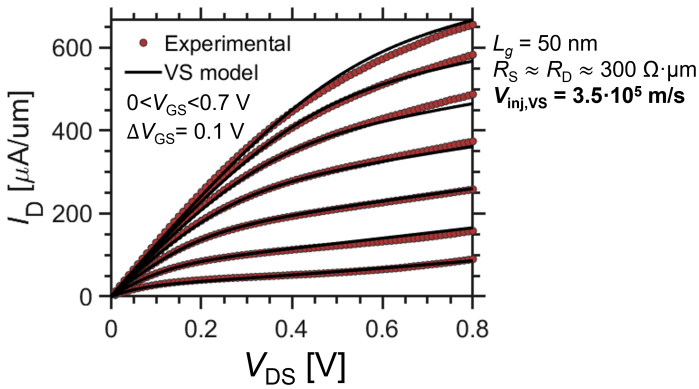

Figure 2.4: Experimental data of n-type vertical nanowire III-V MOSFET (InAs channel) with fitted virtual source model desribed in (2.14).

2.4.2 NATURAL LENGTH SCALE

When pursuing increased performance by scaled channel dimensions, such as minimizing the gate-length L_g, certain design requirements need to be fulfilled in order to avoid detrimental SCEs. Here, the influence of the electric potential from the source and drain contacts on the gate-region is quantified by the natural length scale λ_n which describes the length of the electric field penetration depth into the channel. The requirement

$$L_g \geq 5\lambda_n \tag{2.16}$$

need to be maintained to avoid subthreshold slope degradation and DIBL. For a cylindrical geometry, the natural length scale is calculated as follows

$$\lambda_n \approx \sqrt{\frac{2\varepsilon_c r_{nw} \ln\left(1 + \frac{t_{ox}}{r_{nw}}\right) + \varepsilon_{ox} r_{nw}^2}{4\varepsilon_{ox}}} \tag{2.17}$$

where ε_c and ε_{ox} is the permittivity of the channel and oxide respectively, t_{ox} is the thickness of the oxide, and r_{nw} the nanowire radius. [62] Figure 2.5 shows experimental data, gate-length L_g vs current modulation I_{on}/I_{off}, for p-type GaSb nanowire based MOSFETs. Here the relation of $L_g \geq 5\lambda_n$ can be confirmed, where modulation improves due to less SCEs at gate-lengths longer than 75 nm ($\lambda_n = 15$ nm).

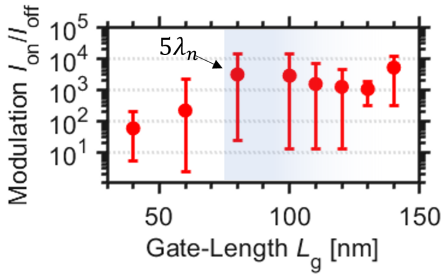

Figure 2.5: Experimental data showing current modulation, represented by I_{on}/I_{off} ratio, vs gate-length of p-type GaSb nanowire MOSFETs. Here I_{on} is defined at $V_{GS} = -1$ V and I_{off} at $V_{GS} = 0.5$ V. The nanowire device has a high-κ with EOT of 1.9 nm and a channel radius $r_{nw} = 12$ nm resulting in a natural length scale λ_n of about 15 nm.

2.4.3 THRESHOLD VOLTAGE MODELLING

To minimize power dissipation and ensure low-voltage operation in CMOS circuits the threshold voltage V_T discrepancy between the n- and p-type MOSFETs need to be minimized. [63] MOVPE grown III-V MOSFETs typically demonstrate a large V_T-spread which makes them less compatible for digital applications. [64] In order to improve V_T stability for n-type III-V nanowire MOSFETs, models describing the threshold voltage behavior with respect to scaling as well as dopant concentration are coveted. Here, we present theory describing the threshold voltage V_T for n-type cylindrical III-V nanowire MOSFETs focusing on the effect of varying dopant concentration as well as quantum confinement. For all models fully ionized donor states are assumed, which is reasonable at room temperature (RT).

Due to charge conservation the depletion based threshold voltage $V_{T,dep}$ can be deduced from depletion of free charge carriers within the channel. Thus, a linear behavior with respect to channel donor concentration $N_{D,channel}$ is attained as follows

$$V_{T,dep} = V_{fb} - qN_{D,channel}K \tag{2.18}$$

where V_{fb} is the flatband voltage (fitting factor), q the elementary charge and K contains all physical parameters according to

$$K = \frac{r_{nw}^2}{4\varepsilon_{ox}} \ln\left(1 + \frac{t_{ox}}{r_{nw}}\right) + \frac{r_{nw}^2}{64\varepsilon_c}. \tag{2.19}$$

Here, ε_c and ε_{ox} represents the permittivity of the channel and oxide respectively, t_{ox} oxide thickness, and r_{nw} the channel thickness. Observe that

the depletion model results in squared dependence of nanowire radius $\sim r_{nw}^2$ for larger structures ($r_{nw} \gg t_{ox}$). This model is derived from calculating the nanowire central potential assuming a doped channel and parabolic bands. [65, 66] Instead, considering a one-dimensional scaled channel with comparably large contacts, acting as electron reservoirs (degenerated semiconductors), the confinement effects only occur within the channel region. Representing a 3D-1D-3D (source-gate-drain) transistor geometry, Figure 2.3, the threshold voltage $V_{T,q}$ dependence can instead be described by

$$V_{T,q} = V_{fb} - \frac{\Delta E_{source}^{3D}}{q} - \frac{\Delta E_{channel}^{1D}}{q} \tag{2.20}$$

where ΔE_{source}^{3D} represents the fermi level on the source side and $\Delta E_{channel}^{1D}$ the position of the first subband within the 1D channel. Considering hard wall confinement and non-parabolic bands the position of the first subband can be calculated as

$$E_{11,channel}^{1D} = \frac{\sqrt{1 + \frac{\alpha \hbar^2 \pi^2}{2 r_{nw}^2 m^*}} - 1}{2\alpha} \tag{2.21}$$

for which α (~ 2.7 for InAs) represent a non-parabolicity factor, and m^* the bulk effective mass. [45] The position of the fermi level at the source ΔE_{source}^{3D} can be described by using the Fermi-Dirac F_n integral of order $n = 1/2$ but can also be calculated using approximations according to

$$E_{source}^{3D} = \frac{N_{D,source}}{N_C} \frac{1}{F_{1/2}} \approx k_b T \ln \frac{N_{D,source}}{N_c} \frac{1}{\left(64 + \frac{3.6 N_{D,source}}{N_C}\right)} \tag{2.22}$$

where k_b is boltzmanns constant, T the temperature (at RT $k_b T \approx 26meV$), and N_c the effective density of states for electrons (for InAs $N_c \approx 8.7 \cdot 10^{16}$ cm^{-3}). Notice that the two different models, in (2.18) & (2.21), capture different effects and complement each other. The depletion model (2.18) originate from the free charges within the channel, and is mainly valid for relatively large density of states and non-degenerate statistics. (2.21) considers the specific geometry in Figure 2.3, with corresponding band alignment, accounting for quantization and density of states at the source. Figure 2.6 depicts the diameter dependence $2 \cdot r_{nw}$ with respect to the different models, where quantization effects dominate for diameters < 15 nm. For long channel MOSFETs, effects from both quantization and free charge carriers should be considered.

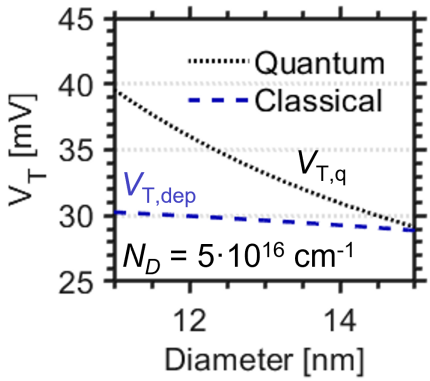

Figure 2.6: Comparison between the classical depletion model (2.18), considering displacement of free charges within the channel, and quantization effects in a 1D channel (2.21). Quantization is calculated considering the physical properties of InAs.

2.4.4 EXTRINSIC MOSFET CONTRIBUTIONS

To accurately model a MOSFET device, parasitic contributions need to be accounted for. Figure 2.7 represents the various parasitic capacitances and resistances in addition to the intrinsic three terminal MOSFET (Figure 2.7-a) as well as for a vertical nanowire based device (Figure 2.7-b). The nanowire schematics illustrates the design challenge for RF devices where lower access resistance tend to form larger gate-overlap capacitance, due to smaller physical separation of the contact layers.

Due to extrinsic resistance, the applied gate-source V_{GS} and drain-source voltage V_{DS} is shared by the intrinsic device as well as the access resistance originating from source R_S and drain R_D according to the following equations

$$V'_{GS} = V_{GS} - I_D R_S \tag{2.23}$$
$$V'_{DS} = V_{DS} - I_D(R_S + R_D). \tag{2.24}$$

Here, V'_{GS} and V'_{DS} are the effective gate-source and drain-source voltages respectively, and I_D is the drain current. Accurately modelling the addition of access resistance thus require an iterative method. Furthermore, the influence on extrinsic transconductance g_m (quasi-static) in relation to parasitic resistance can be described as

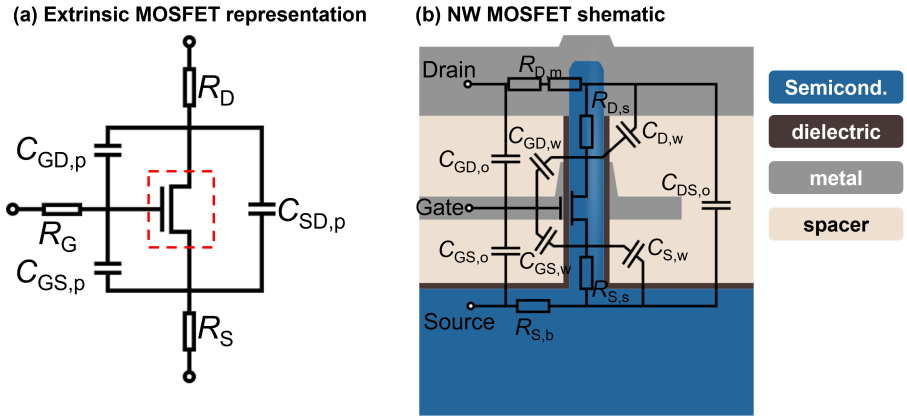

Figure 2.7: (a) Circuit diagram representing the extrinsic MOSFET including the intrinsic device (red highlight) with the parasitic capacitances and resistances. Here Rs, Rd and Rg are the source gate and drain resistances, while $C_{GS,p}$, $C_{GD,p}$ and $C_{SD,p}$ represent the parasitic gate-source, gate-drain, and source-drain capacitances. (b) Physical interpretation of parasitic resistances and capacitances of a vertical NW MOSFET, represented with transistor schematic overlayed by a circuit diagram. The subscripts s, m, b, w and o denote contact (at interface), metal, bottom, wire and overlap respectively, further S, D and G denote source, gate and drain.

$$g_m = \frac{g_{m,i}}{1 + g_{m,i}R_S + g_{d,i}(R_S + R_D)} \approx \frac{g_m}{1 + g_{m,i}R_S} \tag{2.25}$$

where $g_{m,i}$ and $g_{d,i}$ signifies the intrinsic transconductance and output conductance respectively. Output conductance typically has a small contribution due to $g_{m,i} \gg g_{d,i}$ and therefore the equation can be simplified. Studying the dependence of the drain current I_D for drift-diffusion at low fields (triode region) with respect to parasitic resistance yields

$$I_D = \frac{k(V_{GS} - V_T)V_{DS}}{L_g + k(V_{GS} - V_T)(R_S + R_D)}, \text{ where } k = W_{eff}\mu_e ff C_G. \tag{2.26}$$

Here, W_{eff} is the channel width, μ_{eff} channel mobility and C_{inv} inversion capacitance. [67] Figure 2.8 shows fitting to output characteristics of p-type MOSFETs (GaSb channel) measurements with varied gate-length L_g with relatively large parasitic resistance ($R_S + R_D = 20\ \text{k}\Omega \cdot \mu\text{m}$) to calculate field-effect mobility $\mu_e ff$ of charge carriers.

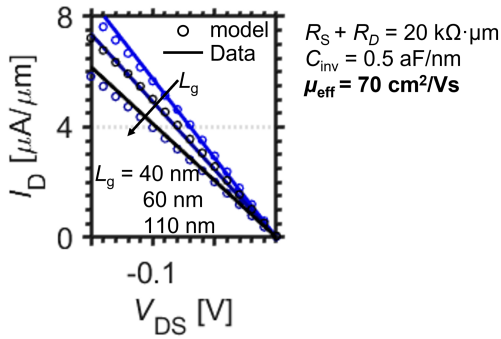

Figure 2.8: Fitting of drift-diffusion based model, equation (2.26) to low field (linear region) of measured output characteristics.

2.5 RF METRICS

The gain of the transistor, quantified by the transconductance g_m is crucial for high-frequency performance. However, minimizing extrinsic capacitances, originating from the MOSFET geometry, are equally important to attain high performance for RF applications. Considering gate-source C_{GS} and gate-drain C_{GD} capacitances (extrinsic and intrinsic), the transition frequency f_T where unity current-gain is acquired can be described as

$$f_T \approx \frac{g_m}{2\pi(C_{GS} + C_{GD})} \tag{2.27}$$

When including extrinsic resistance originating from the source R_S and drain R_D (Figure 2.7) the analytical expression for transition frequency is instead

$$f_T \approx \frac{1}{2\pi}\left(\frac{C_{GS} + C_{GD}}{g_m} + C_{GD}(R_S + R_D)\right)^{-1} \tag{2.28}$$

A more useful metric directly translating to use in RF applications is the maximum oscillating frequency f_{max} which instead captures the frequency behavior with respect to unilateral power-gain as

$$f_{max} \approx \sqrt{\frac{f_T}{8\pi R_G C_{GD}}} \tag{2.29}$$

These simplified expressions capture the essence of the RF design requirements, all extrinsic capacitances as well as resistances will have detrimental influence on the high frequency performance. Notably for increased unilateral

gain a decreased gate-resistance is of importance. The equations are essentially derived from Y-parameters from a small signal model, which can be extended to capture other important time-dependent effects such as charge carrier trapping within the channel. [52]

3

All III-V CMOS

Among the III-V binaries, InAs and GaSb are promising alternatives for CMOS integration. The materials are lattice matched and presents high-bulk mobility for electrons and holes respectively. They also demonstrate advantageous surface Fermi-level pinning typically leading to excellent ohmic-contacts when metallized. [68] Therefore, many methods for co-integrating n- and p-type transistors using this material combination have been proposed and explored. Considering throughput, cost and scalability, all new transistor technologies should preferably be on Si substrates. The promising material combination of InAs and GaSb have previously been explored using various, co-integration methods on Si, including material transfer of nanoribbons [69, 70] and selective etching of epitaxially grown periodic layers of InAs/GaSb sheets [71]. However, transfer of materials to a different substrate, typically Si, always raises concerns regarding throughput and yield.

N-type transistors employing III-V compounds as channel material have had considerable success for RF, where GaAs MESFET [72] and InGaAs HEMTs [19] are commercially available solutions for high-frequency operation while generating low noise. However, providing robust solutions for monolithic integration of logic capabilities combined with III-V high speed devices are coveted features, which requires strong III-V p-type devices. Another frequently suggested combination is utilizing p-type SiGe channel MOSFETs with n-type InGaAs RF transistors to provide strong p- and n-type performance. [18, 73] However, fabricating these circuits is difficult attributed to thermal budget and etch selectivity.

In this chapter, we provide a streamlined solution for co-integrating and co-processing of InAs n-type and GaSb p-type MOSFETs providing competitive

performance. This is enabled by implementation of core-shell nanowires, with a core consisting of an InAs-GaSb heterostructure encapsulated in 5 nm thick InAs shell. All devices are based on NWs ordered in, 300 nm pitch, hexagonal double row arrays. The inter-NW pitch is chosen to increase the absolute current for the final devices while mitigating growth effects related to surface diffusion. [52] Utilizing several nanowires within every device also alleviates yield related issues and ultimately enables higher absolute currents suitable for RF applications.

3.1 NANOWIRE GROWTH

To facilitate monolithic integration of III-V CMOS based on vertical nanowires, a bottom-up approach utilizing material grown by Au seeded metalorganic vapor phase epitaxy (MOVPE) is implemented. Nanowires are thus grown using Au seed particles as catalysts, selectively promoting material adsorption on a substrate, by exploiting the vapor liquid solid (VLS) mechanism. Initially, a substrate is patterned, by electron beam lithography (EBL), with Au dots organized in various structures, such as hexagonal and double row arrays. In this work 10 nm Au disks with varying diameter of 28 – 44 nm are used. The main advantage of MOVPE growth in conjunction with III-V materials is the possibility of formation of various heterostructures, allowing for both bandgap engineering and *in-situ* doping. The design freedom is further extended by growth of thin vertical nanowires, which can relax lattice mismatch induced strain by radial expansion or contraction instead of defect formation. Namely, utilizing nanowire VLS growth provides excellent crystallinity and substitutes the many masking steps needed to realize a doping profile in regular VLSI systems relying on ion-implantation (reported by Taiwan Semiconductor Manufacturing Company [74]). Growth of defect free nanowires on top of a Si (111) substrate is facilitated by the use of a 300 nm thick InAs buffer layer. To provide a sufficiently high quality InAs layer on top of Si, the growth conditions are adapted to maximize the density of Stranski-Krastonov islands which are coalesced by annealing. [75] Furthermore, by growing thin nanowires (20-65 nm diameter) on top of the buffer layer, line-defect propagation into the wire can be avoided. The InAs layer is also highly doped during growth, providing an excellent epitaxial contact as well as simplifying contact routing.

3.1.1 AXIAL HETEROSTRUCTURE

Utilizing a VLS-scheme based on gold seed particles as catalysts, in-situ doped and lattice-matched heterostructure InAs-GaSb nanowires can be grown, see Figure 3.1. These types of nanowires have been studied extensively in

literature due to the possibility of formation of a broken band-alignment. The electrical properties of the broken bandgap are especially useful for tunnel field-effect transistor (TFET), where the requirements of a source providing large density of states is fulfilled by the GaSb-segment. [37] For p-type devices this heterojunction is suitable as an epitaxial tunnel-contact, where high-current densities (large transmission, $\sim$ 2310 kA/cm^2) have been frequently demonstrated when incorporated as Esaki-diodes. [76,77]

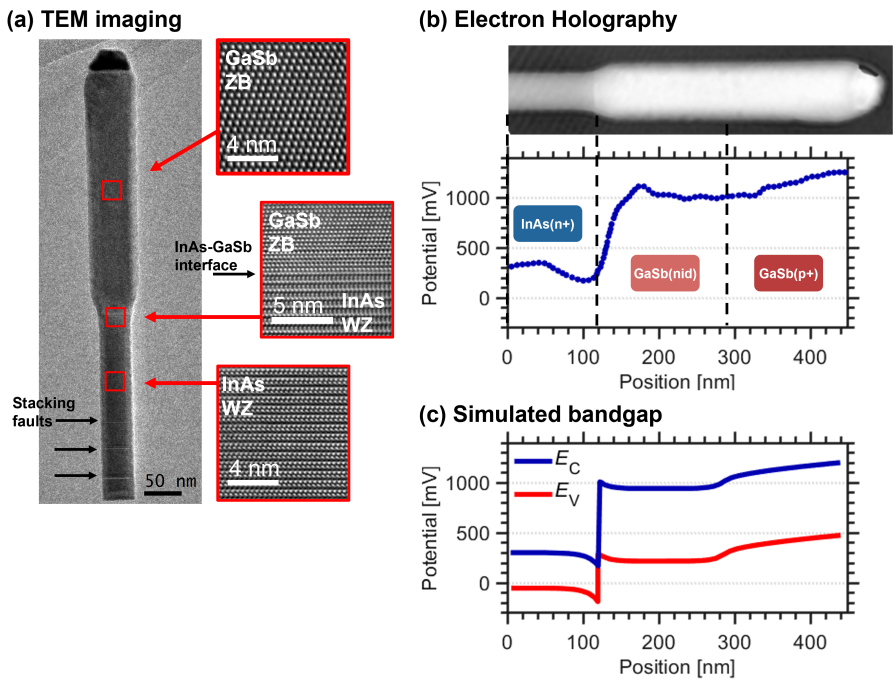

Figure 3.1: Transmission Electron Microscopy (TEM) results of InAs-GaSb heterostructure nanowire (a), including Electron Holography phase map (b) and simulated bandgap (1D poisson solver) (c). The bandgap simulation is based on expected doping profile from nanowire growth conditions (growth-rate, temperature, V/III ratio etc).

The bandstructure and doping of the InAs-GaSb nanowire can be further characterized via Transmission Electron Microscopy (TEM) and Electron Holography to establish crystallinity and axial band-structure, see Figure 3.1. This confirms the expected crystal structure of the zincblende (ZB) GaSb and wurtzite (WZ) InAs segments as well as an abrupt junction between the two lattice matched materials. By using Electron Holography a phase

map is constructed, where the phase difference ϕ corresponds to interference between electrons that pass through the specimen (object wave) and vacuum (reference wave), respectively, see Figure 3.1-b. ϕ is related to specimen thickness t and crystal potential $V(x,y,z)$ according to $\phi = C_E \int_0^t V(x,y,z)dz$ (C_E constant dependent on microscope acceleration voltage). The phase map can thus be used to deduce the relative concentration of free charge carriers, see Figure 3.1-c. [78–81]

3.1.2 GIBBS-THOMSON EFFECT

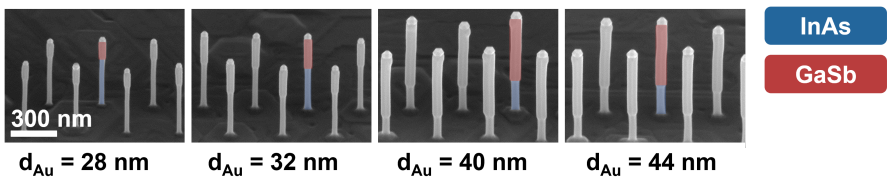

Figure 3.2: InAs-GaSb heterostructure nanowires grown by catalyst seeded MOVPE based on various Au dot diameter d_{Au} sizes.

The proposed material combination of InAs and GaSb, for n- and p-type devices respectively, exhibit comparably low mobility for holes (see Table 3.3). The hole mobililty in bulk GaSb is 40 times lower than the electron mobility in InAs. [18] This discrepancy inevitably translates to lower currents for the GaSb p-type channel devices, a challenge when pursuing balanced current density for III-V CMOS circuits. By utilizing a common effect occurring in small gold seed particles during VLS growth, namely the Gibbs-Thomson effect, the performance discrepancy can be somewhat equalized . Smaller gold particles have greater surface-to-volume ratio which increases the chemical potential within the catalyst seed. This effect is more evident for GaSb growth, therefore suppressing the VLS growth when using small seed particle diameters, see Figure 3.2. [82] Here, the volume of the InAs stem remains constant while the GaSb growth is heavily suppressed for smaller Au dot sizes ($d_{Au} < 35$ nm). Ultimately a wafer, or die, can be patterned with varying seed particle diameters to locally tune the length of the InAs and GaSb segments respectively. In other words, actively utilizing the Gibbs-Thomson effect can therefore provide separate nanowires dominated by either GaSb or InAs on the same sample die, enabling simplified co-integration and co-processing of MOSFETs exploiting the strength of each III-V compound constituent (Figure 3.2). The thicker diameter of the GaSb-dominated nanowires also provides a vital step toward equalizing the CMOS current levels after device formation. However, by using improved fabrication schemes the need for techniques

based on VLS-growth effects can be made obsolete, which is explored further in this thesis.

3.1.3 RADIAL HETEROSTRUCTURE

Sb-based materials are notoriously sensitive and have been reported to be etched in water. This can be attributed to the III-Sb materials being rapidly oxidized. [83] Therefore, many techniques regarding etching of Sb-based materials have been developed during the thesis work and will be explained in detail in subsequent sections. In most cases, to enable any form of complex processing, the bare GaSb require protection. To ensure minimized oxidation and etch selectivity, the GaSb can only be exposed to air for a few seconds prior to critical steps such as gate-oxide formation. Here, we use our previous knowledge regarding formation of radial heterostructures in MOVPE grown nanowires, in order to form a protective shell around the GaSb [45, 84]. We design and implement nanowires consisting of an InAs-GaSb heterostructure core with a highly doped 5 nm InAs shell, see Figure 3.3. By tuning the composition of metalorganic constituents (V/III ratio) within the growth chamber different growth mechanisms can promote either radial or axial growth. This effect is related to a difference in diffusion length of the various atoms after adsorption on the substrate or nanowire surface, where typically As has a comparably short diffusion length. Thus, increasing the partial pressure of the As precursor, compared to In, (high V/III ratio) will promote radial shell growth. This technique also allows for regrown contacts, meaning abrupt material and dopant transitions, for the final devices (Figure 3.3).

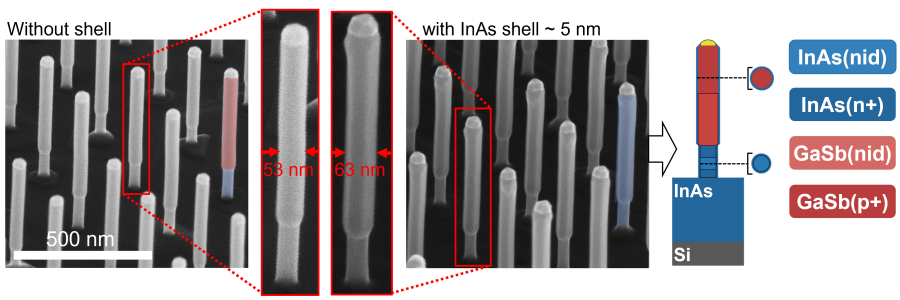

Figure 3.3: InAs-GaSb nanowires grown in hexagonal arrays with 300 nm inter-pitch, with and without InAs radial shell growth. Schematic of the cross-sections of the various segments of the heterostructure nanowire.

3.2 ALL-III-V CMOS FABRICATION

Detailed fabrication recipes can be found in *Appendix A*.

3.2.1 HSQ IMPLEMENTATION

The key to enable greater process control is the implementation of self-aligned processing schemes. In other words, the presented processing schemes allow for locally controlled placement of gate-position in the vertical direction with different positions among devices on the same sample. This is partly enabled by using hydrogen-silsesquioxane (HSQ) based spacers. HSQ is an electron-sensitive resist which in its fully cured state turns into nanocrystalline-Si/SiO2, which leads to excellent thermal budget and mechanical stability. The film thickness can be controlled by underexposing the HSQ using EBL, see Figure 3.4. By using doses lower than those needed for full exposure, allows us to locally define the thickness of a spacer or mask.

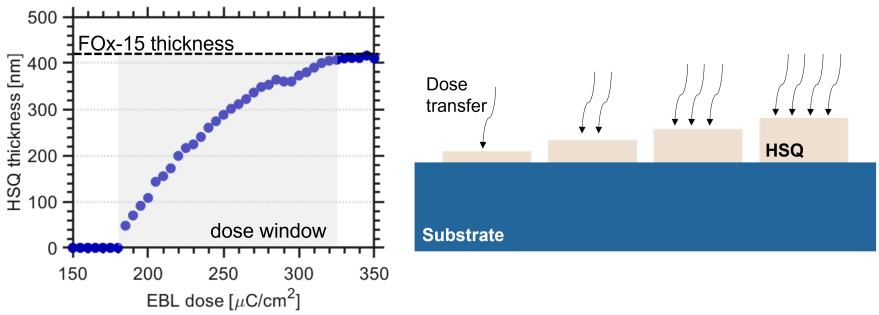

Figure 3.4: Measured contrast curve and schematic for FOx-15 (HSQ) when locally controlling the film thickness by EBL dose. Highlighting a usable dose window between 180 – 330 μC/cm^2.

During this work an HSQ version called FOx-15, which is essentially HSQ diluted with MIBK as carrier solvent, is used resulting in a thickness of about 400 nm after spin coating. [85] Typically tetramethylammonium hydroxide (TMAH) based developers are used with FOx-15, to avoid leaving residual charges prevalent when using e.g. salty developers (NaOH and NaCl). [86] TMAH rapidly etches Sb-based materials, therefore an etch stop is required when implementing GaSb in conjunction with HSQ. As described in section 3.2.3, we use a radial InAs shell to cover the heterostructure nanowire which acts as an etch stop, and also enables extended fabrication capabilities. [87]

3.2.2 TOP METAL DEFINITION & BOTTOM SPACER FORMATION

To minimize access-resistance and enable selective thinning of the channel region, a self-aligned gate-last process is implemented to realize improved performance for the all-III-V CMOS. The gate-last process is achieved by defining a metal top contact as the first fabrication step. Using this method has previously proven to enable optimization of extrinsic resistance originating from the metal-semiconductor interface [88] as well as demonstrating excellent current densities in vertical InAs/InGaAs n-type MOSFETs [44].

To be able to utilize a self-aligned fabrication scheme, all critical steps have been considerably condensed in order to improve yield. We employ a method where the same mask used for alignment of the top metal is later converted to a bottom spacer, see Figure 3.5. Here, the position of the bottom edge of the top metal is defined by the dose-transfer technique discussed in section 3.2.1 utilizing HSQ. This step allows us to define the position of the gate with great precision (<10 nm), ultimately enabling parallel fabrication of nanowires with varying InAs-GaSb length ratios (section 3.2.2). After the dose transfer, the protruding nanowires are coated by a metal layer consisting of 20 nm sputtered W and 50 cycles of TiN, resulting in a total thickness of 10 nm on the nanowire sidewalls. The metal is selectively etched by an anisotropic inductively coupled plasma reactive ion etch (ICP-RIE) process with C_4F_8 and Ar chemistry, to finalize the top contact. The exposed HSQ mask is then thinned down by HF 1:1000 and annealed in N2-environment, at 350^o C, finalizing the first spacer and revealing the channel-region. At this step, only the III-V material constituting the channel region is exposed allowing for straightforward selective etching and surface optimization of the gate stack. Also, the alignment of both the bottom and top contact are defined within these processing steps, thus relaxing the lithography conditions for subsequent gate-alignment.

3.2.3 GATE-STACK FORMATION

Traditionally, the performance of III-V p-type MOSFETs have been greatly limited by the gate-stacks. Many studies have shown that surface-effects serve to reduce the mobility in thin GaSb nanowires. [38] Thus, new methods of surface passivation techniques are required to balance the performance of the III-V CMOS, typically bottle-necked by the p-type MOSFET counterpart. This can be partly attributed to key fabrication techniques used in state-of-the-art III-V n-type MOSFETs [44, 89] not being compatible with Sb-based structures. One key method is digital etching allowing for aggressive trimming of critical channel dimensions. [83] This technique relies on selective etching of the native oxides formed on the surface of the III-V nanowires. However, GaSb

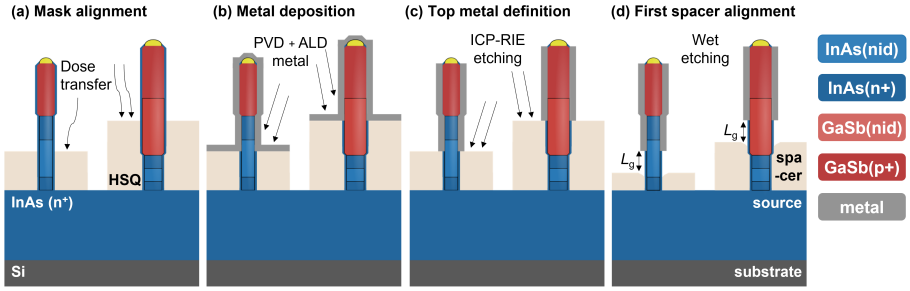

Figure 3.5: InAs-GaSb nanowires grown in hexagonal arrays with 300 nm inter-pitch, with and without InAs radial shell growth. Schematic of the cross-sections of the various segments of the heterostructure nanowire.

based structures are known for their problematic oxidation properties, where Sb-oxides account for poor interface and etch-sensitivity [90], where also Sb_2O_5 is insoluble in most acids or alkali. [83]

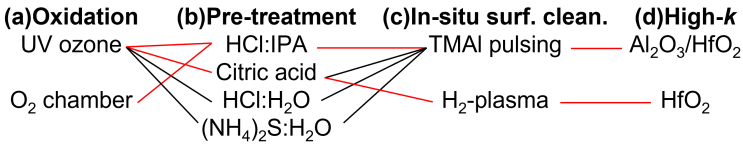

Figure 3.6: Demonstrating the various combinations for achieving optimal surface conditions, considering both InAs and GaSb channel materials. All gate-stacks where metallized by sputtered tungsten (W). (a) Formation of native oxides were performed by oxidation in an O2 chamber or by UV ozone-treatment. (b) Several pre-treatments and digital etches were performed by wet etching, ranging from alcohol based or water based HCl (1:10), citric acid or ammonium sulfide (1:100). (c) In-situ surface cleaning within the ALD chamber was performed by TMAl pre-pulsing or H2 plasma. Note that the H2 plasma was also followed by TMAl pre-pulsing. (d) Two different high-κ oxides were employed, consisting of a regular bi-layer Al2O3/HfO2 (6/36 cycles) and a single-layer HfO2 stack (40 cycles).

The critical steps within the gate-stack formation includes, stripping of the InAs radial shell, digital etching of the channel region, pre-treatment of the surface, ALD in-situ surface cleaning and finally high-k definition. In other words, achieving optimal surface conditions is hugely complex and dependent on many parameters. Therefore, many combinations were explored in this thesis, see Figure 3.6. Certain combinations yielded successful results and led to publications (marked in red). Ozone oxidation followed

by citric acid allows for selective removal of the InAs shell (zincblende and wurtzite) covering both GaSb and InAs channel material. However, further recess etching must be carried out utilizing HCl based etching. To avoid critical failure during pre-treatment digital etching is performed by alcohol-based wet etching, in this case utilizing HCl diluted by isopropanol (1.25 M, 1:10). [83] To stress the importance of using water-deprived chemicals; HCl:H2O diluted with isopropanol, namely HCL:H2O:IPA (1:2:30) were also tested but would consistently lead to critical failure for a 30s acid dip.

The various combinations of surface preparation and high-κ from Paper I & II are summarized in Table 3.1. Here, improvements in digital etching techniques, utilizing oxidation in an O_2 chamber, allowed for all-III-V CMOS achieving 10-20 nm channel diameters. The use of in-situ hydrogen plasma (see Appendix A for details) serves to greatly reduce the InAs diameter. The results from the process of optimizing gate-stack parameters is displayed in Figure 3.7, which serves to further highlight the versatility of the developed HSQ based co-processing techniques. Note that the InAs shell is removed to restore the un-intentionally doped (nid) channel-material.

Table 3.1: Summarizing various pre-treatment conditions and physical attributes of the III-V CMOS device generations. The standout features are highlighted, where improved surface preparation allows for diameters down to 10 nm.

	Paper I - Type I	**Paper I - Type II**	**Paper II**
Oxidation	UV ozone	UV ozone	**O_2 chamber**
Pre-treatment	Citric acid	HCL:IPA	**HCL:IPA**
In-situ surf. clean.	H_2 plasma + TMAl	TMAl	TMAl
High-κ	HfO_2 (40 cycles)	Al_2O_3/HfO_2 (6/36 cycles)	Al_2O_3/HfO_2 (6/36 cycles)
L_g / Diam. (GaSb)	100 / 38 nm	70 / 40 nm	**60 / 22 nm**
L_g / Diam. (InAs)	40 / 12 nm	50 / 20 nm	**150 / 10 nm**

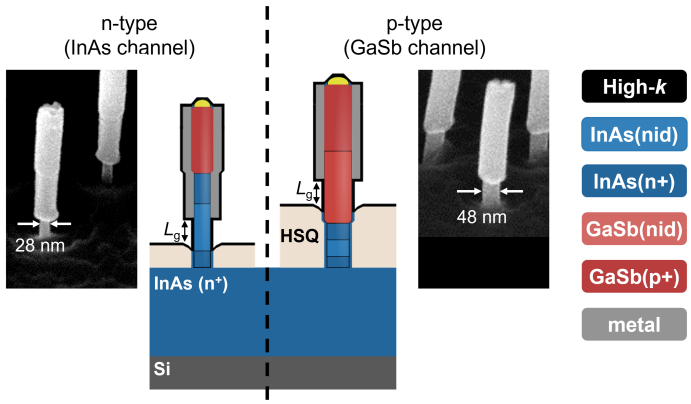

Figure 3.7: Demonstrating the results of co-processing techniques used in Paper I (see Table 3.1) showing schematic associated with SEM images for n- and p-type devices. SEM images representing nanowire diameter with added high-k (4 nm) resulting in 20 and 40 nm diameter for n- and p-type devices, respectively.

3.2.4 CIRCUIT REALIZATION

For vertical nanowire MOSFETs all the contact layers are inherently separated and stacked. This enables simplified contact routing for circuits which can be directly incorporated into the transistor front-end-of-line, without adding fabrication steps. Functioning inverter and NAND gates were demonstrated in this work, including new designs for realizing a ring-oscillator, see Figure 3.8. The front-end-of-line routing is represented here by patterning within the epitaxial mesa (InAs buffer layer) and gate metal layer.

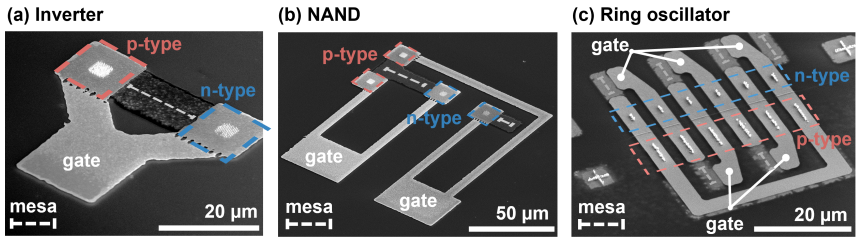

Figure 3.8: Examples of circuits enabled by the developed technology platform. SEM images of (a) Inverter, (b) NAND and (c) ring oscillator where input voltage will be applied to the various gate-contacts. SEM images of circuits are represented after the finalization of the gate electrode, therefore a third metal layer is later added for operation. Observe that the ring-oscillator never provided measurable results due to yield issues.

3.3 ALL-III-V CMOS CHARACTERIZATION

Two fabrication strategies, see Figure 3.9, were developed to enable co-integration of InAs n-channel and GaSb p-channel devices. The first generation (Paper I) focused on n-channel MOSFET performance while introducing a functional p-channel device on the same sample (Figure 3.9-a). In the second generation (Paper II) of devices, balanced performance was achieved for the III-V CMOS by greatly optimizing the p-type GaSb MOSFET. This was facilitated by refined fabrication techniques, where the precision of gate-placement was improved (due to process maturity) allowing the whole process to be based around one type of nanowire (Figure 3.9-b). See Table 3.1 for detailed description regarding physical differences between III-V CMOS generations.

The various leaps in performance is expressed by summarizing the DC metrics of the device generations in Table 3.2. In Paper I, a self-aligned gate-last process was developed to realize monolihically integrated III-V CMOS based on vertical heterostructure InAs-GaSb nanowires. The new fabrication technique enabled minimized gate access-regions leading to improved on-state performance. Therefore, competitive values are demonstrated with $g_{m,max}$ up to 2600 µS/µm. Processing conditions are although heavily biased towards improved n-type InAs performance [46], which is reflected in limited improvements for the GaSb based devices reaching a respectable $g_{m,max}$ up to 74 µS/µm. However, by greatly improved surface pre-treatment routines and scaled dimensions, in Paper II, the p-type GaSb MOSFET performance reached a competitive value of 230 µS/µm.

To summarize the impact of the presented work a survey of the III-V based MOSFET field is performed to provide benchmarking of the individual n-

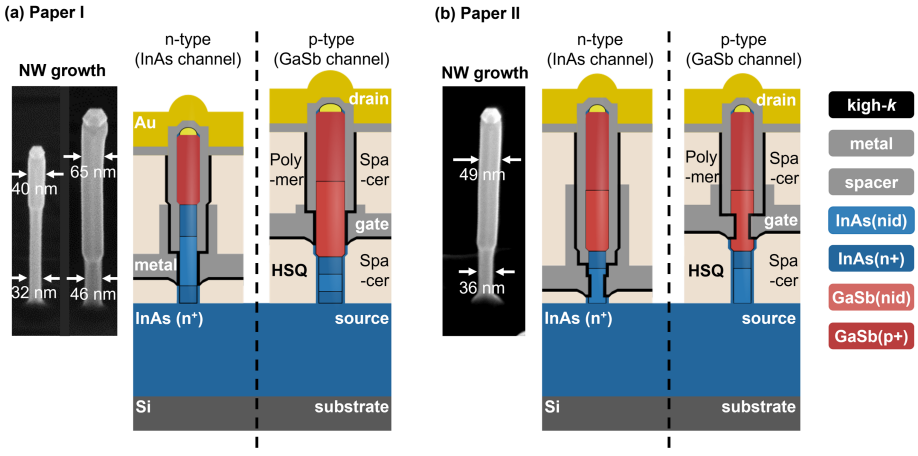

Figure 3.9: SEM of bare nanowires and schematic of finished devices of the III-V CMOS. (a) Generation 1 devices utilizing the gibbs-thomson effect to facilitate suitable nanowires for p- and n-type devices respectively. (b) Generation 2 implementing one type of nanowire, and down-scaling the diameter of the GaSb to 49 nm.

Table 3.2: Summarizing various pre-treatment conditions and physical attributes of the III-V CMOS device generations. The standout features are further highlighted.

	Paper I - Type I	**Paper I - Type II**	**Paper II**
High-κ	HfO_2	Al_2O_3/HfO_2	Al_2O_3/HfO_2
EOT	**0.76**	0.85	0.85
L_g / Diam. (InAs)	**40 / 12 nm**	50 / 20 nm	150 / 10 nm
$g_{m,max}$ (InAs)	**2600 μS/μm**	1200 μS/μm	405μS/μm
SS_{lin} (InAs)	191 mV/dec	74 mV/dec	**74 mV/dec**
I_{on} (InAs)	-	-	**156 μA/μm**
L_g / Diam. (GaSb)	100 / 38 nm	70 / 40 nm	**60 / 22 nm**
$g_{m,max}$ (GaSb)	11 μS/μm	74 μS/μm	**230 μS/μm**
SS_{lin} (GaSb)	622 mV/dec	273 mV/dec	**175 mV/dec**

and p-type devices, see Figure 3.10. The transistors developed in this thesis demonstrate competitive values in relation to both p- and n-type devices,

demonstrating record performance compared to other III-V p-type MOSFETs. Furthermore, benchmarked with all n-type MOSFETs respectable values are achieved which follows the expected scaling trend, with a mean free path λ=35$\pm$15 nm [42], established by vertical NW based devices (InAs-source) using a similar gate-last process.

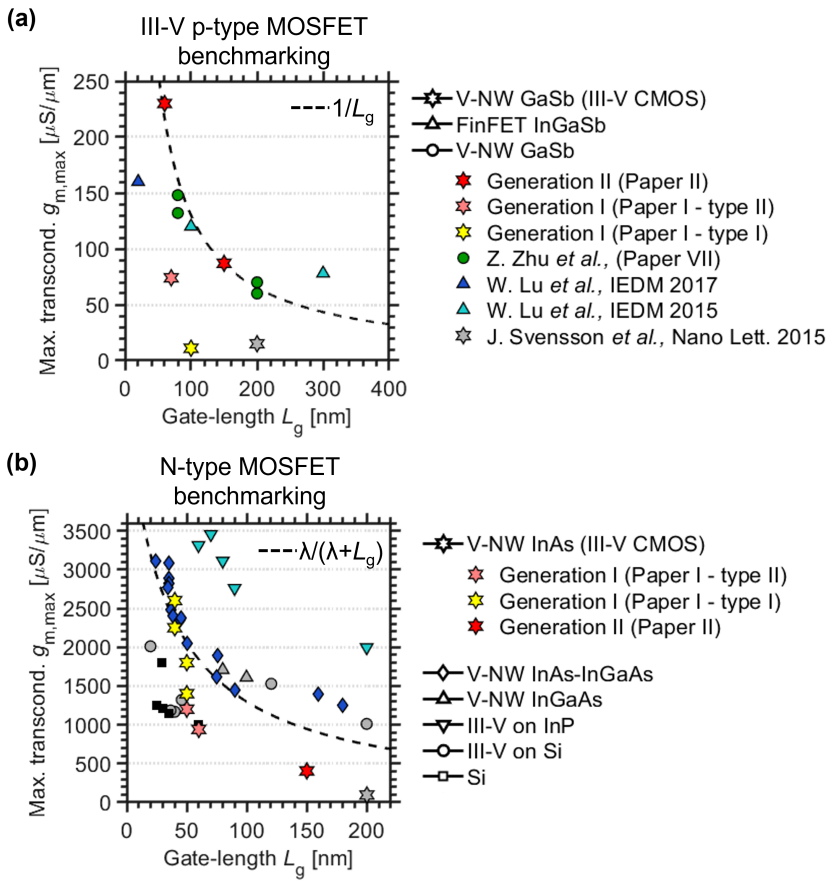

Figure 3.10: Bechmarking of all-III-V CMOS compared to state-of-the-art n- and p-type devices by gm,max vs Lg. Maximum transconductance from Paper I & Paper II are derived using $|V_DS = 0.5\ \mathrm{V}|$. All other technologies are benchmarked using their specific drive voltage. (a) Other III-V p-type MOSFET technologies are based solely on GaSb and InGaSb. The various categories are vertical nanowire (V-NW) GaSb in III-V CMOS configuration (Paper I, Paper II & [20]), V-NW GaSb MOSFETs (Paper VII) and InGaSb FinFETs [83, 91]. Dashed line represents expected trend considering drift-diffusion based physics ($g_{m,max} \sim 1/L_g$). (b) Summarizing all types of n-type MOSFET technologies within the categories of V-NW InAs in III-V CMOS configuration (Paper I, Paper II & [20]), V-NW InAs-InGaAs heterostructure channel devices [44], V-NW InGaAs [92, 93], III-V on InP [59, 92, 94], III-V on Si [55–58]. Dashed line represents expected trend considering a quasi-ballistic channel ($g_{m,max} \sim \lambda/(\lambda + L_g)$). [95]

3.3.1 V_T MATCHED III-V INVERTER & CMOS BENCHMARKING

Designing an inverter requires balanced performance of the n- and p-type MOSFETs with respect to drive-currents, threshold voltage, and modulation. Here we demonstrate a threshold voltage V_T matched III-V CMOS inverter using our developed technology platform (Paper I), see Figure 3.11. Combined transfer characteristics (Figure 3.11-a) display $V_T \sim 0$ V for both the GaSb and InAs based devices. However, the p-type MOSFET require further optimization to acquire balanced drive-current and modulation properties (maximum $I_{on}/I_{off} \approx 10^2$) as compared to the n-type device. The MOSFET discrepancy carries over to the voltage transfer characteristics (VTC) of the inverter further limiting the gain to 2 V/V at supply voltage $V_{DD} = 500mV$ (Figure 3.11-b). However, compared to previous III-V CMOS attempts [20, 68] the voltage operation window at V_{DD} = 0.5 V can be maintained within $0 < V_{in}, V_{out} < 0.5$ V.

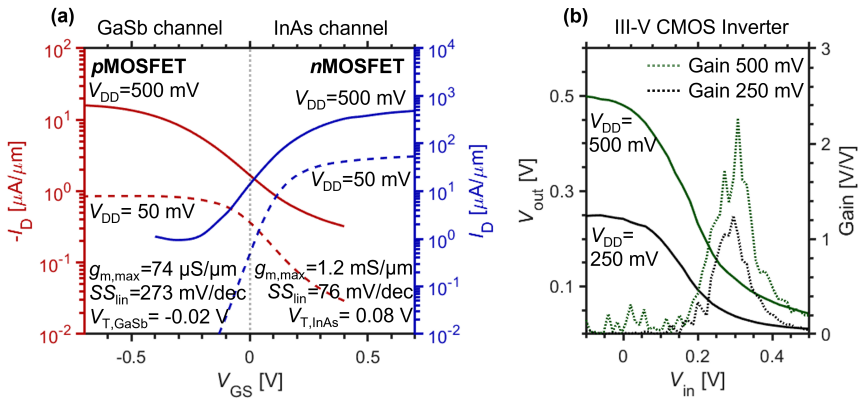

Figure 3.11: V_T matched III-V inverter realized using monolithically integrated n- and p-type V-NW MOSFETs. (a) Combined transfer characteristics of the n- and p-type devices at V_{DD} = 50 and 500 mV, highlighting the matched threshold voltage. (b) Inverter VTC and voltage gain for $V_{DD} = 0.25$ and 0.5 V.

The developed III-V CMOS on Si technology is further compared with established Si CMOS by the digital metric on-current I_{on} vs L_g, see Figure 3.12. The comparison serves to highlight the relevancy of the work, where the various improvements have balanced the on-currents and vastly improved performance for the III-V based p-type MOSFET (Paper II). Comparable n-type MOSFETs (InAs source) serves to highlight the potential improvements by incorporating vertical nanowire based technology, where larger on-currents

are achieved for longer gate-lengths. Also, for vertical geometries larger gate-length does not correspond to diminished packing density due to constant footprint.

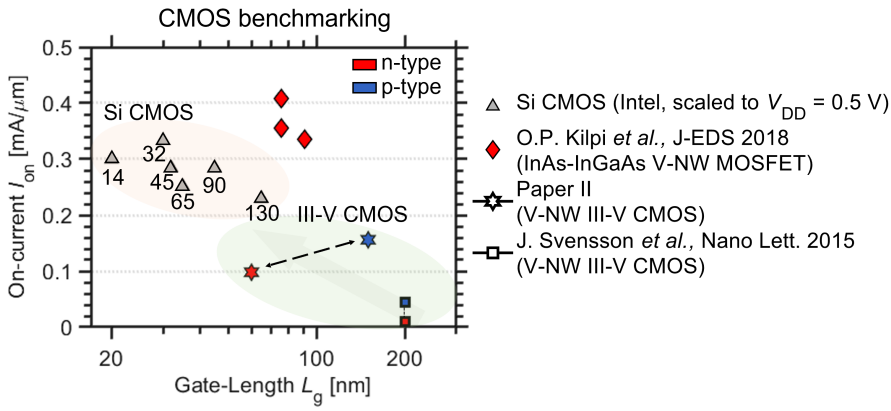

Figure 3.12: Benchmarking of on-currents I_{on}, at $I_{off} = 100$ nA/μm, versus gate-length L_g for established Si CMOS technology and representative vertical nanowire (V-NW) III-V on Si based technology. Here I_{on} is used as a baseline digital metric that ultimately governs switching speed (propagation delay $t_p \sim 1/I_{on}$). Data points representing Si CMOS is accompanied by their respective node numbering. The Si CMOS bias, from 130-nm to 32-nm node, is scaled down to $V_{DD} = 0.5$ V by modelling, a supply voltage typically recurring for III-V MOSFETs. [18] On-current for 14 nm node (finFET) is experimentally determined at $V_{DD} = 0.5$, and is normalized by the fin circumference (normalized by chip area yields on-current at ~ 0.65 mA/μm). [49] III-V CMOS on Si technology are represented by Paper II & [20]. Note that on-current is defined at $|V_{DS}| = 0.5$ V for the p-type MOSFET in Paper II due to limited current modulation. Further, n-type III-V on Si MOSFETs using comparable fabrication methods are included to highlight possibilities of III-V technology for digital applications. [95] Observe that all devices are benchmarked using a supply voltage V_{DD} of 0.5 V.

Table 3.3: State of the III-V CMOS on Si technologies [20, 69–71]. Represented devices are vertical nanowire based (Paper I, Paper II & [20]), nano-ribbons using a material transfer technique, similar to wafer bonding [69, 70], and planar thin InAs/GaSb layers selectively masked and etched [71]. Blank spaces are due to undisclosed data.

n-type	**Pap. I**	**Pap. II**	**[20]**	**[71]**	**[70]**	**[69]**
I_{on} [μA/μm] (at I_{off} = 100 nA/μm)	-	**156**	44	-	80	4
$g_{m,max}$ [μS/μm]	**1200**	405	95	-	-	-
L_g [nm] /Crit.Dim.	**50** /20	150 /**10**	200 /32	500 /20	>500 /13	>500 /**2.5**
SS_{sat} [mV/dec]	158	98	525	185	**84**	-
SS_{lin} [mV/dec]	76	**72**	-	-	-	-
p-type						
I_{on} [μA/μm] (at $\lvert V_{DS}\rvert$ = $-$0.5V)	17	**98**	7	10	22	2.4
$g_{m,max}$ [μS/μm]	74	**230**	15	-	-	-
L_g [nm] /Crit.Dim	80 /40	**60** /22	200 /48	500 /20	>500 /**7**	>500 /20
SS_{sat} [mV/dec]	355	305	300	-	**156**	-
SS_{lin} [mV/dec]	273	**175**	-	-	-	-

4

III-V p-type MOSFETs

The all-III-V CMOS technology platform, presented in Chapter 3, is greatly bottlenecked by its p-type MOSFET counterpart. Therefore, a separate study regarding optimization of gate-stack as well as contacts is necessary for greater understanding of the material properties. To fully characterize the MOSFET devices, gate-length variation is a requirement. Novel fabrication schemes have previously been developed for vertical n-type MOSFETs, which has successfully implemented gate-length scaling and also enabled selective thinning of the channel region. [44–46] However, implementing these schemes for vertical III-V p-type MOSFETs has been challenging due to III-Sb etch selectivity. In addition, the all III-V CMOS developed in this thesis relies on a broken bandgap InAs-GaSb tunnel-junction, at the source, which further complicates detailed analysis. Here we address all these issues and present vertical as well as symmetrical p-type MOSFETs with varied gate-length, from 40 nm up to 140 nm, on the same sample die.

4.1 FABRICATION

In accordance with Section 3.1.3, covering the all-III-V CMOS method, we have established that Sb-based devices cannot be handled without various protection layers. For this fabrication scheme the nanowire is first fully encapsulated in metal and secondly various etch techniques are used to expose the channel, simultaneously forming both source and drain contacts, prior to high-k deposition, see Figure 4.1. Full fabrication recipe can be found in *Appendix A*.

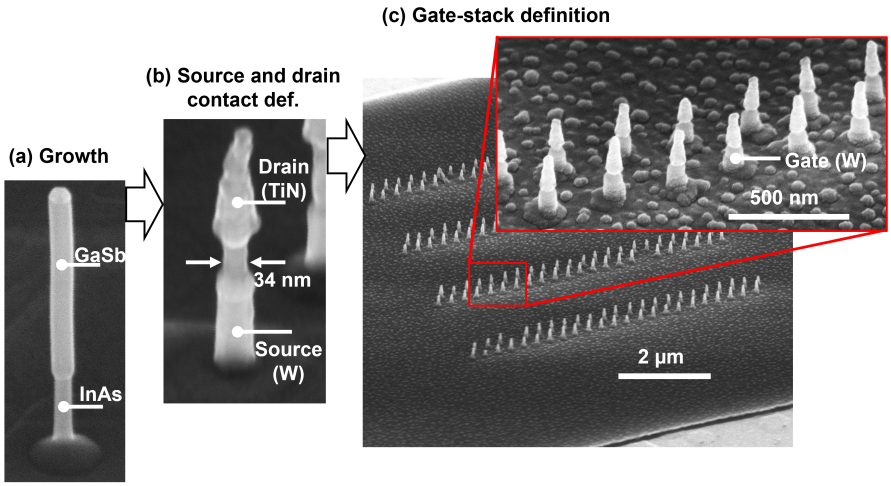

Figure 4.1: SEM images of the critical steps for realizing symmetrical p-type GaSb MOSFETs. (a) Nanowire growth of InAs-GaSb heterostructure nanowire. (b) Post source and drain metal contact definition of single nanowire, showing channel region of 24 nm when considering high-k. (c) Array of nanowires after gate-stack formation, demonstrating 100% yield.

4.1.1 SOURCE & DRAIN CONTACT DEFINITION

The p-type MOSFET fabrication is enabled by optimizing fluorine based dry-etch techniques, essentially by tuning the bias conditions in an ICP-RIE process. Here we utilize etch selectivity between tungsten (W) and TiN metals to our advantage. Using fluorine dry etching in conjunction with W creates volatile etch-products (WF_6) at room temperature allowing a clean etch process with no re-sputtering effects. [96] Etching of TiN using SF_6-based plasma instead produce low-volatility etch products such as TiF_x ($x \leq 4$). Specifically, TiF_3 and TiF_4 have boiling points at 1400^o C and 284^o C respectively, making them difficult to remove using plasma-based etching. However, evaporation rates of the nonvolatile etch-products are heavily dependent on the density and energy of ion bombardment. Therefore TiN can be used to accentuate the anisotropy when dry etching, where non-volatile TiF_x etch-products acts as sidewall inhibitors. [97]

By using different metal layers (W and TiN) in conjunction with the InAs-GaSb heterostructure nanowire the source and drain contacts can be realized as shown in Figure 3.6), thus a comparably thin (GaSb diameter < 40 nm) InAs-GaSb nanowire can be incorporated (Figure 4.2-a). The nanowire is encapsulated in metal acting as an etch stop and protecting the III-Sb from

further oxidation. To align the bottom edge of the top metal an organic ma-N (negative resist) based mask is used. The ma-N can be locally aligned by EBL dose transfer similar to HSQ (see Figure 3.4), using a dose-window corresponding to 90-160 $\mu C/cm^2$. However, the final thickness of the resist is also heavily dependent on development time (Figure 4.2-b).

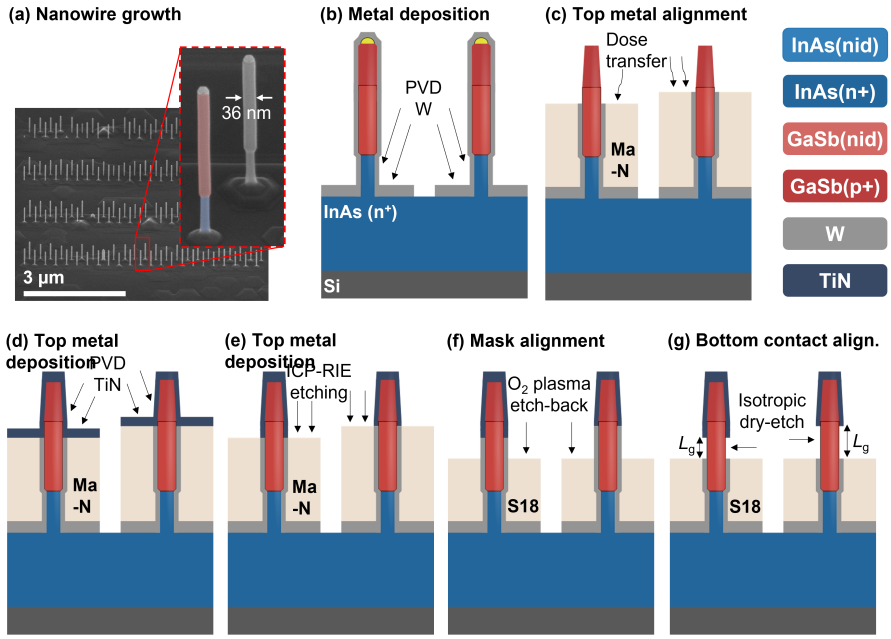

Figure 4.2: (a) SEM image of the nanowire growth. (b) Sputtering of W. (c) EBL dose transfer for locally controlled thickness of Ma-N mask. (d) Sputtering of TiN. (e) Anisotropic dry etching of the planar metal layer. (f) Alignment of S18 polymer mask by O2-plasma. (f) Alignment of the bottom contact by isotropic dry etch of the exposed W.

After aligning the mask, the TMAH (ma-D ~4% TMAH) based developer will start etching the W ultimately removing the metal and continuing by polishing protruding GaSb tip. From this point on the process share many similarities with our other self-aligned fabrication methods (see Figure 3.5). [46] Namely a TiN film is deposited by sputtering and subsequently the planar surface is etched by a high-power (700W ICP and 30 W forward-RF) SF_6:N_2 plasma at low pressures (< 10 mTorr) in an ICP-RIE process (Figure 4.2-d). The etch mask is removed and replaced by a new polymer mask based on S18 resist aligned by O_2 plasma etching, exposing a small segment of the W contact (Figure 4.2-f). Finally, the protruding W segment can be selectively

etched revealing the semiconductor constituting the channel. The isotropic etching is enabled using ICP-RIE with no forward-RF power (150 W ICP and 0 W forward-RF, 30 mTorr), thus the plasma is generated remotely and reaches the substrate only by diffusion. No ion-bombardment is present during these etch conditions, therefore the TiN will act as an etch stop with the help of TiF_x formation.

4.2 SYMMETRY AND TRANSPORT PROPERTIES IN GASB MOSFETS

We provide a method to realize gate-length scaling in vertical GaSb nanowire p-type MOSFETs, see device schematic in Figure 4.3-a. In addition to gate-length scaling down to 40 nm (Paper III), we also provide a symmetrical structure with similar GaSb/metal contacts for both source and drain terminals. Previous vertical attempts has typically featured an epitaxial InAs/GaSb tunnel junction and a p-GaSb/metal as the source and drain contacts, respectively. [20] To further quantify the symmetry of the components, the maximum transconductance $g_{m,max}$ can be compared for switched source and drain positions at various gate-lengths, see Figure 4.3-b. Comparing the mean value of $g_{m,max}$ for the full dataset between top and bottom drain electrode configurations results in 10% higher transconductance for top drain, which means that assuming symmetrical contact resistance for the devices is a reasonable approximation. The discrepancy is expected due to the bottom electrode relying on background doping (acceptor concentration $N_A \sim 10^{16}$ cm^{-3} [98]) to enable sufficiently low contact resistance (current density through Schottky contact $\sim \exp\left(-\sqrt{N_A}\right)$ [99]).

Gate-length scaling allows for extrapolation of the total contact resistance (via on-resistance Ron metric) which yields a source and drain resistance value $R_S + R_D$ of 20 k$\Omega \cdot \mu$m. Assuming symmetrical contacts and calculating the inversion capacitance as C_{inv} = 0.5 aF/nm (by coaxial capacitance), the field-effect mobility of holes can be deduced as 70 cm^2/Vs when considering drift diffusion mechanisms. [67] Figure 4.4 summarizes reported data regarding hole mobility vs diameter dependence for GaSb nanowires, including the mobility μ_h deduced in Paper III. Comparing the hole mobility vs diameter with previously published data for similar VLS-grown nanowires [98] as well as other dedicated studies of GaSb nanowires (including InSb) [38, 100–102] shows reasonable fit to expected trends. In other words, the methodology of metal-encasing followed by dry etching of the channel region is not detrimental to the nanowire transport properties.

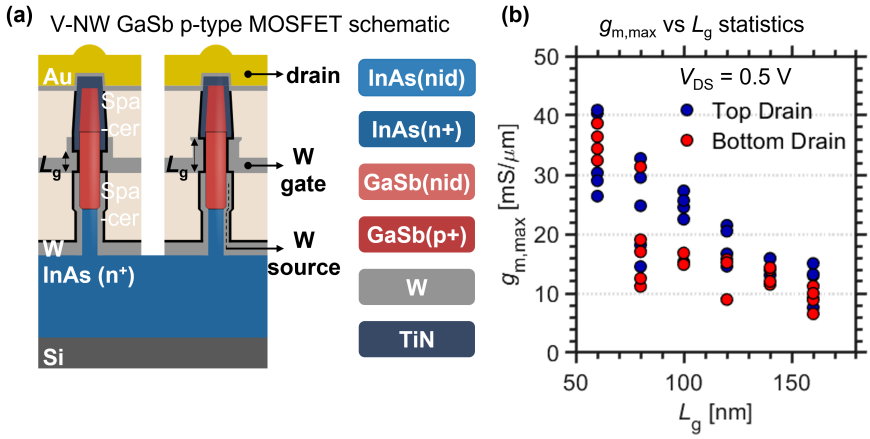

Figure 4.3: P-type GaSb MOSFET statistics, quantifying symmetry in the structure derived by self-aligned metal contacts at drain/source by switching electrode position during measurement. (a) Maximum transconductance $g_{m,max}$ vs gate-length L_g for certain device row not represented in Paper III.

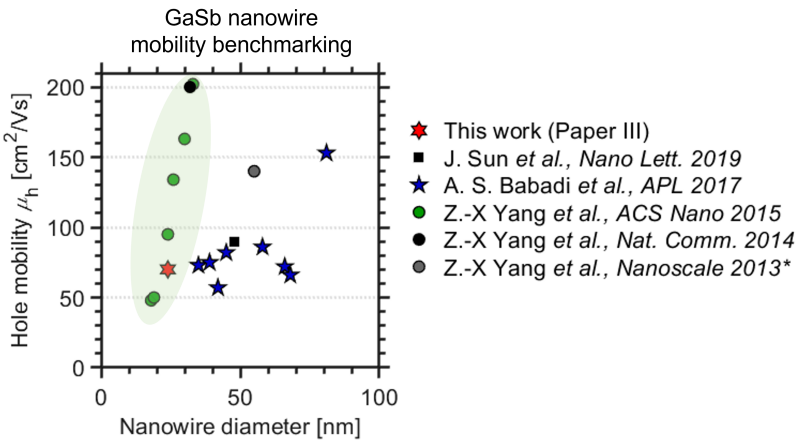

Figure 4.4: Summarizing studies related to field-effect mobility in various CVD-grown GaSb nanowires outlining the strong diameter dependence of hole mobility [38, 98, 100–102]. Mean-values are represented from dedicated studies. Showing a hole mobility (Paper III) well in line with the linear diameter dependence derived from literature (green highlight) [38]. *All nanowires based on GaSb with exception of carbon doped InSb nanowires from [100].

5

III-V n-type MOSFETs for RF and Memory Selector Applications

N-channel III-V transistors are known for their excellent transport properties where InAs and InGaAs channel devices have proven to be suitable for high-frequency applications. To achieve reduced parasitic capacitance for vertical n-type MOSFETs, while maintaining low access-resistance (Figure 2.7), various fabrication techniques need to be developed. [19] In this chapter, we explore different spacer technologies for both sidewall and vertical configuration, developed during this thesis work. Furthermore, the optimized sidewall spacer process module is also utilized to fabricate vertical III-V based GAA selectors for 1-transistor-1-memristor (1T1R) implementation.

5.1 RF MOSFET DESIGN

Many details regarding the fabrication methods for RF optimized vertical nanowire MOSFETs will remain undisclosed.

5.1.1 NANOWIRE HETEROSTRUCTURE DESIGN

A benefit of incorporating III-V materials, in a vertical nanowire MOSFET architecture, is the possibility of performing bandgap engineering by introducing various heterostructures. In this work, we incorporate nanowires with InAs-InGaAs core, with increased Ga-content closer to the top, overgrown with an InGaAs shell, see Figure 5.1. By utilizing VLS growth the nanowire inherently adopts a shape consisting of a substantial foot region, at the nanowire bottom segment. This occurs due to preferential nucleation at the corner of the nanowire during epitaxial growth. [103] The geometry of the

nanowire with a overgrown foot region can be used as a feature to mitigate access-resistance originating from the nanowire bottom segment. [44] The graded core segment, from InAs to $In_{0.7}Ga_{0.3}As$, is designed to provide a channel with high injection velocity at the source, facilitated by the InAs, and larger bandgap closer to the drain, by employing InGaAs, to suppress band-to-band-tunneling (BTBT) and impact ionization. By using InGaAs in the channel, adjacent to the drain side, higher breakdown voltage V_{BD} (empirical relation $V_{BD} \sim E_g^{3/2}$ [104]) can be achieved as well as improved off-state leakage. Incorporating this type of heterostructure has demonstrated vertical nanowire MOSFETs achieving off-currents I_{off} at 1 nA/μm at $V_{DS} = 0.5$ V and stable operation up until $V_{DS} = 1.5$ V (negligible onset of BTBT). [45] Furthermore, the nanowires utilize a highly doped InGaAs overgrown shell acting as δ-doping at the source-side, providing low source-resistance R_S (down to 75 $\Omega \cdot \mu$m [95]).

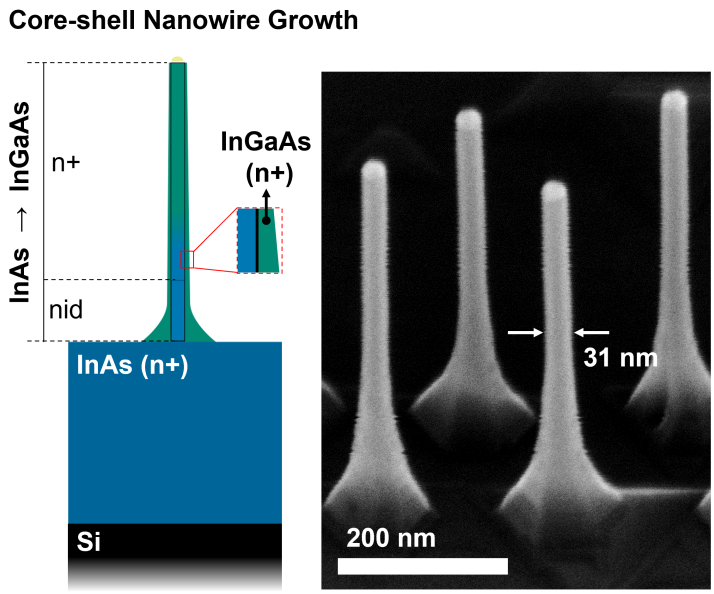

Figure 5.1: Schematic representation (cross-section) and SEM image of core-shell nanowires for optimized RF MOSFET implementation. All nanowires are based on Si substrates.

5.1.2 SIDEWALL SPACER DEVELOPMENT

Employing various techniques to limit access-resistance in a nanowire based devices typically lead to unwanted parasitic capacitance (Figure 2.7). The employed gate-last fabrication methods (section 3.2 & 4.1) achieve improved DC metrics by using a wrap around metal drain contact at the source side. However, this design is detrimental for RF-performance due to gate-drain metal overlap, separated only by a high-κ dielectric (Figure 3.9). [46] In order to further reduce gate-drain overlap capacitance C_{GD}, while avoiding added access-resistance, various spacer technologies optimized for vertical architectures need to be developed. Also, incorporating asymmetric gate-stack design using a field-plate within the high-field region, at the drain, is standard practice to achieve larger operating voltages. For instance *Intel* extends the RF capabilities of their 22-nm node by incorporating a thicker oxide at the drain (field-plate) in addition to threshold voltage engineering with lower V_T (electrostatic field-plate) closer to the drain-side. [11] Figure 5.2 show the developed sidewall spacer technology enabled by SiO_2 deposited at low temperature (plasma enhanced ALD) and anisotropic dry etching.

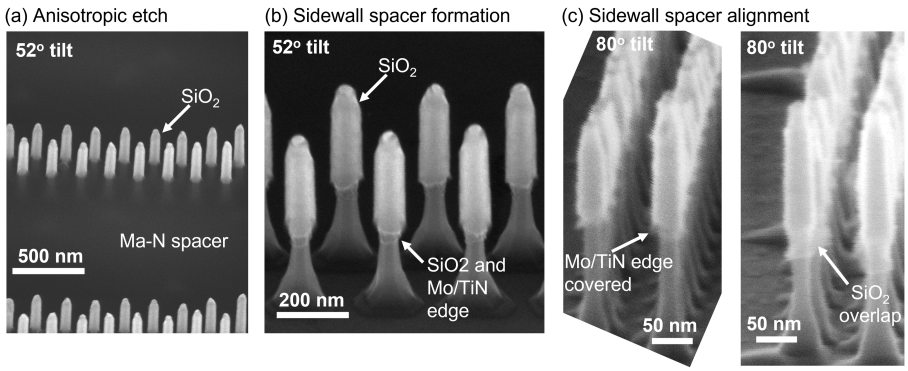

Figure 5.2: Development of gentle anisotropic dry-etch methods for clean definition of sidewall spacer. (a) Showing the results of the clean etching, where no resputtering has occurred from the polymer Ma-N mask. (b) Sidewall spacer formation after stripping the ma-N mask. Clean edges are realized for both SiO_2 as well as the top metal underneath. (c) To confirm the edge of the SiO2 the edge is characterized by SEM-imaging at a greater angle (80^o tilt).

5.1.3 VERTICAL SPACER DESIGN

For realizing circuit integration, robust and scalable manufacturing methods are necessary. Our design employs an epitaxial highly doped, ~300 nm thick,

InAs source-contact (Figure 5.1). Therefore device isolation (mesa isolation), and routing, is performed by masking and etching the InAs layer leaving significant height differences on the sample die. Here, we provide a method of employing planarization layer in conjunction with MOSFET manufacturing, see Figure 5.4. Traditionally the capacitance originating from the gate-pad are mitigated by a finger release process, forming an air bridge underneath the fingers at the mesa edge (Figure 5.4-a). However, this process requires wet etching, and is difficult to reproduce. Therefore we propose a planarization layer, here demonstrated using both S18 polymer and BCB spacer. By optimizing spin-conditions, resist viscosity and dry etching conditions a planarized film can be achieved, where the length of the protruding nanowires can be controlled with precision, see Figure 5.4-c.

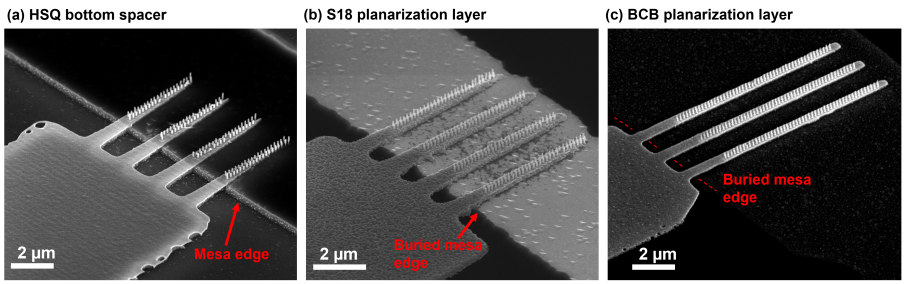

Figure 5.3: Showing the various methods for MOSFET finger definition. (a) Reduced capacitance realized by a finger-release process where the conducting path of the InAs between the pad and fingers (at the source) is released by wet etching. (b) A technique using a planarization layer is developed where the mesa can be completely buried for optimized C_{GS}. (c) Incorporation of commercially used BCB as planarization layer, where new etch processes allow for an extremely stable spacer with low capacitances.

Considering the finger design in Figure 5.4-b combined with the sidewall spacer in Figure 5.2, the gate-drain capacitance can be reduced for RF n-type V-NW MOSFETs, achieving gate-drain capacitance C_{GD} close to the limit of ~ 0.2 fF/μm established by HEMT technology [25,26,105].

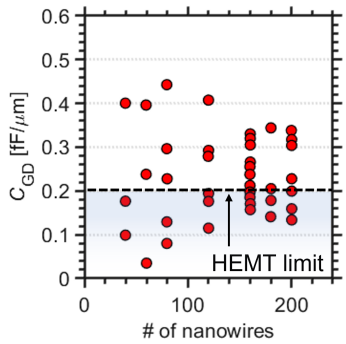

Figure 5.4: Total gate-drain capacitance C_{GD} calculated by small signal analysis of frequency dependence of scattering parameters (S-parameters) of RF optimized V-NW MOSFETs. The mean-value of all data points gives a C_{GD} of 0.24 fF/μm (23 aF/wire).

5.2 MOSFET SELECTOR DESIGN & 1T1R INTEGRATION

Design requirements for large arrays of memory cells require low capacitance to support high bandwidth and transfer speeds. Therefore, the developed sidewall spacer techniques are applicable to vertical MOSFETs employed as memory selectors. Also, vertical based memory selectors allow for simplified contact routing and smaller device footprint, resulting in potentially improved packing density. [42] For this reason, vertical based architectures are already adopted broadly in modern memory technologies. These technologies encompass NAND-Flash and traditional 6-transistor Static Random Access Memory (SRAM), where *Samsung* and *Imec* has respectively reported >200 vertically stacked NAND layers and SRAM using vertical Si nanowires with inter-pitch of 50 nm (0.0205 mm^2 cell area). [106–109] Here, we provide 3d integration of RRAM stacked on top of a vertical memory selector (InAs-based) forming a 1T1R cell, with a minimum footprint of $4F^2$ (minimum feature size F). Furthermore, progress of in-situ plasma-based surface-treatment of InAs allows for the formation of III-V interface layer oxide (IL-oxide) optimized for stable filament formation, in the RRAM dielectric stack. The addition of the IL-oxide enables a novel metal-oxide-semiconductor (MOS) based RRAM stack where the memory cell is directly integrated on an InAs nanowire for reduced complexity.

A complete device overview of the 1T1R cell is provided in Figure 5.5, including the intermediate sidewall spacer fabrication step. By incorporating a SiO_2 sidewall spacer, selective recess etching of the channel region is

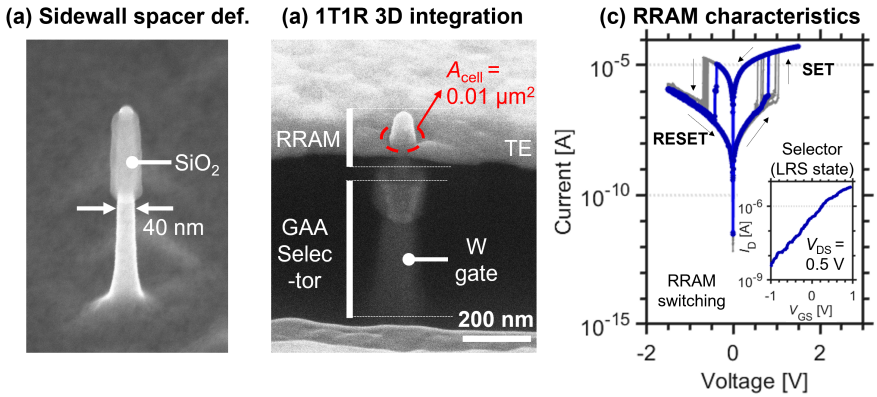

Figure 5.5: (a) Nanowire after high-k deposition where a sidewall spacer was defined and recess etching was performed to trim the channel region. (b) Final FIB-crossection of fully integrated 1T1R cell. Here consisting of a gate all around (GAA) memory selector with a integrated RRAM memristor on top. Device cell area is estimated to 0.01 μm^2. (c) 10 cycles of RRAM switching, where the selector is biased in its on-state (V_{GS} = 1 V). Inset represents transfer characteristics, at V_{DS} = 0.5 V, of GAA selector when the RRAM is biased in its LRS-state.

enabled, which is necessary for improved transistor modulation by removing expected radial Sn-doped InAs growth and restoring the intrinsic channel (Figure 5.5-a). [103] Finalizing the combined 1T1R stack including a gate-all-around (GAA) selector and RRAM directly integrated on the nanowire (MOS-stack) results in estimated footprint A_{cell} of 0.01 μm^2 (Figure 5.5-b). Furthermore, in Figure 5.5-c the RRAM switching behaviour and transistor characteristics of the GAA selector is displayed. Prior to measuring RRAM switching an initial forming cycle is needed to form the conductive filament, consisting of oxygen vacancies, within the RRAM dielectric. The forming process requires the selector to be biased at the on-state with a elevated bias ($\sim$ 3 V) applied to the RRAM top electrode. During forming the IL-oxide helps to prevent hard-breakdown of the InAs GAA selector. Namely, at the instance of filament formation the voltage drop will be shared by the IL-oxide and selector, thus the selector experience a lower bias (<3 V). The RRAM exhibit normal switching behaviour where a positive voltage $\sim$ 0.9 V applied on the top electrode (TE) initialize a SET process where the RRAM maintains a Low Resistive State (LRS $\sim$ 30 kΩ). Similairly the onset of RESET occurs at ~ -0.8 V where the memristor returns to its High Resistive State (HRS $\sim$ 100 GΩ). Utilizing a MOSFET in series with the RRAM is also an effective way

to control the compliance level during switching, in addition to preventing current sneak-paths in large array implementations. [43]

5.2.1 1T1R ARCHITECTURE BENCHMARKING

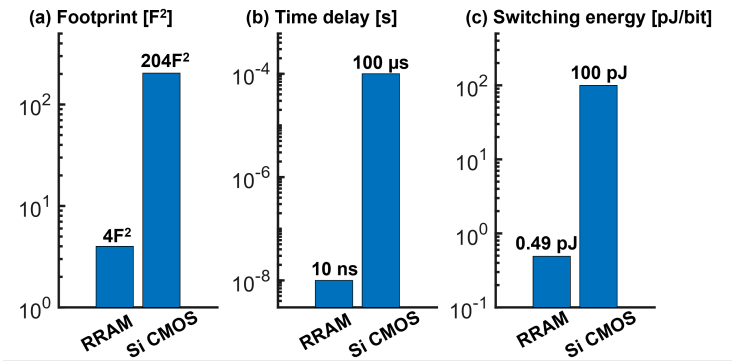

Figure 5.6: (a) Considering 2-input NAND gate and a non-volatile NAND flash element a area of $204F^2$ can be deduced when excluding metal interconnects. Therefore the 1T1R cell provides a 51x reduction as compared to traditional technology. (b) Considering propagation delay and Cu interconnect delay a 10000x reduction in delay is expected from a 1T1R cell due to eliminating intermediate data transfer. [110] (c) By only considering the NAND flash element as the major contribution to switching energy (>100 pJ/bit) [111] a 204x reduction is expected when explicitly comparing it to the proposed RRAM structure, consuming 0.49 pJ/bit. [112]

In a typical memory cross-point array the metal lines consist of two planes (upper and lower) where every intersection between the planes can potentially house a memory cell (Figure 1.2). If the distance between the metal lines, center to center, is defined as twice the minimum feature size 2F, the theoretical limit of the footprint for a single bit per cell is calculated as $2F \cdot 2F = 4F^2$. The proposed 1T1R cell thus enables a minimal footprint of $4F^2$ (1 bit/intersection), which constitutes the ultimate benchmark. Figure 5.6 provides a comparison between in memory computation using a 1T1R cell and traditional Si CMOS consisting of computations using NAND logic (2-input) stored in a non-volatile memory element (NAND flash). In Si CMOS the data has to be transferred between logic to a NAND flash unit via Cu interconnects, thus interconnect delay needs to be considered in addition to the MOSFET propagation delay. For instance, propagation delay and Cu interconnect delay (longest metal line) in 60-nm node technology is >0.1 ns and >1 ns, respectively. For more advanced nodes the transistor density

is greatly increased, therefore interconnects need to be scaled accordingly which adds resistance and further increase interconnect delay. In other words, modern processors are typically memory bottlenecked. Considering a traditional Si CMOS system paired with NAND flash, a 51x (Figure 5.6-a), 10000x (Figure 5.6-b) and 204x (Figure 5.6-c) reduction in footprint, time delay and switching energy, respectively, is expected from adopting a 1T1R architecture. [110,111,111,112]

6

Summary, Conclusions & Outlook

This thesis has explored, and progressed, vertical nanowire based III-V MOSFET technologies within CMOS, RF and memory applications. A great achievement are the developed co-integration techniques for monolithic integration of III-V CMOS, where strong performance for the individual devices are demonstrated with $g_{m,max}$ of 2.6 mS/μm (Paper I) and 0.23 mS/μm (Paper II), at $|V_{DS}| = 0.5$ V, for the n-type (InAs channel) and p-type (GaSb channel) MOSFET, respectively. The demonstrated $g_{m,max}$ of 0.23 mS/μm is the highest reported transconductance among III-V based p-type devices. This performance boost of the GaSb based devices has therefore helped to realize balanced III-V CMOS drive currents in ultrathin devices (10-20 nm diameter).

Despite the improvements, many issues needed to be addressed when optimizing for logic applications. The GaSb channel device still had limited performance with respect to I_{on} and off-state properties. By employing various studies focusing on the GaSb gate-stack (Paper III, VI, VII & VIII) the off-state properties could be addressed achieving record minimum subthreshold swing SS of 107 mV/dec (at $V_{DS} = 0.5$ V) with $\sim 6 \cdot 10^3$ current modulation (Paper VIII). Instead focusing on the III-V based n-type MOSFETs a large threshold voltage V_T spread is usually observed (MOCVD grown channel devices). [64] The origin of the V_T-shift is studied in greater detail in Paper V, where the V_T variation is shown to be mostly dependent on variation with respect to *in-situ* doping and partly due to limited precision of vertical lithography techniques (Paper V).

The research in this doctoral thesis is varied covering many applications regarding III-V based MOSFETs. The employed studies serves to validate vertical nanowire based III-V technologies by exploring various co-integration strategies, where all manufacturing methods are based on Si substrates. Ob-

serve that devices are manufactured on Si(111) substrates, which complicates integration with Si CMOS, traditionally based on Si(100) wafers. [113] However, the low temperature manufacturing (<350^{o} C) involved with narrow-gap III-Vs provide a path to realize wafer agnostic processes where, for instance, application specific III-V transistors (or selectors) can be stacked on top of fully realized Si CMOS back-end-of-line. [18]

All modern technology nodes are essentially memory bottlenecked, in other words reduced overall delay of the system is attained by addressing the memory architechture. [110, 111] In this thesis we take the first steps towards building an efficient 1T1R cross-point array for reduced delay and footprint when performing computations (Paper IV). The initial work can be easily expanded upon by further optimizing the selector design to support larger currents and greater modulation.

The natural continuation of the III-V CMOS is to build more application specific circuits. Using the lessons learned from Paper III, VI, VII & VIII the yield can be greatly improved. Also, the nanowires for the III-V CMOS can be modified to, due to similarities [114], to realize complementary TFETs, or TFET integrated with logic/amplifier circuits.

6.1 SUMMARY OF PAPERS

Here the paper topics are summarized to provide a coherent storyline and vision.

ALL III-V CMOS

Paper I: A Self-Aligned Gate-Last Process Applied to All-III-V CMOS on Si

The first demonstration of a self-aligned process used to realize monolithic co-integration of vertical p- and n-type III-V MOSFETs. This work focuses on optimizing n-type performance introducing a functional p-type MOSFET alongside. Transconductance levels up to 2.6 mS/μm ($V_{DS} = 0.5$ V) are realized for the n-type MOSFETs. The growth scheme utilized is developed by others in the group, where different gold dot sizes are used to selectively suppress GaSb growth for certain devices.

Paper II: Balanced Drive Currents in 10-20 nm Diameter Nanowire All-III-V CMOS on Si

Building on the work presented in Paper I, greatly improving p-type performance with improved transconductance at 230 μA/μm ($V_{DS} = 0.5$ V) as compared to previous work demonstrating 74 μS/μm. Here, the fabrication

methods are greatly improved which serves to scale down the channel dimensions (10 nm diameter for InAs channel device) and further simplify all processing. Also, the n-type MOSFET is adjusted to achieve the necessary off-state (I_{off} = 100 nA/μm) performance for digital applications.

GASB CHARACTERIZATION & VERTICAL P-TYPE III-V MOSFETS

Paper III: Gate-Length Dependence of Vertical GaSb Nanowire p-MOSFETs on Si

Gate-length scaling is achieved (L_g = 40 to 140 nm) for vertical and symmetrical GaSb MOSFETs. Here, a novel new fabrication method is developed to enable systematic gate-length scaling. This enables extrapolation of extrinsic source and drain resistances and estimation of the field-effect mobility (μ_h) within the GaSb nanowire ($\mu_h \sim 80$ cm^2/Vs). Other performance metrics, such as $g_{m,max}$, V_T, SS_{min}, I_{on} scales as expected according to L_g which further validates the fabrication scheme.

Paper VI: Characterization of GaSb surfaces and nanowires during oxide removal

The GaSb nanowire surface and oxidation properties are studied by XPS, enabled by high intensity x-rays from synchrotron radiation. The removal of oxides using an in-situ H_2-plasma cleaning can be tracked in real time by XPS measurement. In contrast to other studies all native oxide could be removed by H_2-plasma treatments, including the Ga-based oxides.

Paper VII: Improvement of GaSb Vertical Nanowire p-type MOSFETs on Si by Using Rapid Thermal Annealing

Building on the previous GaSb-based work in Paper I, II and III, where the effects of rapid thermal annealing vertical GaSb p-type MOSFETs are studied in detail. Two different fabrication schemes are studied closely, using a gate-first and a self-aligned gate-last process achieving transconductance up to $g_{m,max} = 149\mu$S/μm at $V_{DS} = -0.5$ V. with $L_g = 80$ nm. The various fabrication methods are modified, eliminating organic spacers, to support temperatures >350^o C to enable an annealing study with respect to MOSFET performance metrics. An optimum annealing temperature of 300^o C is discovered which provides an 50% improvement in on-currents and transconductance for the devices produced using a gate-first process.

Paper VIII: Improved Electrostatics in GaSb vertical nanowire p-MOSFETs by Employing Controllable Digital Etch Schemes

A study of surface treatment conditions comparing the use of alcohol based HCl:IPA and water based BOE 1:30 (pH neutralized) for native oxide removal and passivation of the channel material in vertical GaSb p-type MOSFETs. Implementing improved and controllable digital etch schemes (~ 1 nm/cycle) achieves the lowest reported minimum subthreshold swing of 107 mV/dec with excellent modulation properties ($I_{on}/I_{off} = 6{\cdot}10^3$). Using HCl:IPA provides the best results which is reflected in XPS measurements mapping the various oxides.

VERTICAL N-TYPE III-V NANOWIRE MOSFETS

Paper V: Doping Profiles in Ultrathin Vertical VLS-Grown InAs Nanowire MOSFETs with High Performance

By using TEM holography and a novel sweeping gate-method the doping profiles for Sn-doped VLS-grown InAs nanowires can be characterized. This is enabled by fabricating high performance (in-situ doped) InAs nanowire MOSFETs with systematically varied position of the gate-length ($L_g = 50$ nm). The varying doping profile along the nanowire gives rise to a V_T-shift. This shift is correlated and modelled to calculate the core dopant concentration with respect to nanowire position. Frequency vs transconductance measurements are also incorporated to probe the boarder traps density N_{bt}, where the N_{bt} is found to not contribute to the V_T-shifts. This study is based on high performance nanowire MOSFETs demonstrating transconductance up to 2.6 mS/μm, which increases the validity of the study. Other performance metrics such as minimum subthreshold swing SS_{min}, on-resistance R_{on} and maximum transconductance gm, max also follow the expected trend according to systematically varied gate-position.

Paper IV: High Density Logic-in-Memory using Vertical III-V Nanowires on Silicon

A 3D integrated stack consisting of an RRAM memory cell and selector is synthesized using vertical InAs nanowires. The RRAM behaviour is realized using an MOS-stack enabled by tuned in-situ plasma oxidation prior to high-k deposition and metallization. In other words, the RRAM memory could be integrated directly on top of the InAs semiconductor. The memory selector consists of an InAs nanowire MOSFET, where the III-V-based devices enable sufficient drive current (40 μA/nanowire) and tunable compliance level for RRAM switching. To realize the co-integration of transistor and RRAM (1T1R cell), a new fabrication method utilizing a SiO_2 sidewall spacer facilitates selective recess etching of the channel region as well as reduced parasitic capacitances for the final device. Notably different high-κ are used to realize

the RRAM and transistor gate-stack, respectively. Where the RRAM MOS-stack is designed to incorporate a III-V/High-κ interface oxide (consisting of native InAs-oxides) tuned by in-situ plasma oxidation, further confirmed by XPS measurements. The transistor gate-stack is instead optimized for reduced D_{it} using a bilayer Al_2O_3/HfO_2 high-κ. Excellent endurance and retention is also demonstrated for the RRAM by performing 10^6 switching cycles where the ratio between low-resistive (LRS) and high-resistive (HRS) states remains.

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APPENDICES

A

Fabrication Recipes

In this appendix, the fabrication methods are fully disclosed. All nanowire growth is accredited to Dr. Johannes Svensson who designed and executed the recipes for MOCVD gold seeded VLS-based growth. MOCVD growth is performed using Aixtron CCS 18313 reactor, with showerhead configuration. Devices are fabricated on 1 cm^2 p-type Si(111) substrates with a 260-nm-thick epitaxially grown n^{++}-InAs layer. To enable VLS-based growth a substrate is patterned by 15 nm thick gold seed particles with varying diameters from 16-44 nm depending on the application. In this work various nanowires where incorporated including: InAs-GaSb heterostructure with/without doped InAs overgrown shell, InAs-$In_{0.7}Ga_{0.3}As$ heterostructure with doped InGaAs overgrowth, and InAs with InAs doped overgrowth.

A.1 CMOS GATE-LAST PROCESS

A.1.1 TOP METAL DEFINITION & FIRST SPACER

- Spin on HSQ (60s at 3000 RPM)
- 2 min bake 200^o C hotplate
- EBL exposure (dose 195:5:215 $\mu C/cm^2$)
- 15 nm W sputtering
- 3 nm PEALD TiN deposition at 250 degree
- Anisotropic W/TiN dry etch (SF_6, C_4F_8, and Ar at 20 mTorr)

- BOE 1:10 to remove the HSQ
- HF 1:1000 HSQ thinning 60 – 120s

A.1.2 DIGITAL ETCHING AND HIGH-K DEPOSITION

- Oxidation in O_2 chamber *or* 2 min O^3 oxidation at RT
- 30s HCl:IPA 1:10 dip
- High-k deposition
  - Surface cleaning with 5 cycles of TMAl
  - 6 cyclesAl_2O_3 deposition at 300 degrees
  - o 36 cycles HfO_2 deposition at 120 degrees

A.1.3 GATE DEFINITION & GATE PAD

- 60 nm thick W sputtering with 16 sccm Ar flow
- Spin on S1813 resist (60s at 4000 rpm)
- Bake at 120 degrees for 10 min
- Thinning the S1813 resist using O_2 plasma (O_2 RIE at 300 mTorr)
- Gate-metal etch (SF_6:Ar RIE at 185 mTorr)
- S1813 resist removal in acetone
- Spin on S1813 resist (60s at 4000 rpm)
- Bake at 115 degrees for 90 s
- Soft UV to define gate-pad pattern (hard contact)
  - MF319 development
  - 30 s O2 plasma descum

A.1.4 MESA DEFINITION (OPTIONAL)

- Spin on 495 PMMA A8 (60 s at 3000 rpm)
- Bake at 180^o C 300 s
- Definition of puncture holes at isolation MESA edge in EBL (560 $\mu C/cm^2$)

- Spin on S1813 resist (60s at 4000 rpm)
- Bake at 115^{o} C for 90 s
- Soft UV to define isolation MESA pattern (hard contact)
  - MF319 development 90s
  - 30 s O2 plasma descum
- InAs etch by H_3PO_4:H_2O_2:H_2O (1:1:25)
- Remove S1813 in acetone

A.1.5 SPACER 2 AND VIA HOLES

- Spin on S1813 resist (60s at 4000 rpm)
- Bake at 200^{o} C for 40 min
- Thinning the S1813 resist using O^2 plasma (O^2 RIE at 300 mTorr)
- Confirm S1813 thickness using SEM inspection
- HF 1:100 high-k etching 2 min alt. BOE 1:10 4 min
- Spin on S1813 resist (60s at 4000 rpm)
- Bake at 115 degrees for 90 s
- Soft UV to define source and via hole mask (hard contact)
  - MF319 development 90s
  - 30 s O2 plasma descum
- Resist ashing S1813 resist using O2 plasma (O2 RIE at 300 mTorr)
- High-k etching using BOE (1:10) for 4 min
- S1813 resist removal in acetone

A.1.6 TOP CONTACT

- Metal sputtering of Ni/W/Au, thickness 5/15/200 nm at Ar flows 9/15/9 sccm
- Spin on S1813 resist (60s at 4000 rpm)
- Bake at 115 degrees for 90 s

- Soft UV to define source and via hole mask (hard contact)
  - MF319 development 90s
  - 30 s O2 plasma descum
- Gold wet etch 35 s using KI-based Au etch
- W etch (SF_6:Ar RIE at 185 mTorr)
- S1813 resist removal in acetone
- Ni etch using H_2O:H_2SO_4:HNO3:CH3COOH (10:5:5:2) for 50s

A.2 P-TYPE MOSFET GATE-LAST PROCESS

A.2.1 METAL ENCASING

- 30 nm thick W sputtering with 16 sccm Ar flow
- Spin on ma-N 2405 (60s at 3000 rpm)
- Bake at 95 degrees C for 3 min
- EBL exposure (dose 90:5:170 uC/cm2)
  - o ma-D 432S development for 60 s
- 10 nm TiN sputtering with 90 sccm Ar flow
- Anisotropic TiN dry etch (SF_6, and N_2 at 10 mTorr)
- 45s O_2 plasma cleaning
- Remove ma-N in acetone

A.2.2 SOURCE AND DRAIN DEFINITION

- Spin on S1813 resist (60s at 4000 rpm)
- Bake at 120^o C for 10 min
- Thinning the S1813 resist using O2 plasma (O2 RIE at 300 mTorr)
- Confirm S1813 thickness using SEM inspection (exposed gate-region)
- Isotropic W dry etch (SF_6, and N_2 at 10 mTorr)
- 45s O_2 plasma cleaning
- Remove S1813 in acetone

A.2.3 FIRST SPACER & GATE DEFINITION

- High-k deposition
  - Surface cleaning with 5 cycles of TMAl
  - 40 cycles Al_2O_3 deposition at 300^o C
- Spin on S1813 resist (60s at 4000 rpm)
- Bake at 200 degrees for 40 min
- Thinning the S1813 resist using O2 plasma (O2 RIE at 300 mTorr)
- Confirm S1813 thickness using SEM inspection (exposed gate-region)
- 30 nm thick W sputtering with 16 sccm Ar flow
- Spin on S1813 resist (60s at 4000 rpm)
- Bake at 120 degrees for 10 min
- Thinning the S1813 resist using O2 plasma (O_2 RIE at 300 mTorr)
- Confirm S1813 thickness using SEM inspection
- Gate-metal etch (SF_6:Ar RIE at 185 mTorr)
- S1813 resist removal in acetone
- Spin on S1813 resist (60s at 4000 rpm)
- Bake at 115 degrees for 90 s
- Soft UV to define gate-pad pattern (hard contact)
  - MF319 development
  - 30s O_2 plasma descum
- Gate-metal etch (SF_6:Ar RIE at 185 mTorr)
- S1813 resist removal in acetone

A.2.4 SECOND SPACER & VIA HOLES

- Spin on S1813 resist (60s at 4000 rpm)
- Bake at 200 degrees for 40 min
- Thinning the S1813 resist using O2 plasma (O2 RIE at 300 mTorr)
- Confirm S1813 thickness using SEM inspection
- HF 1:100 high-k etching 2 min alt. BOE 1:10 4 min
- Spin on S1813 resist (60s at 4000 rpm)
- Bake at 115 degrees for 90 s
- Soft UV to define source and via hole mask (hard contact)
  - MF319 development 90s
  - 30 s O2 plasma descum
- Resist ashing S1813 resist using O2 plasma (O2 RIE at 300 mTorr)
- High-k etching using HF 1:100 for 2 min
- S1813 resist removal in acetone

A.2.5 TOP CONTACT

- Metal sputtering of Ni/W/Au, thickness 5/15/200 nm at Ar flows 9/15/9 sccm
- Spin on S1813 resist (60s at 4000 rpm)
- Bake at 115 degrees for 90 s
- Soft UV to define source and drain pads (hard contact)
  - MF319 development 90s
  - 30 s O2 plasma descum
- Gold wet etch 35 s using KI-based Au etch
- W etch (SF6:Ar RIE at 185 mTorr)
- S1813 resist removal in acetone
- Ni etch using H_2O:H_2SO_4:HNO_3:CH_3COOH (10:5:5:2) for 50s

A.2.6 HYDROGEN PLASMA RECIPE

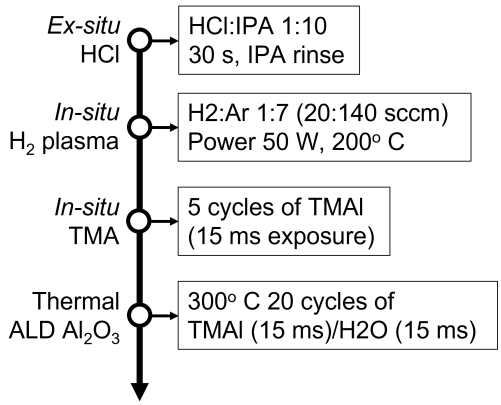

Figure A.1: H_2-plasma recipe designed for optimal pre-treatment of GaSb. Used in Fiji - Plasma Enhanced ALD tool.

PAPERS

Paper I

Paper I

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A. Jönsson, J. Svensson, and L.-E. Wernersson, "A Self-Aligned Gate-Last Process Applied to All-III–V CMOS on Si," *IEEE Electron Devices Letters*, vol. 39, pp. 935-938, June 2018, DOI: 10.1109/LED.2018.2837676.

A Self-Aligned Gate-Last Process Applied to All-III–V CMOS on Si

Adam Jönsson, Johannes Svensson, and Lars-Erik Wernersson

***Abstract*— Vertical nanowire n-type (InAs) and p-type (GaSb) transistors are co-processed and co-integrated using a gate-last process, enabling short gate-lengths (L_g = 40 nm) and allowing selective digital etching of the channel. Two different common gate-stacks, including various pre-treatments, were compared and evaluated. The process was optimized to achieve high n-type performance while demonstrating p-type operation. The best n-type device is scaled down to 12-nm diameter and has a peak transconductance of 2.6 mS/μm combined with a low R_{on} of 317 $\Omega \cdot \mu$m, while the p-type exhibits 74 μS/μm. In spite of increased complexity due to co-integration, our n-type InAs transistors demonstrate increased drive current, 1.8 mA/μm, compared with earlier publications.**

***Index Terms*— Vertical, nanowire, III-V, MOSFET, CMOS, InAs, GaSb.**

I. Introduction

COMPLEMENTARY metal-oxide-semiconductor (CMOS) circuits based on all-III-V channel materials require further development to achieve competitive p-type performance [1], [2]. Although antimonide-based materials such as GaSb have demonstrated high hole mobility [3], transistor performance is, in part, limited by the gate-stacks [4]–[6]. It has been suggested that combinations of a more conventional p-type SiGe channel combined with n-type III-V InGaAs channel is a viable alternative to current CMOS technology [7], [8]. This type of material integration is, however, not straightforward, mainly due to strong material selectivity during processing.

With continued transistor scaling, deteriorated electrostatics leads to various short channel effects [9]. Vertical nanowires with a gate-all-around (GAA) geometry is one alternative with beneficial performance at the 5 nm node [10]. The vertical nanowire geometry in particular decouples the gate length and contact geometry from the footprint area [11].

In this letter, GaSb p-type and InAs n-type MOSFETs are co-integrated in a vertical nanowire gate-all-around structure, utilizing a common gate-stack. The process uses hydrogen silsequioxane (HSQ) spacers with adjustable thickness for development of a self-aligned, gate-last, process compatible with vertical antimonide-based structures.

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Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

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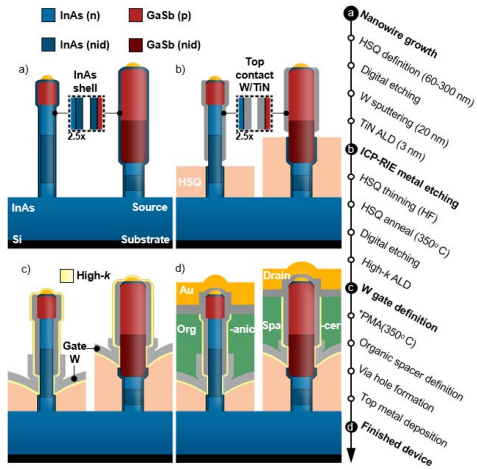

Fig. 1. Schematic illustration of crucial steps in the full process flow attached with an overview of fabrication. The illustrations show nid-channel devices, notice that the process allows for varying gate placement along the nanowire. * Post metal anneal (PMA) is performed only on specific samples.

II. Device Fabrication

Fig. 1 schematically illustrates the process flow for co-integration of p-type GaSb and n-type InAs MOSFETs. The devices are fabricated on 1 cm^2 p-type silicon (111) substrates with a 260 nm epitaxially grown InAs layer [14].

InAs-GaSb nanowires are subsequently grown from 15-nm-thick Au seed particles defined by electron beam lithography (EBL). Sections of the InAs segment is n-doped by Sn and the top of the GaSb segment is p-doped by Zn, see Fig. 1. In the case of GaSb growth, background doping is present attributed to point defects ($\sim 10^{16}$) [15]. By utilizing the Gibbs-Thomson effect during VLS growth,

TABLE I
SAMPLE DESCRIPTION

Sample	Sample A	Sample B
Top contact formation[1]	Ozone oxidation + citric acid 60 s + W/TiN	Ozone oxidation + citric acid 60 s + 1:500 + $(NH_4)_2S$:H_2O 3 min
Gate-stack Pre-treatment	HCL:IPA + 5x TMAl pulses	Citric acid + 8x {TMAl pulse and H_2 plasma}
High-k	[2]6/36 cycles Al_2O_3/HfO_2 EOT = 0.85 nm	[3]40 cycles HfO2 (+PMA) EOT = 0.76 nm
n-type		
doping	nid-channel	n-channel
L_g	50 nm	40 nm
diameter	20 nm	12 nm
$g_{m,peak}$	1.2 mS/μm	2.6 mS/μm
SS_{lin}	74 mV/dec	191 mV/dec
R_{on}	1039 Ω·μm	317 Ω·μm
p-type		
L_g	70 nm	100 nm
diameter	40 nm	38 nm
$g_{m,peak}$	74 μS/μm	11 μS/μm
SS_{lin}	273 mV/dec	622 mV/dec
R_{on}	5.9 kΩ·μm	20 kΩ·μm

Description of processing variations for two different samples highlighting the critical steps involved. An overview is given for the important performance metrics. $g_{m,peak}$ is extracted at drain bias $|V_{ds}|$=0.5 V and SS_{lin} at $|V_{ds}|$=0.05 V.

[1]Contact annealing, post top metal definition, has been performed at 350 degrees C for 60 minutes (Fig. 1). [2]Al_2O_3 (TMAl) and HfO_2 (TDMAHf) is deposited at 300 °C and 120°C respectively. [3]In situ remote plasma treatment of the surface is carried out inside the ALD chamber and HfO_2 (TDMAHf) is deposited at 250°C. Additional post metal anneal (PMA) at 350°C is also performed after gate-definition on sample B.

the GaSb growth rate can be reduced for smaller gold particle sizes [16] (diameter <30 nm) which enables length control of the two separate materials in the heterojunction nanowires [17]. Therefore, 24 nm and 28 nm diameter Au dots are used for growing n-type wires and 44 nm for p-type wires. The Au dots are patterned in structures with a pitch of about 300 nm.

In the first step, the top contact is defined with an HSQ mask, whose thickness is determined by the dose in an EBL process [9]. The thicknesses of the HSQ is gradually varied from 60 to 300 nm to define gate position in separate devices. The InAs shell on the protruding part of the nanowires, that will later constitute the top contact, is digitally etched by oxidation and citric acid treatment. An ammonium sulfide treatment is also used for some of the samples, to passivate the III-V surface [18], processing differences are outlined in Table I. Subsequently, 20 nm tungsten (W) is sputtered followed by a 3 nm TiN atomic-layer-deposited (ALD) film. The metal is removed from all planar surfaces by an ICP-RIE SF_6:C_4F_8 based dry-etch process leaving metal on the nanowire sidewalls defining the top metal contact.

The same HSQ mask is also used as a bottom spacer by thinning it with a diluted HF (1:1000) wet etch so that the nanowire part that constitutes the channel protrudes. This method allows for sub-100 nm gate-length definition. The exposed semiconductor surface is digitally etched by oxidation followed by either citric acid or an HCL:IPA (1:30) treatment. The number of digital etch cycles are adjusted to remove the overgrown doped InAs shell, restoring the core channel material for the p- and n-type wires, that finishes the gate recess.

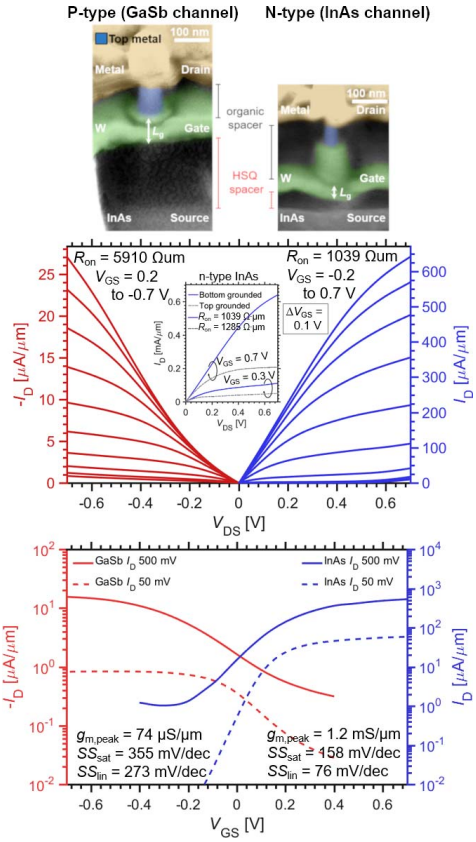

Fig. 2. Falsely colored SEM-images depicting single nanowires inside a p-type and n-type structure for Sample A (Table I), highlighting the different HSQ thickness. Combined transfer and output characteristics is presented for a selected p- and n-type device. The n-type (nid-channel) device consists of 184 nanowire array with a pitch of 300 nm, diameter of 20 nm, and L_g = 50 nm. The p-type consists of 144 nanowires with a pitch of 350 nm, diameter of 40 nm, and L_g = 70 nm. Increased resistance is shown in R_{on} by switching drain and source to realize a top grounded configuration.

To optimize the processing conditions, two types of high-k are compared, a conventional bi-layer Al_2O_3/HfO_2 [19] and a pure HfO_2 dielectric. The HfO_2 only gate-stack is preferred for aggressive EOT scaling [20]. High temperature (≥250 °C) is necessary when forming the interface layers for more effective self-cleaning [19], [21]. The different high-k with corresponding pre-treatments are described further in Table I, representing the best optimization for GaSb p-type (Sample A) and InAs n-type (Sample B) device performance.

The gate metal is deposited by sputtering 60 nm W. A thinned S1813 spacer is used as mask for an SF_6 dry-etch process to vertically align the gate to the top contact. An organic spacer is then applied followed by sputtering of the top metal electrode consisting of Ni/W/Au.

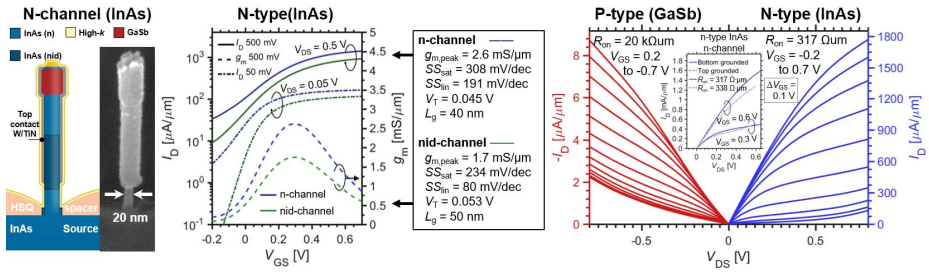

Fig. 3. Comparison between 184 nanowire arrays with $L_g = 40$ and $L_g = 50$ nm from sample B (Table I). Output characteristics of the p-type device in Sample B is also included. The SEM image is showing a 12 nm diameter nanowire, with doped channel (n-channel) after in-situ hydrogen plasma and high-k ALD comprised of 40 cycles HfO_2 corresponding to 4 nm thickness,. The lower curve of each curve-pair (n-type InAs) corresponds to a, not intentionally doped, nid-channel. The HSQ spacer thicknesses for n- and nid-channel devices are 10 and 50 nm, respectively. Contact resistance behaves symmetrically with closely matched R_{on} values for switched bias conditions, due to improved contact processing.

The implemented InAs-Gasb combination introduces a tunneling source contacts with broken bandgap, for the p-type device, where reported values suggest that it may have sufficiently low resistivity (Esaki diodes: $\sim 260\ \Omega \cdot \mu$m) [22], [23]. Thus the InAs-GaSb structure, due to resemblance with state-of-the-art Tunnel-FETs [24], [25], lends itself for future CMOS Tunnel-FET implementations including co-integration of MOSFETs and Tunnel-FETs.

III. Device Characterization

Transfer and output characteristics for sample A with a bi-layer gate-stack is presented in Fig. 2. Transconductance $g_{m,peak}$ values of 1.2 mS/μm for n-type and 74 μS/μm for p-type was achieved with minimum subthreshold slope SS_{lin} of 74 and 271 mV/dec. Both devices exhibit enhancement mode operation with $V_T = 0.08$ and -0.02 V. The limited n-type off-state performance is partly caused by drain tunneling due to the narrow bandgap of InAs [26]. However, for the p-type GaSb device the large diameter of the gate-segment in conjunction with a non-optimal high-k interface degrades the off-state. The 24 times higher drive current for the n-type as compared to the p-type MOSFET is expected due to the large difference in charge carrier mobility [2]. Further, significant gate-length scaling and strained GaSb channels are needed to enable the p-type MOSFET semi-ballistic operation [27], [28].

The resistance originating from the top contact is reduced for the n-type device in sample B (Table I) by adding a sulfur passivation step during the top contact definition, which increases the on-state performance, $g_{m,peak} = 2.6$ mS/μm (n-channel), Fig. 3. This is further quantified by switching the source and drain electrodes during measurement that displays a symmetrical behavior with low R_{on} values of 317 and 338 $\Omega \cdot \mu$m, in contrast to the n-type device in sample A (Fig. 2 inset). This device also utilizes a pure HfO_2 gate-stack with low EOT of 0.76 nm, see Table I. The off-state and electrostatics are limited, which can be attributed to a doped channel and a high-temperature deposition of HfO_2 at 250 °C [29]. The hysteresis window corresponding to the gate-stack is evaluated to 20 mV, on a representative device, at the minimum SS point ($V_{ds} = -0.2$ to 0.7 V). An additional device with nid-channel, based on the same type of nanowire that has a gate shifted upwards along the nanowire, is also available on the same sample and is presented in Fig. 3. Here, improved electrostatics is shown with SS_{lin} decreased from 191 (n-channel) to 80 mV/dec (nid channel). Even though H_2-plasma on InAs may result in increased surface roughness we find that high transconductance values still can be obtained. The n-type devices, on sample B, with peak transconductance $g_{m,peak}$ of 2.6 (n-channel) and 1.7 mS/μm (nid-channel), at $V_{ds} = 0.5$ V, indicate added source resistance due to varied HSQ spacer thickness. The spacer is varied from 10 (n-channel) up to 50 nm (nid-channel), see Fig. 3. Notably the saturation current for the device with doped n-channel is 1.8 mA/μm at $V_{gs} = 0.7$ V. The improved drive current, compared to previous InAs transistor iterations, can be attributed to the addition of doping at the bottom nanowire-segment [12] and n-doped shell growth [13]. The p-type device is demonstrated although with reduced performance and electrostatics as compared to the n-type device quantified by $g_{m,peak} = 11$ μS/μm ($V_{ds} = -0.5$ V) and $SS_{lin} = 622$ mV/dec, see Table I.

IV. Conclusions

A new process for n-type (InAs) and p-type (GaSb) MOSFET co-integration compatible with highly sensitive antimonide-based materials has been developed. Aggressively scaled devices with sub-100 nm gate-lengths and n-type diameters down to 12 nm have been demonstrated using gate-stack variation, giving a highest $g_{m,peak}$ of 2.6 mS/um, see Table I. P-type devices, demonstrating $g_{m,peak}$ of 74 and 11 uS/um, are also co-integrated on the same samples. Further optimization of the GaSb gate-stacks combined with aggressive diameter scaling will increase the balance for the III-V CMOS. The HSQ-spacer utilization allows for future integration of p- and n-type on the same nanowire, ultimately reducing the diameter difference between the devices. The process also enables possibilities for co-integrating MOSFETs with state-of-the-art Tunnel-FETs.

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Paper II

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Balanced Drive Currents in 10-20 nm Diameter Nanowire All-III-V CMOS on Si

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***Abstract*—**We use a self-aligned, gate-last process providing n-type (InAs) and p-type (GaSb) MOSFET co-integration with a common gate-stack and demonstrate balanced drive current capability at about 100 µA/µm. By utilizing HSQ-spacers, control of gate-alignment allows to fabricate both n- and p-type devices based on the same type of vertical heterostructure InAs/GaSb nanowire with short gate-lengths down to 60 nm. Refined digital etch techniques, compatible with both sensitive antimonide structures and InAs, enable channel region diameters down to 16 nm for GaSb and 10 nm for InAs. Balanced performance is showcased for both n- and p-type MOSFETs with I_{on} = 156 µA/µm, at I_{off} = 100 nA/µm, and 98 µA/µm, at $|V_{DS}|$ = 0.5, respectively.

I. Introduction

High mobility materials such as narrow band gap III-V compounds offer a possibility to increase the MOSFET performance for both logic and high-frequency devices. Specifically InAs and GaSb material options present high bulk mobility for electrons and holes, respectively, which makes the combination attractive for CMOS implementation. GaSb based transistor performance is currently limited by the gate-stacks and the reactive nature of the antimony-compounds imposes challenges in both material growth as well as device fabrication. [1]

The continuation of the traditional down-scaling of MOSFETs for digital circuits has led to short channel effects due to deteriorated electrostatics [2]. 3D gate architectures are therefore proposed, and implemented, with gate-all-around (GAA) structures utilizing vertical nanowires as a strong candidate. Fundamentally, vertical nanowire MOSFETs presents a seamless way to decouple gate-length and contact geometry from the device footprint area. The small footprint also allows larger lattice mismatch without propagating defects, which simplifies integration of high mobility materials on top of Si substrates. [3]

In this work, we demonstrate a streamlined co-integration process for p- and n-type MOSFETs, with a common gate-stack, using a self-aligned, gate-last process. State-of-the-art vertical p-type GaSb MOSFET performance is demonstrated, with g_m = 230 µS/µm, co-integrated with a strong InAs n-type device showcasing good off-state with I_{on}=156 µA/µm at I_{off} = 100 nA/µm, all at $|V_{DS}|$ = 0.5 V (**Table 1**). The data includes 5x drive current improvement for the GaSb MOSFET combined with a 3x increase in g_m as well as a decreased SS_{min} as compared to previous results [4]. The improvement is attributed to adjustment in the aspect ratio (Diameter:L_g) for the n-type and p-type devices, from 2:5 and 2:4 to 2:30 and 2:6, respectively, in order to achieve balanced drive currents. For the n-type device this has resulted in improved off-state characteristics reaching the I_{off} = 100 nA/µm limit and simultaneously the p-type current has been improved with a 5 times higher I_{on} of 98 µA/µm (**Table 2**).

II. Device Fabrication

The processed MOSFETs are based on vapor-liquid-solid (VLS) grown InAs-GaSb heterostructure nanowires overgrown with, a highly n-doped InAs shell. The implementation of an overgrown shell protects the GaSb, which circumvents issues regarding etch selectivity and enables processing with hydrogen silsesquioxane (HSQ) allowing development of a self-aligned, gate-last process. Optimization of alcohol based digital etching, in conjunction with the gate last implementation, has enabled scaled diameters and selective digital etch of the channel region. Therefore, GaSb devices with diameters down to 16 nm have been achieved, which has proven crucial for improved performance.

Fig. 1 represents the critical fabrication steps for the co-integration process. The devices are based on 260 nm epitaxial InAs layer grown on p-type silicon (111) substrates. Subsequently, InAs-GaSb nanowires are grown by VLS from EBL defined 32 nm diameter Au discs. The top of the InAs segment and GaSb segment is doped by Sn and Zn, respectively. The nanowires are also overgrown with an InAs shell for improved etch selectivity (**Fig 1-a**).

After nanowire growth, an HSQ mask is applied whose thickness is controlled by the EBL exposure dose. The thickness control allows for varied gate-position along the nanowire, enabling p- and n-type devices to be fabricated from the same type of nanowires. The spacer is used as a template to align the top metal, which is applied by 200 nm sputtered W and 3 nm ALD TiN (**Fig. 1-b**). Prior to metal deposition, a citric acid dip is performed followed by HCL:IPA to remove the protruding InAs shell and restore the core-material. The applied metal is selectively removed from the planar surfaces by reactive ion etching leaving the finished top contact.

The HSQ mask, previously used for top contact alignment, is thinned by diluted HF 1:400 to form the bottom spacer and to expose the nanowire channel-region. The channel region is selectively digitally etched by 4 cycles of short ozone exposure followed by HCL:IPA 1:30 wet etch. The digital etch removes the InAs shell and further serves to trim the channel down to sub 25 nm diameters. A bilayer high-k is applied consisting of

6 cycles of Al_2O_3 and 36 cycles of HfO_2, corresponding to an EOT of 0.85 nm (**Fig. 1-c**). The result after high-k deposition is shown in **Fig 2**, presenting before and after SEM images of a single nanowire p-type device.

Finally, 60 nm sputtered tungsten is used as gate metal and the top edge aligned vertically by a back etched S1813 resist as etch mask for an SF_6 dry etch. Afterwards an organic top spacer is defined followed by sputtering of the top contact consisting of Ni/Au (15/200 nm), see **Fig. 1-d**.

III. Measurements

Fig. 3 and **Fig. 4** represent combined output and transfer characteristics for InAs (L_G = 150 nm, diameter = 10 nm) and GaSb (L_G = 60 nm, diameter 22 nm) channel devices, co-integrated on the same Si substrate. The data are showcasing well behaved characteristics with maximum g_m = 405 and 230 µS/µm, respectively, normalized to the total circumference, see **Table 1**. A high I_{on} = 156 µA/µm (at I_{off} = 100 nA/µm) is also achieved for the n-type device, representing a 14% improvement compared to previous vertical InAs MOSFETs [5]. Both the n- and p-type devices showcase good electrostatics with SS_{lin} = 72 and 175 mV/dec, attributed to the aggressive diameter scaling (**Fig. 5** and **Fig. 6**) and high-quality semiconductor/high-*k* interfaces. Also, the minimum subthreshold slope is maintained over a wide bias range for the n-type device (**Fig. 6**), demonstrated that the co-integration process does not introduce a drastic increase in D_{it} for InAs. Notice that the InAs transistor is fabricated from a 200 nm long InAs segment, which introduces significant constraint on contact formation contributing to a comparably high R_{on} = 1.4 kΩ·µm for the n-type MOSFET. For the p-type device, contributions to the contact resistance from rapid re-oxidation of GaSb and injection via a, not optimized, broken bandgap source serves to further limit the on-state performance. The limited off-state can be attributed to background doping in the GaSb channel (**Fig. 7**). [6]

To demonstrate the improved digital etch technique and technology scalability, a p-type device with diameter down to 16 nm, although with longer gate-length of 150 nm is shown in **Fig. 8**. Alcohol based digital etch techniques enable the aggressive diameter scaling. Notice the large difference between top contact diameter with respect to the channel region, which improves resistance originating from the drain contact. The device transfer characteristics is presented in **Fig. 9**, showing that a high transconductance of 87 µS/µm can be maintained also when the diameter is scaled. Notably, the performance of GaSb p-MOSFETs strongly depends on the gate length. Also the off-state performance is improved, quantified by SS_{sat} = 257 mV/dec (**Fig. 10**). The output characteristics for this device (**Fig. 11**) showcase an exponential behavior that indicates the presence of a potential barrier (**Fig. 12**) which can be resolved by further contact optimization.

To visualize the performance improvements as compared to previous GaSb, as well as InGaSb, devices a g_m versus SS_{sat} plot is presented in **Fig 12**. Here, importance of scaling the gate-length and diameter is clearly emphasized. With a balance between *SS* and g_m metrics also at scaled gate lengths, this work shows improved performance over state-of the-art GaSb MOSFETs, including InGaSb fin-FETs. [1]

IV. CMOS implementations

Many alternative co-integration strategies have been proposed and implemented utilizing the same material combination, namely InAs and GaSb, see **Table 2**. One approach is to use nano-ribbons with a two-step transfer technique. [7] The same technique, utilizing nano-ribbons, with a single transfer step has also been developed and demonstrated. [8] Another method is to use grown periodic InAs-GaSb planar structure with selectively etched segments enabling fabrication of separate lateral GAA InAs and GaSb devices. [9] The CMOS implementation presented in this work, based on vertical InAs-GaSb heterostructure nanowires, on top of Si, [10] has the potential to include heterostructure InAs-InGaAs segments [11] to reduce the off-state leakage and to further increase the transconductance. [4] In fact, we show a technology that can merge high transconductance n-type MOSFETs [11] with balanced CMOS implementation for high-speed logic and mixed applications.

From the benchmarking of various all-III-V CMOS implementations in **Table 2,** we note that the implementation presented in this work, represents the best set of combined metrics including g_m vs SS_{sat}. We show that competitive device performance can be achieved within a co-integrated process, challenging other state-of-the-art III-V devices.

V. Conclusions

We present an all-III-V co-integration process aggressively scaled to gate-lengths (L_G = 60 nm) and diameters (D_{InAs} = 10 nm, D_{GaSb} = 16 nm). This has served to reach balanced drive-currents for the III-V CMOS at 156 and 98 µA/µm for the n- and p-type devices respectively (**Table 1**) as well as demonstration of competitive transistor performance.

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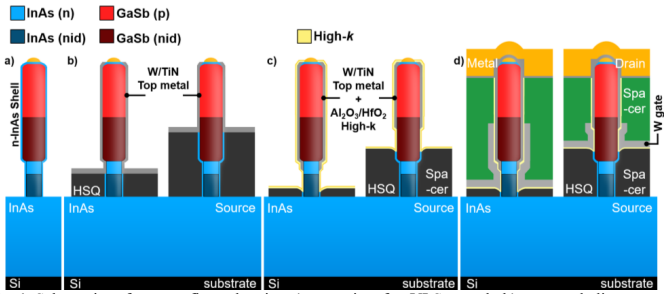

Fig. 1. Schematics of process flow, showing a) nanowire after VLS growth, b) top metal alignment, c) first spacer and high-k deposition, and d) final structure with contacts.

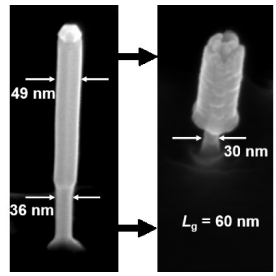

Fig. 2. SEM-image of a nanowire prior to processing and after first spacer and high-k deposition, see Fig. 1-c.

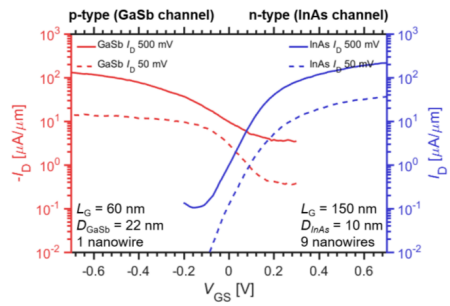

Fig. 3. Combined transfer characteristics for p-type single nanowire GaSb device (L_G = 60 nm, diameter 22 nm) and 9 nanowire n-type InAs device (L_G = 150, diameter 10 nm).

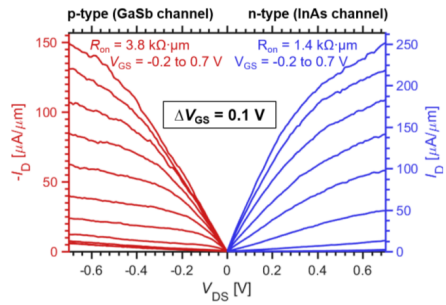

Fig. 4. Combined output characteristics for p-type single nanowire GaSb device (L_G = 60 nm, diameter 22 nm) and 9 nanowire n-type InAs device (L_G = 150, diameter 10 nm).

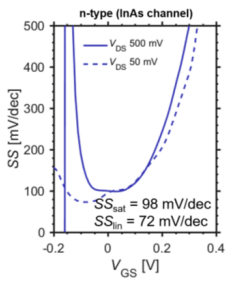

Fig. 5. SS_{sat} and SS_{lin} for the device consisting of 9 nanowires, with L_G = 150 nm and diameter 10 nm.

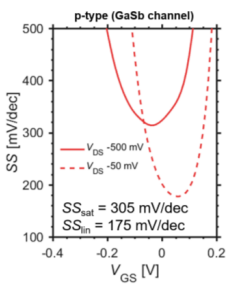

Fig. 6. SS_{sat} and SS_{lin} for the single nanowire device, with L_G = 60 nm and diameter 22 nm.

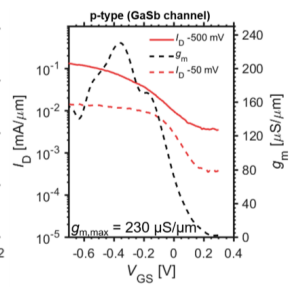

Fig. 7. Transfer characteristics and transconductance g_m for the single nanowire device with L_G = 60 nm and diameter 22 nm. A $g_{m,max}$ of 230 μS/μm is demonstrated.

	n-type	p-type
I_{on} [μA/μm]	156	98
g_m [μS/μm]	405	230
L_G [nm]	150	60
SS_{sat} [mV/dec]	98	305
SS_{lin} [mV/dec]	72	175

Table 1. Summary of DC-metrics for the all-III-V CMOS process. I_{on} defined at I_{off} = 100 nA/um for the n-type device and at V_{DS} = -0.5 V for the p-type device.

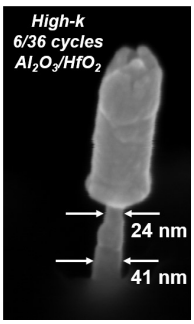

Fig. 8. SEM-image showcasing a diameter of 16 nm (+ 8 nm high-k) inside a 2-nanowire p-type device.

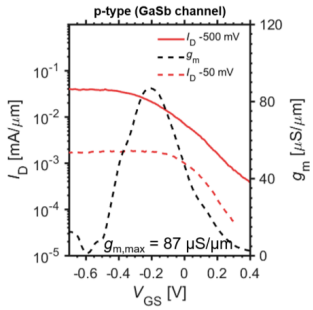

Fig. 9. Transfer characteristics for the 2-nanowire device, with L_G = 150 nm and diameter 16 nm.

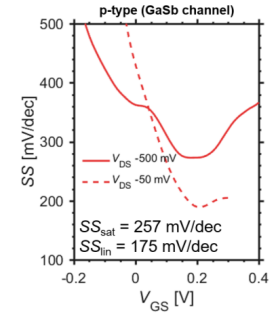

Fig. 10. SS_{sat} and SS_{lin} for the 2-nanowire device, with L_G = 150 nm and diameter 16 nm.

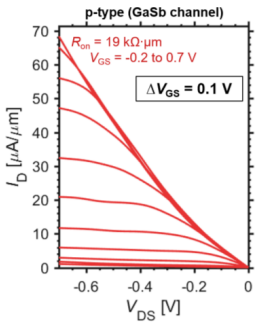

Fig. 11. Output characteristics for the 2-nanowire device, with L_G = 150 nm and diameter 16 nm.

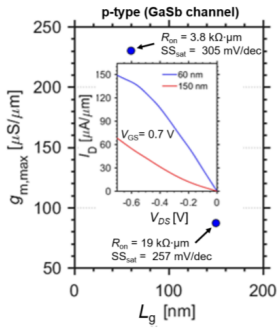

Fig. 12. The $g_{m,max}$ dependence of L_G for the single nanowire and the 2-nanowire p-type device. The inset highlights the difference at the on-state.

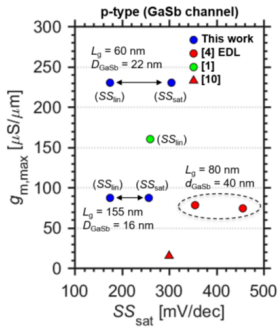

Fig. 13. Benchmarking with respect to GaSb and InGaSb p-type devices.

	III-V CMOS						III-V CMOS					
	n-type [This work]	**n-type EDL [4]**	**n-type [9]**	**n-type [7]**	**n-type [8]**	**n-type [5]**	**p-type [This work]**	**p-type EDL [4]**	**p-type [9]**	**p-type [7]**	**p-type [8]**	**p-type InGaSb [1]**
I_{on} [µA/µm]	156			80	4	140	98	17	10	22	2.4	~100
g_m [µS/µm]	405	1200				640	230	74				160
L_G [nm] /Crit.Dim	150 /10	50 /20	500 /20	/13	/2.5	50 /28	60 /22	80 /40	500 /20	/7	/20	20 /10
SS_{sat} [mV/dec]	98	158	185	84		158	305	355		156		
SS_{lin} [mV/dec]	72	76					175	273				260

Table 2. Benchmarking table with devices from other III-V CMOS processes as well as key p- and n-type standalone processes. I_{on} for InAs devices defined at I_{off} = 100 nA/um limit and for GaSb/InGaSb p-type devices is defined at V_{DS} = -0.5 V. Blank spaces are due to incomplete data.

Paper III

Paper III

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Gate-Length Dependence of Vertical GaSb Nanowire p-MOSFETs on Si

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***Abstract*—The effect of gate-length variation on key transistor metrics for vertical nanowire p-type GaSb metal–oxide–semiconductor field-effect transistors (MOSFETs) are demonstrated using a gate-last process. The new fabrication method enables short gate-lengths (L_g = 40 nm) and allows for selective digital etching of the channel region. Extraction of material properties as well as contact resistance are obtained by systematically varying the gate-length. The fabricated transistors show excellent modulation properties with a maximum $I_{ON}/I_{OFF} = 700$ ($V_{GS} = -0.5$ V) as well as peak transconductance of 50 μS/μm with a linear subthreshold swing of 224 mV/dec.**

***Index Terms*—III–V, GaSb, metal–oxide–semiconductor field-effect transistor (MOSFET), nanowire, scaling, vertical.**

I. Introduction

METAL–OXIDE–SEMICONDUCTOR field-effect transistors (MOSFETs) based on III–V channel materials integrated on Si have proven to be viable technology booster for n-type digital and radio frequency (RF) devices [1]–[3]. Antimonide (Sb) compounds, such as GaSb and InGaSb, are promising alternatives for III–V p-channel MOSFETs, due to high bulk hole mobility [4]. The material is also an essential part of InAs/InGaAsSb tunnel-FETs [5]. However, certain process modules, like gate-stacks and ohmic contacts, for the GaSb MOSFETs are not as optimized as for corresponding n-type MOSFETs, which limits the transistor performance [6]–[8]. Strong p-type MOSFETs based on III–V material is essential for future logic implementation and their integration with state-of-the-art n-type RF transistors. Combinations of more conventional p-type SiGe channel devices integrated with n-type III–V InGaAs-based devices has been proposed [9], [10]. However, material selectivity during processing may limit this type of material integration, which motivates further studies and development of III–V-based p-type transistors.

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TABLE I
BENCHMARKING

	This work	[6] finFET	[1] Sb-sheet	[17] Sb-OI	[18] Sb-OI
L_g [nm]	60	20	500	*	*
Crit.dim.[nm]	24	10	20	7	20
I_{on}/I_{off}	700	50	3000	100	10
$g_{m,max}$ [μS/μm]	50	160	-	-	-
SS_{lin} [mV/dec]	224	260	217	156	-
I_{on} [μA/μm]	20	100	12	-	10
$\lvert V_{DS}\rvert$ [V]	0.5	0.5	0.5	1.0	1.0
$\lvert V_{GS}\rvert$ [V]	1.0	0.5	1.5	1.0	4.0

Benchmarking comparable and symmetric GaSb [1], [17], [18] and InGaSb [6] p-type MOSFETs on Si. I_{on}/I_{off} defined as the maximum current modulation for stated bias-conditions. MOSFETs within this work showcases good overall performance with the best I_{on}/I_{off} for sub-100 nm L_g devices.
*Long-channel devices (>500 nm), therefore gate-length not disclosed.

To circumvent issues, such as various short-channel effects (SCEs) due to deteriorated electrostatics, concerning continued transistor scaling alternative geometries are critical [11]. Gate-all-around (GAA) geometry using vertical nanowires is one option with a projected benefit at the 5-nm node [12].

A vertical nanowire geometry also provides decoupled gate length and contact geometry with regard to footprint area [13]. However, vertical geometries require novel lithography methods to substitute conventional fabrication techniques [14].

In this article, we introduce for the first time a gate-last process [15], [16] for vertical GaSb nanowire MOSFETs that enable gate-length variation. The process is compatible with highly sensitive Sb-based materials [6] that enables a systematical study of scaled p-type MOSFETs in a GAA configuration. The process uses a novel method where the nanowires are fully encapsulated in metal that is selective removed from the sidewalls revealing the channel region. Thus, the sensitive GaSb will remain protected during fabrication and only be exposed prior to the final gate-deposition step. The gate length is varied from 140 to 40 nm at a constant 24-nm channel diameter.

Generally, GaSb transistors exhibit weak modulation properties, with maximum current modulation, at $V_{GS} = -0.5$ V, of barely two order of magnitude considering OFF-state current [1], [6], [17], [18]. Here, we provide substantially improved current modulation when compared with state-of-the-art GaSb-based MOSFETs with a maximum ON/OFF-state current ratio $I_{ON}/I_{OFF} = 700$ ($V_{GS} = -0.5$ V). Complete benchmarking of GaSb p-type MOSFETs on Si is summarized in Table I.

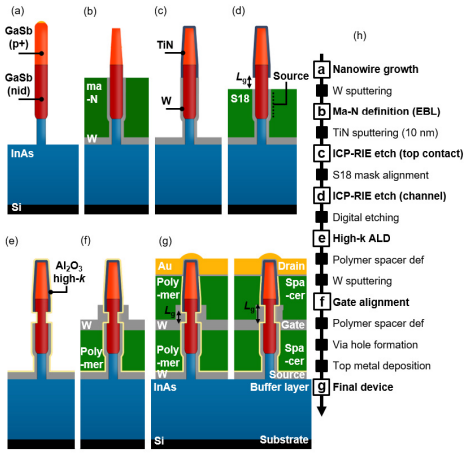

Fig. 1. Schematics for key processing steps realizing gate-length scaling for vertical GaSb p-type MOSFETs. (a) VLS grown heterostructure GaSb nanowire integrated on an InAs buffer layer on Si. (b) Sputtered tungsten encapsulation aligned by ma-N mask with thickness controlled by EBL. (c) TiN sputtered and removed from planar surfaces by anisotropic etching. (d) S18 spacer aligned by plasma etching and channel region exposed by selective dry etching of W. (e) Cycled oxygen exposure and HCL-IPA Dips for recess (digital) etching. (f) S18 polymer spacer aligned by plasma followed by sputtered W with vertical length defined by S18 back-etched mask. (g) Finalized devices after aligning polymer spacer followed by sputtering of drain metal. (h) Itemized overview of the full process-flow.

II. Device Fabrication

Fig. 1 illustrates the critical fabrication steps for the vertical p-type GaSb MOSFETs. The devices are fabricated on 1 cm^2 p-type silicon (111) substrates with a 260-nm-thick epitaxially grown n^{++}-InAs layer [9], [19]. InAs–GaSb nanowires are subsequently grown from 15-nm-thick Au seed particles, with a diameter of 24 nm, defined by Electron Beam Lithography (EBL). The GaSb top segment (∼250 nm) is p-doped by Zn (DEZn/TMGa = 0.36) [see Fig. 1(a)]. For GaSb growth, significant background doping (∼10^{16} cm^{-3}) is present attributed to point defects [20]. Nanowires for each device are ordered in double-row arrays with 300-nm separation, large enough to avoid capillary coalescence during wet processing [21].

In the first process step, following epitaxial growth, the nanowires are etched in an HCL-IPA oxide etch and then encapsulated in 30-nm sputtered tungsten (W) protecting the GaSb surface from subsequent processing steps. An Ma-N polymer layer (spin-on negative resist, ∼500 nm at 2500 r/min) is successively applied to protect the bottom part of the nanowires [9]. Developing the Ma-N with a TMAH-based developer gradually etches both the metal and semiconductor leaving an exposed GaSb tapered, top-segment structure [see Fig. 1(b)]. The thicknesses of the Ma-N is systematically varied from 200 to 350 nm, by varying the dose in EBL, to define the position of the upper edge of the channel region and thus allow for devices with different gate-lengths. In our previous work, hydrogen silsesquioxane (HSQ) has instead been used to enable gate-length scaling for vertical InAs nanowire MOSFETs [13]. Substituting HSQ (fluidic oxide) with Ma-N (organic spacer) leads to a trade-off, sacrificing thermal and mechanical stability in order to gain etch selectivity with respect to Sb-based materials. Subsequent to Ma-N definition, 10 nm of TiN is sputtered and anisotropically dry-etched from planar surfaces by SF_6:N_2 finalizing the top contact [Fig. 1(c)]. TiN-based metals allow for greater anisotropy due to the formation of TiF-based inhibitors on the nanowire sidewalls [22]. The Ma-N mask is stripped by acetone and replaced by an S1813 polymer mask. The polymer mask is thinned in an oxygen plasma to the extent that a segment of the nanowire sidewall, covered with W, protrudes underneath the TiN top contact. An SF6:N2 plasma [inductively coupled plasma (ICP)-reactive ion etcher (RIE)] is used to selectively etch the exposed W, covering the channel region, in between the upper TiN/W layer and the lower S1813 mask [see Fig. 1(d)]. The plasma is generated without any forward RF-bias to enable isotropic etching. W forms volatile etch-products in conjunction with SF6 plasma allowing increased etch selectivity between W and TiN when simulating a remote plasma [22]. This etch process step also defines the bottom contact length [see Fig. 1(d)], where the InAs–GaSb heterojunction is circumvented by a W socket contact. By only introducing Zn doping (*in situ*) at the top of the GaSb segment, excess dopants within the channel region can be avoided [23]. Therefore, the bottom contact relies on the comparably high background doping (∼10^{16} cm^{-3}) present in the GaSb [20].

The S1813 mask is stripped by acetone leaving the finished top and bottom metal contacts. This allows for selective digital etching of the channel by oxidation inside an O_2-chamber followed by an HCL:IPA (1:10) oxide etch. The digital etch cycles are repeated until the nanowire diameter is reduced from 36 down to 24 nm, as confirmed by SEM inspections. Using O_2 environment for oxidizing of the GaSb stabilizes the digital etch rate [6], thus we believe that diameter variation between nanowires originate mainly from variation during epitaxial growth (±2 nm) [24]. A 50 cycle atomic layer deposition (ALD) film of Al_2O_3, deposited at 300 °C, high-k (50 Å, equivalent oxide thickness (EOT) = 1.9 nm) [25] is applied [see Fig. 1(e)] followed by a 100-nm-thick back-etched S1813 resist acting as a bottom spacer. The gate metal is formed by sputtering of 60-nm W followed by a thinned S1813 mask for an SF6 dry-etch process to vertically define the gate overlap rerevealing the top contact [see Fig. 1(f)]. A final polymer spacer is defined followed by a top metal electrode consisting of Ni/Au finishing and capping the device, see schematic in Fig. 1(g).

The results at separate process steps are verified by SEM inspections shown in Fig. 2. Postgrowth inspections show a 500-nm-long heterostructure InAs–GaSb nanowire [see Fig. 2(a)]. After the critical stage of contact formation, recess etching, and high-k (5-nm Al_2O_3) deposition, a 34-nm neck region is exposed that is corresponding to a 24-nm diameter channel-region [see Fig. 2(b)]. Even after aligning the gate

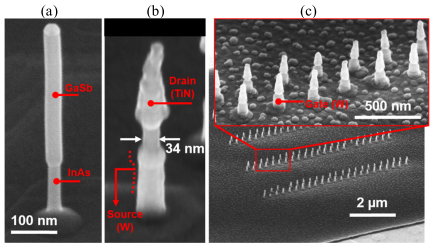

Fig. 2. (a) SEM image of a nanowire implemented in the p-type MOSFET. (b) Device after top and bottom electrode definition. (c) Showcasing a nanowire array contacted by a defined gate-electrode.

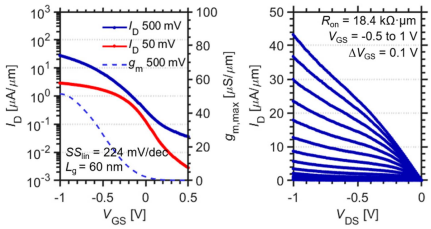

Fig. 3. Transfer and output characteristics for a MOSFET with 60-nm gate-length demonstrating a maximum transconductance of 50 μS/um at $V_{DS} = -0.5$ V.

and rerevealing the top contact, an excellent yield for the full nanowire array is realized [see Fig. 2(c)].

III. Device Characterization

Transfer and output characteristics for a vertical GaSb nanowire MOSFET, with $L_g = 60$ nm, is presented in Fig. 3. A peak transconductance $g_{m,peak}$ value of 50 $\mu S/\mu m$ with minimum subthreshold slope SS_{lin} of 224 mV/dec is achieved. A large current modulation, over several decades, with maximum $I_{ON}/I_{OFF} = 700$ ($V_{GS} = -0.5$ V) is also realized. The device demonstrates well behaved output characteristics, although a large ON-resistance R_{ON} of 18.4 k$\Omega \cdot \mu$m is present.

Fig. 4 presents transfer characteristics and also statistics for key performance metrics with respect to gate-length scaling for 49 devices. Transfer characteristics for transistors with varying gate-lengths is presented in Fig. 4(a). For shorter L_g, the ON-state improves while the OFF-state performance is sacrificed due to degraded electrostatics, considering a fairly large diameter of 24 nm and EOT at 1.9 nm (calculated based on cylindrical oxide capacitance). I_{OFF} (at $V_{DS} = 0.2$ V) and saturation subthreshold swing SS_{sat} (at $V_{DS} = -0.5$ V) vary from 3.8 to 297 nA/μm and 216 to 393 mV/dec, respectively. Statistics with respect to maximum transconductance $g_{m,max}$ versus L_g is presented in Fig. 4(b). A clear correlation between L_g and $g_{m,max}$ is evident where shorter gate-lengths lead to improved ON-state performance. Performance variation can be mainly attributed to varied contact resistance, originating from the reactive nature of GaSb surfaces [26]. Therefore, varied access-resistance is naturally more detrimental to the short gate-length devices ($L_g < 100$ nm) which exhibit greater ON-state performance. Fig. 4(c) demonstrates V_T and SS_{lin} (point slope) behavior with respect to L_g. A clear V_T roll-off is seen at shorter gate-length as well as degraded electrostatics described by SS_{lin} attributed to the unfavorable channel/gate aspect ratio (2:1) at shorter L_g as well as relatively large EOT leading to SCEs [11]. According to scaling theory for cylindrical GAA MOSFET, a five-times larger gate-length is required with respect to field penetration λ_n (calculated to 15 nm) to retain electrostatic control [14], [27], in this case corresponding to a channel/gate aspect ratio of 3:1. Despite SCE, the VT roll-off of 200 mV, for $L_g = 40$–100 nm, is significantly reduced due to the GAA geometry when compared to finFET structures demonstrating a 600-mV shift for fin-widths of 26 nm [6]. Fig. 4(d) presents ON-current I_{ON} and modulation properties I_{ON}/I_{OFF} with respect to L_g for the devices. Smaller L_g grants increased I_{ON} attributed to a decrease in channel-resistance. The L_g scaling is more prevalent for the transistors modulation, demonstrating I_{ON}/I_{OFF} up to four orders of magnitude (I_{ON} and I_{OFF} at -1 and 0.2 V, respectively).

The systematic gate-length variation also enables determination of contact resistance from R_{ON} versus L_g for 18 similar devices [see Fig. 5(a)]. A linear increase in ON-resistance is observed when increasing the gate-length, which enables an extrapolation to 20 k$\Omega \cdot \mu$m of the total contact resistance R_{sd}. Inset shows the g_m versus L_g for the specific p-type devices, increasing for shorter L_g. Transconductance is in fact comparable (within 10%) when reversing the source and drain electrodes indicating symmetrical device with respect to contact resistance, namely providing similar source and drain resistance. By studying the behavior of the output characteristics with respect to L_g [see Fig. 5(b)], a model can be applied in the linear region (see inset). The model is based on drift diffusion considering contact resistances as $I_D = kV_{ov}V_{DS}/(L_g + kV_{ov}R_{sd})$ with overdrive voltage $V_{ov} = V_{GS} - V_T$ and physical parameters contained in $k = W_{eff}\,\mu_h C_{inv}$ with effective gate width W_{eff}, hole mobility μ_h, and inversion capacitance C_{inv}. With $R_{sd} = 20$ k$\Omega \cdot \mu$m and $C_{inv} = 0.5$ aF/nm (calculated considering a coaxial capacitance), the effective hole mobility is determined to $\mu_h = 70$ cm^2/Vs [28]. Earlier work based on vapor–liquid–solid (VLS) grown GaSb nanowires reported a field-effect mobility varying between 50 and 100 cm^2/Vs [20] well in line with our reported values considering that surface effects dominate transport in thin nanowires (<24 nm diameter) [4], [29].

The EOT, at 1.97 nm, of the devices can be considered large in comparison to previous vertical NW MOSFET technology where an EOT below 1 nm have been demonstrated [30]. This implies that a 2x increase in performance can be expected by simply high-k optimization. Further, the large contact resistances ($R_{sd} = 20$ k$\Omega \cdot \mu$m) can be addressed by passivation techniques [4], [31] and heterostructure growth using core–shell structures [6], [32]. The intrinsic channel properties can also be improved by growth and strain engineering [33], [34]. Nonetheless, our novel fabrication techniques

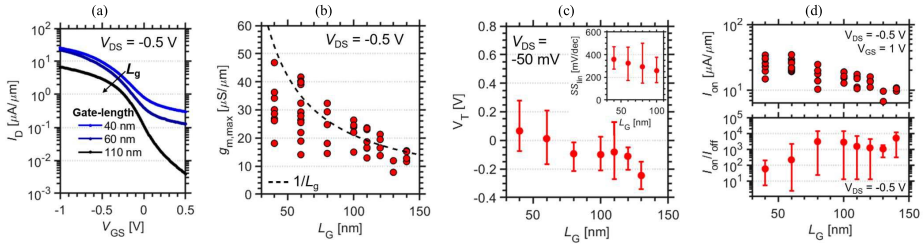

Fig. 4. Statistic for the vertical p-type GaSb MOSFETs based on 42 separate devices. (a) Full transfer characteristics for representative devices at varied L_g. (b) Maximum transconductance versus L_g at $V_{DS} = -0.5$ V, dashed line representing expected trend with respect to drift diffusion ($1/L_g$). (c) Threshold voltage behavior at varying L_g with an inset representing linear subthreshold swing SS_{lin}. (d) I_{ON} for 42 individual devices with respect to L_g and modulation I_{ON}/I_{OFF} at $V_{DS} = -0.5$ V as a function of L_g with I_{ON} defined at $V_{GS} = -1$ V and I_{off} at $V_{GS} = 0.5$ V.

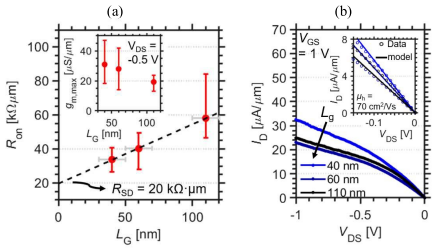

Fig. 5. Statistics and output characteristics for 18 similar devices (same chip location). (a) Extrapolation of contact resistance from R_{ON} versus L_G. (b) Output characteristics for L_g at 40, 60, and 110 nm. Inset shows fitted model for the linear region considering source and drain resistance resulting in a hole-mobility of 70 cm^2/Vs.

pave the way for the next generation of p-type MOSFETs and grant extended design freedom with respect to Sb-based materials.

IV. Conclusion

A new process scheme for vertical p-type (GaSb) MOSFETs has been developed to enable systematic gate-length variation, from 40 up to 140 nm. Fabricated devices demonstrate excellent modulation properties and improved electrostatic control, which are further enforced by a comparably small V_T roll-off. Improved yield enables a significant data set for analysis of both contact and transport properties. Strong modulation properties I_{ON}/I_{OFF} up to four orders of magnitude are also realized. To further elevate performance of the GaSb p-type MOSFET, various passivation techniques and core–shell contacts can be implemented.

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Paper IV

Paper IV

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High-density logic-in-memory devices using vertical indium arsenide nanowires on silicon

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In-memory computing can be used to overcome the von Neumann bottleneck—the need to shuffle data between separate memory and computational units—and help improve computing performance. Co-integrated vertical transistor selectors (1T) and resistive memory elements (1R) in a 1T1R configuration offer advantages of scalability, speed and energy efficiency in current mass storage applications, and such 1T1R cells could also be potentially used for in-memory computation architectures. Here we show that a vertical transistor and resistive memory can be integrated onto a single vertical indium arsenide nanowire on silicon. The approach relies on an interface between the III–V semiconductor nanowire and a high-κ dielectric (hafnium oxide), which provides an oxide layer that can operate either as a vertical transistor selector or a high-performance resistive memory. The resulting 1T1R cells allow Boolean logic operations to be implemented in a single vertical nanowire with a minimal area footprint.

Computers currently have separate memory and computational units. For machine-learning applications, massive volumes of data need to be continuously exchanged back and forth between these units using connections with limited bandwidth and capacity. The performance of such conventional von Neumann architectures is, thus, limited by the rate at which the data is exchanged, a problem commonly known as the memory wall. It is also not area efficient to keep the memory and computational units side by side. In-memory computing—where memory and computational units are co-integrated—has been proposed as a solution to the memory wall, and could save energy and reduce latency[1–4].

Resistive random-access memories (RRAMs) are an ideal candidate for in-memory computation as they consume low power and are scalable, energy efficient and fast. These memory elements integrated in large one-transistor–one-RRAM (1T1R) cross-point arrays are expected to enable both cost- and energy-efficient handling of massive datasets[3]. A memory cross-point array consists of two planes (upper and lower) where intersections have closely spaced wires with the possibility that every intersection can house one memory element. The minimal footprint of such a memory cell is $4F^2$, if half the minimal distance between the centre of two metal lines is taken as the minimum feature size (F). A $4F^2$ architecture can, therefore, achieve the theoretical limit for single bit per cell, the cell area being $2F \times 2F$ (refs. [5,6]).

The International Roadmap for Devices and Systems 2020 (IRDS 2020) has identified the vertical gate-all-around (GAA) metal–oxide–semiconductor field-effect transistor (MOSFET) as a target selector/driver device over the fin field-effect transistor for dense three-dimensional cross-point arrays due to its minimal footprint[7]. IRDS 2020 also highlighted that developing high-density three-dimensional cross-point arrays is challenging due to the lack of highly scaled vertical MOSFET selector/driver devices that offer high-performance memory control. There are only a small number of reports on RRAMs integrated with vertical MOSFET selectors, and these suffer from limited RRAM switching-cycle endurance[8,9]. For integration and operation, it is crucial that the vertical transistor selector and RRAM are compatible with one another. Furthermore, developing vertical transistor selectors and RRAM as isolated elements does not give a direct understanding of the integration challenges or electrical characteristics that a co-integrated 1T1R memory cell might offer.

In this Article, we report the integration of RRAM and vertical MOSFET selectors using a single III–V nanowire. We first create a vertical GAA III–V nanowire–field-effect transistor (FET) selector that has a conventional high-κ/TiN + W gate on a vertical indium arsenide (InAs) nanowire on silicon. We then create a 1T1R cell on the same vertical III–V nanowire by integrating a low-power RRAM stack using an interlayer and high-κ dielectric (hafnium oxide (HfO_2)) oxide layer device above the FET selector. Our approach provides a highly scalable and high-performance 1T1R cell with a minimum footprint of $4F^2$, and the architecture exhibits an RRAM switching endurance of 10^6 cycles.

Vertical transistor selectors integrated with RRAMs

Undesirable short-channel effects in aggressively scaled MOSFETs are a result of diminished electrostatic control. As the transistors are scaled down, the use of double or triple gates (similar to fin field-effect transistors) can improve the gate electrostatic control.

The GAA MOSFET is even better, in which the gate is wrapped around the channel region, leading to strong volume inversion in the channel. GAA MOSFETs with a vertical orientation offer more room for ohmic contacts and spacers, as well as reducing the power consumption by 10–15% in the 7 nm technology node[10]. With increased power saving and better electrostatics, vertical (GAA) MOSFETs are ideal candidates for use in cross-point memory arrays. The vertical geometry allows the cell footprint to remain at a theoretical minimum of $4F^2$ even after RRAM integration.

The first reports of a Si-based vertical GAA MOSFET integrated with an RRAM appeared in 2013 (ref. [8]) and 2014 (ref. [9]). Although encouraging, a maximum RRAM endurance of only 200 cycles was demonstrated. For real-world usability, such as machine-learning applications, a switching endurance of at least 10^5 cycles is needed[11].

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Table 1 | Benchmarking of III–V RRAMs

Stack	Endurance	Retention	Switching window	Geometry	Active area (μm²)
InGaAs-Al_2O_3-Ti (ref. [44])	<40	Not shown	<50	Planar	110,000
InGaAs-InP-HfO_2-Ti (ref. [45])	Not shown	Not shown	7.2	Planar	40
InAs-HfO_2-W (This work)	10^6	10^4 s at 85 °C	>100	VNW	0.01

Also, contemporary RRAM research has considerably evolved, with planar RRAM switching endurance reaching 10^{12} cycles[12].

To provide robust current compliance during oxygen-vacancy-filament FORMING or SET processes needed for high endurance, the GAA MOSFET should preferably operate in the saturation region such that when the oxygen vacancy filament is formed in each cycle, the delivered current is constant, protecting it from variability between the cycles. Moreover, it is beneficial for the MOSFET to operate in its saturation region during the RRAM SET operation to minimize power fluctuations with differences in voltage drop across devices in a cross-point array due to parasitic elements. If current (I) through a device is also dependent on voltage (V), as when the MOSFET operates in its linear region, the power will instead be quadratically dependent ($I \times V$), making it more sensitive to fluctuations throughout the RRAM array[13]. For the vertical Si nanopillar MOSFET selector reported earlier, the current saturation occurs at drain-source voltage (V_{DS}) = 1.5 V with a relatively low channel electron mobility. On the other hand, IRDS 2020 projects that the supply voltage for GAA selector/driver Si MOSFETs will level off at a voltage not less than 0.95 V (refs. [7–9]). However, having a low operational voltage and maintaining a high current density is crucial to enable highly dense, low-power cross-point memory arrays.

Vertical nanowire (VNW) III–V MOSFETs are a promising candidate as selectors for dense cross-point array integration due to their excellent performance. As the programming and erasing speed are crucial for current memory devices, the simulated potential of the III–V vertical MOSFET architecture has been previously examined, where the cutoff frequency (f_t) was estimated to be 1.7 THz at the 12 nm node[14]. Moreover, the radio-frequency properties of a fabricated not fully optimized vertical III–V MOSFET similar to the selector used in this work has been reported, where f_t = 122 GHz and the maximum oscillating frequency f_{max} = 131 GHz (ref. [15]). The advantageous intrinsic properties of III–V materials combined with the knowledge of designing vertical MOSFETs enables the performance required for high-speed RRAM operation in cross-point memory arrays. Furthermore, a VNW III–V MOSFET has been demonstrated with an OFF-state leakage current (I_{OFF}) below 1 nA μm^{-1}, whereas the ON-state current (I_{ON}) saturates at a low supply voltage of only 0.5 V (ref. [16]). A scaled III–V VNW FET with high transconductance (g_m > 3 mS μm^{-1}) and an extremely low ON-state resistance (R_{ON} = 190 Ω μm) at V_{DS} = 0.5 V has also been reported, making III–V vertical MOSFETs a promising selector technology that could be used in dense cross-point RRAM arrays[16–18].

Although III–V MOSFETs have demonstrated higher transconductances and superior drive currents at lower supply voltages than Si MOSFETs, gate oxide traps and oxide/III–V interface traps can considerably degrade the performance of III–V MOSFETs where border traps play a crucial role[19]. An important metric to determine the technology readiness at the device level is the low-frequency noise. It has been previously reported that the border trap density (N_{bt}) in III–V nanowire MOSFETs reaches levels almost comparable to planar Si MOSFETs with HfO_2 gate oxides[19]. Further gate stack optimization to reduce N_{bt} would, nevertheless, be instrumental in improving the variability of III–V MOSFETs. This will also enable wider demonstrated applications such as III–V-MOSFET-based capacitor-less dynamic random-access memories and a platform where III–V MOSFETs are integrated with III–V tunnel field-effect transistors[20,21].

However, to break the von Neumann bottleneck, a technology is needed in which both memory and processor are integrated into a single unit and the need to transfer information between these two units using buses is eliminated. New data-processing schemes based on in-memory computing could achieve this[22], and we envision parallel operation similar to that observed in multicore processors that are increasingly used in parallel computing[23]. We have, thus, explored the vertical integration of a III–V RRAM and a III–V GAA MOSFET on a single nanowire (on a silicon substrate) in an approach that is compatible with silicon CMOS multicore processor technology.

III-V/high-κ-based resistive memory

The III–V/high-κ interface has been extensively investigated and optimized for CMOS devices to reduce the amount of interface oxide using the self-cleaning effect that limits the number of trap states at and in the vicinity of the semiconductor/dielectric interface[24,25]. We have now developed a method that uses plasma oxidation during plasma-enhanced atomic layer deposition (PEALD) to replace the III–V native oxide with a III–V thermal oxide of controlled thickness and composition. The detailed compositional properties of the III–V/high-κ interface that enable high-endurance resistive switching have been obtained from X-ray photoelectron spectroscopy (XPS). With optimized memory performance, we also integrate a (GAA) MOSFET selector on the same VNW and demonstrate NAND functionality for in-memory computing.

The 1T1R configuration for possible future monolithic integration has recently been demonstrated using two-dimensional materials in a planar configuration, showcasing a way to exploit the same material system for the selector and RRAM[26]. So far, resistive switching has been reported at the InGaAs/InP/HfO_2 and InGaAs/Al_2O_3 interfaces, respectively, but with a demonstrated memory endurance of only 30 cycles (Table 1).

III-V VNW as both RRAM and selector

To address the shortcomings in vertical selector integration with RRAM and to simplify the integration scheme, we have developed a process to fabricate an all-III–V 1T1R cell. Figure 1a shows an illustration of a dense cross-point array made using the all-III–V 1T1R cell. The same figure also shows a cross-sectional scanning electron microscopy (SEM) image of the fabricated memory cell. Figure 1b shows the corresponding cross-sectional schematic of the all-III–V 1T1R cell illustrating the two different III–V/high-κ interfaces integrated on the same VNW.

Importantly, we have observed that by varying the pulse length of plasma oxidation during PEALD, one can control the transformation of the III–V/high-κ interface to be suitable for high-performance resistive switching. The VNW MOSFET was fabricated using the gate-last process for VNW MOSFETs[27]. The exact fabrication details are listed in Methods.

Selector functionality was measured by first setting the RRAM to its low resistive state (LRS), after which the applied voltage is

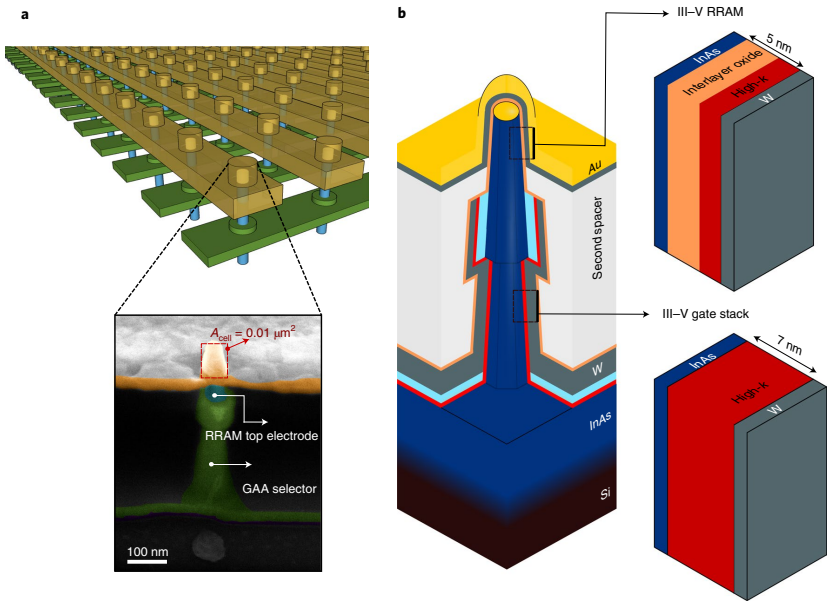

Fig. 1 | Vertical III–V 1T1R structure. a, Cross-sectional SEM image of an all-III–V 1T1R cell with cell area (A_{cell}) = 0.01μm² placed in an illustrative, dense cross-point array. **b**, Cross-sectional schematic of the all-III–V 1T1R cell showing the III–V/high-κ interface used as an RRAM element as well as in the gate stack.

divided between the RRAM LRS and the selector channel. Figure 2a shows the output and transfer characteristics of the III–V-integrated VNW MOSFET selector with good electrostatic gate control over the channel. As III–V MOSFETs have not reached the same technological maturity as Si MOSFETs yet, the current saturation in this work could be further improved by scaling the nanowire diameter and introducing Ga in the drain region. Due to the large nanowire diameter of 55 nm used in this work, the volume inversion may not be fully reached with non-optimal electrostatics for efficient volume inversion. Notably, the current saturation at V_{DS} = 0.5 V in VNW III–V MOSFETs has been experimentally demonstrated to improve with a reduction in the nanowire diameter[28–30].

The *I*–*V* d.c. switching characteristics for five cycles for the InAs/HfO_2/W RRAM are shown in Fig. 2b. With a SET voltage of less than 250 mV, a RESET voltage of less than 1 V and a switching window of ~10^4, the InAs/HfO_2/W RRAM shows excellent d.c. performance. The stack-forming voltage is measured to be ~3.0 V. The retention for the same stack was also measured where the LRS and high resistive state (HRS) were measured for 10^4 s at an elevated temperature of 85 °C (Fig. 2c), demonstrating the non-volatile stability of the RRAM oxide and interfaces. Figure 2d shows the pulsed endurance measurement of the vertical III–V 1T1R cell, where 10^6 switching cycles were measured. The performance of the integrated MOSFET selector does not degrade after RRAM forming and pulsed cycling (Supplementary Fig. 5).

A conventional indium tin oxide/HfO_2/TiN RRAM stack with a cell area of 7 μm² was scaled down to 0.06 μm² (refs. [31,32]). Supplementary Table 1 lists the impact of area scaling of an RRAM cell. The scaling has no negative impact on the switching performance or energy consumption. A previous study has shown that a substantial increase in RRAM switching voltages is observed only when scaled beyond a cell size of 10 nm² (ref. [33]).

All-III–V VNW 1T1R NAND-gate implementation

Two-terminal resistive switching elements have been demonstrated to not only store data but also perform logical operations[34]. The vertical III–V 1T1R structure is highly beneficial for high-density storage, but we also show that the same can be used for computation and not just storage. An important step in this direction is to demonstrate the so-called 'universal gate', the NAND gate, which when used in a combinational circuit, any logic operation can be performed. The universal NAND gate has been shown in other studies to demonstrate logic capabilities[35–37].

In-memory computation using a resistive element (Fig. 3a) would not only address the von Neumann bottleneck by drastically reducing the latency by 10,000 times and lowering the energy consumption by 200 times but the computation scheme also substantially reduces the area footprint by 51 times (Supplementary Fig. 4). For comparison, a conventional CMOS NAND gate comprises a multiple transistor network (Fig. 3b), and the output is stored in a separate memory element connected by metal lines adding undesirable parasitic losses. It is also well known that scaling interconnect metal lines increases the associated latency[38].

The integrated vertical transistor in the 1T1R configuration enables the possibility to fabricate large cross-point arrays by blocking sneak-path currents and cross-talk between two adjacent cells.

Boolean logic can be implemented in a 1T1R configuration based on a two-step (initialization and programming) scheme followed by one READ operation[35]. In the initial implementation, however, the logic was carried out using a 1T1R configuration where the

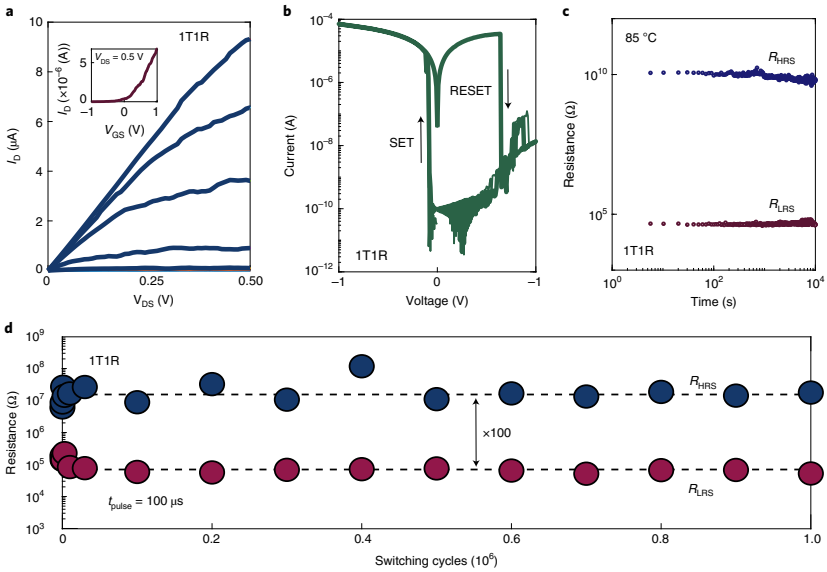

Fig. 2 | Electrical performance of vertical III–V 1T1R. a, Output and transfer characteristics of the integrated III–V VNW MOSFET selector. **b**, *I*–*V* characteristics of the integrated VNW III–V RRAM. **c**, Retention measurement of the low-resistive-state (R_{LRS}) and high-resistive-state (R_{HRS}) measured at 85 °C. **d**, Pulsed endurance measurement of the integrated III–V RRAM with t_{pulse} = 100 μs.

integrated transistor was a conventional planar Si MOSFET. Although the scheme seems to be compact, a major drawback is the cell area consumed by the planar MOSFET. Here we demonstrate that $4F^2$ NAND Boolean logic can be realized with a VNW MOSFET as the selector device. Moreover, the choice of a III–V channel material for the 1T1R cell provides low-voltage operation as well as yielding high current capability for stable RRAM performance. The two-step operation of the NAND gate is described in the following sections.

During the first initialization step, the III–V RRAM is SET to its LRS (~30 kΩ). Second, programming pulses A and B are sent to the two inputs for each NAND gate. The two inputs for the all-III–V VNW NAND gate are the RRAM top electrode (A) and the integrated VNW MOSFET gate (B), whereas source terminal T2 is grounded (Fig. 3a). Third, the resistive state of the NAND gate is read out with a READ pulse. The logic operation result is also stored in situ in the III–V RRAM element until the next initialization.

Electrical measurements were performed on the all-III–V VNW NAND gate to verify its functionality (Fig. 3c). A triangular pulse instead of a rectangular pulse on the RRAM top electrode (input A) has been used by increasing the pulse rise time, and the current overshoot caused by parasitic capacitances is minimized[39].

When input AB = 00, there is no bias applied to the RRAM top electrode (V_{WRITE} = 0 V) and the MOSFET gate is biased to be in the OFF state (V_G = −0.4 V); hence, the RRAM remains in its LRS. When input AB = 01, even though the MOSFET gate is biased to be in the ON state (V_G = 1.0 V), with no programming voltage applied on the RRAM (V_{WRITE} = 0 V), the LRS is retained. With input AB = 10, a programming voltage on the RRAM top electrode (V_{WRITE} = 1.5 V) is applied but with V_G = −0.4 V, the MOSFET restricts the current needed for the RRAM to RESET, and therefore, the RRAM still remains in its LRS. Finally, when input AB = 11, the MOSFET gate is biased to be fully open to allow sufficient current (40 μA) required to rupture the filament and RESET the RRAM to its HRS. Notably, only when input AB = 11 (V_{WRITE} = 1.5 V, V_G = 1.0 V), the RRAM will invert its resistance state from LRS to HRS, functioning as an effective NAND gate. The logic can be performed again by initializing the RRAM back to its LRS. This dataset demonstrates the feasibility of using an individual nanowire as a NAND gate for in-memory computation. Moreover, cycle-to-cycle and device-to-device uniformity of the vertical III–V 1T1R cell (Fig. 3d–f) as well as an endurance of 10^6 cycles of the 1T1R cell shows the practicality of the demonstrated process to perform and store stable logic operations.

To better understand the potential of the demonstrated technology for very-large-scale integration, modelling and simulations were performed using the integrated III–V RRAM characteristics along with the metrics of demonstrated III–V VNW MOSFETs and F = 16 nm (Supplementary Fig. 2)[7,28]. By estimating the worst-case write voltage and read current, the maximum sub-array size was determined to be 10 Mbit, allowing for area-efficient very-large-scale integration with a bit density of 0.98 Gbit mm^{-2} (omitting the peripheral circuitry). The simulations show that Gbit NAND-gate arrays can be densely integrated using an all-III–V VNW 1T1R configuration. The cell size of an individual vertical NAND gate would only be $4F^2$ in contrast to a cell size of ~$200F^2$ when a conventional MOSFET network is used as a two-input NAND gate (Fig. 3). Moreover, the RRAM, being non-volatile, will reduce the static/standby power dissipation that is the main component in scaled technologies today. Implementing all-III–V VNWs for both transistor selector and resistive memory will enable the scaling of both area and supply voltage for in-memory computing.

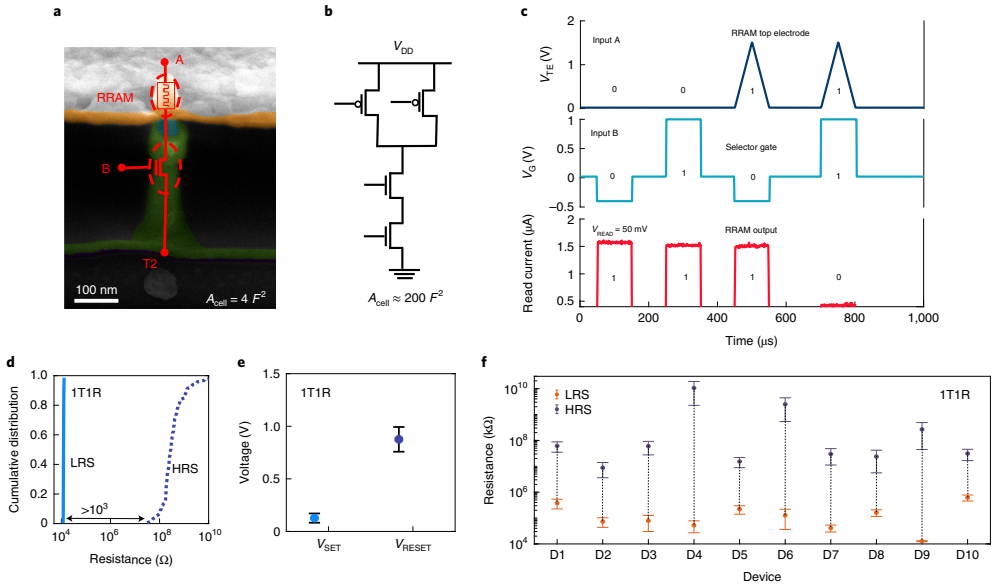

Fig. 3 | Vertical III–V 1T1R NAND-gate implementation and device variability. a, Cross-sectional SEM image of the all-III–V 1T1R cell schematically illustrating a two-input NAND gate, where input A is the top electrode of the RRAM and input B is the selector gate. **b**, Schematic of a conventional two-input NAND gate with a drain-supply-voltage, V_{DD}. **c**, Input conditions AB = 00, 01, 10 and 11 were applied and the resistance state of the integrated RRAM was measured using V_{READ} = 50 mV with a pulse length of 100 μs. **d**, Cumulative distribution of resistance states (LRS and HRS) for cycle-to-cycle variation in the integrated RRAM for 100 switching cycles. **e**, Switching voltage distribution (V_{SET} and V_{RESET}) for the same integrated RRAM where the plotted point is the mean of the first 100 switching cycles and the error bars indicate the standard deviation. **f**, Device-to-device variability of the resistive states for ten different devices on the same sample where the plotted point represents the mean of 10 switching cycles and the error bars indicate the standard deviation.

III–V/high-κ interface oxide control

The key to a successful 1T1R integration is tailoring the atomic layer deposition (ALD) process to meet the distinct performance demands of the gate stack and RRAM element (that is, the ability to modify functionality via processing conditions). Unlike III–V MOSFETs where it is highly important to eliminate interface oxides, we find that critical RRAM switching properties are actually enhanced by oxidizing the III–V/high-κ interface. Oxygen-plasma-enhanced ALD forms a thin, interfacial III–V oxide resistive layer during HfO_2 growth. The result is a dual oxide layer configuration (III–V interface oxide resistive layer and HfO_2 switching layer).

Although the current RRAM stack is demonstrated with ALD-deposited HfO_2, the 1T1R structure would also be operationally compatible with other ALD oxides. The III–V/high-κ-based 1T1R can accommodate the switching voltages and switching currents demonstrated using other commonly used ALD oxides (Supplementary Table 2). The III–V/high-κ-based 1T1R system opens up the possibility of integrating these RRAMs in dense cross-point arrays as well as utilizing the benefits of a vertical III–V MOSFET selector.

The system necessary for stable III–V operation is shown in Fig. 4a. To demonstrate that the interfacial oxide attained during the PEALD of HfO_2 is controlled by the pulse length of oxygen plasma (t_{plasma}), dedicated planar samples with increasing exposure to t_{plasma} were fabricated.

Since oxidation is initiated from the interface, t_{plasma} was adjusted (10, 30 and 80 s) only during the first ten ALD cycles; the remaining 28 cycles were fixed at 80 s for a total of 2 nm HfO_2. Therefore, we study the effect of t_{plasma} only at the III–V/high-κ interface rather than changes in the bulk.

Interlayer oxide thickness and detailed compositional changes were extracted from the photoelectron spectra. Synchrotron-based XPS was performed at the FlexPES beamline of MAX IV in Lund, Sweden, where the soft X-ray excitation allowed for the near-surface depth-dependent characterization of the O1*s*, In3*d*, C1*s*, As3*d* and Hf4*f* core levels. Spectral deconvolution and quantification enabled the thorough modelling of the interlayer (Supplementary Fig. 3).

Increasing t_{plasma} produced two key changes that are highlighted in Fig. 4c. First, 80 s of oxygen plasma was sufficient to double (15 → 30 Å) the thickness of the III–V/high-κ interfacial oxide, despite the HfO_2 overlayer. This is understood as diffusive thermal reoxidation, since the metal–organic precursors of ALD (for example, tetrakisdimethylamido (TDMA)-Hf) are known to remove III–V native oxides[24,40]. Secondly, we observe that the oxidation is not uniform. Indeed, the initially inhomogeneous In_2O_3-rich interlayer concomitant with short plasma exposure gives way to a more stoichiometric interlayer as t_{plasma} is increased. Consistent with previous studies and reported Gibbs energies of formation[41], this suggests a preferential oxidation process, where $In_2O_3 > As_2O_3$. Within the interlayer, a more subtle gradient manifests itself (Supplementary

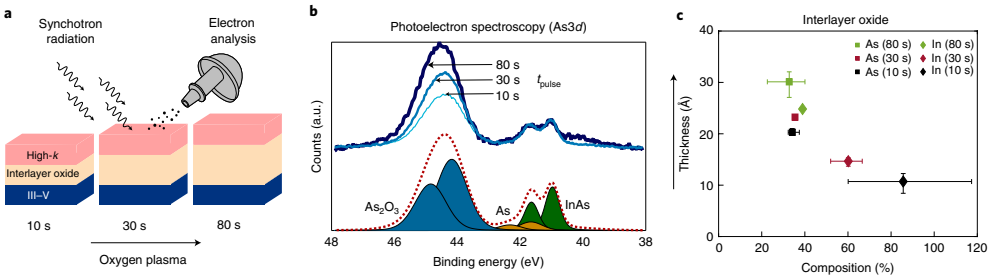

Fig. 4 | XPS characterization of the interlayer oxide. a, Schematic of planar RRAM structures which, on the PEALD of HfO_2 (pink colour), feature a plasma-dependent interlayer oxide growth (tan colour) on the III-V substrate (blue colour). **b**, As3*d* photoelectron spectra depicting the increase in arsenic oxide concomitant with t_{plasma} (top) and example deconvolution (bottom). **c**, Thickness and compositional changes in the III-V/high-κ interlayer expressed as a percentage of volume; arsenic and indium oxides are represented as squares and diamonds, respectively. The plotted point represents the data obtained using the shallow and deep spectra and the error bars represent the range of measured data.

Table 3). Reducing t_{plasma} resulted in inhomogeneity, with a more As_2O_3- and As_0-rich region nearest to the HfO_2 interface, whereas a balanced oxide interlayer was obtained via increased plasma exposure. From a device perspective, this thicker, stoichiometric oxide serves three roles: to aid the one-time FORMING process by preventing a hard breakdown; to act as a resistive layer between the III–V material and HfO_2, which helps assert current compliance needed for stable and high-endurance switching; and to act as an oxygen reservoir that enhances the resistive switching properties[42]. The one-time FORMING current–voltage (I–V) characteristics for five different vertical III–V 1T1R cells are shown in Supplementary Fig. 6. In previous reports, a resistive layer (TaO_x) used in planar RRAMs resulted in high switching endurance values of up to 10^{12} switching cycles[12].

In our investigations, before the actual all-III–V 1T1R integration, III–V RRAMs without an integrated III–V selector were fabricated on single VNWs to better understand the role of interlayer oxide in RRAM switching properties (Supplementary Fig. 7). Three different samples on InAs and InGaAs nanowires were fabricated, where the pulse length of oxygen plasma was varied (10, 30 and 80 s). It was found that the RRAM performance was enhanced for t_{plasma} = 80 s, which resulted in an increased interlayer thickness. For planar InAs samples, the thickness of the interlayer increases from 15 to 30 Å as t_{plasma} increases from 10 to 80 s. The qualitative trend of interlayer growth is expected to be the same on the nanowires[43]. Supplementary Fig. 7a shows that the RRAM performance has a degraded memory window when t_{plasma} = 10 s. The memory window improves with a larger interlayer thickness at t_{plasma} = 80 s. There is also a reduced spread in switching voltages (V_{SET} and V_{RESET}) required for high-endurance switching when t_{plasma} is increased from 30 s ($V_{SET} = 0.74 \pm 0.52$ V, $V_{RESET} = -1.00 \pm 0.33$ V) to 80 s ($V_{SET} = 0.90 \pm 0.27$ V, $V_{RESET} = -1.30 \pm 0.14$ V). We demonstrate that the III–V/high-κ material system using InAs or InGaAs can be used as both MOSFET and high-performance RRAM by carefully controlling the interface oxide layer. The use of the same material system for the vertical selector and integrated RRAM reduces process complexity and—more importantly—maintains operational compatibility.

Conclusions

The integration of selector and memory onto a single VNW capable of performing Boolean operations will enable dense cross-point arrays for in-memory computation in the future. Our work is a step towards implementing the 1T1R configuration with a footprint of $4F^2$ using the all-III–V technology on silicon, and could help reignite efforts to develop vertical MOSFET selectors for RRAMs, as projected by IRDS 2020.

Methods

All-III–V 1T1R cell fabrication. The process flow showcasing the major process steps is shown in Supplementary Fig. 1. The InAs nanowires were grown using metal–organic vapour-phase epitaxy. First, a 300-nm-thick InAs buffer layer was grown on a p-type Si(111) substrate. To facilitate vapour–liquid–solid growth of VNWs, Au seed particles were patterned using electron-beam lithography[25]. The grown VNW acts as the top electrode of the RRAM as well as the active channel material for the selector MOSFET. To selectively etch out the doped shell around the channel segment, SiO_2 using ALD is deposited to cap the top segment of the nanowire. This was done by thinning down the organic S1813 resist to mask the nanowire foot and channel segment. The horizontal SiO_2 layer is then anisotropically etched away by reactive-ion etching using $SF_6 + N_2$ chemistry so that it remains only on the nanowire sidewalls. The highly doped shell is etched away using a digital etch process[16]. The 7-nm-thick gate dielectric (Al_2O_3/HfO_2 bilayer) was then deposited using thermal ALD. The gate metal consisting of 2-nm-thick TiN and 60-nm-thick W was then deposited using ALD and sputtering. The gate length was finally defined by resist thinning and reactive-ion etching of the gate metal, which resulted in a gate length (L_G) of 200 nm.

The gate dielectric covering the top segment of the nanowire is selectively etched away to define the active area of the RRAM.

Once the RRAM area is defined, 2.8-nm-thick HfO_2 at 200 °C using a tetrakis-ethylmethylaminohafnium precursor is deposited using PEALD at t_{plasma} = 80 s, which is required to oxidize the InAs/high-κ interface. A resist spacer (S1813) is used to isolate the III–V RRAM from the III–V gate stack. The resist is thinned down using an oxygen plasma till 100 nm of the InAs nanowire is exposed. The electrical bottom contact (W) for the III–V RRAM is deposited using sputtering and patterned using photolithography.

Data availability

The datasets analysed in this study are available from the corresponding authors upon reasonable request.

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Author contributions

M.S.R. fabricated the 1T1R devices. M.S.R. and K.-M.P. performed the electrical characterization of 1T1R devices. K.-M.P. fabricated the planar devices for XPS characterization. A.I. and R.T. performed the XPS characterization and prepared Fig. 4 with the corresponding analysis. K.-M.P. actively contributed to the writing process and performed the array simulations. A.J. helped with the SiO_2 process module and prepared Fig. 1a. M.S.R. conceptualized the idea of the metal electrode-less RRAM integration. M.S.R. and L.-E.W. wrote the manuscript. L.-E.W. initialized and supervised the project. All the authors discussed and revised the final manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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Doping Profiles in Ultrathin Vertical VLS-Grown InAs Nanowire MOSFETs with High Performance

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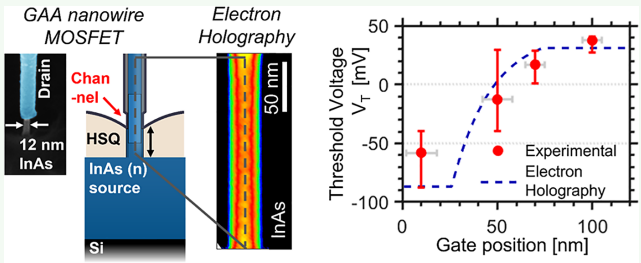

ABSTRACT: Thin vertical nanowires based on III−V compound semiconductors are viable candidates as channel material in metal oxide semiconductor field effect transistors (MOSFETs) due to attractive carrier transport properties. However, for improved performance in terms of current density as well as contact resistance, adequate characterization techniques for resolving doping distribution within thin vertical nanowires are required. We present a novel method of axially probing the doping profile by systematically changing the gate position, at a constant gate length L_g of 50 nm and a channel diameter of 12 nm, along a vertical nanowire MOSFET and utilizing the variations in threshold voltage V_T shift (∼100 mV). The method is further validated using the well-established technique of electron holography to verify the presence of the doping profile. Combined, device and material characterizations allow us to in-depth study the origin of the threshold voltage variability typically present for metal organic chemical vapor deposition (MOCVD)-grown III−V nanowire devices.

KEYWORDS: *III−V, doping, electron holography, MOSFET, nanowire, InAs, VLS growth*

INTRODUCTION

Vertical III−V nanowires (NWs) provide new capabilities in many semiconductor device technologies such as light-emitting diodes,[1] solar cells,[2,3] and improved complementary metal-oxide semiconductor (CMOS) transistor architectures attractive beyond the scaling limit for the conventional Si technology.[4−8] Thin nanowires allow for greater flexibility in material integration due to their smaller footprint, which enables a larger lattice mismatch by radial strain relaxation. The possibility of accommodating larger lattice mismatch is a key benefit for bottom-up integration of nanowires on various substrates as well as for forming heterostructures within the nanowire to an extent not possible in planar technologies.[9,10] However, adequate control of doping levels and gradients within the nanowire is essential for both low contact and access resistances and also for enabling good electrostatics at scaled dimensions. Therefore, new and device-specific characterization methods are critical to support further development of thin vertical III−V nanowire devices.

Vapor−liquid−solid (VLS) epitaxial growth from Au particles enables the formation of high-aspect-ratio nanowires suitable for device implementation. Nanowire doping is typically introduced in situ during nanowire growth, and incorporation can occur both axially through the catalyst particle and radially on the nanowire sidewalls.[11] The amount of axial doping within the nanowires is highly affected by dopant species accumulating in the metal catalyst, typically creating a reservoir effect. Namely, dopants species remain within the gold particle independent of growth chamber conditions. The formation of an abrupt doping profile is therefore challenging, and the optimal conditions will depend

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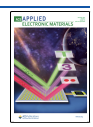

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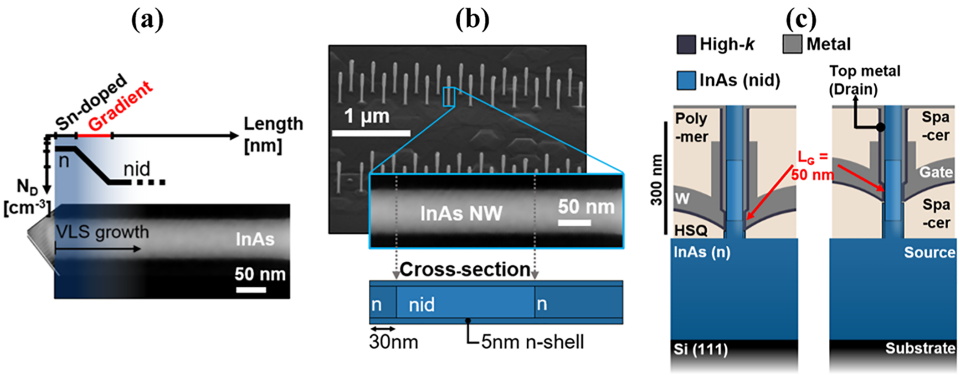

Figure 1. (a) TEM image of the implemented InAs nanowires, highlighting the expected doping gradient induced by in situ Sn doping during metal-seeded VLS growth. (b) Schematic representation of the doping profile as estimated from growth conditions and geometry (Nanowire Growth section) (c) Schematic representation of the finalized vertical nanowire MOSFET with varied gate position retaining a constant L_g of 50 nm.

on dopant solubility in the particle, particle size, and growth rate. However, using VLS enables relatively low temperature during epitaxial growth (<460° for InAs), which serves to suppress diffusion of dopant species already incorporated within the crystal.[12] Particularly, Sn is often used to achieve high n-type carrier concentration in InGaAs, up to 5×10^{19} cm^{-3}. However, Sn is an amphoteric dopant resulting in compensational doping at high concentrations.[13] VLS growth of GeSn nanowires has demonstrated Sn incorporation well in excess of equilibrium solubility in bulk Ge. For InAs nanowires specifically, the Sn doping is typically below the detection limit of energy-dispersive X-ray (EDX) analysis-based methods, indicating incorporation under equilibrium solubility.[14]

Efficient characterization with spatial resolution of the doping within a nanowire remains challenging due to its small geometry. For Au-catalyzed VLS growth, the reservoir effect reportedly leads to a doping grading length on the order of the nanowire diameter.[15] Traditional methods, used for planar films, such as Hall measurements have been applied to large nanowires (diameter >100 nm), but are not applicable to thin nanowires required for transistor applications.[16−18] In addition, capacitance-based measurements have typically been applied to gated nanowires in large nanowire arrays for the evaluation of the doping level, although geometrical limitations such as large surface-to-volume ratio and parasitic capacitances, as well as dynamic carrier interaction at oxide traps present within the gate-stack restrict the measurement accuracy.[19] Approaches that allow sufficient spatial resolution are limited to atom probe tomography and electron holography. Specifically, electron holography offers sensitivity to active doping via the built-in potential they generate, while also maintaining a spatial resolution in the nanoscale range.[20−22] However, these methods require separately prepared samples for characterization of thin nanowires used within devices.

In this paper, we present a novel characterization method used to probe the axial doping distribution in high-performance and scaled (gate length = 50 nm) metal−oxide−semiconductor field-effect transistors (MOSFETs) by varying the gate position along a vertical InAs nanowire and evaluating the resulting threshold voltage (V_T) shift. We apply this method to vertical III−V nanowire-based MOSFETs with thin diameters (12 nm) and state-of-the art performance. Particularly, we systematically study the correlation between the threshold voltage and the varying doping distribution in the axial direction of the incorporated nanowires. The V_T-based characterization method is verified by employing well-established electron holography measurements to independently characterize the axial doping gradient along the nanowire by electrostatic potential. Electron holography thus allows us to evaluate the extent of the reservoir effect prevalent for VLS growth by characterizing the doping distribution gradient; see Figure 1a. The growth results are further characterized by transmission electron microscopy (TEM) imaging, which derives the nanowire crystal structure. The fabricated n-type III−V (InAs channel) transistors exhibit very high transconductance (up to 2.6 mS/μm) and low access resistance (down to 300 Ω μm) attributed to the introduction of a doped segment in the bottom of the nanowire as well as implementing core−shell nanowires (radial shell growth). Furthermore, the doping profile is correlated with actual transistor performance metrics for method validation.[23] Previous studies of V_T shifts in III−V MOSFETs have typically been attributed to quantum size effects for homogeneously doped FinFETs.[24−26] Here, we characterize the axial doping gradient byV_T shift for ultrathin vertical gate-all-around (GAA) nanowire MOSFETs by a novel method enabled by advanced, high-precision, fabrication techniques. Furthermore, this study concludes that the doping gradient within the nanowire provides the main contribution to the V_T shift.

EXPERIMENTAL SECTION

The implemented InAs nanowires are grown from Au dots (32 nm diameter), defined by electron beam lithography (EBL).[5,27] The nanowire VLS growth is performed on a substrate consisting of a 260 nm epitaxially grown n-doped InAs layer on top of a p-type Si(111) substrate. The highly conductive InAs layer facilitates low access resistance and provides an easy path for device isolation by mesa etching of the layer, which are benefits compared to other growth approaches where the nanowires are directly integrated on the Si substrate.[28,29] Sn is used for doping the top and bottom part of the InAs to reduce access resistance, while the intermediate section of the

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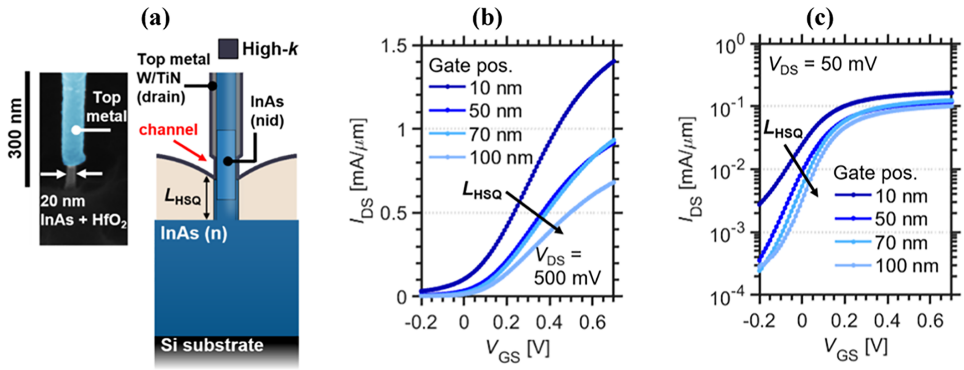

Figure 2. (a) Schematic representation of the nanowire prior to gate deposition, where the thickness of the HSQ spacer defines the position of the gate. (b) Transfer characteristics (linear scale) at V_{DS} = 500 mV representing the on-state for varied gate position L_{HSQ}. (c) Transfer characteristics (log scale) at V_{DS} = 50 mV representing the off-state for varied gate position L_{HSQ}.

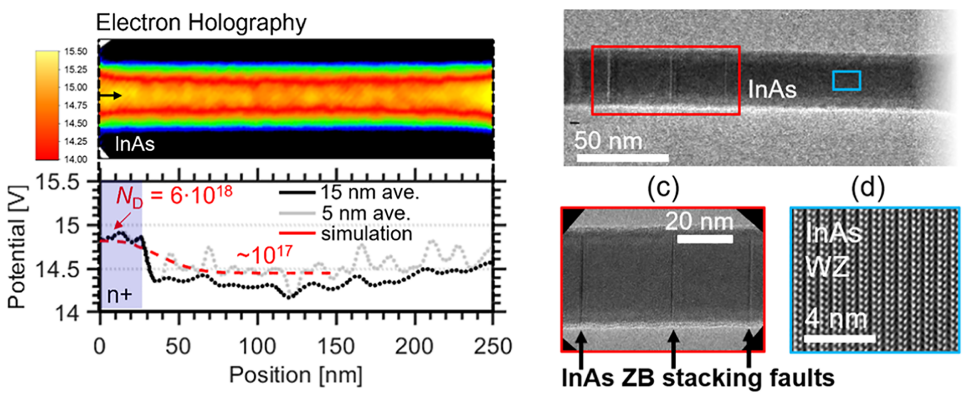

Figure 3. (a) Phase map and axial potential calculated from electron holography data for the InAs nanowire showing the expected initial n^+-region (0 to ~25 nm). Axial potential extracted from the center core (mean value of 15 nm, and 5 nm wide volume) of the nanowire phase map, where oscillations are caused by diameter variation. The simulated potential is calculated using a 1D zero-current model to determine the self-consistent electrostatic potential. The observed potential variation is significantly larger than the measurement error of ±0.092 V. (b) High-resolution TEM image of the heterostructure nanowire showing (c) stacking faults at regions with higher Sn doping incorporation and (d) WZ crystal structure of the InAs segment.

nanowire is not intentionally doped; see Figure 1b. The expected doping profile can be predicted based on geometry and growth conditions, where the gradient from the Sn-doped bottom segment is estimated to be in the order of the gold particle size, in our case about 30 nm (see the Methods section for detailed growth parameters).[15] The nanowires are also radially overgrown with a 5 nm n-doped InAs shell (Figure 1b), which contributes to improved contact resistance for the final devices.[30] Vertical GAA MOSFET devices are formed by following a self-aligned gate last process. This allows selective recess etching of the gate region, which enables nanowire diameters of only 12 nm and further minimizes the drain resistance using a wrap-around drain contact with a gate overlap (detailed description is found in the Device Fabrication section), as illustrated in Figure 1c. We observe that the recess etching leaves a highly doped InAs shell as well as a metal contact adjacent to the source and drain, respectively, which serves to mitigate access resistance further. The fabrication method allows for varied gate positions while retaining a constant gate length of 50 nm. A hexagonal double-row array structure consisting of 184 nanowires is used for each MOSFET, where an internanowire pitch of 300 nm is implemented to minimize proximity effects during VLS growth such as material diffusion.[31] The double-row layout with multiple nanowires provides sufficient absolute current and transconductance for the fabricated devices, which enables high-frequency measurements. The use of multiple nanowires in each device also provides beneficial averaging with respect to process conditions within the array, which serves to suppress unwanted variations of electrical properties for similar devices.[32]

RESULTS

Device schematics and representative transfer characteristics for MOSFETs with varying gate position along the vertical nanowire are presented in Figure 2 (see expanded dataset in the Supporting Information). The selective etching of the

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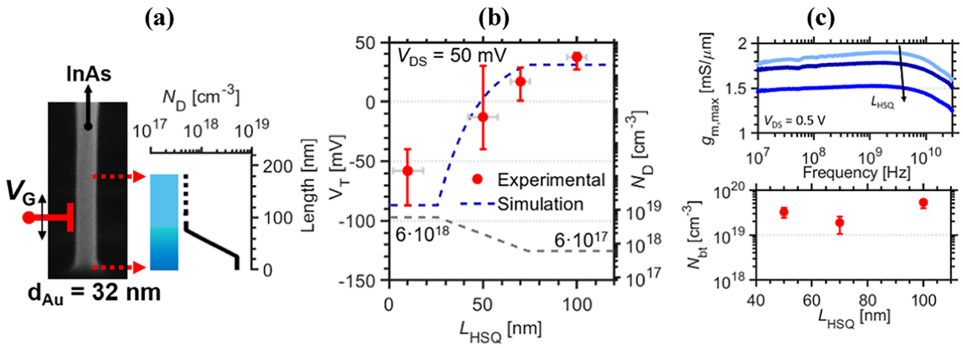

Figure 4. (a) Doping gradient achieved by electron holography varying from 6×10^{18} down to 6×10^{17} cm^{-3} with an exponential decay of 44 nm/decade. (b) Measured threshold voltage V_T dependence of gate position L_{HSQ} and a theoretical model considering the calculated doping gradient from electron holography. V_T is extracted at the linear mode of operation (V_{DS} = 50 mV) to suppress short channel effects. Five devices are measured for each gate position at L_{HSQ} < 90 nm and two devices for L_{HSQ} = 100 nm. The theoretical simulation considers fully doped cylindrical junctionless transistors.[36] (c) Frequency behavior of maximum transconductance $g_{m,max}$ and oxide trap density derived from $g_{m,max}$ vs frequency dispersion for varying gate position. N_{bt} is estimated by considering boarder traps responding within a region of 10^8–10^9 Hz corresponding to an oxide depth of about 0.1–0.3 nm when assuming elastic tunneling.[38]

channel region enables the formation of a thin nanowire channel diameter of 12 nm, which is necessary to suppress short channel effects at short gate lengths (L_g = 50 nm); see Figure 2a.[25] A key process step in our method is that we systematically vary the thickness of the bottom hydrogen silsesquioxane (HSQ) spacer (L_{HSQ}) between the MOSFETs, which translates to a shifted gate position along the nanowires. Therefore, based on the HSQ thickness L_{HSQ}, different parts of the nanowires are covered by the gate and, in effect, this realizes MOSFETs with different doping profiles. Thus, when moving the gate position upwards along the nanowires, the doping within the channel will gradually shift from high doping level (n^+) close to the bottom segment toward nonintentional doping (nid), a change that profoundly influences the transistor metrics. This behavior is evident from the transfer characteristics at V_{DS} = 500 mV (Figure 2b), which exhibit improved drive current when the gate is placed within the highly doped region, thus leaving no ungated resistive regions at the source side.[33] In addition, the transfer characteristics at the lower drain bias, at V_{DS} = 50 mV (Figure 2c), demonstrate a systematic shift from depletion (V_T < 0 V) toward enhancement mode (V_T > 0 V) operation between the devices, as well as improved modulation for elevated gate position. Both effects can be attributed to the variation in the channel carrier concentration. Notably, these devices are processed in parallel on the same sample, removing potential variation due to, for instance, processing and deposition conditions.

By applying electron holography and TEM imaging to a nanowire with the same growth conditions (albeit 44 nm diameter Au dot) the axial doping distribution and crystal structure of the InAs nanowires can be evaluated; see Figure 3. Here, separate samples are prepared where the InAs radial shell is etched after growth to analyze the properties of the core InAs segment (Figure 1b); see the TEM Analysis section. Using electron holography, a phase map is constructed and translated to electrostatic potential (details in the TEM Analysis section) (Figure 3a).[34] The technique is here used to assess the built-in potentials (V_{BI}) and the active doping in the radial and axial directions of the nanowires. The axial potential is calculated as the mean value of 5 nm wide and 15 nm wide volumes, respectively, along the center of the nanowire phase map, to further validate the elevated potential (0 to ∼25 nm) at the beginning of the InAs nanowire section. Electron holography techniques are also highly diameter-dependent, which contribute to the observed oscillations within the data, where many of the oscillations can be attributed to zincblende stacking faults along the nanowire. Fitting a modeled electrostatic potential, based on a 1D zero-current model (1D Poisson-solver) to the measured potential demonstrates the highest doping concentration N_D from 6×10^{18} cm^{-3} [35] at the bottom of the nanowire down to about 6×10^{17} cm^{-3} in the intrinsic segment. Here, an exponentially decaying gradient corresponding to the nanowire Au dot diameter is assumed, which corresponds to a decay of the doping concentration of 44 nm/decade.[15] High-resolution TEM imaging is also performed on the same type of nanowire, visualizing the wurtzite crystal structure with zincblende stacking faults. As expected, the zincblende stacking faults are prevalent for the InAs segment with a higher level of Sn doping incorporation.[9]

Threshold voltage V_T was calculated from the measured transfer characteristics, and frequency-dependent measurements were carried out to verify the negligible influence of gate oxide defects N_{bt} for varying gate position along the vertical nanowire MOSFET. The results are presented in Figure 4, where a schematic image is also provided that represents the axial doping distribution of the nanowire determined via electron holography (Figure 4a). Figure 4b presents V_T versus L_{HSQ}, where V_T is calculated by extrapolating from maximum transconductance at V_{DS} = 50 mV. Here, five devices are measured for each gate position at L_{HSQ} < 90 nm as well as two devices at L_{HSQ} = 100 nm. The V_T shifts by a total of about 100 mV as the gate position is systematically moved from the bottom to the upper part of the nanowire. The threshold voltage can be described (dashed

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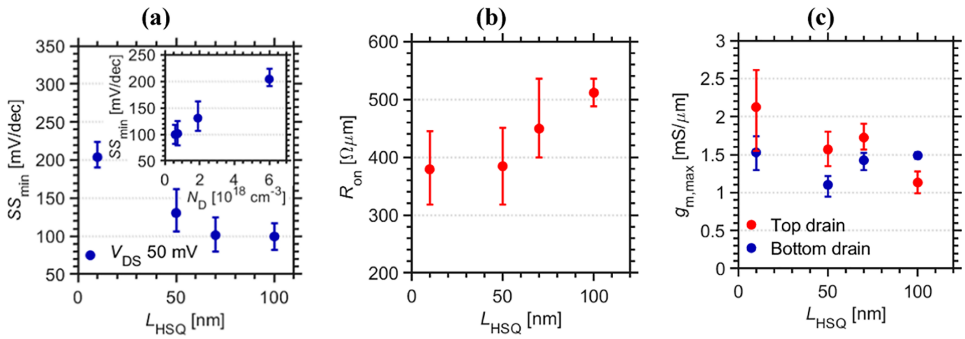

Figure 5. (a) SS_{min} behavior vs gate position L_{HSQ}, with the inset correlating the gate position to expected channel doping N_D according to electron holography (Figure 3a). (b) On-resistance R_{on} vs L_{HSQ}, demonstrating added series resistance with raised gate positions. (c) Maximum transconductance $g_{m,max}$ dependence of gate position indicating degraded performance for larger L_{HSQ}.

line) by an analytical model for doped junctionless GAA nanowires MOSFETs as $V_T = V_{fb} - qN_DK$, where V_{fb} and N_D represent the flatband voltage and channel doping concentration, respectively. Furthermore, $K = r^2(4\varepsilon_r)^{-1}\ln(1 + t_{ox}/r)$ $r^2(64\varepsilon_r)^{-1}$ summarizes different scaling parameters, where t_{ox} is the thickness of the gate oxide, r is the nanowire radius, and ε_s and ε_r represent the relative permittivities of the semiconductor and gate oxide, respectively.[36] This theoretical model is applied by considering the electron holography results, including a difference of an order of magnitude (6×10^{18} to 6×10^{17} cm^{-3}) and a 44 nm/decade decay in doping concentration along the axial direction (Figure 3a). The model describes well the transition in V_T both in magnitude and position as we move along the doping gradient. Variability in V_T between devices at fixed gate position with the same diameter (see Figure 4a) can be mostly attributed to processing variations leading to deteriorated precision in placement of the gate. Particularly, for thinner HSQ spacers, fluctuations in HSQ thickness constitute a larger absolute error of ±10 nm, attributed to the spacer fabrication method using underexposure of an electron beam resist. The HSQ thickness is evaluated by scanning electron microscopy (SEM) of the protruding nanowire during device fabrication; in addition, the thickness variation is determined by measuring the HSQ contrast curve using a profilometer (see the Device Fabrication section for details).[32,37] Within the transitional region of the n^+-/nid-segment, at L_{HSQ} = 50 nm, the spacer variation expectedly manifests as a larger variation due to steep change in V_T (Figure 3b). Notably, a doping concentration of 1×10^{17} cm^{-3} corresponds to only a few active Sn impurities within the channel region; thus, a variation in the Sn doping concentration due to the Au particle size and InAs nanowire diameter will have a large relative effect. Finally, we evaluate the charge density within the dielectric layer of the MOSFET gate-stack, corresponding to border traps N_{bt}, by measuring the frequency dependence of maximum transconductance $g_{m,max}$ in Figure 3c.[38] Measurements are performed for radio frequency (RF)-optimized devices[39] with gate-position L_{HSQ} at 50, 70, and 100 nm. Devices with thinner bottom spacer (L_{HSQ} = 10) nm are dominated by large gate-source overlap capacitance C_{gs} > 150 fF and are therefore unsuitable for RF analysis. The proposed gate-last fabrication method introduces direct gate-drain metal overlap, leading to a capacitance contribution of about $C_{gd} \sim 60$ fF (calculated via small-signal modeling), sufficiently low to enable high-frequency measurements. Optimal bias conditions are obtained from DC measurements as V_{DS} = 0.5 V and V_{GS} corresponding to $g_{m,max}$ ($V_{GS} - V_T \approx$ 0.25 V). For the MOSFETs with the lowest access resistance, i.e., the devices with the shortest HSQ thickness, we observe a very high transconductance reaching values close to 2 mS/μm, which is a competitive value considering the thin nanowire geometry. In agreement with planar III−V MOSFETs, the devices demonstrate the expected behavior of gradually increasing $g_{m,max}$ with higher frequencies, up until parasitic capacitances (in conjunction with extrinsic resistance) dominate (>3 GHz). From these measurements, N_{bt} is calculated from the slope in the frequency range of 10^8−10^9 Hz, which yields similar border trap densities for all devices ($\sim 10^{19}$ cm^{-3}) independent of gate positions (see the Supporting Information for details). The results indicate that the oxide defects are not the main influence of the V_T shifts.

Finally, we evaluate the influence of the obtained doping profile (Figure 4a,b) of the InAs nanowire segment on relevant MOSFET performance metrics, such as minimum subthreshold swing SS_{min}, on-resistance R_{on}, and $g_{m,max}$, with respect to gate position L_{HSQ} in Figure 5. Figure 5a provides off-state characteristics, quantified by SS_{min} (point slope) with respect to L_{HSQ}, where increased channel doping leads to deteriorated off-state performance (figure inset). Improved SS_{min} for lower background doping is well in line with previously reported results for GAA InAs MOSFET devices.[40] When moving the gate position up along the nanowire, the length of the epitaxial contact at the nanowire source (bottom) extends, resulting in an increased on-resistance R_{on}; see Figure 5b.[35] R_{on} represents the combined resistance contribution of the transistor, namely, the sum of source and drain resistance (access resistance) as well as channel resistance. The maximum transconductance $g_{m,max}$ of the devices shows state-of-the-art performance, with the best values exceeding 2.5 mS/μm, although they reduce with respect to raised gate position (Figure 5c). The DC performance of these 12 nm channel diameter devices, with L_g = 50 nm, compare well with previously reported vertical GAA MOSFETs, that demonstrated $g_{m,max}$ > 3 mS/μm and R_{on} = 190 Ω·μm for devices scaled to L_g = 25 nm (17 nm channel

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diameter), albeit these devices provided less favorable off-state characteristics with reported SS_{min} = 440 mV/dec.[41] The $g_{m,max}$ vs R_{on} trends (Figure 5b) confirm the presence of an added ungated resistive regions at the source side for increased spacer thickness L_{HSQ}.[33] The added access resistance, at the source, also serves to reduce the effective voltage drop between the gate and source. This effect is predominantly observed at L_{HSQ} = 100 nm, as evidenced by increased transconductance values when switching the biasing of source and drain electrodes from bottom ground to top ground (Figure 5c). The presence of the axial doping distribution of the InAs nanowire core segment is therefore further validated by the trends measured for SS_{min}, R_{on}, and $g_{m,max}$ vs gate position L_{HSQ}.

CONCLUSIONS

In conclusion, we have characterized the doping incorporation of Sn in ultrathin (12 nm channel diameter) vertical VLS-grown nanowires utilizing a novel method of axial threshold voltage probing validated by the well-established technique of high-resolution electron holography. The V_T probing method is performed by systematically moving the gate position along a vertical nanowire MOSFET and utilizing the measured shift in the threshold voltage to model and evaluate the encapsulated charge due to doping. By also measuring the transconductance−frequency dispersion, we further ruled out gate oxide defects as the main contribution for threshold voltage shift. The MOSFETs used in this study exhibited excellent performance, with highest maximum transconductance of 2.6 mS/μm. The obtained results are further substantiated by other transistor metrics, such as SS_{min}, R_{on}, and $g_{m,max}$, which all scale according to gate position. This study also provided insights regarding the V_T variation typically found in III−V MOSFETs based on metal organic chemical vapor deposition (MOCVD)-grown materials, which has proven to be detrimental for further circuit implementation such as for CMOS applications. To address these issues related to in situ doping, the axial gradients could be mitigated by selective area epitaxy[42] and further circumvented by employing regrown contacts.[43] On a closing note, our proposed, V_T-based, sweeping gate method allows characterization with sufficient resolution to discern various doping gradients present within thin nanowire channels employed in MOSFETs. The presented method, which requires no separately prepared samples, is therefore a welcome addition in the ever-growing library of application-specific devices employing advanced channel engineering.

METHODS

Nanowire Growth. Arrays of Au disks with a thickness of 10 nm and diameters from 20 to 44 nm were patterned by EBL on substrates consisting of 250 nm highly doped InAs layers grown on high resistivity Si(111) substrates. The nanowires were grown using metal−organic vapor-phase epitaxy (MOVPE) in an Aixtron CCS 18313 reactor at a pressure of 100 mbar and a total flow of 8000 sccm. After annealing in arsine (AsH_3) at 550 °C, an InAs segment was grown at 460 °C using trimethylindium (TMIn) and arsine with a molar fraction of $X_{TMIn} = 6.1 \times 10^{-6}$ and $X_{AsH_3} = 1.3 \times 10^{-4}$, respectively. The bottom and top parts of the InAs segment were n-doped by tetraethyltin (TESn) ($X_{TESn} = 1.2 \times 10^{-5}$). The growth was paused in an arsine flow for 3 min to reduce the In concentration in the Au particle. A 5 s pulse of TMIn and another 5 s pulse of trimethylantimony (TMSb) were supplied before a GaSb segment was grown using (TMGa) ($X_{TMGa} = 4.9 \times 10^{-5}$) and trimethylantimony (TMSb) ($X_{TMSb} = 6.2 \times 10^{-5}$) while heating to 515 °C. The top half of the GaSb segment was p-doped using diethylzinc (DEZn) ($X_{DEZn} = 1.9 \times 10^{-5}$). The temperature was then lowered to 460 °C at which a Sn-doped InAs shell was grown using the same molar fraction as for the InAs bottom segment.

Electrical Measurements. DC measurements are realized with Cascade 1100B probe station connected to a Keithley 4200A-SCS parameter, where low-frequency RF probes are used to minimize access resistance originating from the probe-pad contact. RF measurements were carried out with an Agilent E8361A vector network analyzer. The measurement was calibrated off-chip with an LRRM method, and the effect of contact pads was deembedded by measuring dedicated on-chip open and short structures. *S*-parameters were measured from 10 MHz to 67 GHz and transformed to *y*-parameters. A small-signal model was fitted to the *y*-parameters, and the frequency dependence of the transconductance $g_{m,max}$, as well as the defect density N_{bt}, was calculated from $\mathrm{Re}(y_{21})$.

TEM Analysis. Postgrowth nanowires are prepared by ozone oxidation followed by a 30 s HCl/H_2O 1:10 dip (one digital etch cycle) to remove homogeneously doped radial shell growth. NWs were broken off from the growth substrate and transferred onto a TEM Cu grid with a carbon membrane. Electron holograms were recorded using an FEI Titan 80-300ST field emission gun transmission electron microscope, operating at 120 kV and equipped with a rotatable Möllenstedt biprism. This TEM technique of electron holography acquires a spatially resolved phase difference, ϕ, by interference between electrons that pass through the specimen (object wave) and vacuum (reference wave). The ϕ value is related to the crystal potential $V(x, y, z)$ according to $\phi = C_E \int_0^t V(x, y, z)\, dz$, where C_E is a constant that depends on the microscope acceleration voltage (8.64×10^{-6} rad/(m V) at 120 kV) and t is the specimen thickness. Holograms with 10 s exposure time were acquired using a 2 × 2-*k* charge-coupled device (CCD) camera (Gatan Ultrascan US1000 CCD) at a biprism voltage of 122 V. They were then processed through a removal of dead and hot pixels by an iterative local threshold algorithm, as well as a masking out of Fresnel fringes. In addition, to increase the signal-to-noise ratio of the holograms, a modest Wiener filtering in Fourier space was employed. Upon the holographic Fourier reconstruction method, one side band was masked with a circular 10th-order Butterworth filter. Finally, the phase of the reconstructed wave was subtracted by the phase reconstructed from an additionally recorded and equally processed object-free empty hologram. The mean counts per hologram pixel were ≈60 000, the phase resolution was ≈0.2 rad, and the error in the potential was ≈0.09 V.

Device Fabrication. The sample was first spin-coated with hydrogen silsesquioxane (HSQ) thin film and patterned via e-beam lithography (EBL), where the local spacer thickness is controlled by the dose of electrons. After development of the HSQ film by a 25% tetramethylammonium hydroxide (TMAH) solution, the sample was dipped in citric acid followed by 20 nm sputtered W and 3 nm atomic layer deposited (ALD) TiN. A C4F8:Ar anisotropic dry etch was performed, which leaves only the metal on the nanowire sidewalls, forming the top contact.

The exposed HSQ was then thinned by diluted HF 1:1000 to form the first spacer, exposing the channel region, forming a recess gate. This allows for selective etching of the gate by digital etching, namely, repeated oxidization with O_3 and etching by citric acid until the highly doped InAs shell is removed. In situ hydrogen-plasma cleaning is performed prior to high-*k* deposition, at 250 degrees, consisting of 40 cycles of HfO_2. The gate was then finalized by sputtering 60 nm of W, which is vertically aligned by a back-etched polymer spacer, by O_2-plasma, followed by an SF6 dry etch for W removal. Postmetal annealing at 250 °C is performed after gate deposition. The MOSFET is then finished by aligning an S1813 top spacer, forming via holes, and sputtering of Ni/W/Au, 15/30/180 nm, as the final top metal.

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■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.1c00729.

MOSFET virtual source modeling, VT dependence of nanowire diameter (quantization considering nonparabolicity), response of boarder traps with respect to oxide depth derived from RF measurements, and expanded dataset of transfer characteristics with respect to gate position (PDF)

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Notes

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Paper VI

Paper VI

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Characterization of GaSb surfaces and nanowires during oxide removal

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ABSTRACT

The high hole-mobility of GaSb makes GaSb nanowires a promising candidate for high-speed p-channels in electronic devices. However, GaSb-based nanostructure devices suffer from a high interface defect density due to a comparably thick native oxide, which has been proven difficult to remove. Using synchrotron X-ray photoelectron spectroscopy, we present here a characterization of the native oxides on the GaSb surface, both for planar substrates and nanowires, during subsequent steps of H-plasma cleaning. The native oxide is found to have a different chemical composition on the nanowires as compared to the planar substrate. Sb-oxides are successfully removed already during initial cleaning, while the amount of Ga_2O increases at the same time. During continuous cleaning, Ga_2O_3 gets removed from the surface, until finally the amount of Ga_2O gets reduced as well. The cleaning procedure is observed to be most effective for the nanowires, where all native oxides get successfully removed except of a small amount of Ga_2O, which has been reported to be less detrimental than Ga in a higher oxidation state. We suggest to implement this H-plasma cleaning step as a pre-treatment in plasma-enhanced atomic layer deposition of high-k oxides on GaSb nanowire devices.

I. INTRODUCTION

Electronic devices based on III-V semiconducting nanowires have stirred a lot of attention during the last decades [1,2]. The much higher electron mobility in III-V materials such as InAs compared to Si promotes superior device performance. Devices such as gate-all-around nanowire metal-oxide-semiconductor capacitors and field effect transistors have been realized for InAs and InGaAs nanowires [3,4,5]. The high hole mobility of GaSb makes this the material of choice for p-channel conductivity [6], which is needed in order to realize complementary metal-oxide-semiconductor (CMOS) geometry. Indeed, fully nanowire-based CMOS transistors have been realized using InAs and GaSb nanowires monolithically integrated on Si [7]. Another highly promising approach towards novel nanowire-based devices consists of InAs-GaSb nanowire tunneling field effect transistors (TFET) [8], which recently have demonstrated steep slope behavior and high current densities for 10 nm thin nanowires [9].

The main challenge with implementing GaSb into devices is its unideal surface with an excess of surface states partly originating from a high density of defects and a continuously growing native oxide that is not self-limiting [10]. The Ga- and Sb-oxides are also more difficult to remove compared to e.g. In- and As-oxides, especially prior or during atomic layer deposition (ALD) of high-*k* oxides, which is the standard processing approach for almost all electrical devices. While ALD of e.g. HfO_2 or Al_2O_3 on InAs has been found to remove almost all native oxide through the so-called self-cleaning effect [11,12], GaSb suffers from only incomplete reduction of native oxides upon high-*k* ALD [13]. Recently, promising attempts to remove these oxides by N_2 and H_2 plasma pre-treatment prior to ALD have been reported, resulting in an improved quality of the GaSb-high-*k* interface [14,15].

X-ray photoelectron spectroscopy (XPS) and especially synchrotron based XPS is ideal for investigating semiconductor-oxide interfaces and surfaces [16,17,18,19]. We have previously used XPS for studying the self-cleaning effect during ALD on InAs substrates [12,20,21] and nanowires [22] and for evaluating surface cleaning of InSb [23]. McDonnell et al. [24] and Zhernokletov et al. [13] investigated the surface of GaSb after subsequent ALD half-cycles of HfO_2 with XPS and observed a reduction of the amount of Sb-oxides while at the same time the amount of Ga-oxides was increased. A similar behavior was also observed during the annealing of GaSb substrates in ultrahigh vacuum (UHV) [10]. However, surface cleaning and oxide removal of GaSb nanowires has, to our knowledge, not been investigated by XPS yet.

Here, we have used synchrotron based XPS to study the chemical composition of GaSb surfaces, both for planar substrates as well as for nanowires, with native oxide and during H-plasma cleaning performed in UHV. We find a complete removal of Sb-oxides and a strong reduction of the amount of Ga-oxides upon cleaning, accompanied with a transition from Ga_2O_3 to Ga_2O. Remarkably, the oxide removal is even more profound for the nanowires, where the native oxide contained an additional Ga-oxide component, as compared to the planar substrate. The oxide removal was reached with a sample temperature during cleaning of only 200 - 250°C, and without any wet chemical treatment. We suggest to implement a similar H plasma treatment prior to high-*k* ALD during the processing of GaSb nanowire based devices.

II. EXPERIMENT

The growth of the nanowires will now be described. Arrays of Au discs, used as seed particles for nanowire growth, with a thickness of 10 nm and diameters from 22 nm to 42 nm were patterned by electron beam lithography on Si(111) substrates with a 250 nm highly doped

InAs layer on top. InAs-GaSb nanowires were grown from the Au seeds using metalorganic vapor phase epitaxy (MOVPE) in an Aixtron CCS 18313 reactor at a pressure of 100 mbar and a total flow of 8000 sccm as follows: After annealing at 550°C in arsine (AsH_3), a short InAs segment was grown at 460°C using trimethylindium (TMIn) and arsine with a molar fraction of X(TMIn) = $6.1 \cdot 10^{-6}$ and X(AsH_3) = $1.25 \cdot 10^{-4}$, respectively. This InAs stem is required since nucleation of GaSb directly on the substrate surface is challenging [16]. The GaSb segment was grown on top of the InAs stem using trimethylgallium (TMGa) and trimethylantimony (TMSb) with molar fractions of X(TMGa) = $4.9 \cdot 10^{-5}$ and X(TMSb) = $8.9 \cdot 10^{-5}$, respectively, while diethylzinc (X(DEZn) = $3.0 \cdot 10^{-7}$) was added for *p*-doping. GaSb growth was initiated at 460°C, thereafter the temperature was increased to 515°C for a growth time of 30 min. This resulted in nanowires with a thickness of 50 nm and a length of around 1.55 µm shown in FIG. 1 (a).

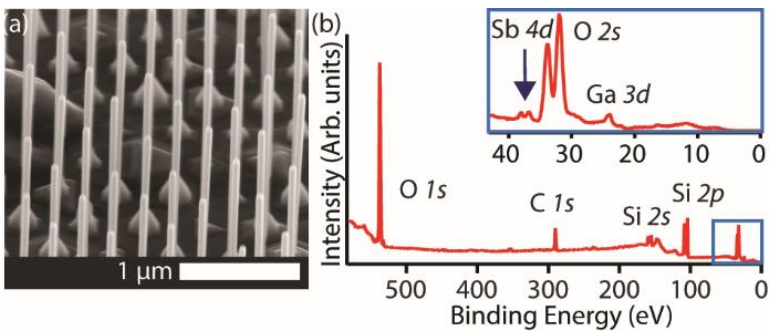

Figure 1 *– (a) SEM image of the nanowire growth sample. (b) Overview of XPS with the inset showing the nanowire footprint, acquired at a photon energy of 650 eV.*

The XPS samples were prepared by mechanically transfering the nanowires from their growth substrate onto a clean Si wafer (rinsed in ethanol). The transfer was done by gently pushing the growth sample against the Si substrate [22], resulting in a nanowire coverage of the Si sample of less than 5%, according to inspection by scanning electron microscopy. Such a

relatively low nanowire coverage is needed to ensure that the distributed nanowires have good electrical contact to the Si substrate and thus to avoid possible charging effects in nanowire piles, but it also results in a relatively weak XPS signal from the nanowires, requiring the superior brightness of a synchrotron source. Figure 1 (b) shows an XPS overview spectrum of the nanowire sample: It is dominated by the O and Si signals and some C contamination from the substrate, but Ga and Sb peaks can be seen as well. Please note that due to the deposition method, the nanowire coverage is varying locally on the sample and also between different samples, and hence no comparison of absolute XPS signals is possible. GaSb films, epitaxially grown on Si(111) substrates with a 250 nm highly doped InAs layer, were used as planar reference samples.

XPS experiments were performed at the high resolution, soft X-ray beamline SUPERESCA at the Elettra synchrotron facility (Trieste, Italy). The samples were cleaned from their native oxide using a hydrogen plasma generated by a Tectra gen 2 plasma source. The H-plasma source was mounted on a preparation chamber separated from the analysis chamber by a valve, allowing cleaning and subsequent XPS measurements without breaking UHV conditions. The sample was cleaned for a total of 20 minutes at a sample temperature of 200°C and a H pressure of about 3×10^{-4} mbar. XPS measurements were taken before any cleaning as well as after 2, 10, and 20 minutes of cleaning.

Core level spectra were recorded for Ga *3d*, Ga *3p*, Sb *3d*, Sb *4d*, As *3d*, In *3d* and Au *4f* using photon energies between 120 eV and 1140 eV. For each core level, spectra of several different photon energies were acquired in order to probe a wide range of surface sensitivity. Spectra of the experimental data were fitted using IGORPro, assuming a Voigt line form and subtracting a linear or polynomic background from each spectrum. In agreement with literature values [ref], the Ga *3d* (Sb *4d*) spectra were fitted as doublets with a spin-orbit

splitting of 0.44 eV (1.25 eV), a branching ratio of 0.67 (0.67), and a Lorentzian full with at half maximum of 0.18 eV (0.22 eV).

III. RESULTS AND DISCUSSION

We start by turning to the Sb *4d* spectra from the GaSb substrate presented in FIG. 2 (a-e). Prior to cleaning (Fig. 2 (b)), the spectrum is dominated by a doublet at a binding energy of 34.4 eV (green), which disappears upon cleaning while another doublet at 32 eV (blue) increases in height. We therefore attribute the doublet at lower binding energy to Sb bound to Ga, and the one at 2.4 eV higher binding energy to Sb-oxides, in agreement with our previous study of InSb [23]. Different oxidation states of Sb have been mentioned in literature, including Sb^{+3} (as in Sb_2O_3), Sb^{+4} (as in Sb_2O_4), and Sb^{+5} (as in Sb_2O_5) [10,25], with Sb_2O_3 being the abundant oxide component. We do however not see evidence for several distinct oxide components in our data, and expect our Sb-oxide to consist of Sb_2O_3. At the chosen photon energy of 340 eV, resulting in a kinetic energy of the Sb *4d* core level electrons of about 300 eV, the electron inelastic mean free path is 1 nm. This and the fact that the Sb-Ga bulk signal is strongly attenuated by the native oxide, as can be seen in Fig. 2 (b), indicates a native oxide thickness of several nm, much thicker than for typical InAs wafers [12].

H-plasma cleaning of the sample was performed during a total of 20 minutes at a sample temperature of 200°C during the first 10 minutes and 250°C thereafter, and XPS spectra were recorded after 2 minutes of cleaning (Fig. 2 (c)), after 10 minutes (Fig. 2 (d)), and finally after 20 minutes (Fig. 2 (e)). The removal of the native oxides is profound already after 2 minutes of cleaning, and no Sb-oxide can be detected anymore after 10 minutes of cleaning.

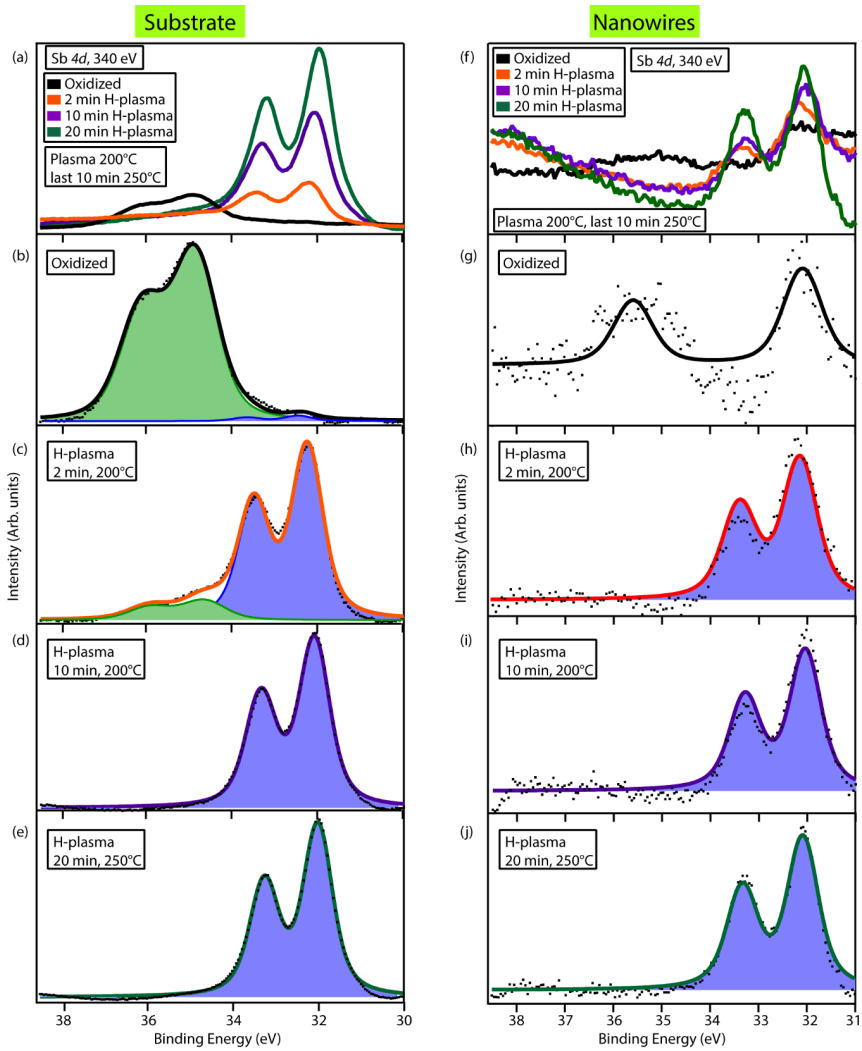

Figure 2 *– XPS spectra of the Sb 4d core level of (a-e) a flat GaSb substrate and (f-j) nanowires, taken at a photon energy of 340 eV. (a,f) Comparison of spectra acquired at different steps of H-plasma cleaning. (b-e and g-j) Individual spectra after subtraction of a polynomic background, fitted with a doublet corresponding to Sb bound to Ga (blue) and a doublet corresponding to Sb-oxide (green), for (b,g) samples with native oxide prior to cleaning, after (c,h) 2 min and (d,i) 10 min of cleaning at 200°C, and (e,j) after additional 10 minutes of cleaning at a sample temperature of 250°C.*

Turning to the Sb *4d* spectra from the GaSb nanowires presented in Fig. 2 (f-j), it is apparent that the nanowire XPS signal is lower as compared to the substrate, due to the low coverage of nanowires. In addition, the background signal is more corrugated, which makes thorough peak-fitting challenging. Still, it is possible to use the parameters obtained from the GaSb substrate and fit also the nanowire data with one doublet for Sb bound to Ga (blue) and one for Sb-oxides (green), even though a quantitative comparison of the different components becomes difficult. Interestingly, the relative amount of native oxide on the nanowire sample prior to cleaning is smaller as compared to the substrate, as can be seen in Fig. 2 (g), where also the Sb-Ga doublet is well resolved due to the lower attenuation of the oxide layer on top. It has to be noted that due to geometric effects the same oxide thickness would for the nanowires lead to stronger attenuation of the underlying signal as compared to the substrate [22], inversely to what we observe, meaning that the actual thickness of the native oxide is significantly smaller on the nanowires than on the substrate. The H-plasma cleaning process is very efficient also for the nanowire sample, where a complete removal of Sb-oxides is observed already after 2 minutes. This result is very promising regarding future native oxide removal from GaSb nanowires prior to device processing, and it could not necessarily be expected, as in the InAs and GaAs material system cleaning of the nanowires takes significantly longer time than cleaning of flat substrates, due to the large surface area and many surface steps of the nanowires [22,26]. We also want to point out that we find no trace of metallic Sb before or after the cleaning, which has been reported to be especially detrimental for device performance [14,27,28].

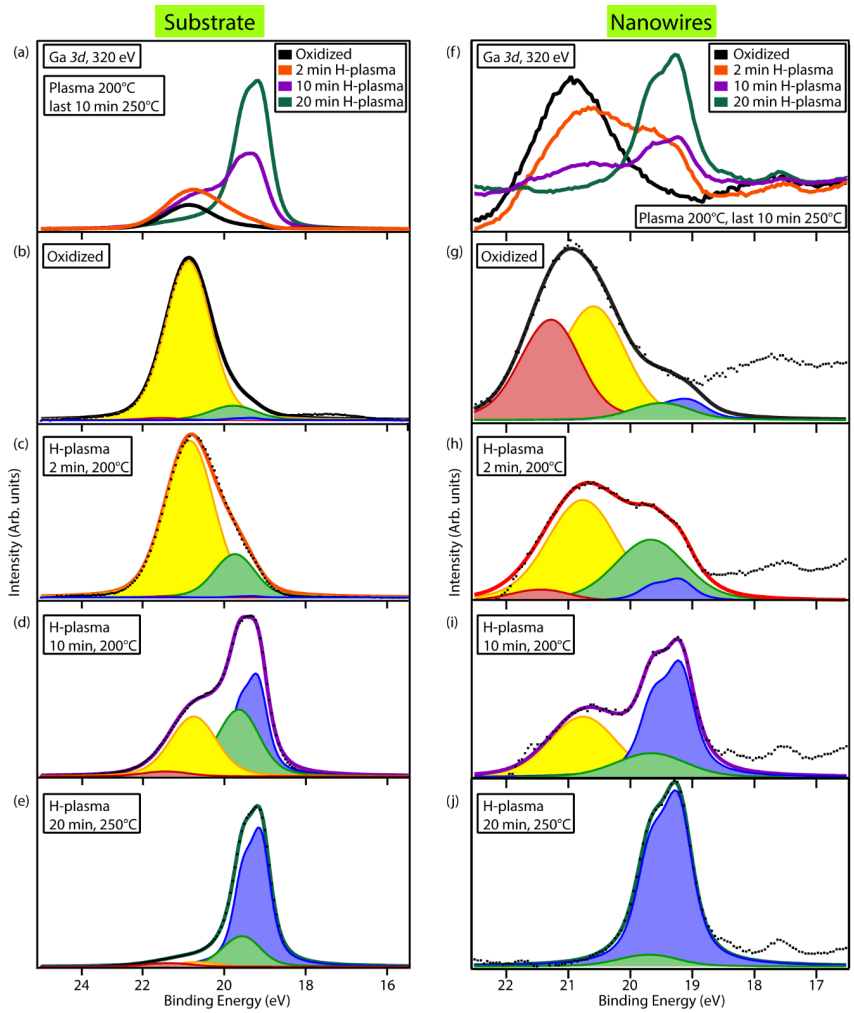

Figure 3 *– XPS spectra of the Ga 3d core level of (a-e) a flat GaSb substrate and (f-j) nanowires, taken at a photon energy of 320 eV. (a,f) Comparison of spectra acquired at different steps of H-plasma cleaning. (b-e and g-j) Individual spectra after subtraction of a linear background, fitted with a doublet corresponding to Ga-Sb (blue) and three doublets corresponding to different Ga-oxides (green, yellow, and red), for (b,g) samples with native oxide prior to cleaning, after (c,h) 2 min and (d,i) 10 min of cleaning at 200°C, and (e,j) after additional 10 minutes of cleaning at a sample temperature of 250°C.*

In Fig. 3 we show Ga *3d* core level spectra from (a-e) the substrate and (f-j) the nanowire sample. These Ga *3d* spectra are taken at the same sample position as the Sb *4d* spectra shown in Fig. 2, and they are acquired with a photon energy of 320 eV, which results in the same kinetic energy of about 300 eV. Four separate doublets are needed in order to fit the Ga *3d* spectra before and after H-plasma cleaning. The bulk peak of Ga bound to Sb is expected to dominate the spectrum at the end of the cleaning procedure, shown in Fig. 3 (e). Therefore, we attribute the doublet with a binding energy of about 19.2 eV to Ga-Sb (blue). All other three doublets are obtained at higher binding energies, with chemical shifts relative to the Ga-Sb peak of +0.31 eV (green), +1.41 eV (yellow) and +2.1 eV (red). According to literature, we attribute the peak at +0.31 eV to Ga in a +1 oxidation state (as in Ga_2O) and the peak at +1.41 eV to Ga^{+3} (as in Ga_2O_3) [18,29,30]. The peak at +2.1 eV is probably due to a mixed oxide component such as $GaSbO_4$ [30]. The native oxide (Fig. 3(b)) is dominated by Ga_2O_3, with a small additional contribution of Ga_2O. The bulk peak is hardly visible due to the attenuation of the oxide, similar as for the Sb *4d* case (Fig. 2 (b)), underlining the existence of a relatively thick native oxide layer, consisting of Sb-oxides (probably Sb_2O_3), Ga_2O_3, and a small amount of Ga_2O.

Upon cleaning, the amount of the Ga_2O_3 component is nearly the same after 2 minutes, but significantly reduced after 10 minutes, and it is almost gone after 20 minutes. Here it has to be noted that the last cleaning step was performed at 250°C instead of 200°C, which seems to be essential for the almost complete removal of this oxide component. Interestingly, the Ga_2O component gets significantly increased upon initial cleaning (after 2 min, Fig. 3(c)), only after the last cleaning step its amount is reduced again. This trend may be explained by a reduction of Ga from a +3 to a +1 oxidation state. However, we also need to consider the Sb *4d* results upon cleaning, where most of the Sb-oxides were removed already after 2 minutes. This does not only demonstrate that the Sb-oxides are easier to remove than Ga_2O_3, in agreement with

the larger negative Gibbs energy of formation of Ga_2O_3 [10], but it also indicates the possibility that the increase in Ga_2O might be connected with the removal of Sb-oxides due to a Ga-Sb-O redox reaction. Indeed, the increase of the amount of Ga-oxide connected to the removal of Sb-oxides during annealing of GaSb has been reported previously [10,13].

We now turn to the Ga *3d* spectra acquired on the nanowire sample, presented in Fig. 3 (f-j). Again, the intensity of the nanowire XPS signal is substantially lower than that of the flat substrates, and the large background makes fitting of the data more challenging. Furthermore, as the GaSb nanowires were grown on InAs nanowire stems, a small In *4d* signal is overlapping at the low binding energy side of the Ga *3d* spectra, and the O *2s* signal of the oxidized Si substrate is overlapping at the high binding energy side. In order to reduce the influence of these signals, fitting of the Ga *3d* data was performed in a narrow binding energy interval between 19 and 22.5 eV. There are two interesting observations regarding the native oxide on the nanowires: First, the amount of Ga-oxides on the nanowires is lower than that on the flat substrate, as can be seen in Fig. 3 (g), where the Ga-Sb doublet becomes clearly visible. The size of the blue and green doublets in Fig. 3 (g) might, however, be slightly overestimated due to the restrictive background subtraction mentioned above. Compared to the Sb *3d* spectra of the nanowires (Fig. 2 (g)), the ratio between oxide peaks and bulk peak is larger for the Ga *3d* data, indicating that the native oxide on the nanowires is more Ga-rich than on the flat substrate. Second, the oxide peak with the highest binding energy, attributed to $GaSbO_4$, which was very small for the substrate, is much more substantial in the nanowire spectra, where it reaches nearly the same height as that of Ga_2O_3 (Fig. 2(g)). This significantly different composition of the native oxide on the nanowires might be due to the different surface orientation – the nanowires are terminated by (110) facets, while the surface orientation of the substrate is (001) – and to the morphology of the nanowire surfaces, which typically contains far more surface steps than the flat substrate.

Upon H-plasma cleaning, the mixed $GaSbO_4$ oxide component follows the same dynamics as the Sb-oxides studied before, as it is strongly decreased in size already after 2 minutes (Fig. 2(h)) and completely removed after 10 minutes of cleaning (Fig. 2(i)). The Ga_2O_3 component, in contrast, shows the same behavior as for the flat substrate, it is strongly reduced in size only after 10 minutes of cleaning, and is removed below the detection limit after additional 10 minutes of cleaning at higher annealing temperature (Fig. 2(j)). The Ga_2O peak, which is the smallest component of the Ga-oxides for the native nanowires, gets strongly increased upon the first 2 minutes of cleaning, its relative size compared to that of the Ga_2O_3 peak is significantly larger than in the case of the flat substrate. This could be connected to the strong decrease of the nanowire-specific mixed GaSbO4 oxide component over the same period, indicating that the Ga atoms get reduced from a +3 to a +1 oxidation state. The amount of Ga_2O is found to be strongly reduced after 10 minutes of cleaning, and even further after 20 minutes. Interestingly, the relative size of the Ga_2O nanowire peak is towards the end of the cleaning procedure significantly smaller than in the case of the flat substrate, highlighting that the H-plasma cleaning is even more efficient for the nanowires also regarding Ga-oxides.

While the removal of Sb-oxides upon cleaning of GaSb has been observed before, the almost complete removal of Ga-oxides observed here has to be emphasized. McDonnell et al. reported a UHV annealing study of planar GaSb [10], where the Sb-oxides were removed at a temperature of about 350°C, but the amount of Ga-oxides got reduced only at temperatures above 550°C, while in our case of H-plasma cleaning a sample temperature of 250°C was sufficient, which is important for implementing the cleaning step in III-V semiconductor device processing. Barth et al. also used a H-plasma source for cleaning of GaSb prior to ALD of Al_2O_3 [15], where they observed a complete removal of Sb-oxides, while a substantial amount of Ga-oxides was left on the GaSb surface, unless the cleaning process

was supported by wet chemical etching. Ruppalt et al. even observed an increase of the amount of Ga-oxides about H-plasma cleaning of GaSb [14]. In addition to the reduction of the total amount of Ga-oxides, also the type of oxide left on the sample is relevant. For the GaAs material system, it has been found that interfacial Ga_2O_3 is detrimental for device performance, while Ga_2O is less harmful [31]. This was correlated to Ga^{+3} states in the GaAs band gap, close to the valence band edge [32]. For GaSb, these states would be expected to be positioned within the valence band, where they might act as border traps, restricting Fermi level movement in GaSb-based transistors. Therefore it is important to note that only Ga_2O was found left on our GaSb nanowires after H-plasma cleaning.

IV. CONCLUSIONS

We have shown the successful cleaning of GaSb surfaces by H-plasma treatment. In agreement with previous reports, we observed a removal of the Sb-oxides combined with an increase of Ga-oxides during initial cleaning. However, in our study continued cleaning resulted in an almost complete removal of Ga-oxides as well. The cleaning was found to be especially effective for GaSb nanowires, where a small amount of Ga_2O was the only oxide to be left on the surface. A further optimization of the nanowire surface topography, reducing the number of surface steps, and of cleaning temperature and duration might even lead to a complete oxide removal. Already now, the cleaned GaSb nanowires are free of Sb-oxides, metallic Sb, and Ga in a higher oxidation state, and therewith free of the major sources of interface defects.

We suggest to implement this H-plasma cleaning step as a standard pre-treatment in plasma-enhanced ALD of high-k oxides for GaSb-based device processing, especially for GaSb nanowires. Cleaning was performed here at a maximum sample temperature of 250°C, which is compatible with most ALD procedures. No wet chemistry was involved, resulting in a

simple, fast, and cost-effective method. Therefore, the results of this work show great promise for effective cleaning and improved performance of GaSb nanowire devices.

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Paper VII

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Performance enhancement of GaSb vertical nanowire p-type MOSFETs on Si by rapid thermal annealing

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Abstract

GaSb is considered as an attractive p-type channel material for future III-V metal-oxide-semiconductor (MOS) technologies, but the processing conditions to utilize the full device potential such as low power logic applications and RF applications still need attention. In this work, applying rapid thermal annealing (RTA) to nanoscale GaSb vertical nanowire p-type MOS field-effect transistors, we have improved the average peak transconductance ($g_{m,peak}$) by 50% among 28 devices and achieved 70 μS μm^{-1} at $V_{DS} = -0.5$ V in a device with 200 nm gate length. In addition, a low subthreshold swing down to 144 mV dec^{-1} as well as an off-current below 5 nA μm^{-1} which refers to the off-current specification in low-operation-power condition has been obtained. Based on the statistical analysis, the results show a great enhancement in both on- and off-state performance with respect to previous work mainly due to the improved electrostatics and contacts after RTA, leading to a potential in low-power logic applications. We have also examined a short channel device with $L_g = 80$ nm in RTA, which shows an increased $g_{m,peak}$ up to 149 μS μm^{-1} at $V_{DS} = -0.5$ V as well as a low on-resistance of 4.7 k$\Omega\cdot\mu$m. The potential of further enhancement in g_m via RTA offers a good alternative to obtain high-performance devices for RF applications which have less stringent requirement for off-state performance. Our results indicate that post-fabrication annealing provides a great option to improve the performance of GaSb-based p-type devices with different structures for various applications.

Supplementary material for this article is available online

Keywords: GaSb, vertical nanowire, p-type MOSFET, performance enhancement, RTA

(Some figures may appear in colour only in the online journal)

1. Introduction

III-V compound semiconductors are a promising channel material for the next generation high speed complementary-metal-oxide-semiconductor (CMOS) circuits thanks to their high carrier mobilities and injection velocities [1, 2]. High performance n-type metal-oxide-semiconductor field-effect transistors (MOSFETs) based on III-As materials, such as In(Ga)As [3, 4], have successfully demonstrated competitive on-state performance with respect to current Si-based n-MOSFETs. For their p-type counterpart, in spite of the high hole mobility in antimonides such as GaSb and InGaSb [2, 5], fabrication of GaSb-based p-MOSFETs with competitive performance is still challenging. III-V p-MOSFETs are mainly limited by gate-stack properties [6] and high-resistive, non-ohmic contacts [7] resulting in unbalanced

performance in all-III-V CMOS technology [8–10]. Although one alternative with co-integration of conventional SiGe p-type and InGaAs n-type MOSFETs has been proposed [11, 12], the difficulty in material chemistry during processing may limit this type of device integration. Moreover, p-type GaSb play an essential role in heterostructure tunneling FETs [13] for emerging low power application. Thus, the motivation of further investigation and development of III-V p-type transistors still remains. Earlier studies based on (In)GaSb MOSFETs with various device structures [5, 14–17] have shown the challenge to retain the off-state performance when scaling from a long channel device to a short channel device ($L_g < 500$ nm). Thus, the trade-off between on- and off-state performance during gate length scaling therefore needs to be solved.

Recently, in a vertical nanowire (VNW) architecture using a gate-all-around (GAA) geometry, we have demonstrated GaSb VNW p-MOSFETs with improved electrostatic control and high transconductance [18, 19], as compared to other reported GaSb-related MOSFETs. Although an on/off current ratio of about 700 was demonstrated within 1.5 V gate voltage modulation in a 60 nm channel VNW devices [18], a further enhancement is doubtlessly required to approach low power logic applications. Rapid thermal annealing (RTA) is an important technique widely used in semiconductor device fabrication to improve the performance by influencing the material properties, such as dopant activation and defect passivation, as well as contacts improvement [20]. By annealing in a forming gas (N_2/H_2), the electrical properties at the interface between the semiconductor and gate oxides can be improved by the RTA process thanks to the passivation of interface defects (D_{it}), as reported for InGaAs n-channel devices [21]. Several investigations regarding contact improvement using RTA in n-MOSFETs have been also demonstrated, applied on both conventional planar devices [22] and nanoscale VNW MOSFETs [23]. In terms of GaSb-based technologies, it has been proven that the sheet resistance of Ni–GaSb can be lowered by RTA [24, 25] which may offer a possibility to improve the contact. However, for using RTA on the device level, only planar GaSb long channel (gate length $L_g \approx 5\ \mu$m) MOSFETs were reported by comparing individual device performance before and after annealing [17, 26], and it is not clear how the annealing affects the electrostatics and the contacts in short L_g devices.

In this work, we for the first time apply post fabrication RTA to nanoscale GaSb VNW transistors with two different device structures (sample 1:200 nm L_g with Ni top contact; sample 2:80 nm L_g with W top contact) and achieve substantial improvements in transistor performance in both samples. Section 3.1 mainly discusses the on-state performance in the different samples with varying RTA temperatures. Section 3.2 focuses on the influence of RTA on the on-resistance (R_{on}) while section 3.3 discusses the annealing effects on the electrostatics and off-state performance. Finally, a further discussion and the corresponding benchmark will be shown in section 3.4 Our statistical results in this study reveal that RTA can be used as a device performance booster for GaSb p-type transistors in order to reach a specific application.

2. Experimental methods

InAs-GaSb NWs were grown on a prepatterned Si substrate with a 260 nm n^+-InAs buffer layer by metal-organic vapor-phase epitaxy (MOVPE) via vapor–liquid–solid process. InAs buffer layer was used for the integration of III-V materials on Si substrates. The NW growth started with a short n-type InAs stem doped with Sn to not only enable nucleation of GaSb NW growth, but also form the source of the device, which has an InAs/GaSb broken band tunneling junction to assist the carrier transport [27]. Subsequently, undoped GaSb with an estimated background doping of $\sim 10^{16}$ cm^{-3} and p-type GaSb NWs doped with Zn (molar fractions: $\chi_{TMGa} = 4.9 \times 10^{-5}$, $\chi_{TMSb} = 5.6 \times 10^{-5}$, DEZn/TMGa = 0.39) were grown for the channel and the drain, respectively. Here, two samples with different structures as well as process schemes were fabricated and compared. Sample 1 (S1) was grown as the above structure and fabricated with a gate-first process starting from the NW bottom. In contrast, a gate-last process starting from the top contact of the NW transistors was employed for sample 2 (S2) which has a 2 nm thick Sn-doped InAs shell as an interfacial layer for the top (drain) contact.

The device fabrication for S1 was initialized by the digital etching while the first step for S2 was the drain contact which requires several additional steps discussed below. Firstly, a 20 nm thick Al_2O_3 was deposited by atomic layer deposition (ALD) as the first spacer which was then removed in the drain region of the NW MOSFET. The length of the drain was defined by a back-etch process with S1813 (photoresist). Next, the drain contact was formed by sputtering 20 nm W which was dry etched anisotropically leaving metal only on the NW sidewalls. The S1813 was further thinned down to define the gate length. Then the Al_2O_3 on the channel region was wet etched and S1813 removed. Next, the diameter of the GaSb channel was reduced by ~10 nm and ~20 nm in S1 and S2, respectively, using repeated digital etching with oxidation inside an oxygen chamber followed by an oxide etch in HCl:IPA (1:10) for 30 s. In the case of S2, the oxidation for the first cycle of digital etch was carried out in an ozone ambient for 30 s at 50 °C to fully oxidize the InAs shell. A bilayer high-k film with 1 nm Al_2O_3/3 nm HfO_2 (EOT ≈ 1 nm) was deposited using ALD. For S1, an extra 20 nm Al_2O_3 layer was grown after the high-k film as the first spacer whose height was defined by the same back-etch process using S1813. The remaining fabrication steps were identical for two samples. A 60 nm W was sputtered for the gate metal and the excess gate-metal was subsequently removed using S1813 mask and dry etching. The gate length in S1 was defined in this step. Both the NW diameter of the channel and the gate length in S1 and S2 were verified by the scanning electron microscopy (SEM) image shown in figures 1(a) and (b), respectively. The samples were finalized by the second spacer deposition and the contact metallization.

Figures 1(c) and (d) illustrate the schematics of the final NW transistor in S1 and S2, respectively. In order to enable post processing annealing of the samples at high temperatures, all the spacers for isolating the terminals are replaced with Al_2O_3 rather than polymers which were usually used as

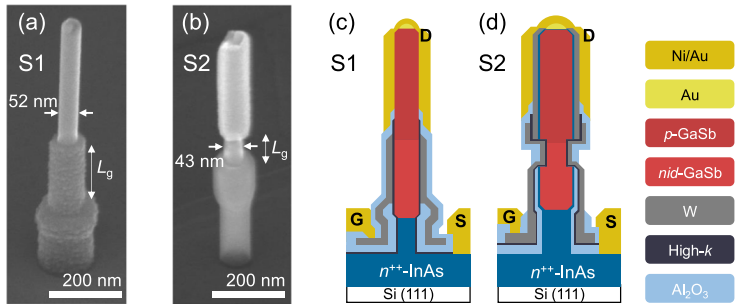

Figure 1. SEM images of the real NW devices: (a) a device in S1 with $L_g = 200$ nm after gate length definition; (b) a device in S2 with $L_g = 80$ nm after high-*k* deposition. The marked diameters include the channel diameter and the high-*k* thickness (4 nm). Schematics of the GaSb single NW transistor are displayed in (c) S1 and (d) S2. G, S and D denote gate, source and drain, respectively. *nid* represents non-intentionally doping.

Table 1. Differences in device structures between two samples.

No.	Process sequence	Top contact	L_g	Channel diameter	RTA
Sample 1 (S1)	Gate-first	Ni/p-GaSb	200 nm	44 nm	200 °C–350 °C
Sample 2 (S2)	Gate-last	W/n-InAs/p-GaSb	80 nm	35 nm	250 °C–350 °C

the second spacer in our previous work [10, 28]. After initial electrical characterizations for the devices, an RTA process was performed in wall-mounted rapid thermal processing (RTP) system, RTP-1200-100, from UniTemp GmbH, with a forming gas (N_2/H_2, 95%/5%) for 2 min at temperatures from 200 °C to 350 °C for S1 and 250 °C to 350 °C for S2. Two step temperature ramping scheme (the temperature first increases to 50 °C less than the setpoint in 30 s and stabilizes for 20 s. Then the temperature continues increasing by a ramping rate of 1.67 °C s^{-1} to the target.) was employed in order to avoid the temperature overshooting. When it reaches the desirable temperature, 2 min is waited before cooling down without supplying any power on the heater. Devices were electrically characterized sequentially after each RTA process. The main information and differences between two samples are summarized in table 1. All the devices in this work are based on single NW transistors. In S2, the highly doped GaSb/InAs core/shell structure in the drain combined with the W–InAs contact can help to lower the resistivity [29, 30].

3. Results and discussion

3.1. Transistor on-state performance improved by RTA

The transfer characteristics of the individual GaSb NW MOSFET in each sample before and after RTA at different temperatures are shown in figure 2. In consideration of the change in threshold voltage (V_T) after RTA (see supplementary material: figure S1 (available online at stacks.iop.org/NANO/33/075202/mmedia)), the gate overdrive voltage, $V_{OV} = V_{GS}–V_T$, is presented in this article instead of the absolute gate bias V_{GS} for better comparison. Generally, as compared to the as-fabricated device performance, the drain current (I_{DS}) as well as g_m increases after RTA and reaches a maximum after annealing at 300 °C in both samples. Further increasing the RTA temperature up to 350 °C, however, degrades the on-state performance in both samples. In S1, an increased on-current (I_{on}, defined at $V_{OV} = -0.5$ V) of 31 μA μm^{-1} as well as a peak g_m ($g_{m,peak}$) of 70 μS μm^{-1} at $V_{DS} = -0.5$ V are achieved in the device after RTA at 300 °C with corresponding increment of ~25% as shown in figures 2(a) and (b), respectively. However, the source depletion of the device in S1 becomes severe after annealing at 350 °C probably due to higher efficiency in hydrogen passivation at the InAs/high-*k* interface than that in GaSb/high-*k* interface so that InAs bands adjacent to the junction move up faster than GaSb bands at high negative gate bias. As a result, the tunneling probability between InAs and GaSb may be reduced, thereby lowering the drain current. Despite a thicker oxide layer including both the high-*k* and the bottom spacer (Al_2O_3) on the InAs segment, substantially lower D_{it} at the interface of InAs/high-*k* likely results in high gating efficiency at high gate voltage. Several reports have shown that the optimal annealing temperature of hydrogen passivation of In(Ga)As/high-*k* interface is close to 350 °C [31, 32]. Therefore, annealing at lower temperatures has relatively limited effects on InAs/high-*k* interface passivation, resulting in less source depletion.

Thanks to a shorter L_g, S2 provides a better on-state performance in both I_{DS} and $g_{m,peak}$, but meanwhile higher

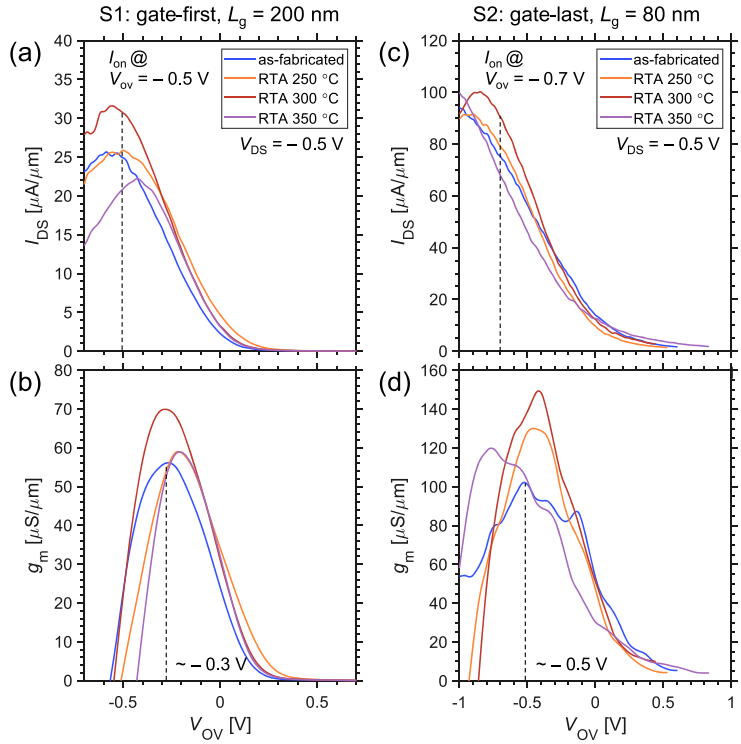

Figure 2. Transfer characteristics of (a), (b) S1 and (c), (d) S2 before (as-fabricated) and after RTA at different temperatures. Here, an overdrive voltage $V_{OV} = V_{GS}–V_T$ is used to align $V_{GS} = V_T$ to 0 in all the cases. $I_{DS}–V_{OV}$ are shown in (a) and (c) while $g_m–V_{OV}$ are shown in (b) and (d). Ion is defined at $V_{OV} = -0.5$ V and -0.7 V for S1 and S2, respectively. The reason of using different V_{OV} for I_{on} definition is to keep the identical gate bias (0.2 V) away from the position of as-fabricated $g_{m,peak}$ in both samples as shown in figures.

overdrive bias (~0.2 V higher in V_{OV}) is needed to achieve $g_{m,peak}$ as compared to S1, seen in figures 2(b) and (d). Thus, to reflect this difference, we defined I_{on} at relatively higher V_{OV} (-0.7 V) for S2. Here, as the comparison of I_{on} only occurs before and after RTA in the same sample, I_{on} may well be defined independently between two samples. In S2, despite only 20% increase in I_{on}, $g_{m,peak}$ is enhanced by almost 50% up to 149 μS μm^{-1} after RTA at 300 °C.

Figure 3 shows the corresponding statistical results based on 28 single NW devices in both S1 and S2, as a function of RTA temperatures. In the case of S1, the median values of I_{on} and $g_{m,peak}$ determined at different RTA temperatures are compared in figures 3(a) and (b), respectively, showing an unambiguous enhancement with increasing the annealing temperature from 200 °C to 300 °C whereas maintaining almost the same value when further increasing the temperature to 350 °C. In figure 3(b), $g_{m,peak}$ increases 50% on average after RTA at 300 °C compared to as-fabricated devices, reaching a maximum median value of 42 μS μm^{-1}. It is noticeable that when increasing the RTA temperature, the minimum $g_{m,peak}$ increases more than 100% and it follows the same trend as the median value while the maximum $g_{m,peak}$ increases roughly 10%. Therefore, the $g_{m,peak}$ increase mainly results from the enhancement in those devices with low as-fabricated $g_{m,peak}$. However, after annealing at 350 °C, those devices start degrading again, resulting in a reduced minimum value in both I_{on} and $g_{m,peak}$. Thus, the spread of the data set after annealing at 300 °C is narrowed but widened again when annealing at 350 °C due to the device degradation. In addition, a similar feature of I_{on} change with the RTA temperature is shown in figure 3(a).

3.2. Annealing effects on R_{on}

Figure 4(a) compares the output characteristics of the same devices plotted in figure 2 before and after RTA. Here, only the output curve at V_{OV} that defines I_{on} is selected to present for both samples, respectively. For the individual devices in S1 and S2, R_{on} first decreases when annealing at 300 °C, reaching 16.7 k$\Omega\cdot\mu$m and 4.7 k$\Omega\cdot\mu$m in the device of S1 and

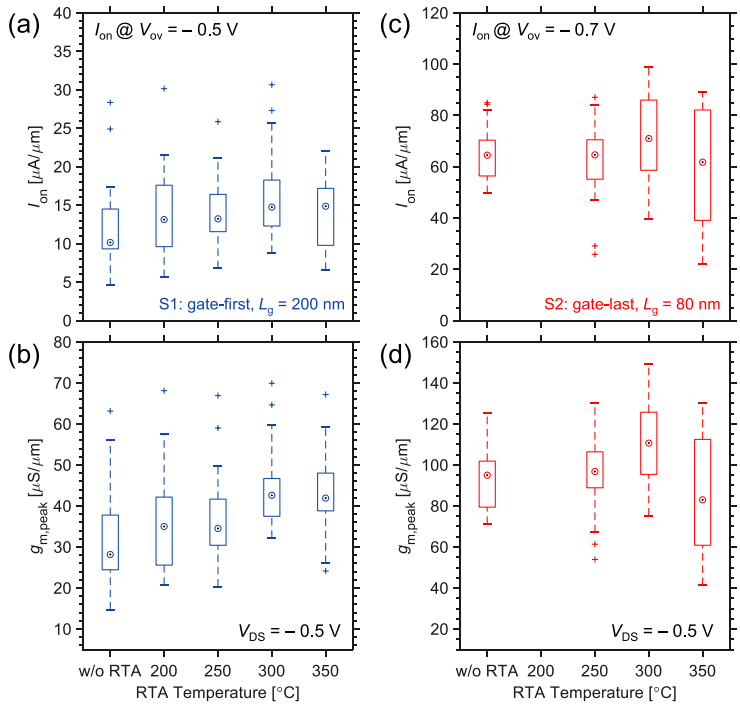

Figure 3. Statistics of (a), (c) I_{on} and (b), (d) $g_{m,peak}$ as a function of RTA temperatures in (a), (b) S1 and (c), (d) S2. Data are shown in a boxplot based on 28 devices in each sample. The same dataset for all other figures in this article. $V_{DS} = -0.5$ V for all plots.

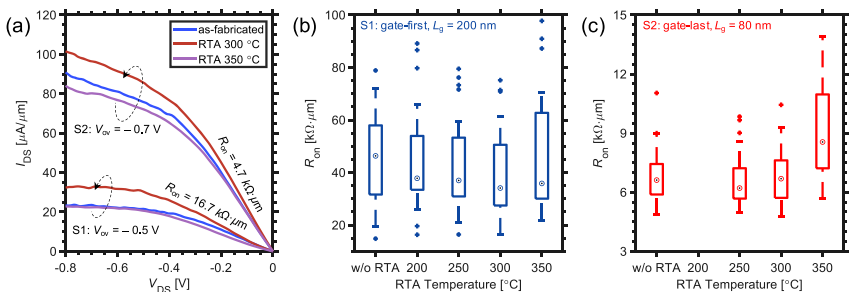

Figure 4. Annealing effects on (a) output characteristics of the same device in figure 2 at the gate bias which is used to define I_{on} in S1 and S2. (b) and (c) show the statistics with boxplots of R_{on} as a function of RTA temperature in S1 and S2, respectively.

S2, respectively, but increases again after RTA at 350 °C. Similar as the individual devices, the corresponding statistical result of R_{on} in S1 shows decreasing R_{on} as increasing the RTA temperature until 300 °C, presented in figure 4(b). In spite of the large variation in R_{on}, it is found that the median R_{on} of all devices annealed at 300 °C is still reduced 26% as compared to that without annealing. In contrast to the clear drop in R_{on} after RTA observed in S1, no noticeable change of R_{on} is observed in S2 in the same RTA temperature interval, shown in figure 4(c). Instead, almost identical median value and device variation are obtained with increasing RTA temperature until 300 °C. Among the 28 studied devices in S2, there are 12 devices with a higher R_{on} after RTA at 300 °C and 16 devices having a lower value. Although the maximum reduction reaches 33%, most of the devices have a change within ±10%, leading to a similar

median value after RTA. As compared to S1, a 7-times lower mean R_{on} (6.5 k$\Omega\cdot\mu$m) is achieved before annealing in S2, while the gate length is only 2.5 times shorter. Hence, the top contact is likely improved with W–InAs/GaSb configuration, thereby contributing to significant R_{on} reduction in S2.

It is reasonable to assume that the access resistance will remain constant when annealing at such moderate temperatures (200 °C–350 °C). The access resistance is mainly determined by the geometry and the carrier density, which relates to the doping concentration in this case. Since the epitaxial growth temperature of the NWs is much higher than the annealing temperatures, the doping profile should be unchanged after RTA. Therefore, we believe that the R_{on} reduction in S1 after RTA can be mainly interpreted as the improvement of the top contact in the NW transistors. Annealing can promote Ni to alloy with GaSb, leading to more Ni–GaSb alloy formed at high temperature thus lowering the sheet resistance of Ni–GaSb alloy layer [7, 24]. Extrapolating to the transistor level, the contact resistance can be lowered by forming higher conducting Ni–GaSb alloy after annealing. However, higher annealing temperatures may degrade the contact attributed to the presence of a new phase Ni_2Ga_3 (forming at 369 °C according to the phase diagram [33] with higher resistivity in the alloy while the desired NiGa (Sb) phase is only formed at relatively low annealing temperature [25]. Consequently, a slight increase in R_{on} occurs after RTA at 350 °C in S1.

Despite unchanged median value and variation in statistical result of R_{on} in S2, a small variance within 10% is still found in most of the devices. R_{on} increasing or decreasing in this case could be attributed to the relatively slight change in the top contact which is W–InAs/GaSb in S2. W is used as a non-alloy ohmic contact for InGaAs transistors [4] and behaves similarly as Mo [28] for contacting InGaAs. Moreover, a recent study on InGaAs VNW devices with Mo–InGaAs (similar as W–InGaAs) non-alloy contact shows a smaller change in R_{on} with varying RTA temperatures as compared to Ni–InGaAs transistors [23]. Thus, W–InAs/GaSb likely provides a rather thermally stable contact below 300 °C as compared to Ni–GaSb. However, we observed a dramatic increase in not only the median value but the spread of R_{on} after RTA at 350 °C, which may highly relate to the deterioration in channel interface thus leading to a dominantly large channel resistance as compared to considerably low contact resistance in S2. The annealing effects on the interface will be discussed in the next section

3.3. Annealing effects on electrostatics and off-state performance

Figure 5(a) presents the statistics of saturation *SS* (SS_{sat}, at $V_{DS} = -0.5$ V) with varying RTA temperature. For S1, SS_{sat} continuously reduces when increasing the annealing temperature even up to 350 °C. Specifically, the reduction in SS_{sat} is mainly determined by the improvement of devices with originally high *SS*, thus a narrower distribution is achieved, reaching a lowest $SS_{sat} = 166\,\mathrm{mV\,dec^{-1}}$ in a device as shown in figure 5(b). A similar trend based on statistics is observed for SS_{lin} (see supplementary material: figure S2(a)) and a minimum value of $144\,\mathrm{mV\,dec^{-1}}$ is obtained in the same device shown in figure 5(b), which is the lowest subthreshold swing among reported GaSb-based p-MOSFETs [8, 17, 19, 34]. In accordance with the equation [35] $SS \approx (kT/q)\cdot \ln(10)(1 + qD_{it}/C_{ox})$, where k is the Boltzmann constant, T the temperature, q the electron charge and C_{ox} the capacitance of the high-k oxides which is assumed to be invariant with annealing [36]. D_{it} refers to the trap density of the MOS interface, usually describing the interface quality. The lower D_{it}, the better interface quality. Based on this equation, the change of *SS* can be determined by D_{it} only. Thus, we estimated $D_{it} \approx 3.6 \times 10^{13}\,\mathrm{eV^{-1}\,cm^{-2}}$ at $V_{DS} = -0.05$ V after annealing by calculating a coaxial oxide capacitance of $C_{ox} \approx 7\,\mathrm{aF\,nm^{-1}}$. By considering the same device before annealing, D_{it} approximates to $4.4 \times 10^{13}\,\mathrm{eV^{-1}\,cm^{-2}}$, thus indicating a reduction of 22%. Therefore, the reduction in *SS* can originate from the MOS interface improvement by lowering D_{it} attributed to the H_2 passivation capability during RTA.

In contrast, S2 exhibits an opposite trend of SS_{sat} (also see SS_{lin} trend in supplementary material: figure S2(a)) with RTA temperature, showing a significant increase after annealing at 300 °C–350 °C. Although S2 has a higher SS_{sat} than S1 before RTA, a similar drain-induced barrier lowering is found in S1 and S2, suggesting a good electrostatic control without short channel effect when scaling down L_g from 200 to 80 nm. Therefore, the high *SS* before RTA in S2 mainly results from the increase of D_{it} at the channel interface as compared to that of S1 fabricated with the gate-first process. For the gate-last process in S2, many additional steps are required prior to the digital etching and subsequent high-k deposition, resulting in unexpected process-induced contaminations. One likely contamination of the channel can be oxygen vacancy from residual GaSb oxides present from the digital etching. The first 30 s ozone treatment at 50 °C is likely to oxidate through the InAs shell and deeply penetrate into GaSb to form a thick GaSb oxide layer [37] which may be insufficiently etched by HCl:IPA for 30 s in the current process. The presence of oxygen vacancy at the interface may generate more traps at the GaSb/high-k interface thereby increasing *SS*. Although these oxygen vacancies might be reduced by annealing in an ambient with hydrogen, other possible contamination originating from the previous process would be active to react with the channel surface when annealing, probably leading to more interface states. Thus, the dramatic increase of *SS* after RTA is likely related to these interface states activated by annealing. As a result, D_{it} increases substantially after RTA at 300 °C or higher, leading to a poor off-state performance. Further detailed material characterizations for the channel interface in our NWs, such as x-ray photoelectron spectroscopy and transmission electron microscopy, are needed to verify of our hypothesis.

The off-state performance in S1 is further studied. The device with lowest *SS* after RTA at 350 °C also reveals a high on/off current ratio (I_{on}/I_{off}) over 1000 with attractive $I_{on} = 23\,\mu\mathrm{A\,\mu m^{-1}}$ and a low $I_{off} = 19\,\mathrm{nA\,\mu m^{-1}}$ at

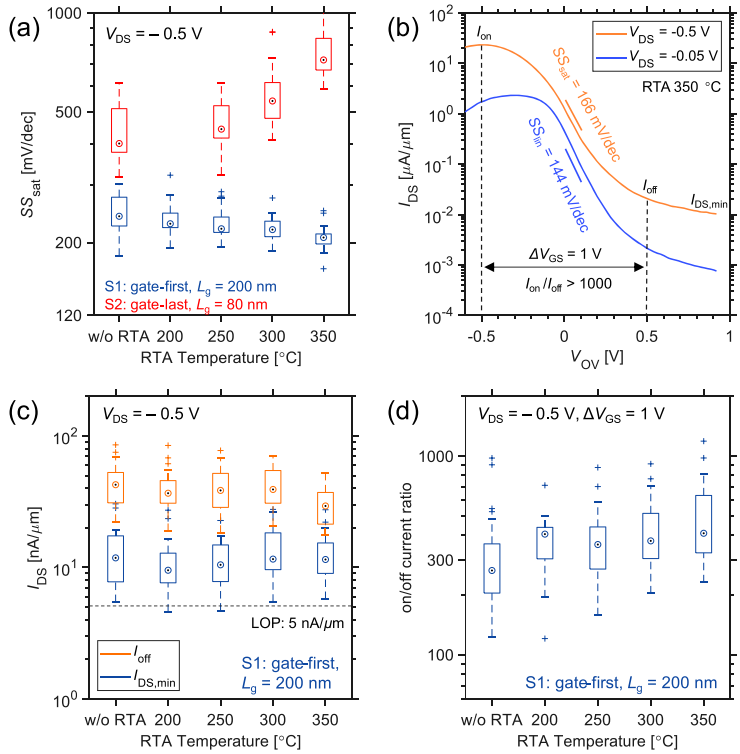

Figure 5. Annealing effects on electrostatics and the off-state performance. (a) Statistics of SS_{sat} in both samples. *Y*-axis is plotted in logarithm. (b) Transfer characteristics of the device with lowest *SS* and highest I_{on}/I_{off} at $V_{DS} = -0.5$ V in S1. I_{on} is defined at $V_{OV} = -0.5$ V while I_{off} is defined at $V_{OV} = 0.5$ V. Statistics of (b) I_{off} and minimum I_{DS} at off-state in the range of $0\text{ V} < V_{GS} < 1\text{ V}$, as well as (c) on/off current ratio I_{on}/I_{off} in S1.

$V_{DS} = -0.5$ V, as demonstrated in figure 5(b). In figure 5(c), a stable $I_{off} = 40\text{ nA }\mu\text{m}^{-1}$ retains until annealing at 300 °C and further reduces to $30\text{ nA }\mu\text{m}^{-1}$ after RTA 350 °C. In addition, the minimum drain current ($I_{DS,min}$) fluctuates with RTA temperatures in a small range around $\sim 10\text{ nA }\mu\text{m}^{-1}$. The lowest $I_{DS,min}$ in all studied devices at off-state reaches $4\text{ nA }\mu\text{m}^{-1}$ after annealing at 200 °C and 250 °C, which fulfills the I_{off} specification of the International Technology Roadmap for Semiconductors low operation power application ($5\text{ nA }\mu\text{m}^{-1}$) [38]. In addition, approximately 50% increase in I_{on}/I_{off} is attained after RTA at 350 °C attributed to both I_{on} increase and I_{off} reduction with respect to as-fabricated performance as shown in figure 5(d). On the other hand, only I_{on} increase accounts for the gradual increase in I_{on}/I_{off} when the annealing at 200 °C–300 °C. The results of S1 show the best balance in on- and off-state performance among recently reported GaSb-related transistors [10, 18, 39], indicating an attractive potential for low power logic applications. In contrast, the off-state performance degrades significantly after RTA process in S2 as both *SS* and I_{off} (see supplementary material: figure S2(b)) increase with annealing temperatures.

Table 2. Summary of the RTA effects on S1 and S2 by comparing the difference before and after RTA at 300 °C.

Ave. change	$g_{m,peak}$	I_{on}	R_{on}	SS_{lin} / SS_{sat}
S1: gate-first	+50%	+47%	−26%	−10%/−9%
S2: gate-last	+20%	+9%	0%	+30/+31%

3.4. Discussion and benchmarking

Based on the analysis in the previous sections, it is evident that RTA at 300 °C provides the best performance improvement with annealing in both S1 and S2. Thus, table 2 summarizes the improvements and changes in each sample after RTA at 300 °C with respect to the as-fabricated performance. For S1, the improvements of not only the top contact but the channel interface after RTA lead to the reduction in both R_{on}

Table 3. Benchmarking devices in S1 with other published GaSb-based p-type MOSFETs at $V_{DS} = -0.5$ V. Blank spaces are due to incomplete data.

	S1 in this work			IEDM18 [19]	TED2020 [18]		IEDM17 [39]	IEDM15 [8]
Structure	VNW-1	VNW-2	VNW-3	VNW	VNW-1	VNW-2	FinFET[a]	LNS[b]
L_g (nm)	200	200	200	60	110	60	20	500
Diameter (nm)	44	44	44	22	24	24	10	20
SS_{lin} (mV dec^{-1})	144	157	162	175		224	260	217
SS_{sat} (mV dec^{-1})	166	189	175	305	216			188
$I_{DS,min}$ (nA μm^{-1})	9	9	4	~3000	~4	28	~2000	5
I_{on} at $V_{GS} = -0.5$ V (μA μm^{-1})	23	31	16	98	3	20	100	~10
I_{on}/I_{off} with $\Delta V_{GS} = 1$ V	1190	980	1210	~30	~750	330	50	~2000

[a] InGaSb channel.
[b] LNS denotes lateral nanosheet.

and *SS*, thus in turn contributing to an enhancement of $g_{m,peak}$ by 50% on average. Surprisingly, for S2, $g_{m,peak}$ achieves 20% increment after annealing whereas R_{on} keeps invariant and *SS* deteriorates due to more unexpected contamination in S2. In spite of an invariant R_{on} on average, slight change still exists in individual devices (see supplementary material), where those devices with reduced R_{on}, the $g_{m,peak}$ increase linearly depends on the reduction in R_{on}. Therefore, the reduction of R_{on} could be the unique contribution to the $g_{m,peak}$ increase, leading to less improvement in percentage of $g_{m,peak}$ for S2 as compared to S1. The detailed correlation of $g_{m,peak}$, R_{on} and *SS* regarding on individual devices in both samples is shown in supplementary material: figures S3 and S4.

The average change reflects the similar conclusions as discussed previously. For S1, it is difficult to significantly improve the top contact and channel interface at the same since effectively improving MOS interface usually requires a higher annealing temperature (approximately 350 °C) [40, 41], which could degrade the top contact of the device (increasing R_{on}) by changing the Ni–GaSb alloy structures as addressed previously. One feasible option to further improve GaSb NW MOSFETs by annealing is probably to include both forming gas (N_2/H_2) annealing directly after gate metal deposition for the MOS interface at a higher temperature and another annealing process at a relatively lower temperature after fabrication to only improve the contacts [41]. For S2, the key issue is the high *SS* which likely results from the process-induced contamination, being strongly degraded by RTA. However, the impressive improvement in g_m exists in those devices with high as-fabricated performance in S2. Thus, although using the characteristics of S2 for digital applications may be challenging, for some RF applications [28] or the current source of all-III-V platform, a high *SS* can still be acceptable. Further gate-stack development can also help to improve *SS*.

Table 3 and figure 6 benchmark this work with recently published GaSb-related p-type MOSFETs with $L_g < 500$ nm. 3 different VNW devices from S1 after annealing are included in table 3, all showing a good off-state current below 10 nA μm^{-1} simultaneously along with a competitive I_{on}, showing a great balance in on- and off-state performance. We

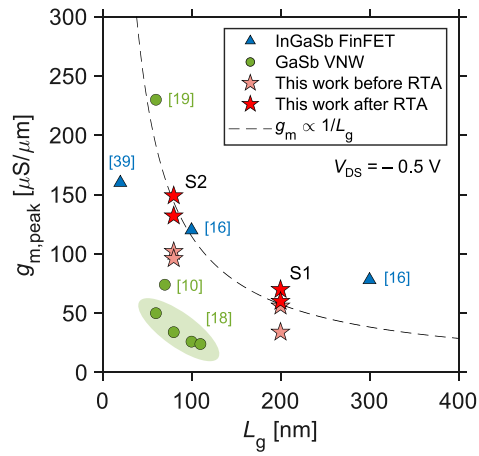

Figure 6. Benchmarking $g_{m,peak}$ versus L_g of the devices in this work and other GaSb-based p-FETs. Stars represent the present work which is in line with state-of-the-art GaSb-based devices after annealing.

have also achieved a record *SS* among all GaSb-based sub-500 nm p-type MOSFETs, verifying a great electrostatic control with the gate-first process. For the benchmarking of $g_{m,peak}$ versus L_g in figure 6, comparing to the performance of not annealed devices, the annealed devices in both S1 and S2 have been improved and both approach the position in line with the gate length scaling in state-of-the-art GaSb-based transistors.

4. Conclusion

We have demonstrated that annealing improves the on-state performance of nanoscale GaSb vertical NW p-MOSFETs on Si with two different structures by RTA. The statistical results show that 50% and 20% increase in $g_{m,peak}$ are achieved in S1 ($L_g = 200$ nm) and S2 ($L_g = 80$ nm), respectively. We also

found that the device structure and processing sequence strongly affect the off-state performance after RTA. For S1, a good off-state is obtained before RTA and remains unchanged after annealing, resulting in an increased on/off current ratio and a low *SS* thanks to the improvement in on-current and channel interface quality, respectively. The results suggest a great balance in on- and off-state performance among all reported sub-500 nm GaSb-based transistors, leading to an attractive potential for III-V based low power logic applications. However, in the case of S2, *SS* strongly increases after RTA probably due to the formation of interface traps during annealing, causing a severe degradation in off-state performance. Despite this, by the means of RTA, a remarkably further enhancement of $g_{m,peak}$ in the devices with as-fabricated high performance is noticed. Thus, RTA can be used as an approach to increase g_m for devices with potential use in III-V RF applications. Our work suggests that the use RTA can be a good strategy to further improve the performance of nanoscale GaSb-based p-type devices with various structures for different applications based on III-V platform technologies.

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Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

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Paper VIII

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Manuscript in preparation

Improved Electrostatics in GaSb vertical nanowire p-MOSFETs by Employing Controllable Digital Etch Schemes

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The performance of III-Sb based MOSFETs are typically inhibited by the formation of the gate-stacks, which leads to detrimental surface conditions. In this study we achieve improved electrostatics of vertical GaSb nanowire p-channel MOSFETs by employing robust digital etch (DE) schemes, prior to high-κ deposition, based on BOE 30:1 and HCl:IPA 1:10, respectively. We demonstrate that water-based BOE 30:1 gives an equally controllable etching for sensitive GaSb nanowires as compared to alcohol-based HCl:IPA, indicating high compatibility with Si-based industrial process flow. Both DE chemicals show good surface quality of GaSb, verified by X-ray photoelectron spectroscopy and electrical characterizations. By implementing these DE schemes into vertical nanowire MOSFETs, a record subthreshold swing of 107 mV/dec is obtained among recently reported III-Sb MOSFETs, suggesting a potential of III-Sb p-type devices for all-III-V CMOS technologies.

1. Introduction

The semiconductor industry is largely Si-based where integrated circuits for processing electronics typically employ various Si-devices, such as the metal oxide

semiconductor field-effect transistors (MOSFETs). However due to physical limitations of MOSFETs employing a Si-channel, the search for alternative materials aimed at substituting the channel is greatly accelerated. Potential replacements for p-type channel devices are semiconductors based on III-antimonide (III-Sb, including GaSb and InGaSb) materials which provide high bulk mobility.[1-3] However, the main challenge of a Sb-based MOSFET to completely benefit from the high mobility of the bulk material is the poor electrostatics. In order to enable greatly improved electrostatic control for scaled transistors, various nanowire based multi-gate architectures such as FinFETs[4] and vertical gate-all-around (GAA) MOSFETs,[5, 6] are being pursued. A key step to achieve scaled nanowire diameters as well as fin-widths for III-V semiconductors has been to employ digital etch (DE) methods to both reduce dimensions and provide native oxide removal.[7, 8] In particular, Sb-based structures are known for rapid re-oxidation leading to high density of interface traps,[9, 10] thus greatly limiting the electrostatic control for MOSFETs. Various surface effects have been detrimental to achieve channel mobilities approaching its bulk counterpart, which also limits the off-state performance of Sb-channel MOSFETs.[11, 12] Many efforts have been taken to improve the GaSb MOS interface quality, such as introducing thin InAs[13] or InGaAs[14] interfacial layer, hydrogen plasma pretreatment,[15] and *in-situ* gate oxide deposition[16]. Moreover, various chemical pretreatments, including $(NH_4)_2S$,[17, 18] $HCl:H_2O$[9, 19] and $HF:H_2O$[5] for GaSb surface passivation have been reported. Although a low density of interface defects (D_{it}) reached ~10^{12} $cm^{-2}eV^{-1}$,[16] the electrostatics of a real MOSFET still needs to be further improved.

In this paper, we achieve the lowest reported subthreshold swing (*SS*) for GaSb-based vertical GAA MOSFETs by digital etching in HCl:IPA 1:10 (the concentration is the same for the entire paper if not specified, thus simplified in HCl:IPA in the following text and figures). In addition, we for the first time introduce BOE (buffer-oxide etcher) 30:1 into DE process in

GaSb device fabrication and find that both water-based BOE and alcohol-based HCl have controllable DE rate for diameter reduction in GaSb NWs. As an alternative, BOE 30:1 is compatible with the industrial process flow in the current Si-based CMOS technology, allowing to directly utilize the same chemical in III-Sb process for potential monolithic integration of III-V with Si. Furthermore, the surface quality of GaSb pretreated by BOE 30:1 and HCl:IPA is evaluated by X-ray photoelectron spectroscopy (XPS) and electrical characterizations which exhibit a reduced *SS* in fabricated MOSFETs for both cases as compared to latest reports regarding on III-Sb transistors, indicating a better electrostatic control.

2. Results and Discussion

2.1. MOSFET structure and performance

Figure 1(a) illustrates the schematic of a single NW MOSFET with GAA architecture. The device fabrication started from the bottom with DE in BOE 30:1 or HCl:IPA and high-κ deposition after the NW growth by metal-organic vapor-phase epitaxy (MOVPE) via vapor-liquid-solid (VLS) process (see experimental method for details). The gate length (L_g) was defined by the vertical photoresist mask which was back etched by oxygen plasma, followed by the gate metal etch on the NW sidewalls shown in Figure 1(b). The actual diameter of the channel is estimated to 46 nm as 4-nm high-κ is included in Figure 1(b). By optimizing the DE condition of GaSb NW MOSFETs, a device with DE in HCl:IPA exhibits the lowest subthreshold swing (*SS*) down to 107 mV/dec at V_{DS} = – 0.05 V, as shown in Figure 1(c), in addition to a minimum off-current (I_{off}) at V_{DS} = – 0.5 V approaching 4 nA/μm which meets the I_{off} specification at low-operation-power (LOP) condition defined by ITRS (International Technology Roadmap for Semiconductors)[20] for low power logic applications.

2.2. Digital Etch comparison

Figure 2(a) shows the schematics of the DE process where the NWs are first oxidized in a O_2 chamber for 8 min and further wet etched by either HCl:IPA or BOE 30:1 for 30 s. Since the oxidation occurs easily for GaSb surface,[10] the exposure of conventional dry oxidations such as ozone[21] and oxygen plasma[7] would generate one of the Sb oxides, namely Sb_2O_5, which is unlikely to be etched by any acids.[22] Therefore, O_2 is selected as a gentle oxidizer for GaSb due to the absence of Sb_2O_5. The wet etch process selectively removes the oxides of both the NW and planar surfaces, thereby reducing the diameter of the NWs. Figure 2(b-i) demonstrate the thinning process of a NW array with original diameter of 48 ± 3 nm and interval of 500 nm after indicated DE cycles in different acids which are compared. In both cases, the NW diameter can be gradually reduced by repeating DE while the etch reaches saturation after certain number of cycles, specifically 5 cycles in HCl:IPA and 7 cycles in BOE 30:1. Additionally, NW breakage appears after 7-cycle DE and increases after doing more DE in BOE 30:1 thereby decreasing the mechanical yield of NWs, but the NW survivability remains 100% after the same amount cycles of DE in HCl:IPA.

Figure 3 summarizes the statistical comparison of DE in BOE 30:1 and HCl:IPA based on the NW array shown in Figure 2 (b-i). It is noticeable that the etch rate initially (first 2 cycles) is similar in both cases and close to 1.2 nm/cycle (2.4 nm/cycle reduction in diameter). However, after 2 cycles, the etch rate gradually shrinks in the case of BOE 30:1 but still retains when etching in HCl:IPA until 5 cycles. The average etch rate in BOE 30:1 is ~1 nm/cycle until the seventh cycle and in consistence with Figure 2, the DE almost stops after 5 cycles in HCl:IPA and 7 cycles in BOE 30:1. The diameter variation increases slightly after DE in HCl:IPA while the variance in diameter remains a constant after DE in BOE 30:1. In contrast with the initial diameter variance of ~5%, the relative variance in NW diameter reaches 4% and 6% after 7 cycles in BOE 30:1 and HCl:IPA, respectively, shown in the inset table of Figure 3. More uniform diameter distribution after DE in BOE 30:1 may result in evener performance between devices (see Figure 5(b)) that are pretreated by BOE 30:1 for the

channel region. Moreover, the mechanical yield after 7 cycles counted from the same NW array in Figure 2(b-i) indicates that DE in HCl:IPA can well prevent NW breaking off as shown in the same table. The reason that a lower yield is found in the case of BOE 30:1 can be water-based acids have higher surface tension as compared to alcohol-based acids,[23] which causes NWs breaking off either during the wet etch step or the following rinsing step.[8]

2.3. Surface-states of GaSb with different pretreatments

XPS characterization of GaSb surface with two different pretreatments is presented in Figure 4. The Ga 3d spectra, on the left column of Figure 4, can be fitted with four doublets, and they are bulk doublet (blue) and three types of oxide states with energy shift of +0.43 eV (green), +1.24 eV (red) and +1.9 eV (grey), respectively, related to the Ga-Sb peak. The First oxide state of 0.43 eV shift is considered to be Ga_2O component (Ga^+) while the second oxide state of 1.24 eV is dominated by Ga_2O_3 (Ga^{3+}).[24, 25] The third doublet with 1.9 eV shift could be due to a mixed oxide component, for instance, $GaSbO_4$. The spectrum of the substrate after air exposure, as shown in Figure 4 (a), shows less Ga bulk signal compared to etched substrates in Figure 4 (b) and (c), but there is no mixed oxide state. By comparing the amount of a certain oxide state to the bulk contributing, we use a ratio calculated by dividing the oxide area to the bulk area. The HCl:IPA etching reduces the first oxide state (normalized by the bulk amount) from 1.14 to 0.065 while the second oxide state ratio from 4.91 to 2.98. A treatment of BOE 30:1 etching also reduce the first oxide state from 1.14 to 0.14 while the second oxide state ratio increase from 4.91 to 5.53. The ratio of mixed oxide state is gained to 0.69 by HCl:IPA and 0.31 by BOE etching.

On the right column of Figure 4, the Sb 4d spectra can also be fitted with four doublets, bulk (blue), +0.36 eV (yellow), +2.42 eV (green) and +3.07 eV (grey), respectively. The state of 0.36 eV higher energy shift is assumed to be metallic Sb, which also can be considered to form during the oxidation process.[26] The state of +2.42 eV is attributing by

Sb_2O_3 while the doublet with 3.07 eV higher energy shift could be Sb_2O_5. The spectrum of the substrate after air exposure, as shown in Figure 4 (d), shows much more Sb_2O_3 than the others. Similarly, no contribution from the highest energy shift states. Table 1 summarizes different types of fitted peak to bulk ratio in two cases. The HCl:IPA etching reduces the metallic state ratio from 0.290 to 0.221 while the ratio of Sb_2O_3 to bulk from 2.194 to 0.850. A treatment of BOE 1:30 etching also reduce the metallic state from 0.290 to 0.258 while the Sb_2O_3 state ratio from 2.194 to 1.136. The ratio of m Sb_2O_5 state is gained to 0.38 by HCl:IPA and 0.20 by BOE etching.

The total amount of oxides dropped after both of the etching treatments, and HCl:IPA solution gives cleaner surface than the BOE 30:1. It is worth mentioning that the metallic Sb could influence the electrical performance more, since it can probably lead to current leakage according to previous study.[27] In general, we see that the total amounts of oxides are reduced considerably. In those treatments, HCl:IPA removes more oxides than BOE 30:1, but more states with the highest energy shift on both Ga (mixed oxide state) and Sb (Sb_2O_5).

2.4. Electrical characterizations with Statistical comparison

Figure 5(a) compares the transfer characteristics of two samples digital etched by BOE 30:1 and HCl:IPA, respectively. We believe that the difference in L_g between two samples can be negligible since one can consider both samples as long-channel device without any short-channel effects, which almost excludes the impact of gate length scaling on transfer characteristics. Therefore, the performances in two samples are reasonably comparable. Although the on-current (I_{on}) with a value of ~25 μA/μm is found at V_{DS} = – 0.5 V in both devices with different channel pretreatments, the off-current (I_{off}) in HCl:IPA pretreated sample is about 5 times lower than that in BOE 30:1 pretreated sample. Thus, I_{on}/I_{off} = 5500 obtained in the sample with DE in HCl:IPA is also 5 times greater than that in the case of BOE 30:1. Furthermore, a lower SS_{min} of 113 mV/dec is achieved in the sample with DE in

HCl:IPA than that of BOE 30:1 pretreated sample with SS_{min} = 160 mV/dec. It is found that I_D drops at high gate bias in the device with DE in HCl:IPA probably due to the presence of the source depletion which can originate from high efficiency of gate modulation in long InAs NW segment as source at high V_{GS} after surface passivation during DE. However, no source depletion is observed in the device with DE in BOE 30:1 since the InAs segment is comparably short while ~200-nm long InAs exists in the sample with DE in HCl:IPA, thereby leading to visible depletion effect (see SEM pictures and output characteristics of two samples in Supporting Information Figure S2).

Figure 5(b) shows the multiple statistics including peak transconductance ($g_{m,peak}$), SS_{min} and I_{on}/I_{off} of two samples based on about 10 devices. Similar as the individual device comparison in two cases, the on-state performance exhibits high consistence in two samples whereas improved off-state performance exists in the sample pretreated in HCl:IPA, resulting in a higher I_{on}/I_{off} and smaller SS_{min} on average, which can be mainly determined by lower D_{it} of the channel and high-κ. In accordance with the equation:[28] $SS \approx (kT/q) \cdot \ln(10)(1 + qD_{it}/C_{ox})$, where k is the Boltzmann constant, T the temperature, q the electron charge and C_{ox} the capacitance of the high-κ oxides which can be assumed as a constant in two samples due to the identical gate stacks and similar channel diameter. Therefore, it is reasonable to directly estimate the D_{it} difference by comparing the statistical result of SS_{min}. In contrast with the sample digital etched in BOE 30:1, the HCl:IPA pretreated sample has approximately 18% reduction in the median value of SS_{min} at V_{DS} = – 0.05 V, leading to a drop in D_{it} by 18% as well. In the case of the individual device in two samples with similar on-performance as shown in Figure 5(a), the difference in D_{it} between two devices, however, reaches ~30%. The worse MOS interface in the sample with DE in BOE 30:1 likely originates from the reoxidation of the GaSb channel surface in water-based BOE[9] either during etch step or the following rinse (in DI water) step. Nevertheless, the variation in performance among devices is lower in the case of BOE 30:1 than that with DE in HCl:IPA, probably attributed to higher

uniformity of NW diameter after DE in BOE 30:1 even for 2 cycles as shown in Figure 3. Despite the presence of potential reoxidation process when using BOE 30:1 as the DE acid for GaSb, the deterioration of the interface is insignificant when comparing the statistical results. On the other hand, BOE pretreatment process for III-Sb based devices is compatible to current industrial Si process, which enables the monolithic integration of III-V on Si by using the same chemical selection.

Finally, the benchmarking to the start-of-the-art III-Sb p-type MOSFETs with various device structures and channel lengths is demonstrated in Figure 6. Our vertical NW devices with DE in either HCl:IPA or BOE 30:1 show a competitive performance in *SS* and I_{on}/I_{off}, in Figure 6(a) and (b), respectively. It is notable that *SS* in our devices is reduced in comparison with both longer and shorter channel devices, while I_{on}/I_{off} reaches a similar value as long channel devices, which indicates a good off-current. One of the reasons is our vertical NW devices benefit from the GAA architecture that provides great electrostatics for gate modulation. However, when compared to other GAA GaSb MOSFETs or our previous vertical GAA transistors fabricated with different DE techniques and process flow (see Figure 6), devices in this work still performs better. This suggests clearly that the surface pretreatment in this work also plays an important role to further improve the electrostatics of the MOSFETs.

3. Conclusion

We have improved the electrostatics of GaSb p-type MOSFETs by passivating the channel surface by DE with HCl:IPA or BOE 30:1 prior the high-κ deposition, achieving the lowest SS_{min} down to 107 mV/dec as well as an increased I_{on}/I_{off} over 3 order of magnitude. The DE comparison of GaSb NWs shows that HCl:IPA provides slightly higher etch rate while BOE 30:1 gives more uniform diameter of NWs. Although BOE 30:1 pretreated surface results in more oxide states and slightly higher *SS* in the transistors compared to HCl:IPA, the

overall transistor performance with DE in BOE 30:1 is still acceptable. Therefore, BOE 30:1 can still be considered as a good alternative for III-Sb surface passivation when it comes to the situation that is involved in current industrial processing of Si-based CMOS.

4. Experimental Methods

Nanowire epitaxy: Heterostructure InAs-GaSb NWs are grown on Si substrates with 260 nm thick n^{++}-InAs buffer layer, from prepatterned Au gold-dots, by metal-organic vapor-phase epitaxy (MOVPE) via vapor-liquid-solid (VLS) process. The NW growth begins by employing a short Sn-doped InAs stem with precursors of trimethylindium (TMIn) and arsine (AsH_3) (molar fraction: $\chi_{TMIn} = 6.1 \times 10^{-6}$, TESn/TMIn = 4) to provide better nucleation for the subsequent GaSb NW growth where trimethylgallium (TMGa) and trimethylantimony (TMSb) are used as precursors. The non-intentionally doped (nid) GaSb with background doping of ~10^{16} cm^{-3} and Zn-doped p-type GaSb (molar fraction: $\chi_{TMGa} = 4.9 \times 10^{-5}$, DEZn/TMGa = 0.39) are subsequentially grown at 515 °C, providing the channel and drain material respectively.

Device fabrication: The device fabrication is initialized, directly after growth, by digital etching using oxidation in O_2 ambient followed by either HCl:IPA 1:10 or BOE 1:30. Directly after the surface treatment (within seconds) atomic layer deposition (ALD) is performed consisting of a bi-layer high-κ with Al_2O_3/HfO_2 (1/3 nm, EOT ≈ 1 nm) with an added 20-nm-thick Al_2O_3 film. The bottom (first) spacer is finalized by selectively etching the top segment of the 20-nm-thick Al_2O_3 using a back-etched S18 mask and HF 1:400 etch. The gate is then defined by using a 60 nm sputtered W aligned via a similar S18 back-etch mask now followed by dry etching (SF6:Ar) which sets the final gate-length. Both the NW diameter of the channel and the gate length are verified by scanning electron microscopy (SEM) imaging (see Supporting Information Figure S2). The samples are finalized by second spacer deposition and contact metallization (Ni/W/Au).

XPS characterization of GsSb: The synchrotron-based X-ray photoelectron spectroscopy (XPS) is ideal for investigating semiconductor-oxide interfaces and surfaces, and the data are acquired at FlexPES of MAX IV, Sweden. The Ga 3d spectra are measured with photon energy 320 eV while Sb 4d are measured with 340 eV, in order to keep the kinetic energy at a same level, i.e., similar penetrating depth from the surface. The native oxidized sample is the same growth sample as described above, while both the BOE 30:1 and HCl:IPA etching followed by ALD samples are processed on GaSb (100) substrate since it is challenging to probe at the NW sidewall surface to during XPS measurements. Here, it is needed to mention that the surface (110) and (100) have very similar behaviors including surface oxidation and D_{it} in one of the III-V family, InAs.[29] Therefore, it is reasonable to only compare the results of the GaSb (100) surface instead of (110) which refers to the NW sidewalls.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

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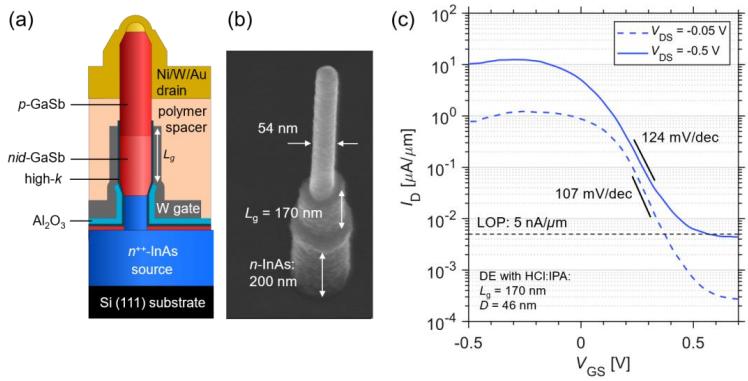

Figure 1. Electrical characterization of the device with lowest *SS*. (a) Schematic of a single GaSb NW MOSFET with digital etch as the first step of the fabrication. (b) SEM image of a single NW device after gate length definition. The measured diameter includes the NW and gate oxides. (c) Transfer characteristics of the NW device with 2-cycle DE in HCl:IPA 1:10 just before high-*k* deposition.

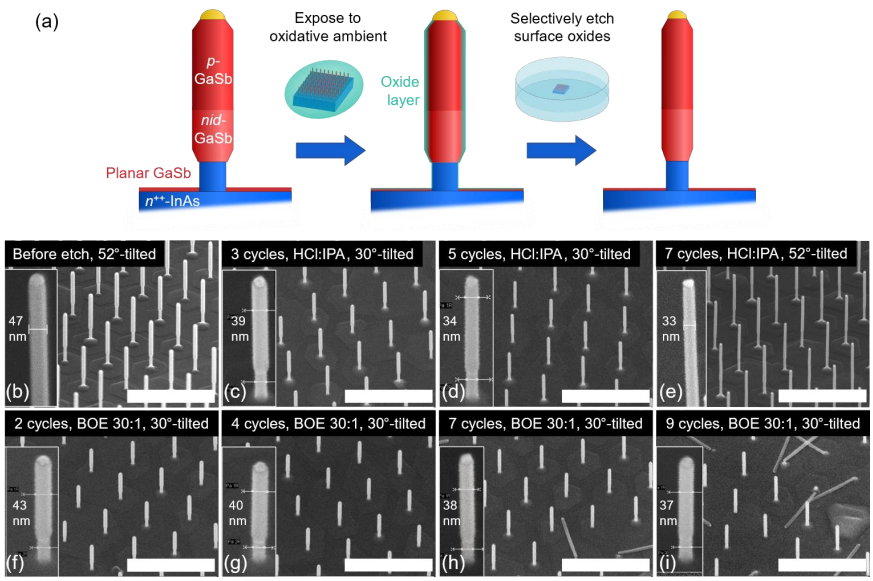

Figure 2. (a) Schematics of 1 cycle digital etch process. Evolution of a GaSb NW array in a sequential etch experiment with different numbers of digital etch cycles in (c-e) HCl:IPA and (f-i) BOE 30:1, respectively. (b) shows the SEM of NWs before digital etch. The insets show a single NW in the array. The scale bars are 1 μm.

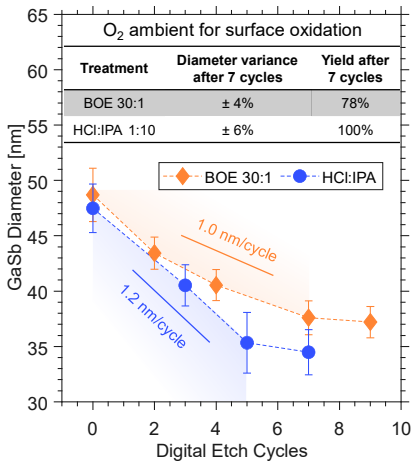

Figure 3. Comparison of GaSb NW diameter with number of digital etch cycles in BOE 30:1 and HCl:IPA. The inset table shows the etch difference in NW diameter variance and yield after 7 cycles between HCl:IPA and BOE 30:1.

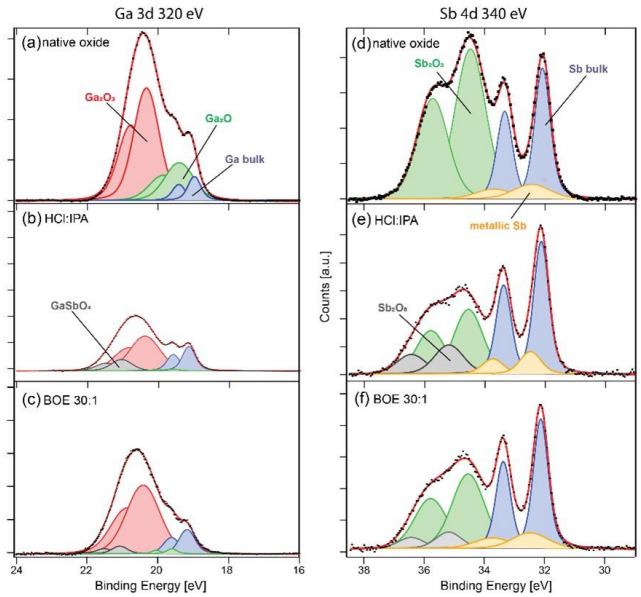

Figure 4. XPS data of Ga 3d and Sb 4d core-shell. (a) Ga 3d spectra of grown substrate after air exposure (b) Ga 3d spectra of grown substrate after HCl:IPA etching followed by ALD (c) Ga 3d spectra of grown substrate after BOE 30:1 etching followed by ALD (d) Sb 4d spectra of grown substrate after air exposure (e) Sb 4d spectra of grown substrate after HCl:IPA etching followed by ALD (f) Sb 4d spectra of grown substrate after BOE 30:1 etching followed by ALD

Table 1. Summary of different types of surface state signal to Ga/Sb bluk ratio.

Ga 3d	Ga_2O / bulk	Ga_2O_3 / bulk	$GaSbO_4$ / bulk
native oxide	1.14	4.91	0
Ga HCl:IPA	0.065	2.983	0.69
Ga BOE 30:1	0.140	5.525	0.31
Sb 4d	**Metallic / bulk**	**Sb_2O_3 / bulk**	**Sb_2O_5 / bulk**
native oxide	0.290	2.194	0
Sb HCl:IPA	0.221	0.850	0.38
Sb BOE 30:1	0.258	1.136	0.20

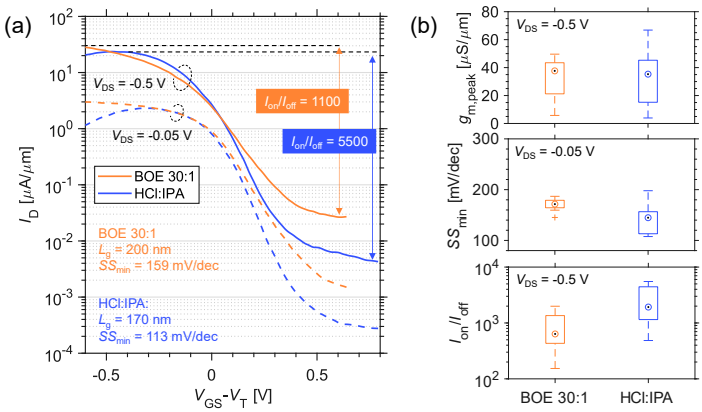

Figure 5. Electrical data of individual GaSb NW p-channel MOSFET in different surface pretreatment. (a) Schematic of the vertical NW MOSFET. (a) Transfer characteristics of the devices with 2-type different DE process for the channel. I_{on} and I_{off} are taken from the maximum and minimum I_D in the range of given V_{GS}, respectively. Here an overdrive voltage $V_{GS} - V_T$ was selected to compare the transfer characteristics in two cases. (b) Statistical result with boxplots including $g_{m,peak}$ SS_{min} and I_{on}/I_{off} based on 10 devices. SS_{min} is taken from the minimum point SS at V_{DS} = – 0.05 V.

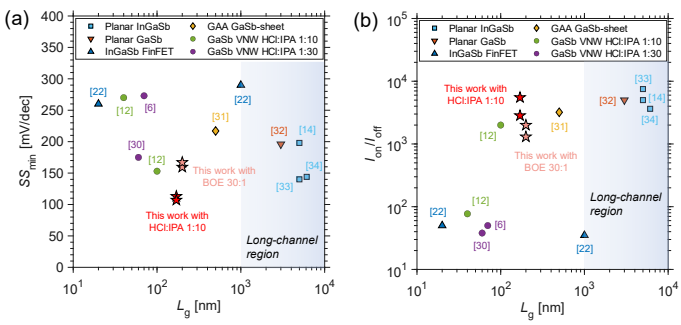

Figure 6. Benchmarking of our devices against to other III-Sb devices in (a) SS_{min} vs. L_g and (b) I_{on}/I_{off} vs. L_g.

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