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Integration of ferroelectric $Hf_xZr_{1-x}O_2$ on Vertical III-V Nanowire Gate-all-around FETs on Silicon

Anton E. O. Persson, Zhongyunshen Zhu, Robin Athle, and Lars-Erik Wernersson

***Abstract*—We demonstrate a successful process scheme for the integration of a CMOS-compatible ferroelectric gate stack on a scaled vertical InAs nanowire gate-all-around MOSFET on silicon. The devices show promising device characteristics with nanosecond write time and large memory window of >1.5 V. In the current implementation, the device performance is mainly limited by access resistance, which is attributed to the thermal sensitivity of InAs. The findings indicate that the ferroelectricity is not intrinsically preventing future improvements of scaled III-V FeFETs.**

***Index Terms*—Ferroelectrics, Ferroelectric field effect transistor (FeFET), gate-all-around MOSFET, hafnium zirconium oxide, InAs, vertical nanowire.**

I. Introduction

Ferroelectric MOSFETs (FeFETs) have been extensively studied on Si and Ge platforms and show great promise especially for non-volatile memories and neuromorphic applications [1], but are also expected to be used in high-frequency applications [2]. The integration of ferroelectric high-κ in the gate stack introduces new functionalities but does not otherwise change the technology's advantages and drawbacks regarding scalability and performance. III-V materials are promising candidates to complement Si and to extend Moore's law thanks to their exceptional electron transport properties [3] that have enabled performance improvement in transconductance [4] and low-power applications [5]. However, contrary to the Si and Ge platforms where high-temperature annealing often is used for dopant activation or high-κ defect reduction, the thermal budget of III–Vs is stricter [6][7]. It is important to explore strategies for the implementation of HfO_2-based ferroelectric gate-stacks also on the III-V technology platform as the technology is not directly transferable due to the annealing step.

Initial results indicate that it is possible to integrate ferroelectric high-κ on III-V using $Hf_xZr_{1-x}O_2$ (HZO) that has a low crystallization temperature [8]. However, those results were obtained on large planar capacitor structures [9] or micrometer scale planar transistors [10][11] and might therefore not be transferable to considerably more scaled dimensions or other geometries. In this work, we present a process flow for a scaled vertical InAs gate-all-around nanowire FeFET on silicon that demonstrates promising device characteristics. InAs is a suitable case material as it is both one of the most thermally sensitive III–V semiconductors[6] and used in high-performance MOSFETs[4]. The gate-all-around architecture enables the ultimate scaling for gate control [12] and important for FeFETs, vertical nanowires decouple contact- and channel-length from the footprint. Since FeFETs transition from digital to analog (multibit) switching with increasing gate length [13], the vertical geometry enables analog switching even at scaled nodes. Vertical integration further supports future technology generations with 3D integration allowing higher integration densities.

II. Device Fabrication

A schematic of the VNW-FeFET together with a summarized process flow is shown in Fig. 1a. Using Metalorganic Vapor Phase Epitaxy (MOVPE), a 300-nm-thick n^{++}-InAs buffer layer was grown on a p-type Si(111) substrate. Gold seed particles were patterned using electron beam lithography (EBL), which were used to grow vertical InAs nanowires by Vapor-Liquid-Solid (VLS) growth in MOVPE at 570 °C. The transistor channel consists of 200-nm non-intentionally doped (nid) InAs followed by a 300-nm-long n^{++}-drain InAs segment at the top. The core of the nanowire has a diameter of 30 nm and during the growth of the highly doped top segment, a 3-nm-thick highly doped shell overgrows the channel region.

The first step in the transistor fabrication was to thin the nanowire by cyclic ozone oxidation and HCl etching to

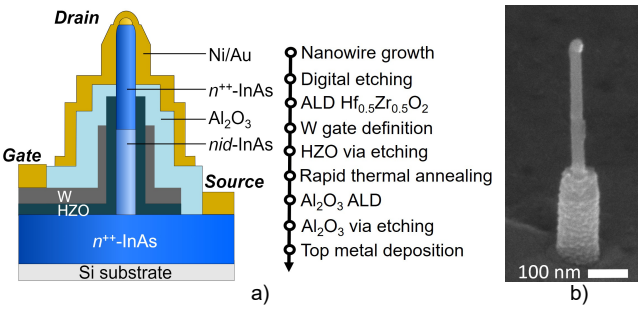

Fig. 1. (a) Schematic and process flow of the devices and (b) SEM micrograph of the structure after the rapid thermal annealing step.

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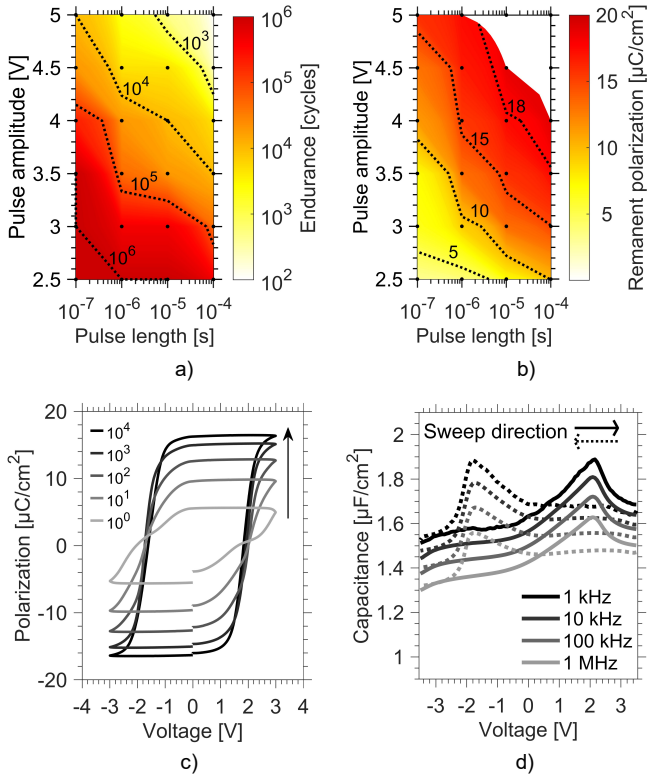

Fig. 2. Measurements performed on planar capacitors identical to the gate structure but without the nanowire. (a) Endurance as a function of voltage and pulse time. (b) Remanent polarization after 1000 cycles of wake up as a function of voltage and pulse time. The white upper right corner indicates a hard breakdown before 1000 wake-up cycles. (c) PE curve after wake up applying 5 V with 100 ns pulses from 1 to 10^4 cycles. (d) Capacitance voltage characteristics.

remove the highly doped shell at the channel region. After the desired channel thickness was achieved, 12 nm HZO was deposited at 200 °C using a thermal Atomic Layer Deposition (ALD) reactor with a 1:1 alternation between the precursors TDMAHf and TEMAZr using water as the oxygen source. A 50 nm W gate metal was sputtered and patterned using UV-lithography S1813 masks and reactive ion etch (RIE). Vias through the HZO were BOE etched using S1813 masks. The sample was annealed at 550 °C for 30 s in N_2 atmosphere in a rapid thermal anneal (RTA) to crystallize the HZO into the ferroelectric orthorhombic phase. In Fig. 1b, a SEM micrograph shows the structure at this stage. 30 nm of ALD grown Al_2O_3 was subsequently deposited as a top spacer and vias were once again patterned by S1813 masks and BOE wet etching. The device was finally contacted by sputtering 10 nm Ni and 200 nm Au that was patterned using S1813 and wet etched by Au and Ni etchants.

III. ELECTRICAL CHARACTERIZATION

Electrical characterization was performed in a MPI TS2000-SE probe station using a Keysight B1500A Parameter Analyzer. To enable pulsed measurements, a B1530A waveform generator module was used and for current-voltage measurements, high-resolution SMUs coupled with E5288A Atto-sense units were used. Capacitance-voltage measurements were performed in a Lake Shore CRX-4K

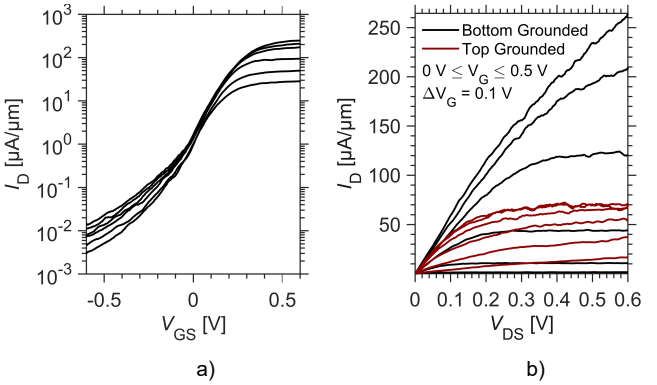

Fig. 3. (a) Transfer characteristic of bottom grounded transistor before pulsing showing V_{DS}=100-500 mV in steps of 100 mV and V_{DS}=50 mV. (b) Output characteristic of the same transistor before pulsing showing V_{GS}=0-500 mV in steps of 100 mV. Black indicates bottom grounded and red top grounded.

cryogenic probe station using an Agilent 4294A Impedance Analyzer.

Initially, on-chip MOS devices identical to the transistor gate structure but without the nanowire were investigated using square pulses with pulse lengths and amplitudes as described in Fig. 2a-b. The data follow the reported trends from Si- and metal-technologies, i.e., degraded endurance and higher polarization for longer pulses with high voltage [14]. All pulsing conditions generate some wake-up of the film compared to only applying the read-out PUND sequence. In Fig. 2c, the evolution of the ferroelectric hysteresis loop for 5V, 100 ns wake up pulses shows a remanent polarization of 17 μC/cm^2 after 10^4 wake up cycles with a coercive voltage of ~1.7 V. The CV-curves in Fig. 2d show the two peaks that are characteristic of ferroelectricity. The frequency dispersion in accumulation at room temperature is ~3.9%/dec, which is slightly lower than reported values for ferroelectric TiN/HZO/InAs capacitors [15].

In Fig. 3a, the DC transfer characteristics of the initial state before any polarization switching are shown for a transistor with a channel length of 200 nm and diameter of 25 nm. The transistor has an on-current of 230 μA/μm at V_{GS}=0.5 V and V_{DS} = 500 mV, with peak g_m = 0.9 mS/μm. In addition, its subthreshold characteristics including slope (113 mV/dec) and off-state (10 nA/µm) are in line with state-of-the-art gate-first VNW InAs transistors [16][17]. The change in subthreshold swing at negative bias conditions is attributed to a U-shaped trap density with a minimum around the threshold voltage[18]. The output characteristics in Fig. 3b are strongly asymmetric with higher on-state current when the bottom substrate is grounded compared to the top grounded case, which we attribute to a large top contact resistance. [19] As the selected annealing temperature is close to the growth temperature of the nanowires, it is assumed that the RTA is causing the degradation of the top contact as it, contrary to the bottom contact, is not encapsulated by HZO during the annealing. Previous studies indicate a high quality HZO/InAs-interface after annealing at elevated temperatures [15] whereas similar on-state degradation has been seen in RTA studies of VNW III-V MOSFETs already at lower temperatures of 350°C [20].

In the bottom grounded transistor in Fig. 4a, the typical transfer characteristic demonstrating a ferroelectric hysteresis is observed for 5V, 100-ns-square-pulses. Although having lower currents and degraded gate control, a top grounded transistor is apparently having the same memory window as in the bottom grounded case. The required write voltages are further tested in Fig. 4b where the gradual increase in memory window above 3.6V is an indication of partial domain switching, i.e., more than one domain contributes to the ferroelectric properties. The analog rather than digital switching behavior is in line with the properties of similarly sized planar Si-transistors[21]. It is assumed that domains switching on the planar InAs are not contributing to the characteristics due to the high doping and the 300 nm thickness of the buffer layer. The required pulse amplitude for ferroelectric switching at this time scale is in line with planar MIM devices,[22] however, comparing this to a similarly scaled state-of-the-art SiGe VNW-FeFET [23], this InAs FeFET has less than half the write voltage which partly can be explained by the intentional choice of not using an interfacial layer. Fig. 4c shows an endurance of the device of >20000 polarization switches followed by an abrupt HZO breakdown. As seen in Fig. 4a, both the off-state and on-state deteriorates with pulsing, which we attribute to defect generation in the HZO during the ferroelectric switching[24]. To evaluate the potential endurance of these III-V VNW-FeFETs, we in this case define the memory window at 10 μA/μm when DC sweeping V_{GS} from +1 V to -2 V having V_{DS} = 0.5 V. The memory window increases with wake-up and reaches >1.5V with rather stable threshold voltages for both the write and erase pulses after the initial wake-up. As the breakdown occurs at a similar endurance as for the capacitors in Fig. 2a, the properties are not deteriorated by the nanowire transistor channel. Adding a spacer between gate and substrate would shrink the area by five orders of magnitude and as the endurance to hard breakdown is strongly area dependent [25], it is expected that the endurance will increase considerably with this addition. In Fig. 4d, the retention on another device is measured at room temperature by defining the memory window at 1 μA/μm when DC sweeping V_{GS} from +1 V to -2 V keeping V_{DS} = 0.5 V. Given the defect concentrations indicated by the deteriorated off-state of the devices after switching, charge trapping is expected to be the dominating factor for the shrinkage of the memory window rather than depolarization fields.

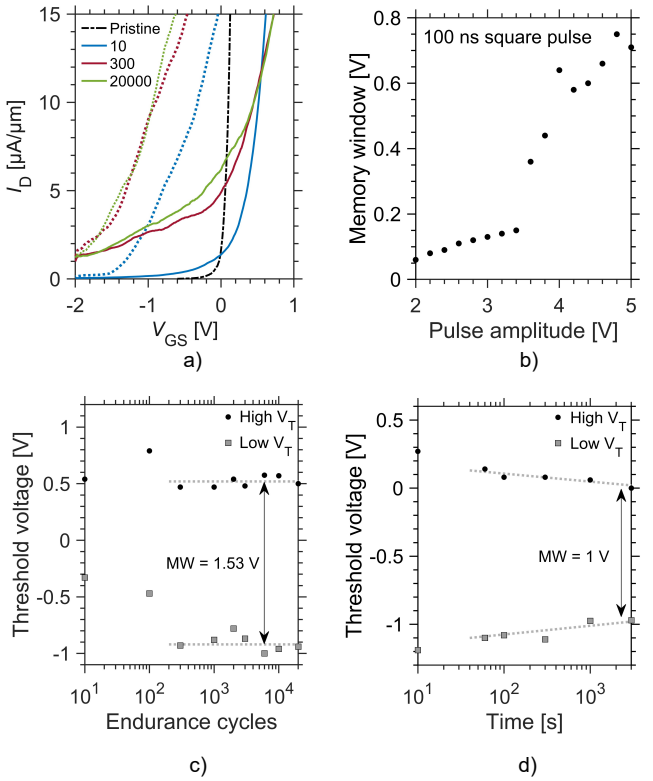

Fig. 4. (a) Transfer characteristic before pulsing (called pristine), in low V_T-state (dotted), and high V_T-state (solid) as a function of wake-up cycles of 5V, 100 ns square pulses. (b) Memory window as a function of pulse amplitude for 100 ns square pulses. (c) Memory window as a function of endurance cycling. Dotted lines serve as guides to the eye. (d) Memory window as a function of retention time. Dotted lines serve as guides to the eye.

To summarize, the performance of these FeFETs is mainly limited by the top-contact resistance and the amount of defects in the high-κ after polarization switching. This is similar to the early reports on VNW III-V MOSFETs [26] and we expect that similar implementations of gate-last processing, interfacial high-κ-layers, less temperature sensitive III-V materials, and especially decreased annealing temperatures will improve the properties also for VNW III-V FeFETs. Based on our findings, we anticipate future VNW III-V FeFET applications to be in line with III-V MOSFETs. RF- and mm-wave applications are prime candidates provided the high on-currents and lower voltage overdrive compared to Si. Exchanging InAs for more advanced heterostructures within the transistor channel with wider bandgaps (e.g., InGaAs) should decrease off-state current leakage[4] and thereby enable memory applications, whereas the inclusion of e.g. GaSb might enable ferroelectric tunnel FETs for reconfigurable sub-60 mv/dec transistors.

IV. CONCLUSION

In this letter, we have successfully demonstrated a process flow for a scaled vertical III-V nanowire gate-all-around FeFET on silicon and show good performance also when using a thermally sensitive material like InAs. We conclude from this proof-of-concept device's performance that it is limited by effects introduced during the annealing step. These issues are thought to be resolvable and thus these results indicate the suitability of ferroelectric high-κ integration on the VNW III–V technology platform, especially for future applications in the RF- and mm-wave domain.

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