



Reusing IEEE 1687-Compatible Instruments and Sub-Networks over a System Bus

Farrokh Ghani Zadegan, Zilin Zhang, Kim Peterse'n and Erik Larsson



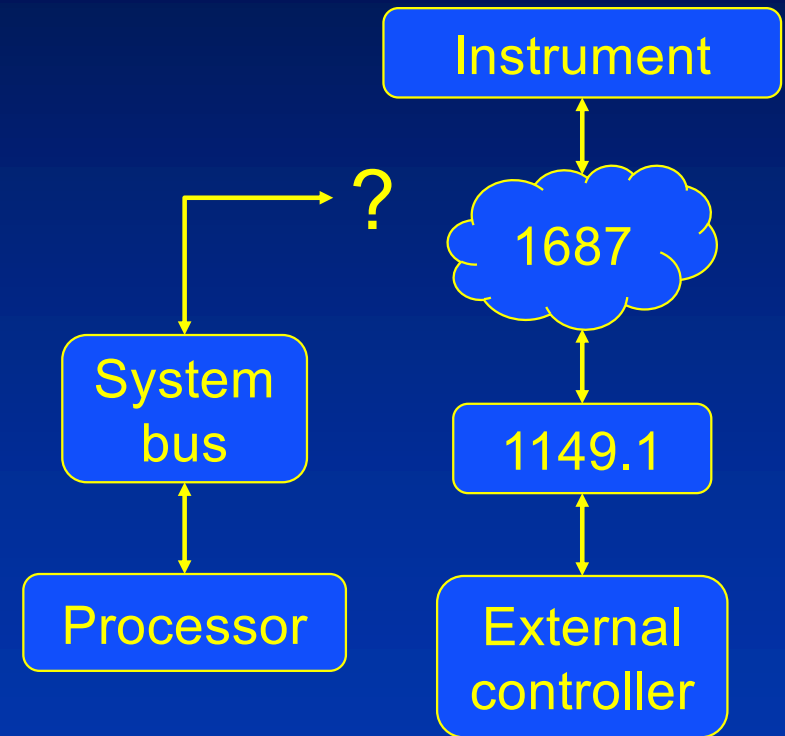
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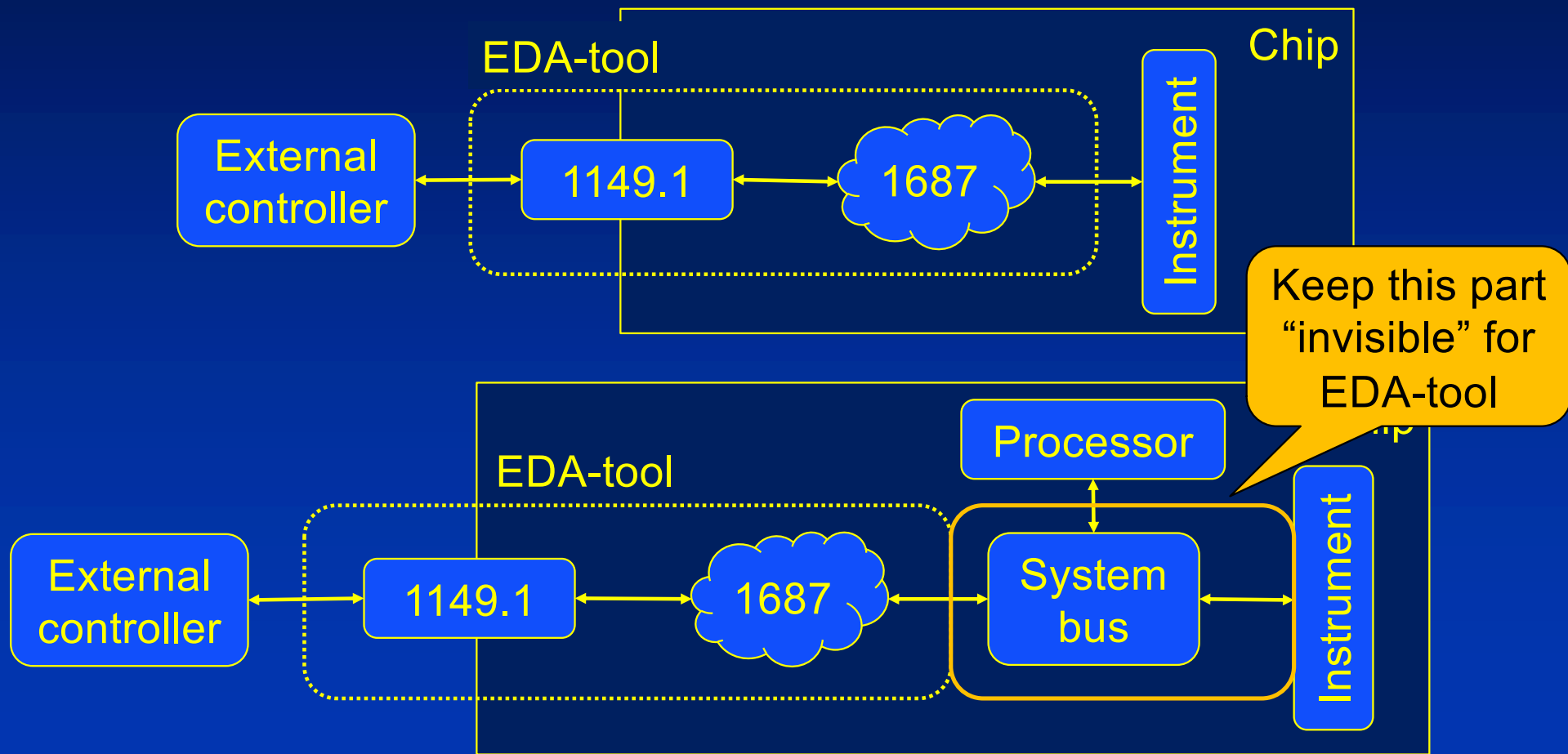
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Purpose

- Modern ICs need on-chip instruments for testing, tuning, configuration, and so on
- Access from an external controller is enabled using IEEE Std. 1149.1 and IEEE Std. 1687
- Desirable to also enable a processor to access instruments via the system bus
- We analyze constraints and demonstrate via an FPGA implementation



Purpose



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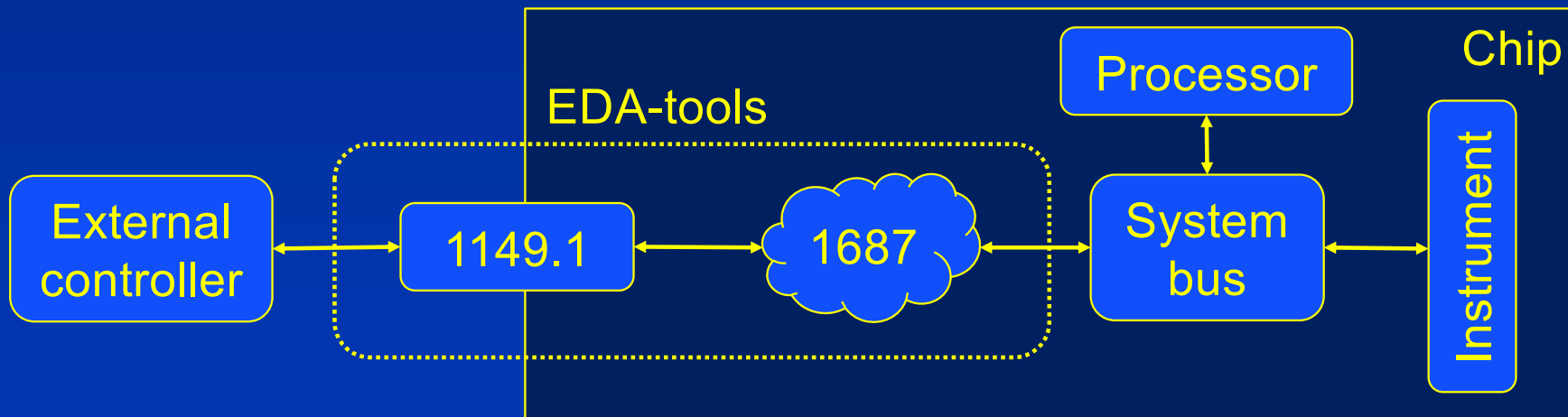
What is needed to avoid modifications?

iWrite Instrument Data;
iApply;

iRead Instrument;
iApply;

iWrite Instrument Data;
iWait xx;
iApply;

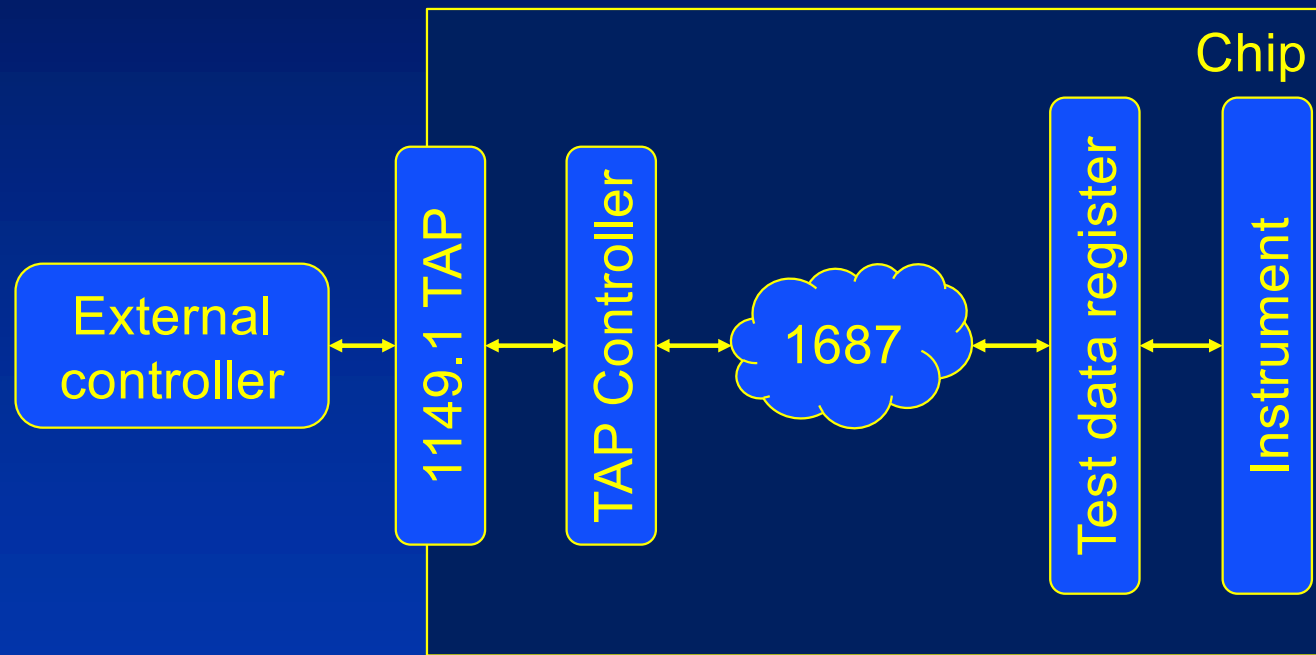
iRead Instrument;
iApply;



Outline

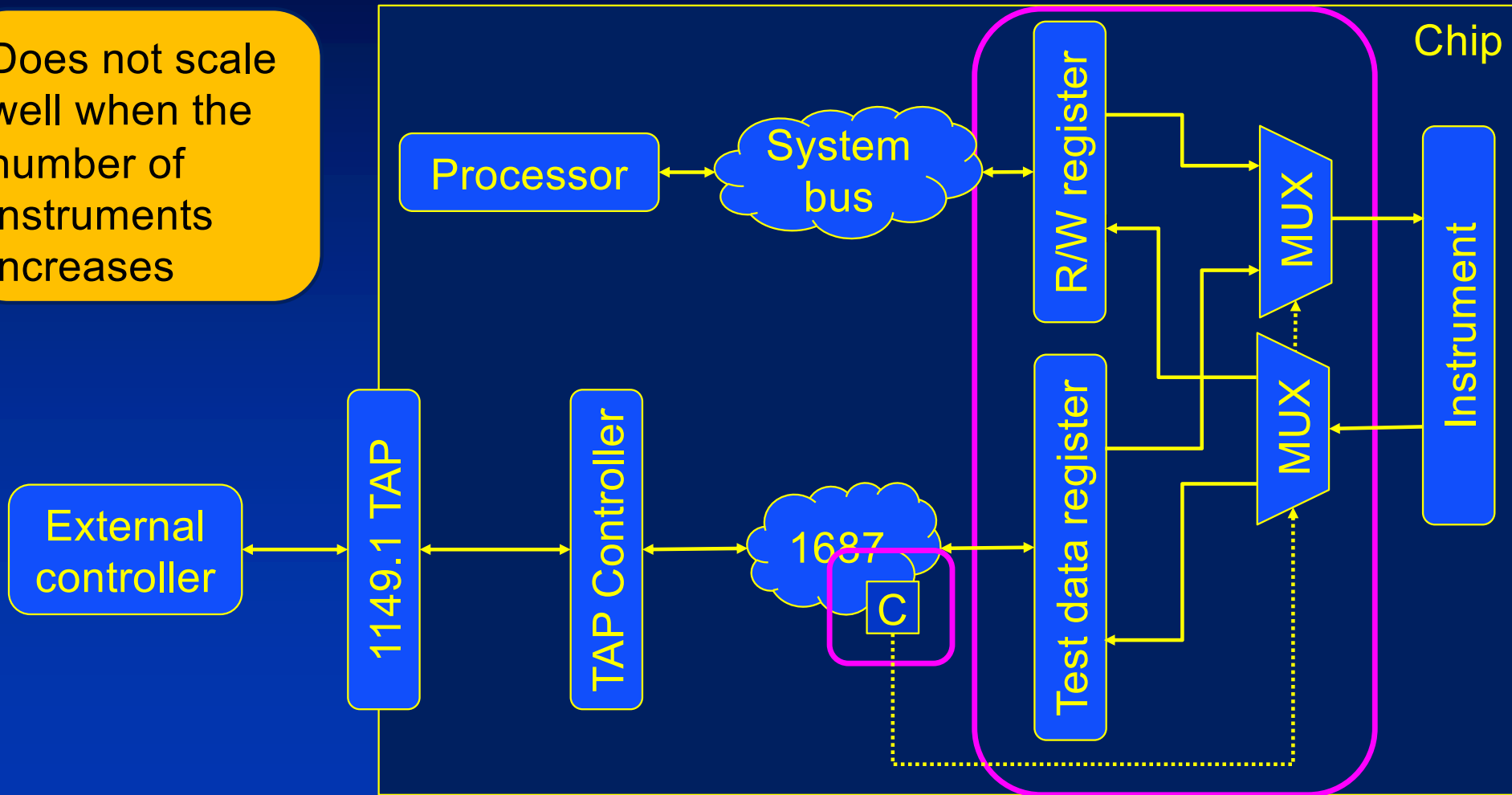
- Architectures
- Organization
- Demonstration
- Conclusions

Standard access

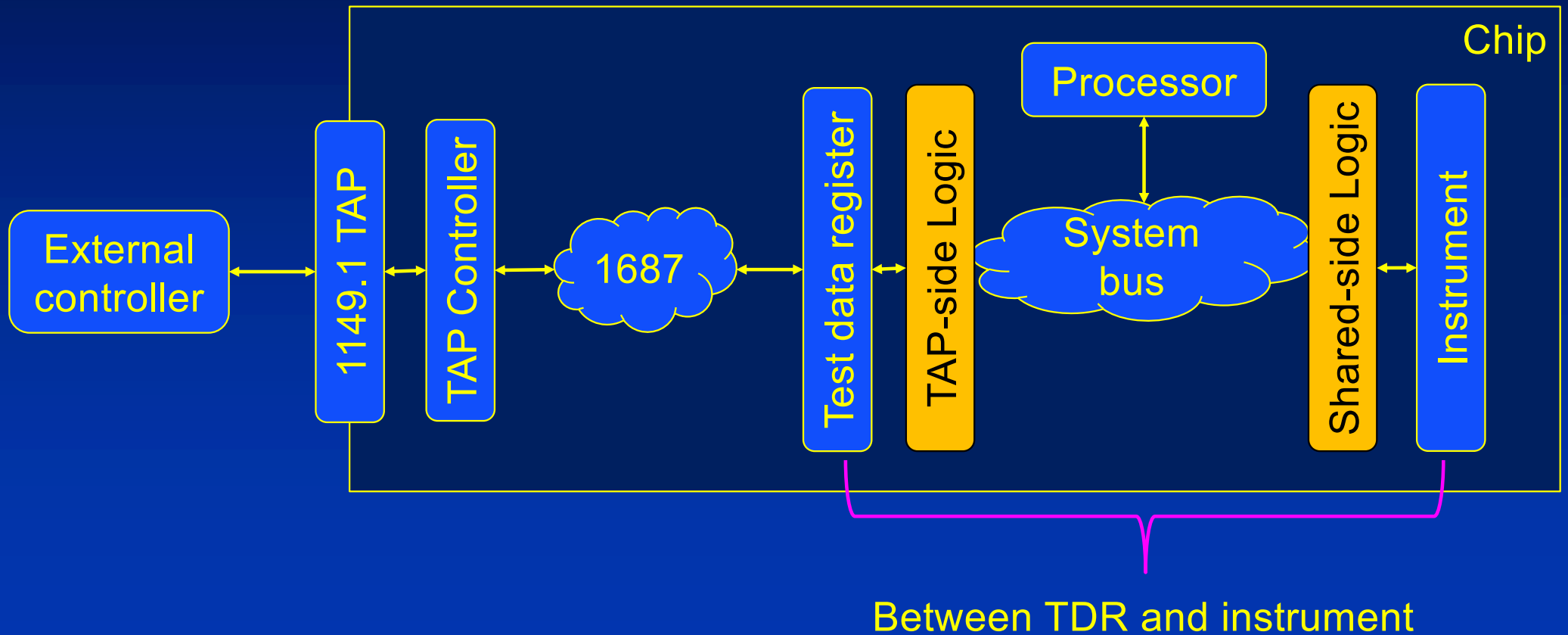


Standard shared access

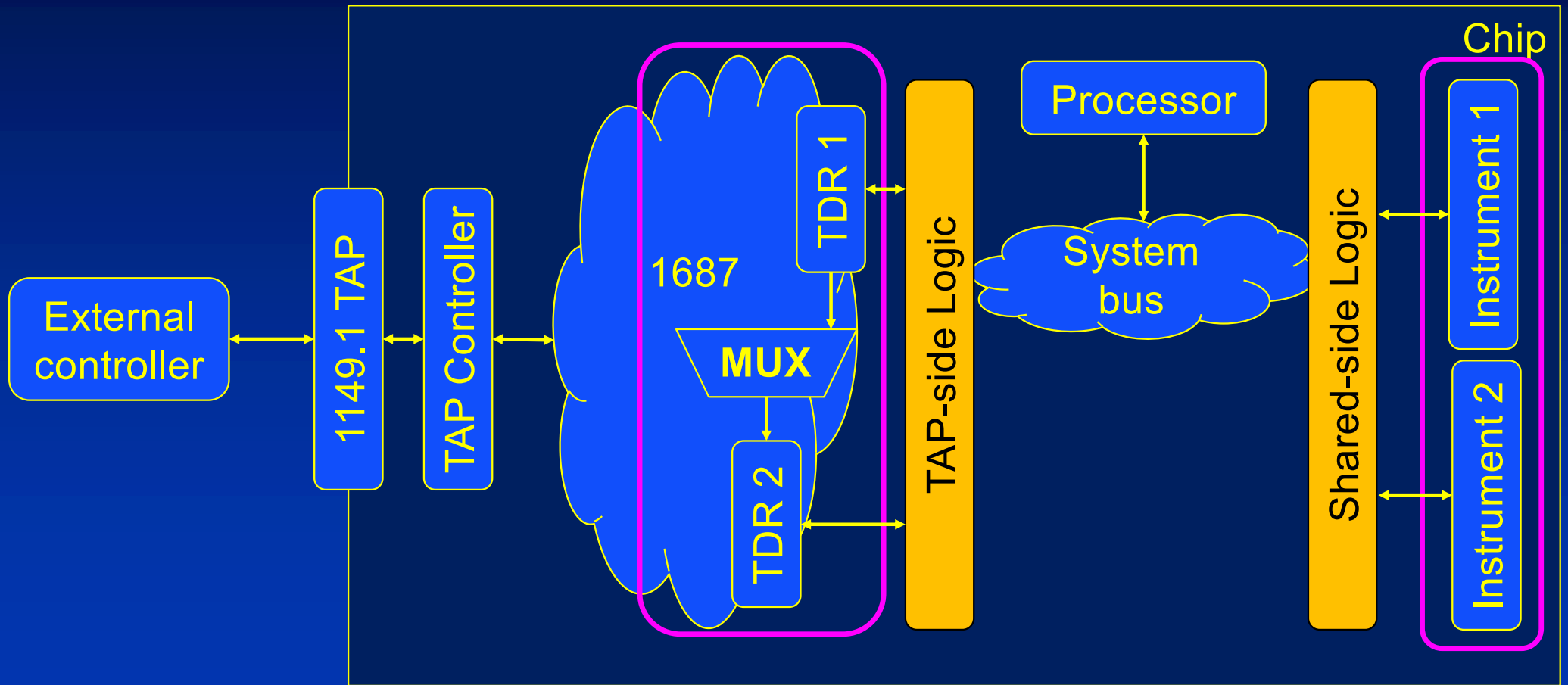
Does not scale well when the number of instruments increases



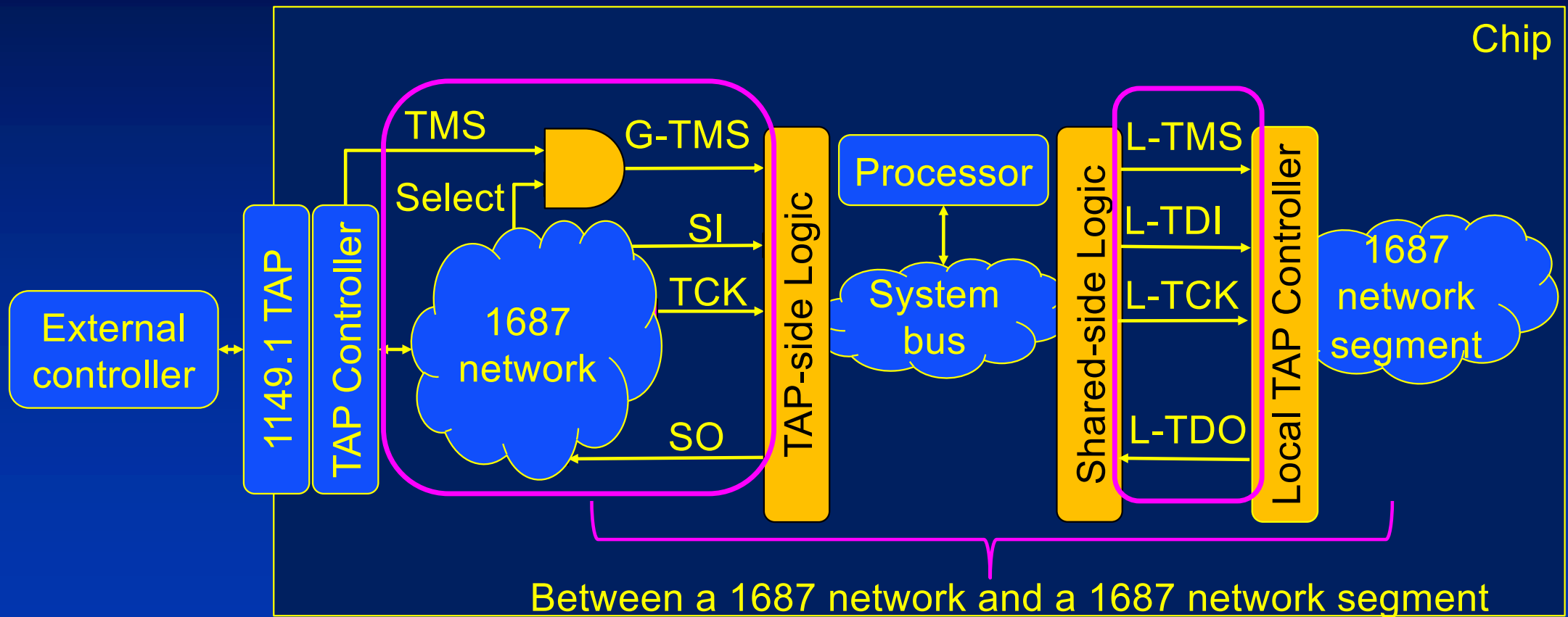
Instrument sharing: Parallel Transfer



Network segment sharing: Parallel Transfer



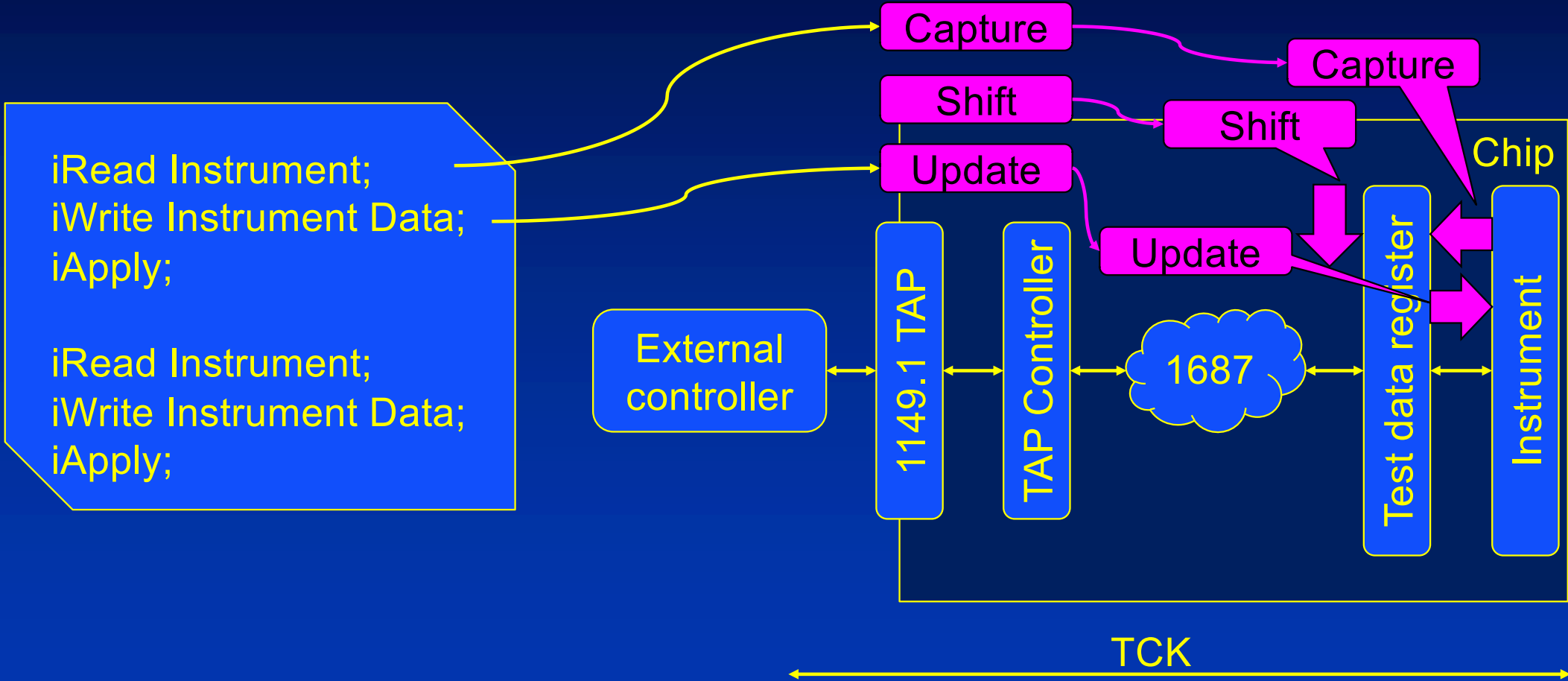
Network segment sharing: Serial Transfer



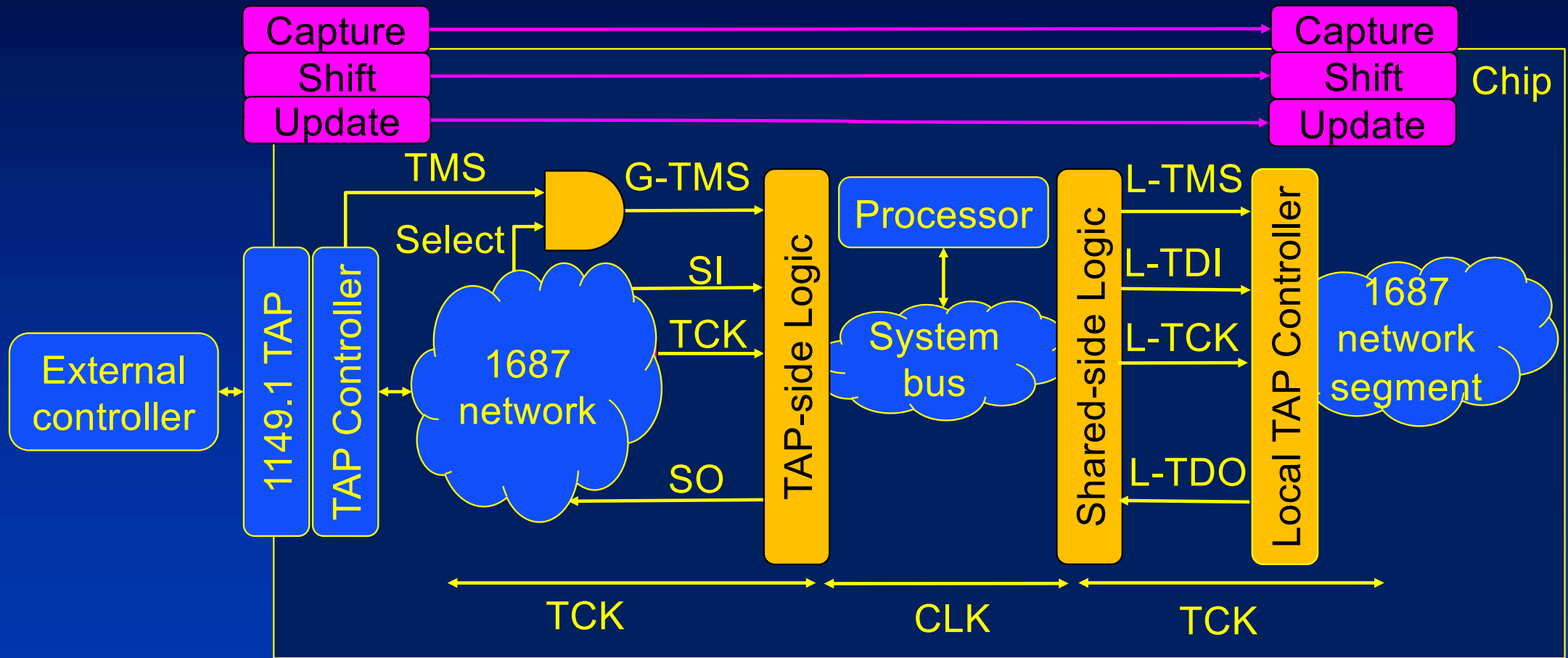
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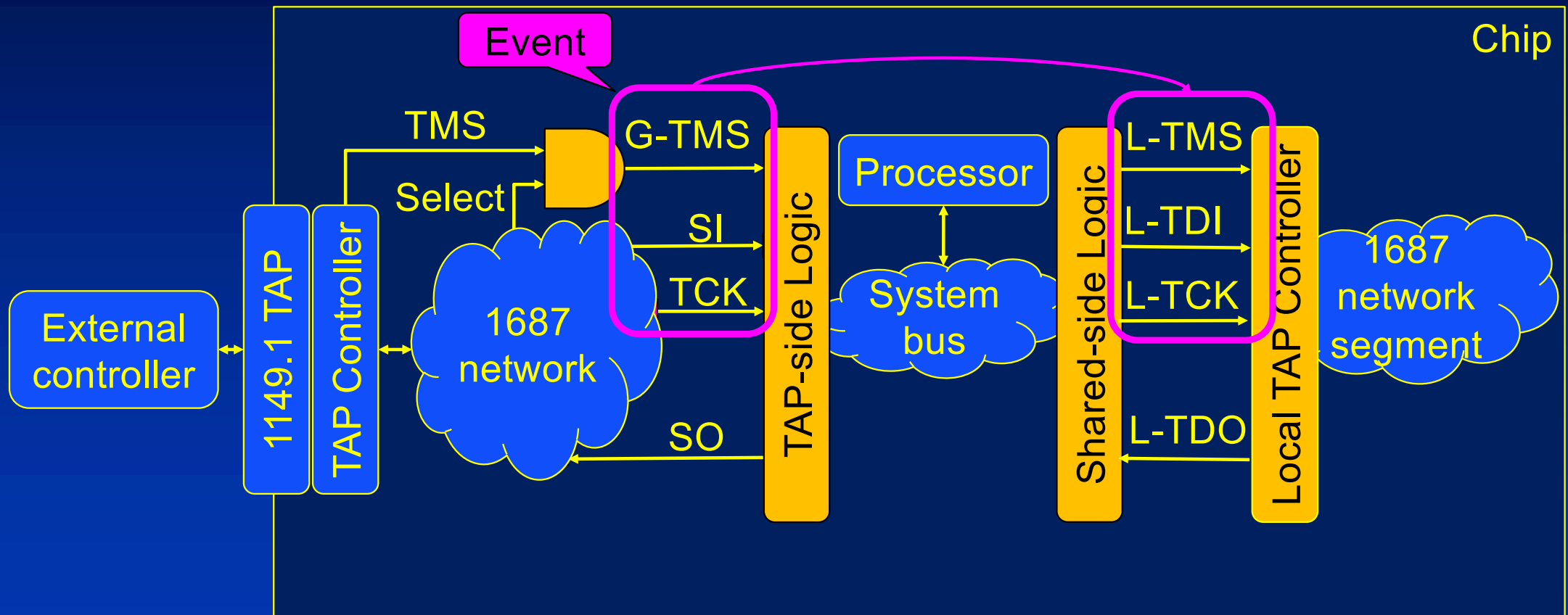
Standard access



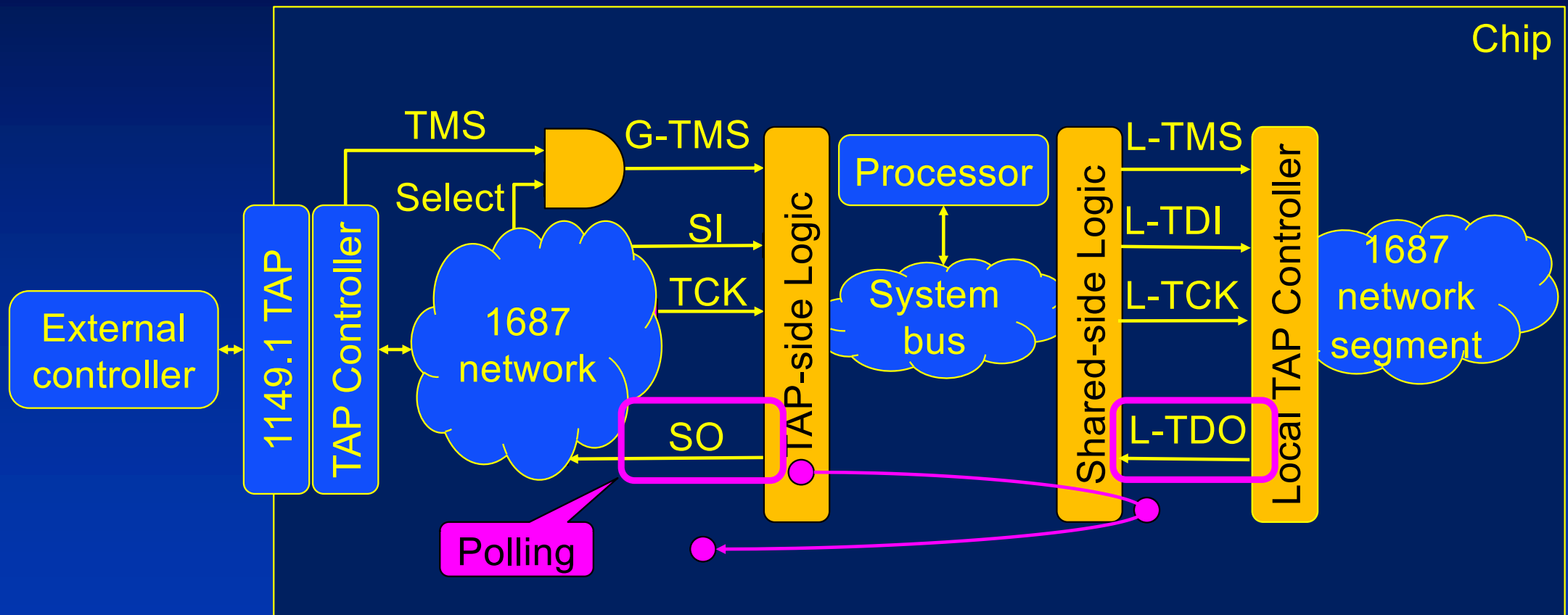
Network segment sharing: Serial Transfer



Network segment sharing: Serial Transfer



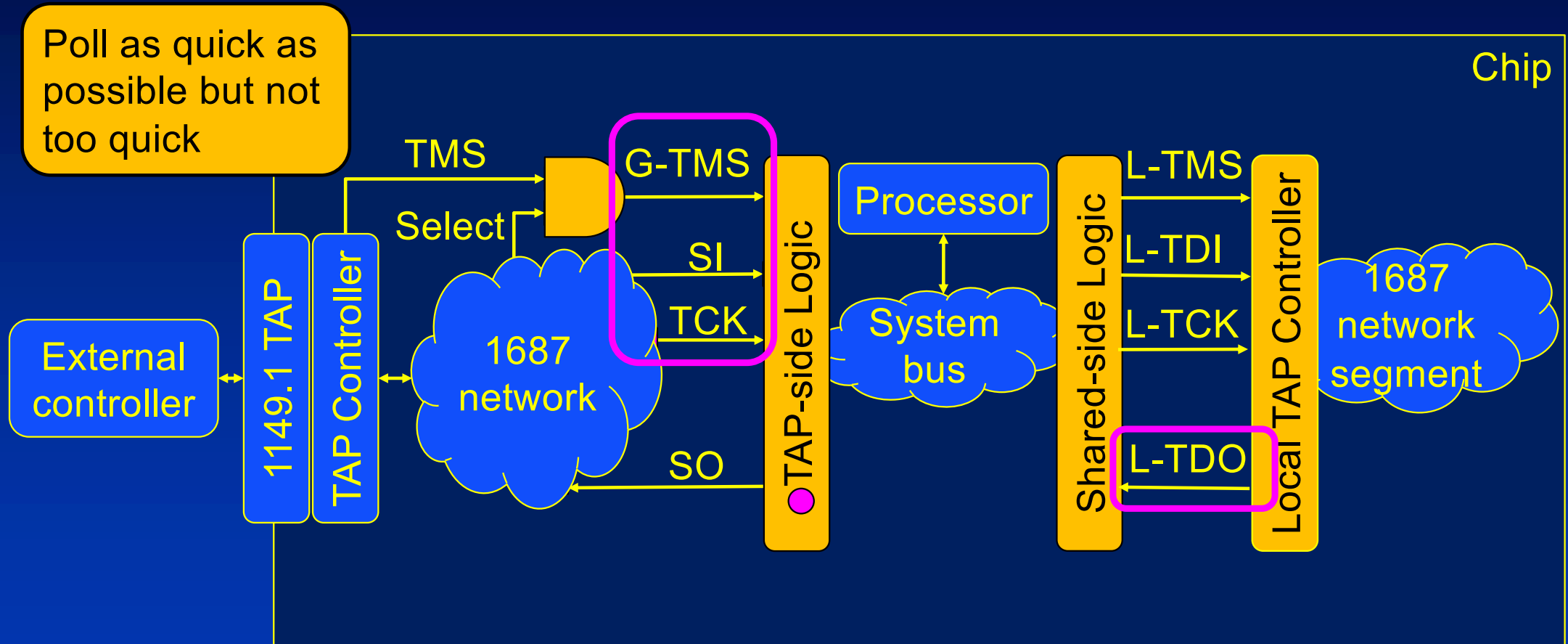
Network segment sharing: Serial Transfer



Network segment sharing: Serial Transfer

Poll as quick as possible but not too quick

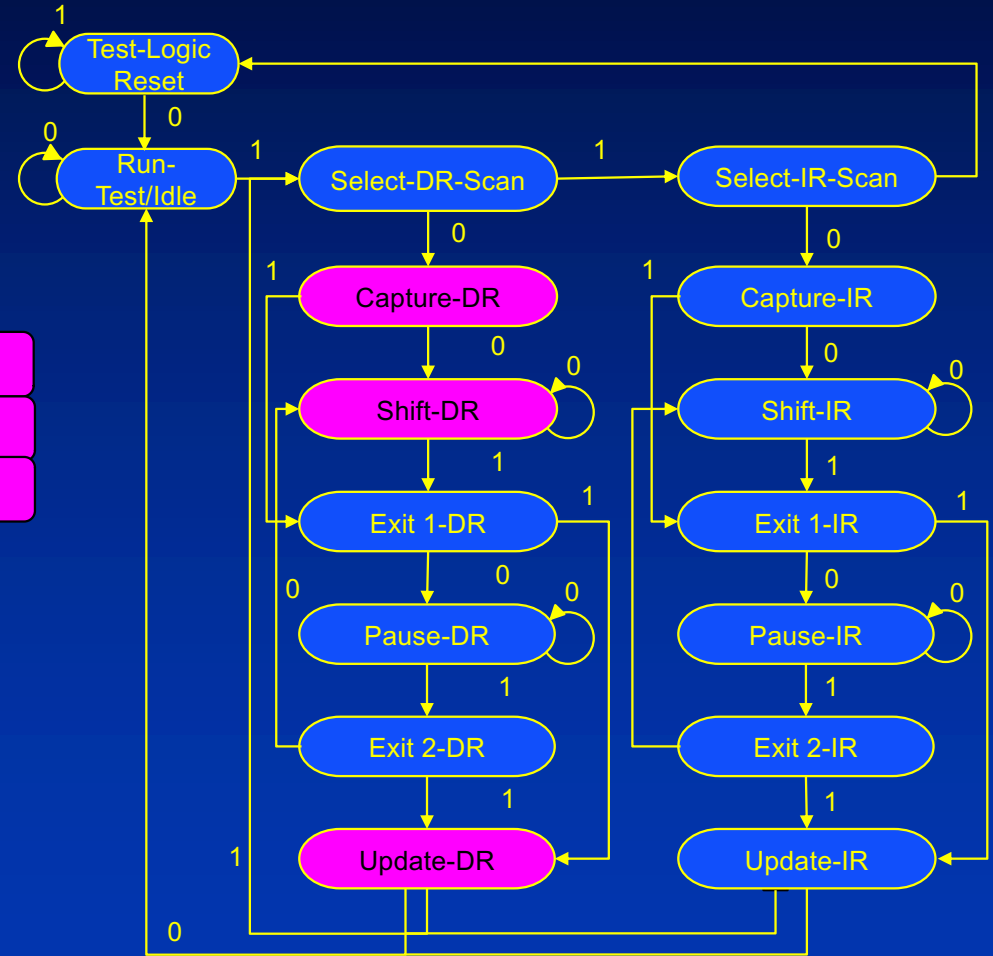
Chip



One iApply group

iRead Instrument;
iWrite Instrument Data;
iApply;

Capture
Shift
Update



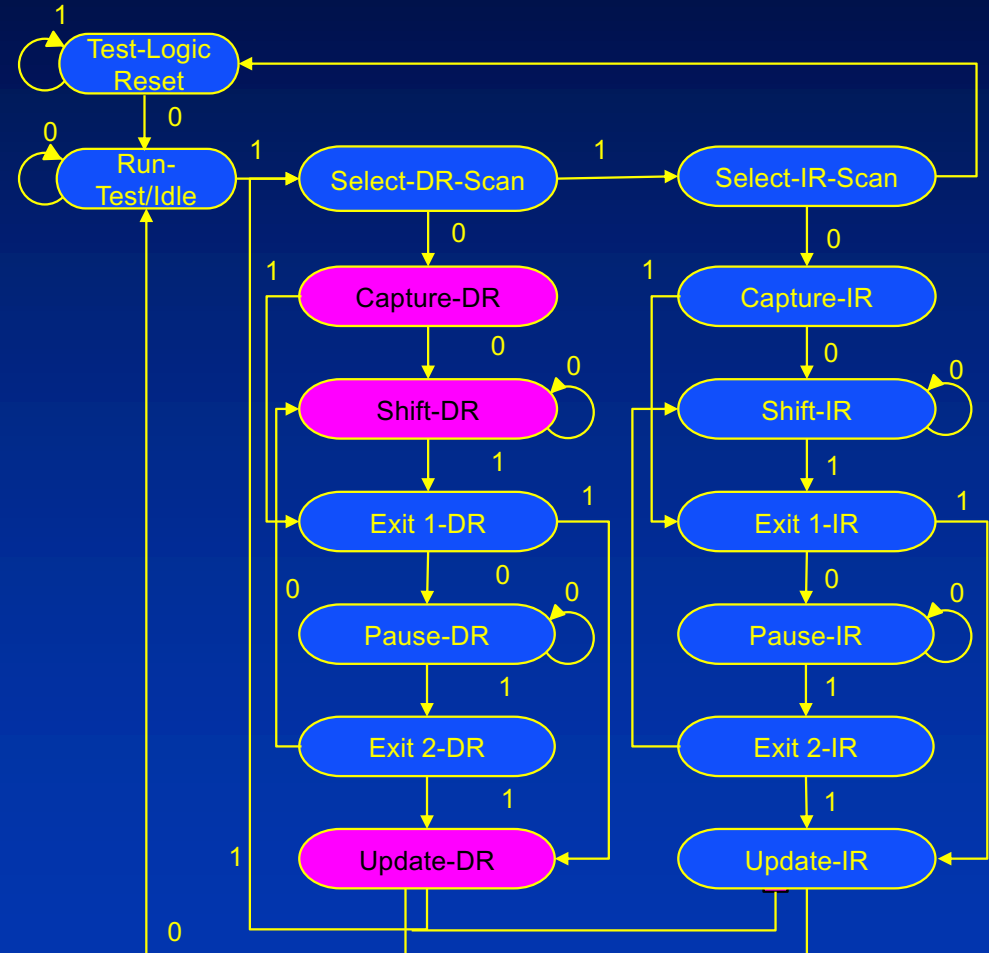
Write Followed by a Read

iWrite Instrument Data;
iApply;

iRead Instrument;
iApply;

Update

Capture

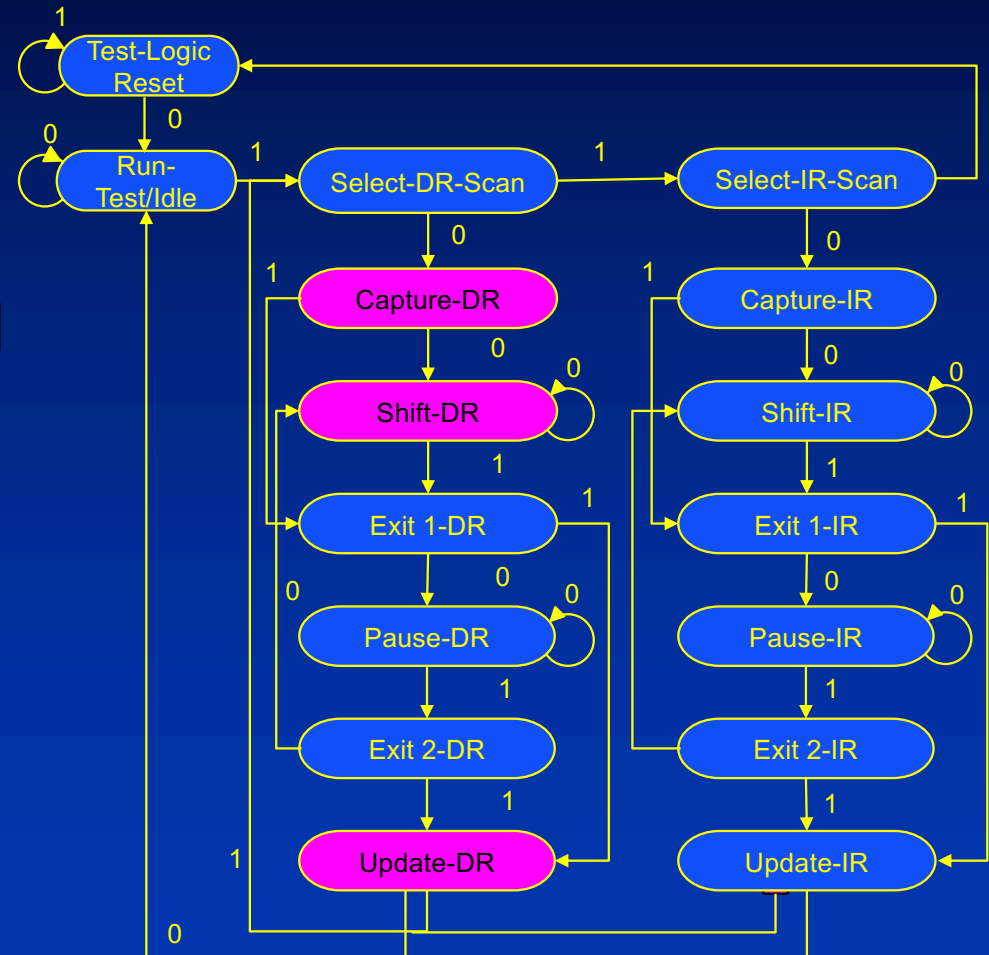


Write Followed by a Write

iWrite Instrument Data;
iApply;

iWrite Instrument Date;
iApply;

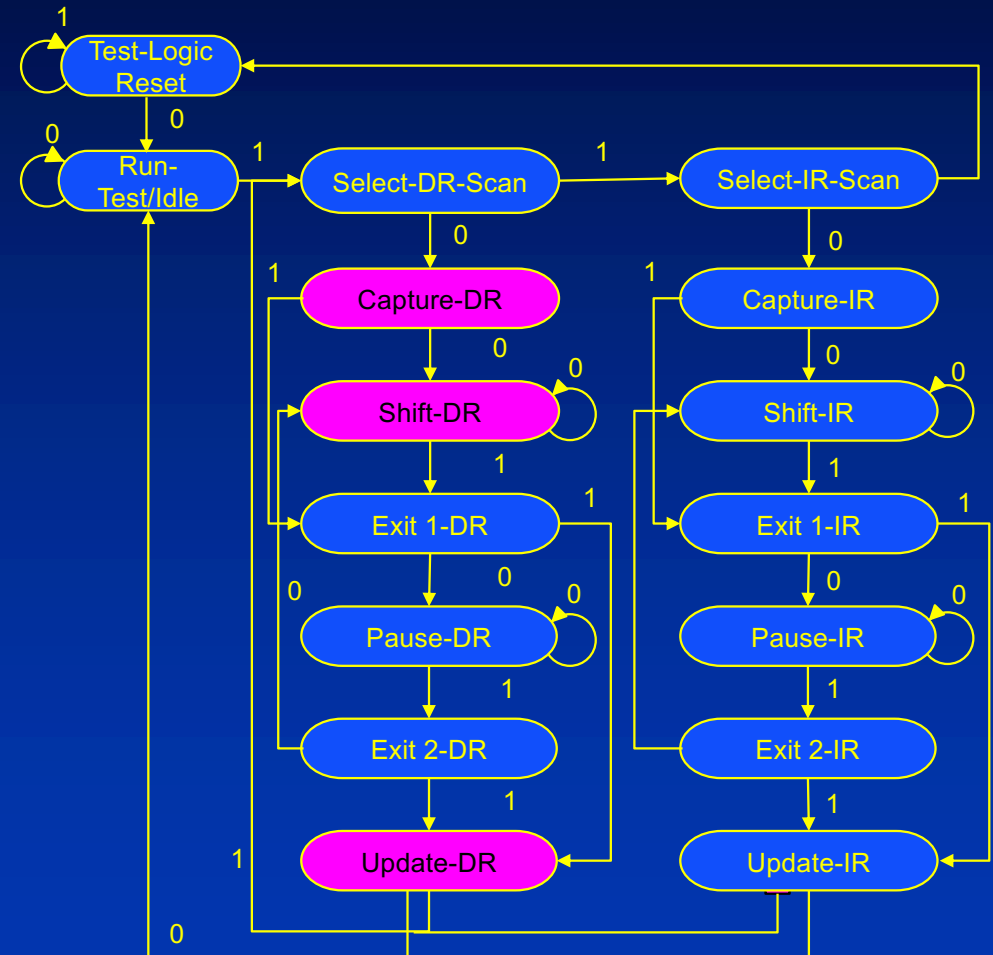
Update
Shift
Update



Cases

- A single iApply group
- Write Followed by a Read
- Write Followed by a Write
- Read Followed by a Read
- Read Followed by a Write

- Need ratio between CLK and TCK, to set TCK



Outline

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Demonstration

- FPGA with an AXI Interconnect as the system bus
- Implemented example with parallel transfer and serial transfer
 - Parallel Transfer leads to $TCK=CLK/20$
 - Serial Transfer leads to $TCK=CLK/78$
- Siemens Tessent IJTAG could use the solution without modifying PDL

Conclusions

- Shown and analyzed two ways to reuse instruments by a processor via system bus during functional operation
- Analyzed constraints to make reuse invisible for EDA-tools so that no modifications of PDL are needed
- Data handling over system bus is event-driven when sending data TO shared instrument and polling-driven when moving data FROM instrument
- Demonstrated via an FPGA implementation that:
 - Parallel Transfer leads to $TCK=CLK/20$
 - Serial Transfer leads to $TCK=CLK/78$



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