Surfaces and interfaces of low dimensional III-V semiconductor devices

YEN-PO LIU
DEPARTMENT OF PHYSICS | FACULTY OF SCIENCE | LUND UNIVERSITY

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Yen-Po Liu

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Surfaces and interfaces of low dimensional III-V semiconductor devices

Abstract
The demand for fast and energy efficient (opto-)electronic applications needs high mobility semiconductor materials, such as InAs with a very high electron mobility and GaSb with a very high hole mobility. Beyond the material itself, also an innovative device geometry is needed, for example, the gate-all-around geometry that provides higher efficiency and electrostatic control for computational units. Vertically or laterally grown nanowires and nanosheets are excellent candidates for realizing such beneficial device geometries. The logic operations and charge transport could be realized in different device architectures, such as the concepts of tunnelFETs instead of classical FETs or new neuromorphic hardware instead of complementary metal-oxide-semiconductor (CMOS).

With both the excellent functional properties of III-V materials and the flexibility of nanostructuring into 1D nanowires and 2D nanosheets, III-V semiconductors could be the stars for next-generation applications. For example, lateral grown $In_xGa_{1-x}As$ nanowires have a high spin-orbit coupling and moderate bandgap promising for quantum computing devices. GaSb nanowires are excellent high-speed p-channels for III-V CMOS, and InAs/InP nanowires have an energy barrier in the axial direction which can be used for photovoltaic and sensor applications. Due to the high surface-to-bulk ratio of nanowires and nanosheets, their surface condition becomes the key to the device performance. In this work, III-V nanowire and nanosheet devices are studied with an emphasis on surfaces and interfaces, using a wide range of characterization methods. The dissertation explores the fabrication of novel nano-devices and the characterization of their surface chemistry, topography, electronic properties, electrical transport and interaction with photons.

The characterization techniques include scanning tunneling microscopy/spectroscopy (STM/S) for atomic level topography and electronic properties. Development of a Scanning gate microscopy (SGM) system with additional single-mode focused lasers for simultaniously probing influence of static and optical fields. Synchrotron based X-ray techniques, mainly X-ray photoelectron spectroscopy (XPS) is used for evaluating surface chemistry. Surface treatment processes, e.g., ultra-high vacuum (UHV) annealing, digital etchants, atomic hydrogen cleaning, and atomic layer deposition (ALD), are applied and the resulting surface chemistry, structure and electronic properties measured. Beyond studying the surface properties, we also investigate the device efficiency and performance down to the nanometer scale. Therefore, we perform measurements to monitor the device while the local gate and/or a focused light interact with the device.

In conclusion, in this thesis the surfaces and interfaces of low-dimensional materials for future device applications are studied using many different characterization methods. It is the hope that the thesis will assist in the progress toward novel devices and improve the energy efficiency and performance of devices. Both the method development and the results give relevant contributions opening for future quantum technologies and (opto)electronics.

Key words
III-V semiconductor, nanowires, nanosheet, nano-device fabrication, STM, AFM, SGM, OBIC, XPS

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Surfaces and interfaces of low dimensional III-V semiconductor devices

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Front cover:
SEM images of vertically grown InAs nanowires (upper, top view), InAs nanosheets (lower, side view), and transferring the nano-materials to pre-patterned electrodes for devices using micro-probe in the SEM chamber.
Back cover:
SEM image of long GaAs NWs.

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Crystals are like people; it is the defects in them which tend to make them interesting!

- Colin Humphreys.

Table of Content

Abstract

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Popular science

In the classic movies, watching people during world war II struggle to send letter or telegram to their family, I realized how much a video call could have helped them. I can still remember how my dad had a huge Motorola mobile phone when I was 5-year old, a manual antenna was a fashion essential. A much simpler way of connecting people is present everywhere nowadays, due to the development and revolution of the semiconductor technology. A self-driving / auto-pilot car was also something hard to imagine when I was young, but it is realistic now thanks to new technologies. The future world will be a new adventure with new ideas everywhere, and we are taking part in it by prototyping new device concepts and novel material applications.

Semiconductor devices, like transistor and memory, are the basic functioning unit for electronic applications. Silicon is so far the most common semiconductor material and has the most developed supply chain, but the III-V semiconductors are the better candidates to high-end applications, for instance, 6G high-frequency communication and quantum computing. Furthermore, a smaller device can scale down the applications and save energies. Low dimensional nano-materials are able to confine the spatial freedom for charge carriers. For example, a one-dimensional material, e.g., nanowire (NW), can limit the electrons moving only forward or backward, which avoids electron collisions during transport that cause heat waste.

Once the device shrinks to a size in nanometer range, the surface to bulk ratio becomes very high. Therefore, the surface starts to influence the material behavior significantly, so the surfaces and interfaces of the low-dimensional material play a critical role to the device performance. In my dissertation, fabricating new type of devices and characterizing the chemical, structural, and electronic properties with synchrotron techniques and scanning probe microscopy (SPM) down to the atomic level is the main goals. This can lead to an improved understanding of the surfaces and interfaces of III-V semiconductor nanowire/nanosheet devices in relation to their function and help improve the nano-devices for a better performance.

Three main achievements of this thesis toward high technology and green future are these: *I.* reporting the surface morphology and electrical properties of the novel 1D III-V semiconductor device down to atomic-scale using STM/S to further solve the

interface difficulty for building quantum devices. *II.* Combined with synchrotron techniques for the surface components and its chemical states on the nanomaterials, we demonstrated the full oxide removal on GaSb NWs and correspondingly improved device performance of vertical GaSb NW MOSFET by surface control. *III.* Energy harvesting devices are extremely important for limiting global warming and instead providing sustainable energy sources. In order to study photovoltaic devices for energetically higher efficiency, we built a high resolution laser combined scanning probe microscopy (SPM) system for studying and engineering the electrical transport properties by coherent laser light and precise local static electrical fields that can be used to study a wide-range photovoltaic devices.

By implementing different advanced characterizing techniques for developing new types of novel III-V nanomaterial devices, efforts in this thesis on the device fabrications and device characterization methods are for higher end technology, lower energy consumption, and a greener environment.

List of Papers

This doctoral thesis is based on the following papers, which will be referred to in the text by their Roman numerals.

I. **Low temperature scanning tunneling microscopy and spectroscopy on laterally grown $In_xGa_{1-x}As$ nanowire devices**
Yen-Po Liu, Lasse Södergren, S Fatemeh Mousavi, Yi Liu, Fredrik Lindelöw, Erik Lind, Rainer Timm, Anders Mikkelsen.
Applied Physics Letters, 117(16), p163101 (2020)

In this paper we present the geometric and electronic surface structures of $In_xGa_{1-x}As$ laterally grown nanowires and contacts using LT-STM/S.

I was the main responsible for planning of the experiment, performing the measurements, analyzing the data, and writing the manuscript.

II. **Combined light excitation and Scanning Gate Microscopy on Heterostructure Nanowire Photovoltaic Devices**
Yen-Po Liu, Jonatan Fast, Zhe Ren, Yang Chen, Adam Burker, Rainer Timm, Heiner Linke, Anders Mikkelsen.
In manuscript.

In this paper we present the electrical transport on a InAs/InP axial barrier NW device using LED and laser sources in combination with SGM.

I was the main responsible for planning of the experiment, building the setup, performing the measurements, analyzing the data, and writing the manuscript.

III. **Optical-beam induced current in InAs/InP nanowires for hot-carrier photovoltaics**
Jonatan Fast*, Yen-Po Liu*, Yang Chen, Lars Samuelson, Adam Burke, Heiner Linke, Anders Mikkelsen.
*J.F. and Y.-P.L. contributed equally.
ACS Applied Energy Materials.2022,5,7728−7734 (2022)

In this paper we present the hot carrier extraction on the InAs/InP barrier NW device using OBIC.

I was the main responsible for building the experimental setup and perform the measurements. I took part in the data analysis and writing of the manuscript.

IV. **Hydrogen plasma enhanced oxide removal of GaSb surfaces and nanowires for transport device**

Yen-Po Liu, Sofie Yngman, Andrea Troian, Giulio D'Acunto, Adam Jönsson, Johannes Svensson, Anders Mikkelsen, Lars-Erik Wernersson, Rainer Timm.

Applied Surface Science, 593, 153336 (2022)

In this paper we present full oxide removal from GaSb NW surfaces using effective hydrogen plasma cleaning in UHV and in ALD, as a protective high-k layer, environment studied *in-situ* by XPS.

I took part in the experiment planning, sample preparation and the XPS beamtime. I did the data analysis and I was the main responsible for writing the manuscript.

V. **Improved Electrostatics through Digital Etch Schemes in Vertical GaSb Nanowire p-MOSFETs on Si**

Zhongyunshen Zhu, Adam Jönsson, Yen-Po Liu, Johannes Svensson, Rainer Timm, and Lars-Erik Wernersson.

ACS Applied Electronic Materials. 2022, 4, 1, 531–538 (2022).

In this paper we present improved electrostatics of vertical GaSb nanowire p-channel MOSFETs by employing robust digital etch schemes, prior to high-κ deposition.

I took part and contributed to the XPS experiment and analysis, and I joined the discussion of the manuscript.

VI. **Interface and Morphology Control of Graphene on InAs Surfaces and Nanowires by Annealing in Atomic Hydrogen**

S. Fatemeh Mousavi, Yen-Po Liu, Giulio D'Acunto, Andrea Troian, José M. Caridad, Yuran Niu, Lin Zhu, Asmita Jash, Vidar Flodgren, Sebastian Lehmann, Kimberly A. Dick, Alexei Zakharov, Rainer Timm, Anders Mikkelsen.

Submitted to ACS Applied Nano Materials.

In this paper we present high quality morphological and chemical control of the hybrid material system of graphene and InAs NW.

I took significant part in the planning of the experiment, making the samples, joining the AFM, PEEM and XPS measurements, and discussing the manuscript.

Publications to which I have contributed, but are not included in this thesis:

VII. **GaN Nanowires as Probes for High Resolution Atomic Force and Scanning Tunneling Microscopy**
Sofie Yngman, Filip Lenrick, Yen-Po Liu, Zhe Ren, Maryam Khalilian, Lars Samuelson, Jonas Ohlsson, Dan Hessman, Rainer Timm, Anders Mikkelsen.
Review of Scientific Instruments, 90(10), p103703. (2019).

VIII. **Few-cycle lightwave-driven currents in a semiconductor at high repetition rate**
Fabian Langer, Yen-Po Liu, Zhe Ren, Vidar Flodgren, Chen Guo, Jan Vogelsang, Sara Mikaelsson, Ivan Sytcevich, Jan Ahrens, Anne L'Huillier, Cord L Arnold, Anders Mikkelsen.
Optica, 7(4), 276-279 (2020).

IX. **Atomic Layer Deposition of Hafnium Oxide on InAs: Insight from Time-Resolved in Situ Studies**
Giulio D'Acunto, Andrea Troian, Esko Kokkonen, Foqia Rehman, Yen-Po Liu, Sofie Yngman, Zhihua Yong, Sarah R McKibbin, Tamires Gallo, Erik Lind, Joachim Schnadt, Rainer Timm.
ACS Applied Electronic Materials, 2(12), p 3915-3922 (2020)

X. **Bismuth surface alloying on 2D InAs nanoplatelets**
Sandra Benter, Yi Liu, Lassi Linnala, Chin Shen Ong, Dong Pan, Austin Irish, Yen-Po Liu, Renan Da Paixao Maciel, Jianhua Zhao, Hongqi Xu, Olle Eriksson, Rainer Timm, Anders Mikkelsen.
In manuscript.

XI. **Bismuth-oxide nanoparticles: study in a beam and as deposited**
M.-H. Mikkelä, M.Marnauza, C. J. D. Hetherington, R. Wallenberg, E. Mårsell, Yen-Po Liu, A. Mikkelsen, O. Björneholm, M.Tchaplyguine.
In manuscript.

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The PhD life in Sweden is the best time in my life so far, and my PhD work is done with great support both technically and mentally from everyone who participated in my life. To begin with my sincere appreciation, most importantly, I am grateful for my supervisors, Anders Mikkelsen and Rainer Timm, who chose me five years ago to come to Lund and to work with great people in the very international division.

I would like to thank Anders, you are the best supervisor ever! You gave me so much freedom to do whatever experiments I enjoyed doing, and you have such adequate funding that allows me to build many lab equipments without worrying about the cost. I admire your broad knowledge, broad connections, open-minded thinking, and the way interacting with people! Talking and meeting with you always broaden my mind. For example, the non-typical annoying trapping states on InAs nanowires can be a temporal memory for neuron calculation applications. The most amazing thing is that you can turn my unexpected data into an interesting story. Most importantly, I appreciate so much for your support in everything.

My dear co-supervisor, Rainer Timm, is not just a supervisor or a colleague; you are also my close friend that I like to share everything about my life with. Further, you are the first one I met after I came to Sweden! Traveling with you for beamtime always has many fun talks and good stories. Your trust in me since the beginning of my PhD makes me flattered, and your way of talking always makes people feel warm and pleasant. I really hope to work much more with you, not just because you helped me improve but also because you make me feel like I am important. Thanks for your well support on good science, careful reading and polishing, and even helping me search for future jobs. My gratitude for the last five years is beyond what words can describe.

My PhD cannot be done this well without my lovely colleagues. I performed my first experiment with Zhe Ren, and you are very professional in explaining everything about the Unisoku and pump-probe laser system to me. I would like to thank Yi, Andrea, Sarah, Estephania, Sofie, and Filip for working with me since the beginning of my PhD. You made me enjoy life in Sweden since then. Also for people who joined the great group after and had a good time with, Fatemeh, Austin, Vidar, and Rohit, we have very good organization and communication in our group,

you really helped me a lot. There are many people in the division that I don't take you as colleagues, sorry, you are my best friends: Giulio, Sanna, Virgi, Sandra, Hanna, Lukas, Alfred, Stefano, Nils, Nelia, Foqia… Literally everyone in the division! Lukas, thank you for building the greenest and coziest office with me in the last five years, and you are my best badminton teammate! Besides, I want to tell Jesper that I appreciate your efficiency at work and that you can always get to the point immediately. Further, there are some essential people in the division who brought fun and make the environment relaxing; Patrik, without you I probably cannot get all the reimbursements back. I am very proud and happy to be in SLJUS.

One thing I really like about working in SLJUS is that we have so much cooperation that broadens my view. The people in EIT make the most advanced devices in the world! Johannes, Adam, Lasse, Erik, Saketh, Zhongyunshen, and Lars-Erik, the experience working with you on the big kT/q project is amazing and valuable. Also, it is quite a pleasant experience working with the solid state physics people, Heiner, Jonatan, Yang, Claes and Dan. You have the ability to dig a physics phenomenon very deeply and then make it clear.

Friends around during my PhD are very important as well! I really appreciate everyone around talking about everything, hanging out, cooking, and drinking. These are really good memories of my life! There is a special one who joined my life from the very last part of my PhD, but make a big influence, Annika. Thank you for bringing me so unique experiences and lifestyle and taking the time to understand me.

Last but most important, my family, especially my parents and Da-Mei group, support me by holding welcoming parties with fantastic food every time when I come back and letting me feel proud of what I am doing.

Abbreviations and symbols

1D, 2D, 3D	One-, two-, and three-dimensional
III–V	Compound composed of one group III-element and one group V-element
AFM	Atomic force microscopy
ALD	Atomic layer deposition
CB	Conduction band
CCD	Charge-coupled device
CMOS	Complementary metal-oxide-semiconductor
CPU	Central processing unit
DOS	Density of states
EBL	Electron beam lithography
E_F	Fermi energy
E_g	Bandgap
FET	Field-effect transistor
FIB	Focused-ion-beam
FWHM	Full width at half maximum
GAA	Gate-all-around
HSQ	Hydrogen silsesquioxane
ICs	Integrated circuits
I_{set}	Setpoint tunnel current
LDOS	Local density of states
LED	Light-emitting diode
MBE	Molecular beam epitaxy
MOSFET	Metal-oxide-semiconductor field-effect transistor
MOVPE	Metal-organic vapor phase epitaxy
NPC	Negative photo-conductance
NW	Nanowire

OBIC	Optical beam induced current
PL	Photoluminescence
PPC	Positive photo-conductance
QD	Quantum dot
QW	Quantum well
RAM	Random access memory
SEM	Scanning electron microscopy
SGM	Scanning gate microscopy
SPCM	Scanning photo-current microscopy
SPM	Scanning probe microscopy
SPEM	Scanning photoelectron microscopy
STM	Scanning tunneling microscopy
STS	Scanning tunneling spectroscopy
TEM	Transmission electron microscopy
TFET	Tunneling field-effect transistor
UHV	Ultra high vacuum
VB	Valence band
WZ	Wurtzite
XPS	X-ray photoelectron spectroscopy
ZB	Zinc-blende

Chapter 1: Introduction

Since the discovery of semiconductor material properties in the early 19th century, semiconductor devices have been developed, and the technology for electronics emerged in all aspects, enabling advances in communications, computing, medical healthcare, clean energy, and many other applications. In modern times, electronics are an essential part of our lives as a daily necessity, and COVID-19 pandemic made the use of information technology even bigger. Semiconductor electronic devices for information processing, usually referred to as integrated circuits (ICs) or microchips, are mainly based on silicon and produced in a mature industry. Due to the needs of modern applications for higher response frequency, efficiency, and optoelectronic applications, compound semiconductors, that is, III-V based semiconductor materials, have become of importance.

In the 1940s, the first solid state transistors were invented. These transistors have kept becoming smaller and significantly increasing the numbers on a single chip. Moore's law, suggested by Gordon Moore in 1965 from his perception, predicts that the number of transistors in a microchip doubles about every two years. For a long time, the industrial trend followed the law well, as shown in Figure 1-1. The process node size of a metal-oxide-semiconductor field-effect transistor (MOSFET) was 10 μm in 1971, while the most advanced manufacturing nowadays is 3 nm by TSMC in September 2022. [1] Around 2014, when the MOSFETs were down-scaled below 20 nm, the slope for Moore's law curve flattened, when thermal issues and quantum tunneling leaking started to interfere with the transport process.

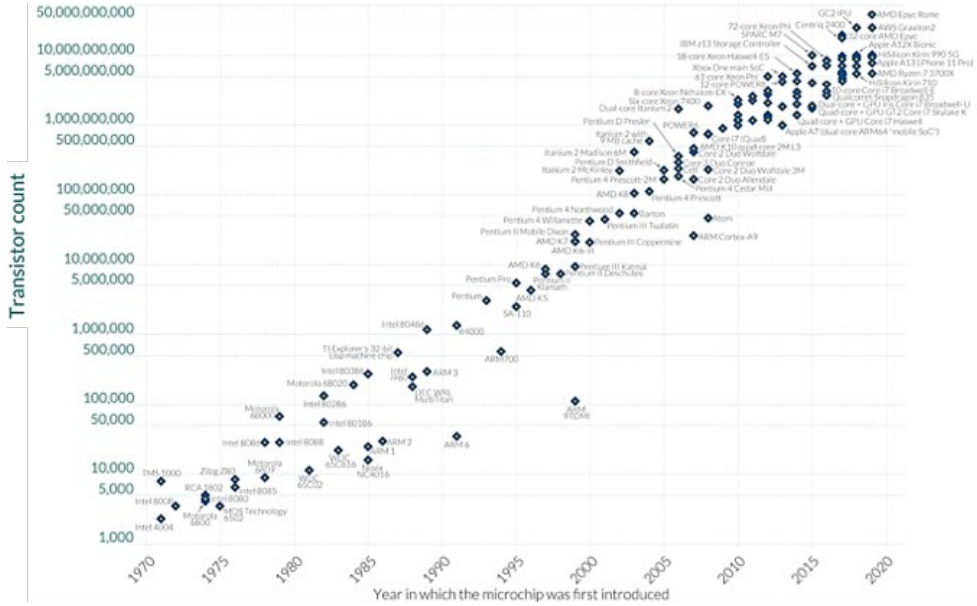


Figure 1-1. Moore's law diagram from 1970 to 2020 showing how the number of transistors doubles every other year. Every point represents the highest transistor number in a chip die of the year. Figure courtesy from [2].

To continue the miniaturization of transistors, the geometry of transistors has changed from planar structure, as seen in Figure 1-2 (a, b), to the FinFET geometry (also called tri-gate transistor due to the triple gate sides around the channel) as shown in Figure 1-2 (c, d). FinFET took the transistor to its third dimension and extended Moore's law. The enhanced FinFET was improved from a single-Fin structure to multiple-Fin channels, as shown in Figure 1-2 (e, f). This technique facilitates the transistor technology developed from sub-20 nm to nowadays state-of-the-art 5 nm process. In order to have even lower working bias, less thermal perturbation and higher efficiency, the gate-all-around (GAA) field-effect transistor with high-k passivation seems to further continue Moore's prediction in silicon-based electronics. The GAA geometry, as shown in Figure 1-3, increased the gate sides around the channel from three (FinFET) to four, which gain the gate field more effective.

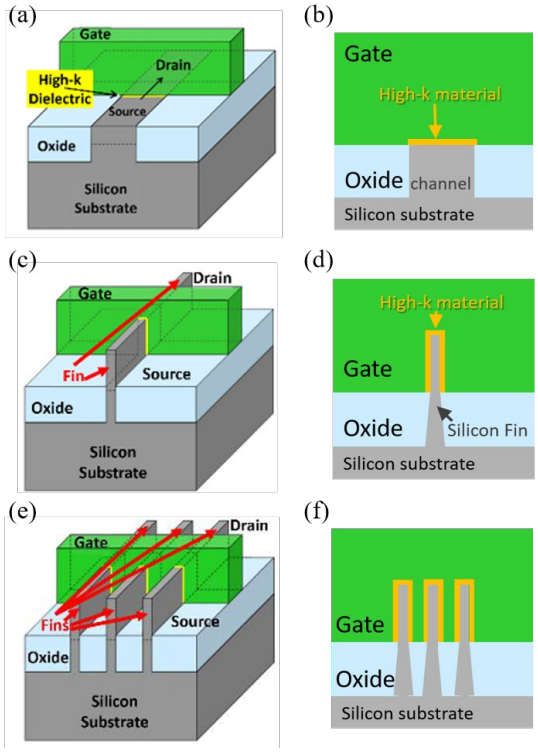


Figure 1-2. The developing of field-effect-transistor (a) 3D image of a plain FET (b) cross-section of a plain FET (c) 3D image of a FinFET (d) cross-section of a FinFET (e) 3D image of a multiple FinFET (f) cross-section of a multiple FinFET. (a)(c)(e) are courtesy from [3].

III-V semiconductors generally have a direct bandgap, and the properties of higher electron/hole carrier mobilities and lower thermal conductivity compared to Silicon make them a great candidate for radio frequency and opto-electronic applications. For example, it is already difficult for Si based semiconductors to support 5G communication at high radio frequency (spectrum band in the range of 1 to 6 GHz) due to the comparably lower electron mobility of Si. The needs for next generation technology require a much higher responding frequency and high-power efficiency; therefore, a replacement of silicon is pressing. Now it is reversed, GaAs is used in the 5G RF signal receiver due to its higher electron mobility. Some III-V semiconductors have much high electron mobility to fulfill the demands for next generation communication, such as the 6G communication band in a frequency range of 100 GHz. The III–V semiconductors consist of materials from group III (e.g. In and Ga) and group V (e.g. As and P) on the periodic table. Compared to Si (the most used industrial semiconductor material), most of the III–V materials have advantages of higher electron/hole mobility, tunable bandgap sizes, customized crystal structure and strong spin-orbit coupling. [4]

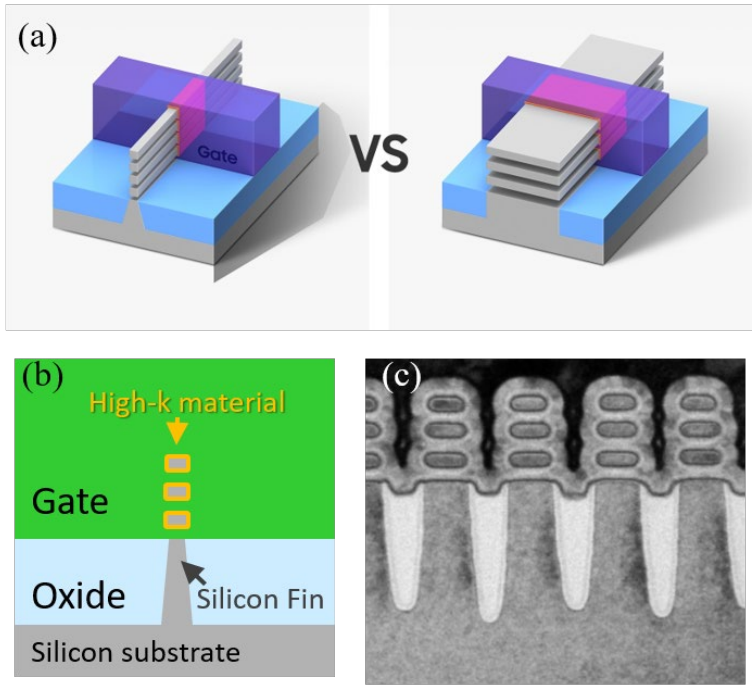


Figure 1-3. Gate-all-around (GAA) field effect transistor (a) the channel structure for GAA: nanowires vs. nanosheets. Figure courtesy from [5] (b) sketch of GAA device cross-section (c) SEM image of the cross-section of a demonstration GAA-FET. Figure courtesy from [6].

The III-V semiconductors, particularly in nanowire (NW) and nanosheet structures, have drawn most of the attention and they have the highest potential for promising future nanometer-scale applications owing to the great properties of III-V semiconductors and the well-defined crystal structure. NWs are crystallized nano-rods with diameters from less than 10 to hundreds of nanometers and lengths usually in the micrometer range. Due to the one-dimensional nano-shaped structure, confinements of electron and photon occur, which leads to unique (opto-)electric transport and thermoelectric behaviors. Therefore, the research in NWs with promising candidates, for example, III-V materials, has become a hot spot. These properties make III–V NWs optimal for high-performance electronics[7], photonics[8][9], and energy harvesting[10][11]. Not only in research, but also in industry it is urgent to develop the GAA-FET, which channels require the material to be in the form of nanowires or nanosheets. In this dissertation, these III-V nano-structured semiconductors are studied in the transistors and photovoltaics device geometry with various techniques from synchrotron based XPS to low-temperature STM to discover the surface and electrical properties and further improve their performance.

To investigate and develop the function of these excellent semiconductors, I fabricated the devices made of these nano-materials, like transistors or opto-electronic components. The fundamental concept for semiconductor devices is to control the conductivity with an external potential; for example, the FET uses a gate electrode to apply a local electric field on the channel material. Hence the current flowing through the channel depends on the gate voltage, bit 1 (current) and 0 (no current), which is how the binary unit forms. Furthermore, light with moderate photon energy (above the bandgap) has the ability to control the semiconductor as well, such as photo-detector, solar cell, and other photovoltaic products. Semiconductor engineering includes doping to create extra states within the bandgap, material heterojunctions for building customized band engineered devices, e.g., p-n junction or potential barrier, in both axially and radially directions, mixing different material concentration for bandgap engineering and many other technical methods. Once the nano-structure can be well defined and grown in the precision of atomic layers for specific applications, (e.g. a 25 nm InP segment in a few micrometer InAs NW) the precise gate position of the device determines the device functionality and performance.

Not only the semiconductor material structure engineering, but also the interface and surface structure can play an important role, especially when the materials are scaled down and the impact from the surface gets higher. As a consequence of low-dimensional geometry, NWs and nanosheets have a considerably higher surface-to-bulk ratio, making them much more sensitive to surface effects compared to larger-scale components. Research shows that the NW device properties are greatly influenced both electronically and optically by the surface conditions[12], [13]. Therefore, the surface morphology, surface defects, surface states, and possible oxidation of the NW facets play an important role. Once the NW comes to the device fabrication steps, the surface will turn into an interface to other materials, which increases the complexity since they may vary depending on the material of the NW and the combination of the NW and the other material, for example, Al_2O_3, HfO_2, Ti, or Al.

The surface of the nano-device plays a determinant role in the device performance. As nano-device development become more complex with the technology demands, the fundamental understanding and characterization of the nano-materials are essential. However, the understanding of the correlation between electronic and morphologic properties of NW surfaces is inadequate, and the characterization of the surface of the NW itself and in its device geometry is not straight forward. Advanced characterization methods can in principle characterize semiconductors, including e.g., transmission electron microscopy (TEM), scanning tunneling microscope (STM) scanning tunneling spectroscopy (STS), photoluminescence

(PL), and X-ray photoelectron spectroscopy (XPS). But they are limited regarding nano-structure dimension, surface contribution, or device geometry. The STM/S is limited to scan only on a conducting surface while all the nano-devices need an insulating substrate, the X-ray techniques are limited to beam sizes larger than the NW itself, the TEM measurement needs to have thin samples in a hundred nanometer scale for transmission which is challenging for operando devices, and the PL results show the properties contributed mainly from the bulk.

The primary goal of this work is to come beyond the obstacles, for instance, STM/S measurement of the transistor device geometry, in characterizing the surfaces of III–V NWs and nanosheet devices in electronic, morphologic, and structural properties down to the atomic scale. In this respect, I have fabricated suspended single NW/nanosheet devices where the materials used for the top surface are all conductive, optimized for STM/S measurements of both electrical and morphologic aspects. The same technique was used to observe the lateral NWs used in quantum devices. Further, I developed the laser combined scanning gate microscopy (SGM) to study hot electron dynamics and electrical transport of InAs/InP NW devices with mobile gate precision down to the nanometer scale. The chemical composition of NW surfaces was studied using X-ray photoelectron spectroscopy (XPS) and scanning photoelectron microscopy (SPEM), which are capable of detecting elements and chemical compounds for homogeneous surfaces and nanometer scale structures, respectively.

Outline of the thesis

This dissertation includes the core topics of novel nano-material, NW, and nanosheet based devices. It covers the III-V NWs for next generation GAA MOSFET, ALD for high-k passivation around the FET channel, and other scientific issues for future electronics. We investigated electrical devices during operation down to atomic scale at low-temperature, studied the electrical transport under the mobile local gate combined with laser/LED illumination, and characterized its surface chemistry. In Chapter 2, the semiconductor materials, their surface crystal structure, and the nano-structure will be introduced. These novel nano-materials need to be fabricated into devices to make them functioning. The fabrication process and details for different characterization techniques will be described in Chapter 3. Since the materials are scaled down to one-dimensional (1D, NW) or two-dimensional (2D, nanosheet and graphene) structures, the surface-to-bulk ratio becomes tremendous. To see the surface with high resolution, we use STM to investigate the surface down to the atomic scale and use STS to study the local surface electrical properties. The STM and STS techniques are presented in Chapter 4. While operating devices are sensitive to electric fields and the light conditions, we developed a system combining single-mode laser and SGM for transport and hot

electron studies. The system and its abilities are introduced in Chapter 5. Apart from the atomic scale topography and the surface band structure, also the surface chemistry, which is still missing, has high impact on the device performance. Therefore, we use synchrotron-based XPS to probe into the issue, as presented in Chapter 6. Data from the semiconductor nano-materials and devices measured by the above mentioned techniques will be shown in Chapter 7.

The results of this dissertation show the surface morphology, the effectiveness of the cleaning, and the elemental composition along the NW resulting in local bandgap changes of lateral $In_xGa_{1-x}As$ NWs using low-temperature STM/S in ***Paper I***. The surface of GaSb NWs and different treatments to improve their interface quality, on the other hand, were studied by XPS. Here we demonstrate full oxide removal on the GaSb surfaces in UHV and that the NWs are cleaned faster and more efficiently than planar substrates. Cleaning suggestions with pre-treatment and surface protection for scalable fabrication are suggested. (***Paper IV***) The relevance of surface treatments also became relevant for vertical GaSb NW MOSFETs, which after improved removal of the Sb-oxides, proved by XPS, reach an improved state-of-the-art subthreshold swing value. (***Paper V***)

In order to study carrier transport in devices with nanometer precision heterojunctions, characterization techniques with especially high spatial resolution are required. InAs/InP NW photovoltaic devices include such nm-scale heterojunctions, where OBIC demonstrates hot-electron extraction across the InP segment, thus generating electrical power. (***Paper III***) With the SGM combined with LED/laser excitation, setup, interactive effects of photon-excitation and local band alignment contributing to the device electron transport are studied. The demonstrated setup has significant advantages to study optoelectronics. (***Paper II***) New types of future devices may require hybrid integration of one-dimensional, i.e., III-V NWs, and two-dimensional, i.e., graphene, nanostructures, combining their excellent complementary properties. ***Paper VI*** affirms high quality morphological and chemical control of this hybrid material system.

Chapter 2: Low-dimensional Semiconductor Materials

As technology develops, the size of electronics scales down and new semiconductor materials could be introduced. The material and the structure of semiconductors to the atomic scale become central for future technology. In this chapter, semiconductor materials and their structure are introduced in section 2.1. The geometry of low dimensional semiconductors and their surfaces are discussed in section 2.2, and the semiconductor materials used in this dissertation are presented in section 2.3.

2.1 Semiconductor materials and their structure

A semiconductor is a material with electrical properties between a conductor and an insulator with a moderate bandgap, which is the area between the bottom of the unoccupied conduction band and the top of the occupied valence band where there are no electronic states. Thanks to the appropriate bandgap, the semiconductor conductivity can be controlled by introduction of impurities, doping, and devices operated with some assistance from a small external electrical field, gating. Thus one can control the transport properties of the materials for various applications. The bandgap of semiconductors makes it possible to interact with photons of specific energies, both emitting and absorbing in the visible range. Usually, the semiconductor is defined with a bandgap larger than 0eV and below 3 eV. For instance, the bandgap energies of the most common semiconductors are 1.1 eV for silicon, 0.4 eV for InAs, and 1.3 eV for InP at room temperature. [14] An exception is Nitride semiconductors with a high bandgap, for example, GaN with a 3.49 eV bandgap is classified as a semiconductor, and it is famous for high power communication devices and blue LEDs.

The most common semiconductor in our daily used technologies is silicon. It is earth abundant, and the fabrication procedure is very well-developed in industry.

Commercial electronics, like the central processing unit (CPU) of a computer consisting of billions of transistors (there are 16 billion transistors on Apple M1 chip[15]), random access memory (RAM), and sensors, are silicon-based. Since Si is a group IV material, it is convenient to process with doping for p-n junction for wide range applications. However, higher operational speed and higher efficiency/power are needed as technology develops, and the properties of many III-V semiconductors fit the requirements. Most III-V semiconductors have a direct bandgap which is needed for optoelectronics, and some have strong spin-orbit coupling needed for quantum technologies. The III-V semiconductor materials are important in both research and industry due to the need for high speed and low consumption for modern electronics.

Applications in broad fields can be achieved by engineering of the electrical properties, such as p/n-doping and heterojunctions, and the fabrication geometry of semiconductors can be engineered. Doping variation in the semiconductors grants the material with spatial defined heterostructures structures, for example, p-n junctions. The fundamental of doping is to intentionally introduce specific impurities into a semiconductor crystal to modify the conductivity caused by externally implemented electrons or holes. Doping is a very matured and widely used process in the silicon-based semiconductor industry, for example, B, In, and Ga are used as p-type dopants; while P, As, Sb and Li are used as p-type dopants, for products, like CMOS, photodetector, LED and solar cell. The doping techniques can be well applied to the growth of III-V NWs, creating the functions in the nanometer scale.

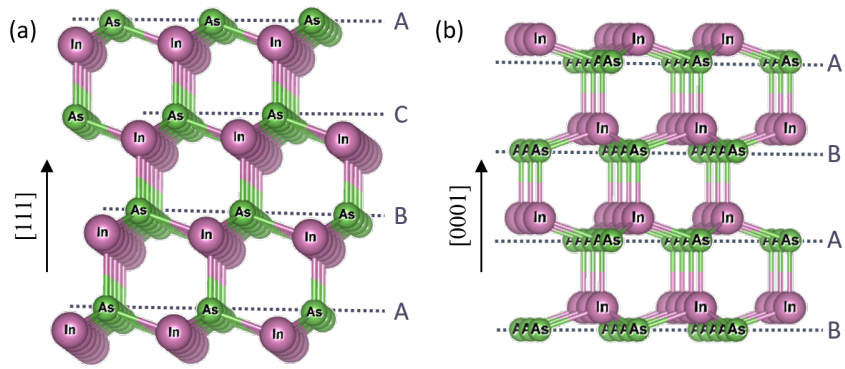


Figure 2-1. The unit cell schematic views of InAs in (a) ZB and (b) WZ crystals using software VESTA. The difference in stacking sequence (ABC or AB) is seen for both structures. The purple spheres represent for group III atoms, i.e. In, and the green ones, i.e. As, denote for group V-atoms.

The structure of the semiconductor nanomaterials has impact on their band structures and, therefore, varies their optical and electronic properties. Most III-V materials, except the nitrides, occur naturally only in the cubic zinc-blende (ZB) crystal structure, which has a stacking …ABCABC… of hexagonal layers along the crystal [111] direction, as shown in Figure 2-1 (a). The hexagonal wurtzite (WZ) structure, with stacking of …ABABAB… as shown in Figure 2-1 (b), has instead been found more often in NWs[16]. The low-dimensional materials have large surface-to-bulk ratio, and different surface facets could result in a different surface status, e.g., surface oxidation and surface reconstruction. The surface, incorporating differently with other materials, would be an interface in device geometries affecting the device properties, and will be discussed in the next section.

2.2 Low-dimensional semiconductors and their surfaces

Nano-material science has been developed for several decades. The low dimensional materials, like one-dimensional NWs or two-dimensional nanosheets, have unique and different properties as compared to the bulk. For example, monolayer graphene shows Dirac points in its band structure and has extraordinary mechanical and electrical properties, but not in multi-layer graphene or bulk graphite.[17], [18] Due to the confined and guided photon and electron transport, the low-dimensional semiconductor materials have also helped extending the understanding of fundamental optical, structural, or electrical properties.

NWs define their transport function in large part due to the confinement of electrons and holes in space. The significant control in two dimensions benefits the future electronic devices, for instance, GAA transistors. The size and geometry of the NWs can be customized by the growth mechanism and parameters, which allows for band structure engineering by combining different materials and crystal structures, axially or radially. One of the large advantages of NWs is that they have minimal effects from strain so that a rather large lattice constant mismatch without dislocations is possible, due to their small footprint. This for example allow the growth of III-V NWs on silicon or integration of very lattice strained combinations III-V materials. Further, III-V NWs can be grown in crystal structures that were previously unavailable in bulk, such as the hexagonal WZ structure. In this thesis, all the nano-materials studied are either NWs (30-100 nm diameter for III-V semiconductors with length a couple of micrometers) or nanosheets (10 nm thickness for InAs with an area of around 3 μm^2).

There are two distinct types of III-V NWs studied in this dissertation: vertically grown NWs or laterally grown. The vertically grown NWs in this thesis are grown in the ZB structure with side facets typically {110} or {111}A/B twin plane facets, or WZ structure with typically $\{11\bar{2}0\}$side facet.[4], [19]–[21] For laterally grown NWs, the top facet of the NW is in surface direction (001), comparable to the side facet of vertically grown NWs. The angle between the NW (001) top facet and its side facets amounts to ~45 degrees, indicating that the side facets consist of {011} surface planes.

The III-V NWs in this thesis are mostly grown epitaxially on crystalline substrates using Au particles, except for the laterally grown $In_xGa_{1-x}As$ NWs of Paper I. The epitaxially grown III-V NWs have been found to prefer to grow in the $[\overline{111}]$ direction and are usually grown on (111)B substrates so that they grow perpendicular to the growth substrate. Here is an example of the growth procedure: We first expose the desired size for Au seeds using electron beam lithography (EBL) on a growth substrate and then deposit Au, Figure 2-2 (a). After lift-off, the substrate with Au particles is inserted into a metal-organic vapor phase epitaxy (MOVPE) growth chamber. Second, the temperature is increased under group V precursor flow in order to alloy the Au-particle with the substrate and to remove oxide residues and contaminants on the substrate, see Figure 2-2 (b). To initiate the growth, the temperature is reduced so that nucleation only occurs under the Au-particle (and not on the substrate), typically to 400-600 °C. The group III material is then thought to enter the Au-particle and supersaturate it, see Figure 2-2 (c). At the interface in between the vapor, the Au-group-III alloy, and the substrate, growth material precipitates into a nucleus which rapidly grows and forms a new layer of crystal directly beneath the Au-particle. A single crystalline NW with diameter set by the Au-particle and the length corresponding to the growth time would then be grown, as shown in Figure 2-2 (d). The growth of NWs is an epitaxial process, meaning that the crystal structure of the growth substrate continues into the NW.

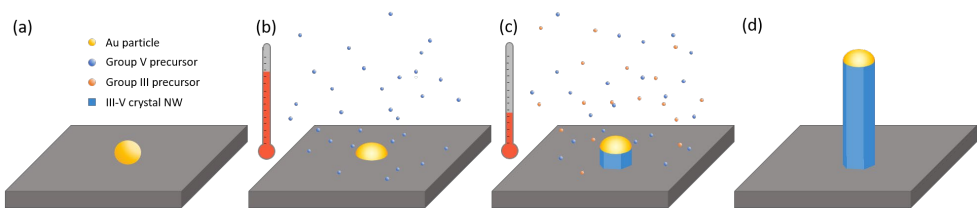


Figure 2-2. Epitaxial III-V NW growth. (a) Size selected Au particles are deposited on a growth substrate using EBL. (b) The sample is annealed under group-V flow to allow the Au-particle to alloy with the substrate and for removal of surface oxides/contaminants. (c) Temperature is lowered and group III-precursor is introduced. III–V materials precipitate directly under the Au-particle. (d) After growth the vertical NW still resides with the Au-alloy on top.

Like the crystal structures discussed above, also the surfaces differ depending on the facet terminations. NW growth control to achieve different surface facets is possible, as an example of a WZ-ZB InAs NW in Figure 2-3, and the surface facets have an impact on the band structure. [19], [22]. The electronic structure of a material can be altered by the surface states around the Fermi level. Surface states located within the fundamental bandgap can be detrimental to the performance of semiconductor devices where they can act as unwanted recombination centers for charge carriers or change band alignment at a heterojunction *via* Fermi level pinning[23]. The surface states within the bandgap can be seen in the STS measurements, as will be discussed later. In the case of GaAs and InAs NWs, there are no intrinsic surface states located within the bandgap for non-polar {110} and {11-20} surface facets[23]. However, recent publications show that the surface states in the conduction band can trap the free carriers, thus also influencing the device performance[19,20], and it has been proven that the trapped electrons are possible to be de-trapped back into the NW again as free electrons to improve the conductivity.[20], [25] This effect is observed on both plain InAs NW and nanosheet[26] devices under laser and LED lamp illuminations. The surface state trapping situation can be complex giving either positive photo-conductance (PPC) or negative photo-conductance (NPC) depending on the light intensity. More discussions will be in Chapter 7. Further, surface oxides and defects, such as vacancies, atomic steps, adsorbates, and material interfaces, can potentially cause surface states; therefore, the surface condition and proper surface passivation[27] play important roles in device properties.

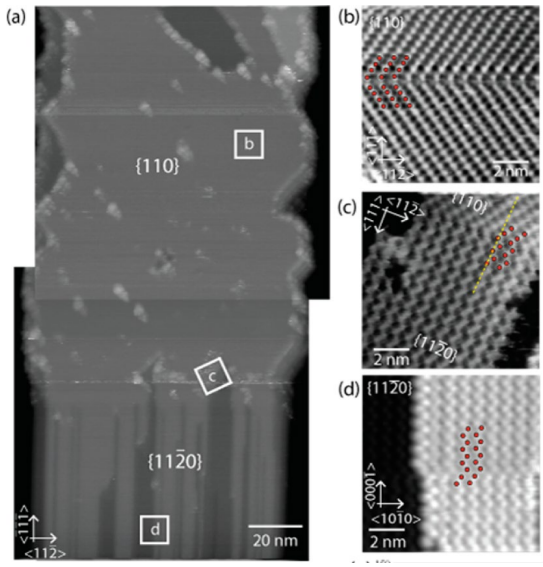


Figure 2-3. STM results on a WZ-ZB InAs NW from Reference [19]. (a) Overview image of a {11-20}-{110}-type WZ-ZB interface on a NW. V_{sample} = -1.0 V, I_T = 50 pA. (b) Micrograph depicting As atoms on part of a rotationally twinned {110} facet. V_{sample} = -2.2 V, I_T = 100 pA. (c) Atomic arrangement on the {11-20} facet. V_{sample} = -2.3 V, I_T = 160 pA. (d) Atomically sharp interface between {110} and {11-20} facets. V_{sample} = -2.5 V, I_T = 100 pA.

2.3 III-V semiconductor nanowires and nanosheets

III-V semiconductors are the compounds made of group-III materials (with 3 valence electrons), e.g. Ga and In, and group-V materials, e.g. P, As, and Sb, on the periodic table. They are relevant for the next generation semiconductor technology because of the higher flexibility in engineering the crystal structure and its electrical properties compared to the most popular semiconductor nowadays, silicon. III–V semiconductor NWs have demonstrated significant promise for applications in (opto)electronics and quantum computing. The properties for nanostructured III-V can be quite different to the bulk material, for example, the InAs NWs have superb electrical conductivity in contrast to the bulk substrate due to the free electrons at the surface caused by surface band bending.

In the following sections, the main III-V materials used in this work will be introduced starting from the high electron mobility material InAs for n-channel in section 2.4.1 to high hole mobility GaSb for p-channel in section 2.4.4. Also, the lateral $In_xGa_{1-x}As$ NW for quantum computing will be presented in section 2.4.2 while Indium Arsenide and Indium Phosphide heterojunction (InAs/InP) NW for photovoltaic applications in section 2.4.3. The NW growth is supported by our cooperators in Lund.

2.3.1 Indium Arsenide (InAs)

InAs promotes superior device performance due to its high electron mobility and direct bandgap of 0.35 eV at room temperature[28], and it is widely researched in the fields of transistors[29]–[33], photovoltaics[34], and terahertz laser[35], [36]. Quantum dots and quantum computing bits are demonstrated with low-dimensional InAs materials.[37] Devices such as gate-all-around (GAA) NW metal-oxide-semiconductor capacitors and field-effect transistors (FET) have been realized for InAs and InGaAs NWs. In this dissertation, both InAs NWs and nanosheets are used for single suspended nano-devices, as shown in Figure 2-4 (a) and (b), respectively. The device fabrication and its geometry are described in chapter 3.

The InAs NWs, used in Paper VI, are grown using low pressure MOVPE on InAs <111>B substrates with Au aerosol particles with diameters around 30 nm acting as seeds for the growth of the NWs. A close coupled showerhead AIXTRON 3x2" system was used. The growth process was initiated by annealing the aerosol-covered growth substrate for 10 minutes in an AsH_3/H_2 at 550°C. After setting a growth temperature of 470°C, a short stem and alternating WZ and ZB segments were grown. NW growth was terminated by cutting the precusors supply and cooling under the same AsH_3/H_2 ambience as used for the annealing down to 300°C. The diameter for the used NWs is 30 nm with a length of around 2 μm, as shown in Figure 2-4 (a), consisting of both WZ and ZB segments.

The InAs nanosheets used in this work were grown on p-type Si (111) substrates in a molecular-beam epitaxy (MBE) system using silver as seed particles. The quality of the nanosheets is highly dependent on the growth temperature[38], and high quality samples are grown at a relatively high temperature at 525 °C for 40 min with the V/III beam equivalent pressure ratio being set at 6.3 to achieve a reasonable density for the micro-manipulator to pick up a single nanosheet at once – a process which will be discussed in section 3.5. The indium flux here determines the dimensional tunability to be 1D or 2D structure. As soon as the indium-rich growth condition was reached, the silver−indium alloy droplets start segregation, and the morphology of InAs evolved from 1D NW to 2D nanosheet gradually due to the anisotropical growth caused by catalyst alloy segregation. Due to the high indium flux, high-density and large-size free-standing 2D InAs nanosheets were acquired and the structure is mixed with WZ and ZB phases[26].

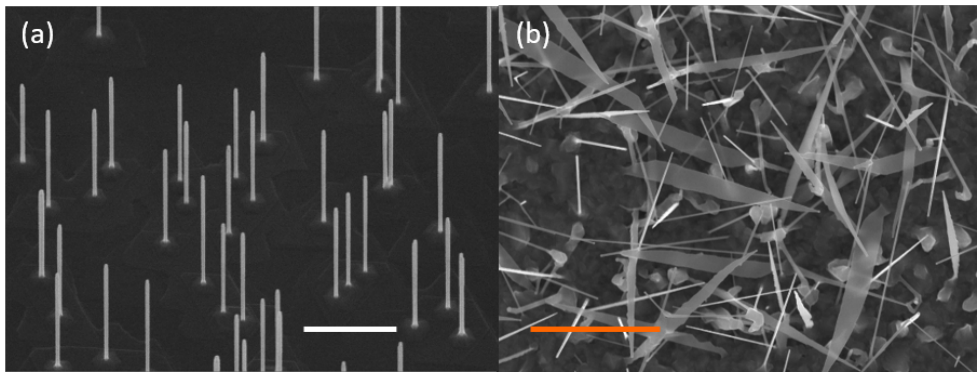


Figure 2-4. (a) InAs NWs of growth run number 3110 CCS with a diameter of 30 nm on the growth substrate. The white scale bar is 1 um. (b) InAs nanosheets on growth sample. The orange scale bar is 2 µm.

2.3.2 Indium Gallium Arsenide ($In_xGa_{1-x}As$)

As for InAs, an alloy of InAs with gallium arsenide (GaAs) forms indium gallium arsenide ($In_xGa_{1-x}As$) - a material with a bandgap dependent on the concentration ratio of the In/Ga components. The bulk lattice constants of InAs and GaAs are 6.06 Å and 5.65 Å, respectively, which is within the lattice mismatch tolerance and close enough to form an alloy. The bandgap of the $In_xGa_{1-x}As$ almost linearly changes from that of InAs, around 0.35 eV at room temperature, to that of GaAs, about 1.4 eV, according to the In/Ga ratio.[39]

The laterally grown $In_xGa_{1-x}As$ NWs, which are described in Paper I, are relevant for radio frequency and quantum computing applications. The $In_xGa_{1-x}As$ NW devices were selectively grown in a lateral growth approach on a semi-insulating InP:Fe (001) substrate by MOVPE. The process starts from electron beam lithography (EBL) to define hydrogen silsesquioxane (HSQ) lines aligned to [100] with a spacing of 50 nm, which ultimately would be the width of the NWs. After defining the HSQ patterns by EBL, a 13 nm $In_{0.63}Ga_{0.37}As$ is grown on all areas that are not covered by HSQ. The NW facets are defined by [001] top-surface and {011} sidewalls. The composition and thickness of the 2D layer were confirmed by X-ray diffraction, however, due to different growth kinetics close to the small feature of the HSQ mask, the NWs are expected to have a lower Ga content[40]. After the growth of the 2D layer including the lateral NWs, a following process for forming the contacts begins with a second HSQ exposure with lines aligned in the [110] direction, covering the NWs. A second growth step of ~25 nm Sn doped $In_{0.63}Ga_{0.37}As$ contacts ($N_D = 5x10^{19}$ cm^{-3}) was then performed. Due to the 45° rotation relative to the NWs, the contacts are defined by {111}B facets. With such a specialized sample, we aim to understand the surface morphology and electrical properties of the NWs to further progress the sample into the application.

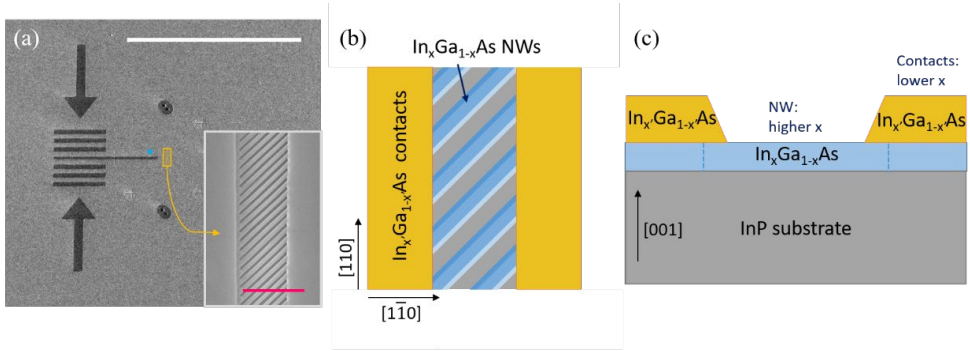


Figure 2-5. Lateral $In_xGa_{1-x}As$ NW device schematics: (a) SEM image of the laterally grown NW sample with Ti markers for STM navigation. The length of the white scale bar is 200 µm. The inset shows the zoomed in image from the yellow rectangle, where the NWs are grown. The length of the pink scale bar is 500 nm. (b) Top view illustration of the NW sample design and material. x=0.63 for the composition of the contact material, while x is higher in the NW material. (c) Cross-sectional schematic of the NWs and contacts. The dashed lines show where the NWs end.

2.3.3 Indium Arsenide and Indium Phosphide heterojunction (InAs/InP)

Heterostructures consisting of InAs NW s with InP segments have shown to produce a photocurrent under optical illumination with a higher open circuit voltage than the Shockley-Queisser limit for a corresponding bulk InAs photovoltaic device.[41] The observed high photovoltage is believed to be generated by hot electrons diffusing over the InP energy barrier with a higher bandgap. An InAs NW with a diameter of about 50 nm and a length of 2 µm, embedded with an InP segment located roughly at the center in axial direction, was studied. The length of the InP segment is chosen to be long enough to rule out tunneling but shorter than expected relaxation lengths, and it is around 25 nm. It results in a potential barrier of 0.56 eV and 0.38 eV in the conduction and valence band, respectively, as shown in Figure 2-6 (b). Growth is done by chemical beam epitaxy using gold seed particles deposited on an InAs (111)B surface; all segments are of WZ crystal structure. High crystalline quality with few defects is expected, except for some stacking faults in the growth direction, and the samples are weakly n-type.

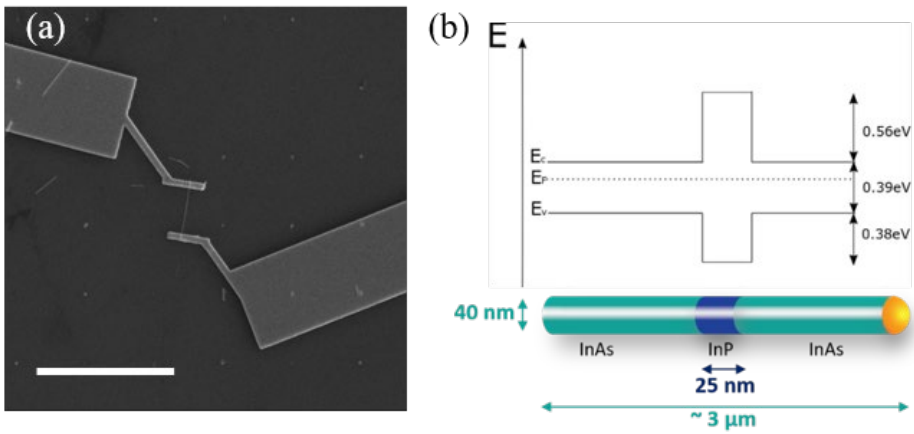


Figure 2-6. (a) SEM image of an InAs NW with an InP segment in a device configuration. (b)The graphic sketch and the band diagram of the InAs/InP NW are labeled with its dimension.

2.3.4 Gallium Antimonide (GaSb)

In contrast to the high electron mobility material InAs, the high hole mobility material GaSb makes the material of choice for p-channel conductivity. Fully NW-based complementary metal-oxide-semiconductor (CMOS) transistors have been realized using InAs and GaSb NWs monolithically integrated on Si[42]. Another highly promising approach towards novel NW-based devices consists of InAs-GaSb NW tunneling field-effect transistors (TFET)[43], which recently have demonstrated steep slope behavior and high current densities for 10 nm thin NWs[43].

The growth of the GaSb NWs starts with the same procedure as described in section 2.2, using EBL to pattern arrays of Au particles as seeds for the NW growth on Si(111) substrates with a 250 nm highly doped InAs layer on top. Then, InAs-GaSb NWs were grown from the Au seeds using MOVPE in an Aixtron CCS reactor. A short InAs segment was grown first, and this InAs stem is required because the nucleation of GaSb directly on the substrate surface is challenging[44]. The GaSb segment was grown on top of the InAs stem. The NWs grown by our cooperators obtain a diameter of about 50 nm and a length of around 1.55 µm.

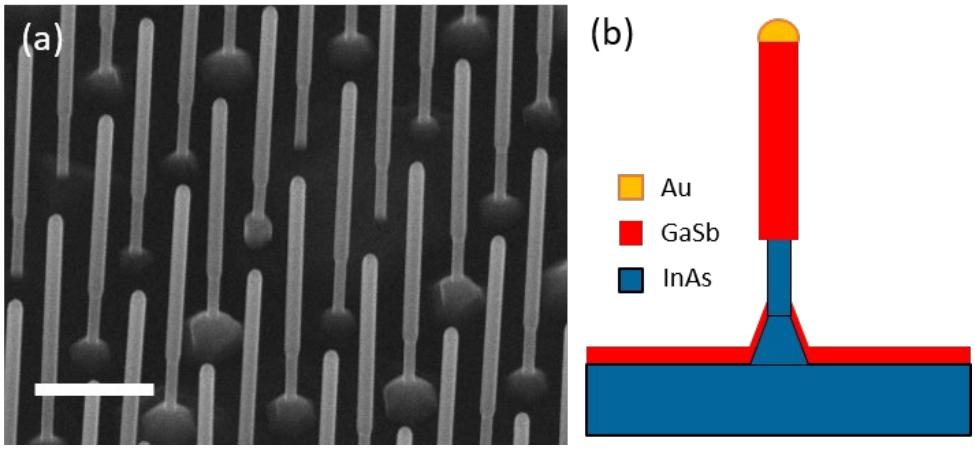


Figure 2-7. (a) SEM image of the NW growth sample. The white scale bar is 500 nm. (b) A schematic diagram of the grown GaSb NW.

Chapter 3:
Nano-device Fabrication and Surface Control

Nanoscale semiconductor fabrication is the key to advancements in modern technology, e.g., self-driving cars, 6G communications, and artificial intelligence. A transistor is the fundamental device used in the logic and calculating, and its dimension has been scaled down following Moore's Law in the past decades. In the most advanced modern foundries, companies like Intel handles both advanced IC design and manufacturing, Taiwan semiconductor manufacturing company (TSMC) currently produces 92% of the world's most advanced chips (5 nm node technology) in 2021[45], [46], [47], and Samsung leads in the dynamic random access memory (DRAM) industry[48]. Furthermore, new types of devices are released from the latest research; for instance, Microsoft is developing quantum computers with combined fabrication techniques of semiconductors and superconductors[49], in which the new and advanced fabrication methods play an important role.

The present work is centered on low dimensional nano-devices, including 2D InAs nanosheets and 1D III-V NWs, investigating the surfaces, interfaces, and electrical and optical properties with the long term aim for applications such as transistors, quantum computers and photovoltaic devices. The device fabrications typically include basic procedures, like material transfer, layout design, chemical processes, lithography, metal deposition, and lift-off. The specific processing methods and order of these can be different depending on the type of sample desired. Among many fabrication procedures used, I would like to emphasize on the devices for STM measurement which display many of the involved methods. For this type of device, the sample has to be conductive everywhere on the top over the whole sample, as shown in Fig 3-1, to allow the STM scanning (as will be discussed in Chapter 4.1). In this case, the nanomaterials are suspended across the two contact electrodes, which can rule out the interface effects between the material surface and the substrate. It is worth mentioning that not many experimental methods can characterize and observe the surface of operating semiconductor devices down to the atomic scale. For example, TEM gives averaging atomic resolution along a

crystal direction but not surface information, also, it requires a nanometer thin sample to let the transmitting electron pass through. Further processing, such as, focused ion beam (FIB) cutting, could thin down or give a cross section of the devices, but it would also change the pristine status of the sample surface and make the devices non-functioning.

The entire fabrication procedures of the STM devices follow pattern design, surface cleaning, photoresist spin coating, electron beam lithography, plasma cleaning, contact material deposition, and material transfer. The illustrations of the whole procedure are shown below in Fig 3-2.

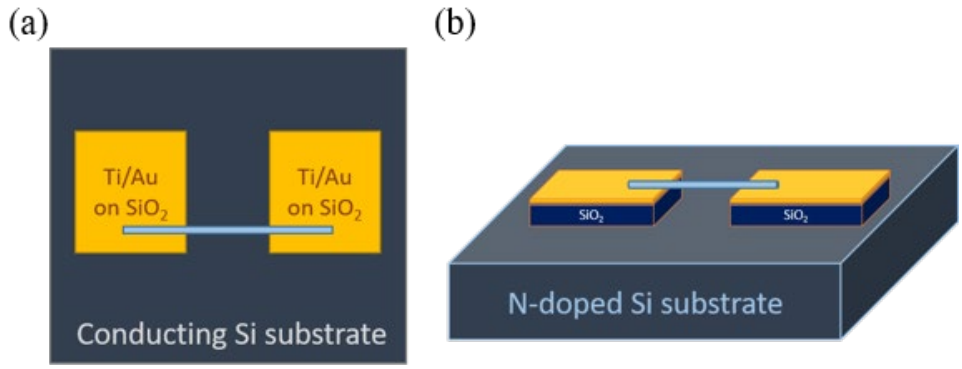


Figure 3-1. Sketch graph of the single suspended NW device for STM measurement (a) top view of the device showing that the whole surface of the sample can be conductive (b) a 3D view of the device showing that the SiO_2 underneath the metal contacts isolates the device from the Si substrate.

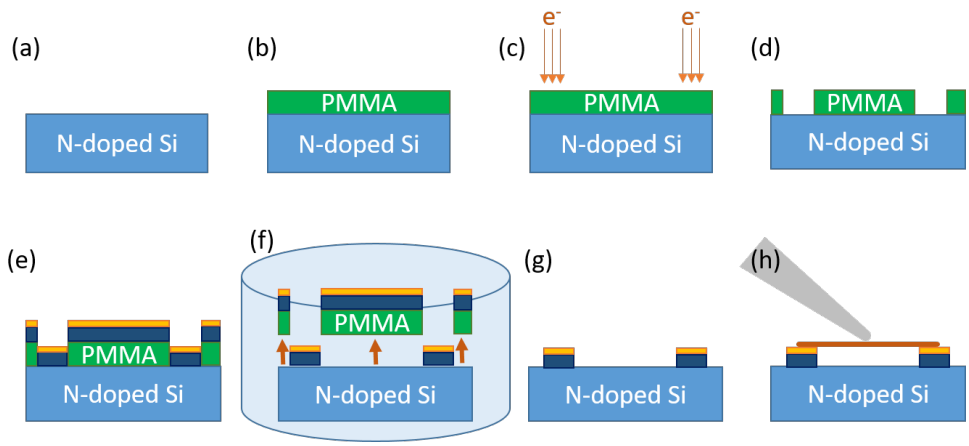


Figure 3-2. The device fabrication procedure for STM measurement (a) cleaning the Si wafer with IPA and acetone in an ultrasonic bath (b) spin-coating the photoresist, PMMA, on (c) exposing the designed pattern layout by electron beam lithography (d) developing the exposed PMMA in MIBK:IPA (methyl isobutyl ketone:isopropanol)=1:3 (e) depositing SiO_x, Ti and Au on the exposed and developed sample (f) lift-off the non-exposed part by acetone. (g) the pre-patterned electrodes ready (h) transfering the nano-material across the electrodes.

3.1 Pattern design

The software Klayout is used to design a lithographic mask pattern. It has integrated functions for layout patterns and supports numerous image files, including GDSII; which is the primary file format used by Raith, the lithography software used in the EBL systems in the lab. For a semiconductor device, at least two electrical contacts are needed for the source and drain. Each set of contact patterns, as shown in Figure 3-4(a), contains two large pads for wire bonding (for external contacts) and long horizontal lines toward the fine structure gap, where the center of Figure 3-3(b) or Figure 3-4(c) is, for placing the material. Some small features as markers, i.e., stripes with width of two hundred nanometers and length of a few micrometers (see Figure 3-3(a)) are patterned to provide us the actual position of the tip related to the device, which makes the navigation before the STM measurement easier. In my design as shown in Figure 3-4(a), the long horizontal lines have different widths, for example, the initial width of the horizontal electrodes nearest to the bond pads is 20 μm, which tapers off to a width of 10 μm when it is 100 μm away from the gap for the nanomaterial in the x-axis, which might still be visible by the microscope to the CCD camera. The width of the finest horizontal line is only 5 μm, which is within the maximum STM scanning range. The width differences can benefit for the STM navigation. Once we come to the end of the horizontal contact, the opposite side to the bonding pad, the vertical contacts are leading to where the nano-material is placed, with width from 4 μm at the connection to the horizontal contact smoothly shrinking to 2 um wide at the trench. Hence, one can tell the direction to the nano-material by the width change. The nano-material would be there at the trench, so then we are at the device. The descriptions above are for one set of the device electrodes, and I usually put 5 sets of the electrode on one substrate, as shown in Figure 3-4 (a) and (b), so if one device failed, I don't need to take everything out from the UHV chamber, wire-bond new devices, pump to UHV and clean the surface again.

It is worth mentioning that all the surfaces features must be able to conduct a current, in order to scan/navigate with the STM tip. Otherwise, the STM cannot detect the tunneling current, and then the feedback loop would push the tip crashing into the sample. There is a failure example in Figure 3-3 (a), a thin stripe aside the contact electrode could give a hint that the tip is on the top electrode to the material. Vice versa, if one sees two stripes on the sides in STM image, the tip at the bottom part of the nanomaterial. However, the nicely-looking thin fingers for navigation cannot be biased, since they are not connected to any electrical pad. That means the potential of the stripes is floating and they cannot create a current loop for tunneling mechanism. As a result, the tip would scratch through the thin features if they are scanned over, instead of telling a relative position. The SEM image of the device

colored by the potential is presented in Figure 3-3 (b), and one can see that once both contacts have a voltage applied.

The aperture diameter of the electron beam after the objective lens would lead to different beam sizes, depths of focus and intensities (electrical current). For example, a larger diameter, i.e., 200 μm, provides a higher current, exposing stronger and faster but less precise. On the other hand, a 30 μm aperture gives a better resolution but requires a longer exposure time. Therefore, the contact features in different scales need to be designed at a different layer in layout for individual apertures, dose factors and step sizes in the settings. In the layout pattern in Figure 3-3 (a), the pink features, extending all the way to the bonding pads are exposed with aperture 60 μm and the purple features are exposed with 30 μm. In this way, it gives higher resolution to the delicate contacts, in additional to also saving exposure time.

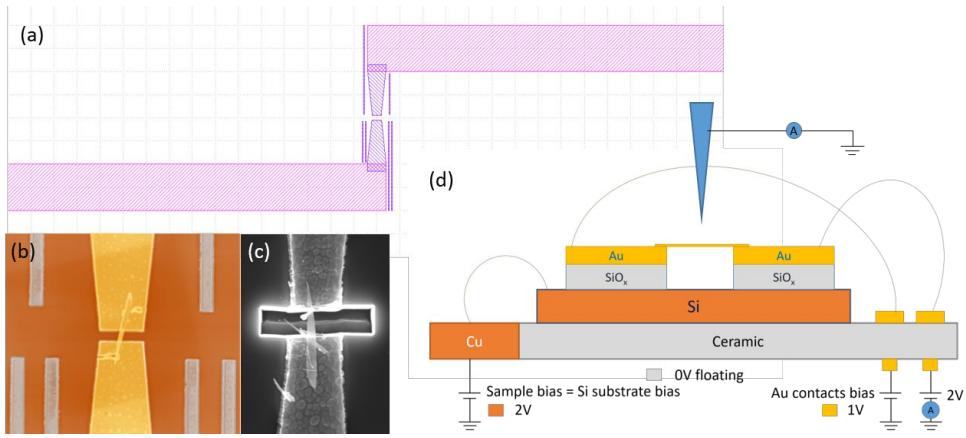


Figure 3-3. (a) Original layout design for the pre-patterned electrodes with thin fingers on the sides, one stripe on the top contact and two stripes at the bottom contact for tip navigation. (b) SEM image of the InAs nanosheet device after fabrication with bias colored map (c) A failure example on fast deposited contact electrodes with bubbles (d) Schematic image of the sample on the low-temperature STM sample holder colored by different biases.

3.2 Surface cleaning and Spin coating

Before EBL, we need to coat a layer of the electron sensitive photoresist. The material used here is a long chain polymer called methyl methacrylate (PMMA), with chemical notation $CH_2=C(CH_3)COOCH_3$. It is a positive photoresistor, meaning the electron beam (E-beam) exposed parts would be dissolved away by the developer. The chain length and the concentrations we used are 950 and A4/A5/A6, depending on the dose factor and expose profile one requires. For example, a thicker PMMA, A6, would give a thicker photoresist layer using the same spin and baking

parameters as an A4 one. Before the spin coating, samples are sonicated in acetone, followed by IPA, for a minute each, after which the sample is annealed on a hotplate at 180°C for 3 minutes. The spin coater parameters are set to accelerate from zero to 4500 RPM in 5 seconds, maintain at 4500 RPM for 60 seconds, and finally decelerate to a halt in 5 seconds. The backside of the substrate will usually have photoresist residues that will cause crucial focus issues during the electron beam lithography. The residues have to be cleaned by acetone carefully after the spin coating, avoiding the acetone come to the front side, to get a flat surface on the back. Otherwise, the residues left at the back (and been baked hard) vary the electron beam focal point over the sample. After the backside gets cleaned, the sample needs to be baked again at 115°C for 6 minutes. The thickness of the backed PMMA can be examined by interferometer, or the datasheet may also be found from the chemical provider. The photoresist of my recipe is around 250 nm, and this needs to be thicker than the total thickness of the aimed deposition materials.

3.3 Electron beam lithography & plasma cleaning

After the backing, the PMMA photoresist layer is dried and stable enough for electron beam lithography. The bonding of the PMMA carbon chain can be changed after decent electron beam dosing. Once the chains are broken, the changed polymer can be removed by immersing first in the solutions of MIBK *(methyl isobutyl ketone)*:IPA(*isopropanol)*=1:3, followed by rinsing in pure IPA.

The EBL process first involved inserting the PMMA coated sample into load-lock, after which the sample was moved into the EBL chamber. After the vacuum set point was being reached, alignment was performed by calibrating the three corners for global coordinate and then focusing the beam roughly to a corner on the substrate. After these steps, we calibrate the beam current using the Faraday cup on the sample holder, the parameters of which can then be used to calibrate the exposure. Dust particles on the substrate surface can then be used to determine optimal beam focus and stigmation, while using a 30 μm aperture, the beam shape can be adjusted by wobbling in X and Y.

The process where the Raith 150 calibrates accurate mechanical stage movement, along with electric field tilt for precise electron beam displacement across a substrate surface is known as a write field alignment. The process starts with course alignment to a dust particle at a lower magnification, where the beam is deflected back from a range of 100 μm. This process is then repeated for 25 μm and 5 μm step sizes, which refines the calibration each time. In the end, the alignment window gives the displacement calibrated values in both X and Y (U and V in the local

coordinate). Smaller values indicate better alignment, and a good alignment typically can give displacement below 3 nm.

After the write field alignment, the previously defined lithography pattern was written by electron beam exposure. The exposure process is associated to the dose factor and exposure calculation. Different photoresists, different feature sizes, and different feature densities all need different exposure parameters. These parameters control the opening time of the shutter a single point, which is calculated by the computer by taking into consideration the E-beam current, area/line/point dosing parameters, and the shape of the pattern. Furthermore, we can set different dose factors for different layers. After the finer structures are exposed, we can change the aperture to 60 μm for all larger features. The benefit of exposing the finer structures first is that once the aperture is changed from a shorter length one to a longer length one, the focus will already be good enough for larger structures.

After the lithography, developing the exposed PMMA part with solutions MIBK:IPA=1:3 for 90 seconds followed by pure IPA for 30 seconds could remove the exposed photoresists. Photoresist residues usually persist even after development, as such, a plasma cleaning process is most often required to remove any such residues, especially around the very fine features. The homemade plasma source is used for 30 seconds. This process can also improve the metal adhesion to the substrate.

3.4 Contact material deposition

There are two evaporators we used for contact electrode deposition: thermal evaporator (AVAC) and electron beam evaporator (Temescal). The first one allows more types of material, such as Au, Al, Ni, NiCr, FeNi, Pd, Zn, Ti, Ge, and SiOx, while the latter one provides a higher vacuum, a cleaner environment, and is more digital/automatic. For the STM devices, we deposited silicon oxides after the EBL pattern in order to insulate the devices from the substrate. Because the silicon oxide source would contaminate the chamber, and because it needs a higher power to melt the rock-like source grains, the AVAC thermal evaporator was instead used for this purpose. To get a homogeneous dielectric layer, a lower deposition rate of around 1-2 Å/s was needed. The SEM image of inhomogeneous contacts deposit above 5 Å/s is shown in Figure 3-3(c), which was proven to have a low resistance of a few kOhm leading to a leak from the top metal electrodes to the Si substrate due to the non-continuous bubble-shape SiO_x layer. The electrical properties of the device cannot be measured if the gate resistance is not higher or at the same level as the nanostructure to be measured. Otherwise, the measured current would be from the

substrate instead of from the nanomaterial under measurement. In the typical cases, the metallic contacts come with Ti or Ni as wetting layer and then Au as metallic electrodes in my recipe, because Ti/Ni adheres much better to the silicon substrate than Au, but oxidize easily due to a higher reactivity, while Au conducts better and can prevent oxidation[50]. Another approach to create the adhesion layer is to use Cr, but Cr can diffuse into Au while annealing the sample[50], [51]. Only a few nanometers, usually 5-10 nm, of wetting layer is needed for adhesion. Below 2 nm could lead to non-continuous islands and thick Ti layer above 20 nm could lead to oxidation from the edges.[52] Here, we deposit 10 nm Ti on top of 150 nm SiO_x for insulation and adhesion, plus a 50 nm Au as the main electrode material. Notice that the total deposition thickness needs to be thinner than the photoresist thickness, which should be considered already before the spin coating process, described in section 3.2.

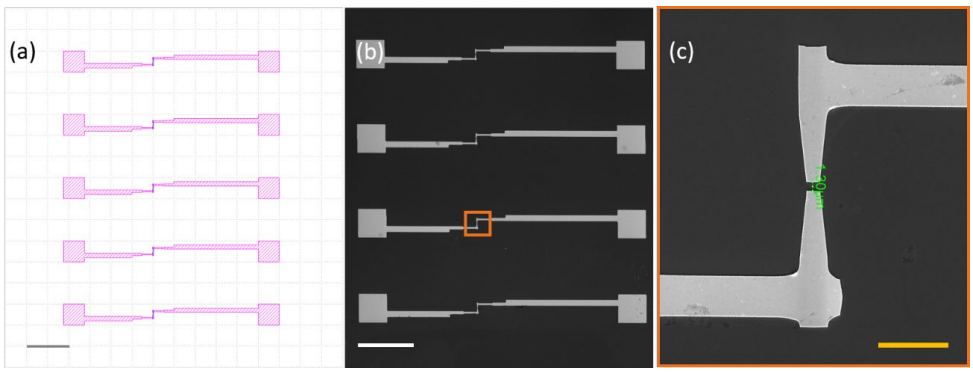


Figure 3-4. (a) Klayout design of the pre-pattern electrodes for devices. The grey scale bar is 200 μm. (b) SEM image of the InAs NW device after deposition. The white scale bar is 200 μm. (c) The finest part of the electrodes for material transfer with a gap of 1.3 μm. The yellow scale bar is 10 μm.

3.5 Nano-material transferring

The FEI-SEM equipment, which is a SEM combined with a focused ion beam (FIB) and a microprobe – Omniprobe, is used for the material transfer. We use the SEM to image the transfer process, which starts from approaching the probe to the NW (as well as nanosheet) on the growth sample (a), breaking down and picking up the NW (b), moving the NW to the pre-pattened contacts (c), and then depositing the NW (d) and the nanosheet (e) down onto device electrodes. The SEM images of the whole process step by step are shown in Fig 3-5. Breaking the NW in the vacuum can make the NW fly away, so a bias applied on the probe could create some charge to enhance the chance that the nano-materials stay on the probe. It is considerably difficult to accurately deposit the nano-materials onto a specific electrode, because

the NWs and the nanosheets prefer to stay on the W probe instead of the Au contacts, so an opposite bias is needed. The voltage we apply to the probe varies on the material, the sample surface and the probe condition. A positive bias between 0.5 V to 1 V is applied to the probe when picking the NW up and a negative bias, within -0.5 V to -1 V, when depositing it onto contacts. It makes the process easier, note that the charging and repulsing mechanism will not be discussed further in this work.

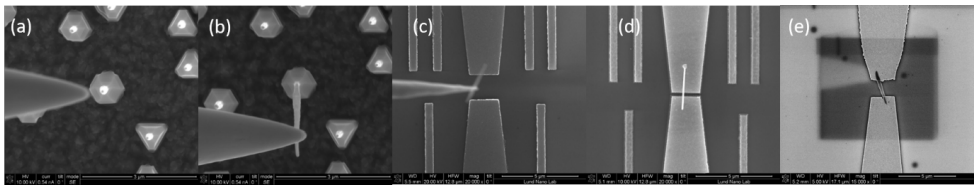


Figure 3-5. The SEM images of the NW transfer process (a) micro-probe approach the standing NW sample (b) get the NW to the probe by breaking down from its feet (c) move the probe to the pre-patterned electrodes (d) deposit the NW down to the electrodes and remove the probe (e) the same process for InAs nanosheet device.

3.6 Atomic hydrogen cleaning

The surface quality of III-V semiconductors is important in defining its optical and electrical properties. However, the surface will never be clean after exposing to the air because the III-V materials get oxidized very quickly. Further, native oxides limit the accessibility to many surface characterization instruments, especially STM. There are many ways to remove native oxides, which include both wet chemistry treatments (e.g. HF, and chalcogenides solutions) and dry treatments (e.g. H-plasma or atomic hydrogen, and ion sputtering). The atomic hydrogen treatment is highly suitable for UHV techniques, because it is done in UHV by annealing the substrate under a flux of atomic hydrogen, so the sample can be directly transferred to the STM chamber or synchrotron end-station chamber for measurements without air exposure. Therefore, the atomic hydrogen cleaning is important and is widely used in this dissertation. The technique is used in LT-STM lateral NW (Paper I), InAs nanosheet device and GaSb NW XPS (Paper IV).

Atomic hydrogen, so called hydrogen radicals, is produced by thermal cracking of hydrogen molecules using a W filament heated to 1700 °C. The hydrogen radicals are extremely unstable, and they are thought to react with the native oxides on the surface of III-V materials (e.g. InAs nanosheet/NWs and GaSb NWs) producing volatile byproducts, such as H_2O or -CH_x. On the material side, the sample heating assists the oxygen of the native oxides to gain higher kinetic energies, and they may react more actively with the hydrogen radicals. This, in turn, enhance the possibility for atomic hydrogen to remove the oxygen. The annealing temperature is important

here, because it must be high enough to make the oxygen removal possible, while also being low enough to not melt any of the nano-structures. Therefore, the cleaning parameters differ according to the material of the samples. Illustration of the atomic hydrogen cleaning for STM measurement is shown in Figure 3-6.

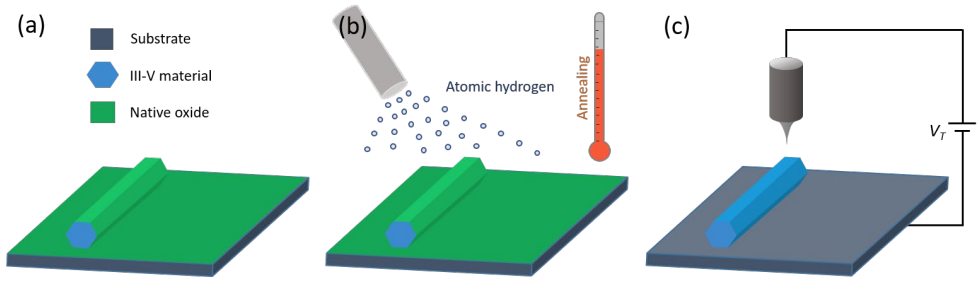


Figure 3-6. Schematic illustration of atomic hydrogen cleaning on III-V NW sample to enable STM measurement (a) a III-V NW sitting on top of a substrate with native oxide covering the surface (b) annealing the sample and exposing it under atomic hydrogen to take the native oxide layer away (c) the surface is now conductive under a tip bias V_T for STM measurement.

3.7 ALD passivation

Atomic layer deposition (ALD) is a technique for Ångström precision thin layer growth. It can be done with various types of materials, for example, oxides (SiO_2, TiO_2, HfO_2 etc.), nitrides (TiN, BN etc.), chalcogenides and organic materials. In this dissertation, I focus on high-k oxides, such as HfO_2 and Al_2O_3. The ALD process consists of two separated half-cycle self-limited gas-solid reactions. A high degree of uniformity and conformity makes ALD suitable to perform on samples of any topology, even samples with complex-geometry. Therefore, ALD has become a primary thin-film growth method in many materials science and technology fields, like the semiconductor industry, solar photovoltaics, and catalysis. For example, ALD is widely used as a high quality high-k material for insulating layer for MOSFET between the semiconductor channel and the metallic gating material. In some special cases, the first ALD cycle is crucial to remove the native oxides on III-V surfaces, especially on InAs, which is known as "*self-cleaning effect*".[53] Here, I use ALD as an interfacial oxide passivation method for removing the native oxide on III-V NWs and making controlled condition of the interface.

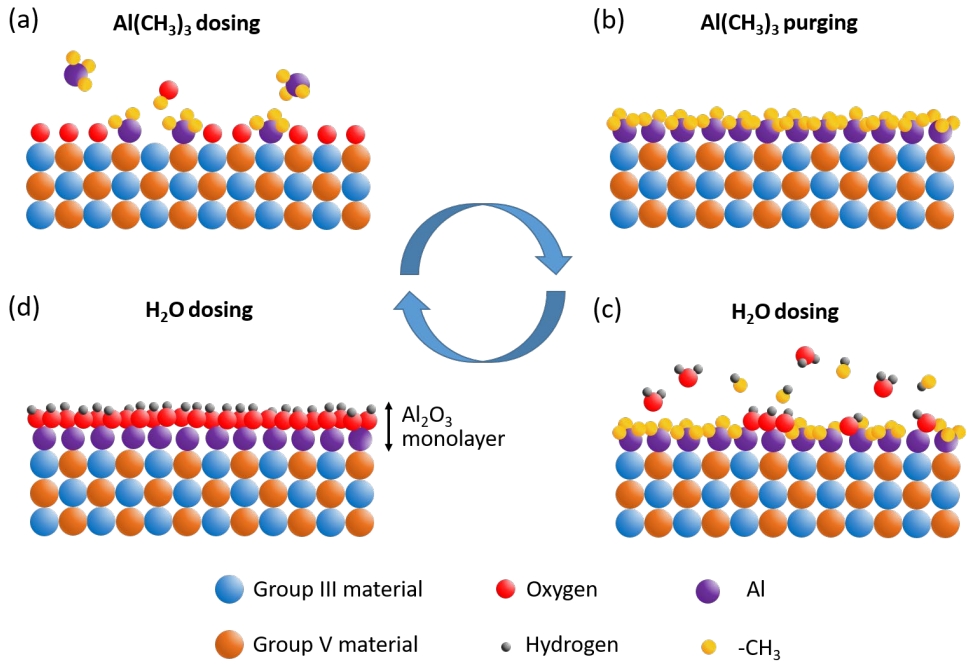


Figure 3-7. Brief illustration of Al_2O_3 ALD process on a III-V substrate. (a) Dosing the metalorganic reactant $Al(CH_3)_3$ to the III-V surface, as the first half-cycle of ALD (b) The metalorganic reactant $Al(CH_3)_3$ is purged, and the $Al(CH_3)_3$ homogeneously bind to the surface. The surface is now ready for the second half-cycle of the ALD process (c) Dosing oxidant reactant, water, replacing $–CH_3$, to form a stable oxide (d) Purging the water to form a uniform oxide layer and complete a full cycle of ALD.

As mentioned above, ALD is an Ångström precise thin film deposition process, which grows one atomic layer at a time by two precursors sequentially dosed to the surface. The two precursors here are first metalorganic compounds and then secondly water, which acts as an oxidizer for the metal, resulting in a high-κ oxide. The metalorganic compounds used in the dissertation are trimethylaluminum (TMA) $Al(CH_3)_3$ for alumina Al_2O_3 ALD in InAs NW device works and tetrakis-dimethylamino hafnium (TDMA-Hf) $Hf(N(CH_3)_2)_4$ in case of hafnia HfO_2 in Paper IV. Due to the self-terminating cycle, meaning that the reactants of the gas phase precursors only incorporate in the surface when the proper reaction sites are available, the thickness of an ALD-grown film is well controlled.

The schematic illustration of one ALD cycle process is shown in Figure 3-7. The first step is to dose the metalorganic compound precursor in gas phase while the sample is annealed in the reactor, then the reactants of the first precursor react with the sample surface, typically leaving volatile products, as shown in Figure 3-7 (a). Once the first precursor uniformly occupied the surface, forming a monolayer, the first half-cycle of an ALD reaction is then done. Before the second half-cycle starts,

a metalorganic compound purge is implemented, as shown in Figure 3-7 (b), making sure that the gas molecules related to the first reactant are completely pumped out and will not cause undesired reactions between the two precursors.

In the second half-cycle, water is dosed into the reactor in gas phase, as shown in Figure 3-7 (c). This oxidizer, H_2O, reacts with the metalorganic precursor covering the surface, exchanging the $-CH_3$ ligand with an -O atom and providing a homogeneous oxide layer (e.g. Al2O3 or HfO2) and organic volatile byproducts. After the second half-cycle, another purge step is practiced, as shown in Figure 3-7 (d). This completes a full ALD cycle, where the number of cycles can be adjusted in order to acquire the required thickness.

The tool that we used to grow the ALD layer of Al_2O_3 and HfO_2 in is a Cambridge Nanotech Savannah 100 reactor. According to Figure 3-7, the thickness of one cycle of a controlled monolayer would be a couple of Ångströms, but in reality, it is approximately 1 Å due to the fact that far less than a monolayer stick to the sample per cycle. The thickness is calibrated by a ten cycles layer sample under XPS study to be around 1 nm from our group. There are more studies support for the same result[54].

3.8 Other sample fabrication examples

The fabrication process can be very flexible depending on the demands. Device fabrication for STM is rather unique, while the typical nano-material transistor fabrication is slightly different. In 3.8.1, an OBIC device fabrication using a typical process is introduced. Other semiconductor devices are used at advanced light sources with a focused X-ray beam. With a 50-100 nm beamsize on nanomaterials, aligning the X-ray beam to the nanoscale sample and further navigating becomes non-trivial work. To offset the difficulty of this measurement during beamtimes, a well-designed lithography pattern can greatly assist in the beam alignment process, increasing the time available for interesting science measurements. Some examples of the lithography patterns are given in section 3.8.2 and 3.8.3. These samples are also commonly used in this dissertation with AFM and STM measurements. Finally, Au on mica is a helpful sample to conditioning the STM tip, and the fabrication of this is mentioned in section 3.8.4.

3.8.1 OBIC SGM devices

Due to the fact that the SGM measurement do not require a complete conductive surface, the device is fabricated in a simpler way. A 25-set large lithography pattern,

shown in Figure 3-8 (a), on the substrate consisting of markers, electrodes and bonding pads (originally designed by C. Thelander). Firstly, the NWs are mechanically deposited from growth substrate to a n-type Si substrate with a grown layer of 100 nm SiO_2 for electrical insulation. Then, EBL followed by metal evaporation of 25 nm Ni and 75 nm Au were performed for electrically contacting the specific NWs. The device image is shown in Figure 3-8 (a).

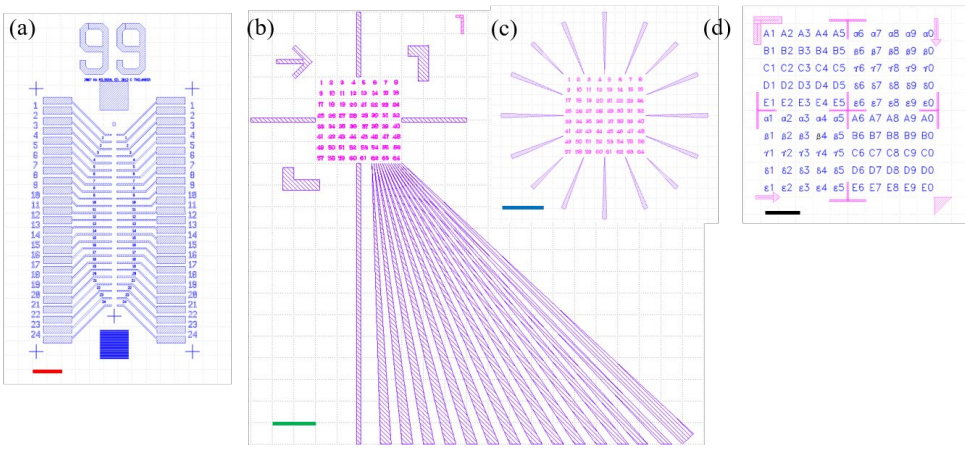


Figure 3-8. (a) Standard device design, the red scale bar is 400 µm (b) InGaN depostion pattern, the green scale bar is 20 µm (c) siemens star, the blue scale bar is 20 µm (d) Elettra SPEM design, the black scale bar is 100 µm.

3.8.2 Hard X-ray nano beam combined conductive AFM samples

The objective here is to observe the crystal flexo-photovoltaic (FPV) effect[55], and we performed the measurements on $SrTiO_3$ (STO) crystals and InGaN pyramids in two individual beamtimes at P10, DESY, Germany and NanoMAX, MAX IV, Sweden. The FPV effect[55], [56] was observed by a photovoltaic current generated in a bulk $SrTiO_3$ crystal by illuminating the area of local indentation with a visible light laser (405 nm wavelength) where the indentation breaks the symmetry of the material inducing the local bulk photovoltaic effect. The illustration of the FPV experiment is shown in 3-9 (a).

In DESY P10, we performed in-situ nano-indentation experiment by combining conductive atomic force microscopy (AFM) and Bragg coherent diffractive imaging (CDI) on a single STO sub-micron crystals, as shown in Figure 3-9 (b). A similar measurement on InGaN pyramids was performed in NanoMAX with an improved pattern, the design of Figure 3-8 (b), for better visualization by the cameras at beamlines and direct indication for orientation. The crystals were placed by Omniprobe as described in Chapter 2 and the patterns were deposited with 10 nm

Ti and 50 nm Au. The same transfer process was again used here, as shown in Figure 3-9 (c). It worth mentioning that the consumption of the Omniprobe is much higher than making the NW devices, because the nitride crystals are much harder and well attached on the substrate. However, less crystalline distortion would be expected in this case. To make the pyramids adhere well on the gold pattern during sample transport, mounting on the beamline, and scanning under AFM, we anneal the sample to 500 °C for 10 minutes to glue them on.

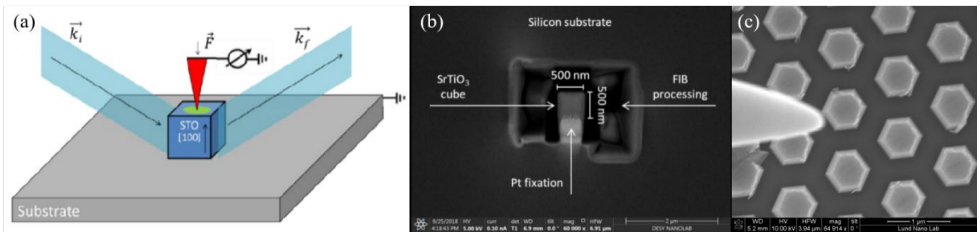


Figure 3-9. Experimental schematic and samples of flexo-photovoltaic measurements. Figure courtesy by [57]. (a) Mechanism illustration of the FPV effect beamtime idea (b) STO crystal sample preparation in the Omniprobe combined FIB-SEM instrument (c) SEM image of the transfer process of InGaN pyramids.

3.8.3 Navigation patterns for synchrotron measurements

A PEEM measurement on the graphene/InAs NW sample in the Paper VI performed at MaxPEEM requires pre-patterned markers for overview and navigation, and the Figure 3-8 (a) pattern with 25 sets electrodes was used in this measurement. As Figure 1 (c) in the Paper VI, the secondary electron XPEEM images show good contrast for further investigations. Further useful pattern for scanning Photoelectron microscopy (SPEM) on InAs nanoflakes with Bi deposition performing at Elettra is shown in Figure 3-8 (d) that divides the area into four regions, A to E in left upper and right lower with numbers 1 to 5 and 6 to 0, respectively, while α, β, γ, δ, ε on right upper and left lower with numbers 6 to 0 and 1 to 5, respectively. Both the sample markers are with 10 nm Ti and 50 nm Au.

3.8.4 Au 111 surface

Au on mica sample is helpful for STM tip conditioning, but more importantly, it can be used to see how good the tip condition is in by looking at the herringbone reconstruction of a Au surface. Therefore, making a high-quality surface reconstruction in 111 at atomic scale is critical. Mica is used here for reshaping the crystalline of Au due to its well-matched FCC crystal structure and the layered structure for easily peeling fresh surface.[58] Freshly peeled mica by Scotch tape in clean room with a complete flat layer is appreciate, and then we anneal the mica to

120°C during Au deposition. The deposition rate is crucial here and we keep it at 0.5 Å/s during the process.[59] After the deposition, a delayed switching-off crystal cooling and venting was conducted. The sample then needed to be annealed in ultra-high vacuum (we perform the annealing in our STM preparation chamber at low 10^{-10} mbar) to 300°C for 12 hours for well-structured crystallization and then shortly ramp up to 500°C for 10 minutes. The samples are examined by the STM showing herringbone reconstruction and by LEED showing the same pattern as a bulk Au (111) cube.

Chapter 4:
Scanning Tunneling Microscopy and Spectroscopy

Most of the research topics in this thesis include the use of Scanning Probe Microscopy (SPM) on the surface of the NWs or nanosheets. The surface morphology and chemistry have high influence on the device functionality and efficiency. Here comes an example from $In_xGa_{1-x}As$ lateral NWs (Paper I) for quantum computing device, where the surface properties, in this case, the surface reconstruction (which implies specific electronic properties), may restrain the electron transport from the semiconducting NW to a superconductor. The surface Local Density of States (LDOS) and the surface band gap are an important point for observing detailed quantum effects[60]. Further, the doping and defects, for example, on InAs-GaSb tunneling FET (tFET) NWs, have significant impacts on the device efficiency.[61] STM/S techniques have the advantage of studying the atomic level surface properties in regards to both geometric and electronic structure.

The typical way for us to study a device by SPM starts with an AFM surface overview investigating in a larger range, and then we use STM/S to study the surface morphology and its electrical properties down to atomic resolution (Ångström length scale). Both AFM and STM/S are important, since AFM gives us an overview of device geometry and proves whether the surface is sufficiently flat and clean (e.g. from organic contamination from the processing) to perform STM in UHV without the risk of damaging the tip. Briefly, AFM is a fine technique for monitoring the topography from tens of μm to a few nm and can work on many different types of surfaces, e.g., conducting/insulating surfaces and even soft matter. STM usually gives even higher resolution allowing to see the atoms; however, it usually needs UHV conditions. The limitation for STM is that it works only on conductive surfaces. In this chapter, we focus on STM/S and we will give further details of AFM in Chapter 5. STM theory and the surface imaging technique are introduced in section 4.1, while STS, the investigation of electronic properties, is introduced in 4.2. For obtaining higher quality images and further information, technical issues, including vacuum condition, tip preparation, low-temperature STM (LT-STM), and

electrical characterization, are introduced in 4.3. How the techniques can then be applied to an electrically functioning nano-device with its own electrical leads is then presented in 4.4.

4.1 Scanning Tunneling Microscopy

An STM is an instrument using tunneling currents between an electrically biased sharp metallic tip and a conductive sample to investigate both geometric and electronic surface properties down to atomic level. The technique was invented by Binning and Rohrer in 1982 at IBM Zurich, and they were awarded the Nobel Prize in Physics for their invention of STM in 1986. The physical principles of STM were based on the quantum mechanical tunneling effect, in which an electron can act like a wave-function, propagating through a potential barrier with a finite probability even when the barrier height is higher than the kinetic energy of the electron.

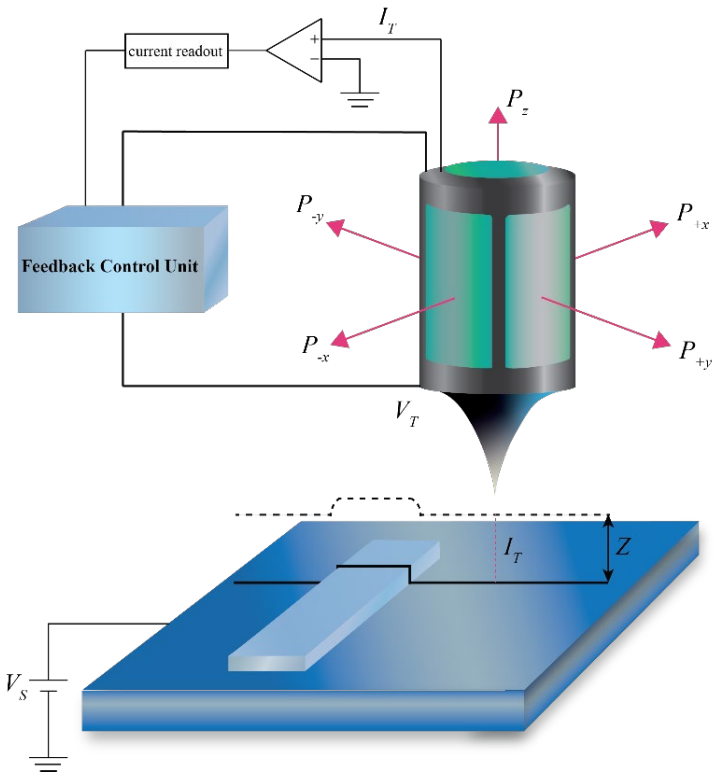


Figure 4-1. Schematic diagram of the STM experiment showing sample bias Vs, tunneling current I_T, tip-sample distance Z, piezo stage in X, Y and Z directions and a feedback control unit. The dashed black line shows the STM scan profile convoluting the topography and the tip shape over the step structure on a flat surface, while the solid black line shows the projected profile of the tip movement path.

The setup of an STM consists of an atomically sharp metal tip, usually W or Ir/Pt. A bias V_S is applied between the tip and the sample, which allows the electron tunneling effect to be measured when the tip is approached close enough to the metal or semiconducting surface (typically < 1 nm). The approach is done using piezo motors with a feedback control. The default bias in this thesis is set on the sample, V_S. However, depending on the setup, one can also apply a bias (see Figure 4-1) to the tip, V_T. As a result, for the actual tunneling potential, the relative potential between the sample and the tip may need to be considered carefully, especially when the sample structure becomes complex and voltages are applied to it. An illustration of the STM setup is shown in Figure 4-1. The pre-amplifier measures the tunneling current I_T through the tip and sample, and it is exponentially depending on the tip-sample separation a. The I_T can be expressed by the formula:

$$I_T \propto e^{(-2a\kappa)}$$

Equation 4- 1

, where κ is the wave vector of the electron wave function,

$$\kappa = \sqrt{\frac{2m}{\hbar^2}(V_o - V_S)} = \hbar^{-1}(2m\phi)^{\frac{1}{2}}$$

Equation 4- 2

, where m is the effective electron mass, ħ is the Planck's constant, V_o is the barrier height ,V_S is the sample bias, and ϕ is the effective local work function.

The tunneling current is quantum mechanics corresponding to that the electron is regarded as a wave function—having a distribution in space—which may propagate through sufficiently thin barriers, which is not valid in classical mechanics. The barrier here is created by vacuum and the width is determined by the distance between the STM tip and the investigated sample. With sufficiently small distances, the wave functions of electronic states at the surfaces of tip and sample may overlap, and it leads to a non-zero interaction probability of the tip and sample states, which allows electrons shifting from one object to the other. An expression for the tunneling current was developed by Bardeen[62] that the tunneling probability for an electron to tunnel between the tip and the sample, T, can be expressed by Fermi's golden rule:

$$T = \frac{2\pi}{\hbar}\left|M_{i,f}\right|^2 \delta\left(E_i - E_f\right),$$

Equation 4- 3

Where the $\delta(E_i - E_f)$ function states that the tunneling possibility between the initial state E_i and the final state E_f is non-zero for the same energy electronic states. The tunneling matrix, $M_{i,f}$, between the initial state E_i and the final state E_f can be expressed as an integration function:

$$M_{i,f} = -\frac{\hbar^2}{2m}\int \left(\psi_i \nabla\psi_f - \psi_f \nabla\psi_i{}^*\right) dS,$$

Equation 4- 4

Where S is an arbitrary surface, ψ_i and ψ_f are the wave functions of the initial state and final state, $\psi_i{}^*$ is the complex conjugate of the initial state wave function, and *m* is the electronic mass.

Using Bardeen's expression for the tunneling matrix, the tunneling current, I_T, can be described using first-order perturbation theory[63]:

$$I_T = \frac{2\pi e}{\hbar}\sum_{i,f} f(E_i)[1 - f(E_F + eV_S)]\left|M_{i,f}\right|^2 \delta(E_i - E_f)$$

Equation 4- 5

where $f(E)$ is the Fermi distribution function, and E_F is the Fermi level. Here, equation 4-5 implies that tunneling occurs from occupied to empty electronic states, but $M_{i,f}$ is unknown in most of the cases. There are some conditions needed to be assumed to relate the tunneling current to the sample properties: 1) a geometrically symmetric and electronically isotropic tip apex and 2) an s-like wave function that is dominating the tunneling current. By these assumptions Tersoff and Hamann showed that the tunneling current is proportional to the integrated DOS in an energy interval between the Fermi level, E_F, and $E_F + eV_S$ at a position $\vec{r}$ of the tip[64]:

$$I_T \propto \rho_{tip}\int_{E_f=0}^{eV_S} \rho_{sample,L}(\vec{r}, E_F + \varepsilon) d\varepsilon$$

Equation 4- 6

where ρ_{tip} is the local density of states (LDOS) of the tip apex and $\rho_{sample,L}$ is the LDOS of the sample at a position $\vec{r}$ and energy ε.

Using theoretical derivation for relation between the tunneling current and the LDOS, let us move forward to the experimental procedure on STM imaging. In constant current mode, a feedback control adjusts the height between the sample and the tip to keep the tunneling current I_T as close as possible to the set point current I_{set} while the tip is scanning on the surface. The corresponding height-change

sensitivity and speed should depend on the surface morphology: The proportional gain (m/A) sets the feedback for how the distance the tip needs to move by the tunneling current change. The integral gain (m/A/s) states how fast the feedback loop reacts. In an atomically resolved STM image, the contrast shows the atom positions relating to the wave function overlapping - local variations in the LDOS of the sample, which is the main contrast mechanism. A larger number of states will result in an increased tunneling current and thus show up as a brighter area in the STM image and vice versa for dark areas.

For equation 4-5, we also see that only states in the energy range of $E_F + eV_S$ contribute to the tunneling, which can be illustrated as in Figure 4-2, such that empty states (b) and filled states (c) are imaged separately depending on the polarity of the applied bias, V_S. Therefore, the brighter and dark areas in polarity dependent STM images can tell more than the states, which is especially meaningful to the type of elements in the III-V system. Based on sample biasing, the STM resolve more clearly on III atoms with positive sample bias and V atoms with negative sample bias, because the filled and empty states are localized at the group V and III atoms, respectively. More discussions about the device sample bias are in 4.4.

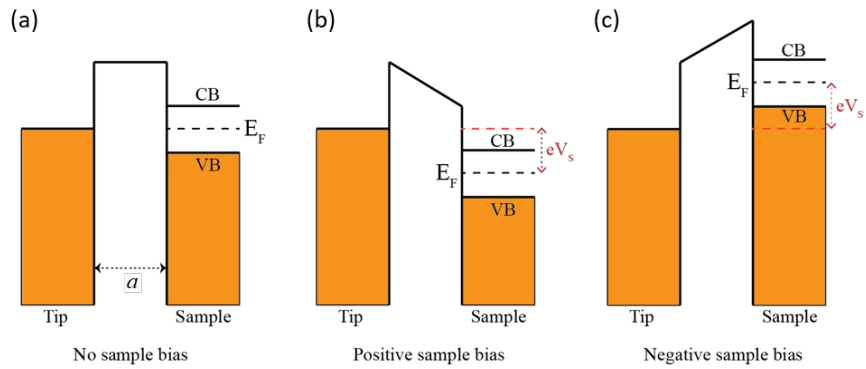


Figure 4-2. Band diagram of the STM tip and sample under the sample bias case (a) Fermi level aligned after the tip approached to the sample surface without bias (b) band energy shifted with positive sample bias (c) band energy shifted with negative sample bias.

However, the interpretation is based on the assumption that the tip geometry and tip electronic configuration can be ignored, for example, the LDOS of the tip apex, ρ_{tip}, is independent with respect to V_S because the tip material (usually metals) have an approximately constant LDOS near the Fermi level, E_F. In reality, the image contrast depends not only on the LDOS of the sample but also the tip. The LDOS of the tip is often neglected because the same part of the tip is always used for tunneling on a flat surface. However, a different part of the tip can be used for tunneling if the

surface variation is larger than the variation of the tip geometry, and hence a change in the tip apex geometry could result in an altered contrast pattern. e.g., an asymmetric tip scanning on lateral NW facets. Also, the electronic configuration of the outermost atom of the tip apex could be changed, for instance, an s-orbit assumed in the Tersoff-Hamman approximation could change to a p-orbit, which could result in different states being probed. Not only geometry but also the chemistry of the tip can be different if an adatom from the surface or a molecule from the chamber adsorb on the tip apex. The tip LDOS is then different from the ideal model and if the specific atom is not metallic, ρ_{tip}won't be a constant and the influence to the contrast behavior would be significant. This is the important reason for keeping the same tip condition when performing atomic resolution imaging and STS, especially crucial for measuring relative changes on the devices.

4.2 Scanning Tunneling Spectroscopy

Both the topography and electronic properties of a sample can be acquired simultaneously with a combined STM and STS, which could characterize surface electronic properties of nanostructures, such as bandgaps[65]–[67], surface defects[68], [69], and quantum phenomena[70]–[72] on semiconductors. From the tunneling theory, we learn how the tunneling current depends on an external bias V_S, ρ_{tip} and ρ_{sample}, and V_S is applied at a fixed bias for consistent data for STM images. The STS measurement can study local (Ångstrom) electronic properties by ramping the applied bias, V (it is the simplified expression of V_S), and meanwhile reading out the LDOS of the sample by measuring *dI/dV*.[73], [74]. The theory of STS, including the *dI/dV* formula and tip-induced band bending (TIBB), will be introduced in this sub-chapter.

The reason to measure the differential conductance *dI/dV* is that the *dI/dV* is proportional to the sample LDOS: In equation 4-6, the tunneling current I_T is equal to the integrated density of states of tip ρ_{tip} and a position $\vec{r}$ related density of states of sample $\rho_{sample,L}(\vec{r}, E_F + \varepsilon)$. While performing STS, the tip is sitting at a fixed position instead of scanning, so the sample DOS at the same position should be the same, hence the sample LDOS ρ_{sample} can be expressed without position variation in STS. Here, the ρ_{tip} is assumed to be a constant because the density of states of a metal (tip material) below the Fermi level are uniform, which can be neglected, so the equation becomes:

$$I_T \propto \int \rho_{sample} dV$$

Equation 4- 7

In other word, I_T is proportional to the integration part. Now, if we differentiate dV on both sides of the equation, we get that the dI_T/dV is proportional to the density of state of the sample.

$$\frac{dI_T}{dV} \propto \rho_{sample}$$

Equation 4- 8

dI_T/dV now reflects the ρ_{sample} directly. However, even if we do not move the tip, it is important to still evaluate the LDOS of the sample at the position of the tip, $\rho_{sample,L}(\vec{r})$, since this includes the exponential distance dependence. Since the tunneling current also depend exponentially to the tip-sample distance (equation 4.1), this will make it more difficult to only observe the LDOS. To remove this dependence to the first order, we use the conductance normalized *dI/dV*, that is *(dI/dV)/($\overline{I/V}$)*, which gives a more clear electronic band information around the fermi level.[75]

On the technical side, the *dI/dV* can be obtained from a lock-in amplifier, which gives a small voltage oscillation on top of the STS sweeping voltage and records the current only with the same frequency as the small voltage oscillation, so that the differentiated value *dI/dV* could be acquired and low noise on the STS could be achieved thanks to the lock-in amplifier playing a role as a frequency filter.

Tip induced band bending

When analyzing the *(dI/dV)/($\overline{I/V}$)* data for semiconductors, the measured bandgap is usually somewhat higher than the nominal bandgap of the material. This is due to tip induced band bending (TIBB). The TIBB phenomenon is caused by the applied tip–sample voltage which drops in the sample close to the surface, as a dielectric impedance, instead of only across the tunneling barrier. The surface impedance then causes bending of semiconductor bands because of energy pinning effect, changing the band gap of the spectra effectively compared to the corresponding bulk value. There are many parameters that determine TIBB, for example, Fermi level, tip-sample separation, tip radius, applied voltage, tip work function ϕ_t, sample carrier concentration and electron affinity χ_s[76]. It is worth mentioning that the tip work function, among others, is mainly determined by the material used and the shape of the tip apex, making it the hardest parameter to determine, as it is difficult to know the real tip apex during the scanning. To characterize only the sample properties

without being interfered by the tip, only spectra obtained using the same tip in the same measurement run on the same crystal facet can be directly compared.

This effect is illustrated in Figure 4-3 for a low-doped semiconductor and metallic tip. The TIBB behaves differently depending on the polarity of the tip–sample bias, curving upwards with positive sample voltages and downwards with negative voltages, as shown in Figure 4-3 (b) and (d), respectively. For a moderate positive bias scenario as in Figure 4-3 (b), electrons can tunnel from the tip to the empty states in the sample conduction band. If one keeps increasing positive voltage, the band bending becomes large enough that the valence band states at the surface are above the Fermi level, as shown in Figure 4-3 (c). In this case, tunneling can occur in both conduction band and valence band, and the top part of the valence band is lifted above the Fermi level becoming empty states.

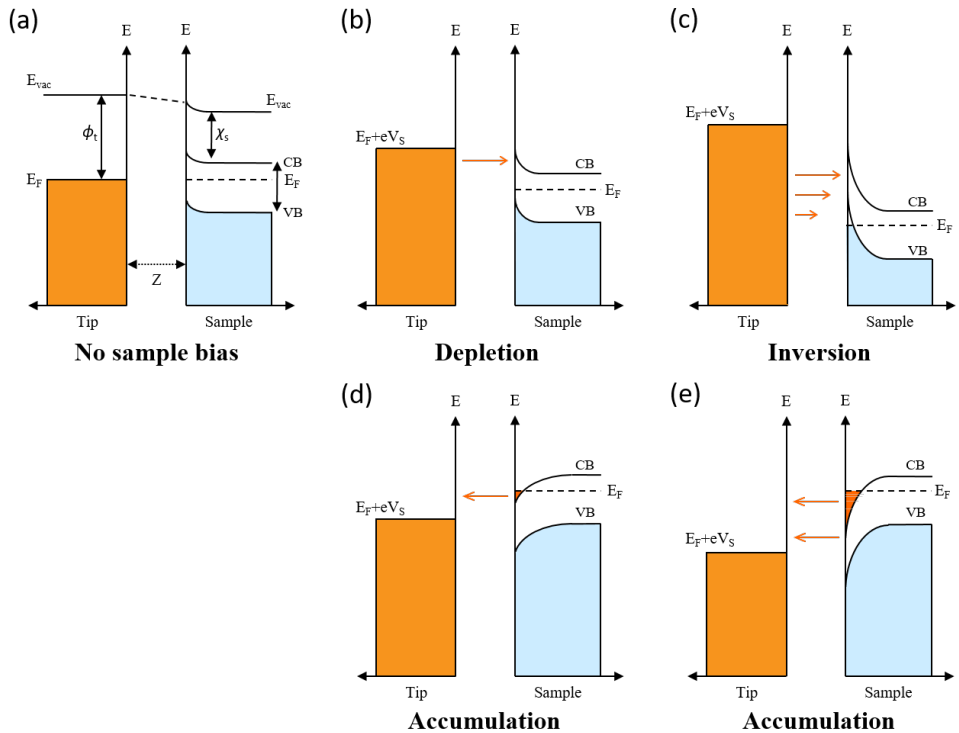


Figure 4-3. TIBB with different sample bias situations: (a) with no bias. (b) and (c) are with positive bias in the case of depletion and inversion, respectively. (d) and (e) are with negative bias in the case of accumulation.

Opposite to depletion, electrons can tunnel from the conduction band to the tip with a proper negative sample bias applied, as shown in Figure 4-3 (d). The negative bias,

leading to the conduction band at the surface bending below E_F, causes more electrons accumulating at the surface. With a higher negative bias, electrons are allowed to tunnel to the empty states of the tip from the accumulation states as well as the valence band. There could even be a chance that the electrons will be trapped at confined states induced by TIBB, causing tip-induced QDs[77], [78].

To estimate the absolute energies for features within a spectrum, like band edges and quantum states, a calibration with a 3D Poisson solver model[60][73][74] uses parameters like tip–sample separation, tip radius, tip and sample work function, sample carrier concentration, and carrier effective masses. I have used the SEMITIP software[80], developed by R. M. Feenstra, for interpreting the results and aiding discussions in Paper I. As mentioned above, TIBB modeling requires information regarding the tip characteristics, such as its shape and work function, unless only comparing the spectra performed by the same tip in the same measurement. The TIBB modeling software can then also be used to interpret the tip shapes, surface states.

4.3 Instrument description

The tunneling properties and the surface cleanliness depend on the environmental condition, especially the vacuum, tip profile and low temperature. Several techniques will be introduced in this section: 1) ultra-high vacuum (UHV) 2) STM tip preparation 3) Low-temperature STM 4) electrical measurement system. If there are many gas molecules or ions, the deionization and electrolysis processes limit the surface preparation that requires UHV. Further, after the surface is cleaned and stabilized, remaining UHV is crucial. The importance of the tip condition is another key, which is discussed in Chapter 4.1 and 4.2. There are clear benefits in low temperature environment for STM/S, as described below. Last, the electrical measurement system for combining the device measurement to the STM will also be introduced.

Ultra high vacuum

For a good working environment for STM and maintaining the surface cleanliness, the chamber pressure must be in UHV range (lower than 1×10^{-9} mbar). In theory, 1×10^{-9} mbar can only keep the surface clean for less than 1 hour before a monolayer gas molecule adsorbs on top according to the ideal gases law $nk_BT = PV$, where P is the pressure, V the volume, T the temperature, k_B the Boltzmann constant, and n the number of molecules. Each residual gas molecule in average bounces once on the sample surface every second at a pressure of 1×10^{-6} mbar. Luckily, in most cases, the gas molecule is not adsorbed, i.e. the sticking coefficient of the samples is low

and so it will not lead to surface oxidation or contamination. Surface molecular condensation can be an issue a low temperature, since the cold parts in LT-STM act like a cryopump which traps the rest gas molecules to the cold surface, thus keeping a good vacuum. The lateral NW work in Paper I with atomic resolution was performed in UHV with high 10^{-11} mbar to keep the surface clean and stable.

Tip Preparation

The STM image quality highly depends on the tip. Sharp tip apex gives good condition for single-point tunneling. There are two types of tip materials used in my research:

Tungsten (W) and platinum/iridium (Pt/Ir)[81]. For LT-STM in UHV, we use W wire, one of the hardest and stable materials, which is etched into tip shape with an electrochemical etching method by an Omicron DC electrochemical tip etching system using 9 V and a threshold current of 3.5 mA. 0.3 mm diameter polycrystalline W wire is used as an anode and a stainless-steel ring acts as the cathode in the solution of sodium hydroxide (NaOH, 2 mol/liter). The individual chemical formulas for both cathode and anode of the process are shown below:

Cathode: $6H_2O + 6e^- \rightarrow 3H_2\ (gas) + 6OH^-$

Anode: $W + 8OH^- \rightarrow WO_4^{2-} + 4H_2O + 6e^-$

Then the overall formula is simplified to:

Overall: $W + 2OH^- + 2H_2O \rightarrow 3H_2\ (gas) + WO_4^{2-}$

The process at the anode creates volatile WO_4^{2-}, thus being etched away from the W wire. The W wire at the electrolyte/air interface would be etched sophisticatedly following the profile shape due to the surface tension effect, and hereafter being cut into an extremely sharp tip. Then the tip needs to be immersed into distilled (DI) water and ethanol to take the etchant residues off. There will be residues, surface contaminations and even a thin layer of oxide on a freshly etched tip surface, therefore, removing them will take place after inserting the tip into vacuum. Two different types of tip cleaning are used in our STMs. Firstly, argon (Ar^+) sputtering of the tip for 20 minutes at a pressure of 2×10^{-5} mbar at argon gun acceleration voltage 3 kV and an emission current of 20 mA. The other method is to anneal the tip by applying a direct electric current through. There is a spring touching at a higher position of the W wire applying a voltage, and the tip holder at a lower side connects to the ground to form a circuit. Once the tip is heated to around 1075K (glowing in orange by experience) for a couple of seconds, tungsten oxide sited on the tip will sublimate.[82], [83]

Low-Temperature STM

The closed cycle LT-STM in our lab is a type of variable temperature (VT-) STM integrated with a thermal cooling tower, which is cooled down by a closed-cycle Helium cryostat which keeps the system at around 9K during the scanning. A preparation chamber connected to the analyzing chamber has a tip annealing stage, a Hydrogen cleaning cracker, an Argon sputter gun and a sample heating stage.

One of the benefits of low temperature is a low atom diffusion mobility that makes for high-quality imaging on a stable surface. Thermal drift due to temperature variations can be a difficult issue for atomic resolution imaging. The image can be distorted and the relative position between the tip and the sample will not be constant. Typical drift velocities, mostly in X and Y axis, at room temperature are up to several nm/min, while at low temperatures, drift rates as small as a few Å/hr are obtained.[84] More than STM, the low temperature helps with STS measurement significantly, because drift in Z is much more severe when the feedback is turned off. The central benefit of low temperature, however, is that more detailed STS spectra can be found, resolving features smeared out at room temperature. Some states can only be observed at low temperature, e.g., sub-band splitting and quantum effects.

Beside all the advantages of LT-STM, one drawback is that the extension range of the piezo materials are shortened, and the scanning range is extremely important for navigating the tip to a specific device of a few μm over the sample in several mm range. The scanning range of the piezo in x, y direction is around 2 μm in our LT-STM, while it is around 20 μm for our room temperature STM. A careful step-size calibration in X and Y is crucially needed for LT-STM when it comes to navigation on nano-device samples. The navigation process and details are introduced in section 4.4.

Electrical characterization system for the LT-STM

There are separate electrical connections to the sample holder in the STM stage, which can be connected to device on the sample holder, providing extra potentials in addition to the bias voltage between sample and tip. Such electrical connections are not standard for STMs. A special LT-STM sample holder has 10 screw pins, thereafter wire bonded to the device samples, as shown in Figure 4-5 (d), to make electrical contacts, electrically connecting the electrodes of the device to an external measurement box. An extra 10-channel electrical grounding box is self-made here to safely connect the extra contacts on the sample holder to external equipment (power supply, amperemeter, etc.) while taking special care of the very sensitive nanostructure devices, in order not to destroy them by charge spikes. Thus, with such a 10-channels system, if one device fails to work, the measurement can move on to the neighbor devices, instead of taking the sample out, exposing to air, wire-

bonding, pumping, atomic Hydrogen cleaning and then moving the device into the STM chamber and cooling down again.

One of the most important reasons to do electrical characterization at low temperature is that some quantum states appear at the band edges with a current in tens of pA at low bias; therefore, an electronic system with low-noise and high resolution with a high sensitivity is important. Our setup includes power supplies, Keithley 2401 and Yokogawa GS200, a current amplifier, SRS 570, and a digital readout, HP 3410A, which are connected via National Instrument GPIB interface and controlled by a LabView program for typical III-V NW and nanosheet device studies. Keithley 2401 is an useful power source because the output current can be read out simultaneously to understand the device leaking condition. Further, a compliance, current limit, can be set to protect the devices. This electrical measurement system is broadly used in my research. One exception is that if switching is faster than the maximum sampling rate of Keithley 2401, 400 Hz, a higher sampling rate electronic is needed for this. Here, an Agilent B2910A with sampling rate 100,000 Hz, 10 μs/point, is used.

4.4 STM on nano-devices

Calibration of the piezo motor

In order to find the nano-device on the sample, we first need to calibrate the movement of the piezo stage. We use the edge of the Au electrode to calibrate the movement of the piezo stage in four directions, +x, -x, +y and –y. Each direction has a step size ranging between 203 nm to 262 nm. The calibration is performed when the stage is completely cooled down and the temperature is steady at around 10K. With the calibration values, the movement would be much easier. For example, if one needs to move 4 μm in –y according to the layout design and one step in –y is around 224 nm, 18 steps on the correct direction would bring the tip to the desired position. However, the x and y directions of the sample are not aligned to the x and y directions of the piezo. Even though one could mount the sample orientation as best as possible, there are still many other things to be considered while mounting the sample, for instance, the maximum piezo scanning range, the wire-bonding pads orientation, and no wire on top of the device for space running the STM. Therefore, patience and carefulness have higher impact on the device navigation.

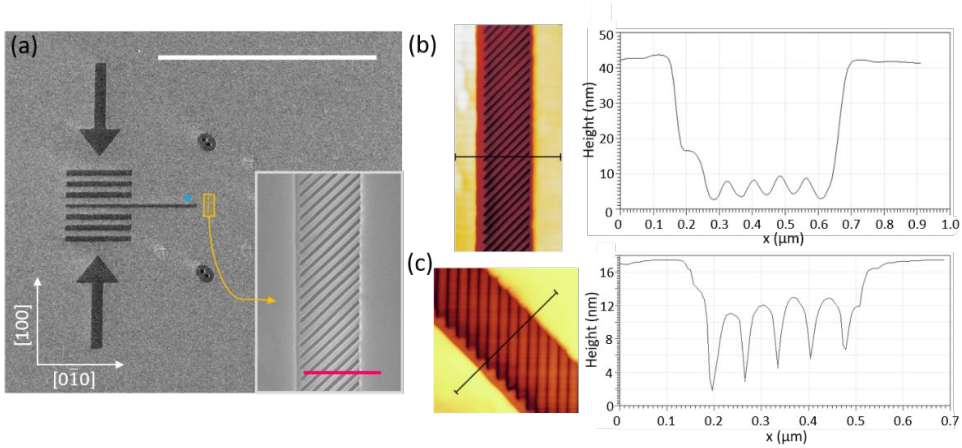


Figure 4-4. (a) SEM image of the sample with navigation marker patterns. The length of the white scale bar is 200 μm. The inset shows the zoomed in image from the yellow rectangle, where the NWs are grown. The length of the pink scale bar is 500 nm. (b) AFM image and its scan profile of the whole device. (c) STM image and its scan profile of the same area with a 40° rotation.

Device navigation

Then we can move toward the nano-device structure based on the device layout. It is worth mentioning that we usually pattern navigation markers in the layout design, for example, the strip-like markers made of Ti shown in the lateral NW SEM image of Figure 4-4 (a). We followed the center stripe, the thinnest and longest one, to approach the lateral NW region, as shown in Figure 4-4 (b) and (c). Another example, the thin finger features next to the source-drain electrodes, shown in Figure 4-5 (a), can tell on which electrode the tip is scanning on by the number, one or two, of the finger features. The features help the navigation to the nano-device that we aim to study, but there is a lesson that we have learned during the experiments: The finger markers are deposited together with the electrodes, which are isolated to the substrate by a 200 nm SiO_2 layer. Therefore, the small finger features, without a bonding pad, need extra wire-bonding to electrical channels to be biased; otherwise, they are floating. In this case, once the tip scans over them, no electrical circuit can be formed, so the STM feedback control will approach the tip into the sample and cause crash. This is the reason why we removed the finger features in a later version of the sample design. The bias diagrams for navigating and scanning on top of the nano-material are shown in the Figure 4-5 (b) and (c). We intend to keep the device material in pristine status without activation and observe the surface topography before the device is operated, so that both contacts have to be kept at the same bias during navigation and the pristine scan. A potential difference between the tip and the sample has to be applied in order to detect tunneling current. We connected our LT-STM to the sample bias, so we can avoid the device current leaking issue

causing STM problems. If we swap the cables of the STM to tip bias configuration, the tunneling current will be ending up at different channels on the 10-channel grounding box, which increases the complexity of the measurement. Once we reach the NW/nanosheet material, the atomic scale condition surface can be observed, and then we can vary the potential difference between the contacts. The lower voltage here has to be biased above a certain value, so there will still be enough potential between the tip to the lower voltage contact to keep the tunneling current running. For instance, if we know a stable tunneling current on the InAs NW can be achieved at 1V and we would like to apply 1 V to the device, then 1 V is the minimum on the lower bias contact and 2 V would be the applied voltage for the other contact, as shown in Figure 4-5 (c).

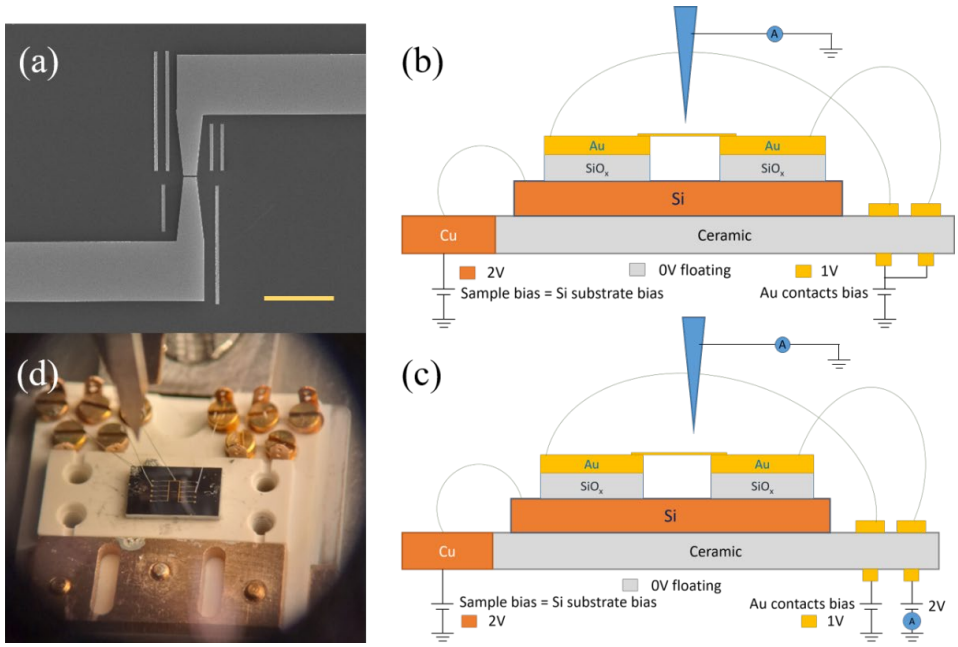


Figure 4-5. (a) Pre-patterned device electrodes with thin finger stripes for navigation. Yellow scale bar is 10 μm (b) STM sample biasing geometry during the STM navigation and (c) STM sample biasing geometry during device operation. (d) Devices in a chip mounted on a sample holder with wire bonding electrically connected to the separate electrical connections, the golden screw pins on the upper part of the photo, on the LT-STM sample holder. The image is taken under the optical microscopy of a wire bonding machine.

Chapter 5:
Combining Laser Excitation and Scanning Gate Microscopy

While studying the devices with the scanning probe techniques, lighting for navigation is required. Light sensitive properties of many III-V materials make the device measurement interesting and tricky, and optical memory effects were seen on both InAs NW and nanosheet devices. To study the light influence on the III-V NWs more systematically, we combine laser and LED sources with our AFM setup to study the optical and electrical effects simultaneously. The AFM technique is introduced in 5.1. If a conductive AFM tip scans over the NW device it works as a mobile gate and it can create local potential on the nano-devices which is termed Scanning Gate Microscopy (SGM), which is introduced in 5.2. Light sources, LEDs and CW lasers from 405 nm to 1310 nm, are implemented to the SPM with focusing down to the diffraction limit (roughly wavelength/2) corresponding to the scale of a nano-device. By scanning the nano-device under the focused light spot one can excite electrons. The technique called optical beam induced current (OBIC) in this thesis, or so-called scanning photo-current microscopy (SPCM), is introduced in 5.3, and the equipment is used for Paper III. By combining the focused laser and SGM, one can study hot carrier and local gating caused band bending simultaneously with high precision. SGM combined with lasers and LEDs promotes the possibility of studying carrier dynamics and local band bending on nanostructures, and Paper II shows the technique well utilized on the barrier NW device.

5.1 Atomic Force Microscopy

SPM techniques measure surfaces using several different physical mechanisms. In STM, the tunneling current derived from a voltage potential difference between the tip and the sample allows the tip to follow the surface changes. Instead of using tunneling current, AFM uses the tip-sample interaction forces, *F(d)*, as shown in Figure 5-1 (a). Different attractive and repulsive forces are active, with relevant

length scales of 10 nm to 0.01 nm, as shown in Figure 5-1 (b). The tip-sample interaction force diagram is shown in Figure 5-1 (a). A force-distance relation curve is shown in Figure 5-1 (c), and can as an example be described by the Leonard-Jones potential model depending on the tip-sample distance:

$$F(d) = -\frac{\partial U(d)}{\partial d}$$

Equation 5- 1

Where the Leonard-Jones potential consists of two major individual terms, i) $\propto d^{-12}$ part: short-range repulsive forces due to the Pauli exclusion principle and acting within a nm range, and ii) $\propto d^{-6}$ part: long range Van der Waals force, up to 100 nm. The two terms differentiate the attractive and repulsive forces, respectively.

$$U(d) = 4 \in \left[\left(\frac{\sigma}{d}\right)^{12} - \left(\frac{\sigma}{d}\right)^{6}\right]$$

Equation 5- 2

where d is the interatomic separation between the sample surface and the outermost atoms of the tip apex, as illustrated in Figure 5-1 (a), ϵ is the depth of the interaction potential well, and σ is a finite distance for the interactions at zero potential, where an extension of the x-axis is shown in Figure 5-1 (c).

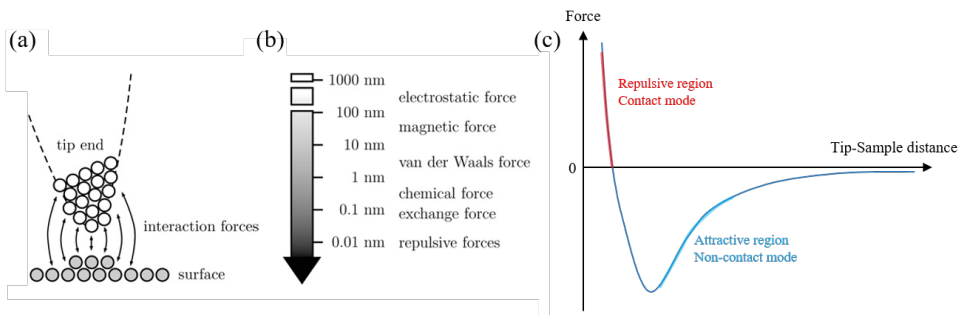


Figure 5-1. AFM interaction force diagrams. (a) Tip apex-sample surface interaction force in atomic scale illustration. (b) Types of tip-sample interaction force correlating to the distance range. Figure (a) and (b) are from [85].(c)) Simple diagram of AFM interaction force as a function of distance.

The force diagram shows two regions where the slopes are high, that is, the tip can be operated sensitively to the surface. The two regions, showing as red and sky blue curves in Figure 5-1 (c), are corresponding to contact mode and non-contact mode, respectively. Since scanning with contact mode would gently scratch on the surface, it could damage the sample or the tip. On the other hand, non-contact mode may

lose resolution of the real surface as the interaction is weaker. The intermittent mode, or so-called tapping mode, works between the two modes, periodically contacting ("tapping") the surface. A conventional AFM tip consists of a sharp tip mounted at the end of a cantilever. One way to sensitively measure the forces is to use that the AFM cantilever has a resonance frequency, at which frequency the tip acts very sensitive. For AFM scanning on the surface in dynamic mode, one can first choose the type of force to scan with on the surface by picking up a frequency shift to the natural resonant frequency, f_r, negative value for attractive force while positive frequency shifts for repulsive force.

Besides conventional intermittent mode AFM, there is also the so-called qPlus mode, typically operating in the non-contact regime, where a very stiff probe (with high Q-factor) is oscillated at very high frequency and only small amplitude. They are using different mechanisms, optically measured deflection or electrical measured quartz crystal oscillation, respectively. The conventional cantilever tip is usually made by silicon, while the qPlus sensor consists of a metal tip and a quartz tuning fork (which is the same as what we have in many watches, to keep time). The microscopy images of the two types of cantilevers with tips are shown in Figure 5-2 (a) and (b), respectively. In non-contact mode, an applied force is in the range of 1 nN (cantilever) or lower (qPlus). A qPlus sensor operates as frequency modulated AFM, which can provide atomic spatial resolution with sub-nanonewton sensitivity. Due to the high resonant frequency of the quartz tuning fork, a qPlus AFM works with greater harmonics and signal-to-noise ratio. The qPlus sensor can be used as STM, too, since the tip is conductive and electrically connected, and it can run in both STM and AFM modes simultaneously when needed, for instance, scanning on a transistor device geometry where most of the surfaces are insulating. Many SPM systems, including Omicron, Sigma and Unisoku, in our group have qPlus options, and they are using the same basic mechanism with slightly different qPlus sensor design. Here, I would like to describe the qPlus sensor of Unisoku STM/AFM. There are three electrodes on a qPlus sensor, two electrodes, s+ and s-, for resonating the quartz and one extra for tip bias. The amplitude and frequency are then detected by a piezo material where a qPlus sensor is directly glued on. The quartz fork has a fixed resonant frequency of around 32 kHz before a tip is mounted; therefore, the f_r of a qPlus sensor is usually a few kHz below 32 kHz. By oscillating a sharp tip close to the resonance frequency f_r, with a shift of usually 3-10 Hz for qPlus AFM, one can adjust the interaction force between the tip and the sample. As the frequency shift is fixed, i.e., constant force, one can scan and resolve the surface in Ångström resolution. In my study of lateral NWs (Paper I), a cantilever AFM is used, while qPlus AFM is used in (Paper II). Here, I would like to focus more on the qPlus AFM, because we built the SPM combined with lasers/LEDs with it and this is less common than the cantilever setup.

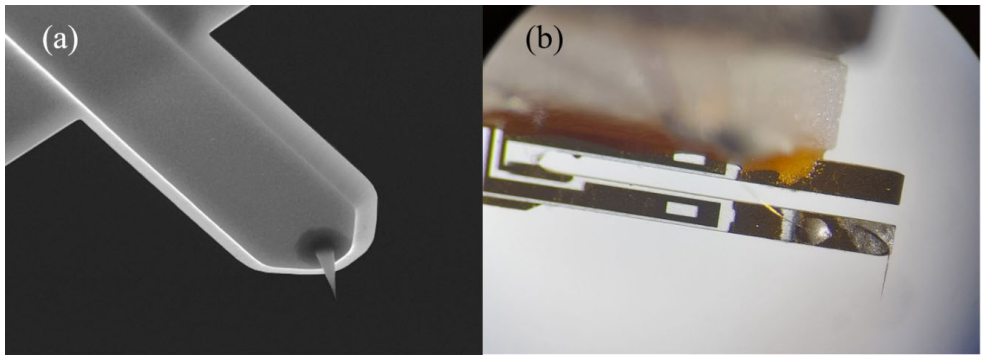


Figure 5-2. AFM tips (a) cantilever with a sharp tip mounted at the end. Figure from [86]. (b) qPlus sensor consisting a quartz folk and a metal tip mounted on.

5.2 Scanning Gate Microscopy

As the electronics are scaling down to nanometer scale and even with an atomic scale barrier, the nanometer position of a potential gate over the device starts to play a big role. For a nano-material field-effect transistor, the gate position around the nano-channel causes major influences. Also, a side antenna at a specific position of the NW device could change the transport property significantly. The SGM set-up equipment is based on a conductive AFM, and it is combined with simultaneous electrical transport measurement over the device. It is the best candidate for observing, with high spatial resolution, the local gating effect on the surfaces with nanometer spatial features, like on heterojunction devices. Here, the AFM tip is not only investigating the topography, but also plays the role as a mobile local gate moving over the device, as described for example in Paper II, where the device source-drain device current is recorded simultaneous to the tip position. Hence, the varying current as a function of local gate position and the AFM topography are obtained at the same time. With our Unisoku system, there are four electrical channels on the sample stage for gating and electrical characterization plus two external connectors for the tip bias and tunneling current reading. In Figure 5-3 (a), the band diagram of an InAs NW with InP segment is sketched with an applied source-drain bias, V_{SD}, and a tip with positive bias which approaches the left part of the NW. Band bending on both valence band and conduction band due to the local gate is schematically displayed. The local gating effect is easier to anticipate on a single composition, but the scenario gets complicated when the tip gets close to the heterojunction, such as, the InP barrier. An image of the SGM setup can be seen in Figure 5-5 when there is no light coupled in.

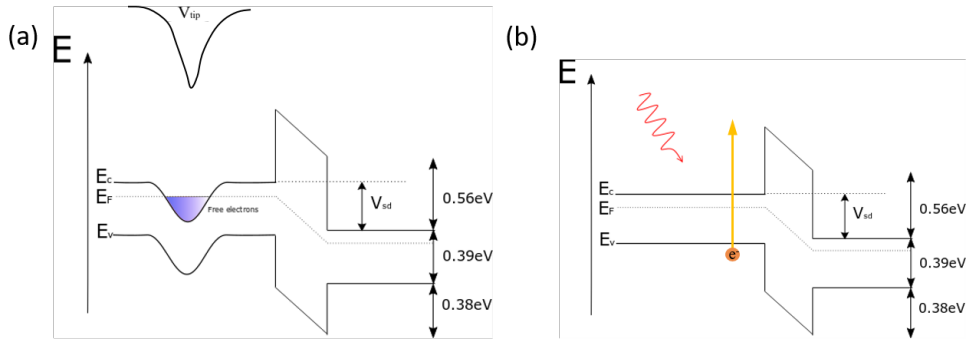


Figure 5-3. Band diagram influenced by external field. (a) Local band bending induced by biased AFM tip on a InAs/InP NW device with a source-drain bias, Vsd. (b) Focused laser excitation on the left InAs segment of the device.

5.3 Optical Beam Induced Current

The optical beam induced current (OBIC), or so-called scanning photo-current microscopy (SPCM), technique is inspired by many nano-heterojunction materials in modern optoelectronic research and applications. One can focus a laser beam, excite the local electrons to a higher energy state, and study electron transport and hot carrier dynamics. The laser beam can be focused close to its diffraction limit and the piezo moving stage of SPM reach sub-Å level. The combination of the two advantages give the light excitation map of a heterojunction with high spatial resolution. Here, an Unisoku SPM system, customized designed for use with advanced light sources has been combined with an optical setup, including collimating lens, objective lens, two beam splitters, LED lamp, and a CCD camera. The optical setup diagram is shown in Figure 5-4. It is equipped with laser diode sources ranging from violet to IR with wavelength 405 nm, 450 nm, 515 nm, 660 nm, 780 nm and 1310 nm. With a single mode laser fiber and a 100x objective, a roughly 500 nm beam size can be achieved with a 780 nm laser. With the focused beam, one can raster the sample with high precision to scan the beam across the device and record the current of the device simultaneously with the Unisoku system (described below). A current map with precise X- and Y- axis can then be established across a device. This has been done in practice for the InAs/InP NW device in Paper III, using it for hot-carrier studies, and a sketch of the band diagram and carriers across the wire are shown in Figure 5-3 (b).

For the laser wavelength options introduced above, an Olympus LMPLFLN100x objective works well in the wavelength range of 400 to 800 nm, except 1310 nm laser. Therefore, an infrared (IR) objective is needed for the longer wavelength (lower photon energy). An IR objective, Optosigma PAL-100-NIR-HR, is then implement to our system, but other optical parts are also not completely compatible

to the IR wavelengths. The CCD camera is based on doped-Si detectors, and the bandgap of the detector materials are larger than the photon energy of a 1310 nm laser, about 0.95 eV, which leads to the fact that the beam at the wavelength cannot be seen on the camera, however, OBIC scanning is still possible. To align the IR beam, introducing two laser beams for position calibration is an option, one in IR for measurement and the other one in visible range for alignment. This solution requires one more 2-way mirror cube module and a space for mounting on the optical system. One other solution is to mark the relative position of the beam to the CCD image with the present optical system. The latter one is used in the present case for IR beams.

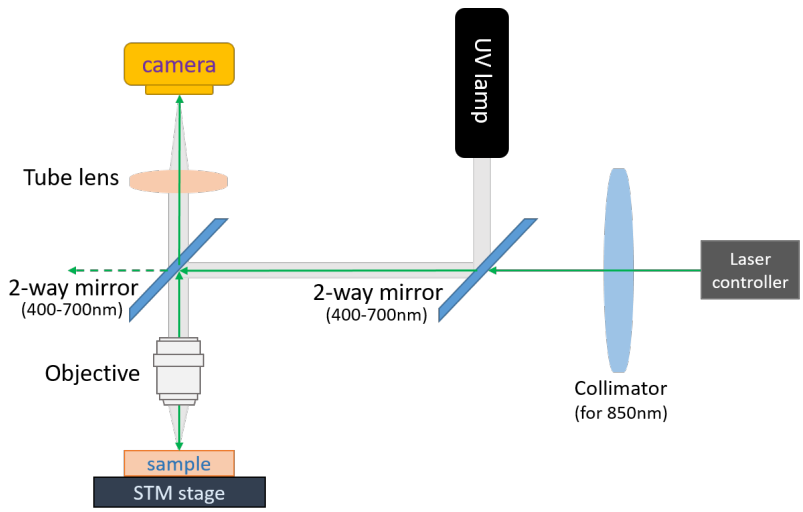


Figure 5-4. Optical design diagram showing the path and the focusing mechanism for the OBIC and laser that combined SPM.

5.4 Combining Lasers illumination with SPM

A setup combing lasers with SPM is developed by using a constant wave (CW) laser as in the OBIC setup and a qPlus AFM as SGM (as described above). Laser induced excitation combined with SGM is then demonstrated as a method for careful studies of hot electrons in a variable band alignment environment. Gating effects induced by a local electrical field and carrier excitation by an incident laser/LED pumping essential features governing opto-electronics. We thus combine two important techniques, nanometer precision mobile gates with a sharp photon energy bandwidth laser, on a heterojunction NW device. The illustration of the complete concept is

illustrated in Figure 5-3 with the example of InAs/InP NW. As seen in Paper II, the device current behaves dramatically different with tip gating position.

The simultaneous combination of laser light and SGM need is not a one-to-one combination of the OBIC with SGM because of the limitation on the space for the AFM tip. That means, the working distance of the 100x objective have to be large enough, so that the AFM tip can work in between. The working distances for Olympus LMPLFLN100x is 3.4 mm, which is not enough for the tip holder module stay in between. An alternative would be using a 20x objective, Olympus LMPLFLN20X, with working distance 12 mm but sacrifice the beam size. The laser combined SGM setup illustrations are shown in Figure 5-5 (a) and (b). As seen in the figures, the laser beam comes with an angle, because the tip has to always stay at the normal angle, which blocks the laser beam if the laser is also from the normal angle. Therefore, tilting the whole optical setup would be the option. In Figure 5-5 (d), a tilted optical system is mounted on top of the Unisoku SPM system with 30 degrees, and the view from the camera shows the laser beam, the tip apex and the sample, which indicated that the laser beam is not shadowed by the AFM tip and can reach the sample simultaneous with the tip.

The SGM combined with lasers is developed from an original idea of combining the highest temporal resolution (fastest) technique, pump-probe laser down to femtosecond, with the highest spatial resolution (last fastest) technique, SPM down to atomic scale. This was tested during the PhD in an attempt to combine the STM with a pump-probe laser with a delay time step size of 10 fs range and peak width of around 200 fs. The first pulse of 2.4 eV for pump is with green laser of about 532 nm and the second pulse of 1.2 eV in IR range of 1000 nm. The laser was operating at 7 W of repetition rate 210 kHz on the Ti:Sapphire laser source of FWHM about 60 μm for both of the colors. The thermal expansion on the STM tip however makes the tunneling current unstable, but after 1) the lock-in amplifier with a proper repetition rate 2) defocus and lower the power, the current could be stable enough for reading out the two-photon process on the GaN substrate of 3.49 eV bandgap. The power for the pulses are adjusted close to 0.5 μW for both the green and the IR. However, our measurements were not reproducible and consistent enough, and one more lock-in amplifier would be needed for filtering out the thermal expansion effect. Since the challenging experiment takes time to fulfill, the urging for device characterization innovated us alternating the equipment toward more general applied direction.

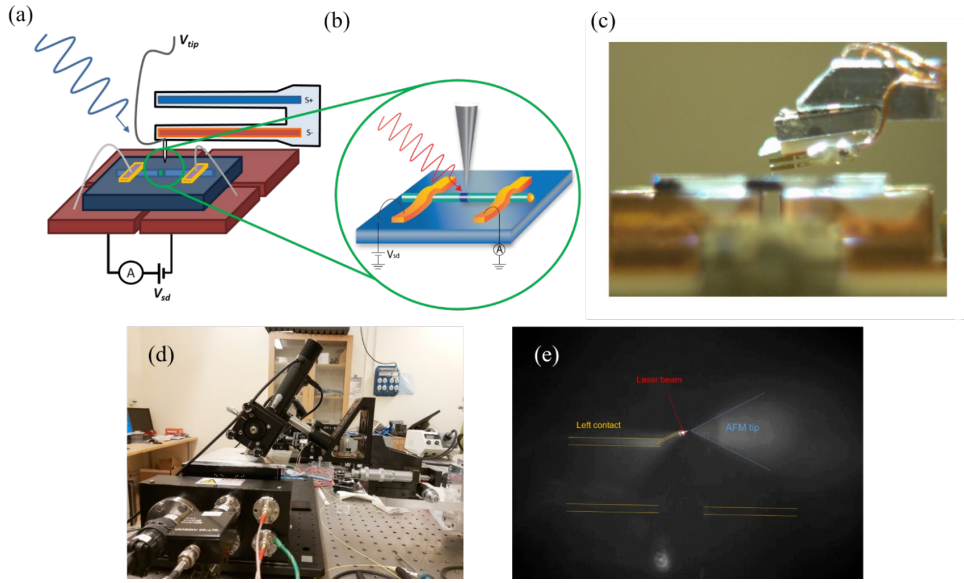


Figure 5-5. SGM combined with laser diode setup. (a) Illustration of the laser combined SGM setup including the sample stage (with 4 individual electrical channels for device measurement), qPlus AFM tip, and laser coming in with a tilted angle. (b) Zoom in from (a) to emphasis on the tip and laser to the device (c) A real photo on the working SGM measurement. (d) A photo on tilted optical system coupled to the Unisoku SPM system. (e) The view from the camera showing that the laser beam is not shadowed by the AFM tip.

Unisoku electrical control system

The Unisoku SPM setup uses SPECS controllers of I. Real-Time Controller RC5 as a main controller communicating with other controllers and computer software, II. Signal Conversion SC5 for output voltages and input readout channels, III. Oscillation Controller with PLL Nanonis OC4 for AFM oscillation, IV. High Voltage Amplifiers Nanonis HVA4 for course stage movements, and V. Piezo drivers Nanonis PD5 for headset controller and piezo scanning state. They talk to each other through low noise cables and an Ethernet cable to the computer controlling with Nanonis software. A current amplifier Femto DLPCA-200 and a charge amplifier HQA-15M-10T amplify the STM and AFM signal, respectively. In SGM setup, we take Femto for amplifying device current.

Chapter 6:
Synchrotron based X-ray Photoelectron Spectroscopy

In Chapter 3 and Chapter 4, STM/S was introduced as powerful for surface atomic resolution and electronic properties. However, information about the elements of the material, the chemical bonds, and the states of the materials, is not easily derived from STM/S, and it is also important for studying devices.

We use XPS to study these aspects of surfaces and nanostructures to enable surface engineering of devices. Several works in this dissertation use synchrotron-based X-ray techniques, which will be introduced in chapter 6.1. The most used one is XPS for studying the surface chemical composition, to monitor, e.g., native oxide cleaning and surface treatments. In chapter 6.2, XPS and the effects of atomic hydrogen cleaning and ALD process observed by XPS are discussed. The analysis of the XPS spectra will be discussed in chapter 6.3.

6.1 Synchrotron X-ray sources

Synchrotron X-ray sources have an extremely high brilliance radiation (a 4th generation synchrotron can provide 9 orders higher X-ray brilliance compared to a lab-based source). Synchrotrons can emit radiation ranging from infrared to hard X-ray range. Further, the spatial and energetic resolution can be adjusted to attain the project demands. A synchrotron facility usually consists of an injector accelerating electrons to quasi relativistic speeds, and then injecting the electrons into a storage ring (the synchrotron). An undulator, consisting of periodic arrays of magnets placed along the path of the electrons in the ring, imposes regular oscillations perpendicular to the electron trajectory, which results in X-ray emission mostly at some specific energies depending on the separation between the magnets. The resulting X-ray beam can then monochromatized through advanced X-ray optics at each beamline using gratings, mirrors, slits, etc. A standard XPS beamline setup and the photon-sample interaction will be introduced in the next section.

6.2 X-ray Photoelectron Spectroscopy

Heinrich Hertz observed the effect that electrons can be emitted from a surface under light irradiation in 1887, and the theory of the photoelectric effect was explained by Einstein, for which he was awarded the Nobel Prize in 1921. It was later realized that by illuminating a sample with monochromatic light and observing photoelectrons with specific kinetic energies one could retrieve chemical information about the sample. The technique, which was initially called electron spectroscopy for chemical analysis (ESCA) and is commonly known as X-ray Photoelectron Spectroscopy (XPS) nowadays, was developed by K. Siegbahn and his co-workers, and he was awarded the Nobel prize in 1981. XPS is today used as a powerful tool for determining chemical and electronic structure characteristic of surfaces.

The principle of XPS is that a monochromatic photon beam with energy $h\nu$ (with h being the Planck constant and ν the frequency) irradiates the sample surface and interacts with the electrons in the surface region. The XPS is described in the following with a focus on core level spectroscopy. While the valence electrons of a material are delocalized, as they participate in the bonding, electron in core-level states bound closer to the atomic nucleus and localized around the atom retain the sharp level nature of a free atom. The minimum energy required to remove an electron from the core-level, letting these core electrons reach the Fermi level, is called binding energy, E_B, which can be obtained from literature derived from both theoretical calculations as well as from experiments. As the core-level electrons absorb a large enough photon energy $h\nu$ to leave the sample becoming observable photoelectrons, the photon energy $h\nu$ have to be higher than the sum of E_B (energy from the initial core-level state to the Fermi level) and the sample work function Φ_s (energy from the Fermi level to the vacuum level). The remaining photon energy will then be the kinetic energy E_k that can be detected by an electron energy analyzer, determining the number of electrons and their E_k. The illustration of the process is shown in Figure 6-1 and its energy conservation equation is expressed as:

$$h\nu = E_B + E_k + \Phi_s$$

Equation 6- 1

where $h\nu$ is the photon energy of the incoming X-ray beam, E_B is the binding energy of the electron, E_k is the kinetic energy of the photoelectron in vacuum and Φ_s is the sample work function. Both valence and core-level excitations are shown in Figure 6-1, as the pink and blue peaks in the spectrum, respectively.

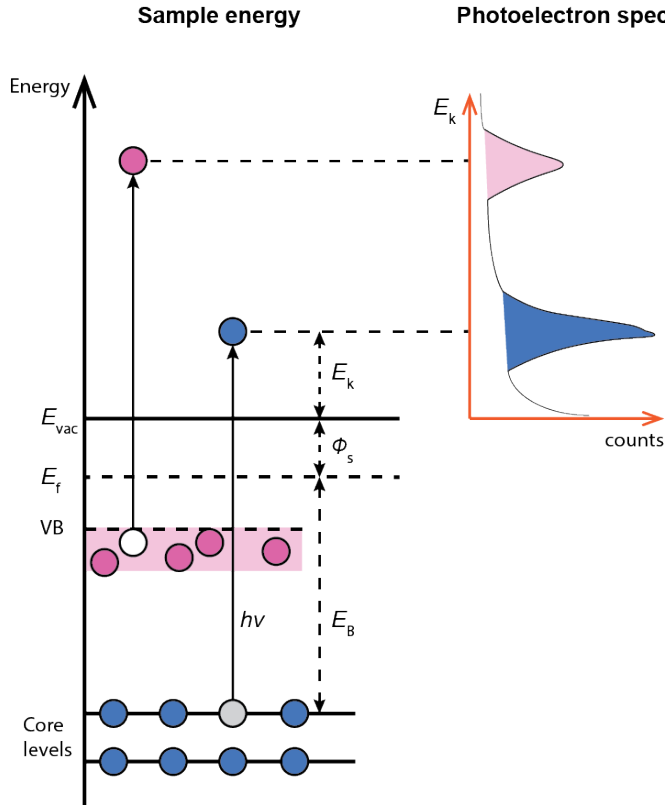


Figure 6-1. Energy diagram of XPS working mechanism. The core-level electrons absorb the photon energy hv from the synchrotron light and get excited from the initial core level state to the vacuum level E_{vac}, requiring minimum energy of E_B plus Φ_s. The rest of the energy left from the photon would be the kinetic energy of the photoelectron resolved on the energy analyzer detector.

After describing the XPS process of photon-electron interacting, and energy transferring, let us move on to the experimental part. First, a typical XPS analyzer has a hemispherical shape with inner and outer shields on to which there is applied positive and negative bias, respectively. A photoelectron leaves the surface with kinetic energy, E_k, will then enter the hemisphere. Higher kinetic photoelectrons would travel a longer way while lower kinetic photoelectrons would travel a shorter way, ending up at different position on the detector, as shown in Figure 6-2. There are many pixels in array on the detector, and each of them can evaluate the intensity of photoelectrons. Every pixel at different position corresponds to a specific kinetic energy for energy spectra. One benefit of this is that a snapshot can already give an energy spectrum, which is helpful for beam sensitive samples avoiding beam damage. For instance, the properties of some nanostructure samples change quite fast under a focused X-ray beam (120 nm), so we avoid too long exposure of sensitive single nanostructures.

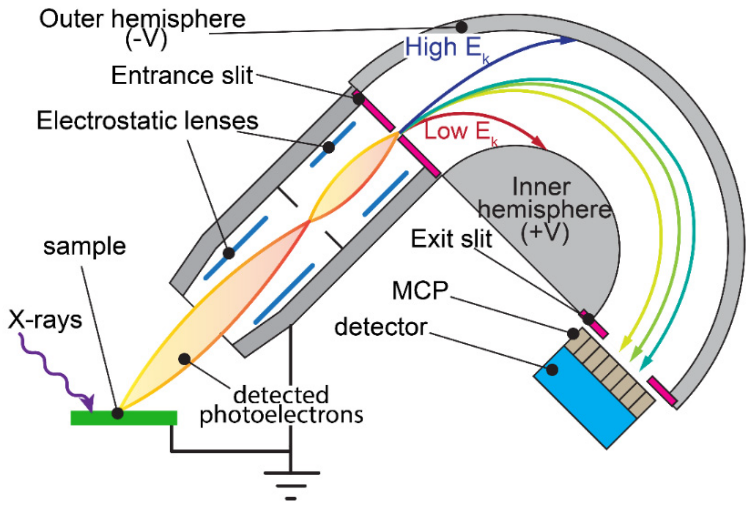
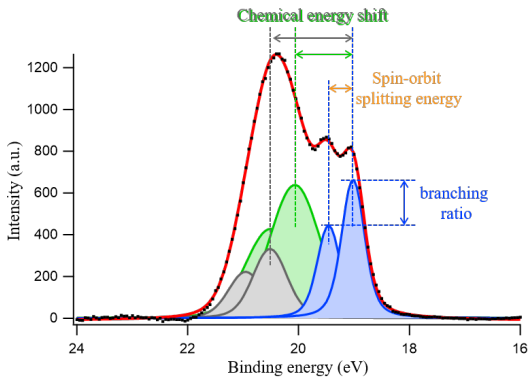


Figure 6-2. Schematic diagram of a semi-sphere XPS electron energy analyser (EEA) showing the photoelectrons from the sample going through the analyzer and being energy separated by different voltage applied on the outer hemisphere and inner hemisphere. Adapted from reference[87].

6.3 XPS spectrum analysis

The spectra acquired from XPS need to be fitted with reasonable parameters, such as, Lorentzian width, Gaussian width, spin-orbit splitting energy, spin-orbit branching ratio, etc. Every parameter is essentially important, because they correspond to each chemical component and make the curve fitting physically meaningful. The meaning of each parameter will be introduced below followed by analyzing steps with examples of Ga 3d core-shell spectrum from a GaSb substrate. **I.** *Background* subtraction: A low-order polynomial function is mostly used for compensating secondary photoelectrons. **II.** *Peak intensity:* this parameter is proportional to the quantitative amount of each component, as a result relative changes in the surface composition can be derived from this and with suitable calibration even quantified. **III.** *Gaussian* and *Lorentzian*: Voigt is a convolution of Gaussian and Lorentzian functions. *Lorentzian* broadening is a fixed value for each individual core-level relating to the physical properties such as the lifetime, while *Gaussian* broadening comes from crystalline quality, as well as the detector resolution and instrumental uncertainties. **IV.** *Spin-orbit splitting energy* and *branching ratio*: They are fixed values for photoelectrons from a given core level. Because the spin-orbit splitting energy will not change, e.g., the energy separation between Ga $3d_{3/2}$ and $3d_{5/2}$ peaks, even at a different bonding state, the splitting energy is fixed for a certain core-level. The same theory is applied to the branching ratio such that the available states with the same angular momentum cannot vary,

so the intensity ratio of core level doublets always stays the same. **V.** *Chemical energy shift:* a different chemical bonding would lead to different bonding energy, for example, in Ga 3d core-shell, Ga_2O and Ga_2O_3 would show different chemical shift due to a different energy of the covalent bonds. The energy shifts compared to the bulk of different states should stay the same. Therefore, it is important to set the correct energy shifts to the elements they stand for. There is an example in Figure 6-3 showing the fitting of a spectrum from a GaSb substrate after 80 seconds atomic hydrogen cleaning using the parameters described above.



Peak parameters	Ga bulk (GaSb)	Ga^{1+} (Ga_2O)	Ga^{3+} (Ga_2O_3)
Background	-11	-11	-11
Lorentzian	0.18	0.18	0.18
Branching ratio	0.67	0.67	0.67
Spin-orbit splitting energy	0.44	0.44	0.44
Peak intensity	403	776	286
Gaussian	0.39	0.97	0.63
Energy position	19.02	1.05	1.5

Figure 6-3. Ga 3d core-shell XPS data analysis with fitting parameters indicated, obtained on a GaSb substrate after 80 seconds atomic hydrogen cleaning. Graph on the left showing the 3 doublets, Ga(blue), Ga^{1+}(green), and Ga^{3+}(grey) states, with corresponding fitting parameters marked. The black dots are the raw data measured by the detector while the red line is the fitting curve. Table on the right displaying the values for each parameter to fit the XPS curve.

6.4 Examples of XPS studies

I was involved in many projects that include XPS experiments, and I would like to give two very different examples on the XPS studies, soft X-ray based XPS on nanostructure-GaSb NWS in section 6.4.1 and hard X-ray based XPS on ferroelectric devices in section 6.4.2.

6.4.1 XPS on GaSb NWs

Due to its high hole-mobility, GaSb is a promising candidate for high-speed p-channels in electronic devices. However, GaSb exhibits a comparably thick native oxide causing detrimental interface defects, which has been proven difficult to remove. In the work described in paper IV, we use *in-situ* synchrotron-based XPS to show full oxide removal from GaSb surfaces using effective hydrogen plasma cleaning under UHV.

The NWs are deposited by tissue transfer to a silicon substrate. Here, one needs to be careful on the substrate material that the XPS peaks do not overlap with any Ga or Sb core-shells, to have clear signals and make the analysis of background subtraction easier. Further, the intensity of the signal from the NWs is usually quite low due to the low coverage, and therefore we need a higher NW density. However, by increasing the density of NWs, they start to stack up, which causes charging issues. A proper NW density is then important for the experiment, and we examine the NW deposition condition with SEM for all the samples. Then we perform in-situ Hydrogen cleaning and ALD process, as introduced in chapter 3.6 and 3.7, on the NW samples. The results are shown and discussed in paper IV.

6.4.2 Hard XPS on ferroelectric devices

Regular XPS is a very surface sensitive technique measuring the surface atoms at the depth of a few nanometers, which corresponds to the inelastic mean free path of the electrons, an average distance for electrons traveling between inelastic collisions. The photoionization cross-section of the electrons depends on the energy itself and the mean free path of the media material. In order to investigate atoms further into the sample by XPS, we need higher photon energies, so that the photoexcited electrons have a higher kinetic energy and thus a larger inelastic mean free path. Further high binding energy spin-orbits or materials deeper from the surface can then be studied. In some research projects, especially for layered structure devices, the interfaces of deeper layers are interesting rather than the composition on the top surface, which means higher photon energies is needed. At the synchrotron, the photon energy at a higher energy range (typically above 5-10 keV), often called hard x-ray, can be used for this purpose. With this, the high energy photons will be able to excite the inner electrons to energies above the vacuum level and let the excited electrons scatter inelastically for a few nanometers before reaching the surface.

Hafnium oxide or hafnium zirconium oxide (HZO) thin films between the InAs (001) substrate and a metal top contact TiN layer are a promising material combination for developing faster switchable memory devices for neuromorphic networks and realizing ferroelectric tunnel junctions.[88] In our ferroelectric memory work, we study the interfaces of TiN, HZO, and InAs with hard X-ray photoelectron spectroscopy (HAXPES) at Diamond synchrotron I09 beamline to probe the chemical bonds of the HZO film using 6 keV and 8 keV x-ray beams. After deposition by ALD, the HZO film should be amorphous and exhibit no ferroelectric behavior. Then the sample gets annealed to 550°C, which should change the oxide film into a polycrystalline phase. However, the polycrystalline phase of the HZO film does not have the ferroelectric properties, unless it is in the

orthorombic phase. Therefore, we put a TiN film on top since annealing the HZO film in between the InAs substrate and the TiN film gives sufficient strain to obtain the orthorombic phase. With the operating crystal phase, activating the device using a wake-up process, which was set to be five to ten thousand positive-up-negative-down (PUND) electrical pulses with triangular wave function and a period of 10 ns. Here, we could investigate whether the wake-up process and device switching process would lead to a change of the core-shell bonding, which should be seen in the XPS spectrum.

Chapter 7:
Summary of Results

This chapter introduces the papers included in this work and provides a summary of the main results of each study. As mentioned in the introduction, the work behind this thesis centers around devices with nanostructure components. In the first section, 7.1, the result of $In_xGa_{1-x}As$ laterally grown NWs studies with LT-STM/S are summarized, while the main results of the effort can be found in Paper I. The optical laser combined with an SPM system can be applied to very broad fields for optoelectronics. The work demonstrating this system for the study of InAs/InP NW devices is summarized in section 7.2 and the main results can be found in Papers II and III. Going beyond SPM on devices, XPS is a complementary technique for studying the surface chemistry. The XPS results on GaSb NWs for device applications are concluded in section 7.3 while the main findings can be found in Papers IV and V. A hybrid material system of combined 1D and 2D structures using InAs NWs and graphene characterized with multiple techniques will be summarized in section 7.4, and its main results can be found in Paper VI. The single suspended InAs nanosheet devices work is not yet published, but still in progress, and the results will be summarized in section 7.5.

7.1 $In_xGa_{1-x}As$ lateral nanowires studies with LT-STM/S

Laterally grown $In_xGa_{1-x}As$ NWs show promise for quantum computing applications. A qubit can theoretically be achieved by combining such lateral NWs and a superconductor contact, for example, Al, Nb and Pb. However, the NW surface, which will then be the interface to the superconductor contact, can require atomic scale control. A starting point is to control the basic surface of the NW sample after being exposed to ambient air (often unavoidable in processing) which results in forming native surface oxides that can be a stumbling block for creating the precise controlled conditions with atomic scale precision. To prepare an atomically controlled surface for further experiments, we performed atomic

hydrogen cleaning to remove the surface oxides residues and performed STM/S measurement. The geometric and electronic surface structures of $In_xGa_{1-x}As$ NWs and contacts, which were grown directly in a planar configuration, are then studied using LT-STM/S.

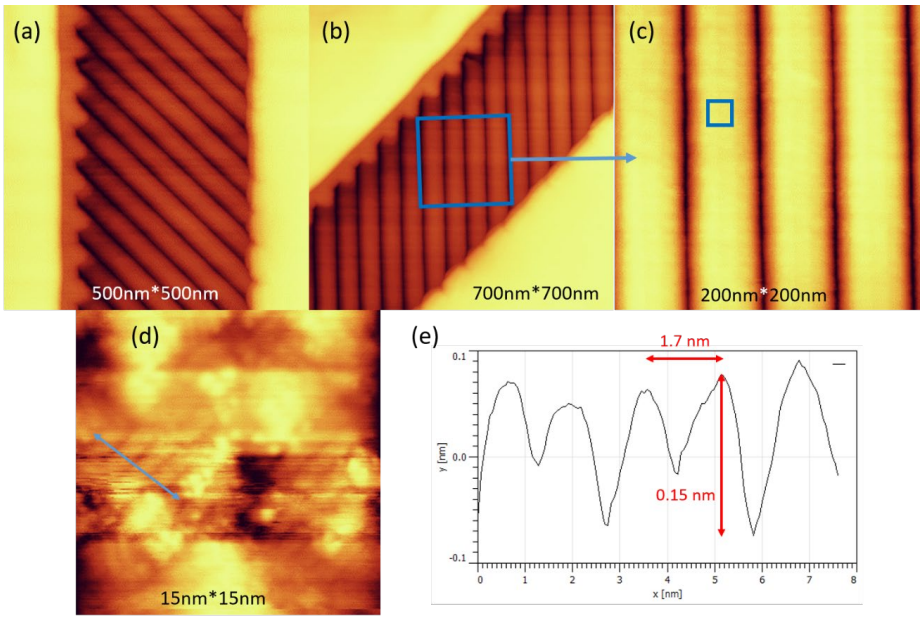


Figure 7-1. STM topography images on the lateral NWs: (a) 500x500nm^2 STM image shows the geometry of contacts and NWs with scan orientation perpendicular to the contacts. (b) A 700x700nm^2 STM image, 43° rotated scan direction from (a), shows the geometry of contacts and NWs (aligned vertically in this image). The blue square area is shown in (c). (c) 200x200 nm^2 STM image showing more detailed facets of the NWs. (d) 15x15 nm^2 STM image acquired at the smaller blue square in (c) on a top facet of the NW. (e) Height profile along the blue arrow shown in (d) showing the scale of the 4 x 2 surface reconstruction. STM images were taken with sample biases of -3.0 V and tunneling currents of 80 pA.

The navigation method for bringing the STM tip to the lateral NW region is discussed in section 4.4. After the sharp STM tip arrived at the relevant device area, the STM imaging on the NWs could be performed. STM images of the $In_xGa_{1-x}As$ NWs with step-by-step zoom-in is shown in Figure 7-1. To further image the surface with atomic resolution, a 15 nm by 15 nm STM image in the flat area is seen in Figure 7-1 (d), where the exact position for the image is shown in Figure 7-1 (c) marked with a blue square. A 4 x 2 surface reconstruction of InGaAs (001) is observed on the top facet of the NWs (see Figure 7-1(d)) and the contacts (see Figure 7-2(a and b)). In Figure 7-2 (a), surface steps and small atomically flat terraces can be seen, and a zoomed in view is shown in Figure 7-2 (b). The detail of the 4 x 2 surface reconstruction model with the height and spacing, as in Figure 7-1 (d and e)

and 7-2 (a-c), is shown in Paper I. The difference in distance between neighboring stripes is about 1.7 nm on the NW and 1.5 nm for the contact, which implies a higher Ga concentration on the contact. (Lattice constant of InAs is slightly larger than that of GaAs)

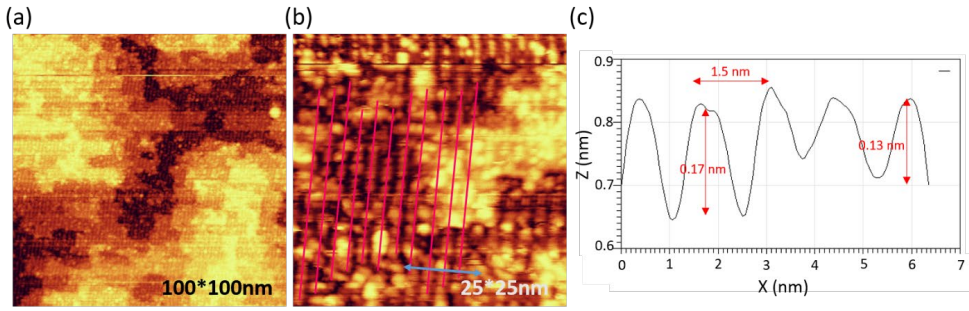


Figure 7-2. Surface reconstruction: (a) 100 x 100 nm^2 STM image taken on the contact. (b) 25 x 25 nm^2 STM image taken on the contact. The pink parallel lines show the pattern of the 4 x 2 surface reconstruction. (c) Height profile along the blue arrow shown in (b). STM images were taken with sample biases of -5.5 V and tunneling currents of 50 pA.

With a clear map on the NWs, we perform STS to show surface bandgap at different positions of the NW. A surface bandgap variation is observed that can be attributed to a compositional variation (because In and Ga atoms have a different diffusion rate). A bandgap size change of 30 meV from the middle (position 1) to the end (position 3) of the NWs which corresponds to a 5% In/Ga element concentration change (if compared to 8-band k*p theory calculation shown in Figure 7-3 (b)). The calculation is based on the model of a 50nm wide and 14 nm thick lateral NW, as shown in Figure 7-3 (b) inset. The well-defined facets and small bandgap variations found after area selective growth and atomic hydrogen cleaning demonstrate a good starting point for achieving high-quality interfaces during further processing.

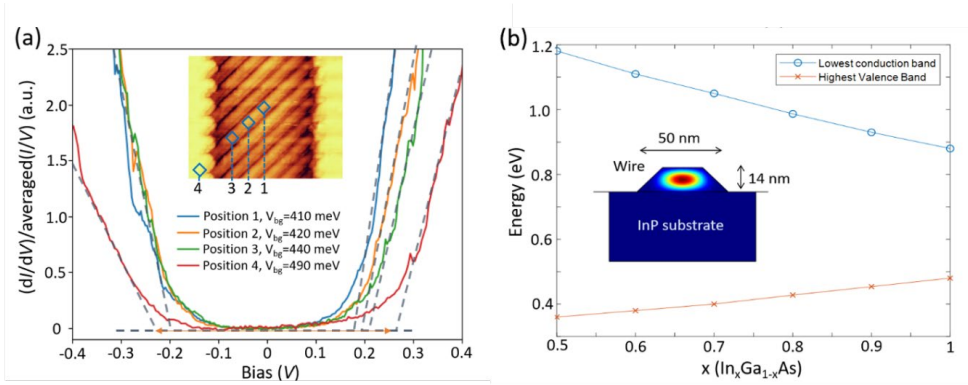


Figure 7-3. (a) Bandgap variations along the NW: Averaged (dI/dV)/(I/V) spectra at positions 1–4, as indicated by blue squares in the inset. Dashed black lines show a linear fit of the VB (left) and CB (right) onset. (b) 8-band k*p theory calculation showing the dependence of the CB and VB edges on the In/Ga concentration x. The model assumes a 50 nm wide, 14 nm high, and infinitely long fully strained NW placed along the [100] direction on InP (001).

There are two additional points about this work worth discussing in additional detail:

I. dI/dV formula used in the analysis

The normalized conductance $(dI/dV)_m/\overline{(I_m/V)}$ equation for analysis of the STS data is used from reference[75], where the $\overline{I_m/V}$ broadening is obtained by convoluting the raw data with an exponential function: $\overline{I_m/V} \equiv \int_{-\infty}^{\infty} \left[\frac{I_M(V')}{V'}\right] exp\left\{\frac{-|V'-V|}{\Delta V}\right\} dV'$, where the ΔV is the broadening width.

In the analysis code, we set the ΔV a bit larger than the bandgap, so that it can convolute well with the neighbor data points, as suggested in the referenced paper.

II. Sub-bands separation model

Thanks to the advantage of the low temperature, our first ambition was to observe standing wave states of such a well-confined nanostructure. With the simulation of quantum standing waves on lateral NW, as shown in Figure 7-4, we attempt to acquire high energy resolution of meV range around the band edges for investigating sub-band splitting. Concluding over several hundreds of STS attempts, the energy peaks do not always stay at exactly the same energy, which means either the tunneling condition changes resulting in the observed sub-band energies shifting, or the peaks on the STS are noise. Due to the complexity of analyzing the data with many unknown factors, we focus on the surface morphology properties first in this work. The STS stability required for observing a few meV energy states on the surface is not trivial.

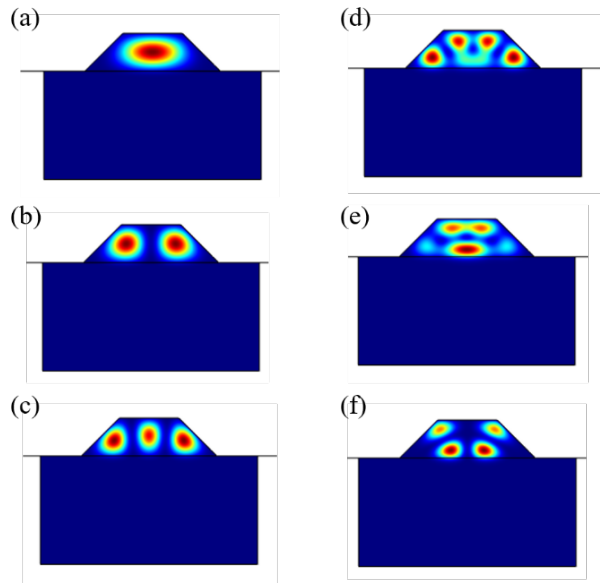


Figure 7-4. Sub-bands separation of $In_{0.8}Ga_{0.2}As$ infinite long NW with potential splitting of (a) uniform energy state (b) band splitting to two by additional potential of 21 meV to uniform state (c) 30 meV (d) 31 meV (e) 0.3 meV (f) 23.6 meV.

7.2 InAs/InP NW device studied with the combined laser and SGM system

Opto-electronics are naturally sensitive to externally induced light and applied electrical potentials. SPM combined with laser excitation was developed to have sharp bandwidth laser down to its diffraction limit and an electrical gate down to nm scale. The setup is shown in Figure 7-5 (a) while the illustration of a focused laser beam for OBIC measurement for hot carrier study is shown in Figure 7-6 (a). The SEM image, AFM image and electrical characterization under different illumination intensity of the device are shown in Figure 7-5 (b), (c) and (d), respectively.

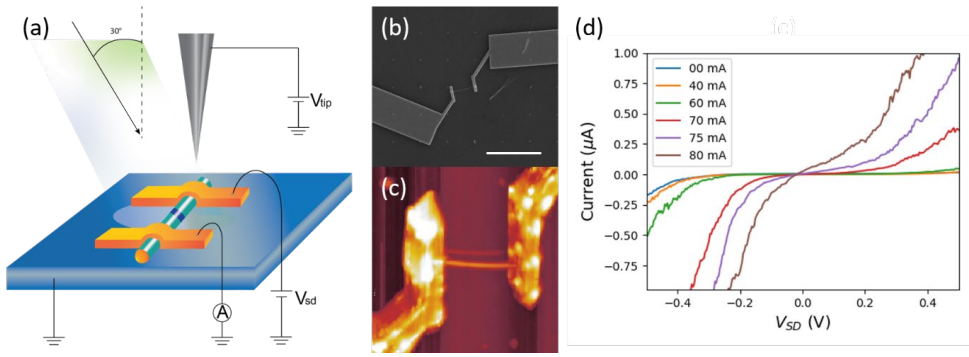


Figure 7-5. Illustration of the combined SGM and laser system. (a) schematic of the InAs NW with InP segment device scanned under a mobile gate tip, homogeneous laser and external bias V_{sd} (b) SEM image of the InAs/InP barrier NW device with a white scale bar of 5 μm (c) AFM image of the device taken simutaneously with the SGM measurement (d) IV curves of the InAs/InP NW device under 780 nm laser with different light intensities.

We use an InAs NW with 50 nm diameter including a 25 nm long InP segment, located at the NW center for the devices. The use of these wires has been described previously in chapter 2.4.3. The band diagram of the NW is shown in Figure 7-6 (a), where the InP segment results in a potential barrier for both holes and electrons. The NW is deposited on a 100 nm SiO_2 insulating layer on top of a Si substrate and contacted at both ends with lithography electrodes. A focused laser beam scans across the device generating photo–current, which is recorded as a function of the beam position. The mechanism of the generated photo-current could be described in three steps: (1) excitation of electron–hole pairs. The electron gains a majority of the excess energy because of its lower effective mass; (2) with the excess energy, the hot electrons would be able to surpass the barrier; and (3) the exceeded charge carriers drift toward the contacts, resulting in a measured photo-current. The photo-current map is shown in Figure 7-6 (b), and the measurement electric circuit connection is marked on the SEM image of the device in the inset. A current profile captured from z-axis in Figure 7-6 (b) is shown in (c) with black crosses, which experimental data fit well with the hot-electron calculation model of a diffusion length of L_e = 280 (±30) nm.

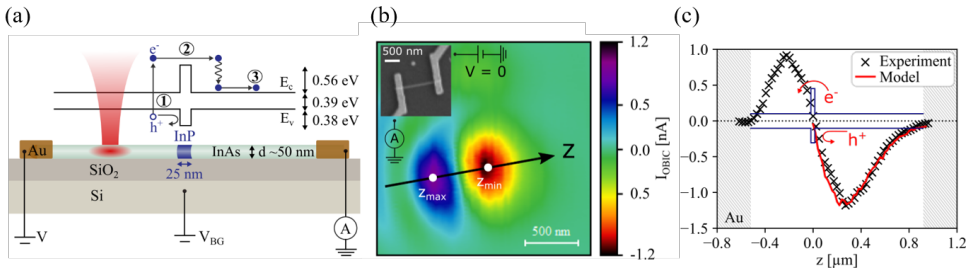


Figure 7-6. OBIC experiment on the InAs/InP NW device[89] (a) Schematic of the sample structure and the mechanism of the OBIC. (b) OBIC of the same NW device, with scanning electron micrograph (SEM) of the device (inset) and circuit schematic showing drain/source contacts. No bias voltage, V_{SD}, is applied, all current observed corresponds to generated photocurrent. z_{max} and z_{min} indicate the points with largest and smallest current. (c) I_{OBIC} current profile taken from the z-axis indicated in (b). Band diagram is plotted in blue with assumption that the InP barrier is at the location where $I_{OBIC} = 0$.

Further, the technique can be applied with different wavelengths by changing the laser diode. We are using the 100x objective, supporting wavelength range from 400 nm to 1800 nm with a high transmission rate above 80%. Therefore, even using the laser in IR range for small bandgap semiconductors is possible. Here, we use a 1310 nm laser, corresponding to 0.95 eV photon energy, smaller than that of the InP bandgap, to probe the hot carrier transport on such a device. The 1310 nm IR OBIC current map is shown in Figure 7-7 (a). A few different power irradiance of the 1310 nm laser OBIC data are obtained in the Figure 7-7 (b), showing that the IR laser with a photon energy close to the potential difference between the VB of InAs and the CB of InP could work well in OBIC.

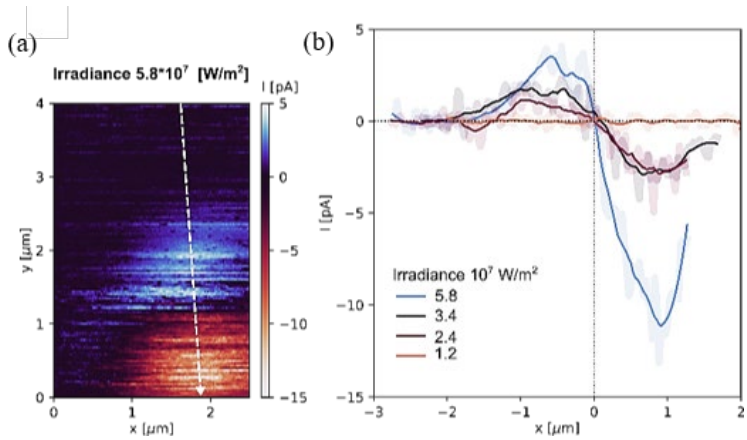


Figure 7-7. IR excitation OBIC from Paper III work (a) OBIC with 1310 nm (0.95 eV) laser at irradiance $E_e = 5.8 \times 10^3$ W cm^{-2}. (b) Current profile of the four different irradiance, 1.2×10^7(orange), 2.4×10^7(red), 3.4×10^7(black), and 5.8×10^7(blue) W/m^2, along the NW, indicated with a white dashed line in (a). The data are averaged with the neighboring 5 points, and the brighter color thick lines behind the thin data line are the raw data without processing.

The data shown above are exclusively with the focused laser beam on the SPM stage without any additional scanning probe. Local electrical field influence on such devices is of interest too, so we performed SGM measurement with mobile local gate rastering on the device. A qPlus AFM tip is used to acquire the topography of the device while applying an electrical bias to further study the gate influence on the operando device. The SGM measurement on the device starts in a dark environment to better demonstrate the mobile gate fundamental influence on the InAs/InP NW device. In Figure 7-8, a set of SGM data with device bias V_{SD}=+0.6 V and V_{tip}=+1 V of scanning range 3 μm by 1 μm is shown. The first part of the data (Figure 7-8 (a)) is an AFM image and a simultaneously obtained device electrical current map is shown in Figure 7-8 (b). By selecting the current at the NW region by the corresponding area in the AFM image, a current profile over the device, averaging 12 lines, is shown in Figure 7-8 (c). In this profile, a clear change in current consisting of an asymmetric peak and a dip can be seen. The current fluctuation is concluded to be at the position where the InP segment. The current peak was expected under a positive bias local gate from an electrostatic model, but a dip right after the peak must be explained by additional surface states.

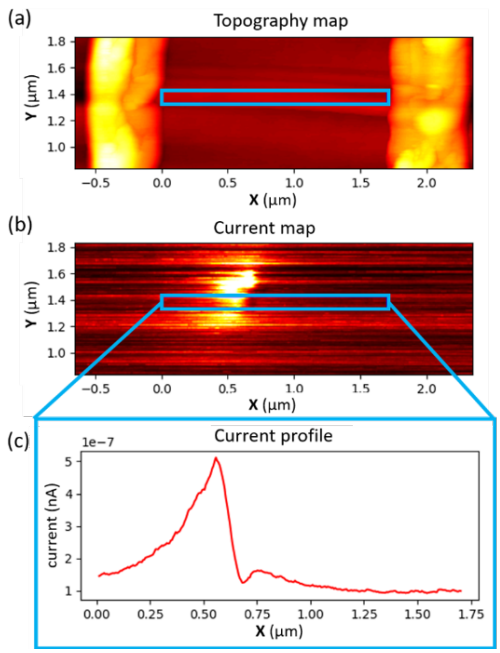


Figure 7-8. SGM data measured with V_{SD}=+0.6V and V_{tip}=+1.0V in dark. (a) Topography map measured with the q-plus AFM (b) Device current map measured simultaneously with topography (c) Device current profile, averaging 12 lines, corresponding to the blue squares, where the NW is located.

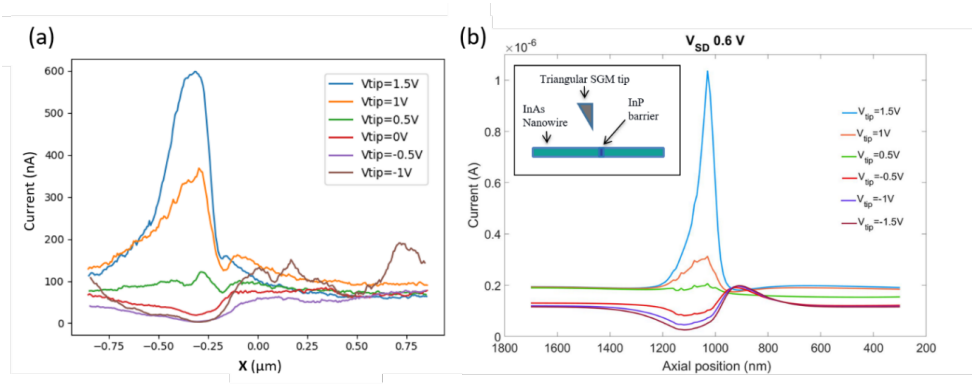


Figure 7-9. Experimental and simulated SGM data on the device (a) SGM measured with V_{SD}=+0.6V and V_{tip} from +1.5 V to -1 V with step size 0.5 V (b) Computational SGM simulation of the InAs/InP NW device with V_{SD}=+0.6V from tip bias -1.5 V to +1.5 V, 0.5 V per step. The tip in the simulation is asymmetry but surface states are not considered. Inset: the graphic of the simulation model.

The current profiles under different tip biases, shown in Figure 7-9 (a), give further insights in the SGM behavior at different local electric fields. The source-drain bias V_{SD} is kept at +0.6 V, and we vary the tip bias from -1 V to +1.5 V with step sizes of 0.5 V. The magnitude of the current follows the trend of the tip bias from positive 1.5 V to negative 0.5 V, high to low. To further dig into the physics of the current behavior lying behind, Comsol multiphysics simulations were performed on a 1.4 μm InAs NW including a 25 nm InP segment using the Comsol partial differential equation (PDE) model. The device current is calculated with the integration of the carrier density along the wire. To capture the asymmetric current behavior, a triangular tip of 300 nm on top and 100 nm long is used in the simulated, as shown in the inset of Figure 7-9 (b). There are many similarities to the experimental result, for instance, the peak shape and the dip behavior. This demonstrates that this reasonably simple model can capture many features in the experiment and help interpret the results.

When implementing the laser together with the SGM, as discussed in Chapter 5, we need to compromise the beam size to allow enough space for an AFM tip running in between the objective and the sample. SGM curves with illumination of 515 nm and 780 nm lasers were recorded. The 515 nm laser, corresponding to 2.4 eV photons, combined with SGM tip assists the electron transport through the NW at the InP segment, where the peaks are located. On the other hand, the 780 nm laser, corresponding to 1.6 eV photons, shows a dip at the InP energy barrier. While the understanding of the behavior is a complex interplay between the interior NWs heterostructure and surface states, it can be concluded that this setup has the potential to reveal the different role of these mechanisms.

7.3 GaSb NWs studied with XPS

As described in 2.3.4, GaSb with its high hole mobility is promising for p-channel. InAs-GaSb NW-based CMOS transistors[42] and TFET[90] – which have been demonstrated with high electrical performance recently[43]. However, the GaSb surface oxide removal is proven to be hard and the knowledge of GaSb surface control is still lacking.

A successful cleaning of GaSb surfaces for both planar substrates and NWs is presented here. Hydrogen plasma treatment in UHV is used and the process is monitored *in-situ* by synchrotron based XPS. Not only performing in the UHV lab scale, but the cleaning technique also needs to be scaled up for industrial fabrication eventually, decoupled from the UHV environment. Since the sample will expose to the air during the fabrication steps, a high-*k* passivation layer as surface protection would be one solution. The ALD technique, giving the surface high degree of uniformity and conformity, is used for passivation here. By implementing a similar H-plasma treatment prior to the actual ALD deposition, the cleaned GaSb surface can directly get protected by the desired high-*k* layer. In the end, we present the correlation of the GaSb surface oxide condition and the performance of the single GaSb NW MOSFET.

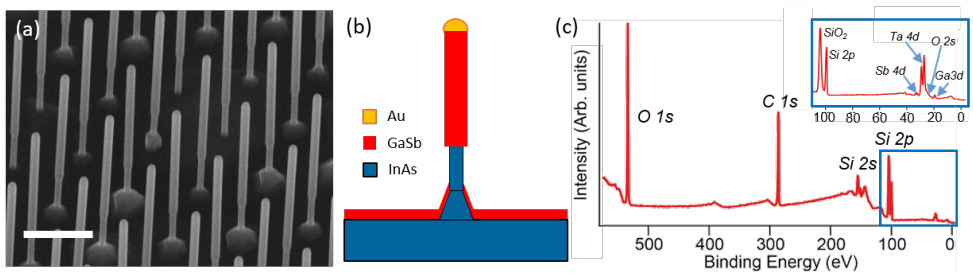


Figure 7-11. (a) SEM image of the NW growth sample. The white scale bar is 500 nm. (b) A schematic diagram of the grown GaSb NW. (c) Overview of XPS shows the (small, but clearly visible) chemical footprint of NWs with native oxide after transfer onto a Si substrate. XPS spectrum acquired at a photon energy of 650 eV.

The NWs, shown in Figure 7-11 (a), are grown on a Si(111) substrate with a 250 nm highly doped InAs layer on top, and the illustration of the grown NW structure is schematic in Figure 7-11 (b). An overview of the XPS spectrum of binding energy from the valence band to 600 eV on the native oxidized NWs is shown in Figure 7-11 (c), however, the intensity of Ga and Sb peaks from the NWs are low. Luckily, the signal gots stronger after the surface oxide removal and that the high brilliance synchrotron light allows high resolution spectra with reasonable integration time.

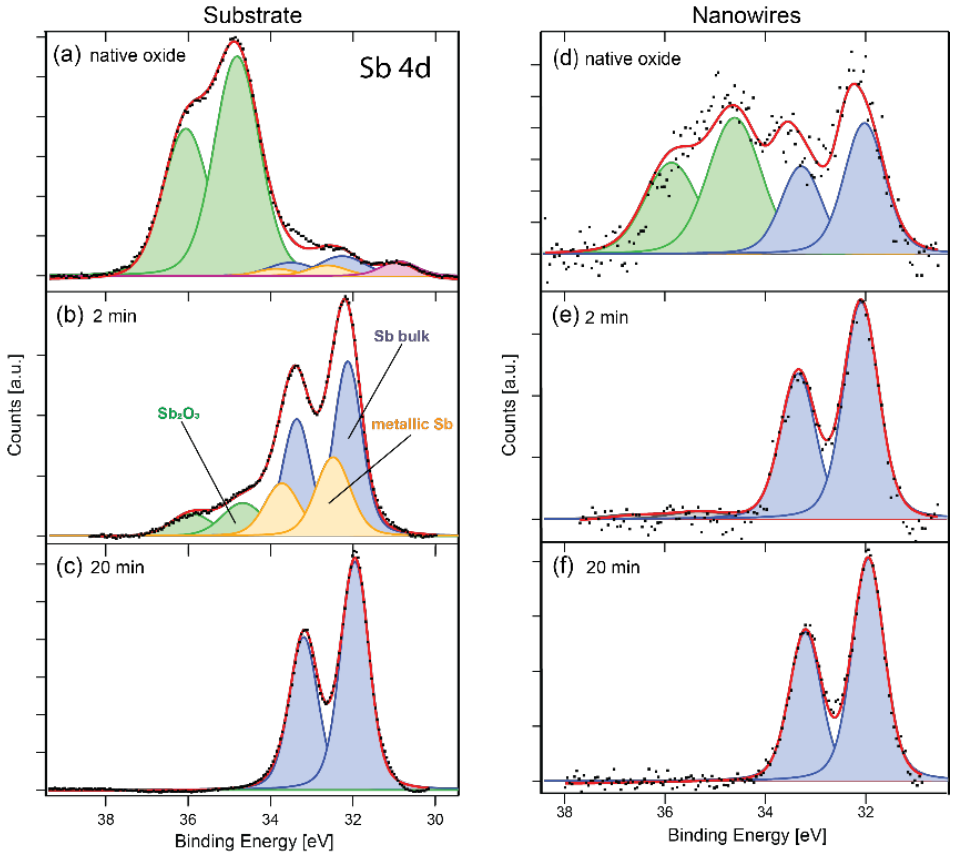


Figure 7-12. XPS spectra of the Sb 4d core level of (a-c) a flat GaSb substrate and (d-f) GaSb NWs, taken at a photon energy of 340 eV. Individual spectra fitted with a doublet corresponding to Sb bound to Ga (blue), a doublet corresponding to metallic Sb (yellow) and a doublet corresponding to Sb-oxide (green). For (a) and (d) samples with native oxide prior to cleaning, (b) and (e) after 2 min, and (c) and (f) after 10 min of cleaning at 200°C plus additional 10 minutes of cleaning at a sample temperature of 250°C. Raw data are displayed as black dots and fitted spectra as red lines. The background of all the spectra has been treated with polynomic background removal.

After *in-situ* hydrogen plasma cleaning, we observe the full removal of all native oxides from the NW surfaces, where the *Sb 4d* core level monitoring is shown in Figure 7-12 (d-f), and *Ga 3d* core level in Figure 7-13 (d-f). On the other hand, the substrate sample is observed with a complete removal of Sb-oxides and a strong Ga-oxides amount reduction after the same cleaning procedure, which data presented in Figure 7-12 (a-c) for *Sb 4d* core level and Figure 7-13 (a-c) for *Ga 3d* core level. The NWs, surprisingly, are easier to get cleaned than the planar substrates. Details of the XPS at each cleaning step and the XPS fittings are in Paper IV. The oxide removal was achieved at a lower sample annealing temperature between 200 - 250°C without any wet chemical pre-treatment.

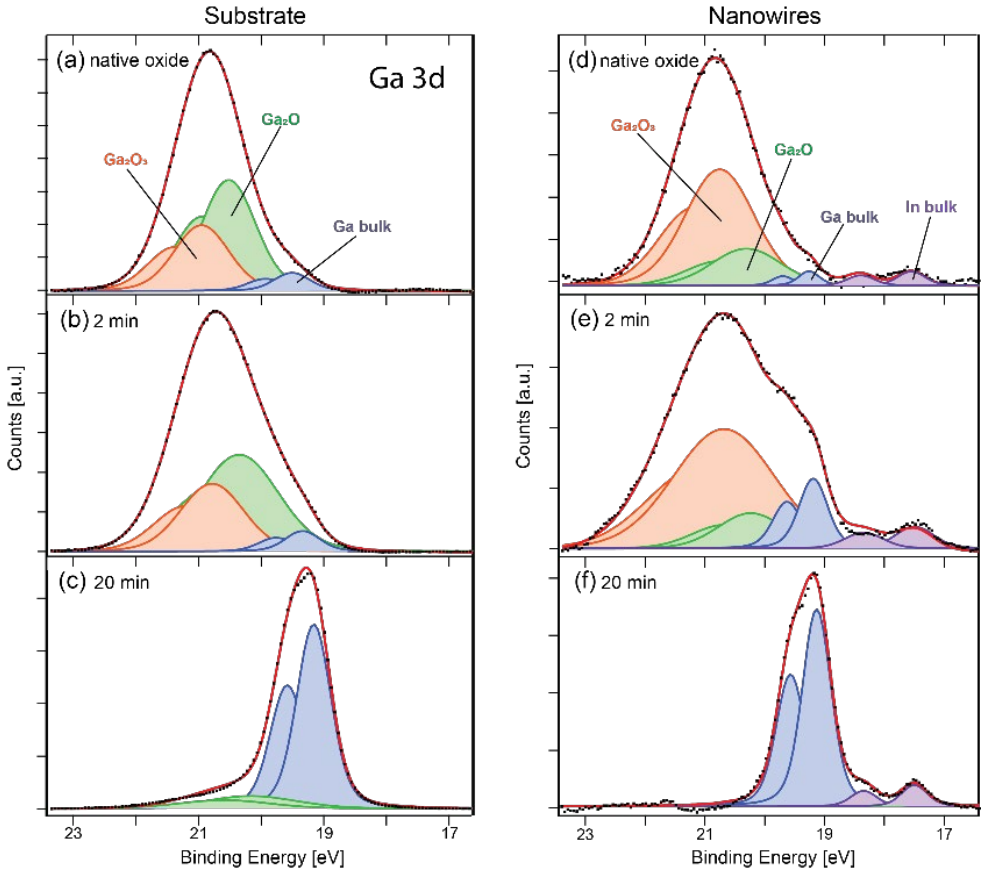


Figure 7-13. XPS spectra of the Ga 3d core level of (a-c) a flat GaSb substrate and (d-f) GaSb NWs, taken at a photon energy of 320 eV. Individual spectra fitted with a doublet corresponding to Ga-Sb (blue), two doublets corresponding to different Ga-oxides (green and orange), and a doublet of In 4d (purple) in the spectra of NWs. for (a) and (d) samples with native oxide prior to cleaning, (b) and (e) after 2 min and (c) and (f) after 10 min of cleaning at 200°C plus additional 10 minutes of cleaning at a sample temperature of 250°C. Raw data are displayed as black dots and fitted spectra as red lines. The background of all the spectra has been treated with polynomic background removal.

The H-plasma pre-treatment followed by ALD process has the limitation that usually the commercial ALD reactors cannot reach the UHV cleanliness level. It is understandable that UHV environment is not efficient enough in both cost and time perspective for industrial processing. We so performed the ex-situ experiment of ALD passivation, using 20 cycles of Al_2O_3 from TMAl and water, on the GaSb surface right after the built-in H-plasma treatment in the same chamber. From the *ex-situ* result, as shown in Figure 7-14, it is clear that the surface cleanliness of the samples prepared by H-plasma pre-treatment in an ALD setup does not reach cleanliness of the *in-situ* UHV H-plasma cleaned samples. Still, the results show reduction on both Sb-oxides and Ga-oxides, and the amount and composition of the interfacial oxide of the ALD samples is comparable with the interfaces of high

performance GaSb-based MOS devices. We suggest that the cleanliness of the ALD environment needs to be improved to make it worth integrating H-plasma cleaning and the H-plasma parameters need to be carefully optimized, to obtain oxide-free GaSb interfaces upon device processing.

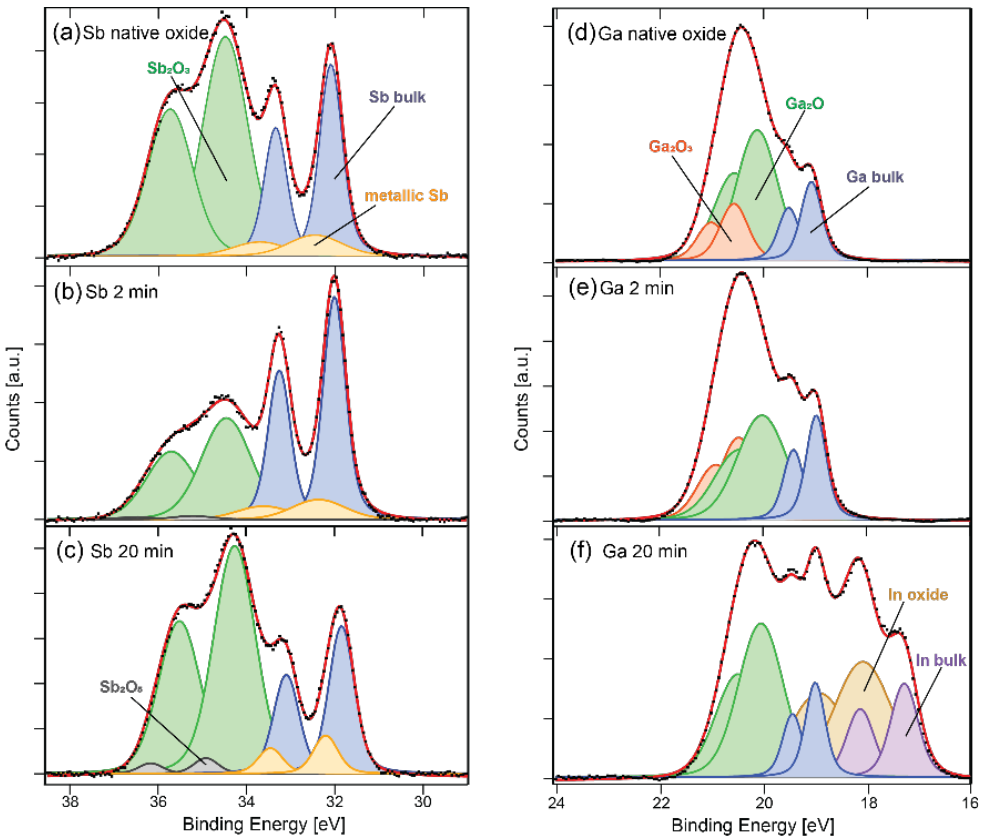


Figure 7-14. XPS data of (a-c) Sb 4d and (d-f) Ga 3d core levels, obtained from (a,d) the GaSb growth substrate after air exposure, i.e. with native oxide, and from samples treated with (b,e) 2 minutes, (c,f) 20 minutes H-plasma prior to ALD of about 2 nm of Al_2O_3. Raw data are displayed as black dots and fitted spectra as red lines, individual fitted doublet components are indicated. The background of all the spectra has been treated with polynomic background removal.

To further prove that the surface oxide removal has high impact on the device performance, we employ digital etch (DE) schemes prior to high-κ deposition on vertical GaSb NW p-channel MOSFETs, which device geometry schematic is shown in Figure 7-15 left. To improve electrostatics of the devices, we examine the surface oxide states after two different processes, buffer-oxide etcher (BOE) 30:1 and HCl:IPA 1:10, by XPS.

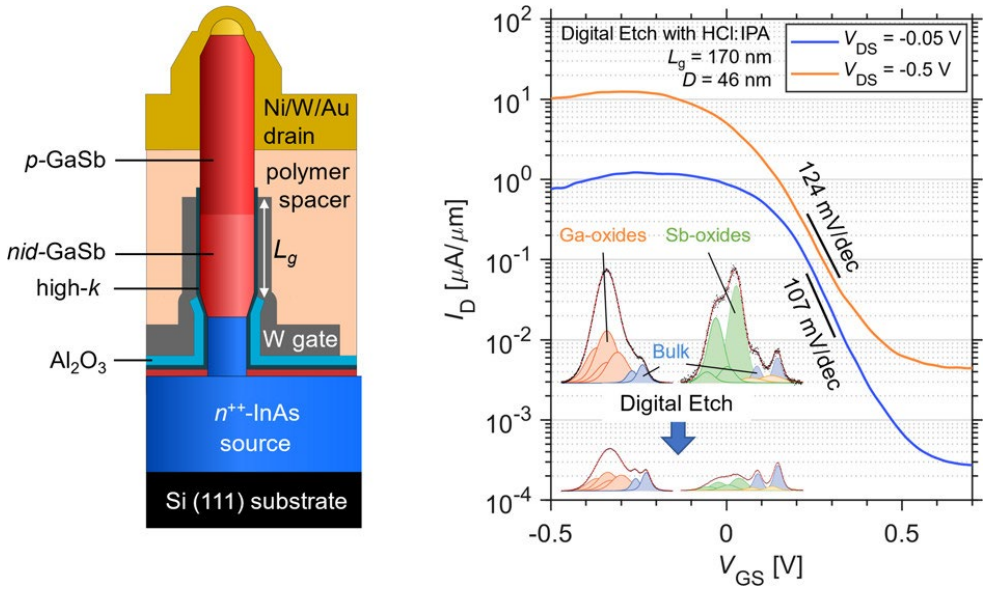


Figure 7-15. Schematic geometry and electrical characterization of the vertical GaSb NW p-channel MOSFETs. Left: Schematic of a single GaSb NW MOSFET with digital etch as the first step of the fabrication prior to ALD. Right: Transfer characteristics of gate voltage V_{GS} sweeping on the NW device with two-cycle DE using HCl:IPA 1:10. Inset: The XPS spectra showing the relative oxide amount of Ga and Sb before and after the DE. Figure from reference [12].

The XPS spectra of *Sb 4d* core level and *Ga 3d* core level before DE, after HCl:IPA, and after BOE treatments are shown in Figure 7-16 (a-c) and (d-f), respectively. The results of the DE followed by ALD on GaSb show improved interface quality of GaSb with a considerable reduction in Sb oxides for both etchants in Figure 7-16 (e,f), while the HCl:IPA lead to a stronger reduction in the Ga oxides, as shown in Figure 7-16 (b). BOE still works as a competent DE that the sample revealed a mild reduction in the amount of Ga oxides, as shown in Figure 7-16 (c), and, again, a significant reduction in the amount of Sb oxides, but the HCl:IPA treatment gives higher level of cleanliness on both Sb and Ga core levels. The result aligns with the electrical characterization showing that the HCl:IPA pretreated sample performs the highest subthreshold swing with a cutting-edge number of 107 mV/dec, as shown in Figure 7-15 right.

By combining this result and the *in-situ* cleaning result in Figure 7-12 and 7-13, a mixed interfacial oxide with mainly Ga^{1+}-oxides and less Ga^{3+}- and Sb-oxides was observed. The relatively low amount of Sb-oxides seems to be important, as Sb-rich interfaces have been reported to be detrimental for electrical device performance[91].

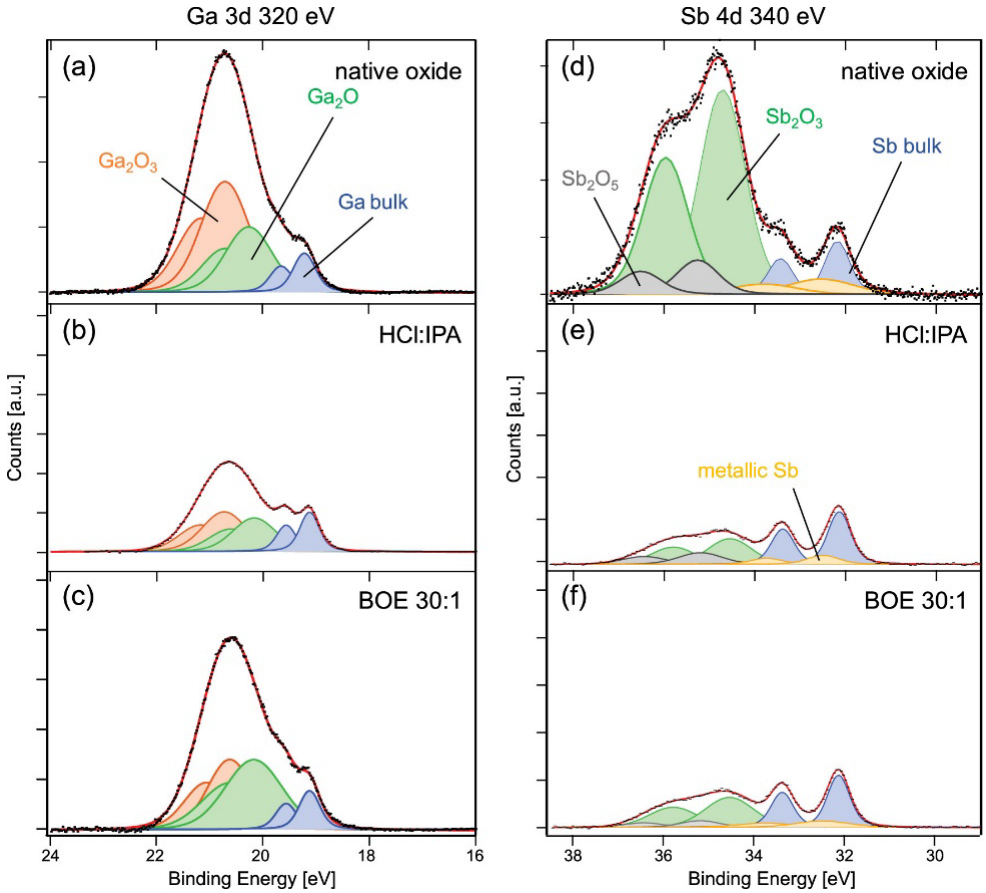


Figure 7-16. XPS data of (a–c) Ga 3d and (d–f) Sb 4d core levels, obtained from (a, d) the GaSb(100) substrate with native oxide (no surface pretreatment); (b, e) a GaSb(100) substrate after HCl:IPA 1:10 etching followed by ALD; and (c, f) a GaSb(100) substrate after BOE 30:1 etching followed by ALD. Raw data are displayed as black dots and fitted spectra as red lines, individual fitted doublet components are indicated. To visualize the oxide removal, intensities from all samples are normalized to the peak heights of the Ga bulk and Sb bulk components, respectively.

7.4 A hybrid material system of 1D InAs NWs and 2D graphene

Hybrid nanomaterials of 2D graphene and 1D III-V NWs combine low dimensional structures with complementary properties. This is another approach to obtain high quality electronics and optoelectronics. However, interface and morphology control for low-dimensional materials are in high degree of importance. The sample preparation and details are shown in Figure 7-17. Graphene can be identified from mono-/bi-/multi-layer by Raman spectroscopy and the contrast in optical microscopy when they are on the Si wafer with 200 nm SiO_2 (before transferring to

InAs substrate). To understand the impact of graphene on III-V NWs, we transfer both single and multiple layer graphene flakes onto InAs NWs on InAs substrate. In this case, we can compare the graphene covered/uncovered InAs in NW geometry and planar substrate. Using AFM to explore the surface geometry, we find that the single layer fold tightly around the wires, as shown in the image and line profiles of Figure 7-18 (a) and (c) where the width difference between covered and uncovered NWs is almost identical. while looking at the multilayer flakes in Figure 7-18 (b) and (d), they fold loosely with a lower slope showing a clear width difference between covered and uncovered parts of the NW.

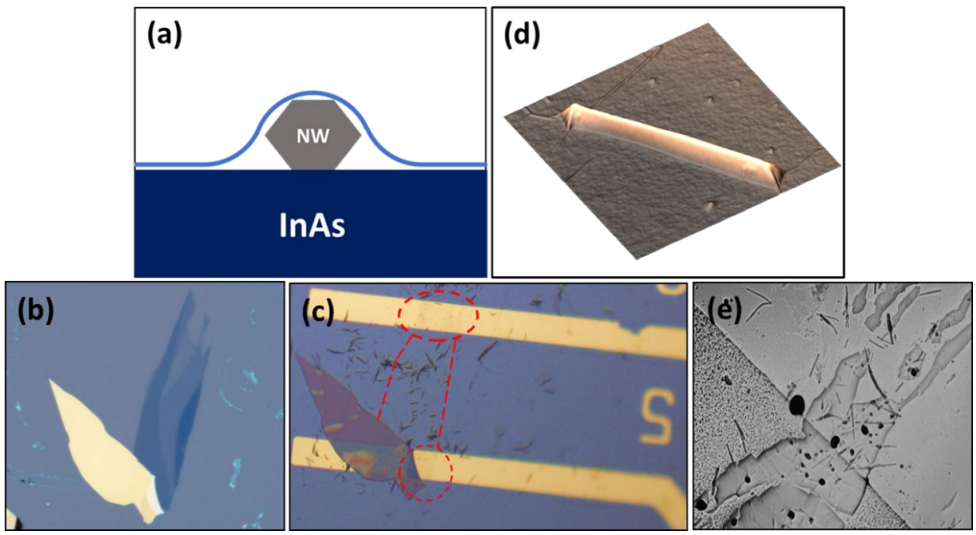


Figure 7-17. Illustration and microscopy images of the InAs NW-graphene samples. (a) Schematic representation of the sample structure. Graphene is folding over an InAs NW placed on an InAs substrate. (b) Graphite and graphene identified on SiO_2/Si. Here, the very bright blue region is single layer graphene. The darker the blue, the thicker the layer. (c) Magnified optical microscopy image, showing gold markers and a graphite flake in vicinity of graphene. While graphene is invisible on an InAs substrate, it can be seen on gold markers (red dashed lines). (d) 3D AFM image of a NW covered with graphene. (e) LEEM image showing graphene, NWs and gold markers clearly.

To investigate the interface chemistry between the graphene and InAs, we use surface sensitive imaging techniques, Low Energy Electron Microscopy (LEEM) and X-ray Photoemission Electron Microscopy (XPEEM) at MAXPEEM in MAX IV, to study interface control by treating the samples with atomic hydrogen cleaning. The Hydrogen cleaning, as described in section 3.6, was performed at a Hydrogen gas pressure in the chamber of 5 x 10-6 mbar, filament thermally cracked at about 1700°C, while the sample is annealed at 400 °C at the same time.

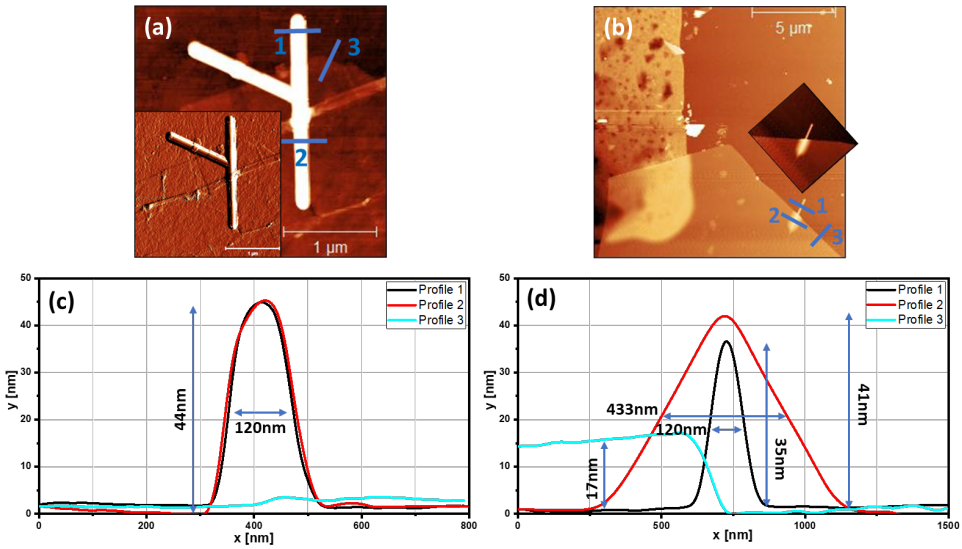


Figure 7-18. AFM on NWs covered with graphene/graphite. a) Two NWs partially covered under thin graphene. Inset: the amplitude mode AFM. b) NW partially covered with graphite flake. Inset: AFM image of the selected region showing the graphite folding over the NW with a better contrast. c) Width comparison between uncovered NW and NW covered with graphene (the distance from the layer to the substrate is 2nm and is shown with profile 3, cyan color). d) Width comparison between covered and uncovered parts of the NW under thick graphite (the distance between the layer and substrate is 17nm as shown with profile 3).

As 3d XPS spectra can then be obtained locally by XPEEM, from identified areas with and without graphene coverage before Hydrogen cleaning, are shown in Figure 7-19 (a,b), respectively. The comparison for the Hydrogen cleaning effect is shown in 7-19 (c,d). After the cleaning procedure the As^{3+} (sky blue) and As^{5+} (yellow) components of the native oxide have disappeared completely, both in the graphene and non-graphene covered area. This show the possibility of cleaning graphene covered materials with a lower melting point around 400 °C. This is important as a previous work reported that Hydrogen treatments underneath graphene can be hindered up to 800 °C[92]. The XPS studies show that the oxide removal using atomic hydrogen is possible under the graphene, but a longer treatment is required to reach a similar result than on a bare surface.

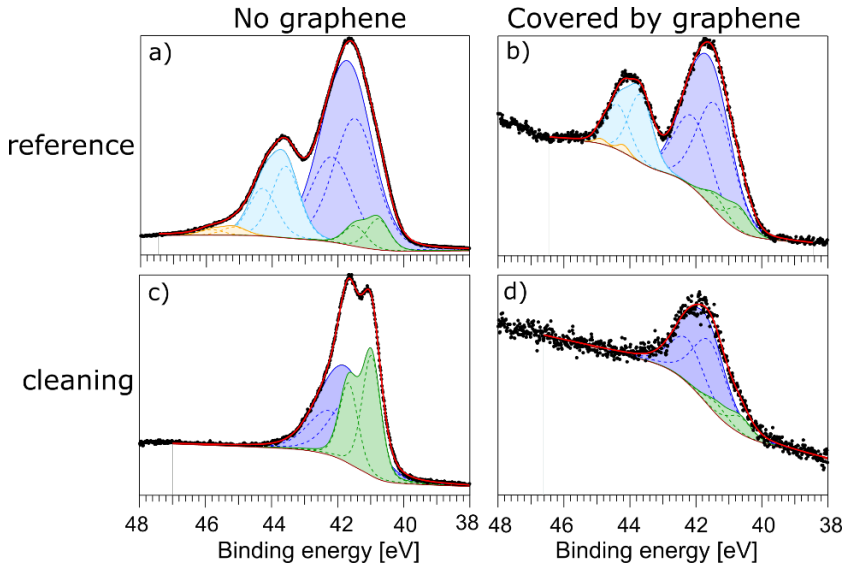


Figure 7-19. As 3d core level spectra obtained from areas in the XPEEM images identified as covered (a,c) and not covered (b,d) by graphene, before (a,b) and after (c,d) hydrogen cleaning.

In conclusion, it is possible to reduce the interfacial native oxide between graphene and the covered InAs substrate and NW using atomic hydrogen cleaning, characterized with XPS and XPEEM. A few/single layer graphene can fold tightly around InAs NWs, and they can stay well intact after the cleaning procedure. Graphene can be widely utilized for wraparound gate electrode, transparent electrode and conjunction to a semiconductor for nano-electronics[93], solar cells[94] and photovoltaic applications[95]. In these applications, the interface control is crucial to enhance efficiency and to avoid carrier scattering or trapping in defects. Thus, the effective cleaning of the hybrid nanostructures demonstrated here open for several applications.

7.5 Single suspended InAs nanosheet devices

Besides the works that have been published or in the manuscript, single suspended InAs nanosheet devices also take part in my PhD work. Due to the fact that the materials can be customized with different aspect ratio and with accurate crystal phase, the InAs nanosheets have attracted great interest for applications. The surface facet can influence the Bi deposition sitting sites[96], and further influence the device performance. The surface topography with different preparations, for example, with native oxide and after Hydrogen treatment, and 0.5 monolayer Bi deposition on the surface, shows that the surface can be cleaned with atomic. We

characterize the suspended InAs nanosheet device transport properties, as shown in Figure 7-23, before and after atomic Hydrogen cleaning. The device transport highly depends on the surface and interface conditions, and the suspended devices would not be limited by the interface trapping state issue, which is reported happening at the interface between InAs nanostructures and SiO_2 layer on the substrate.

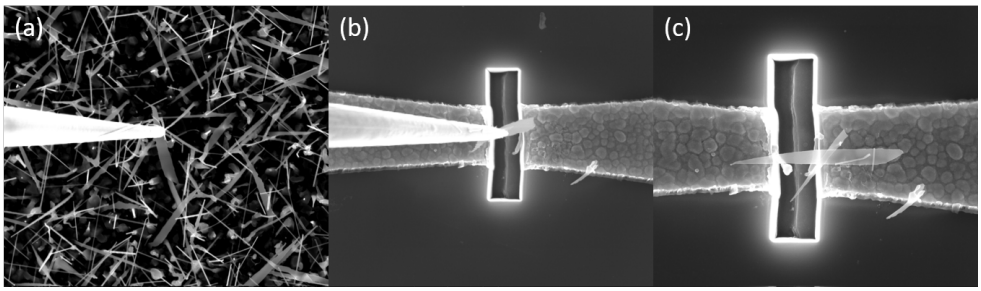


Figure 7-21. SEM images of the InAs nanosheet devices transfer process: (a) approach a W micro-probe to the nanosheet growth sample, and acquire a single piece of the nanosheet with a probe bias of -1.3 V, (c) move the probe to the pre-patterned electrodes, (d) deposit the NW down to the electrodes with a tip bias of 1.1 V, and remove the probe.

Similar to the single suspended NW devices introduced in section 3.5, transferring a nanosheet to the pre-patterned electrodes, as shown in Figure 7-21 (a-c), needs much practice and patience. Different from the NWs, the nanosheets are grown much denser and have much higher contact area than the NWs due to their geometry. Therefore, it is harder to pick only one nanosheet since the grown nanosheets are attached with each other. Further, once the nanosheet is brought to the W micro-probe, it adheres tightly on the probe. A careful adjustment of applied bias and probe-sample orientation for deposition have much higher requirements. Last but not the least, the self-deposited SiO_x layer, as discussed in 3.4, may have more defects than the SiO_2 on the thermal oxide Si wafer, therefore, a single probe press on the electrode can lead to electrical leaking.

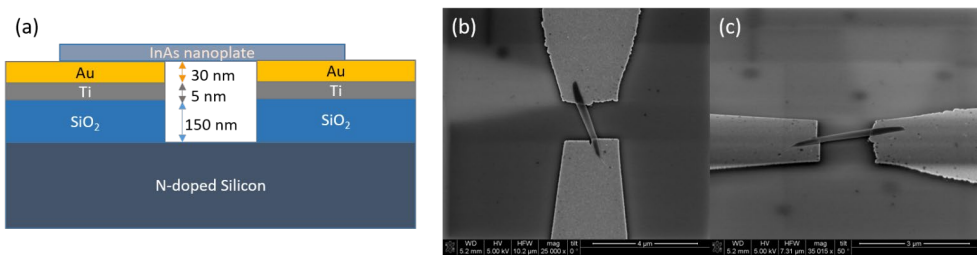


Figure 7-22. Device schematic: (a) Illustration of single suspended nanosheet devices, (b) top view of a well transferred clean nanosheet device, (c) a 52° incident angle tilt view of the device.

The device geometry of the single suspended InAs nanosheet device is shown Figure 7-22 (a), and SEM images of a good electrically isolated device from top view and a tilt view of 52° are shown in Figure 7-22 (b) and (c), respectively. After transferring and exposing in air, the device barely conducts in the voltage range of +/-1V. This could be caused by a poor electrical contact by placing the nanomaterial down or surface residues/oxides limiting the free carrier density. We then anneal the device in UHV for removing the organic residues from the fabrication process. The sample, including the sample holder, de-gas a lot when we ramp up the temperature, so a slow increase in temperature to 130 °C followed by an overnight heating is done as a pre-annealing. Once the pressure in UHV goes back to the normal pressure, in 10^{-10} mbar range, we ramp up to an acquired temperature of 450 °C for one hour to purge out the organic molecules and enhance the contact for the nanosheet and the electrodes. The sample needs to be cooled down and then transferred to the LT-STM chamber of 10 K for electrical characterization. It can be seen from the IV-curve after annealing, shown in Figure 7-23 (a), that the device is non-conducting over a large voltage area from -0.6 V to +0.6 V, but a current at the 0.1 nA scale can be measured for larger absolute voltages. Atomic Hydrogen cleaning as described in section 3.6 is performed at a H_2 pressure of $2x10^{-6}$ mbar with the sample annealed to 450 °C for improving electrical performance, and an IV-curve after H cleaning can be seen in Figure 7-23 (b) where a current of a few nA is obtained already at +/-0.6 V, a voltage at which no conductivity was observed before the H^+ cleaning.

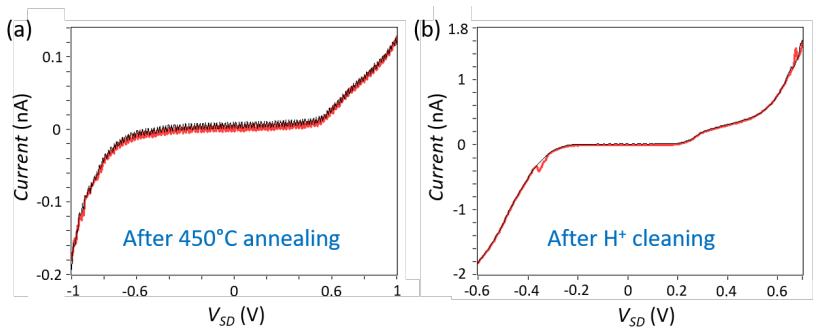


Figure 7-23. Electrical characterization of the InAs nanosheet device (a) after annealing at 130 °C for 10 hours and then at 450 °C for an hour (b) after atomic Hydrogen cleaning for 30 minutes with the device annealed at 450 °C.

After electrical measurements, we start STM navigation at low temperature, as described in section 4.4. The LT-STM has a big analysis chamber, in which the STM part is about 40 cm away from the closest window where we install the camera with a long focus lens. Due to the cooling tower attached to the chamber, vibrations

from the compressor can be linked to the optical lens and camera, and therefore, a relatively hard-to-focus image is obtained in which it is difficult to resolve the fine features of the sample. Nevertheless, enough patience can overcome the difficulty. We can reach the trench and image the morphology of the contact electrodes with the STM, however, no nanosheet was seen across the electrodes after many long-lasting navigations. SEM images of the device before and after STM navigation are seen in Figure 7-24 (b) and (c), respectively. An explosion of the nanosheet seemed to happen, which could be caused by electrical spikes. A test sample with fixed resistor was inserted to the sample receiver, and electrical spikes were found once we move the sample stage. A high voltage unit controls the movement of coarse motors and piezo motors, which is operating at a 160 V range, and the electrical channels for the stage movement are soldered on the D-sub connector shared with sample electrical signals. The crosstalk in 1 V range on the sample can be observed once clicking stage movement on the software, and there is no easy upgrade available at the moment to overcome this problem.

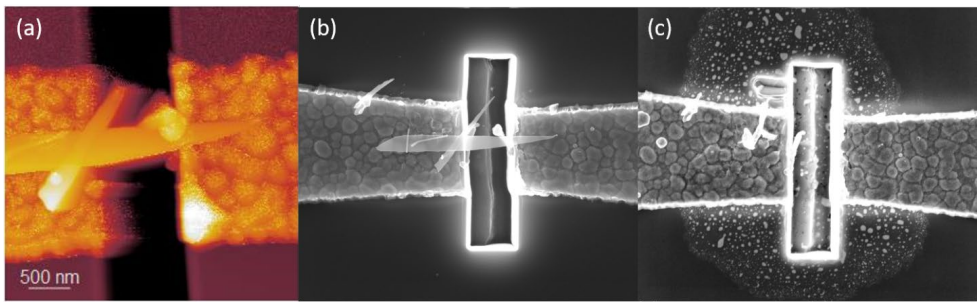


Figure 7-24. InAs nanosheet device after AFM/STM measurements (a) AFM image of the InAs nanosheet device (b) SEM image of the same InAs nanosheet device (c) SEM image of the same InAs nanosheet device after STM measurement.

Chapter 8:
Conclusion and Outlook

In this thesis III-V nanostructures and nano-devices has been studied using a broad range of techniques including in-situ and operando characterization. This is necessary to gain insights into how surfaces and interfaces influence the properties and performance of nano-devices. A lot of work has been centered around developing these methods as in particular direct studies of nanostructured devices is very difficult. As both the characterization method as well as the samples have to be specially tailored for the measurements and measurement strategies that need to be developed, this is time-consuming. However, the thesis has shown that progress can be made and that it is possible to apply a wide range of probe methods onto actual functioning devices. The results of this dissertation has made contributions towards understanding how devices for lower energy consumption and more powerful computation can proceed forward as well as how energy harvesting devices using hot electrons can be understood and then perhaps improved. In particular, the work has centered on solving the pressing technology issues through surface modification and interface engineering. More specifically, the local gating and light excitation using lasers combined with SGM on InAs/InP NW devices help the development of future photovoltaic applications, the surface studies with XPS on GaSb NWs can further improve the efficiency and performance of the computational devices, and the interface treatment and control of lateral $In_xGa_{1-x}As$ NWs and graphene on InAs NW sample makes the lateral NWs for quantum computation and future 1D-2D hybrid material system more feasible.

Finally, I would like to give an outlook of the studies in three aspects, *I.* STM characterization on devices, *II.* SPM combined with lasers, and *III.* XPS on nano-structures.

STM characterization of devices during operation is not trivial and needs many experiences at every step. From the layout design, device fabrication, material growth/transferring to the navigation step, these processes are just the preparation for a real measurement, and each step needs much patience and experience. A real STM measurement on operating devices is very exciting but can be even more challenging. Paper I was the first work that I performed with STM on the lateral III-

V NW device that reports the importance of the surface/interface to the device. A follow up work to continue this study would be measuring with STM on a single functioning lateral NW device, so that transport measurements can be performed in parallel. The single lateral NW could be regarded as part of a future quantum device perhaps even a qubit. Correlating the electrical performance to their surface properties, further help optimizing for the noise free and high quality structures needed for quantum technology. Furthermore, in the InAs NW and nanosheet device work introduced in chapter 7-5, the devices are very different, but the similar technique would apply to all. Now the technique and the experiences are developed, and there are more interesting devices ready to be measured, for example, an InAs-GaSb TFET NW device.

The system with lasers combined with SPM took years for Zhe Ren and me to develop, and now it can run for various kind of measurements, for instance, OBIC, SGM, opto-electrical characterization, electrical probe station with laser assist or spectra detection. Paper II and Paper III use this system, revealing the electron transport with light and gate precision down to nanometer scale. Further studies on power-wavelength dependence of the hot-carrier transport and understanding of the gate-photon combination effect in an InAs/InP NW device would be worth continuing in a more systematic fashion including surface preparation and more devices. During the last measurement described in Paper III, a new IR objective with long working distance was implemented to the optical system, it can focus the laser light down to its diffraction limit in the wavelength range of 400 nm to 1800 nm, plus the possibility with enough space to run the SGM at the same time. With such an opportunity, a double-barrier InAs/InP NW device would be interesting to study, because the focused laser beam can pump the well in between the InP segments, while the gate tip can tune the band structure over the device. Furthermore, broader applications are already going on with the system, for example, p-n junction InP NW devices for wave-guide neuron applications and $PbCsBr_3/PbCsCl_3$ heterojunction Perovskite structures for photovoltaic devices. Not only combining the STM with CW lasers, I also implemented an IR-green pump-probe laser (with our cooperators from Lund Laser Center) to the STM system to detect a two photon-process on GaN substrate with a bandgap of 3.49 eV. Recently, further progress on THz laser combined STM (collaborating with Chemical Physics group) performing on a monolayer WSe_2 sample is going on with this instrument, which is open to wide interesting research possibilities.

XPS is one of the most powerful surface chemistry characterization techniques. During my PhD study, several skills were acquired for large scale facility X-ray measurements, for example, nanomaterials deposition, *in-situ* H^+ cleaning, electrical measurement at the beamline, and so on. The method can be applied to

nanomaterials, too, and it was used in the work described in Papers IV, V and VI. Furthermore, a focused XPS setup, also known as scanning photoelectron microscope (SPEM), was used for device studies, where patterning of markers, contact material choices, *in-situ* operation characterization and a specific sample holder was developed for each beamline that need to be well thought through. Within future research, I would apply this technique widely to operando device studies. There is an example that I got a SPEM beamtime for operando heterojunction $PbCsBr_3/PbCsCl_3$ perovskite device studies performed at ELETTRA, Italy, and further data analysis will be continued.

Many fun experiences were gained in my PhD, for instance, laser beam profile characterization device using InP substrate, Gold on mica for STM tip conditioning, sample preparation and fabrication for all kinds of measurements (STM, ultra-fast laser (femto-second region), Bragg CDI, SPEM, PEEM…), setting up an electrical measurement system for devices in STM, synchrotron beamlines, mega Hertz lab, etc. Every single part of my PhD is intriguing! Due to the very positive experiences of my PhD, I would like to continue the fruitful life in exploring and developing new materials, devices, and ways of characterization to gain research insights into nanoscale devices.

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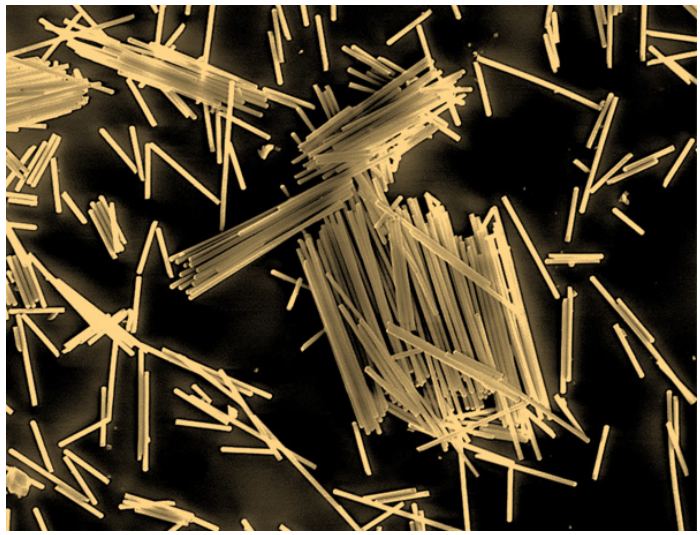

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