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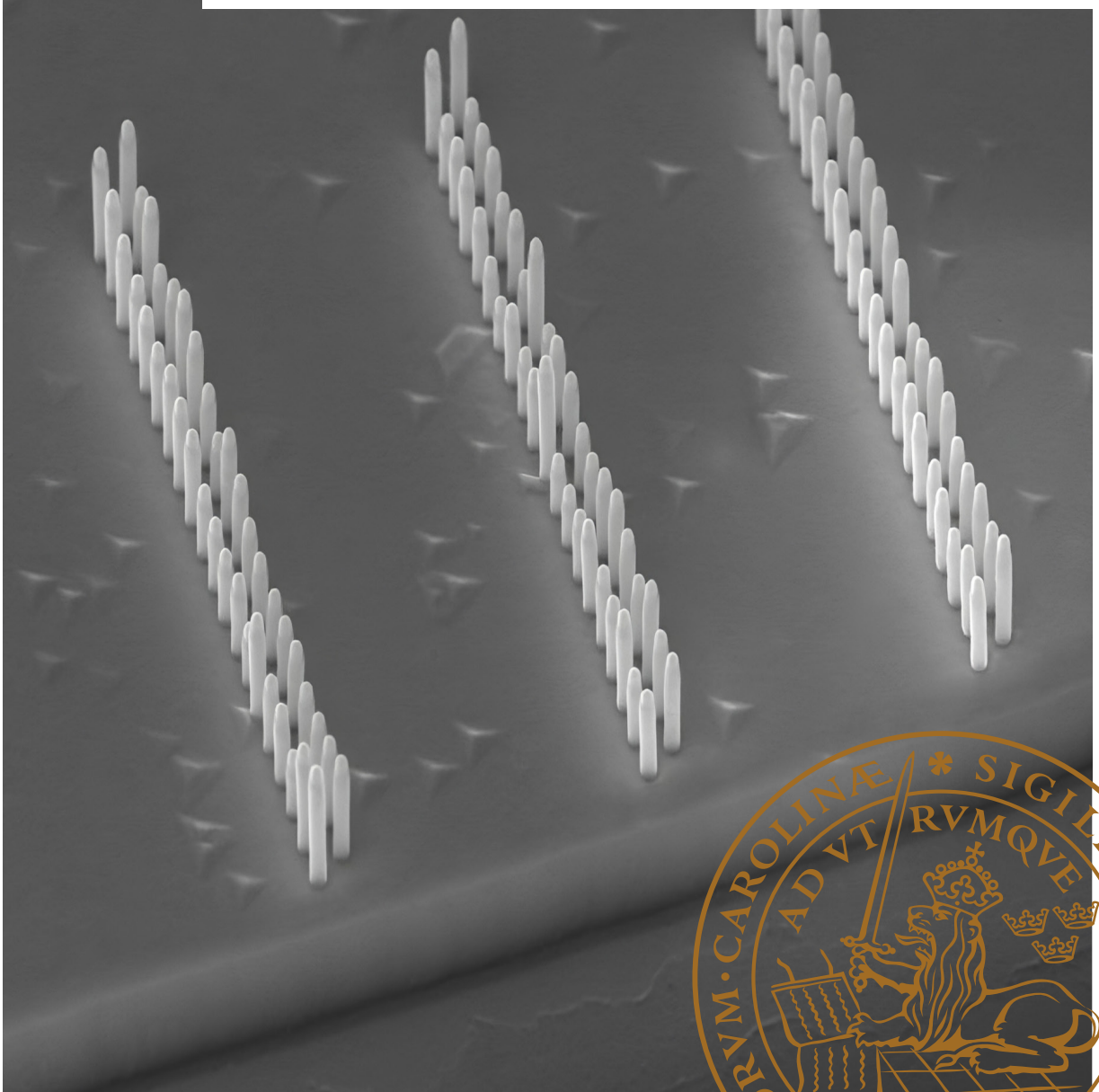

Integration of Ferroelectric HfO_2 onto a III-V Nanowire Platform

Doctoral Thesis

Anton E. O. Persson

LUND
UNIVERSITY

Department of Electrical and
Information Technology
Lund, April 2023

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The fabrication of metal-oxide-semiconductor (MOS) capacitors is treated as well as the measurement methods developed to investigate the interfacial quality to the narrow bandgap III-V materials using both electrical and in-operando synchrotron light source techniques. After optimization of both the films and the top electrode, the gate stack is integrated onto vertical InAs nanowires on Si in order to successfully implement FeFETs. Their performance and reliability can be explained from the deeper physical understanding obtained from the capacitor structures.

By introducing an InAs/(In)GaAsSb/GaSb heterostructure in the nanowire, a ferroelectric tunnel field effect transistor (ferro-TFET) is fabricated. Based on the ultra-short effective channel created by the band-to-band tunneling process, the localized potential variations induced by single ultra-scaled ferroelectric domains and individual defects are sensed and investigated. By intentionally introducing a gate-source overlap in the ferro-TFET, a non-volatile reconfigurable single-transistor solution for modulating an input signal with diverse modes including signal transmission, phase shift, frequency doubling, and mixing is implemented.

Finally, by fabricating scaled ferroelectric MOS capacitors in the front-end with a dedicated and adopted RF and mm-wave backend-of-line (BEOL) implementation, the ferroelectric behavior is captured at RF and mm-wave frequencies.

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Frontispiece: Scanning electron microscopy image of an InAs mesa on silicon with InAs nanowire arrays covered by a ferroelectric zirconium-doped hafnium oxide and tungsten.

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Abstract

The discovery of ferroelectricity in CMOS-compatible oxides, such as doped hafnium oxide, has opened new possibilities for electronics by reviving the use of ferroelectric implementations on modern technology platforms. This thesis presents the ground-up integration of ferroelectric HfO_2 on a thermally sensitive III-V nanowire platform leading to the successful implementation of ferroelectric transistors (FeFETs), tunnel junctions (FTJs), and varactors for mm-wave applications. As ferroelectric HfO_2 on III-V semiconductors is a nascent technology, a special emphasis is put on the fundamental integration issues and the various engineering challenges facing the technology.

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reconfigurable single-transistor solution for modulating an input signal with diverse modes including signal transmission, phase shift, frequency doubling, and mixing is implemented.

Finally, by fabricating scaled ferroelectric MOS capacitors in the front-end with a dedicated and adopted RF and mm-wave backend-of-line (BEOL) implementation, the ferroelectric behavior is captured at RF and mm-wave frequencies.

Populärvetenskaplig sammanfattning

Skiftet från analoga mekaniska lösningar till digitala datorer kallas ofta för den tredje industriella revolutionen i analogi till den första (ångmaskinen) och den andra industriella revolutionen (elektrifieringen och förbränningsmotorn). Oavsett om digitaliseringen ska tillskrivas samma vikt som ångmaskinen och elektrifieringen, så råder det ingen tvekan om att elektronikutvecklingen har haft och kommer att ha en stor påverkan på vårt samhälle. Nu börjar det talas om en fjärde industriell revolution som kännetecknas av en fusion av teknologier som suddar ut gränserna mellan de traditionellt digitala och biologiska sfärerna.

När man blickar framåt så börjar den tekniska forskningen tala om kvantdatorer, sakernas internet och elektriska kretsar som efterliknar den mänskliga hjärnan. En anledning till detta är att elektronikindustrin under flera decennier har förlitat sig på att beräkningskraft och effektivitet förbättras genom att minska kiseltransistorers storlek (den så kallade Moores lag). På grund av kostnaden för fortsatt nedskalning och kvantmekaniska effekter som orsakar problem vid dessa storleksordningar så har denna utveckling saktat in. Utvecklingen av elektronik rör sig därför in på okänt territorium, vilket kräver nya material, komponenter och kretsarkitekturer. Denna tes berör dessa frågeställningar och undersöker möjligheterna att kombinera så kallade ferroelektriska material med III-V material för att möjliggöra nya komponenter och kretsarkitekturer.

Ett ferroelektriskt material är en elektrisk motsvarighet till de ferromagnetiska material som bildar det vi i vardagligt tal kallar för magneter. Men i stället för en magnetisk nordpol respektive sydpol, så bildas istället elektriska

poler med en positiv respektive negativ laddning på var sin sida av materialet. Dessa attraherar och repellerar negativ respektive positiv laddning i omkringliggande material. Precis som när nordpolen och sydpolen byter plats på en magnet genom ett pålagt magnetfält (såsom i datorhårddiskar) så kan ett ferroelektrisk materials positiva och negativa sida byta plats genom en pålagd spänning. I analogi med hårddiskars ferromagnetiska minnen så kan man därigenom skapa ferroelektriska minnen. III-V material är liksom kisel halvledare och fyller en kompletterande roll inom elektroniken då de har vissa avgörande egenskaper som gör dem väl lämpade till högfrekvenselektronik samt i lågeffektselektronik för mycket energieffektiva applikationer.

I denna tes undersöks nya ferroelektriska minnen, i form av ferroelektriska transistorer och ferroelektriska tunnlingsbarriärer, för nya kretsarkitekturer. Dels undersöks deras funktion såsom memristorer, d.v.s. resistorer vars resistans kan ändras och sedan "minnas" av komponenten, och dels i form av en rekonfigurerbar komponent för högfrekvenselektronik. Målet är att kunna åstadkomma så kallade neuromorfa kretsar, d.v.s. kretsar anpassade för artificiell intelligens genom att de i sin uppbyggnad efterliknar den mänskliga hjärnan med synapser (memristorer) och neuroner.

Acknowledgments

DURING the years leading up to this thesis, I have had the opportunity to work with a lot of great and inspiring people. First and foremost, thank you *Lars-Erik Wernersson* for offering me this journey. Without your expertise and inspiring discussions, I would never have reached the end of it. I also want to thank my second supervisor *Mattias Borg* who always had the door open and answered my barrage of questions.

A great thank you to *Robin Athle* who were the first to join me on this ferroelectric endeavor and who more than anyone has listen to my problems. *André Andersen*, *Hannes Dahlberg*, and *Zhongyunshen Zhu* may have joined the endeavor later, but your contributions to ferroelectricity in Lund are equally important! A big thank you to *Erik Lind* to whom I often went with my trickiest questions and to my surprise often answered them. A big thank you to *Johannes Svensson*, *Olli-Pekka Kilpi*, and *Karl-Magnus Persson* to whom I owe most of my cleanroom skills! And to *Lars Ohlsson Fhager* who has spent more hours than I want to admit teaching me how to perform proper electrical measurements. Thank you, *Saketh Ram Mamidala* for the early days of my PhD when you stayed happy even at midnight in the lab!

The group is big and writing memories for all of you would go beyond the scope of this thesis. But I would like to thank all of my colleagues for these years. Not only have we spent countless hours in the lab and office together, but we have also become good friends and enjoyed many non-work activities together. To the remaining co-workers *Andrea, Stefan, Markus, Gautham, Adam, Marcus, Anette, Abinaya, Lasse, Heera, Fredrik, Navya, Philipp, Duc, Patrik, Louise, Sebastian, Pramoda, Tobias, Ben, Niklas, Alexandros, Johan, Daniel*, and *Mats*: a big thank you for this time! I have also had great collaborations with people outside of my own department who have taught me about synchrotron measurements. *Austin, Rainer, Yen-Po, Zhihua, Sandra*, and *Anders*, thank you!

I have had many teachers inspiring me throughout the years and even if all of you should be acknowledged, a special thank you goes to *Eva*, *Nedzad*, *Per*, *Bengt-Olof*, and *Jonas* who made physics, chemistry, and mathematics my favorite topics in school! I would also like thank the professors of Chalmers who built my basis in physics and the professors of TU Munich who inspired me into choosing a path towards semiconductor devices. A big thank you to *Eva Olsson* to whom I owe my choice of an academic career. Without you believing in me, I would never have discovered academia!

I would also like to thank *Martin, Martin*, and *Antti* for being great and loyal floorball players.

My grandfathers *Erkki* and late *Olle* who during my early days showed me their workshops and made me want to become an inventor. A special thanks goes to *Clara*, for all your love and care, even in the most stressful moments. And my parents *Arne* and *Marja* who have been my biggest cheerleaders throughout the years. You deserve the biggest thanks!

Lund, April 2023

Contents

Preface

This thesis is the culmination of more than five years of work in the *Electromagnetics and Nanoelectronics* division at the Department of Electrical and Information Technology, Lund University, and investigates the functional integration of ferroelectric hafnium oxide onto III-V nanowires for various ferroelectric device implementations. The work was supervised by Professor *Lars-Erik Wernersson* and Associate Professor *Mattias Borg*.

STRUCTURE OF THE THESIS

This is a compilation thesis, meaning that it is a collection of research papers with an introductory section providing a summary of the research field comprehensible for aspiring researchers with a M.Sc. degree interested in pursuing similar research. The appended publications form the main body of the thesis.

- **INTRODUCTION**
  The aim of the introduction is to provide a broader and more comprehensive view than the focused publications that are written for researchers in the field. That is, the textbook required for someone with a general physics and electronics background to be able to understand most of the content in the appended publications. I expect the reader to have a basic prior knowledge of semiconductors, electronic devices, and material characterization techniques.

- **PAPERS**
  The papers forming the main body of the thesis are reproduced in the back and listed in the following section.

INCLUDED PAPERS

The following papers form the main body of this thesis and the respective published or draft versions are appended in the back.

Paper I: A. E. O. Persson, Z. Zhu, R. Athle, and L.-E. Wernersson, "Integration of ferroelectric $Hf_xZr_{1-x}O_2$ on Vertical III-V Nanowire Gate-all-around MOSFETs on Silicon", *IEEE Electron Device Letters*, vol. 43, pp. 854-857, May 2022, doi: 10.1109/LED.2022.3171597.

► *I developed the process flow, fabricated the structures, carried out all measurements and analyses and wrote the paper.*

Paper II: A. E. O. Persson, R. Athle, J. Svensson, M. Borg, and L.-E. Wernersson, "A method for estimating defects in ferroelectric thin film MOSCAPs", *Applied Physics Letters*, vol. 117, pp. 242902, Dec 2020, doi: 10.1063/5.0029210.

► *I developed the process flow, fabricated the structures, carried out all measurements and analyses and wrote the paper.*

Paper III: A. E. O. Persson, R. Athle, P. Littow, K.-M. Persson, J. Svensson, M. Borg, and L.-E. Wernersson, "Reduced annealing temperature for ferroelectric HZO on InAs with enhanced polarization", *Applied Physics Letters*, vol. 116, pp. 062902, Feb 2020, doi: 10.1063/1.5141403.

► *I developed the process flow, fabricated the structures, carried out all measurements and analyses and wrote the paper.*

Paper IV: A. E. O. Persson, S. Andrić, and L.-E. Wernersson, "Millimeter-Wave Characterization of Ferroelectric MOS Capacitors", Manuscript in preparation.

► *I fabricated the structures, helped measure the sample, analyzed parts of the results, and wrote the paper.*

Paper V: R. Athle, A. E. O. Persson, A. Troian, and M. Borg, "Top Electrode Engineering for Freedom in Design and Implementation of Ferroelectric Tunnel Junctions Based on $Hf_xZr_{1-x}O_2$", *ACS Applied Electronic Materials*, vol. 4, pp. 1002-1009, Feb 2022, doi: 10.1021/acsaelm.1c01181.

► *I helped develop the process flow, the measurement methods, the analyses, and the writing of the paper.*

Paper VI: A. Andersen, A. E. O. Persson, and L.-E. Wernersson, "As-deposited ferroelectric HZO on a III-V platform", *Applied Physics Letters*, vol. 121, pp. 012901, Jul 2022, doi: 10.1063/5.0097462.

► *I developed the process flow, and helped fabricate the structures, carry out the measurements, the analyses, and the writing of the paper.*

Paper VII: H. Dahlberg, A. E. O. Persson, R. Athle, and L.-E. Wernersson, "Ferroelectric-Antiferroelectric Transition of $Hf_{1-x}Zr_xO_2$ on Indium Arsenide with Enhanced Ferroelectric Characteristics for $Hf_{0.2}Zr_{0.8}O_2$", *ACS Applied Electronic Materials*, vol. 4, pp. 6357-6363, Dec 2022, doi: 10.1021/acsaelm.2c01483.

▶ *I developed the process flow, and helped fabricate the structures, carry out the measurements, the analyses, and the writing of the paper.*

Paper VIII: R. Athle, A. E. O. Persson, A. Irish, H. Menon, R. Timm, and M. Borg, "Effects of TiN Top Electrode Texturing on Ferroelectricity in $Hf_{1-x}Zr_xO_2$", *Applied materials & interfaces*, vol. 13, pp. 11089-11095, Feb 2021, doi: 10.1021/acsami.1c01734.

▶ *I helped develop the process flow, the measurement methods, the analyses, and the writing of the paper.*

Paper IX: Z. Zhu, A. E. O. Persson, and L.-E. Wernersson, "Sensing single domains and individual defects in scaled ferroelectrics", *Science Advances*, vol. 9, pp. eade7098, Feb 2023, doi: 10.1126/sciadv.ade7098.

▶ *I developed the process flow, helped in the fabrication, the measurement methods, the analyses, and the writing of the paper.*

Paper X: Z. Zhu, A. E. O. Persson, and L.-E. Wernersson, "Signal Modulation in a Ferroelectric Tunnel Field-Effect Transistor", accepted in *Nature Communications*.

▶ *I developed the process flow, helped in the fabrication, the measurement methods, the analyses, and the writing of the paper.*

Paper XI: A. Irish, A. E. O. Persson, V. Flodgren, R. Athle, L.-E. Wernersson, and R. Timm, "Switching Dynamics and Interface Chemistry of Ferroelectric Hafnia Devices", Manuscript in preparation.

▶ *I developed the process and did the fabrication, performed the electrical measurements, and helped with analysis and writing of the paper.*

RELATED WORK

The following publication is not included in the thesis, but is a related work that I was involved in.

Paper I: R. Athle, T. Blom, A. Irish, A. E. O. Persson, L.-E. Wernersson, R. Timm, and M. Borg, "Improved Endurance of Ferroelectric $Hf_{1-x}Zr_xO_2$ Integrated on InAs by using Millisecond Annealing", *Advanced Materials Interfaces*, vol. 9, pp. 2201038, Aug 2022, doi: 10.1002/admi.202201038.

► *I helped develop the process flow, the measurement methods, the analyses, and the writing of the paper.*

Acronyms and Symbols

Here, important acronyms, abbreviations, and symbols are listed, which are recurring throughout the thesis. Some parameters, which only occur in a narrow context, are intentionally omitted; some parameters are used in more than one way, but the context is always explicitly clarified in the corresponding text. Some (compound) units are provided with prefixes to reflect the most commonly encountered notations in literature.

ACRONYMS AND ABBREVIATIONS

1T1C	One-transistor, One-capacitor
AC	Alternating current
AFM	Atomic force microscopy
ALD	Atomic layer deposition
BCB	Benzocyclobutene
BEOL	Back end of line
BERT	Bit error tester
BOE	Buffered oxide etch, a mixture of NH_4F, HF, and H_2O
CMOS	Complementary metal–oxide–semiconductor
CPU	Central processing unit
CPW	Coplanar waveguides
CSD	Chemical solution deposition
CV	Capacitance-voltage
DC	Direct current

DRAM	Dynamic random-access memory
EBL	Electron beam lithography
EBSD	Electron backscatter diffraction
EDX	Energy-dispersive X-ray spectroscopy
FeFET	Ferroelectric field-effect transistor
FEOL	Front end of line
FeRAM	Ferroelectric random-access memory
FIB	Focused ion beam
FLA	Flash lamp annealing
FTJ	Ferroelectric tunnel junction
GIXRD	Grazing incidence X-ray diffraction
HAXPES	Hard X-ray photoelectron spectroscopy
HEMT	High-electron-mobility transistor
HSQ	Hydrogen silsesquioxane
HZO	Zr-doped HfO_2, $Hf_xZr_{1-x}O_2$
IC	Integrated circuit
ICP	Inductively coupled plasma
IMPF	Inelastic mean free path
KAI	Kolmogorov-Avrami-Ishibashi model
LRRM	Line-Reflect-Reflect-Match
MIM	Metal insulator metal
MIMCAP	Metal insulator metal capacitor
MLA	Maskless aligner
mm-wave	Millimeter wave (30–300 GHz)
MOS	Metal oxide semiconductor
MOSCAP	Metal oxide semiconductor capacitor
MOSFET	Metal oxide semiconductor field effect transistor
MOVPE	Metalorganic vapor phase epitaxy
MW	Memory window
nid	Non-intentionally doped
NLS	Nucleation limited switching
PCM	Phase change memory
PFM	Piezoresponse force microscopy

PLD	Pulsed laser deposition
PUND	Positive-Up-Negative-Down
PV	Polarization-voltage
PZT	Lead zirconate titanate, $Pb(Zr_{1-x}Ti_x)O_3$
RF	Radio frequency
RIE	Reactive ion etching
RRAM	Resistive random-access memory
RT	Room temperature
RTA	Rapid thermal anneal, synonymous with RTP
RTN	Random telegraph noise
RTP	Rapid thermal processing, synonymous with RTA
SEM	Scanning electron microscope
SPM	Scanning probe microscopy
SRAM	Static random-access memory
SRAM	Scanning transmission electron microscope
STT-MRAM	Spin-transfer-torque magnetic random-access memory
TEM	Transmission electron microscope
TER	Tunnel electroresistance
TFET	Tunnel field-effect transistor
TFR	Thin-film resistor
UV	Ultraviolet
VLS	Vapor-liquid-solid
WGFMU	Waveform generator module
XPS	X-ray photoelectron spectroscopy

LATIN SYMBOLS

$\boldsymbol{A}$	m^2	Area
$\mathbf{Al_2O_3}$		Aluminum Oxide
$\boldsymbol{D}$	$C\,m^{-2}$	Displacement field
$\boldsymbol{E}$	$V\,m^{-1}$	Electric field

E_C	$\mathrm{MV\,cm^{-1}}$	Coercive field
E_F	eV	Fermi Level Energy
E_g	eV	Band Gap
f	Hz	Frequency
GaSb		Gallium Antimonide
I	A, A	Current
I_D	A, $\mathrm{mA\,\mu m^{-1}}$	Drain Current, often normalized by the gate width
I_{DS}	A, $\mathrm{mA\,\mu m^{-1}}$	Source-to-Drain Current, often normalized by the gate width
I_G	A, $\mathrm{mA\,\mu m^{-1}}$	Gate Current, often normalized by the gate width
InAs		Indium Arsenide
I_S	A, $\mathrm{mA\,\mu m^{-1}}$	Source Current, often normalized by the gate width
k_B		$\approx 1.381 \times 10^{-23}\ \mathrm{kg\,m^2\,K^{-1}\,s^{-1}}$, Boltzmann Constant
L_G	m	Gate Length
m_0		$\approx 9.109 \times 10^{-31}$ kg, Electron Rest Mass
P	$\mathrm{\mu C\,cm^{-2}}$	Polarization
P_R	$\mathrm{\mu C\,cm^{-2}}$	Remanent polarization
Q	C	Charge
q		$\approx 1.602 \times 10^{-19}$ C, Elemental Charge
TDMAHf		Tetrakis(dimethylamido)hafnium
TEMAZr		Tetrakis(ethylmethylamido)zirconium
V_{DS}	V	Drain-to-Source Voltage
V_{GS}	V	Gate-to-Source Voltage
V_T	V	Threshold Voltage

GREEK SYMBOLS

ε_0	$\approx 8.854 \times 10^{12}\ \mathrm{F\,m^{-1}}$, Vacuum permittivity
ε_r	Relative permittivity
κ	Relative Permittivity
χ_e	Electric susceptibility

INTRODUCTION

1

Background

"One should not work on semiconductors, that is a filthy mess; who knows whether there are semiconductors at all!"

Wolfgang Pauli, 1931

When researchers started investigating the theory of electronic conduction in semiconductors in the early 1930s, they had no idea that they were soon to change the lives of future generations. They laid the foundation for the perhaps most important invention of the century, the transfer resistor (transistor) by Bardeen, Brattain, and Shockley in 1947, i.e., a device in which the electrical current between two electrodes can be controlled by a third electrode. The transistor is the most important device in electronics and constitutes the foundation of the digital revolution, also known as the third industrial revolution. It has truly revolutionized society by providing an incredible increase in computational power, memory storage, and transfer of information. On its own, a transistor can serve as a signal amplifier, which is very important for communication engineering. But it was not until the late 1950s and the invention of the integrated circuit (IC) that the true impact would be felt. By integrating a number of transistors as one indivisible unit, rather than interconnected after individual device fabrication, the cost of advanced circuits could be dramatically decreased [1].

Until the 1980s, the dominating technology was the bipolar transistor, but its power consumption became unsustainable, and the industry instead moved to the self-aligned silicon metal–oxide–semiconductor field-effect transistor (MOSFET) that was first invented in 1960. With this came the com-

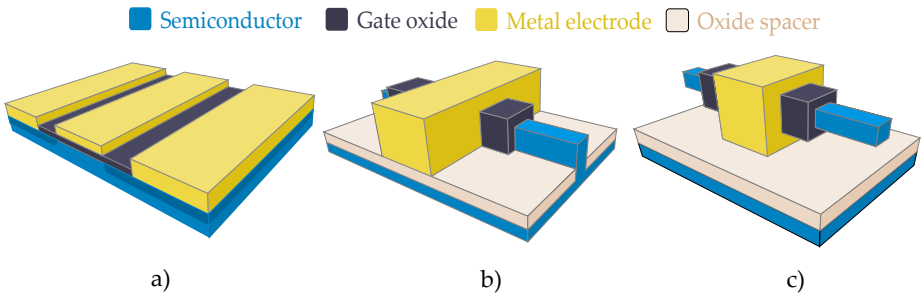


Figure 1.1: Schematic representations of a) a planar MOSFET, b) a tri-gate MOSFET in which the gate covers three sides of the semiconductor instead of one, and c) a gate-all-around structure in which the gate covers all sides of the semiconductor.

plementary metal-oxide-semiconductor (CMOS) technology that is still the workhorse of the semiconductor industry [2]. Further technological development has relied on an incremental downscaling of silicon MOSFETs that for each new generation has improved speed, power efficiency, and fabrication cost. In 1965, the CEO of Intel, Gordon Moore, predicted that the number of transistors in an IC would double every other year for the coming decade [3]. This, perhaps self-fulfilling prophecy, has basically remained true until today and there are nowadays ICs with trillions of transistors [4]. The total number of transistors ever fabricated was in 2018 estimated to be ~1.3×10^{22}, i.e., the most fabricated thing in the history of humanity [5]. Given the exponential yearly growth, it is reasonable to assume that the number by great margin is bigger than both the number of grains of sand on planet Earth (~8×10^{18}) [6] and similar to the number of stars in the known universe ($3 - 7 \times 10^{22}$) [7].

Even if the CMOS technology has prevailed, the massive size downscaling has meant considerable changes to the transistor design and the used manufacturing processes. In 1974, Robert Dennard and IBM colleagues introduced the geometric MOSFET scaling rules that steered the development for decades [8]. While keeping the general planar structure of the MOSFET the same, Fig. 1.1a), the physical gate length of transistors shrunk from 1 µm in 1974 to 35 nm in 2003, whereas the clock frequency increased from 2 MHz to 3 GHz. But in the beginning of the 2000s, Dennard's scaling laws had made the threshold voltage so low that the off-state leakage current made the standby power unsustainable whereas an increasingly thinner gate oxide (~1.2 nm SiO_2) caused gate leakage through quantum mechanical tunneling. A new approach was needed, and the research field changed to the equivalent scaling era. The SiO_2 gate oxide was exchanged with alternative high permittivity (high-κ) materials such as HfO_2 and the geometry was, as shown in Fig. 1.1, changed

from planar to nonplanar multigate architectures. This allows for superior electrostatic control of the channel and since the electronic conduction occurs on three sides of the fin, the current per chip area increases [9]. The tri-gate FinFET remained the flagship design until 2022, when Samsung finally moved over to a gate-all-around approach using nanosheets as in Fig. 1.1c) in order to increase the electrostatic control of the channel even further [10].

1.1 THE FUTURE OF ELECTRONICS

Through incremental downscaling, new materials, and innovative architectures, transistors have become a powerful tool whose impact will continue to shape the future. The current trends point towards stacking several gate-all-around structures on top of each other to further increase current per chip area, and even stacking NMOS and PMOS devices on top of each other. According to the latest version of the International Roadmap for Devices and Systems 2022 (IRDS) [11], i.e., the leading roadmap for electronics development, the outlined approaches are expected to keep up development for the coming decade. But the silicon MOSFET scaling is coming to an end. To enable computing system advances, IRDS predicts that new types of devices and circuit architectures are required by the end of the 2020s. Ferroelectric transistors and memristors for neuro-inspired computing are mentioned among the most promising technologies, whereas Ge and III-V materials are mentioned as leading semiconductor candidates to complement Si.

The work presented in this thesis is positioned at the center of this development and involves research on ferroelectric integration on III-V materials and its applications. Below, the case for III-V materials in MOSFETs, tunnel field-effect transistors (TFETs), and neuromorphic circuit architectures is made while the topic of ferroelectricity has been granted its own chapter.

1.1.1 III-V NANOWIRES

III-V compound semiconductors are alloys of elements from groups III (B, Al, Ga, and In) and V (N, P, As, and Sb) in the periodic table of elements. The mobility of III-V materials, i.e., how fast an electron moves through a material under an applied electric field, is several times that of silicon making them well suited for high-frequency electronics as this property decides how fast electrons can cross the channel of a transistor [12]. Faster means a quicker response to a varying gate potential and this has enabled III-V high-electron-mobility transistors (HEMTs) to excel in high-frequency applications having an operational frequency above 1 THz [13].

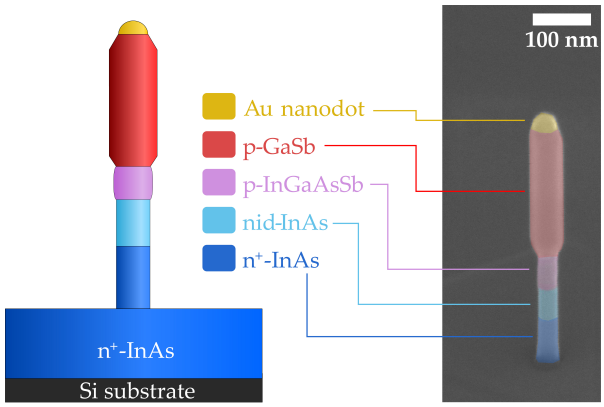


Figure 1.2: a) A schematic of a VLS-grown III-V nanowire with a complex heterostructure and b) a corresponding scanning electron microscope (SEM) image of the structure.

In this thesis, III-V nanowires similar to the one depicted in Fig. 1.2 are used for all transistor implementations. Besides the outstanding carrier transport properties of III-V semiconductors combined with the optimal gate-all-around geometry for electrostatic control, the vertical implementation is beneficial as it decouples contact and channel length from the chip footprint. This enables dense implementation of devices, even for relatively large contacts and long gate lengths. Furthermore, as indicated by Fig. 1.2, the vertical geometry enables advanced semiconductor heterostructures as the strain from mismatched lattice constants can relax radially. Thereby, advanced band structures can be achieved, which in this thesis is utilized for implementing the energy-efficient steep-slope devices described below in section 1.1.2. For compatibility with industrial fabrication methods, all nanowire devices in this thesis are integrated on standard silicon substrates.

1.1.2 UNCONVENTIONAL TRANSISTORS

As schematically indicated in Fig. 1.3a), the current flow in a conventional MOSFET is modulated by the height of the potential barrier in the channel region which is changed by the gate voltage. Only charge carriers with an energy higher than the top of the barrier contributes to the current, but as the charge carriers follow Boltzmann statistics, high-energy electrons in the tail of the distribution are injected across the channel even in the off-state. This causes a thermal limit (the so-called Boltzmann tyranny) for which the gate

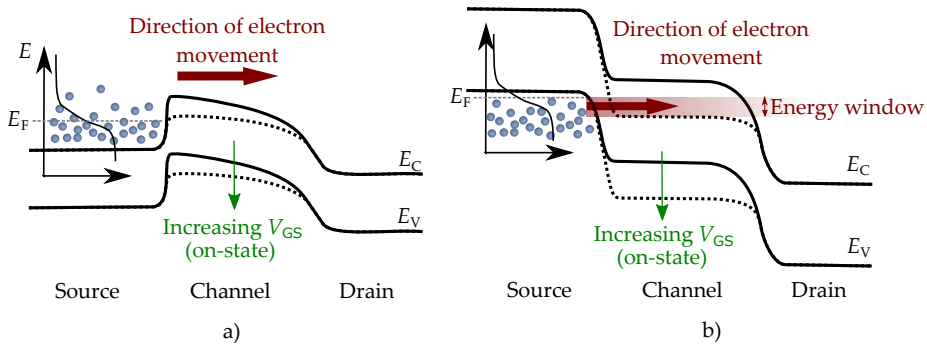


Figure 1.3: Schematic illustration of the band diagrams and working principles of a) MOSFETs and b) TFETs. Full lines correspond to the off-state and dotted lines to the on-state. In the MOSFET in a), charge carriers easily overcome the channel energy barrier in the on-state. Due to the band tails caused by the Boltzmann statistics, a few charge carriers can overcome the channel energy barrier even in the off-state. In the TFET in b), the charge carriers can tunnel when the conduction band in the channel is lower than the Fermi level in the source, but not when the energy window closes with the decreased gate voltage in the off-state.

voltage must be decreased by 60 mV to decrease the source-drain current by one magnitude. To have off-state leakage acceptably low, these 60 mV/decade sets a lower threshold voltage limit of ~200 mV, whereas overdrive voltage need to be ~300 mV. In total, an operating voltage of 500 mV is required, which sets a practical limit on MOSFET power efficiency [9].

To overcome the Boltzmann tyranny to allow for sub-500 mV operating voltage, several unconventional transistor designs exist such as tunnel field-effect transistors (TFET) [14], negative capacitance transistors, [15] and Dirac-Source transistors [16]. Even if the basic transistor functionality of a TFET is the same as for a MOSFET, the carrier transport is fundamentally different. Instead of thermionic injection over a barrier, TFETs utilize the quantum mechanical band-to-band tunneling between the valence band in the source and the conduction band in the channel. The current is still modulated by moving the bands in the channel region by applying a voltage to the gate, but due to the filtering of high-energy carriers in the Fermi-tail, the devices can obtain a subthreshold swing below the thermal limit of 60 mV/dec. Due to their reliance on tunneling, TFETs usually have lower current densities than MOSFETs. However, by using III-V heterojunctions, this may be partially avoided due to a low bandgap and low effective mass providing a small tunneling distance and tunneling mass [14]. In depth treatments of the vertical

III-V nanowire MOSFETs and TFETs developed in Lund can be found in [17] and [18], respectively.

The introduction of a material with negative capacitance [19] in the gate oxide of a MOSFET is also a suggested method to overcome the Boltzmann tyranny [15, 20]. As the commonly stated approach is to stabilize the negative capacitance of a ferroelectric material by the positive capacitance of a semiconductor, it must be noted that the sub-60 mV/decade behavior in the ferroelectric TFETs in this thesis is not thought to arise from the concept of negative capacitance, but from the previously described energy filtering in TFETs.

1.1.3 NEUROMORPHICS

To enable further development in computing system advances beyond transistor scaling, even the foundation of computer architecture, the von Neumann architecture (VNA) from 1945 that physically separates the computation and memory units, is being reconsidered. Large data sets in the VNA must be shuttled back and forth between computing and memory chips, making data-centric applications struggle with latency and power inefficiency. To solve this problem, non-von Neumann architectures are being investigated and especially neuro-inspired approaches, such as in-memory computation, have caught interest. This approach merges the computation and memory into one unit, similar to the brain, where memory and processing are deeply intertwined [21]. The complexity and use of neuro-inspired systems varies, but the most common application is as artificial intelligence (AI) accelerators, i.e., computer chips specialized for the matrix-vector-multiplications ($y = Ax$) that are extremely abundant in machine learning computation. There have been implementations of AI accelerators using different kinds of memristors such as spin-torque-transfer memories [22], phase change memories [23], and resistive random-access memories [24] proving the viability of the technology.

The memristor is a device storing information as distinct and stable conductance states caused by differences in the atomic arrangements of a material [21]. This makes them useful as highly scalable synapses in neuro-inspired systems as they provide a tunable connection strength (conductance) between the neurons as in Fig. 1.4a). In IRDS, it is predicted that ferroelectric transistors and memristors for neuro-inspired computing will be needed in the coming decade [11] in order to enable computing system advances. The ferroelectric field-effect transistors (FeFETs) and ferroelectric tunnel junctions (FTJs) investigated in this thesis are potential solutions.

As seen in Fig. 1.4b), memristors can be used as the weight elements in M × K (A) matrices and are on the chip implemented in a fully connected crossbar array, i.e., every input is connected to every output through a memristor. In

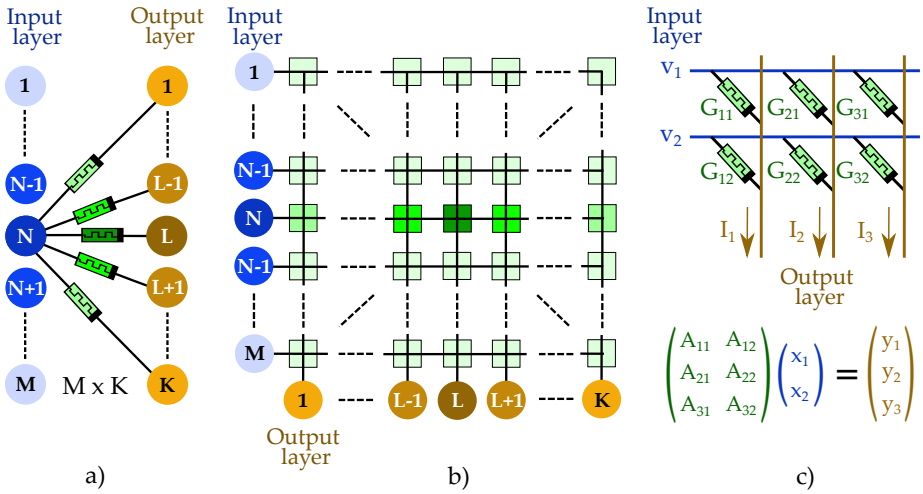


Figure 1.4: Illustration of an artificial neural network in a crossbar array. a) Each neuron is a node in one layer (blue) connected to all other nodes in the next layer (brown) via memristors (green) that correspond to the connections of biological axon-synapse-dendrites. b) This is implemented through a fully connected crossbar array which has a memristor at every cross point. c) Matrix-vector multiplication in a crossbar array.

practice, this is commonly implemented by long lines of metal strips of word and bit lines with a memristor at each cross point [25]. The conductance of the memristor multiplied by the input voltage gives the output current. If there is a linear mapping between the conductance of the memristors and the elements in the matrix A (Fig. 1.4c), the x values can be encoded into the voltage of the input layer. The currents measured at the output layer will then, due to Ohm's law and Kirchhoff's current law, be proportional to the matrix vector result y. If the input is instead duration rather than voltage, the output becomes the total charge (i.e., the time integral of the current). By applying the input at the output, the matrix multiplication is instead performed on the transpose of A. In principle this could be implemented using resistors, but the strength of using memristors is that the matrix values are reprogrammable which enables on-chip training of the neural network [26, 27].

2

Ferroelectricity

A ferroelectric material has a spontaneous electric polarization which can be switched by applying an external electric field. The property is caused by the crystal structure of the material in which a remanent polarization is created by a non-centrosymmetric lattice. A theoretical prediction of ferroelectricity was made in 1912 by Debye, drawing on an analogy to ferromagnetism, [28] which in turn made Schrödinger coin the term ferroelectricity (ferroelektrisch) the same year [29]. Hysteresis, nonlinearity, saturation, large permeability, and a Curie temperature all have a counterpart. Ferroelectricity was experimentally discovered when Prof. Swann, apparently unaware of the previous predictions, speculated that the abnormal dielectric behavior reported for Rochelle salt might be explained by some kind of electrical hysteresis. His student Valasek investigated the topic and could in 1920 indeed verify a polarization hysteresis in the material. Until the finding of ferroelectric $BaTiO_3$ during World War II, the fragility of ferroelectric materials made them mainly a theoretical interest [30]. However, with $BaTiO_3$, Devonshire [31] was able to formulate a model of ferroelectricity based on previous work on phase transitions by Landau [32] and Ginzburg [33].

2.1 A SIMPLE FERROELECTRIC MODEL

Although phenomenological, the Landau-Ginzburg-Devonshire model of dielectric and ferroelectric materials is useful for understanding ferroelectricity. As shown in Fig. 2.1a), it describes a ferroelectric as having two (dielectric) states separated by an energy barrier, i.e., a double-well potential. In the model material lead zirconate titanate ($Pb(Zr_{1-x}Ti_x)O_3$, PZT) in Fig. 2.1b),

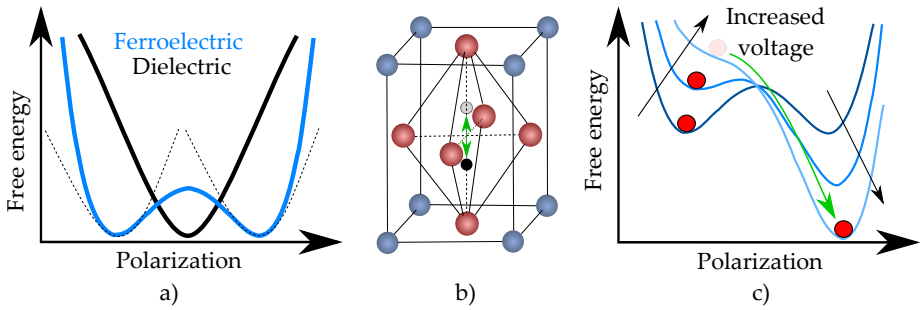


Figure 2.1: a) The free energy of a ferroelectric as a function of the electric polarization P forms a double-well landscape. b) Lead zirconate titanate ($Pb(Zr_{1-x}Ti_x)O_3$, PZT) has become a model ferroelectric material in which an ion moves between two stable off-center positions marked by the green arrow. c) When applying an electric field, the free energy landscape gets distorted and the current state might no longer be the one with lowest energy, making the state switch as indicated by the green arrow.

these states can be thought of as two thermodynamically stable atomic configurations, in between which a Ti/Zr ion can move if a strong enough electric field is applied. The movement makes the polarization dipole of the unit cell switch. As seen in Fig. 2.1c), this occurs as the electric field distorts the double well landscape and at a certain field, the energy minimum is no longer the state currently occupied and the state switches. This creates a relationship between the polarization and the applied field (voltage) that is described by a hysteresis curve as in Fig. 2.2. The measurement of the hysteresis curve will be explained in section 5.1.1. The curve can be used to retrieve the characteristic parameters of a ferroelectric material: the remanent polarization (P_R) and the coercive field (E_C). P_R represents the macroscopic polarization of the material when no electric field is applied, while E_C is the electric field where the macroscopic polarization becomes zero [34].

A volume of the ferroelectric having an identically oriented spontaneous polarization is referred to as a domain. Domains are in this simple model assumed to have a constant spontaneous polarization with an abrupt wall towards the surrounding. Due to energy minimization, ferroelectric materials are normally multidomain and this is especially true for polycrystalline thin films such as those studied in this thesis. A commonly used model for polycrystalline multidomain thin film ferroelectrics is an Ising-like one as in Fig. 2.3a). The assumptions are 1) that the polarization magnitude is intrinsically connected to the crystal structure of the material and 2) that the crystal orientation, i.e., the direction of the polarization axis, of each crystallite is statistically distributed. All crystallites are assumed to have the

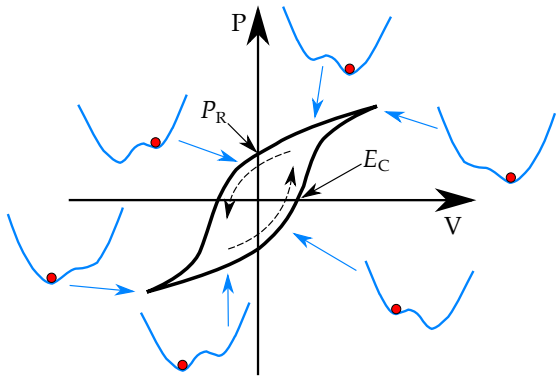


Figure 2.2: A characteristic polarization-voltage hysteresis loop for a ferroelectric material and the corresponding thermodynamic free energy landscape at the corresponding voltage.

Figure 2.3: a) In a simplified model, ferroelectric films can be regarded as similar to an Ising model but with electric dipoles instead of magnetic dipole moments. b) A crystal whose polarization axis aligns to the applied electric field (E_{Aligned}) has a considerably smaller coercive field than one with a non-aligned polarization axis (E_{Tilted}).

same coercive field, E_C in Fig. 2.3b), but only the electric field component parallel to the polarization axis contributes to the switching of the remanent polarization. This leads to a spread in the coercive field across the material and the effective polarization with which it affects its surroundings. A more in-plane switching has a higher coercive field and contributes less to the macroscopic polarization [34].

The above view of a ferroelectric as a Landau-based Ising-like model is highly useful as an idealized conceptualization of the phenomena, however, it is a simplification that rarely holds if used for actual modeling of material properties. For instance, the thermodynamic switching described by the Landau approach typically overestimates the coercive fields by orders of magnitudes, whereas inhomogeneities such as impurities, crystal defects, and charge trapping are also needed to explain switching dynamics [35]. For this

thesis, an Ising-like view is mostly sufficient and further refinements will be treated when necessary to understand the results.

2.1.1 ANTIFERROELECTRICITY

In line with the analogy of ferroelectricity and ferromagnetism, antiferroelectricity is the electrical counterpart of antiferromagnetism. Here, the electrical dipoles of the material are understood as being antiparallel when no voltage is applied, i.e., adjacent dipoles point in opposite directions making the remanent polarization cancel out to zero. Thermodynamically this can be understood as in Fig. 2.4a) where there is a single minimum when no voltage is applied, but that an energy barrier emerges at a certain voltage causing a new stable state at high electric fields as in Fig. 2.4b). This means that a sufficiently large electric field results in an alignment of the dipoles as in a ferroelectric material, however, when the voltage is removed the dipoles relax back to their antiparallel ground state again [36]. As the free energy landscape is symmetric in Fig. 2.4a), the same phenomena arise for both negative and positive voltages and when plotted in a polarization-voltage graph a double hysteresis loop arises as in Fig. 2.4c).

2.2 FERROELECTRICITY IN ELECTRONICS

Ferroelectricity has been connected to electronics ever since its discovery while trying to fabricate a new kind of seismometer during World War I [30]. The scientific research soared in the 1940s and it got recognized that a stable electrically switchable device could be used as a binary computer

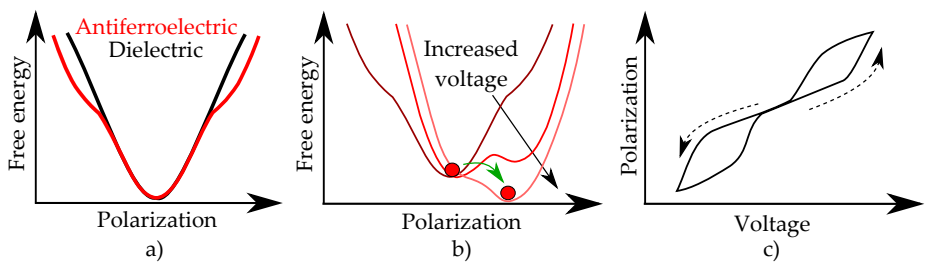


Figure 2.4: a) The free energy of an antiferroelectric material as a function of the electric polarization P forms a single stable state at $P = 0$. b) But due to the shape of the free energy two other states become lower in energy for high applied fields and the state switch as indicated by the green arrow. c) A characteristic polarization-voltage hysteresis loop for an antiferroelectric material.

memory. Already in the 1950s, the first initial ferroelectric memories were developed [37], but it was not until the 1990s that they found widespread use in memories and radio frequency (RF) devices. For instance, they were mass produced for Sony PlayStation 2 which contained a ferroelectric random-access memory (FeRAM) chip [38].

But then they slowly faded out of use as the perovskite ferroelectrics were incompatible with standard fabrication processes in semiconductor industry (i.e., CMOS-incompatible). They degrade under forming gas annealing [39], cannot be conformally deposited, and are difficult to scale due to a complicated structure [40,41]. Device downscaling is essential for the semiconductor industry, and a device technology must be scalable in order to enable implementation in future technology nodes. Other ferroelectric material classes exist, e.g., polymer-based [42], triglycine sulfates [43], moiré pattern based [44], or even ice [45,46], but as with perovskites, they have not been able to compete with more conventional memory technologies.

Instead, it has been the lately discovered HfO_2-based fluorite-type ferroelectrics that have caught industrial interest. HfO_2 is a well-established oxide material in semiconductor industry and thus fully CMOS-compatible [9]. The films are highly scalable and a 1.5 nm thick film has been shown ferroelectric by back-to-back connecting two films [47]. By more heavily relying on material characterization rather than electrical characterization, ferroelectricity has been indicated for ferroelectric HfO_2 in even thinner films [48,49]. HfO_2-based fluorite-type ferroelectrics will be treated more in depth in section 2.3.

2.2.1 MEMORY DEVICES

There are many potential applications for ferroelectricity in electronics, but as with the past, memory will probably remain the main application. Below, the three most promising technologies summarized in Fig. 2.5 are presented in their order of technological maturity. Ferroelectric random-access memory (FeRAM) has successfully been commercialized using perovskites and is one of the most energy efficient memory technologies. The ferroelectric field-effect transistor (FeFET) is a versatile complement to flash technology and may become the key component in future data-centric computer applications. The ferroelectric tunnel junctions (FTJ), as with other memristive technologies, might on top of being a binary memory also enable neuromorphic computing. Less commonly, ferroelectric RF and mm-wave technologies are discussed, but there is reason to believe that ferroelectric HfO_2 will find applications also in that field [50–52].

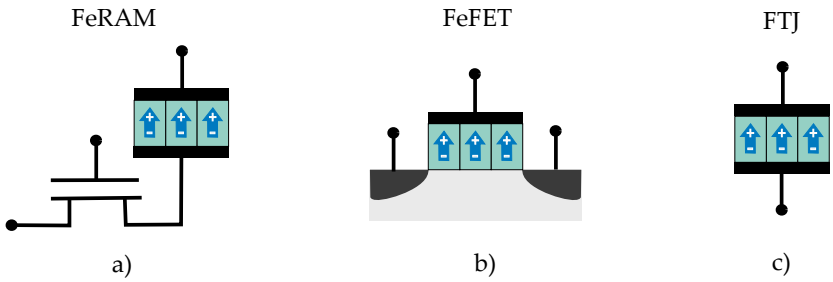


Figure 2.5: a) The 1T1C structure of a ferroelectric random-access memory, b) the 1T structure of a ferroelectric field-effect transistor, and c) the 1C structure of a ferroelectric tunnel junction.

FeRAMs

The dynamic random-access memory (DRAM) cell was developed in the mid-1960s and has become the standard technology for main memory in computers. Just like the FeRAM in Fig. 2.5a), it uses a 1T1C architecture, i.e., a capacitor as the storage element and an access transistor to control the charge stored on said capacitor. The transistor gate is activated by a voltage to read or write data to the storage capacitor and the data is sensed on the transistor source as the current response is dependent on whether the capacitor was charged or not (”1” or ”0”). The memory is cheap, fast, and durable; however, it comes with caveats such as 1) the storage capacitor must be large in order to store a measurable amount of charge and 2) the access transistor will inevitably leak current making the memory eventually lose its state. Because of reason 2), to keep the stored data, the memory must be periodically refreshed and is therefore a volatile memory solution. When powered off, its data is lost [53].

Ferroelectric random-access memory (FeRAM), based on ferroelectric perovskites, was commercialized in the early 1990s and is still used in certain niche applications where ultra-low-power non-volatile memory is critical [54]. The 1T1C technology is similar to DRAM, but the charge is non-volatile as the storage capacitor is ferroelectric rather than dielectric, see Fig. 2.5a). The data is read by activating the transistor by a gate voltage and then applying a voltage across the ferroelectric. If the ferroelectric switches (”1”), the current response will be considerably bigger than if it does not switch (”0”). Furthermore, compared to DRAM, there is the benefit that the capacitor area can be reduced as the polarization charge density in a ferroelectric is high compared to a dielectric charge density (e.g., $\sim 20 - 30\ \mu C/cm^2$ for ferroelectric HfO_2 compared to $\sim 2 - 3\ \mu C/cm^2$ for dielectric HfO_2). This enables area shrinkage and reduction in manufacturing complexity, i.e., it lowers the cost.

The major issue is currently cycling endurance, which is considerably lower than for DRAM [55], but at least for the current niche applications it is virtually unlimited [54].

FeFETs

As indicated in Fig. 2.6a), flash memories resemble standard MOSFETs, however, they have an extra floating gate which is insulated all around. Through direct tunneling or hot electron injection, electrons can be trapped at this floating gate by applying a voltage. The trapped charges change the electrostatics of the MOSFET and by screening the electric field from the regular gate electrode, the threshold voltage (V_T) of the transistor can be changed. By reading out the current at a certain gate voltage, one can readily assign the two V_T-states to ”1” and ”0”. The major issue of flash memories is the endurance and the energy consumption during the write cycle [56]. The market for non-volatile memory is currently dominated by flash memory and hard disk drives (HDD). The electro-mechanical HDDs are cheap but slow, and with the market trend being towards portable devices, flash memory is preferred due to its mechanical shock resistance [53].

The ferroelectric field-effect transistor (FeFET) effectively fills the same function as flash memory, but with several advantages. The FeFET is a device

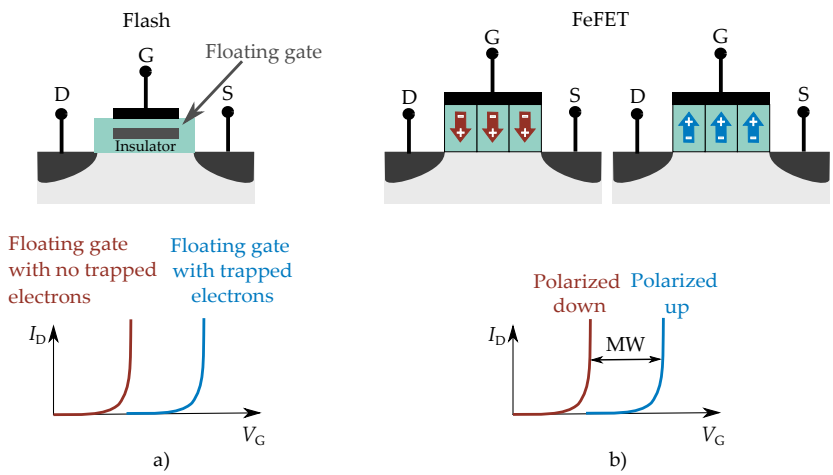


Figure 2.6: Schematic illustrations of a) a flash memory cell with a floating gate encapsulated by the oxide insulator and b) ferroelectric field-effect transistors with the ferroelectric domains polarized in opposite direction. The two technologies have similar transfer characteristics, and their threshold voltages are both changed by the application of a voltage pulse to the gate.

integrating a ferroelectric material in the gate stack of a standard MOSFET, see Fig. 2.5b). Like the floating gate of a flash memory, the ferroelectric polarization changes the electrostatics of the MOSFET and depending on the polarization state, the threshold voltage of the transistor shifts as in Fig. 2.6b). By applying a voltage bigger than the coercive voltage of the ferroelectric to the gate, the polarization state switches. The difference between the high-V_T state and the low-V_T state is commonly referred to as the memory window (MW). To a first order approximation, the memory window is twice the coercive voltage of the ferroelectric film. By only switching a portion of the ferroelectric state, intermediate threshold voltages are obtainable which makes it possible to use the device as a three-terminal memristor [57]. State-of-the-art FeFETs have an endurance ranging from 10^5–10^9 cycles, which is significantly better than flash memories while at the same time considerably more energy efficient [58].

FTJs

Memristors have found some commercialization in e.g., Intel's product Optane, however, they are in general less industrially mature than previously mentioned technologies of DRAM and flash. Commonly, three memory technologies are identified as the most promising memristor technologies: spin-torque-transfer memory, phase change memory, and resistive random-access memories (RRAMs) [21]. Ferroelectric tunnel junctions (FTJ) are an emerging alternative and, as seen in Fig. 2.7, they consist of a thin ferroelectric sandwiched between two electrodes. When applying a bias, the tunneling transmission probability through the film is strongly dependent on the ferroelectric polarization, i.e., there is an OFF/ON resistance ratio called the tunnel electroresistance (TER) that changes with the reversal of the ferroelectric polarization [59].

The polarization charges present at the surface of the ferroelectric repel or attract electrons and holes depending on the polarization state. In metal electrodes, this happens over a short distance as the electron density is high (usually a few tenths of nanometers), whereas in semiconductors, the screening length can reach tens or hundreds of nanometers. The imperfect screening creates a potential drop at the electrode/ferroelectric interface which in turn creates a band bending. By using two different electrodes, different screening lengths (d_1 and d_2 in Fig. 2.7) create an asymmetric device with an average barrier height that depends on the ferroelectric polarization. As the tunneling transmission probability is dependent on the barrier height, the resistance of the device is dependent on the ferroelectric polarization state [59, 60]. FTJs are commonly fabricated with two metal electrodes, i.e., metal-insulator-metal (MIM), as presented in this thesis. The highest TER is though usually

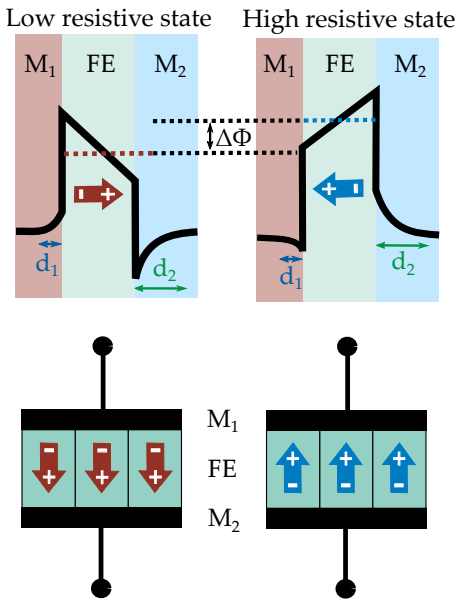


Figure 2.7: Schematic of the band diagram of an asymmetric metal-insulator-metal ferroelectric tunnel junction (FTJ). Without the ferroelectric polarization, the energy barrier would have been a square potential. Due to different screening lengths in the metals (d_1 and d_2), the electronic potential profile is altered by the polarization state. As the average energy barrier height is lower in the left state (by $\Delta\Phi$), the tunnelling current becomes bigger and the FTJ is in the low resistive state (the ON-state). In the opposite state, the average energy barrier height is higher resulting in the high-resistive state.

found when one of the electrodes is a semiconductor, which probably can be attributed to the even more asymmetric screening length in a metal-insulator-semiconductor (MIS) compared to a MIM [61].

2.2.2 HIGH-FREQUENCY ELECTRONICS

Microwave communication systems are expected to be increasingly more flexible and adaptable, requiring reconfigurability [62]. This means that ferroelectric devices might make a comeback due to the ferroelectric HfO_2 as it in contrast to perovskites is CMOS-compatible and scalable. The high-frequency applications of HfO_2-based ferroelectrics are barely treated in literature even if it has been an active field of research for ferroelectric perovskites for decades. The benefit of ferroelectrics is that they provide a frequency independent tunable permittivity (capacitance) which can be

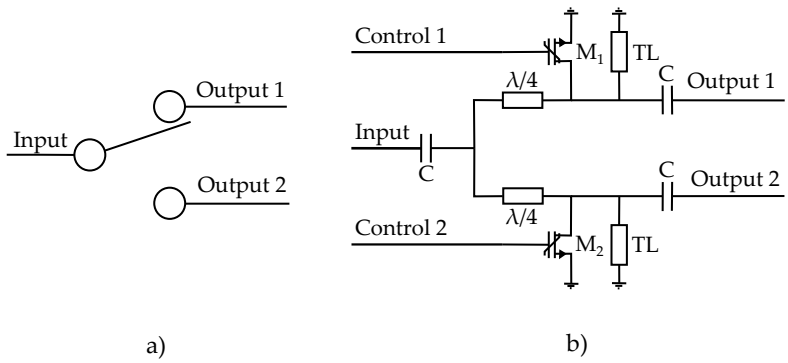


Figure 2.8: a) The symbol of an SPDT (single pole, double throw) switch, i.e., a break-before-make switch in which the input is either connected to output 1 or 2. b) A schematic circuit for a FeFET SPDT. The transistors M are FeFETs with control lines connected so that the remanent polarization can be switched. By utilizing both a NMOS FeFET and a PMOS FeFET, a single control input can be used but that would also remove the possibility of implementing simultaneous transmission through both or none of the outputs. Capacitors are added to block DC signals from both the input and outputs. When a FeFET is in the on-state, the corresponding output will be shorted to ground, while in the off-state the signal is transmitted. The $\lambda/4$-lines transforms a short to a high impedance which reflects the input power making the output low. The transmission lines TL are inductive stubs designed to resonate the parasitic capacitances of the FeFETs, thus minimizing losses at the output.

applied in varactors for implementations in amplifiers, filters, phase shifters, and voltage-controlled oscillators.

For mm-wave applications, ferroelectric HfO_2 has a clear disadvantage compared to perovskite ferroelectrics due to its high Curie temperature of several hundred degrees Celsius [63]. Although seldom mentioned, there is a general assumption that polar ferroelectrics should not be used for high-frequency devices. This is due to their piezoelectricity, which creates big microwave losses at <10 GHz, and their domain wall movements that contribute to further losses. The hysteresis associated with the polar phases makes them less desirable as it sets further design restrictions. Therefore, the proposed applications in HfO_2-based applications have mainly focused on using the capacitance tunability of the ferroelectric response in the sub-coercive voltage region, where domain switching can be neglected [64]. This allows for a capacitance tunability of a couple of tens of percent that with simulated filters have shown promising results. However, at a high enough frequency it is expected that domain walls and piezoelectricity stop responding to the small signal and will therefore not contribute to losses, e.g., at frequencies up to 50

GHz in a ferroelectric perovskite [65]. The same is expected to remain true for HfO_2-based ferroelectrics, however, it is yet to be investigated. Metal-insulator-metal capacitors of ferroelectric HfO_2 have been investigated up to mm-wave frequencies (30-300 GHz) by Abdulazhanov et al. [66], but the films show a high permittivity and loss tangent which is assumed to be caused by the deembeddning procedure. Nevertheless, the results indicate the applicability of the technology and are in line with the metal-insulator-semiconductor results in paper IV in this thesis.

Combining ferroelectrics with semiconductors might create even further flexibility and functionality. Contrary to the historical usage of ferroelectricity as tunable capacitors (varactors), the integration of ferroelectricity on III-V materials in this thesis is mainly to add reconfigurability to the III-V technology platform. For instance, among transistor-based RF-switches, III-V semiconductor devices have achieved the highest operation frequency [67]. In its simplest form, an RF-switch fills the same purpose as a regular light switch (a SPST, Single pole single throw), i.e., either the two terminals are connected or they are not. The simplest possible SPST FeFET RF-switch is to configure the polarization so that the transistor is in either the off-state or the on-state, i.e., either blocking or transmitting the signal. Commonly, RF-switches are used for routing signals on a chip for which the SPDT (Single pole double throw) switch, Fig. 2.8a), can choose whether the input signal passes to output 1 or 2. RF-compatible FeFETs would in these circuits fulfill the same purpose as the currently used MOSFETs, but doing it in a non-volatile reconfigurable fashion which does not need a continuous control signal. For the circuit in 2.8b), only short polarization switching voltage pulses are required to set whether the signal is transmitted through both outputs, routed up, down or not transmitted at all.

From a security perspective, this is useful for hardware obfuscation in which one intentionally can conceal the functionality of the circuitry as it will behave differently depending on the state of each ferroelectric element. Without the correct key, normal functionality is not enabled and can, depending on the complexity of the circuitry, be very difficult to reverse-engineer even if having the blueprint or a physical example of an unlocked device. This concept has in Paper X been implemented in a ferroelectric TFET which has different functionality depending on the ferroelectric state and in Paper IV, in which the reconfigurable varactor has different capacitance depending on the ferroelectric state. By intentionally designing the circuit using a ferroelectric with a short retention time, it is even possible to fabricate a circuit whose functionality is lost a short time after the key is used. This would enable usage of a functioning device without the risk of a competitor reverse-engineering even an unlocked device as it effectively becomes ”self-destructive”.

2.3 FERROELECTRICITY IN HAFNIUM OXIDE

Ferroelectricity in HfO_2 was discovered by Tim Böscke at Qimonda in 2006 when trying to replicate an earlier study by Toriumi's group showing a permittivity maximum for annealed films when doped by 4-5 atomic percent Si [68]. Through extensive electrical and structural analysis, Böscke et al. [69] were able to show that the permittivity enhancement was not due to the assumed increase of tetragonal crystal phase ($P4_2/nmc$) but due to a ferroelectric orthorhombic phase ($Pca2_1$). As industrial research at a memory company, the work focused on scaled ferroelectric field-effect transistors (FeFET) and ferroelectric random-access memory (FeRAM). Finally, in 2011, several important papers were published with material analysis of ferroelectric HfO_2 [69–72] and importantly a 65-nm technology node Si FeFET [69]. This was followed up in 2012 by a 28-nm Si FeFET [73] together with the first report of Zr-doped ferroelectric HfO_2 (HZO) [74], which has by time become the de facto standard material choice.

The following section will treat the material properties of ferroelectric HfO_2 as it in some regards differs from the conventional perovskites. In this thesis, unless otherwise specified, any reference to ferroelectric HfO_2 will from this point on assume Zr-doping ($Hf_xZr_{1-x}O_2$, HZO). The fabrication and deposition methods for ferroelectric HfO_2 will be treated in chapter 3, while the electrical properties of ferroelectric HfO_2 will be treated together with the measurement methods in chapter 5.

2.3.1 MATERIAL CHARACTERISTICS OF FERROELECTRIC HAFNIUM OXIDE

The intuitive model for ferroelectricity introduced in section 2.1, in which an off-center ion in a non-centrosymmetric sublattice is moving between two stable states is true for many perovskite ferroelectrics but has been proven too simplistic for ferroelectric HfO_2. The ferroelectricity in HfO_2 is rather described as arising from a fluorite structured crystal lattice (crystallographically similar to calcium fluorite) in which the remanent polarization is caused by an off-centering of half of the eight oxygen ions in the unit cell [75]. The unconventional polarization mechanism with a strong atomic bonding compared to perovskites creates robust properties that in most cases are beneficial for implementation in electronic devices. Most importantly, it gives rise to a coercive field that is ten times higher than in conventional perovskites, which enables relatively big coercive voltages and memory windows even at scaled thicknesses [76].

Bulk crystalline HfO_2 and ZrO_2 have been shown to exist in several polymorphs: monoclinic (space group: $P2_1/c$), tetragonal (space group: $P4_2/nmc$), and cubic (space group: $Fm\bar{3}m$). All these crystal phases are centrosymmetric

and thus not ferroelectric. However, for thin polycrystalline films, the surface energy becomes comparable to the volume energy and other phases can occur. Several forms of orthorhombic phases have been reported: antipolar orthorhombic-I (space group: Pbca), orthorhombic-II (space group: Pnma), and nonpolar orthorhombic-V (space group: Pbca). The two orthorhombic phases oIII (space group: $Pca2_1$) and oIV (space group: $Pmn2_1$, never observed experimentally) are ferroelectric. Also the polar rhombohedral phase (space group: R3m) has been reported ferroelectric [77]. Following what is conventional in the research field, this thesis will refer to the phases as monoclinic (m), tetragonal (t), cubic (c), and orthorhombic (o) where the last one is assumed to be the ferroelectric oIII-phase.

Thus, to obtain ferroelectric HfO_2, the fabrication process should be aimed at obtaining a large proportion of o-phase in the film. The main issue is that most deposition methods give an amorphous film and the o-phase is not the thermodynamically stable state unless precautions are taken. This includes engineering the deposition conditions (e.g., the dopant and oxygen vacancy concentrations), the crystallization annealing process, the mechanical stress from electrodes, and the thickness of the film.

Annealing

The as-deposited state of doped HfO_2 films grown by atomic layer deposition (ALD), see section 3.1 for further details, is generally amorphous and an anneal is required to crystallize it into the ferroelectric o-phase. During the annealing, it is assumed that the crystallization follows Ostwald's rule, i.e., the less stable polymorphs crystallize first [78]. As schematically shown in Fig. 2.9, the crystallization process is commonly described as starting with the formation of small, mainly t-phase, nuclei but with the existence of other phases as well. The t-phase has both the lowest surface and interface energy and will therefore be the most abundant. These 'precursor' nuclei grow and, importantly, the t-phase may, due to a decreased bulk free energy, change phase to the ferroelectric o-phase at a certain grain size. All phases may by further growth eventually change into m-phase as it is the most stable polymorph in bulk. These t-to-o, t-to-m, and o-to-m transitions are nucleation-limited, and the critical nuclei size is for a given film the most important factor governing the phase transformations. As will be treated below, the critical nuclei size and the energy barriers between the phases are dependent on several factors such as dopants, oxygen vacancy concentration, peak temperature, the cooling rate, strain, etc. By balancing these factors correctly, it is possible that the ferroelectric o-phase remains after the cooling when the crystallites transition to more stable polymorphs at room temperature. For thin films, due to interface energy differences and strain, the energy barrier of

the t-to-o transition is often found to be lower than t-to-m and considerably lower than the o-to-m transition [77].

As can be expected from any thermally excited process, the amount of polarization is dependent on both temperature and time at that temperature. A lower crystallization temperature can be achieved if annealing for a longer time, e.g., a 300°C thermal budget has been achieved using a two hour anneal [79]. However, the crystallization process is fast and also via nanosecond laser annealing, ferroelectric films have been obtained [80]. For the formation of ferroelectricity it has also been shown that quick cooling (quenching) is beneficial for o-phase formation [81].

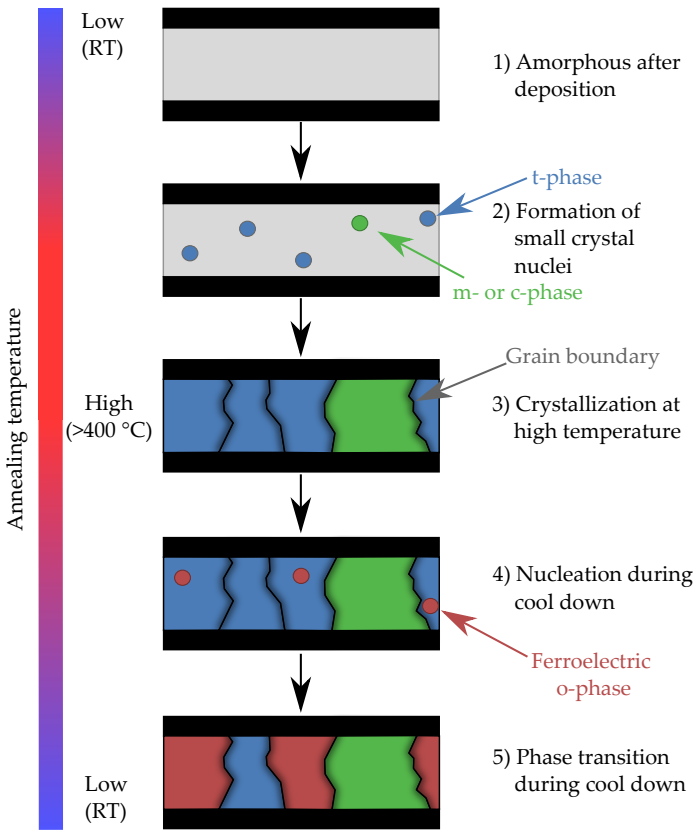


Figure 2.9: Schematic of the formation of ferroelectric o-phase in an amorphous HfO_2 film during a rapid thermal annealing.

Doping

Although dopant-free ferroelectricity has been achieved, doping HfO_2 films is generally regarded as the key method of tuning the ferroelectricity as the free energy difference between the o- and t-phase relative to the m-phase decreases [82]. The main function of the dopant is to stabilize the t-phase at the annealing temperature so that it can transition into the o-phase during cooling [77]. Many dopants have been proven to successfully induce ferroelectricity, but over time Zr-doped HfO_2 (HZO) has become the standard doping thanks to the wide dopant concentration window that it possesses. A concentration window is existent for all dopants and means that there is a doping level at which a maximum remanent polarization is obtained and that a smaller or bigger dopant concentration leads to a decreased remanent polarization or an antiferroelectric-like behavior [34, 74, 82]. Furthermore, Zr-doped films require a comparably low annealing temperature to obtain ferroelectricity which is beneficial for integration on thermally sensitive III-V materials [83].

Stress

Long before the idea of ferroelectric HfO_2, it was reported that orthorhombic ZrO_2 can be stabilized by tensile stress or hydrostatic pressure and due to the similarity of the materials it was early on expected that the same would occur for HfO_2 [84, 85]. The choice of electrodes has been shown to mechanically confine the film and, depending on the stress transferred from the electrode to the HfO_2, it affects the ferroelectricity of the sample. E.g., the increase in remanent polarization with increasing electrode thickness in a TiN/HZO/TiN MIMCAP was interpreted to be caused by an increased tensile strain in the film [86]. It has further been shown that higher tensile strain results in higher remanent polarization [87]. It has even been suggested that the strain arising from the piezoelectric effect of an applied bias can induce t-to-o phase change in films with antiferroelectric-like behavior [77].

Oxygen Vacancies

In perovskite ferroelectrics, oxygen vacancies are considered almost purely negative as they increase the leakage current and pin the domains [88]. For ferroelectric HfO_2, it is a bit more intricate as the same leakage current and domain pinning issue exists, however, seemingly, a slightly oxygen-deficient film is beneficial for inducing ferroelectricity [89]. In dopant-free ferroelectric HfO_2, it is seemingly even the case that oxygen vacancy concentration is of utmost importance for the ferroelectricity [90]. The reactivity of the interface layers and electrode materials can therefore be an important factor for induc-

ing ferroelectric properties [91]. But oxygen vacancies are inherently causing reliability issues in non-ferroelectric devices [92] and the situation becomes even worse with ferroelectric devices. From a reliability perspective, oxygen vacancies must be minimized even if they help induce o-phase. Oxygen vacancies are diffusive and their redistribution in the ferroelectric HfO_2 affects the switching dynamics in ferroelectric applications, such as the switching kinetics, wake-up, and imprint [89].

Thickness

The scaling limits for ferroelectric materials are important for applications. From a thickness point of view, HfO_2-based ferroelectrics have proven interesting due to their big coercive field that is ten times higher than conventional perovskites [76]. Generally, higher annealing temperatures are seemingly needed for thinner films, and it becomes increasingly more difficult to achieve around 5 nm thickness, which corresponds fairly well with the critical nuclei diameter for the t-phase transition at roughly 4 nm for HZO. Ferroelectricity has been electrically measured down to 1.5 nm by back-to-back connecting two films [47]. Impressive results from Cheema et al. [48, 49] indicate ferroelectricity for even thinner films, however, the results are somewhat ambiguous in the obtained crystal structure. The GHz capacitance–voltage measurements and in-plane polarization measurements were used to prove field-induced switching, however, oxygen vacancy movements or other ion movements in the films might give rise to similar phenomena [93] thus making further verification of ferroelectric properties needed. For ultra-thin films, it becomes increasingly more difficult to measure the ferroelectricity electrically as the leakage current becomes higher than the switching current. Different structural characterization techniques can be used such as synchrotron X-ray diffraction, but in the end electric field-induced switching is usually necessary to show technical applicability.

3

Fabrication of Ferroelectric Devices

In this chapter, the fabrication methods used to integrate ferroelectric HfO_2 onto III-V materials will be treated. The chapter intends to give an overview of the devices presented in this thesis, but will only treat those steps directly related to ferroelectric integration on III-V materials in greater depth. The structural and electrical characterization of said integrations will be described in chapter 4 and 5, respectively. The chapter starts with standard implementations of metal-insulator-metal capacitors (MIMCAPs) fabricated by metal sputtering and atomic layer deposition. Then III-V metal-oxide-semiconductor capacitors (MOSCAPs) are introduced and the corresponding structures used for in-operando synchrotron measurements are presented. Then, the fabrication schemes for vertical nanowire FeFETs are treated, both for conventional FeFETs and the implications for III-V ferroelectric TFETs. Finally, both planar and nanowire-based implementations for mm-wave applications are treated.

3.1 ATOMIC LAYER DEPOSITION

There are several techniques for depositing ferroelectric HfO_2, e.g., sputtering, pulsed laser deposition (PLD), and chemical solution deposition (CSD), however, atomic layer deposition (ALD) is the most used method for depositing ferroelectric HfO_2 thin films. Any deposition technique has its strengths and weaknesses, but the key advantage of ALD is the monolayer control with conformal deposition. This means that the film thickness can be controlled on the Ångström level, and the film becomes equally thick no matter the orientation or shape of the surface [94]. This, and that ALD is widely used

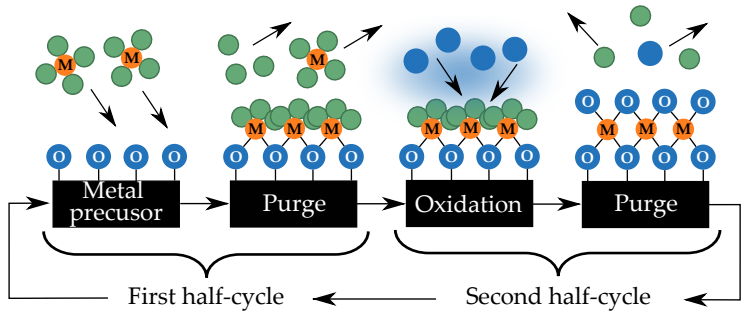


Figure 3.1: Schematic illustration of the two half-cycles making up an ALD cycle. 1) The starting surface is exposed to the metal precursors, 2) the reactor is purged of all precursors not attached to the surface, 3) the oxidizer is introduced and reacts to create the monolayer, 4) the reactor is again purged, and the process can be repeated.

in the semiconductor industry, makes it the ideal technique for the nanowire structures used in this work.

As described in Fig. 3.1, the basic principle of ALD is the usage of two self-limiting processes. The first is the introduction of a metal precursor that is pulsed into a reaction chamber, and which absorbs onto all surfaces until a monolayer is created. Secondly, an oxidizer, in this work water or oxygen plasma, is introduced into the chamber which reacts with the metal precursor and forms a monolayer of metal oxide. In between the two self-limited processes, the chamber is purged in order to remove excess precursors in the first half-cycle and to remove reaction by-products in the second half-cycle [95]. In the ideal case, one monolayer of the desired material is grown in each cycle and complex material stacks can be deposited as is indicated in Fig. 3.2.

Although the basic working principle is fairly straightforward, a considerable effort of this work has been to optimize different ALD processes in different ALD chambers. Many parameters influence the resulting quality of the films, of which the choice of precursor, oxidizer, deposition temperature, film stoichiometry, thickness, pulse, and purge times have considerable influence [94]. The difficulty with optimization increases even further as the quality of the electrodes and the annealing of the ferroelectric film changes the properties of the films. The optimization leads to trade-offs and optimizing for one property often results in degradation of another property.

In this work, early attempts of making ferroelectric films were made in a Fiji ALD using oxygen plasma as the oxygen agent, whereas aluminum (Al_2O_3 interlayers) and oxygen vacancies (varying the oxygen plasma time) were used

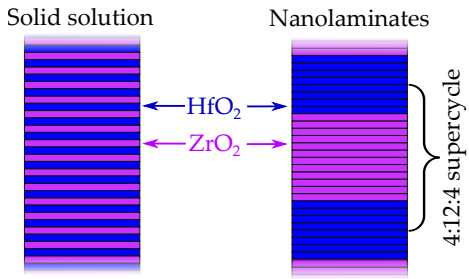


Figure 3.2: Schematic illustration of the two primary atomic layer deposited material stacks during this thesis. The conventional solid solution in which each monolayer is different and the nanolaminate structure in which several monolayers of the same material is deposited after each other.

as the dopant. Successful ferroelectric MIMCAPs were fabricated using both dopants, however, these films require a high annealing temperature (>600°C) which affects thermally sensitive III-V materials. Furthermore, plasma may oxidize the underlying semiconductor [96]. Contrary to silicon technology, for which SiO_2 is a good interlayer, III-V oxides are generally regarded as detrimental to device performance [97]. Therefore, the deposition was changed to a thermal ALD system from Picosun in which Zr-doped HfO_2 could be deposited using water as the oxidizer.

As indicated in Fig. 3.2, the films deposited during this work can be classified as either the conventional solid solution (alternating between Hf- and Zr-precursor each ALD cycle) or nanolaminates in which several monolayers using the same precursor are deposited before changing to the other precursor. Normally, the deposition temperature of an ALD is held so low that the film becomes amorphous, but by increasing the chamber temperature, it crystallizes during the deposition. As ZrO_2 films crystallize at ~300°C, this was used in paper VI to crystallize Zr-doped HfO_2 (HZO) into the ferroelectric o-phase during the ALD.

3.2 THERMAL PROCESSING

As described in section 2.3.1, one of the critical steps to obtain ferroelectricity in HfO_2 is annealing, i.e., heating the film to an elevated temperature. The issue that arises is that III-V semiconductors are thermally sensitive to the annealing temperatures required to obtain ferroelectricity [83]. The interface between the III-V material and the high-κ is sensitive to elevated temperatures and deteriorates at temperatures commonly used for ferroelectric HfO_2 [98], seemingly due to diffusion of the semiconductor elements into HfO_2 [99]

and oxidization of the interface [100]. Due to this, a considerable effort has been spent on investigating and improving the III-V ferroelectric interface through measurements on MOSCAPs. For the III-V nanowire MOSFETs, it has furthermore been observed that especially the top contacts deteriorate at elevated temperatures, which is well-known from annealing studies in literature [101, 102]. Top contact deterioration due to thermal processing has been a recurring issue during the course of this thesis, and even if working contacts were achieved in paper I, IX, and X, this has required an ongoing effort throughout. However, on large planar contacts, annealing schemes of up to 800°C can be found for W-contacts on InGaAs [103] which indicates that well-functioning solutions may exist.

In this thesis, three methods for annealing have been investigated: rapid thermal annealing, furnace annealing, and flash lamp annealing. Rapid thermal processing (RTP) involves heating the sample several hundred degrees Celsius on the second time scale (normally 1-60 seconds for ferroelectric HfO_2), [94] which in this thesis is achieved by high powered infrared lamps. Commonly, furnace annealing is made in purpose built tools that allow for annealing at elevated temperatures for extended time, however, in the field of ferroelectrics, any annealing scheme running for longer than conventional RTP time scales is referred to as ”furnace annealing” even if they in practice were annealed in a RTP tool. Finally, flash lamp annealing (FLA) is an annealing method in which surfaces are heated on the millisecond time regime by the usage of highly energetic flashes of a lamp. In this thesis, this has primarily been used as a tool to reduce diffusion processes occurring at the interface between the semiconductor and the ferroelectric HfO_2.

3.3 PLANAR STRUCTURES

The quickest solution for characterization of ferroelectric properties is through capacitors. Electrical measurements of these, see section 5.1, provide a systematic and reliable method for quickly assessing the remanent polarization, coercive fields, leakage, endurance, and retention of a particular film. The quick and inexpensive fabrication process enables a rapid procedure to predict the behavior of the films when integrated on more advanced devices. The fabrication process of FeFETs and RF devices is time-consuming and expensive. In practice, it is only attempted after initial testing on capacitor structures.

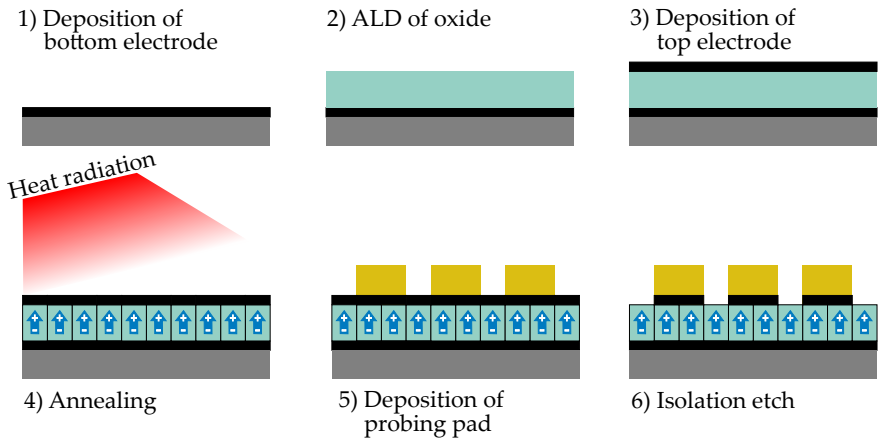


Figure 3.3: Schematic illustration of the conventional fabrication process of metal-insulator-metal ferroelectric capacitors. Commonly TiN/HZO/TiN has been used in this thesis. See appendix A.1 for a detailed process flow.

3.3.1 MIMCAP

Metal-insulator-metal capacitors (MIMCAPs) are the simplest of all investigated structures regarding both processing and data interpretation. Due to a general lack of literature on integration of ferroelectric films on III-V platforms, they enable an important benchmark to compare the films performance to the literature.

The exact process is dependent on the material choices and what to investigate, but the baseline process is outlined in Fig. 3.3 and a detailed process flow is presented in appendix A.1. 1) A bottom electrode is deposited by sputtering or ALD onto a highly-doped Si-wafer, 2) followed by the ALD of a doped HfO_2 film. 3) A top electrode is once again deposited by sputtering or ALD and 4) the structure is annealed in a RTP. 5) Electrodes suitable for electrical probing in a probe station are deposited by an evaporation lift-off (commonly 5 nm Ti and 200 nm Au). 6) Finally, the top electrode metal between the Ti–Au electrodes are wet etched to make individual capacitors.

Ferroelectric Tunnel Junctions

Ferroelectric tunnel junctions (FTJs) have a structure similar to the MIMs in Fig. 3.3 with TiN bottom electrode sputtered onto a silicon wafer followed by a thin (<5 nm) $Hf_xZr_{1-x}O_2$ film. However, the top electrode fabrication is different as the quality of the HZO top electrode interface is of outmost importance as it determines the screening length of the polarization charge. Therefore, the

annealing is performed using a sacrificial crystallization electrode of 50 nm W, which is removed by a heated H_2O_2 wet etch followed by a heated NH_4OH wet etch to remove the WO_x interfacial layer. Finally, a new replacement top electrode with the desired properties for FTJ behavior is deposited. Devices fabricated without the removal of the WO_x interfacial layer show little to no tunnel electroresistance (TER), and an electrical behavior almost independent on the choice of top electrode.

Attempts were made with MOS-based FTJs on our III-V platform, but as no encouraging results were achieved, the effort has been on MIM-based devices. The absence of TER using InAs as a bottom electrode has been attributed to the comparably poor interface compared to state-of-the-art MOS-implementations with oxide electrodes [61].

3.3.2 MOSCAP

MIMCAPs are great for rapid testing, but since the main aim of this work has been to integrate ferroelectric HfO_2 onto III-V materials, the bottom electrode must be exchanged for a semiconductor. In practice that is done by not depositing the bottom electrode in Fig. 3.3 and instead starting at step 2) with some prior surface treatment. Even if two films behave similarly in a MIM, the difference in processing may affect the semiconductor interface considerably. For any device implementation, the semiconductor-oxide interface has a key role and should be evaluated before expensive transistor or RF implementation. MOS capacitors fill a similar purpose as MIMs regarding a systematic and reliable method for quickly assessing the most important properties (remanent polarization, coercive fields, leakage, and endurance) without time-consuming device fabrication. As is presented in chapter 5, several methods have during the course of this thesis been developed to also measure the quality of the interface, and the interaction of the ferroelectric with the semiconductor.

Structures for Synchrotron Measurements

As will be outlined in section 4.3.2, XPS measurements are useful for understanding and optimizing interface properties of high-κ integrations on semiconductors [104, 105]. However, the method has a measurement depth of only a few nanometers [106] and as the MOS stack of a ferroelectric film with a realistic top electrode is considerably thicker than that, this creates issues when trying to conduct studies. The common solution is to fabricate very thin layers of ferroelectric HfO_2 without a top electrode (either etched away after annealing or never deposited on that part of the sample) or to only investigate the interface between the top electrode and the ferroelectric.

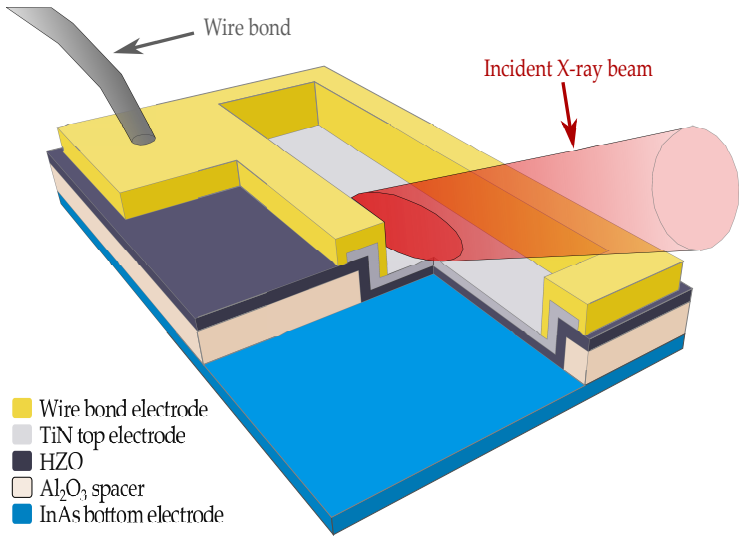


Figure 3.4: A not to scale schematic of the devices used for in-operando synchrotron measurements. The lower left part is a cross section of the structure above the substrate in order to visualize the placement of layers. Note that dimensions are not to scale. The top electrode is electrically connected through wire bonding while the bottom electrode is connected through the substrate.

To enable measurements of the entire MOS-stack, hard X-ray photoelectron spectroscopy (HAXPES) can be used as the higher photon energy compared to XPS enables measurement depths of more than 10 nm [107]. Using this, the structure in Fig. 3.4 was developed, which enables operando HAXPES measurements of a realistic III-V/ferroelectric/top metal structure, i.e., the same capacitor can simultaneously be electrically biased and measured by HAXPES. It has a measurement window of InAs/HZO/TiN which is big enough for the 20 µm × 135 µm beam footprint at the I09 beamline at the Diamond Light Source, United Kingdom. The Au pad surrounding the measurement window enables electric connection to the TiN top electrode by wire bonding.

The first step in the fabrication is to define the active capacitor structure. Using a maskless aligner (MLA) and 1:30 buffered oxide etching (BOE), a hole corresponding to the active device is defined in an 80 nm thick Al_2O_3 layer deposited by atomic layer deposition on an undoped InAs substrate (~2×10^{16} cm^{-3}). The Al_2O_3-spacer is added to 1) decrease the size of the active capacitor area (i.e., the InAs/HZO/TiN structure) as smaller area makes for a higher device yield and higher endurance [108] and 2) to create a hard to

punch through area for later wire bonding. The resulting InAs surface is cleaned by repeated digital etching using ozone and HCl:IPA 1:10. 9 nm of HZO is deposited at 200°C using thermal ALD with a 1:1 alternation between the precursors TDMAHf and TEMAZr with water acting as the oxygen source. A 10 nm TiN top electrode was sputter deposited followed by RTP annealing at 500°C. To define the TiN top electrode, a 25 nm sacrificial Al_2O_3 layer was deposited at 200°C by thermal ALD and patterned using MLA an. The resist was removed by acetone followed by a $NaOH_4/H_2O_2/H_2O$ (1:2:5) TiN wet etch for 30 s at 60°C. The Al_2O_3 on top of the electrode was removed by BOE, which is highly etch selective to the crystallized HZO. Finally, wire bonding pads were defined by MLA followed by an evaporation lift-off using Ti/Au (5/200 nm), leaving the Au-free measurement window on each device.

3.4 VERTICAL TRANSISTOR INTEGRATION

Semiconductor nanowires are fabricated either top-down (etched out) or bottom-up (grown from seed-particles). Throughout this thesis, a bottom-up approach has been used in order to grow the nanowires from gold dots defined by electron beam lithography (EBL). The growth is done by Vapor-Liquid-Solid (VLS) using metalorganic vapor phase epitaxy (MOVPE) using group III-precursors (TMGa, TMIn) and group V-precursors (TMSb, AsH_3). To dope the semiconductor, TESn is used for n-doping and DEZn for p-doping. Through many years of research, Lund has obtained extensive knowledge on nanowire growth and much of the success of this thesis can be attributed to high material quality [109, 110]. Due to a low thermal budget in the existing process modules for the III-V nanowire MOSFET platform available in Lund, many parts of the process schemes had to be changed in order to enable the integration of ferroelectric HfO_2. In practice, this meant reverting to simpler process schemes and developing new process modules with higher thermal budget.

3.4.1 VERTICAL FERROELECTRIC FET

A schematic of the process flow for the FeFET in paper I is shown in Fig. 3.5 and a more detailed process flow than the following is found in appendix A.2. Using MOVPE, a n^{++}-InAs buffer layer is grown on a Si substrate. Gold seed particles are patterned using EBL and are used to grow vertical nanowires by VLS growth in MOVPE. The bottom 200 nm form a non-intentionally doped (nid) InAs channel and followed by a 300-nm-long n^{++}-drain InAs segment at the top. During the growth of the highly doped top segment, an approximately 3-nm-thick highly doped shell overgrows the channel region. The sample does at this point look as in Fig. 3.5a).

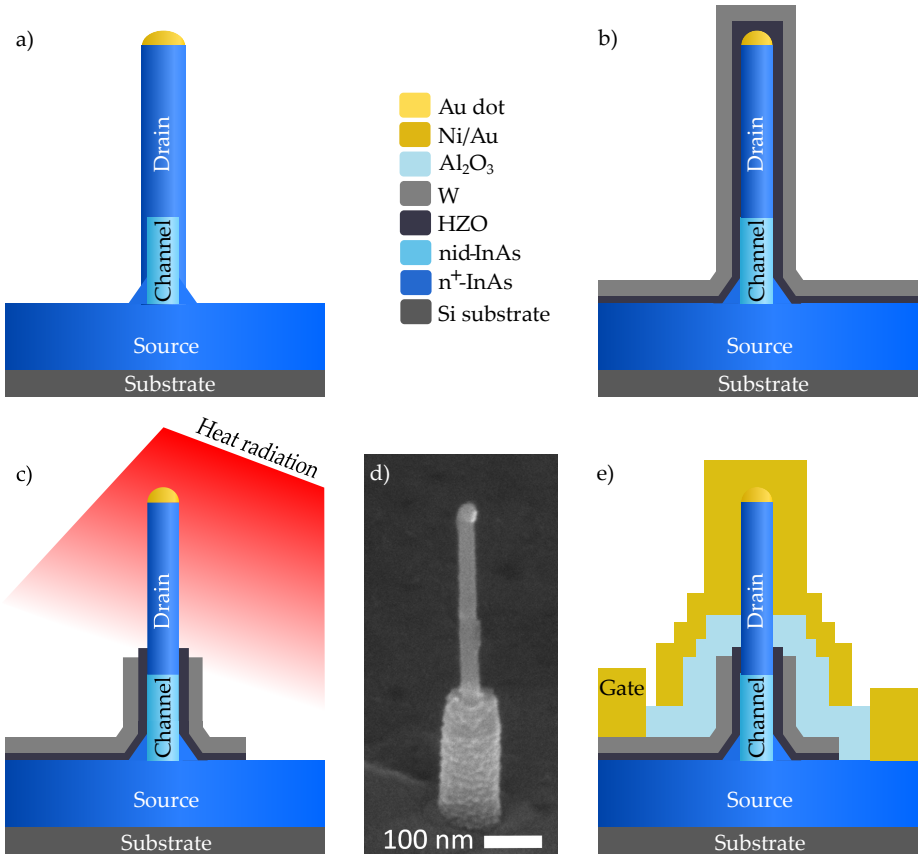


Figure 3.5: Schematic of the process flow to fabricate the III-V nanowire FeFETs. a) The nanowire after growth in metalorganic vapor phase epitaxy, b) after the ferroelectric gate oxide and gate electrode deposition, c) after the rapid thermal annealing step, d) SEM micrograph at same step, and e) the final structure.

The first step in the process is to thin the nanowire by cyclic ozone oxidation and HCl etching in order to remove the highly doped shell at the channel region. After the desired channel thickness is achieved, the HZO film is deposited at 200°C using a thermal ALD reactor with a 1:1 alternation between the precursors TDMAHf and TEMAZr using water as the oxygen source. A 50 nm W gate metal is DC sputtered making the sample look as in Fig. 3.5b). In order to define the transistor gate pad, the W is patterned using UV-lithography and reactive ion etch (RIE). The gate length is defined by spin-coating the sample with resist, which is thinned by O-plasma to a desired

thickness, i.e., the gate length. The W is once again etched by RIE. Vias through the HZO (to the source and drain) are etched by BOE using a S1813 mask patterned by UV-lithography. As seen in Fig. 3.5c), the sample is at this stage annealed in N_2 atmosphere by RTP to crystallize the HZO into the ferroelectric orthorhombic phase. A SEM micrograph of the structure after the annealing step is seen in Fig. 3.5d). 30 nm of ALD grown Al_2O_3 is subsequently deposited as a top spacer and vias to the three transistor terminals are once again patterned by resist masks and BOE. The device is finally contacted by sputtering 10 nm Ni and 200 nm Au patterned using resist and wet etch by Au and Ni etchants.

Vertical Ferroelectric TFET

The integration of ferroelectric HfO_2 onto nanowires for TFETs (in papers IX and X) followed the procedure described in section 3.4.1 and appendix A with some slight modifications. To enable the band-to-band tunneling described in section 1.1.2, a staggered nanowire heterostructure of InAs/(In)GaAsSb/GaSb as in Fig. 1.2 was grown. The III-V oxide etchant was exchanged from HCl to citric acid, as it selectively etches InAs oxide but not the GaSb at the top of the nanowire [111].

A Future Outlook

In MOSFET fabrication, there is an important distinction between gate stack deposition before and after the formation of the source/drain contacts. Since the bottom of the nanowire is connected to the InAs-substrate in all presented fabrications schemes in this thesis, a process flow starting with the definition of the top electrode would be referred to as a gate-last process whereas any other process is referred to as a gate-first process. Gate-last devices have substantial benefits in enabling a thicker wire at the top contact for lower contact resistance and also a smaller ungated region between the drain and gate which decreases the access resistance. Due to issues with deteriorated top contacts after the annealing step, no FeFET was successfully implemented using a gate-last process during the work described by this thesis. As described in section 3.2, annealing temperatures compatible with ferroelectric HfO_2 has been successfully implemented on bulk InGaAs and the effort of finding a suitable top metal for gate-last processing on nanowires should be continued.

A conceivable gate-last III-V nanowire FeFET could look as in Fig. 3.6a). Due to the high thermal budget of ferroelectric HfO_2, all spacers should preferably be oxide-based. Hydrogen silsesquioxane (HSQ), which transforms into a low-κ Si rich oxide (SiO_x) upon electron exposure, has been used in

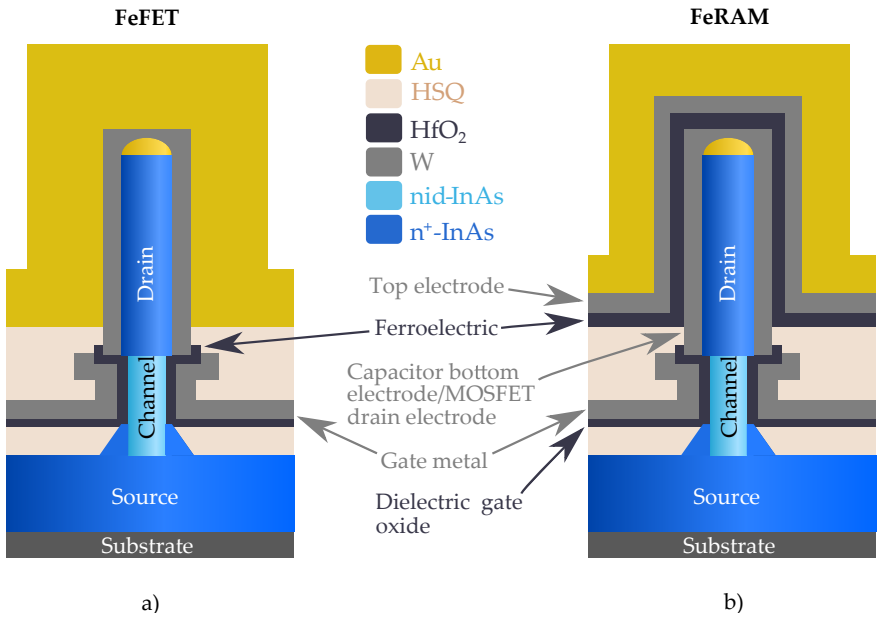


Figure 3.6: Schematic illustrations of proposed gate last III-V nanowire implementations of a) the 1T structure of a gate-last ferroelectric field-effect transistor and b) a 1T1C ferroelectric random-access memory. In b), a regular gate-all-around III-V nanowire MOSFET is at the bottom of the nanowire and a metal-insulator-metal ferroelectric capacitor is wrapped around the drain electrode. In b), the dielectric gate oxide of a regular gate-all-around III-V nanowire MOSFET is exchanged for a ferroelectric oxide.

this thesis as it enables grayscale lithography, i.e., the resist mask is not only patterned in the lateral plane but also the thickness is defined by the EBL dose. This way, both the drain contact height and the spacer oxide thicknesses can be defined [112]. Compared to paper I, IX, and X, oxide spacers would also improve the high-frequency performance by reducing parasitic capacitances [113] and would, due to a considerably smaller gate area, also increase the cycling endurance of the device [108].

A further improvement would be the optimization of a high-quality interlayer oxide between the semiconductor and the ferroelectric HfO_2 at the gate. This is expected to improve both the cycling endurance, retention characteristics, and the subthreshold swing by an improved interface [114]. The electrical performance of the III-V FeFETs presented in this thesis is comparable to early Si FeFET implementations [73, 115], and further interface engineering could be expected to yield a similar performance improvement as has been observed on the Si platform. Due to the high permittivity of

La_2O_3, which is beneficial for reducing polarization-induced electric fields across the interface [114], and its high interfacial quality on InGaAs [116], it seems to be a suitable candidate. However, Al_2O_3 would serve as the most easily implementable due to its widespread use in III-V MOSFETs.

If a successful gate-last process is achieved, it also enables FeRAM implementations where the ferroelectric capacitor is directly integrated on the top electrode as in Fig. 3.6b). A vertical nanowire MOSFET is an interesting selector device as its footprint is low ($4F^2$), while the III-V semiconductors enable a high on-current beneficial for fast operation. Commonly, the small bandgap, and thus big off-state leakage, in III-V transistors is assumed to be a major issue for memory applications. But importantly for III-V based FeRAMs, transistor leakage is not a major issue for FeRAM technology as DC leakage is blocked by the ferroelectric capacitor. The height and radius of the transistor drain electrode can be almost arbitrarily chosen and a capacitor area in line with state-of-the-art FeRAM implementations (e.g., a radius of 50 nm and height of 300 nm [117]) is easily conceivable. As the fundamental structure of a FTJ integrated onto a selector is identical to a FeRAM, the proposed FeRAM-structure in Fig. 3.6b) is a potential application scheme also for FTJs. Just like FeRAM, the big off-state leakage in III-V transistors is not an issue and the high on-current is equally beneficial for speed.

3.5 MM-WAVE INTEGRATION

The capacitor and FeFET structures described above work well for low-frequency characterization, however, for mm-wave applications this is not enough and specialized samples are required to reduce capacitances and access resistances. To enable this, a modified millimeter-wave back end of line (BEOL) was implemented based on Andrić [118] which allows for the connection to a ~30 μm^2 front end of line (FEOL) ferroelectric MOSCAP. The important steps are the introduction of a thick benzocyclobutene (BCB) layer, which due to the low dielectric constant of $\varepsilon_{r,BCB} \approx 2.8$ makes the structure extend measurements well into mm-wave frequencies. An on-wafer-measurement calibration kit (Line-Reflect-Reflect-Match, LRRM) is implemented for removing parasitics in the measurement. The structure minimizes the extension from the calibration reference plane so that the remaining connection structures can be neglected at RF frequencies.

A schematic of the structure is seen in Fig. 3.7. The fabrication starts by growing a 250-nm-thick Sn-doped InAs layer (~$5 \times 10^{19} cm^{-3}$) followed by 50-nm-thick unintentionally doped InAs layer (~$3 \times 10^{18} cm^{-3}$) on a high-resistive (>15 000 Ω cm) Si substrate using MOVPE. The devices are isolated by wet etching InAs mesas after a UV lithography device definition. The native oxide

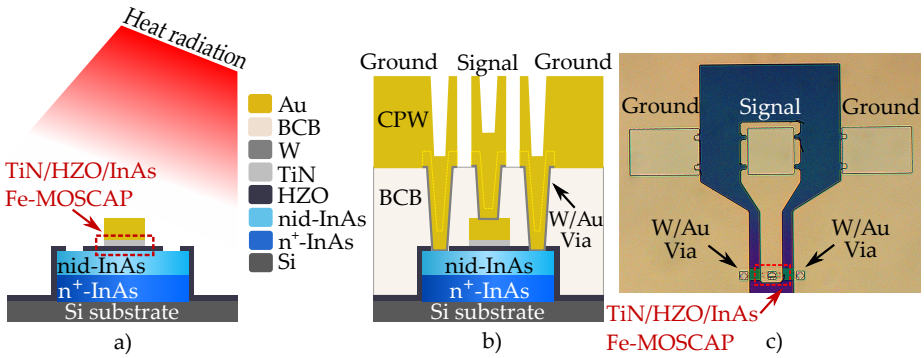


Figure 3.7: Schematic illustration of the mm-wave fabrication process: a) MOSCAP structure at the RTP annealing, consisting of a ferroelectric HZO film, sandwiched between an isolated InAs mesa and a TiN/Au metal, and b) complete structure, including the BCB planarization layer, interconnect vias, and CPW lines. c) A microscope image of the finished structure.

on the InAs is then etched using HCl:H_2O (1:10) followed by the immediate atomic layer deposition (ALD) of HZO deposited at 200°C in a thermal reactor with a 1:1 alternation between the precursors TDMAHf and TEMAZr. A 30-nm thick TiN thin-film resistor (TFR), not shown in Fig. 3.7, is defined by UV lithography and sputtered in order to create 50 Ω match resistances for the mm-wave calibration. 10 nm/100 nm TiN/Au MOSCAP top contacts are defined by UV lithography and sputtered with varying area down to 30 μm^2. Vias through the HZO to the InAs were defined by UV lithography and etched using buffered-oxide etch (1:10), after which the samples were annealed using RTP. The structure at this stage is shown in Fig. 3.7a).

Following the formation of the ferroelectric film, the samples were planarized by spinning and subsequently curing Cyclotene 3022-35 electronic resin into a 1 µm benzocyclobutene (BCB) polymer. The BCB is a low permittivity dielectric ($\varepsilon_r \approx 2.8$) used for high-frequency integrated circuits, which is here also used as a passivation layer. Aside from planarization, the BCB layer improves isolation of the RF/mm-wave propagation from the lossy Si substrate. The BCB layer was thinned to 550 nm by reactive ion etching (RIE) and interconnect vias were defined by UV lithography and dry etched by RIE. Metal contacts to the capacitors were defined by UV lithography and etched out from a sputtered 20 nm W/150 nm Au layer using a KI-based Au wet etch and a RIE W-dry-etch. The vias were sputtered to ensure good connection between layers. Finally, coplanar waveguides (CPW) were deposited by a UV lithography defined thermal evaporation lift-off of 5 nm Ti/500 nm Au.

A Future Outlook

As seen in paper IV, the planar mm-wave integration in section 3.5 indicates that ferroelectric HfO_2 on III-V enables a reconfigurable capacitance with a clear memory window extending into the mm-wave frequencies, i.e., an indication that planar III-V FeFETs can operate at mm-wave frequencies. To pave the way for future vertical nanowire RF FeFETs, structures as in Fig. 3.8 were fabricated to investigate the same properties on nanowires.

Using MOVPE, a 300-nm-thick n^{++}-InAs buffer layer is grown on a p-type Si(111) substrate. Gold seed particles are patterned using EBL and are used to grow vertical nanowires by VLS growth in MOVPE. The devices are isolated by wet etching InAs mesas after a UV lithography device definition. The native oxide on the InAs is then etched using $HCl:H_2O$ (1:10) followed by the immediate atomic layer deposition (ALD) of HZO deposited at 200°C in a thermal reactor with a 1:1 alternation between the precursors TDMAHf and TEMAZr. A 20 nm W top metal is DC sputtered followed by 3 nm ALD TiN. The sample is then anisotropically ICP-RIE etched etching all planar surfaces while retaining the top electrode on the sides of the nanowire. Vias through the HZO to the InAs were defined by UV lithography and etched using buffered-oxide etch (1:10), after which the samples were annealed in N_2 atmosphere by RTP to crystallize the HZO into the ferroelectric orthorhombic phase. See Fig. 3.8a) for a schematic and the front page of the thesis for a SEM image of the sample at this stage.

Following the formation of the ferroelectric film, the samples were planarized by spinning and subsequently curing Cyclotene 3022-35 electronic resin into a 1 µm benzocyclobutene (BCB) polymer. The BCB layer was thinned to 450 nm by Reactive Ion Etching (RIE) so about 100 nm of the wires were sticking up and interconnect vias to the InAs were defined by UV lithography and dry etched by RIE. Metal contacts to the top electrode of the nanowires and the InAs mesa were defined by UV lithography and etched out from a sputtered 20 nm W/150 nm Au layer using a KI-based Au wet etch and a RIE W-dry-etch. The vias were sputtered to ensure good connection between layers. Finally, coplanar waveguides (CPW) were deposited by a UV lithography defined thermal evaporation lift-off of 5 nm Ti/500 nm Au resulting in a structure as in Fig. 3.8b).

As seen in Fig. 3.8c), the unannealed samples work as nanowire capacitors. The behavior closely corresponds to a similar study in literature [119], indicating that the design is functioning. However, the annealed (ferroelectric) films are too leaky for CV measurements. The reason for this leakage in the annealed films was never figured out as the ALD broke down and no more samples could be made during this PhD project. Possible reasons could be 1) that the gold particle diffuses into the HZO during the RTP and shorts the

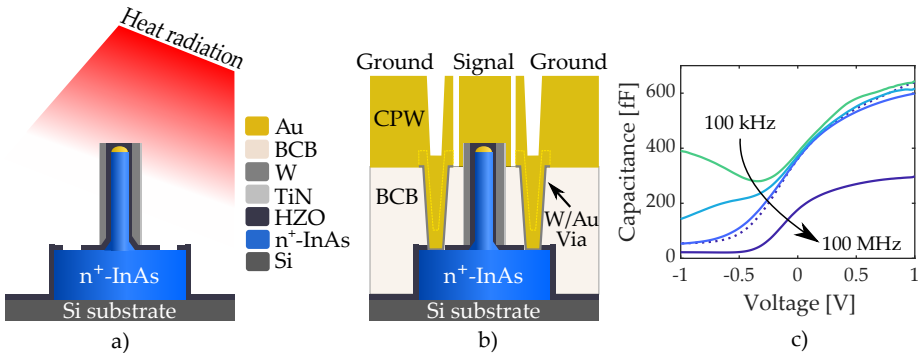


Figure 3.8: a) Schematic illustration of the nanowire MOSCAP at the RTP annealing, consisting of highly doped InAs wires covered by a ferroelectric HZO film and a W/TiN top metal. b) The complete structure, including the BCB planarization layer, interconnect vias, and CPW lines. c) Capacitance-voltage measurements of an unannealed sample showing clear capacitance modulation. Full lines are using a parallel equivalent circuit as the films are leaking, but for 100 MHz the nanowire resistance starts dominating and the capacitance drops. To compensate for this, the dotted line corresponds to 100 MHz with a series equivalent circuit.

capacitor or 2) that the RIE damages the HZO on top of the wire or at the foot down to the mesa, but that this only matters for an annealed sample. Nevertheless, the structure in Fig. 3.8 is promising and if the leakage issue for the annealed HZO could be figured out, it would be a suitable method to investigate the defects in the ferroelectric film when integrated on nanowires.

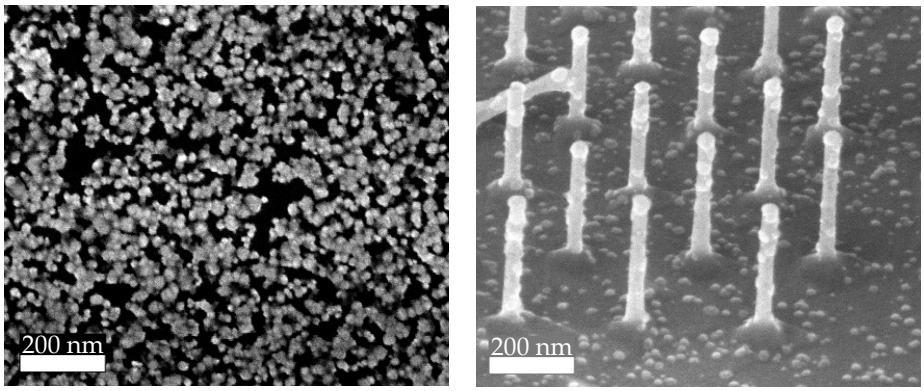
4

Microstructural Analysis

As pointed out in chapter 1 and 2.3, the properties of III-V nanowires and ferroelectric HfO_2 are governed by effects on the nanometer or even Ångström scale. Even if optical methods are very valuable and commonly used while investigating samples during processing, it does not have enough lateral resolution for investigations on the nanoscale. Therefore, nanostructures are generally imaged by electron or scanning probe microscopy techniques (when interested in a specific position) or diffraction techniques (when an average property across a larger area is of interest). Light-based methods are though excellent for out-of-plane thickness resolution by interferometry and ellipsometry, and furthermore provide excellent chemical determination through photoelectron spectroscopy. This chapter aims at providing an overview of the methods used during this work.

4.1 ELECTRON MICROSCOPY

The maximum resolution obtainable with light microscopy is limited by the wavelength of the photons used and sets a practical resolution limit on the micrometer scale. Electron microscopy techniques build upon the fact that the electron wavelength is considerably smaller than visible light wavelengths (e.g., 1.2 nm at 1 eV) and that the imaging resolution is instead limited by non-idealities in the electrostatic lenses [120].



a) b)

Figure 4.1: Scanning electron microscopy images of a) a HZO film deposited by atomic layer deposition at 300°C showing clear crystallites after a buffered oxide etch (BOE). b) HZO crystallites on InAs nanowires formed after a 60 nm W/10 nm HZO/InAs-stack had been annealed at 450°C for 30 s. The sample had the W removed by reactive ion etching and no crystallites were visible before the subsequent BOE.

4.1.1 SCANNING ELECTRON MICROSCOPY

Scanning electron microscopy (SEM) has been extensively used throughout this thesis as it excels at the length scales used in the nanowire MOSFET fabrication process. When scanning a focused electron beam across the sample, the electrons interact with the sample producing various signals. Depending on what detector is used, e.g., measuring the amount of secondary or back-scattered electrons, images can be obtained with both information on surface topography and atomic composition. A major advantage of the technique is that one obtains real space images similar to optical images making the data easy to analyze [120]. This is highly useful working with nanowire MOSFETs, e.g., placement of gates and thickness of spacers.

But the polycrystalline ferroelectric films are in general difficult to image as they just look like a smooth surface. However, there is an etch selectivity between amorphous and crystalline HfO_2 in BOE, meaning that the ferroelectric grains can be investigated by SEM if the films are etched as in Fig. 4.1. A fully crystallized HfO_2 film is not etched by BOE, so the analysis is limited to partially etched films. Electron backscatter diffraction (EBSD) is a SEM technique that could be used to map fully crystallized HfO_2 films in order to investigate size, orientation, and crystal phase of the grains [121].

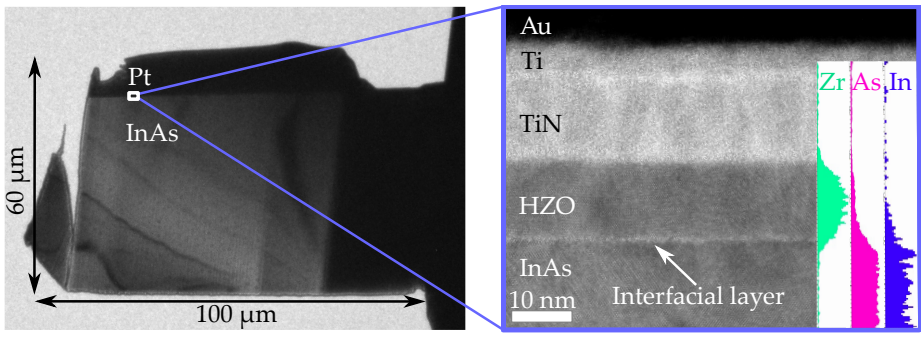


Figure 4.2: Transmission electron microscopy (TEM) images of a) a lamella from a ferroelectric MOSCAP annealed at 470°C for 30 s. b) A well-defined sharp InAs/HfO_2 interface can be seen with a 2–3 atomic layers thick interfacial layer between the crystalline InAs and HfO_2. The inset is an energy-dispersive X-ray spectroscopy (EDX) mapping using scanning mode TEM (STEM). The absolute positions in the EDX should be treated cautiously as the sample drifts during the measurement, but a relative comparison to the Zr signal indicates a slight diffusion of In and especially As into the HZO.

4.1.2 TRANSMISSION ELECTRON MICROSCOPY

By relying on transmission of electrons through the sample rather than energy losses from a variety of mechanisms as in SEM, transmission electron microscopy (TEM) achieves a considerably higher resolution. This resolution comes at the cost of complexity in both sample preparation and data analysis. To enable TEM, a lamella of the material (usually less than 100 nm thick) has to be cut out by focused ion beam (FIB) as is seen in Fig. 4.2a).

When electrons pass a thin crystalline material, the electrons are diffracted. By Fourier-transforming the diffraction pattern (usually through an electrostatic lens), an atomic resolution image is obtained. If the TEM is instead operated as a SEM, e.g., by scanning a focused electron beam across the sample, it is called scanning mode TEM (STEM). This is for instance used in order to obtain high resolution spatial elemental analysis of the sample as the inset in Fig. 4.2b) through the method of energy-dispersive X-ray spectroscopy (EDX). The method is utilize the fact that atoms have a unique atomic structure, i.e., shell energy levels, giving each element a unique electromagnetic emission spectrum. The STEM beam ionizes the atom and when an electron from an outer shell fills the newly created hole an X-ray of a very specific wavelength is emitted and can be measured [120].

4.2 SCANNING PROBE MICROSCOPY

Scanning probe microscopy (SPM) is a family of techniques aimed at understanding materials at nanoscopic or even atomic resolution. A sharp tip on a flexible cantilever is raster-scanned across the sample to retrieve information about the surface. Depending on method, it can provide insight into structural, mechanical, electronic, vibrational, magnetic, and chemical properties [122]. In this thesis, the main methods used are atomic force microscopy (AFM) and piezoresponse force microscopy (PFM). Both are based on sensing the deflection of the cantilever in order to retrieve the topographic and piezoelectric properties of the sample, respectively.

In AFM, when the tip gets close to a surface, local forces between the tip and sample affects the cantilever and these small deflections can be detected by a laser beam that is reflected on the backside of the cantilever. This way, the method can achieve real space imaging of the topography with a height resolution on atomic scale and spatial resolution on the nanoscale [122].

All ferroelectric materials are also piezoelectric, meaning that they acquire a polarization when subjected to mechanical stress and conversely are undergoing deformation when subjected to an electric field. This is utilized in PFM by applying an AC electric potential to the tip, which causes the material to deform and thereby deflect the cantilever. This response is often on the picometer scale making the use of a lock-in amplifier necessary to distinguish between signal and noise [123]. As the piezoelectric response of a ferroelectric material is different depending on the polarization state, the method can be used to image the ferroelectric domains in HfO_2-based ferroelectrics [124].

4.3 OPTICAL MEASUREMENTS

Due to its speed and low cost, optical microscopy is by far the most used characterization technique throughout this project. But as stated above, the in plane resolution is insufficient for nanoscale characterization. However, optical methods such as interferometry and ellipsometry are excellent tools for thickness determination and may very well outperform electron microscopy in terms of speed and resolution. Through photoelectron spectroscopy, chemical determination can be achieved, whereas diffractometry provides an excellent method for investigation of crystal lattices.

4.3.1 INTERFEROMETRY AND ELLIPSOMETRY

Due to the short wavelength of visible light, the interference of light waves is highly useful for measuring the thickness of layers. For thin materials, best seen in the fringes of a soap bubble, the color of a material is dependent on

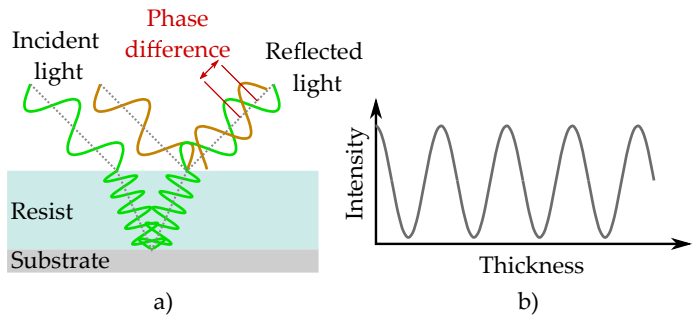


Figure 4.3: a) Principle of interferometry for thickness in-situ thickness control during etching. b) Due to the constructive and destructive interference occurring as a function of the resist thickness, the thickness can be well controlled by knowing how many wavelengths a certain thickness thinning corresponds to.

its thickness and refractive index [125]. For a trained eye, the color of the material is enough to give a rough estimate of its thickness within a few tens of nanometers.

By shining a laser, i.e., monochromatic and coherent light, onto the films as in Fig. 4.3, clear interference can be seen in the reflected light depending on if constructive or destructive interference occurs at the upper interface. Since constructive and destructive interference occurs with path difference of half a wavelength, the spatial resolution for a common laser interferometer is below 200 nm for common resists. In practice, considerably better resolution is achieved as intermediate values of intensity between the maxima and minima can also be used. Interferometry is the go-to way for achieving thickness control in films thicker than 50 nm throughout this thesis. A benefit of the technique is that it can be used in-situ during the backetch of a resist in order to control the resist thickness. In spectral reflectance thickness measurements, several wavelengths are used at once, meaning that not only relative thicknesses can be measured but also the absolute thickness of the film [125].

Due to the wavelength of visible light being on the order of a couple hundred nanometers, single nanometer thick films are though difficult to measure by interferometry. To overcome this, spectroscopic ellipsometry has been used throughout this thesis to measure films when high resolution of the absolute thickness is required. In this setup, elliptically polarized light is at different angles reflected onto the surface containing the thin film. Since the reflectivity and phase shift of the reflected light is polarization dependent, measurement of these properties enables exact thickness determination down

to sub-nanometer level and can be used to measure other properties such as dielectric constant (useful in ALD optimization) and surface roughness (useful in etch development) [126].

4.3.2 PHOTOELECTRON SPECTROSCOPY

Photoelectron spectroscopy builds upon the photoelectric effect (that awarded Einstein his Nobel prize in 1921), i.e., the principle that electrons are emitted when electromagnetic radiation (light) hits a material if the photon has an energy bigger than the binding energy of the emitted electron. Uppsala researcher Kai Siegbahn received the Nobel Prize in 1981 for his development of X-ray Photoelectron Spectroscopy (XPS). The method uses a monochromatic photon beam, i.e., all photons have the same energy. When a photon excites an electron, the photon energy in excess of the binding energy (and the energy to the vacuum level from the Fermi level) becomes kinetic energy. The energy distribution of the kinetic energy can be detected by an electron energy analyzer and the acquired spectra is fitted to determine the chemical components and the surface composition. Important for this thesis, different chemical bondings have different bonding energies making it possible to determine what materials bond to each other [127]. This is highly useful to determine what occurs at interfaces when different materials are integrated onto each other.

In collaboration with the synchrotron physics group in Lund, XPS has been extensively used throughout this project to investigate the interface between ferroelectric HfO_2 and III-materials. As described in section 3.3.2, the main issue for these measurements is the short inelastic mean free path (IMFP) of the photoelectrons which for common XPS energies 100 eV to 1.5 keV result in 0.4 – 2 nm IMFP [107]. The interface between the HfO_2 and the III-material will in a realistic MOSCAP structure inevitably be at several nanometers' depth, meaning that the signal is weak. This unfortunately lowers the methods applicability as measurements require considerable signal averaging, making time a major constraint during allocated beam times at synchrotron radiation facilities.

To overcome this, the Hard X-ray photoelectron spectroscopy (HAXPES) available at the I09 beamline at Diamond Light Source was used as the higher photon energy of 5.9 keV enables an IMFP of about 5 nm [107]. Using the device described in section 3.3.2, a realistic ferroelectric MOSCAP structure could be electrically biased and measured in operando. As shown in paper XI, this enabled the direct investigation chemical changes at the oxide/semiconductor interface induced by the ferroelectric switching.

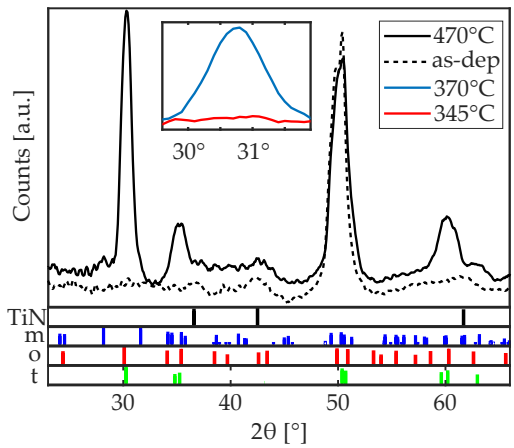


Figure 4.4: Grazing incidence X-ray diffraction of HZO measured at an incidence angle of 0.5°. The inset shows the clear crystallization of the HZO at 370°C. The insets below are simulated powder diffractograms of cubic TiN, monoclinic HfO_2, orthorhombic $Hf_{0.5}Zr_{0.5}O_2$, and tetragonal HfO_2.

4.3.3 DIFFRACTOMETRY

In order to characterize crystals, x-ray diffraction is one of the central techniques. The method builds upon irradiating the crystal with x-rays with a certain angle followed by measuring the reflected light. Due to the highly ordered atomic structure of a crystal, light is only reflected at certain angles in which the reflections from the atomic planes interfere constructively with each other. For most angles, the reflected light interferes destructively and only a low intensity is measured. The reflected light pattern provides information of the distance between crystallographic planes and using this, the crystal structure can be deduced. This means that the microscopic structural information is averaged over a large volume, in contrast to most scanning microscopy techniques which instead provide real-space images.

The materials studied in this thesis are generally very thin polycrystalline films with thicknesses on the nanometer level. As X-rays typically have a penetration depth on the millimeter scale, there is a need to use grazing incidence angles to increase the surface sensitivity. The technique is generally referred to as grazing incidence X-ray diffraction (GIXRD) and builds on the fact that for most materials, the refractive index for x-rays is lower than (but very close to) 1. This means that low-incidence x-rays are totally reflected at a very small critical angle, α, with respect to the sample surface, α_c, i.e., between 0.1-1° for most materials. By keeping the angle above the critical angle, the penetration depth can be tuned down to a few nanometers close to

the critical angle; thus, maximizing the signal from the thin film and reducing the background from the substrate [128, 129]. For HfO_2-based ferroelectric films, the incidence angle is usually chosen around 0.5°, but in the presence of top electrodes the angle might need to be increased.

5

Electrical Characterization

All electrical measurements in this thesis are based on the structures described in chapter 3. Since the measurement techniques for vertical III-V nanowire transistors and capacitors have been described in earlier theses, e.g., by Hellenbrand [130] and Wu [131], the focus in this chapter will be on those measurement techniques that are specific to FeFETs.

5.1 CAPACITOR MEASUREMENTS

For measurements on capacitors, one would ideally want to electrically connect to the two electrodes using Ohmic contacts. This is for instance done in the mm-wave structures by the usage of vias. For most capacitor measurements, the extra steps required to fabricate low resistance vias do not bring enough advantages compared to the extra fabrication complexity. Thus, most capacitors follow the processing described in section 3.3 and, as shown in Fig. 5.1, a low resistance connection to the bottom electrode is created by shorting two capacitors on the sample and then using one of them as the bottom electrode while measuring a third capacitor. The resistance of a shorted capacitor is below a few hundred ohms, which is sufficiently low for most low-frequency measurements.

5.1.1 POLARIZATION MEASUREMENTS

As described in section 2.1, the characteristic parameters for a ferroelectric material are retrieved from the polarization-voltage (PV) hysteresis loop, i.e., the remanent polarization, P_R, and the coercive field, E_C. This loop can be measured in a multitude of ways, but most are based on measuring the displacement current of a capacitor as a function of voltage. The displacement

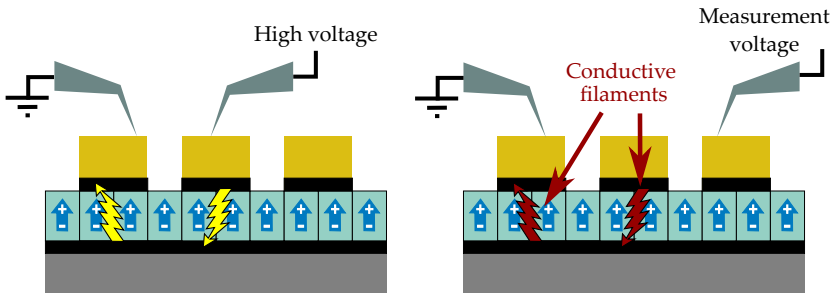


Figure 5.1: To measure ferroelectric capacitors, a common method is to 1) short two capacitors by applying a big voltage. This creates a conductive filament which connects the top electrode to the bottom electrode by a low resistance. 2) By using one of the shorted capacitors as the bottom electrode, measurements can be performed on a third capacitor.

field of a capacitor, D, is an areal charge density defined as

$$D = \varepsilon_0 E + P = \varepsilon_0(1 + \chi_e)E = \varepsilon_0 \varepsilon_r E = \frac{Q}{A} = \frac{\int I(t)\mathrm{d}t}{A} \tag{5.1}$$

where ε_0 is the electric permittivity of free space, E the electric field, P the polarization, χ_e the electric susceptibility, ε_r is the relative permittivity of the material, Q the capacitor charge, A the capacitor area, I the displacement current, and t time.

As one is generally interested in P rather than D, one has to subtract the vacuum contribution $\varepsilon_0 E$. But in practice, due to the high permittivity of the ferroelectric material, the simplification $D = P$ is often made as the difference is often less than 1% in a ferroelectric HfO_2 film [132]. The measurement of the remanent polarization is entirely unaffected by this error as the electric field by definition is zero, and the coercive field is essentially unaffected as the flanks of the hysteresis curve usually are steep.

Measuring absolute values of polarization is difficult as only changes in charge are measured. Commonly, the polarization is therefore assumed to be symmetric so that $|P_{max}| = |P_{min}|$. This may be a reasonable assumption on a symmetric device, however, for a capacitor with different top- and bottom electrodes or a MOS-system this is not necessarily true and the polarization may be bigger in one direction than the other.

The way of measuring the hysteresis loop is similar, but it is measured and analyzed differently in the two most common techniques: polarization-voltage (PV) and positive-up-negative-down (PUND). The current response

of a ferroelectric capacitor does, to a first approximation, consist of three contributions:

1. The dielectric current: $I(t) = \frac{\mathrm{d}Q(t)}{\mathrm{d}t} = C\frac{\mathrm{d}V(t)}{\mathrm{d}t}$
2. The ferroelectric switching current, i.e., the current at the coercive voltage which corresponds to the charge movement inside the film when the ferroelectric switches
3. Leakage current

Current 1. and 2. are, to a first approximation, linearly dependent on the time derivative of the voltage, which makes the measured charge Q independent of the measurement frequency. On the other hand, 3. is dependent on the voltage, which means that the measured charge through the capacitor is time dependent. The leakage current is unwanted and causes a distorted hysteresis loop, which makes measurements on thin films difficult due to the tunneling leakage. The distortion caused by leakage can either be reduced by increasing the measurement speed or by leakage subtraction (e.g., the soon to be explained PUND technique).

PV-measurements are performed by applying a triangular voltage wave as in Fig. 5.2a) and concurrently measuring the current through the device. By integrating the current over time and dividing it by capacitor area as in eq. (5.1), a polarization value is obtained at each voltage, which plotted in a PV-graph gives the characteristic hysteresis for a ferroelectric, see Fig. 5.2b).

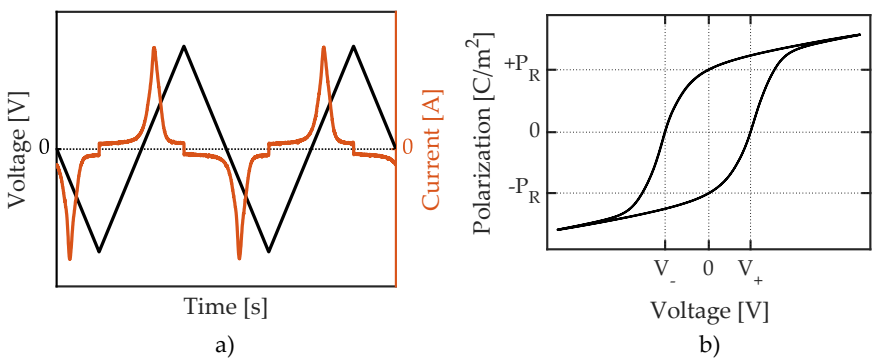


Figure 5.2: a) A PV current-voltage measurement of a TiN/HZO (10 nm)/TiN MIMCAP annealed at 600°C with b) the corresponding polarization-voltage hysteresis curve where P_R is the remanent polarization and V_- and V_+ the negative and positive coercive voltage of the film. The contribution from the dielectric current is seen in that the saturation polarizations at the peak voltages are larger than the remanent polarization.

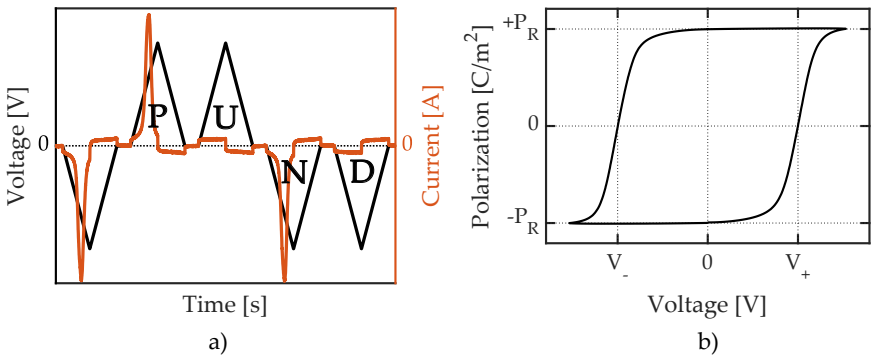


Figure 5.3: a) A PUND current-voltage measurement of a W/HZO (13 nm)/InAs MOSCAP annealed at 550°C with b) the corresponding polarization-voltage hysteresis curve.

The PUND-method is a further development whose main goal is to subtract the leakage 3., but it does at the same time also subtract the dielectric current 1. It does this by the application of two positive pulses (P and U) followed by two negative pulses (N and D) as in Fig. 5.3). The initial negative pulse is used to set the state before the actual measurement. By subtracting the U current (second pulse) from the P current (first pulse) and similarly the D current (fourth pulse) from the N current (third pulse), the remaining current is assumed to be purely the ferroelectric switching current. This as the dielectric response 1. and the leakage 3. stay the same in two consecutive pulses. By tuning the time in between the two consecutive pulses, e.g., P and U, it is possible to measure how quickly the film depolarizes (loses its polarization state).

The three contributions above are not an exhaustive list and many other contributions exist such as defect charging or mobile ions in the film (two rather common issues for ALD-grown films). Especially the case of mobile ions is difficult to differentiate from ferroelectricity as both involve moving charged ions in the film. For instance, if measuring an amorphous HfO_2 from our ALD, we measure a small remanent polarization of <0.5 $\mu C/cm^2$ using PUND, which can probably be assigned to defect charging or mobile ions in the film. Misinterpreting something as ferroelectric by polarization measurements is unfortunately rather easy for an untrained eye and claims of ferroelectricity in new materials should therefore be taken cautiously if based purely on polarization measurements. That is the reason why most researchers chose to use several methods to verify ferroelectricity [133].

5.1.2 CYCLING BEHAVIOR

Using polarization-voltage measurements and PUND, most fundamental properties of the ferroelectricity in a film can be investigated. When a film is electrically cycled for the first time, there is generally a so-called wake up phase during which the ferroelectric properties become increasingly more prominent the more voltage cycles that are applied. This can be seen in Fig. 5.4a) where further cycling results in an increasing remanent polarization. Commonly, this behavior is attributed to the redistribution of oxygen vacancies in the ferroelectric film [134]. After a certain number of cycles, the measured remanent polarization peaks and starts decreasing again as seen in Fig. 5.4b). This decreasing behavior is referred to as fatigue and is commonly attributed to a generation of charged defects in the films upon switching which either pin the domains (electrostatically change the potential landscape around the domain so that the coercive field increases) or inhibits the nucleation of the opposite polarization state [135]. Finally, the films undergo a hard breakdown when the defects create a conductive filament which at some point causes a runaway current which shorts the device. The number of ferroelectric switching cycles that the film handles is referred to as the endurance of the film.

The field-cycling endurance of state-of-the-art MIM-structures is $>10^{11}$ [78] and the highest measured endurance during the course of this thesis is 10^8, e.g., in Fig. 5.4b). 10^8 is a test limit set by our measurement setup rather than the actual endurance of the device and some MIMCAPs do therefore have a higher endurance than 10^8. As seen in Fig. 5.4c) and Fig. 5.4d), the III-V HZO MOSCAPs do in general have a lower endurance than MIM devices reaching $>10^6$ for lower voltage switching and $<10^5$ for higher voltage pulses.

The ferroelectric MOSCAPs integrated on III-V materials, such as in Fig. 5.4c) and Fig. 5.4d), have followed the same trends as is commonly observed on Si and MIM integrations. The required operating voltage to fully wake up and switch the remanent polarization is about twice the coercive voltage, meaning that it is rather close to the breakdown voltage of the films. As the coercive field is independent of thickness, while the breakdown field increases with thickness, thinner films are expected to have a higher endurance [136]. However, for the III-V integration in this project, this is not trivial to implement as thinner films also require a higher annealing temperature which has proven detrimental to the III-V nanowires. Another method for high endurance is, as in 5.4c), to use short voltage pulses to switch the ferroelectric. It has been shown that the number of endurance cycles in MIMCAPs is proportional to the operating frequency, indicating that it is the total stress time which generates the breakdown rather than the ferroelectric switching [136]. A similar albeit not as clear of a trend is

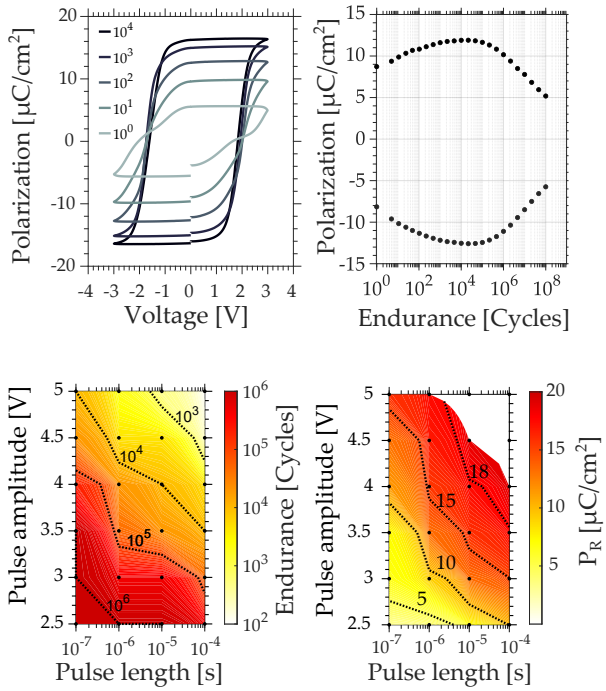


Figure 5.4: a) A PUND current-voltage measurement of a W/HZO (13 nm)/InAs MOSCAP annealed at 550°C as a function of wake up cycles. b) The remanent polarization of a W/HZO (13 nm)/TiN annealed at 540°C showing a clear wake up during the first 10^4 cycles and a clear fatigue beyond 10^6 cycles. c) Endurance as a function of voltage and pulse time. (b) Remanent polarization after 1000 cycles of wake up as a function of voltage and pulse time. The white upper right corner indicates a hard breakdown before 1000 wake-up cycles.

seen in 5.4c), but undoubtedly higher frequency gives higher endurance also on III-V integrations. An important factor is though that higher frequency has been accompanied by fatigue-limited endurance rather than breakdown-limited endurance [136].

Another important factor for high endurance is the area of the capacitor, meaning that the endurance in Fig. 5.4c) should be regarded as a lower limit for actual device implementations which will be orders of magnitudes smaller. Earlier work has shown that for MIM devices, the endurance may increase by as much as an order of magnitude per order of magnitude decrease in area [108]. Finally, as indicated in 5.4c), decreasing the operating voltage will increase the endurance but, as seen in Fig. 5.4d), at the cost of a decrease in

the switched remanent polarization. Partially polarized states obtained by a lowered operation voltage have shown poor retention [137]. In practice, there is therefore a clear trade-off between the applied voltage, the time scale the devices are operated at, and the achievable number of switching cycles.

5.1.3 SWITCHING DYNAMICS

As described in section 2.1, the ferroelectric film consists of many domains with different coercive voltages depending on their crystal orientation. When switching a ferroelectric film by a voltage pulse, the time evolution can be described by Fig. 5.5. Starting at a saturated state -P_S and applying a positive voltage, the domains will switch until eventually obtaining the positive saturated state, $+P_s$. If the voltage pulse is sufficiently short, a partially polarized state is stabilized.

To describe ferroelectric switching, two models are commonly used: the Kolmogorov-Avrami-Ishibashi (KAI) model and the nucleation limited switching (NLS) model. KAI is common for bulk ferroelectrics and assumes that domain wall migration is slower than the nucleation of reversed domains. In thin polycrystalline films, such as ferroelectric HfO_2, the distance the domain wall can move is limited and instead the NLS model can be used [77]. NLS is based on the free energy for domain nucleation and gives a switching time-voltage relation of

$$t_{sw} = t_0 \exp\left(\frac{\alpha}{k_B T}\frac{1}{V_{pulse}^2}\right) \tag{5.2}$$

where t_0 is the minimal nucleation/switching time, α a domain wall energy dependent parameter, k_B the Boltzmann constant, T the temperature, and V_{pulse} the applied voltage across the ferroelectric film [138]. The model's applicability has been confirmed by PFM studies [139], over eleven orders of magnitude in time [140], and in grain by grain switching in nanoscaled few

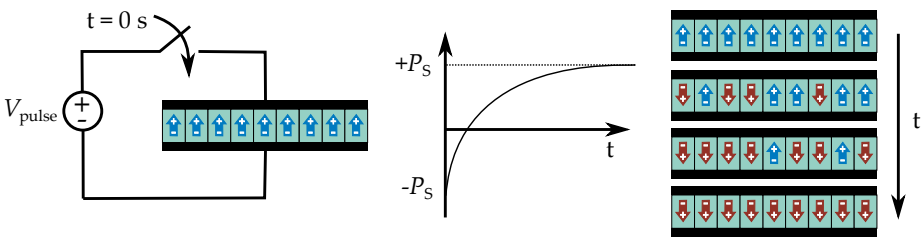


Figure 5.5: Schematic showing how individual domains switch independently of each other when a voltage is applied.

domain FeFETs [138]. In line with a common assumption that polarization switching in one grain occurs without strongly affecting neighboring grains, [141] we in paper IX measure the switching dynamics of a single ferroelectric domain integrated onto a III-V nanowire transistor and find that it can be fitted to the NLS model.

Nanosecond Pulsing

In order to test the switching speed of the ferroelectric films integrated on III-V materials, a set-up as in Fig. 5.6a) is used to measure the mm-wave capacitors described in section 3.5. The usage of the bit-error-tester Agilent N4906B (BERT) as a pulse generator enabled pulsing down to 80 ps with 1.8 V_{p-p}. The measurement method is similar to the PUND method and uses a millisecond long pre-set pulse to set the state followed by short voltage pulses of opposite polarity. As seen in Fig. 5.6c), switching speeds of some tens of nanoseconds were measured depending on the definition of switching. By accumulative pulsing, i.e., comparing the current response before and after 100 pulses, switching was observable down to 5 ns albeit not visible when comparing two consecutive pulses. This is slightly slower, but in line with earlier research that accumulative switching can be obtained at shorter pulses. For instance, a capacitor has in a similar setup been switched on a sub-ns time scale when applying 9 V pulses whereas accumulative switching has achieved threshold voltage shifts of transistors [142, 143].

5.1.4 CAPACITANCE-VOLTAGE

Capacitance-voltage (CV) measurements are arguably the most common method for MOS characterization and extensively used in ferroelectric characterization. It provides the basic information on film properties such as thickness, permittivity, flat-band voltage, and defect states. In this part, the basics of the method will be treated and especially the measurement complications caused by a narrow bandgap III-V semiconductor compared to the more conventional MIMCAPs and silicon-based MOSCAPs.

The working principle is that the differential capacitance is measured using a small oscillating voltage superimposed on a DC bias that is swept. By measuring the displacement current and the phase shift compared to the applied AC-voltage, a complex admittance is obtained which through an equivalent circuit is converted into a capacitance and conductance. There are increasingly more complex models depending on the system under investigation, but a serial equivalent circuit is reasonable when the access resistance (contact resistance, substrate resistance, etc.) dominates the leakage through the films,

whereas the parallel equivalent is reasonable when the leakage through the film dominates the access resistance.

For a simplified dielectric MIMCAP, the measured differential capacitance consists purely of the oxide capacitance $C_{ox} = \varepsilon_0 \varepsilon_r A / t_{ox}$ where ε_0 is the vacuum permittivity, ε_r the relative permittivity of the oxide, A the area of the capacitor, and t_{ox} the thickness of the oxide. Importantly, this means a bias independence. For a ferroelectric MIMCAP, the situation becomes more complex as ferroelectric materials possess a double-peaked CV characteristic (often referred to as butterfly-like) with a strong bias dependence. This effect of capacitance maxima around the negative and positive coercive voltages is usually attributed to a non-linear domain wall capacitance close to the coercive voltage, [144] but other explanations such as space-charge concentrations at the ferroelectric-electrode interface are also given [145].

For a simplified dielectric MOSCAP, the measured differential capacitance consists of two capacitive components connected in series and can be described as

$$C_{tot} = \frac{C_{ox} C_s}{C_{ox} + C_s}$$

where C_{ox} is the oxide capacitance and C_s is the semiconductor capacitance. As in the dielectric MIMCAP above, C_{ox} is bias independent. But C_s is related to the number of free charge carriers close to the semiconductor interface, i.e., a highly bias dependent property that moreover is dependent on the

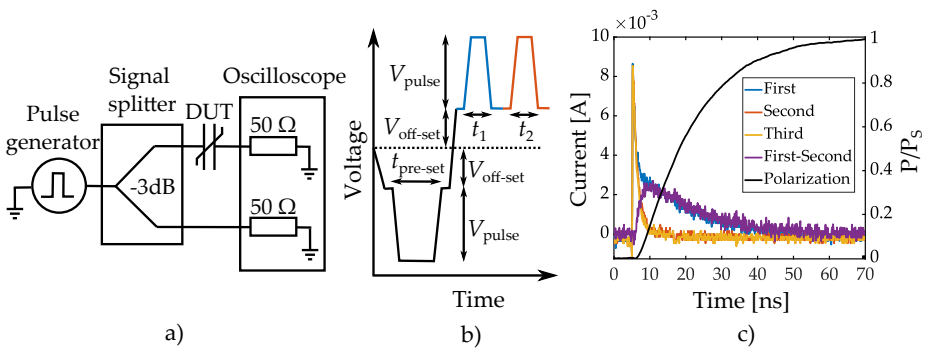


Figure 5.6: a) A schematic of the setup used for nanosecond pulsing. b) The films were first pre-pulsed in order to set the polarization state followed by repeated pulses with the opposite voltage polarity. Due to a peak-to-peak V_{p-p} limitation, the voltage was DC-offset to enable higher maximum voltages. c) By pulsing a 6 nm HZO on InAs by 100 ns long 1.8V pulses (DC-offset 1V), a clear difference in the current response can be seen in the first and second pulse (third pulse is almost identical to the second). By integrating the current difference, half of the remanent polarization switches in 11 ns.

measurement frequency, temperature, etc. The capacitive behavior of III-V MOSCAPs has previously been treated by Wu [131] and Babadi [146]. III-V MOSCAP modelling is already non-trivial and by further adding a non-linear ferroelectric oxide capacitance whose capacitive response is poorly understood in MIMCAPs, the modelling of our ferroelectric III-V MOSCAPs proved inaccurate. Nevertheless, CV measurements on ferroelectric MOSCAPs can provide important information on their working principles. Below different methods to measure defects and threshold voltage shifts in ferroelectric III-V integrations are described.

Traps in HfO_2

The deposition of high-κ materials, typically by ALD, typically give rise to material imperfections which, depending on their chemical and structural nature, have a varying probability to capture (acceptors) or emit (donors) free carriers in the semiconductor [147]. Oxide non-stoichiometry, i.e., oxygen vacancies and interstitial atoms, are usually regarded to be the main origin of these traps [148]. A basic classification of the traps can be given by their distance from the oxide/semiconductor interface. Those located in the "bulk" are referred to as border traps whereas those close to the interface are called interface traps [149]. Through tunneling processes, the traps interact with carriers in the semiconductor and may cause reliability issues such as time-dependent variability depending on the charge state of the defect.

All states well below the Fermi level can be regarded as filled whereas defect states close to the Fermi level of the semiconductor, i.e., in and close to the semiconductor bandgap, will interact with the semiconductor. The capture/emission time constants of defects are dependent on both the tunneling distance into the oxide, x, and the activation energy of the capture/emission process, E_A:

$$\tau_{c/e} = \tau_0 \exp\left(\frac{E_A}{k_B T}\right) \exp\left(\frac{x}{\lambda}\right) \tag{5.3}$$

where k_B is the Boltzmann constant, T the temperature, and λ the tunneling attenuation length [150]. In CV measurements, this means that a certain measurement frequency measures the capture and emission of defects with a response time faster than the measurement frequency. When the measurement frequency exceeds $1/\tau_{c/e}$, the trap no longer responds and the measured capacitance decreases. E.g., at $f = 1$ MHz, defects with capture and emission time constants faster than 1 µs will contribute to the measured capacitance. The frequency dispersion, i.e., how much the capacitance changes as function of frequency, is therefore a way of investigating the defect density close to a semiconductor interface [151].

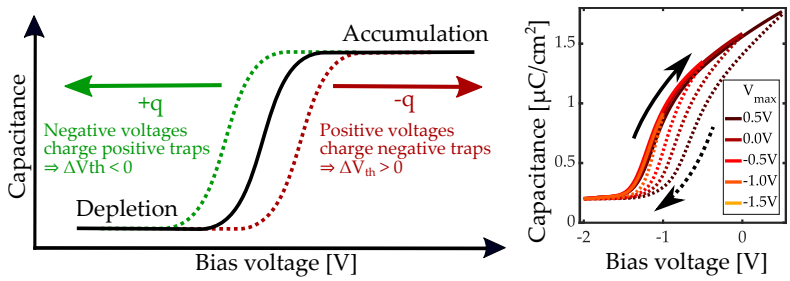


Figure 5.7: a) The effect of charged defect states on CV measurements. b) Due to increasingly more negatively charged traps at higher positive bias, a low-to-high-to-low bias sweep will induce a clockwise hysteresis in a CV measurement.

In highly scaled devices, the electrostatics can be governed by small changes in the trapped charge and so-called random telegraph noise occur due to the capture and emission in a single defect [152]. For instance, in paper IX, a single charge trapping event can give rise to random telegraph noise (RTN) in a TFET with a ferroelectric gate oxide. The single elemental charge being captured and emitted gives rise to a 19 millivolts threshold voltage shift in the device.

Also slower traps (almost fixed charges) affect the CV measurements as the corresponding charge buildup in the oxide changes the electrostatics of the high-κ. They do not directly affect the differential capacitance by repeated capture and emission as in the case of frequency dispersion, but their electrostatic effect caused by either a remanent capture or emission event shift the CV curve as indicated in Fig. 5.7a). Since there is a distribution in the interaction time constants and energy levels of the traps, the charge buildup depends on bias sweep rate, the start and stop voltages, and the temperature. By Gauss' law, these charges, Q_t, shift the threshold voltage,

$$\Delta V_T = -\frac{1}{C_{ox} d} \int_0^d x\rho(x)\, dx \Rightarrow Q_t = \frac{\Delta V_T C_{ox}}{q} \tag{5.4}$$

as a function of the charge density of the defects $\rho(x)$ in a film of thickness d and an oxide capacitance density C_{ox} [153]. Although it has been shown that the spatial distribution of defects is important to the dynamics within the high-κ, [154] it is, for simplicity, commonly assumed that Q_t can be regarded as a charge sheet located at the semiconductor-oxide interface. For dielectric silicon MOSCAPs, this method of investigating bias dependent V_T-shifts is

a well-established technique to give an estimation of the defect density in films [1].

Bias dependent V_T-shifts are though seen in all MOS-systems and, as seen in Fig. 5.7b), results in a clockwise hysteresis in CV-measurements. Due to charge trapping at defect sites, a low-to-high voltage sweep has more positive charge in the oxide than a high-to-low voltage sweep. As indicated by Fig. 5.7a), this lowers the threshold voltage and makes a CV measurement underestimate V_T, while a high-to-low voltage sweep overestimates V_T. In a bidirectional sweep, i.e., low-to-high-to-low or high-to-low-to-high, this causes the clockwise hysteresis seen in both CV and MOSFET transfer sweeps. For the ideal defect free case, no defect-associated V_T-shift would occur and low-to-high and high-to-low voltage sweeps would overlap [1].

On the other hand, the ferroelectric polarization charge gives, if switching, rise to a counterclockwise hysteresis in the same measurement scheme [155]. But due to the defect trapping causing the opposite effect, the memory window of the device cannot be unambiguously determined with these bidirectional CV measurements. As seen in paper II, the memory window can even become non-existent in the measurements if the defect response dominates the ferroelectric response. This, even if a memory window would be observed in devices operated using small bias voltages considerably below the coercive fields, where defect hysteresis is reduced. In most devices, especially transistors, the biasing voltage would be almost constant or at least swept in the same way for both ferroelectric states, i.e., a unidirectional

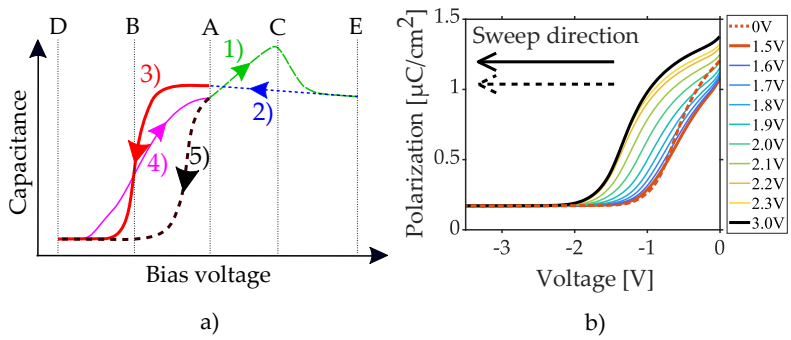


Figure 5.8: a) The bias sweep order of the unidirectional method, in which the memory window of the capacitor is measured as the threshold voltage difference between sweep 3) and 5). b) By varying the maximum voltage E, the threshold voltage of a InAs/HZO/TiN capacitor can be continuously shifted. The difference between the 1.5 V and 3 V lines constitutes the memory window.

measurement. To address this discrepancy, this thesis mainly relies on unidirectional measurements in which the ferroelectric state is first set by a voltage pulse and the measurements are subsequently always performed in the same sweep direction. This is true for both the capacitance measurements in paper IV and in the transistor measurements in paper I, IX, and X.

As illustrated in Fig. 5.8a), the unidirectional CV measurements start from a voltage (A) smaller than the coercive voltages (B and C). As long as the ferroelectric polarization does not switch, the V_T-shifts will be governed by the defect trapping. The V_T-shift caused by the ferroelectric polarization state is measured by two CV sweeps in the same direction (3 and 5). Doing this, V_T will be overestimated for both sweeps due to the negative sweep direction; however, the overestimation will be similar for both polarization states as essentially the same defects will be charged during the two sweeps (see paper II for further discussion). So the actual V_T might be overestimated, but the difference, i.e., the memory window of the device, should be reasonably well estimated. A similar approach investigating perovskite ferroelectrics integrated on silicon has resulted in good agreement between CV and FeFET measurements [156].

In Fig. 5.8b), the measurement scheme in Fig. 5.8a) was used to shift the threshold voltage as a function of the maximum voltage (E). This way, the retention and cycling endurance of the memory window can be investigated for various material integrations without the cumbersome fabrication of transistors. Furthermore, by keeping of the polarization state and thereby ensuring that it never switches, estimations of the relative defect density between samples can be investigated as is done in paper II.

5.2 TRANSISTOR MEASUREMENTS

Polarization and capacitance-voltage measurements serve as the base electrical characterization methods used in more or less all publications on ferroelectricity. It provides considerable input to understanding of the more complex FeFETs, but in the end actual device implementation is necessary to investigate the technology's performance.

5.2.1 PROGRAMMABILITY

The most basic functionality of a FeFET is the reconfigurable threshold voltage, which is achieved by switching the remanent polarization in the ferroelectric gate oxide. The programmability of FeFETs is investigated through a pulsing and measurement sequence as in Fig. 5.9a). The device is first set to the low threshold voltage state by applying a pulse of duration

t_{pulse} and amplitude +V at the gate while keeping source and drain grounded. Typical values have been 250 ns pulses with an amplitude of 4 V for a 13 nm HZO film. The transfer characteristic is then measured, i.e., a DC sweep of I_D-V_G over a smaller voltage range, to determine the threshold voltage. Ideally, this voltage range is well below the coercive voltage of the ferroelectric film. The procedure is repeated for the high threshold voltage state by a $-V$ pulse. As shown in Fig. 5.9b), the result is two transfer characteristics of the FeFET with a considerable threshold voltage difference, i.e., the memory window.

The programmability of the investigated FeFETs follow similar trends as the cycling behavior observed in capacitor structures (section 5.1.2). For the investigated InAs FeFETs, as seen in Fig. 5.9c), there is an initial wake up phase of some hundred cycles during which the threshold voltage states are having a considerable cycle-to-cycle variation. As indicated in Fig. 5.9b), the subthreshold swing of the FeFET deteriorates quickly. Already after the first ferroelectric switching event, the subthreshold swing increases from about 110 mV/dec to several hundred mV/dec. As seen in Fig. 5.9b), it becomes >1000 mV/dec after 300 cycles. This behavior can probably be attributed to the chemical reactions at the HZO/InAs interface investigated in paper XI. The results in paper XI indicate a generation of As^0 at the interface upon ferroelectric switching. As this kind of metallic As defect lies close to the bandgap of InAs, [157] it seems reasonable to believe that its generation may be one of the causes for the deterioration of the subthreshold swing. Interestingly, the deterioration of the InAs/(In)GaAsSb/GaSb TFETs subthreshold swing is similar, but the memory window is continuously shrinking in contrast to the rather stable memory window of the InAs FeFETs in Fig. 5.9c). Performing similar operando HAXPES measurements as in paper XI also on GaSb might provide further insights.

Due to the nucleation-based switching mechanism of ferroelectric HfO_2 described in section 5.1.3, there is a clear trade-off in the required pulse amplitude and pulse length. This trade-off was investigated for single domain switching in paper IX, but the switching dynamics seemingly breakdown around 100 ns pulses which has been attributed to the measurement setup using DC probes and a B1530A waveform generator module (WGFMU) rather than the devices themselves.

5.2.2 RETENTION

Retention is defined as the capability of a memory element to store its data when no external power is supplied. Normally, this is specified as the loss over 10 years at an elevated temperature of 85°C. For ferroelectric devices, the retention loss is mainly changing due to two effects: 1) depolarization fields and 2) charge trapping.

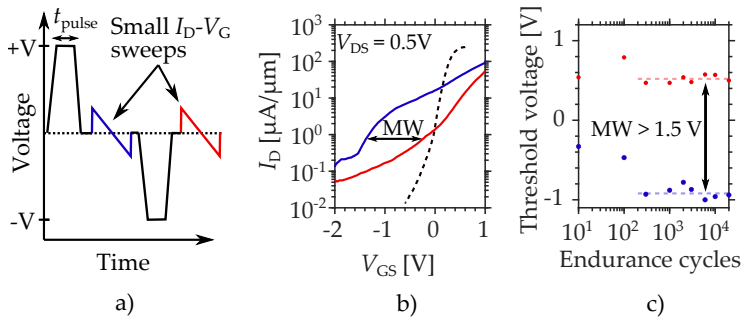


Figure 5.9: a) Measurement sequence for a basic characterization of the memory window of a FeFET. b) The corresponding transfer characteristics of an InAs FeFET after 300 endurance cycles (blue and red). The dotted line is the transistor in the pristine state before any switching. A deterioration of the subthreshold swing is apparent. c) The memory window of the same InAs FeFET becomes relatively stable beyond 300 endurance cycles.

The depolarization field is induced by incomplete charge compensation by the electrodes [76] due to "dead layers" at the interface to the electrodes [158, 159]. Since metals generally can provide enough compensation charge, this effect is generally negligible for MIM-structures unless dielectric layers exist at an interface. For a semiconductor, the charge compensation is less ideal, and thus a depolarization field is created across the oxide of any MOS-structure. This field will always be pointing in the direction that decreases polarization and will therefore lower the thermodynamic barrier for polarization switching [160]. As the coercive field of HfO_2-based ferroelectrics is considerably higher than in perovskites, this gives HfO_2-based ferroelectrics generally good retention characteristics. The polarization switching by NLS is, as seen in eq. (5.2), thermodynamically driven, making polarization switching easier at higher temperature, but also retention worse.

After the initial fast drop in polarization caused by the depolarization field, charge trapping from gate leakage and electron/hole injection from the semiconductor and the electrode tend to dominate retention loss in FeFETs. This does not necessarily mean that the ferroelectric domains depolarize (i.e., this retention loss is less relevant for FeRAM implementations), but the trapped charges diminish the electrostatic effect of the remanent polarization in FeFETs as the traps have the opposite charge [76]. The memory window shrinkage is proportional to the trap concentration, and as the number of traps is normally described as increasing with field cycling, [144] this problem may be expected to worsen by field cycling. Trapping at defect sites may also give rise to imprint, i.e., an asymmetrical electric field which will favor the stability

of one of the two memory states and thus severely deteriorate the retention of the device. A device that is normally written in a certain state may thus start to drift over time and start to behave differently from a device that is normally written in the opposite state.

As could be expected, the retention time of the III-V nanowire integrations in this thesis is generally shorter than corresponding planar MIM devices. In some implementations, >10 years retention is seen, however, it is a property which need future attention.

6

Summary and Outlook

The papers appended to this introduction investigates the prospects of integrating ferroelectric HfO_2 onto III-V nanowires. They cover work ranging from fabricating the first ever ferroelectric HfO_2 film in Lund to the successful circuit implementation of non-volatile reconfigurable signal modulation using ferroelectric TFETs.

The papers can be categorized as either 1) material characterization (paper II, III, IV, V, VI, VII, VIII, and XI) or 2) vertical III-V nanowire integrations (paper I, IX, and X). The papers outline the benefits and issues with the developed technology platform, but most importantly, they indicate that the currently observed limitations are thought to be resolvable by further device engineering.

Early on, it became clear that the thermal sensitivity of III-V nanowires poses the greatest challenge to the technology platform. The wires structurally decompose at annealing temperatures commonly used for ferroelectric HfO_2 (i.e., >600°C) and a considerable part of this thesis has been to develop low thermal budget processing. Zirconium-doped HfO_2 was chosen as the test case ferroelectric material given its low thermal budget, while InAs was chosen as the test case III-V semiconductor both due to its relative thermal sensitivity compared to other III-V materials, but also its technological relevance in high-frequency MOSFETs and low-power TFETs.

Material Characterization

In paper III, a low thermal budget ferroelectric integration on InAs was presented. When developing methods to electrically characterize the defects at this HZO/InAs interface, paper II also clearly indicated that the integration achieves technologically relevant memory windows. To lower the thermal

budget even further, paper VI investigates films that turn ferroelectric already during the ALD deposition. This is promising for avoiding nanowire decomposition, but the relatively low polarization for thin films requires further work. By increasing the Zr concentration in the films, paper VII investigates the integration of antiferroelectric-like films on InAs and shows a promising trade-off between remanent polarization and high-permittivity. As an increased Zr concentration is known to lower the thermal budget, this indicates a promising path forward in regard to III-V integration.

To improve the ferroelectric properties, paper VII explores the impact of the top electrode on HZO/InAs MOSCAPs and shows the importance of achieving a beneficial TiN texturing. However, over time, W proved to be a more suitable top electrode for nanowire processing due to easy pattering using RIE. TiN was thus gradually phased out and has mainly been kept as the bottom electrode in FTJ implementations. After many attempts of using InAs as a bottom electrode in FTJs, this path was abandoned after the realization of how important the metal-to-ferroelectric interface is in paper V. It might be possible to use a III-V material as the bottom electrode in a FTJ, but the relatively poor interface quality is currently thought to be the limiting factor. To understand the chemical reactions occurring at the ferroelectric-semiconductor interface during ferroelectric switching, operando synchrotron measurements were performed in paper XI.

Nanowire Integration

The first vertical nanowire FeFETs were successfully implemented in paper I. Despite being proof-of-concept devices, the transistors had relatively good performance with a stable memory window but were top contact limited by the thermal budget. For the future, the addition of a bottom spacer and a high-quality interlayer between the ferroelectric and the semiconductor is recommended. The development of a gate-last process will also be of outmost importance for mm-wave applications.

With a functioning process flow, the InAs FeFETs were quickly followed by the first ferroelectric TFETs in paper IX and X. The realization that ferro-TFETs can be used as sensitive detectors of single domains in ultra-thin ferroelectric films (paper X) gives the ferroelectric research field new measurement capabilities. For the future, it is highly relevant to continue this path by integrating thinner ferroelectric films to investigate the ultimate scaling limits of ferroelectric devices.

Despite only superficially treated in this introduction, as the focus of the paper is on the circuit level rather than materials integration, paper X indicates the maturity of the developed technology platform. By the introduction of a gate-source overlap, an almost perfectly parabolic concave transfer char-

acteristic is obtained. By the introduction of a ferroelectric gate oxide, the position of the peak position can be shifted as with the threshold voltage in a conventional FeFET. In the paper, this is used to implement a circuit for non-volatile reconfigurable signal modulation. The combined properties of ultra-low operational voltage, ultra-scaled footprint, and multiple functionalities may be attractive to lower the design complexity and power consumption of high-density analogue/mixed signal circuits.

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APPENDICES

A

Fabrication Details

This appendix contains a detailed outline of two important process flows during the work leading up to this thesis. First, the standardized HZO MIMCAP process which is used for benchmarking and tool drift. Second, the vertical FeFET in paper I which was described in section 3.4.1 and forms the fabrication basis for the ferroelectric TFETs in paper IX and X.

A.1 STANDARDIZED MIMCAP

The purpose of this process flow is to regularly test the baseline tools for ferroelectric processing in order to find drift and other issues. The samples are fabricated on highly doped 2-inch silicon-wafers (100) diced into 1 cm^2 pieces.

1. 10 nm TiN sputtering using AJA Orion 5 with rotation 30% (RF power 150 W, 9 sccm Ar flow, ~0.9 nm/min).
2. 1:1 alternation of tetrakis(dimethylamino)hafnium (TDMAHf) and Tetrakis(dimethylamino)zirconium (TDMAZr) for 50 cycles (100 cycles in total) at 200°C in Picosun ALD. Precursor source temperatures at 85°C, pulse times 1.6 s, purge times 5 s, and carrier gas 150 sccm. Water source at RT (normally 25°C), pulse time 0.1 s, purge time 10 s, and carrier gas 150 sccm. Chamber gas flow at 300 sccm, intermediate space 350 sccm, boost 600 sccm with pre empty 0.5 s, master fill 1.2 s, and post empty 0 s. Flush reaction space three times. MFC100 and MFC 200 set as master. Put in test sample at 200°C. Add a piece of silicon wafer without TiN for thickness measurement in step 3.

3. Measure thickness on Si piece using Woollam RC2 variable angle spectroscopic ellipsometer using incident angles 60°, 65°, and 70° and model Si_JAW/NTVE_JAW (2.1 nm)/Savannah HfO2 Tauc-Lorentz by fitting in wavelength range 400-900 nm.
4. 10 nm TiN sputtering using AJA Orion 5 with rotation 30% (RF power 150 W, 9 sccm Ar flow, ~0.9 nm/min).
5. Anneal in RTP-1200-100 in N_2 atmosphere at 150 liter/hour for 30 s at 600°C.
6. Sample dehydration at 150°C for 10 min on hotplate
7. Spin on ma-N 440 resist (45 s, 6000 rpm)
8. Soft bake the resist on a hotplate (95°C, 3 min)
9. Capacitor patterning using Mask-less Aligner Heidelberg MLA150
10. Develop the resist in ma-D 532/S with continuous stirring (105 s)
11. Rinse in deionized water with continuous stirring (60 s) and blow dry with N_2 gun
12. Clean the sample using O_2-plasma ashing in Plasma Preen without cage (30 s, 5 mbar)
13. Evaporate 5/200 nm Ti/Au in Temescal E-Beam evaporator without any tilt and rotation
14. Acetone lift-off
15. TiN etch using $NaOH_4/H_2O_2/H_2O$ (1:2:5) at 60°C for 20 s
16. Rinse in deionized water (30 s) and blow dry with N_2 gun

A.2 VERTICAL FEFET

The samples are fabricated on lightly p-doped 4-inch silicon-wafers (111). A low-resistive 300-nm-thick Sn-doped InAs layer (n^{++}, $\sim 5 \times 10^{19}$ cm^{-3}) is grown using metalorganic vapor phase epitaxy (MOVPE) filling the purpose of a buffer layer for the nanowire growth. The samples are then patterned by EBL and an evaporation lift-off is used to deposit 15 nm thick gold dots. The core diameter of the nanowire depends on the size of the gold seed, which is intentionally changed across the sample to enable a diameter and length variation. The samples are diced into 1×1 cm^2 pieces containing a bit over 2000 individual devices.

The InAs nanowires are grown by Vapor-Liquid-Solid (VLS) growth using MOVPE with trimethylindium (TMIn) and arsine (AsH_3) as the In and As precursor, respectively. The wires are made 500 nm long with the bottom 200-nm non-intentionally doped (nid) while the upper 300 nm drain being n^{++}-doped using triethyltin (TESn) as precursor. During the growth of the highly doped top segment, an approximately 3-nm-thick highly doped shell

overgrows the channel region. The nanowire growth has been performed by Dr. Johannes Svensson or Zhongyunshen Zhu.

- **Removal of the highly doped shell** (etches 1-2 nm per cycle and is repeated until the shell is etched away at the channel).
  1. Oxidize the InAs surface by ozone using UV-Ozone Cleaning system UVOH 150 at an elevated temperature (50°C, 10 min, O_2 flow of 500 sccm)
  2. Etch the InAs-oxide with HCl:IPA 1:10 (30 s)
  3. Rinse in IPA (30 s) and blow dry with N_2 gun
- **Gate stack deposition**
  1. HZO deposition by alternating 1:1 tetrakis(dimethylamino)hafnium (TDMAHf) and Tetrakis(ethylmethylamino)zirconium (TEMAZr) with H_2O as oxidizer for 75 cycles (150 cycles in total) at 200°C using Picosun ALD
  2. 60 nm W sputtered using AJA Orion 5 with rotation (DC power 100 W, 16 sccm Ar flow, ~0.09 nm/s)
- **Gate length definition**
  1. Spin on S1813 resist (60 s, 4000 rpm, 1000 rpm/s)
  2. Hard bake the S1813 on a hotplate (120°C, 15 min)
  3. Thin down S1813 using O-plasma in Trion Sirius T2 Plus RIE using Intellevation LEP400 laser interferometric etch depth monitor for thickness control (~0.66 nm/s, 300 mTorr). Use edge pieces to avoid uneven etching.
  4. Remove the exposed tungsten on top of the nanowire by SF_6/Ar plasma in Trion Sirius T2 Plus RIE (45 s, 45/10 sccm, 140 W, 185 mTorr)
  5. Etch residual Teflon from the SF_6 etch using O-plasma ashing in Plasma Preen without cage (60 s, 5 mbar)
  6. Remove the S1813 with acetone (10 min)
  7. Rinse in IPA (30 s)
- **Gate pad definition**
  1. Spin on S1813 resist (60 s, 4000 rpm, 1000 rpm/s)
  2. Soft bake on a hotplate (115°C, 90 s)
  3. Pattern the resist using Mask aligner MJB4 (6 s, 20 mW/cm^2)
  4. Develop the S1813 in MF319 (80 s)
  5. Rinse in H_2O (80 s)
  6. Hard bake on a hotplate (120°C, 15 min)
  7. Clean the sample using O_2-plasma ashing in Plasma Preen without cage (30 s, 5 mbar)

8. Remove the exposed tungsten by SF_6/Ar plasma in Trion Sirius T2 Plus RIE (45 s, 45/10 sccm, 140 W, 185 mTorr)
9. Etch residual Teflon from the SF_6 etch using O-plasma ashing in Plasma Preen without cage (60 s, 5 mbar)
10. Remove the S1813 with acetone (10 min)
11. Rinse in IPA (30 s)

- **Source via etch**
  1. Spin on S1813 resist (60 s, 4000 rpm, 1000 rpm/s)
  2. Soft bake on a hotplate (115°C, 90 s)
  3. Pattern the resist using Mask aligner MJB4 (6 s, 20 mW/cm^2)
  4. Develop the resist in MF319 (80 s)
  5. Rinse in H_2O (80 s)
  6. Hard bake on a hotplate (120°C, 15 min)
  7. Clean the sample using O_2-plasma ashing in Plasma Preen without cage (30 s, 5 mbar)
  8. Etch the HZO by BOE 1:30 (~0.6 nm/min)
  9. Rinse in deionized water (30 s)
  10. Remove the S1813 with acetone (10 min)
  11. Rinse in IPA (30 s)
- **Etch HZO on top of nanowire**
  1. Spin on S1813 resist (60 s, 4000 rpm, 1000 rpm/s)
  2. Hard bake the resist on a hotplate (120°C, 15 min)
  3. Thin down S1813 using O-plasma in Trion Sirius T2 Plus RIE using Intellevation LEP400 laser interferometric etch depth monitor for thickness control (~0.66 nm/s, 300 mTorr). Use edge pieces to avoid uneven etching.
  4. Etch the HZO by BOE 1:30 (~0.6 nm/min)
  5. Rinse in H_2O (30 s)
  6. Clean the sample in acetone to remove the resist (10 min)
  7. Rinse in IPA (30 s)
- **Annealing in RTP (550°C, 30 s)**
- **Top spacer deposition**
  1. 300 cycles Al_2O_3 using trimethylaluminium (TMA) as precursor and H_2O oxidizer at 200°C in Picosun ALD
- **Top spacer source and gate vias**
  1. Spin on S1813 resist (60 s, 4000 rpm, 1000 rpm/s)
  2. Soft bake on a hotplate (115°C, 90 s)
  3. Pattern the resist using Mask aligner MJB4 (6 s, 20 mW/cm^2)
  4. Develop the resist in MF319 (80 s)

5. Rinse in H_2O (80 s)
6. Hard bake on a hotplate (120°C, 15 min)
7. Clean the sample using O_2-plasma ashing in Plasma Preen without cage (30 s, 5 mbar)
8. Etch the Al_2O_3 by BOE 1:30 (~0.3 nm/s)
9. Rinse in deionized water (30 s)
10. Remove the S1813 with acetone (10 min)
11. Rinse in IPA (30 s)

- **Top spacer top etch** (to expose drain contact)
  1. Spin on S1813 resist (60 s, 4000 rpm, 1000 rpm/s)
  2. Hard bake on a hotplate (120°C, 15 min)
  3. Thin down S1813 using O-plasma in Trion Sirius T2 Plus RIE using Intellevation LEP400 laser interferometric etch depth monitor for thickness control (~0.66 nm/s, 300 mTorr). Use edge pieces to avoid uneven etching.
  4. Etch the Al_2O_3 by BOE 1:30 (~0.3 nm/s)
  5. Rinse in deionized water (30 s)
  6. Clean the sample in acetone to remove the resist (10 min)
  7. Rinse in IPA (30 s)
- **Top metal definition**
  1. Etch with HCl:IPA 1:10 (30 s) to remove InAs oxide on top of the nanowire to improve the metal-semiconductor contact
  2. Metal sputtering of Ni/Au, thickness 10/200 nm using AJA Orion 5 with rotation
  3. Spin on S1813 resist (60 s, 4000 rpm, 1000 rpm/s)
  4. Soft bake on a hotplate (115°C, 90 s)
  5. Pattern the S1813 using Mask aligner MJB4 (6 s, 20 mW/cm^2)
  6. Develop the S1813 in MF319 (80 s)
  7. Rinse in deionized water (80 s)
  8. Hard bake on a hotplate (120°C, 15 min)
  9. Clean the sample using O_2-plasma ashing in Plasma Preen without cage (30 s, 5 mbar)
  10. Etch Au using 1:2:17 KI:I_2:H_2O (35 s)
  11. Rinse in deionized water (30 s)
  12. Clean the sample in acetone to remove the resist (10 min)
  13. Rinse in IPA (30 s)
  14. Etch Ni using 2.5:2.5:1:15 CH_3COOH:HNO_3:H_2SO_4:H_2O (100 s)
  15. Rinse in deionized water (30 s)