Vertical III-V Nanowire Transistors for Low-Power Electronics

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Vertical III-V Nanowire Transistors for Low-Power Electronics

Doctoral Thesis

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Abstract

Power dissipation has been the major challenge in the downscaling of transistor technology. Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) have struggled to keep a low power consumption while still maintaining a high performance due to the low carrier mobilities of Si but also due to their inherent minimum inverse subthreshold slope ($S \geq$ 60 mV/dec) which is limited by thermionic emission.

This thesis work studied the capabilities and limitations of III-V based vertical nanowire n-type Tunneling Field-Effect Transistor (TFET) and p-type MOSFET (PMOS). InAs/InGaAsSb/GaSb heterojunction was employed in the whole study. The main focus was to understand the influence of the device fabrication processes and the structural factors of the nanowires such as band alignment, composition and doping on the electrical performance of the TFET. Optimizations of the device processes including spacer technology improvement, Equivalent Oxide Thickness (EOT) downscaling, and gate underlap/overlap were explored utilizing structural characterizations.

Systematic fine tuning of the band alignment of the tunnel junction resulted in achieving the best performing sub-40 mV/dec TFETs with S = 32 mV/dec and I_{ON} = 4 $\mu A/\mu m$ for I_{OFF} = 1 nA/μm at V_{DS} = 0.3 V. The suitability of employing TFET for electronic applications at cryogenic temperatures has been explored utilizing experimental device data. The impact of the choice of heterostructure and dopant incorporation were investigated to identify the optimum operating temperature and voltage in different temperature regimes. A novel gate last process self-aligning the gate and drain contacts to the intrinsic and doped segments, respectively was developed for vertical

InGaAsSb-GaAsSb core-shell nanowire transistors leading to the first sub-100 mV/dec PMOS with S = 75 mV/dec, significant $I_{ON}/\ I_{OFF} = 10^4$ and I_{MIN} < 1 nA/μm at V_{DS} = -0.5 V.

Popular Science Summary

Why do the mobile phones today have a bad battery life? Are we just polishing up the old school transistors to quench the thirst of today's technology? This thesis work focused towards developing unconventional low power transistors to make our future gadgets much better.

A fine day can get easily ruined when you get stranded on a street - trying to make an important call, use google maps to get to somewhere or pay digitally at a store - and your mobile phone gets switched off! Such a problem might have been unimaginable 40 years ago. But today life has become easier and more comfortable with a smartphone to the extent that without it, life seems impossible. In 1973, Motorola made the first mobile phone and Martin Cooper made the first call from AT&T Bell Labs at New York. Since then, the development in the mobile phone technology has been remarkable. They have come a long way from heavy brick sized ones that needed to be kept inside cars to the tiny ones today that can be carried around in a pant-pocket. The functionalities that they provide though has kept expanding with cameras and processors integrated on the handsets to take, process and store pictures and technologies that could offer internet services. In addition to the smartphones, the assortment of portable devices we use today has grown tremendously ranging from wearable health watches to fully connected smart homes and cars. Each generation of the smart devices developed, have greatly eased the way we live our lives. However, efficient consumption of energy to provide long battery lives without compromising the performance have always been a challenge for the electronic industry.

Have you ever thought how we could keep expanding the features on such small devices? We shrank the transistors and increased their number to improve performance. But this scaling has not come for free. The leakage current from each transistor kept increasing and has reached a point today where the devices are power hungry, getting heated up and eating away the battery charge very quickly. The power problem would continue to limit the capabilities of the new era of smart internet connected electronic devices and in a fast-growing technology dependent world this cannot be overseen.

In this thesis work, we attempt to tackle these issues by developing transistors with binary materials (III-V) including elements from group 3 and 5 of the periodic table that can offer higher performance at lower supply voltages as compared to conventionally used silicon. A new type of transistor called the Tunnel Field-Effect transistor has been studied in this thesis. The transistors have been fabricated using III-V materials and operate at voltages five times lower than today's mobile phone circuits which would mean 25 times decrease in mobile phone power consumption. Moreover, we have attempted a step forward in the scaling process by implementing this technique on nanowires that are just 10nm wide and 400nm long. The studied technology has great potential to be integrated on the current silicon fabrication schemes and could ease the development of future big technologies such as brain-like computing and Internet-of-Things (IoT).

Acknowledgments

This journey of doctoral studies has been an enjoyable and a great learning experience not only from a research perspective but also in my personal growth for which I wish to express my gratitude to many people. First of all, I would like to thank my supervisor Lars-Erik for believing in me and providing me this opportunity. You have inspired me in many ways, not just technical but beyond that, and I will carry these values through the rest of my life. Johannes, you have been a dependable mentor answering my endless questions with great patience and having my best interest always at heart for which I am forever grateful. Erik, thanks for having your doors always open for a discussion. Your deep insights and great advices have helped me understand science better.

My start to this project would not have been easy without the knowledge transfer from my predecessors Elvedin and Markus. I have admired your laboratory manners and the organized work which I have tried to follow as much as I could during my studies. Zhongyunshen, I have always learnt something new from our discussions and thanks for all your simulation and modelling insights. Heera, you have been a good and trustable friend during my difficult times and I hope these years were just the beginning of our friendship. My working days as a PhD had been joyful due to friendly conversations with Adam, Stefan, Olli-Pekka, Lasse, Saketh, Karl-Magnus, Marcus, Hannes, Ben, Philip, Anette and Fredrik. I have always looked forward to our lunches and coffee breaks to learn more about scientific as well as non-scientific matters. I would like to thank all colleaugues in our group for providing a great working atmosphere and sharing your valuable opinions when needed - Gautham, Lars, Mattias, Anton, Andre, Robin, Navya, Patrik, Louise, Daniel, Mats, Niklas, Ngoc, Alexandros and Johan. Thanks to personnel at the department administration - Pia, Stefan, Linda,

Erik Jonsson, Erik Gothe, Elisabeth Nordstrom and Elisabeth Ohlsson for your help in administrative and technical support. Considering the dependency of the project on laboratory work, the achievements during this thesis would not have been possible without help from the technicians and engineers at the Lund Nano Lab. Thanks to George, Dmitry, Sarah, Alex, Elvedin, Anders, Natalia, Peter and Mariusz for your constant support during difficulties in the lab.

Out of some great friendships in Lund developed during my PhD that have made my life outside of work enjoyable, I wish to express my special thanks to my good old best friend Sudhakar. You have been a great support helping me through several major decisions during these last five years and I am truly thankful for your kindness. Lastly but most importantly, I would like to thank my parents, my husband Adhi and daughter Venba for your unconditional love. Appa and Amma, thanks for fighting your fears and trusting my decision to move to a distant land far beyond your reach. Adhi, you inspire me everyday with your great positivity and energy and constantly remind me that I am capable of achieving more. Venba, you have changed my perspective of life, work and world and I have much more to learn from you.

Lund, April 2023

Contents

Preface

This thesis is the culmination of more than five years of work in the *Nanoelectronics* group at Lund University and presents detailed studies of vertical nanowire III-V TFET and MOSFET suitable for low-power applications. The work has been performed under the supervision of Doctor *Johannes Svensson*, Professor *Lars-Erik Wernersson* and Professor *Erik Lind*.

STRUCTURE OF THE THESIS

The thesis is divided into three main parts: Introduction, Appendices and Papers. The thesis is a compilation of the articles appended at the back with the introduction acting as a discussion of the devlopments within the research field and providing an outline of the fundamental concepts on which the papers are built upon. The introduction together with the appendices is aimed to help future doctoral students to deepen their understanding and ease the developments of the device fabrication without difficulty.

- **INTRODUCTION**
  The introduction firstly motivates the thesis work presenting its necessity and application. Fundamental principles behind device operation are discussed along with a survey of the relevant literature both from academia and industry. The device fabrication process developments performed during this thesis resulting in the publications are discussed. The influence of different process schemes and the critical factors deciding the device performance are highlighted. Finally, the performance improvements achieved and the knowledge obtained of the device operation over the five years of this thesis work are presented with an outlook on future optimization strategies.

- **APPENDICES**

  A Fabrication of Vertical Nanowire Field-Effect Transistors
  Appendix A details the process steps involved in the fabrication of vertical nanowire FETs.

  B Fabrication of Core-Shell Vertical Nanowire Field-Effect Transistors
  Appendix B details the additional process steps than those in Appendix A that are involved in the fabrication of FETs from core-shell nanowires.

- **PAPERS**
  The papers forming the main body of the thesis are reproduced in the back and listed in the following.

INCLUDED PAPERS

The following papers form the main body of this thesis and the respective published or draft versions are appended in the back.

Paper I: A. Krishnaraja, J. Svensson, E. Lind, and L.-E. Wernersson, "Reducing ambipolar off-state leakage currents in III-V vertical nanowire tunnel FETs using gate-drain underlap", *Applied Physics Letters*, vol. 115, no. 14, 2019, doi: 10.1063/1.5115296.

▶ *I developed the process for gate-drain underlap, fabricated, and measured the devices, analyzed the data as well as wrote the paper.*

Paper II: A. Krishnaraja, J. Svensson, E. Memišević, A.R. Persson, E. Lind, L.R. Wallenberg, and L.-E. Wernersson, "Tuning of Source Material for InAs/InGaAsSb/GaSb Application-Specific Vertical Nanowire Tunnel FETs", *ACS Applied Electronic Materials*, vol. 2, no. 9, pp. 2882-2887, Sep 2020, doi: 10.1021/acsaelm.0c00521.

▶ *I developed the process, fabricated, and measured most of the devices, analyzed the data as well as wrote the paper.*

Paper III: A. Krishnaraja, J. Svensson, and L.-E. Wernersson, "Vertical InAs/InGaAsSb/GaSb Nanowire Tunnel FETs on Si with Drain Field-Plate and EOT = 1 nm Achieving S_{MIN} = 32 mV/dec and $g_{\mathrm{m}}/I_{\mathrm{D}}$ = 100 V^{-1}", *IEEE Silicon Nanoelectronics Workshop*, pp. 17-18, 2020, doi: 10.1109/SNW50361.2020.9131656.

▶ *I developed the process, fabricated, and measured the devices, analyzed the data as well as wrote the paper.*

Paper IV: A. Krishnaraja, J. Svensson, Z. Zhu, and L.-E. Wernersson, "III-V Tunnel Field-Effect Transistor operation at different temperature regimes", *Under Review in Applied Physics Letters*.

► *I fabricated and measured most of the devices, analyzed the data as well as wrote the paper.*

Paper V: A. Krishnaraja, Z. Zhu, J. Svensson, and L.-E. Wernersson, "Low-power, Self-aligned Vertical InGaAsSb NW PMOS with S<100 mV/dec", *Under Review in IEEE Electron Devices Letters*.

► *I developed the process for core-shell gate-last device process, fabricated and measured the devices, analyzed the data as well as wrote the paper.*

Paper VI: M. Hellenbrand, E. Memišević, J. Svensson, A. Krishnaraja, E. Lind, and L.-E. Wernersson, "Capacitance Measurements in Vertical III-V Nanowire TFETs", *IEEE Electron Devices Letters*, vol. 39, no. 7, pp. 943-946, July 2018, doi: 10.1109/LED.2018.2833168.

► *I assisted in fabricating the RF compatible devices and performed DC measurements.*

Paper VII: D. Dzhigaev, J. Svensson, A. Krishnaraja, Z. Zhu, Z. Ren, Y. Liu, S. Kalbfleisch, A. Bjorling, F. Lenrick, Z.I. Balogh, S. Hammarberg, J. Wallentin, R. Timm, L.-E. Wernersson, and A. Mikkelsen, "Strain mapping inside an individual processed vertical nanowire transistor using scanning X-ray nanodiffraction", *Nanoscale*, vol. 12, pp. 14487-14493, 2020 doi: 10.1039/d0nr02260h.

► *I fabricated the devices and assisted in the preparation of lamella.*

RELATED WORK

The following publications are not included in the thesis, but summarise related work that I was involved in.

Paper viii: M. Hellenbrand, E. Memišević, J. Svensson, A. Krishnaraja, E. Lind, and L.-E. Wernersson, "Effect of Gate Oxide Defects on Tunnel Transistor RF Performance", *76th Device Research Conference*, pp. 137-138, Jun. 2018, doi: 10.1109/DRC.2018.8442145.

Paper ix: A. Krishnaraja, E. Memišević, M. Hellenbrand, J. Svensson, E. Lind, and L.-E. Wernersson, "Fabrication of Tunnel Field-Effect Transistors", *Swedish Microwave Days*, May. 2018.

Paper x: M. Hellenbrand, E. Memišević, J. Svensson, A. Krishnaraja, E. Lind, and L.-E. Wernersson, "RF Characterisation of Vertical III-V Nanowire Tunnel FETs", *Swedish Microwave Days*, May. 2018.

Paper xi: A. Krishnaraja, J. Svensson, E. Lind, and L.-E. Wernersson, "Fabrication of Tunnel FETs demonstrating sub-thermal subthreshold slope", *21st International Vacuum Congress*, July. 2019.

Acronyms and Symbols

Here, important acronyms, abbreviations, and symbols are listed, which are recurring throughout the thesis. Some parameters, which only occur in a narrow context, are intentionally omitted; some parameters are used in more than one way, but the context is always explicitly clarified in the corresponding text. Some (compound) units are provided with prefixes to reflect the most commonly encountered notations in the literature.

ACRONYMS AND ABBREVIATIONS

Al_2O_3	Aluminum oxide
ALD	Atomic Layer Deposition
Ar	Argon
As	Arsenic
AsH_3	Arsine
Au	Gold
BOE	Buffered Oxide Etch
BTBT	Band-To-Band Tunneling
C_4F_8	Octafluorocyclobutane
CH_3COOH	Acetic acid
CMOS	Complementary Metal-Oxide-Semiconductor

DeZn	Diethylzinc
DIBL	Drain Induced Barrier Lowering
DOS	Density Of States
EBL	Electron Beam Lithography
EOT	Equivalent Oxide Thickness
FET	Field-Effect Transistor
Ga	Gallium
GAA	Gate-All-Around
GaAs	Gallium arsenide
GaSb	Gallium antimonide
Ge	Germanium
H	Hydrogen
H_2O	Water
H_2SO_4	Sulphuric acid
H_3PO_4	Phosphoric acid
HCl	Hydrochloric acid
Hf	Hafnium
HfO_2	Hafnium dioxide
HNO_3	Nitric acid
ICT	Information and Communication Technology
In	Indium
InAs	Indium Arsenide
InGaAs	Indium Gallium Arsenide
InGaAsSb	Indium Gallium Arsenide Antimonide
InP	Indium Phosphide

IoMT	Internet-of-Medical Things
IoT	Internet-of-Things
IPA	Isopropyl alcohol (2-propanol)
Mo	Molybdenum
MoS_2	Molybdenum disulphide
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MOVPE	Metal-Organic-Vapour-Phase-Epitaxy
N_2	Nitrogen
NaOH	Sodium hydroxide
NDR	Negative Differential Resistance
Ni	Nickel
O_2	Oxygen
O_3	Ozone
PVCR	Peak-to-Valley Current Ratio
RIE	Reactive Ion Etching
Sb	Antimony
SEM	Scanning Electron Microscopy
SF_6	Sulfur hexafluoride
SiGe	Silicon Germanium
SiO	Silicon monoxide
SiO_2	Silicon dioxide
SiO_x	Silicon oxide
Sn	Tin
TASE	Template Assisted Selective Epitaxy
TAT	Trap Assisted Tunneling
TDMAHf	tetrakis(dimethylamido)hafnium(IV)

TEM	Transmission Electron Microscopy
TESn	Tetraethyltin
TFET	Tunnel Field-Effect Transistor
Ti	Titanium
TiN	Titanium Nitride
TMA	Trimethylaluminum
TMAH	Tetramethylammonium hydroxide
TMD	Transition metal dichalcogenides
TMGa	Trimethylgallium
TMIn	Trimethylindium
TMSb	Trimethylantimony
ULP	Ultra Low Power
UV	UltraViolet
UVL	UltraViolet Lithography
VLS	Vapor Liquid Solid
W	Tungsten
WKB	Wentzel-Kramers-Brillouin
WZ	Wurtzite
ZB	Zincblende
Zn	Zinc
ZrO_2	Zirconium dioxide

LATIN SYMBOLS

C_s	F	Semiconductor Capacitance
C_{ins}	F	Insulator Capacitance

E_F	eV	Fermi Level Energy
E_g	eV	Band Gap
$E_{c,c}$	eV	Channel conduction band
$E_{v,s}$	eV	Source valence band
$E_{F,s}$	eV	Source Fermi level
f	Hz	Frequency
g_m	S	Transconductance
g_d	S	Output conductance
I_{ON}	A	ON Current
I_{OFF}	A	OFF Current
I_{MIN}	A	Minimum Current
I_D	A	Drain Current
I_{DS}	A	Drain-to-Source Current
I_{SD}	A	Source-to-Drain Current
I_G	A	Gate Current
I_{GS}	A	Gate-to-Source Current
I_S	A	Source Current
k_B		$\approx 1.381 \times 10^{-23}$ kg m^2 K^{-1} s^{-1}, Boltzmann Constant
L_G	m	Gate Length
m_0		$\approx 9.109 \times 10^{-31}$ kg, Electron Rest Mass
m^*	m_0	Effective Mass
q		$\approx 1.602 \times 10^{-19}$ C, Elemental Charge
R_{on}	Ω	ON resistance
S	mV/dec	Subthreshold swing
S_{MIN}	mV/dec	Minimum subthreshold swing

S_{lin}	mV/dec	Minimum linear subthreshold swing
S_{sat}	mV/dec	Minimum saturation subthreshold swing
T	K	Temperature
V_{DS}	V	Drain-to-Source Voltage
V_{DD}	V	Supply Voltage
V_{SD}	V	Source-to-Drain Voltage
V_{GD}	V	Gate-to-Drain Voltage
V_{G}	V	Gate Voltage
V_{GS}	V	Gate-to-Source Voltage
V_{T}	V	Threshold Voltage
x		Generic Latin Symbol

GREEK SYMBOLS

α	eV^{-1}	Non-Parabolicity Factor
κ		Dennard Scaling Factor, Relative Permittivity
ϕ		Generic Greek Symbol

FUNCTIONS AND OPERATORS

$\ln(\cdot)$	Natural logarithm
$\log(\cdot)$	logarithm to the base 10
$\sin(\cdot)$	sine

INTRODUCTION

1

Motivation

1.1 THE POWER STRUGGLE

Information and Communication Technology (ICT), which refers to technologies used to transmit, receive, store, create, share, and exchange information, has seen an unprecedented growth in the last two decades. This has led to an explosive growth in the global market for ICT devices such as PCs, laptops, smartphones, and tablets especially after the beginning of the internet era. While the total power consumption of the stationary PCs had been increasing by 10x every decade, the portable devices' energy consumption had increased by 10^4 [1]. The alarming trend if continued without action would, by 2040, result in portable devices consuming power equivalent to that of supercomputers. From a global electricity usage perspective, the ICT share currently is 6-9% and is predicted to double in the next decade [2]. The energy consumption of ICT is usually analyzed by using four categories: consumer electronics, datacenters, network infrastructure and manufacturing of the above categories. Consumer electronic devices were the major energy consumers in the early 2000s. With development in digital media and internet, cloud storage and online information sharing increased drastically which led to heavy usage of datacenters increasing their share of energy usage. Recent advances in the Internet-of-Things (IoT) concept would wirelessly connect several ICT devices to each other and to datacenters and networking services taking a major share of ICT electricity usage in the coming decade [3]. Such a system requires the devices to be on standby all the time to allow prompt communication with each other. Transistors, which are the fundamental building

block of most electronic devices, dissipate power not only during active circuit operation (dynamic power) but also when a supply voltage is applied but no new input given to the circuit due to leakage currents (static power). With the developments in the transistor technology over the years achieved through transistor scaling, the leakage power has increased exponentially accounting to nearly 70% of the total power dissipated by the transistors [4]. Though improvements in the transistor architecture has helped alleviate this issue, the future of ICT poses strict constraints on the static power consumption of the transistors requiring novel technology developments.

1.2 EVOLUTION OF TRANSISTORS

The first transistor developed in 1947 by Bell Laboratories was nearly 4000 times larger than today's 10nm node transistor [5]. Gordon Moore, the co-founder of Intel, observed in 1965 that integrating larger and larger circuit functions on a single substrate by increasing area efficiency and reducing the cost per component were key to the growth of the IC industry. In this

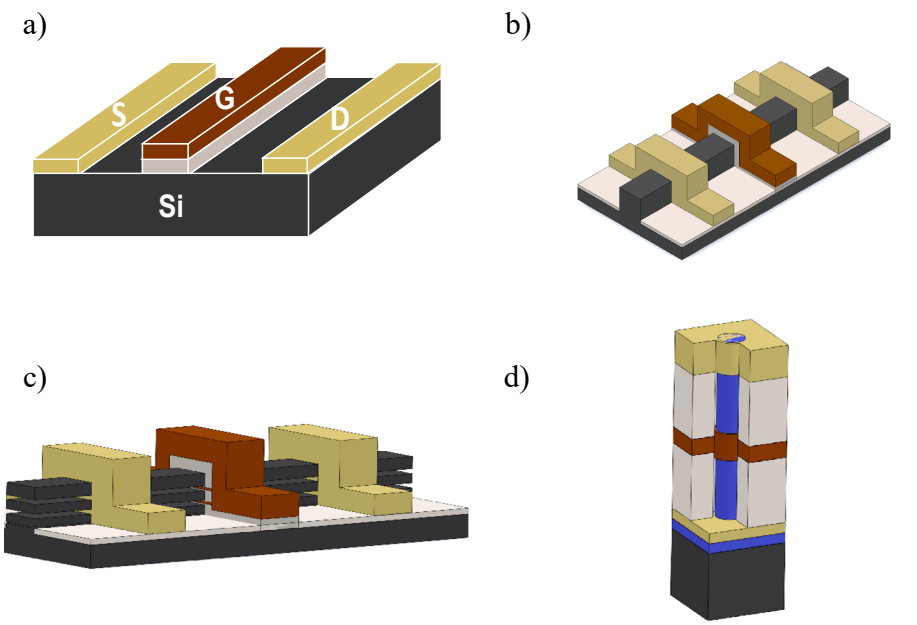

Figure 1.1: Transistor technology evolution (a) Planar FET (b) FinFET (c) Stacked Nanosheet/Nanoribbon FET (d) Vertical Nanowire FET.

regard, Moore's law came into practice which states that the transistor density per chip doubles every 18-24 months. To keep up with Moore's predictions, Dennard formulated the transistor scaling rules in 1974 which states that all dimensions and supply voltage of the transistor device must be scaled by the same factor to improve the transistor performance while maintaining constant power density. Reducing the area of the transistor reduces the necessary drive voltage and the capacitance thereby allowing circuits to operate at higher frequencies at the same power. However, Dennard scaling failed to account for the increasing leakage currents with downscaling and the semiconductor industry hit a power wall saturating the supply voltage at 0.7-0.5 V. The power wall problem was overcome by introducing parallel computing using multicore processors. Amidst the power constraint era, the transistor scaling has continued owing to the introduction of new materials such as strained Si, high-k gate oxide and metal gate and new process development schemes such as self-aligned multi-patterning lithography techniques.

A great leap forward happened at the 22nm node when planar Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) device architecture was replaced by FinFET with tri-gate (Fig 1.1) to reduce leakage currents and improve gate control [6]. The FinFET has proven to deliver the intended performance per watt up until the 3 nm node. New device architecture consisting of 3D stacked nanosheets/ribbons with gate-all-around configuration have been demonstrated to serve beyond the 3 nm node [7, 8]. A transition from horizontal to vertical transport has also been suggested to reduce device footprint. Such vertical devices has recently been demonstrated by IBM using vertical nanosheets [9]. In line with the roadmap for future technology developments, this thesis work studies the vertical nanowire gate-all-around transistors [10].

1.3 III-V SEMICONDUCTORS

Silicon has dominated the semiconductor industry for several decades now. With the constraints limiting the scaling of the current transistor technology, it is necessary to look beyond Si and materials such as III-V compounds have demonstrated to be an attractive alternative [11]. III-V materials have lower effective mass and higher carrier mobility than Si which refers to how easily the charge carriers can flow through the transistor. InAs exhibits 30 times higher electron mobility than Si while GaSb exhibits 2 times higher hole mobility as listed in Table 1.1 and could thus be used as n-type and p-type alternatives to Si in Complementary MOS (CMOS).

In the electronics industry, the III-V High Electron Mobility Transistor (HEMT) has been commercialized for high-frequency applications for several

Table 1.1: Comparison of carrier mobility of Si with potential III-V compounds for electronics applications. The stated mobilities are for bulk crystals [12].

Materials	Electron mobility ($cm^2V^{-1}s^{-1}$)	Hole mobility ($cm^2V^{-1}s^{-1}$)
Si	1.4*10^3	4.5*10^2
InAs	4*10^4	5*10^2
$In_{0.53}Ga_{0.47}As$	12*10^3	3*10^2
GaSb	3*10^3	1*10^3
InSb	7.7*10^4	8*10^2

years now. For low-power applications, III-V CMOS are better suited due to their oxide barrier providing relatively lower leakage currents than HEMT. However, III-V CMOS has been lagging in performance due to their poor oxide interface and lack of good III-V p-type MOSFET (PMOS). The native oxide of Si gives a high-quality semiconductor-oxide interface which in turn provides good electrostatic control of the transistor device. The III-V materials on the other hand form poor native oxides and dangling bonds that act as defect centers and lead to Fermi level pinning which prevents effective electrostatic control. The high-k gate oxide alleviates this issue somewhat, but the material still requires development to reach the quality of a Si-oxide interface [11].

1.4 NEED FOR STEEP SLOPE DEVICES

Although the transistor density has increased 100x between the 45nm and 14nm nodes, the performance and power improvements have only been 2x and 0.25x respectively [13]. This discrepancy is mainly due to the power-performance counterbalancing problem. Both the static power and dynamic power consumption can be reduced by supply voltage V_{DD} scaling. However, the same overdrive voltage (V_{DD} - V_T) is required to deliver the required on-current (I_{ON}) and hence a simultaneous reduction in threshold voltage V_T is needed. Unfortunately, such a downscaling increases the off-state current (I_{OFF}) as shown in Fig 1.2(a) leading to increased static leakage power which is unfavorable especially for today's growing smart phones and portable devices that rely on limited cooling and battery resources.

This trade-off between the on- and off- state in MOSFET arises from its inherent charge transport mechanism, thermionic emission. The subthreshold swing S, which is defined as the gate voltage change required to increase the current by one order of magnitude, is given by

$$S = \frac{\partial V_{GS}}{\partial \log(I_{DS})} = \frac{\partial V_{GS}}{\partial \psi_s} \frac{\partial \psi_s}{\partial \log(I_{DS})} = m \times n = \left(1 + \frac{C_s}{C_{ins}}\right) \frac{k_B T}{q} \ln(10), \quad (1.1)$$

where V_{GS} is the gate voltage, ψ_s is the surface potential, I_{DS} the drain current, C_s the semiconductor capacitance and C_{ins} the insulator capacitance. At room temperature (300 K),kT = 25 meV gives a minimum limit of S = 60 mV/dec in MOSFETs due to their temperature dependence. The "m" factor in equation 1.1 describes how efficiently the gate voltage modulates the surface potential and the "n" factor describes how the drain current changes as the surface potential is modulated. The power constraint in the current technology platform requires the state-of-the-art low power MOSFETs to have S as close to 60 mV/dec as possible as explored with PMOS in this thesis.

To overcome this bottleneck and have reduced leakage with physical scaling of the transistors, a steep slope device demonstrating S < 60 mV/dec is required. This can be achieved by enhancing the translation of gate bias to the surface potential thereby reducing the body factor m in equation 1.1

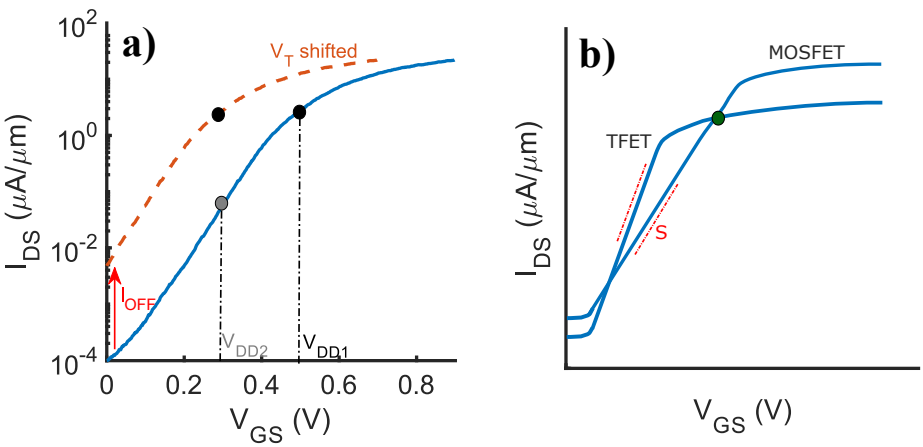

Figure 1.2: (a)Schematic transfer curve illustrating the power challenge in a MOSFET. Reducing V_{DD} from V_{DD1} to V_{DD2} reduces the I_{ON} as shown by the gray dot and hence V_T shift (red dotted line) is required to maintain I_{ON}. However this results in an increased I_{OFF}. (b) Comparison of TFET and MOSFET switching characteristics. The green dot denotes the transition point below which TFETs are advantageous compared to MOSFETs.

as in negative capacitance FET, Metal Insulator Transition FET and Electro-Mechanical FET [14]. The sub-60 mV/dec switching can also be achieved by reducing the factor n in equation 1.1 by changing the conduction mechanism of the device as in Tunnel Field-Effect Transistor (TFET) that are explored in this thesis. The TFET, due to its steep switching capabilities as seen in Fig 1.2(b), offers improved performance compared to the MOSFET for the same operating voltage or reduced leakage for the same performance [15]. Such an operation is especially suitable for applications that require low standby power as discussed in section 1.1. At operating power supply voltages beyond the green transition point in Fig 1.2(b), the MOSFET offers higher I_{ON} and is hence suitable for high performance applications.

1.5 THESIS CONTRIBUTION

The primary motive of this thesis is to explore the potential of III-V PMOS and III-V n-type TFET to replace Si CMOS for low power applications. The analysis is performed by designing, fabricating, and characterizing transistors using vertical InAs/InGaAsSb/GaSb heterostructure nanowires. Thus, this work aims to address the device scaling requirements and power dissipation problems of the current semiconductor technology.

Paper I discusses the drawback of using the gate-drain underlap device structure to suppress ambipolar off-state leakage currents in a TFET.

Paper II presents a systematic study of the influence of the band lineup at the tunnel junction on the performance a TFET device.

Paper III is the outcome of the investigation performed in Paper II togther with optimizations in device design to suppress leakage paths resulting in sub-40 mV/dec TFET with the highest drive currents reported.

Paper IV attempts to identify the optimum operating voltage and temperature for a TFET and provides a thorough analysis of the operating principle of the device in different bias conditions and temperature regimes.

Paper V presents the sub-100 mV/dec switching capabilities of an InGaAsSb channel for a PMOS device.

Paper VI studies the intrinsic capacitances in a vertical nanowire TFET and identifies the device design changes that are required to improve the RF performance.

Paper VII presents the measurement of the strain of the wrap gate on an individual vertical nanowire structure.

1.6 THESIS OUTLINE

The introduction chapters provide a broader overview of the studies presented above towards the goal of further understanding the papers.

Chapter 2 provides a background of the critical electrical parameters for analysis of a FET. The fundamentals of TFET, the steep slope low supply voltage alternative to MOSFET, are also discussed describing the physics and the unique electrical characteristics of these devices. An overview of the research efforts in the field of III-V n-type TFET and PMOS is also presented.

Chapter 3 describes the design and fabrication of III-V vertical FET. The process schemes developed during this thesis targeting specifically to reduce leakage currents is explained in detail. The critical factors governing each process step in the fabrication flow are also highlighted. The device fabrication of a hybrid PMOS-TFET on a single vertical nanowire is described.

Chapter 4 focuses on the device characterization techniques adopted to understand the physical limitations of the transistors. The role of defects in the structure and their contribution to the device performance is examined. The benefits of electrical characterization in different temperature regimes are presented. Finally, the performance of the different generations of transistors developed during this thesis are compared and benchmarked against other III-V devices in the field.

Chapter 5 summarizes the contribution of this thesis work to the research field and provides an outlook of the future device optimizations required to improve the performance.

2

Background

This chapter will give an overview of the important concepts to understand the fundamental physics of the devices studied in this thesis work. The electrical characterization techniques used to get insights into the performance and the structural quality of the materials are also discussed. A brief review of the research efforts reported in literature in the field of III-V TFETs and III-V PMOS is presented to provide a background to the devices developed within this thesis work.

2.1 TUNNEL FIELD EFFECT TRANSISTORS

A conventional MOSFET transistor consists of a potential barrier as illustrated in Fig 2.1(a) and the charge transport over the barrier is based on thermionic emission. The high-energy carriers in the Fermi tail govern the transport and influence the device on-off switching limiting the subthreshold swing as discussed in section 1.4. Hence if the participation of the exponential tail of the Fermi distribution in the conduction process is cut off, the leakage of these high-energy charge carriers in the off- state can be prevented.

The tunnel diode and the TFET derived from it circumvent this problem by operation based on inter-band tunneling mechanism as illustrated in Fig 2.1(b) unlike the thermionic emission process in MOSFET. In 1958, Esaki invented a narrow junction diode that conducts more in the reverse direction than in the forward direction which was later named the tunnel diode [16]. A TFET consists of a p-i-n junction with p-source, intrinsic channel, and n-drain. In the on- state, when the band alignment is in favor of tunneling, the electrons tunnel from the valence band of the p+ source to the conduction band of the n- channel and the carrier transport is governed by the width of the tunnel

junction. This way, the exponential tail of the Fermi distribution is filtered by the bandgap like in a band pass filter resulting in electrons with lower energy participating in the conduction process. Such a filtering reduces the leakage currents and significantly improves the OFF-state performance of a TFET compared to MOSFET assisting in steep switching.

The transmission probability of carriers through the tunnel barrier can be calculated using the Wentzel-Kramer-Brillouin approximation [17],

$$T_{WKB} = exp\left(-\frac{4\lambda\sqrt{2m^*\sqrt{E_g{}^3}}}{3qh(E_g + \Delta\Phi)}\right) \tag{2.1}$$

where λ is the screening tunneling length, m^* effective mass, E_g bandgap, and $\Delta\Phi$ is the energy window for tunneling. Just as how the gate bias V_{GS} controls the Fermi energy for transport in MOSFET, V_{GS} in a TFET controls $\Delta\Phi$ and only the carriers within $\Delta\Phi$ can tunnel into the channel. A positive drain bias V_{DS} reverse biases the p-i-n junction for TFET operation. A channel material with small m^* and E_g will improve the tunneling probability as seen in equation 2.1 and thereby increase the on-current (I_{ON}). The tunneling current in a 1D single subband nanowire can be calculated using Landauer-Buttiker formalism as stated in equation 2.2 [18].

$$I_{ON} = \frac{2q}{h}\int_{E_{v,s}}^{E_{c,c}} T(E)f(E, E_{F,s})dE \tag{2.2}$$

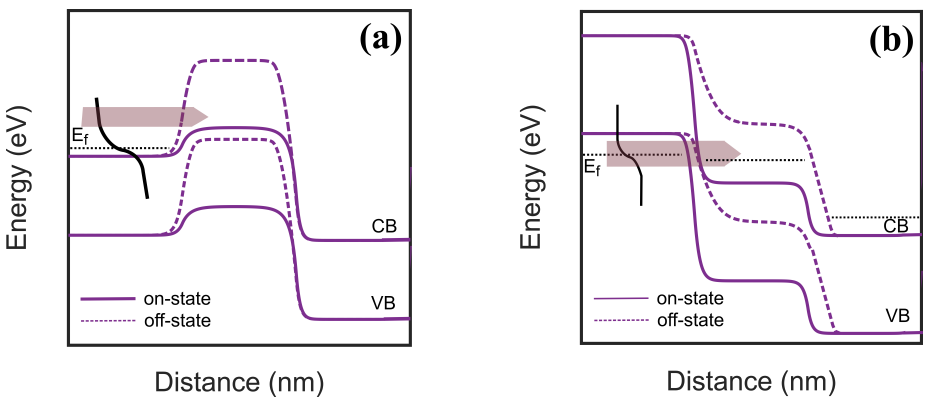

Figure 2.1: Band structure of (a) MOSFET and (b) TFET under ON- and OFF-states. The carrier transport in MOSFET is enabled by thermionic emission over the potential barrier while in TFET conduction is by tunneling through the heterojunction barrier. The arrows indicate the carrier transport.

where f is the Fermi Dirac distribution function, $E_{F,s}$ the Fermi level of the source, $E_{c,c}$ the channel conduction subband edge, $E_{v,s}$ the source valence subband edge.

Though ideally band-to-band-tunneling is the phenomenon governing current flow in TFET, several non-idealities of the device could contribute to additional currents. Fig 2.2 shows the different leakage paths through the gate oxide for any type of FET and also those that arise due to material defects and short-channel effects. Though a band structure of a TFET is utilized to describe the different leakage paths, many of them are also applicable to MOSFETs. Defects in the gate oxide and at the oxide-semiconductor interface can change the electrostatic control of the device and act as leakage paths. Defects in the channel, source or heterojunction can induce trap states and band tail states in the bandgap resulting in leakage paths and currents [19]. A degenerately doped source can have its Fermi tail within the conduction path resulting in increased leakage currents and worse S. A narrow tunnel barrier at the drain-channel heterojunction can result in tunneling in the off-state leading to ambipolar conduction for both positive and negative V_{GS}.

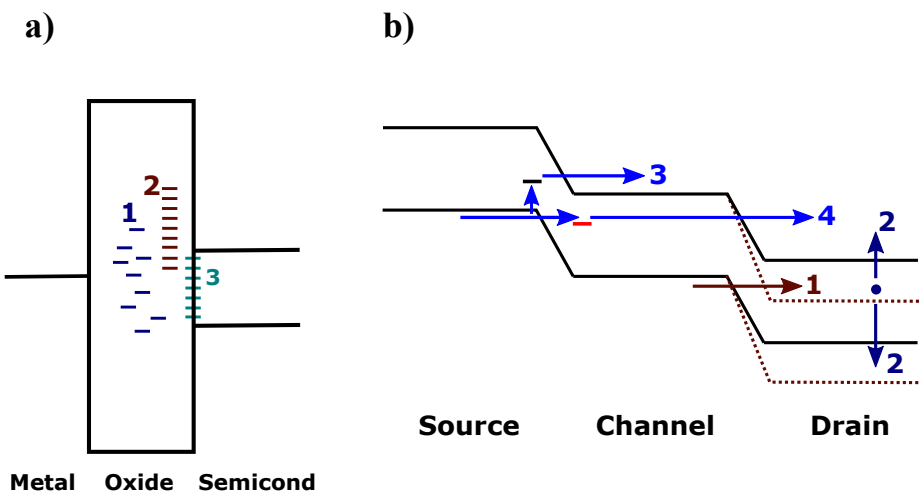

Figure 2.2: (a) Schematic illustration of the leakage paths through the gate oxide. (1) Oxide traps within the material, (2) Border traps a few monolayers from the oxide-semiconductor interface and (3) Interface traps at the oxide-semiconductor interface. (b) Schematic illustration of the leakage paths in a TFET. (1) Ambipolar conduction in the off-state due to narrow tunnel barrier at drain junction. (2) Shockley Reed Hall generation recombination. (3) Tunneling through band tail state or defect state in the source. (4) Trap-assisted tunneling.The red dash represent the trap state.

Efforts taken during this thesis in optimizing the device design to suppress ambipolarity are discussed in section 3.3. A more detailed discussion of the influence of defects on the device performance studied during this thesis can be found in chapter 4.

Since Band-To-Band Tunneling (BTBT) is the dominant transport mechanism in TFET, the I_{ON} achieved is usually lower than that obtained with a MOSFET. However, this can be overcome by engineering the band alignment of the source valence band edge to the channel conduction band edge to increase the tunneling probability. Fig 2.3 illustrates the different possible band alignments. Silicon would have been the favorable material of choice due to their industrial compatibility. However, TFETs made from Si suffer from poor on- state due to indirect and large bandgap as seen from the devices demonstrated within the research field (section 2.3) driving the search for alternative materials [20]. Also, homogeneous tunnel junctions can be engineered only with dopant engineering or electrostatically, leading to challenges in achieving balanced I_{ON} and off- current (I_{OFF}). Using a small bandgap material at the source to improve the tunneling current and large bandgap material at the drain to reduce the ambipolar reverse tunneling can be used to balance the on- and off- state performance of a TFET. This can be achieved by using different III-V materials to form heterojunctions. Apart from their high-performance deliverability, III-V materials also have a direct bandgap unlike Si which eases the tunnelling phenomenon in TFET thereby improving the on- currents [18]. The existence of several III-V compounds enables the formation of heterogeneous tunnel junctions. Such a possibility of band engineering provides an extra degree of freedom to reach an optimum tunnel junction as studied during this thesis work. Between the different types of heterojunctions, a broken band alignment to achieve high I_{ON} can worsen the I_{OFF} and S while a staggered band alignment will result in low

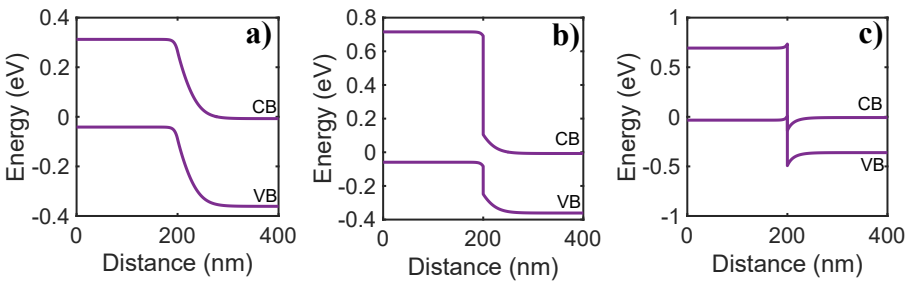

Figure 2.3: Band edge alignment for different III-V configurations (a) Homojunction (b) Heterojunction with a staggered band alignment (c) Heterojunction with a broken band alignment.

I_{ON}. A near-broken band structure is ideal for a good performing TFET [17]. Finding the right balance between S, I_{ON} and I_{OFF} using band engineering is the challenge currently in tapping the full potential of the TFETs.

2.2 TRANSISTOR ELECTRICAL CHARACTERISTICS

The electrical performance of a transistor can be evaluated using certain measurement techniques. The preliminary requirement for the measurements is to define the device configuration. For all transistors used in this thesis, the voltage bias was applied with reference to the source and hence the gate and drain bias and drain current are denoted as V_{GS}, V_{DS}, and I_{DS}, respectively. All currents, including those measured and extracted, are normalized to the number of nanowires in the device and the circumference of the nanowire. Such a normalization eases the comparison of performance between different devices irrespective of their dimensions.

2.2.1 PERFORMANCE METRICS

The drain current I_{DS} is commonly measured for various V_{GS} and V_{DS} sweeps resulting in transfer and output curves as shown in Fig 2.4. Several metrics can be extracted from the data to evaluate the device for specific applications. The polarity of V_{GS} and V_{DS} are opposite between n- and p-type devices to assist electron and hole transport respectively.

ON & OFF CURRENT

The transfer curve describes the switching capabilities between off- and on-state of the device. The I_{OFF} is the current that flows when the device is turned off ($V_{GS,off}$) and ideally it is 0 A at V_{GS} = 0 V. However, in reality the non-idealities as described in Fig 2.2 result in non-zero leakage currents resulting in non-negligible I_{OFF}. Depending on the application, I_{OFF} = 100 nA/μm, 1 nA/μm and 100 pA/μm are required for high performance, standard and low power applications, respectively. The I_{ON} is defined with respect to the used I_{OFF} as described in equation 2.3. The ratio between I_{ON} and I_{OFF} is an important DC metric, and several orders of magnitude (10^5) is desired for a good switch for digital logic applications.

$$I_{ON} = I_{DS}\left(V_{GS,off} + V_{DS}\right) \tag{2.3}$$

THRESHOLD VOLTAGE

Threshold voltage (V_T) is defined as the gate voltage at which significant electrons start to flow from source to drain. It can be extracted by fitting a tangent to the transfer curve in linear scale and the x-intercept gives the threshold voltage. Below threshold, I_{DS} decreases exponentially which is seen as a linear segment in the logarithmic transfer curve and indicates the subthreshold region of operation.

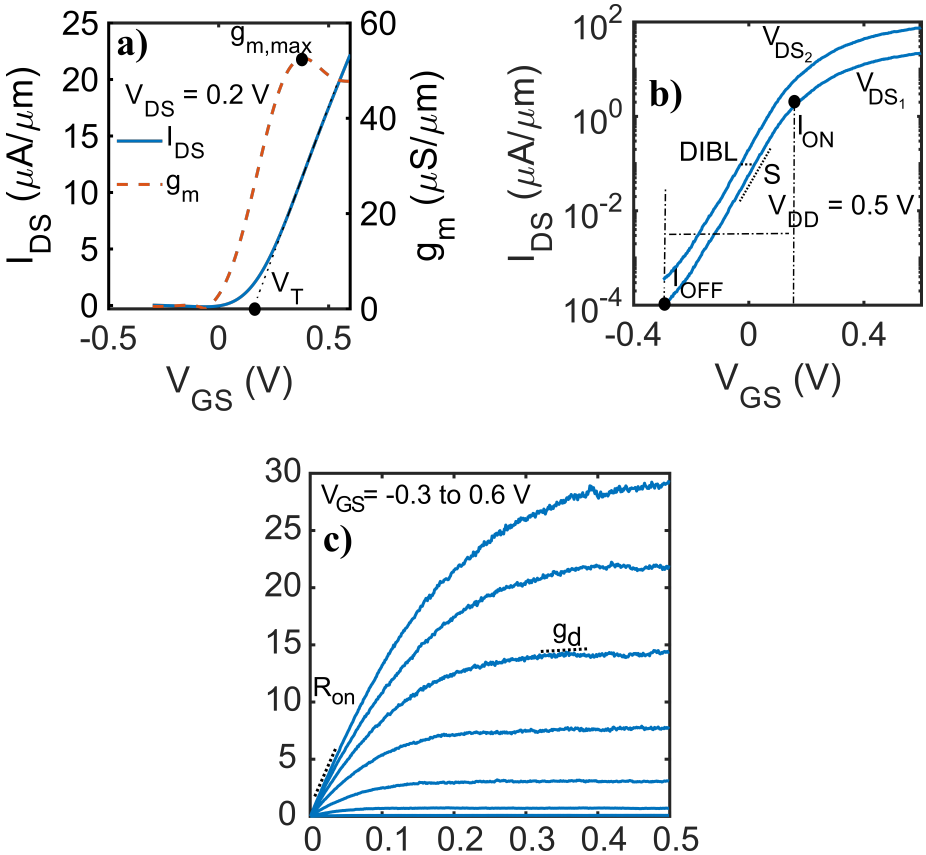

Figure 2.4: Electrical characteristics for an InAs nanowire n-type MOSFET. (a) Linear characteristics specifying the evaluation of maximum transconductance (g_m) and threshold voltage (V_T). (b) Logarithmic characteristics with S indicated. The definition of I_{ON} for a given I_{OFF} and overdrive voltage is also illustrated. (c) Output characteristics showing the evaluation of on-resistance (R_{on}) and output conductance (g_d). The characteristics and critical parameters for a p-type FET are similar with opposite polarity.

SUBTHRESHOLD SWING

The inverse subthreshold slope or subthreshold swing S, as discussed extensively in the previous sections of the thesis, is the gate voltage change required to increase the current by one order of magnitude as described in equation 2.4 and is an important DC metric that identifies the device switching capabilities.

$$S = \frac{1}{\frac{\partial \log(I_{DS})}{\partial V_{GS}}} \tag{2.4}$$

S can be extracted from the subthreshold region of the logarithmic transfer curve and a steep S signifies a large I_{ON}/I_{OFF} ratio.

TRANSCONDUCTANCE

Transconductance is an important metric for RF applications especially for signal amplification. It is, as described in equation 2.5, the current amplification obtained from small changes in the gate voltage.

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \tag{2.5}$$

Fig 2.4 (a) shows the extracted g_m that peaks in the strong inversion region of the device operation. The ratio of g_m/I_{DS} is an important metric in circuit design that states the capability of the transistor to translate power (i.e the current) into gain (i.e the transconductance) and is called the transconductance efficiency [21].

ON RESISTANCE

The on- resistance (R_{on}) of a transistor is the resistance between source and drain in the on-state and can be extracted from the output curve at $V_{GS} > V_T$ and V_{DS} = 0 V. R_{on} captures the intrinsic resistance of the material as well as the extrinsic parasitic resistances due to poor contacts and uncontacted lead regions. TFET suffers from a large resistance at the tunnel junction leading to a high R_{on} as seen from Fig 2.4 (c).

OUTPUT CONDUCTANCE

The output conductance (g_d) is the change in the current for small changes in the drain bias as described in equation 2.6 and is extracted from the saturation region of the output curve.

$$g_m = \frac{\partial I_{DS}}{\partial V_{DS}} \tag{2.6}$$

Ideally, g_d should be zero as I_{DS} is independent of V_{DS} and should depend only on V_{GS}. But, for short channel MOSFETs, Drain Induced Barrier Lowering (DIBL) as seen in Fig 2.4 (b) results in a large g_d. The intrinsic gain or the self-gain of a transistor is the maximum possible voltage gain and is given by

$$A_v = \frac{g_m}{g_d} \tag{2.7}$$

A small g_d and large g_m is crucial for obtaining a large gain and hence an amplifier is usually biased in the saturation region.

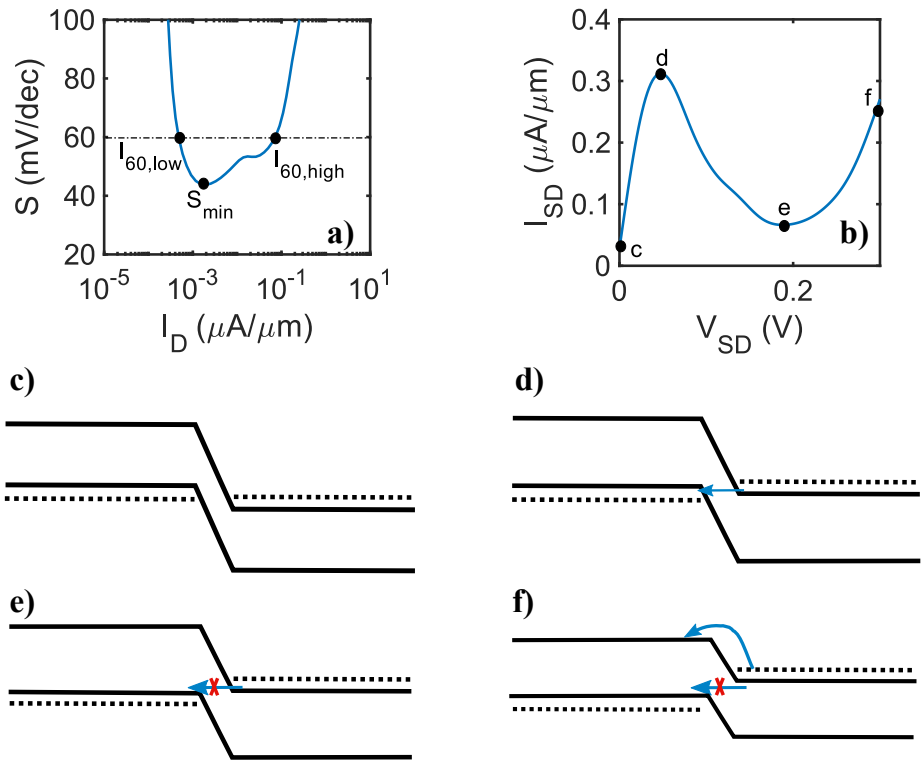

Figure 2.5: Characteristics and parameters specific to TFET. (a) I_{DS} vs S plot specifying $I_{60,low}$ and $I_{60,high}$. (b) Electrical Characteristics measured in forward bias showing the NDR behavior in a TFET. (c)-(f) Band diagrams illustrating the conduction paths at the critical points marked in (b). The arrows indicate the direction of carrier flow.

2.2.2 UNIQUE TFET CHARACTERISTICS

Apart from the characteristics and metrics discussed above, TFETs exhibit some other inherent behavior and they use specific metrics which will be discussed in this section.

Fig 2.5 (a) shows the S plotted against I_{DS} giving an overview of the current range over which the device operates as a steep switching transistor with sub-60mV/dec. In this regard the figure of merits $I_{60,low}$ and $I_{60,high}$ are defined as the lowest and highest I_{DS}, respectively when the device transitions from sub-60 to super-60 behavior [22]. This metric is useful not only for comparing different TFETs but also in comparing the subthreshold operation of TFETs with MOSFETs to assess their competitiveness.

The output characteristics of the TFET exhibit a superlinear onset in comparison to the MOSFET resulting in a higher R_{on} as seen in Fig 2.4. As stated earlier, this is related to the high tunnel resistance that depends on factors such as source degeneracy and occupancy probability of the available energy window for tunneling in addition to the tunneling probability [23].

The characteristics and metrics discussed so far are observed when the device is reverse biased. The forward bias behavior of a tunnel device can be measured using a common drain configuration sweeping V_{SD} to control the source valance band edge w.r.t. the channel conduction band edge. Under such a configuration, a negative differential resistance (NDR) is observed as shown in Fig 2.5 (b) where an increase in voltage results in a decrease in the current. Fig 2.5 (c) to (f) illustrate the conduction corresponding to the points in Fig 2.5 (b). With increasing V_{SD}, tunneling commences in the reverse direction from the conduction band of the channel into the valence band of the source reaching its peak when all the empty states in the source align with all the filled states in the channel. Further increase in V_{SD} shuts the tunneling path and any conduction observed at the valley e in Fig 2.5 (b) is due to carrier transport through the defect states located at the heterojunction and is often called the excess current. At even higher V_{SD}, the potential barrier gets lower facilitating thermionic emission resulting in increased I_{SD} as observed at f.

2.3 STATE-OF-THE-ART

The research developments in the field of III-V MOSFET and TFET have been briefed in this section focusing on n-type TFET and p-type MOSFET with an aim to provide a fundamental background to the devices studied during this work. Several reports of simulation studies to understand the device behavior and engineer devices to improve performance have been undertaken by the research community. They can be a great resource for

an experimentalist. However, only experimental reports will be reviewed in this section considering the scope of this work.

TFET

The Esaki diode, which forms the basis for TFETs have been studied extensively since its first demonstration in 1958 and the unique NDR characteristics as discussed in section 2.2.2 has found applications in oscillators. Only after 2004 when Appenzeller et al., demonstrated the sub-thermal switching of dual gated carbon nanotube FET by tunneling, the potential use of TFET for beyond CMOS began being extensively explored [24]. Si TFET was the first choice for research due to its compatibility with the current fabrication process and the established high-quality interface to high-k gate oxides. But the large and indirect bandgap of Si reduced the tunneling efficiency resulting in poor performance [25]. Strained Si and SiGe have been explored to achieve small bandgap and direct tunneling. Knoll et al., demonstrated strained Si NW n- and p-TFET with $I_{ON} > 10\ \mu A/\mu m$ at $|V_{DS}| = 0.5$ V, $|V_{GS}| = 1.6$ V and S_{MIN} = 30 mV/dec and 90 mV/dec, respectively reporting the first demonstration of an inverter with complementary Si TFET [26].

Knoch et al., provided the first insights into improving the performance by using a type-II near-broken band lineup [17]. III-V semiconductors with a wealth of high carrier mobility materials allowing band engineering was found to be an appealing candidate for TFETs. Initial implementations of III-V TFETs were on III-V substrates since the large lattice mismatch to Si substrate would lead to high defect density. Seabaugh et al., studied planar InAs/AlGaSb, InAs/InP and InAs/GaSb airbridge TFETs with gate both in-line and normal to the tunneling direction [27, 28]. Contact and access resistances were seen to limit the performance and was circumvented using forming gas anneal (FGA) and SiN_x passivation. Datta et al., explored InGaAs TFET as homojunctions, highly doped pocket at the junction and InGaAs/GaAsSb heterojunction and found that tuning the Sb:As ratio of the source helps vary the band offset and hence the tunnel barrier width [29, 30]. Pulsed I-V measurements that mitigate the effects of interface traps on the transistor characteristics and the first report of RF characterization of TFET was demonstrated [31]. Takagi et al., investigated the dopant implantation and diffusion in InGaAs to achieve abrupt doping profile at the tunnel junction [32, 33]. Further optimization of the In content and strain engineering resulted in TFET with S = 62 mV/dec. Zhao et al., improved the dry etching process for a top-down fabricated NW and demonstrated the first fully vertical III-V TFET with S = 79 mV/dec. Improving the spacer technology helped reduce the S further down to 53 mV/dec [34]. Alian et al., reported InGaAs/GaAsSb vertical NW TFET with S = 47 mV/dec and I_{ON} =

0.7 μA/μm [35]. Development of EOT scaling process and analysis of defects helped in the realization of the steep switching devices. Moselund et al., were among the first few to integrate III-V TFETs on Si substrate by utilizing template-assisted selective area growth of NW [36]. InAs/Si p-TFET achieving S = 70 mV/dec and I_{ON} = 4 μA/μm at V_{DS} = -0.5 V had been presented. Complementary TFET and hybrid MOSFET-TFET integration on Si platform have also been explored. Tomioka et al., has developed core-shell vertical nanowire TFETs on Si substrate with strain engineering and modulation doping to enhance the performance [37]. Core-Shell vertical InAs/GaSb TFET with GaAs barrier has been reported by TSMC to achieve line tunneling improving the I_{ON} to 40μA/NW and S = 40 mV/dec at V_{DS} = 0.3 V [38]. The different generations of VLS grown vertical InAs/InGaAsSb/GaSb NW TFETs on Si, developed prior to this thesis work within the group, focused on understanding the scope of the studied heterojunction. Junction engineering to achieve balanced on- and off-state performance led to previous works of TFET with S = 48 mV/dec and I_{ON} = 10 μA/μm for I_{OFF} = 1 nA/μm at V_{DS} = 0.3 V [39]. For a TFET to be competitive with MOSFET, the $I_{60,high}$ and I_{ON} must ideally be 1-10 μA/μm and 10-100 μA/μm while meeting the I_{OFF} requirements for the specific applications as described in section 2.2.1 [22]. This means 6 orders of magnitude change in current under a reduced V_{DD} = 0.3 V requiring an average S<50 mV/dec.

PMOS

The challenges in the downscaling of Si CMOS have led to the exploration of alternate channel materials. III-V antimonides (Sb) and Germanium (Ge) had been the promising contenders due to their high hole mobility [40]. However, the reported devices reveal poor performances due to their limitations with respect to interface quality and leakage currents [41]. Surface passivation and interfacial Si layer has helped improve the high-k/Ge interface [42]. The small bandgap of Ge results in increased BTBT-induced leakage currents degrading the off-state which has been overcome by taking advantage of the band broadening induced by quantum confinement. GAA Ge nanowire PMOS with channel diameter down to 9 nm and L_G = 40 nm has been realized delivering I_{ON} = 500 μA/μm at I_{OFF} = 100 nA/μm and V_{DS} = -0.5 V with I_{MIN} 1 nA/μm [43]. Integration of Ge PMOS on Si NMOS has been demonstrated using wafer bonding with PMOS devices achieving I_{ON} = 630 μA/μm at similar off-state conditions [44].

Though III-V based PMOS are an obvious complement to the high performing III-V NMOS, research efforts focusing on Sb-based PMOS has lagged due to several limitations. The lattice mismatch is too high to directly grow antimonides on Si (GaSb - 12%) resulting in poor crystal quality at the

interface. This led to initial demonstrations of III-V PMOS on III-V substrates resulting in 10x lower power dissipation or 2x higher speed than strained Si PMOS [45]. GaSb, InSb, InGaSb have been the channel materials explored for PMOS implementation. InSb suffer from high leakage currents due to its low bandgap even though it can offer high performance. InGaSb offers enhanced mobility and reduced interface defects and are hence the most studied [46]. First attempts to integrate III-V PMOS with Si had been through layer transfer and wafer bonding [47, 48]. This technique however required an InAs interfacial or capping layer to protect the highly sensitive Sb layer and improve the interface to gate-oxide and metal contacts. However, the InAs layer also led to reduced gate coupling degrading the performance. III-V p-type FinFETs have suffered from rough fin edges due to reactive ion etching (RIE) employed for the dry etching in a top-down approach leading to degraded performance. W. Lu et al., studied wet chemical etching of Sb-based materials through digital etching process as discussed in section 3.2.1. Digital etching preserves the surface of the channel material without inducing roughness as in RIE. Different etchants and oxidation environments have been explored resulting in fin width of 10 nm and devices with L_G = 20 nm [49]. VLS grown vertical nanowire III-V PMOS, which had been developed within the research group previous to this thesis work, provide reduction in the device footprint and allow integration on Si platform by using an InAs buffer layer [50]. However, the InAs/GaSb heterojunction in the reported devices contribute to poor on-state which is circumvented in the subsequent developments using a W socket allowing contact to the GaSb segment of the nanowire directly. Improvements in the digital etching scheme and studies on post-process annealing have resulted in achieving I_{ON} = 20 μA/μm at I_{OFF} = 100 nA/μm and V_{DS} = -0.5 V with vertical NW devices [51]. In addition to the device material studies, the effect of metal alloying with Sb to improve the contacts had been investigated. Co-integration of III-V vertical NW NMOS and PMOS on Si have been demonstrated with balanced drive currents I_{ON} = 156 μA/μm and 98 μA/μm, respectively at I_{ON} = 100 nA/μm [52].

3

Transistor Design and Fabrication

The number of features that an electronic ICT device can offer is limited by the capabilities of the physical hardware available. Optimization of the device through meticulous material and fabrication process engineering is crucial in achieving the required performance. When working at the nanometer regime, due to the large surface-to-volume ratio, surface effects such as roughness, dangling bonds and interface quality come into play which cannot be ignored as in their bulk counterparts. In addition, the developed novel devices and processes are required to be industry compatible with reduced complexity to have a competitive edge demanding cautious planning of the fabrication process flow. In this regard, critical steps involved in the fabrication of vertical nanowire transistors and their corresponding impact on the device performance are elaborated in this chapter. The details of the entire process flows can be found in the Appendices.

3.1 VERTICAL NANOWIRE GROWTH

Vertical nanowires can be produced using either a top-down or a bottom-up approach. The top-down method is limited by the stringent requirements on the lithographic techniques to achieve nanoscale devices. The planar epitaxial growth from which the nanowires are carved out in this type of method is challenging for the growth of lattice-mismatched heterostructures as they result in high defect density at the heterointerface. The bottom-up approach overcomes this problem by using a thin seed particle to relax the lattice-mismatch strain and terminate the threading dislocations at the surface a very short distance from the heterojunction through radial expansion or contraction [53]. Such a reduction in the defect density allows the growth of

several heterojunctions within a single nanowire and eases the integration of III-V materials on highly mismatched substrates such as Si.

Nanowires that were epitaxially grown using Metal-Organic-Vapor-Phase-Epitaxy (MOVPE) on Si substrates with an n+InAs buffer layer was used for the devices discussed in this thesis work. Free-standing nanowires were grown out from Au seed particles that act as nucleation centers. The volume of the Au dot decides the length and diameter of the grown nanowire; therefore the dots need to be carefully patterned using Electron Beam Lithography (EBL) followed by lift-off.

InAs/InGaAsSb/GaSb nanowires are used for both TFETs and PMOS devices in this work as seen in Fig 3.1. TMIn, TMGa, AsH3 and TMSb were the precursors used as source materials for the growth. The gradual transition from InAs to GaSb through a short quarternary segment prevents a near-broken band alignment. The suggested heterostructure with arsenic rich channel also provides better gate-oxide interface than an all-Sb as discussed in Paper V making it a potential candidate for III-V PMOS [54]. The growth

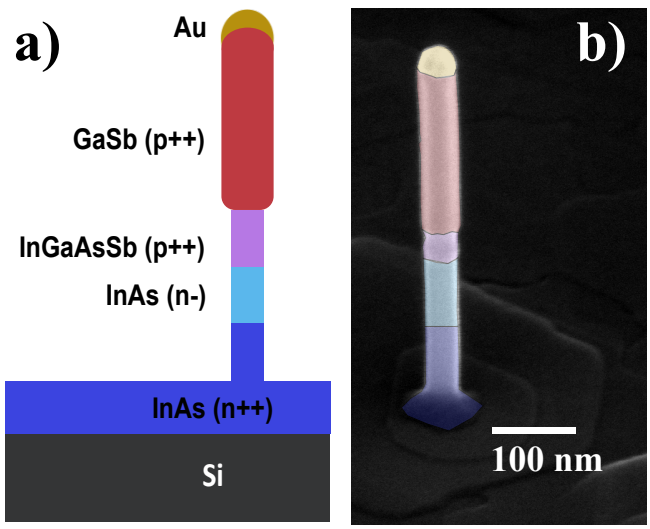

Figure 3.1: (a) Schematic and (b) False-colored SEM image of an as-grown nanowire for a TFET before device fabrication. The doped InAs segment acts as the drain while the non-intentionally doped n- InAs is the channel. The p-doped segments act as the source. The same InAs/InGaAsSb/GaSb heterojunction was used throughout the thesis with variations in the composition, doping concentration and nanowire dimensions. For the PMOS, the contact terminals are reversed, and the doping profile is altered for the same architecture as mentioned in Paper V.

temperature, precursor flow rate and V/III ratio are the critical parameters in deciding the growth rate, dimensions, and the composition of the nanowire [55]. The InAs and InGaAsSb/GaSb segments of the nanowire are doped with TESn for n-type doping and DEZn for p-type doping, respectively to make it useful for transistor operation. The particle assisted nanowire growth technique suffers from the reservoir effect, where the Au particle acts as a reservoir of precursors and dopants even after they are removed from the reactor chamber [56]. This memory effect makes the growth of an abrupt heterojunction challenging thereby hindering the realization of a thin tunnel barrier favorable for TFET devices.

3.2 IMPROVING ELECTROSTATICS

Short-Channel transistors suffer from large leakage currents in the off-state due to reduced gate control. This is often observed as increased DIBL (Drain-Induced-Barrier-Lowering) in the transfer characteristics as described in section 2.2 which signifies that not only the gate bias but also the drain bias exhibit control over the conduction barrier in the channel. Poor gate control also results in poor S which could further worsen the off-state as described in 1.4. To improve the switching behavior of a FET device, a thin channel body that can be solely controlled by the gate through a well-designed gate stack is required. Smaller Au dot sizes and hence smaller as grown nanowires have however shown to suffer from dopant segregation

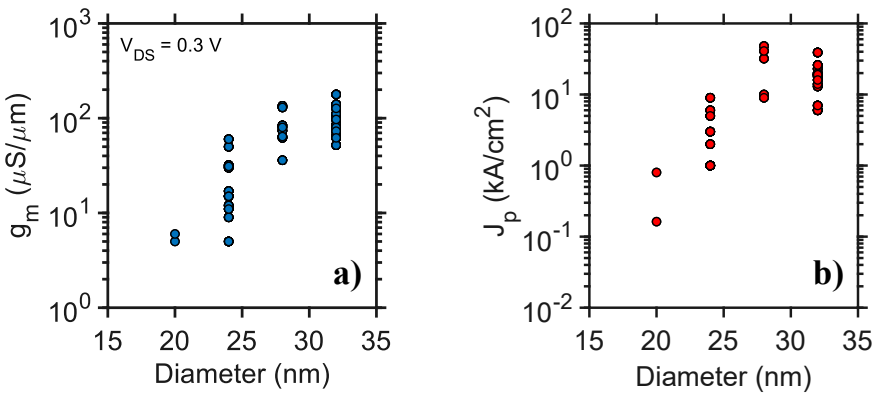

Figure 3.2: Diameter dependence of the device performance considering (a) g_m and (b) peak current density (J_p). A significant degradation is observed with decreasing diameter due to doping and source depletion effects.

close to the surface, reduced dopant incorporation and/or inflated dopant ionization energies [57, 58]. Such a low and location specific concentration of dopants would further get diminished while etching the native surface oxide to establish a good interface to the high-k gate oxide degrading the device performance as observed in Fig 3.2. Therefore, different diameters of the nanowires were grown in this work in the range of 35-40 nm which were then further thinned down to 17-27 nm, as discussed in the following section, to obtain good electrostatics. Further approaches for improving the gate electrostatics are surface treatment to have good interface to the gate oxide, choice of the gate oxide material and finally the gate metal used. Fig 3.3 illustrates the process flow involved in fabricating the gate stack for all devices in this thesis.

3.2.1 DIGITAL ETCHING

A special kind of wet chemical etching technique called digital etching is used to thin down the channel material. Digital etching is a two-step process that consists of oxidation and oxide removal in separate steps. This concept is extensively used in etching of III-V vertical nanowires. This self-limiting technique has precise etch control with nanometer-scale resolution making it a suitable solution for device scaling. The surface of the nanowires were oxidized in O_3 atmosphere for a duration of 5 min before the wet chemical etching. Acids that have high selectivity between InAs and GaSb are required to etch the channel material selectively without affecting the source(drain) in

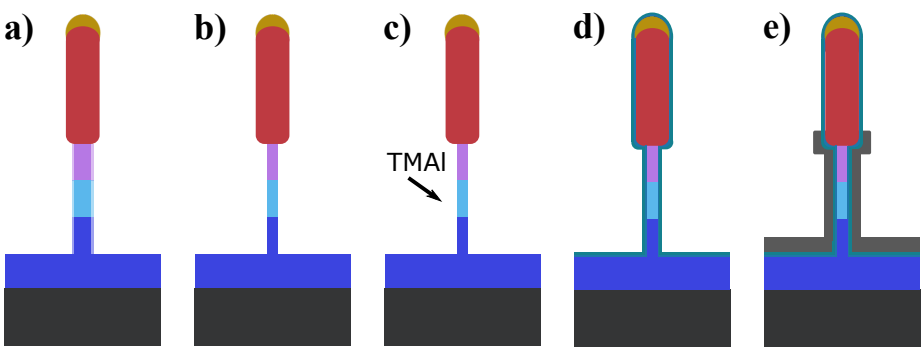

Figure 3.3: Fabrication process flow towards gate stack formation. (a) and (b) illustrate the digital etching process where the nanowire is (a) oxidized in an ozone or oxygen environment followed by (b) wet etching to thin down the channel. Gate stack is deposited with (c) an ALD self-cleaning, (d) High-k gate oxide ALD and (e) Sputtering and contact pad definition of the gate metal.

an nTFET (PMOS). Citric acid and HCl have been proven to selectively etch InAs and GaSb, respectively and were hence employed in this thesis. Fig 3.4 (a) and (b) show the microscopy image of a nanowire before and after digital etch of the InAs bottom segment with citric acid. Note that after 3 cycles of etching, the diameter of the InAs reduced by 10 nm, while the top GaSb segment remains unaltered.

Depending on the composition of the quarternary InGaAsSb segment, it etches differently using citric acid as compared to HCl. An example of etching of the InGaAsSb segment at a higher rate than the InAs segment resulting in a very thin connecting point between the top and the bottom segment can be seen in Fig 3.4 (c). A systematic calibration of the etch rates for each growth scheme is crucial in improving the process yield. In addition, oxidation using O_3 has shown to form insoluble non-uniform Sb-oxides such as Sb_2O_5 that cannot be easily removed [49]. A SEM (Scanning Electron Microscopy) image of such a nanowire during digital etch process is shown in Fig 3.4 (d). Such an oxidized surface can be detrimental for forming a good contact to a TFET and for the gate stack for a PMOS with an InGaAsSb channel. Hence, oxidation in O_2 atmosphere for 8 min instead of O_3, which has been shown to circumvent this issue, was adopted [49]. Core-shell nanowires processed during this thesis work used HCl:IPA to etch the GaAsSb shell with an etch rate of 2 nm/cycle and citric acid to thin down the InAs (InGaAsSb) channel for TFET (PMOS) with an etch rate of 1.5 nm/cycle. The shell was partially removed from the channel region while remaining intact on the source (drain). For a selective area etching scheme as employed for the core-shell structures, the

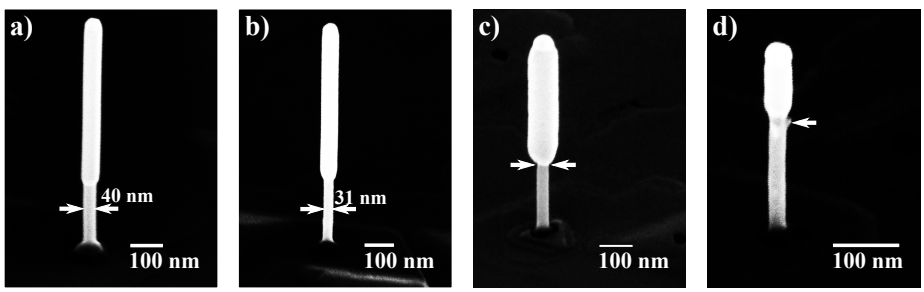

Figure 3.4: Scanning Electron Microscopy (SEM) images of nanowires during digital etch process. (a) As-grown nanowire before subjecting to any processing. (b) Digital etching of the bottom InAs segment after 3 cycles resulting in a 9 nm reduction in the diameter. The effect of digital etching on the quarternary InGaAsSb segment is seen in (c) where the etch rate of the quarternary segment is higher leading to possible breaking and (d) where the segment is oxidized to insoluble oxides.

rate of under-etch beneath the top metal needs to be calibrated based on the shell composition to position the shell precisely. In addition, blow drying the nanowire to remove the liquid after etching may result in breaking of the nanowires depending on their aspect ratio and the surface tension. This can be resolved by rinsing in IPA instead of water or by using zero surface tension drying techniques such as critical point drying. Also, to etch Sb oxides, HCl dissolved in water has shown to result in significant surface roughness and hence HCl:IPA is a suitable solution [49].

3.2.2 GATE STACK FORMATION

Transistors made from III-V materials usually have high-k materials as gate oxide as their native oxides forms a poor interface resulting in high interface trap density [59]. In this regard, several high-k layers have been tested on III-V materials including Al_2O_3, HfO_2 and ZrO_2 [60]. In this thesis, an Atomic Layer Deposited (ALD) bilayer high-k consisting of Al_2O_3 followed by HfO_2 has been adopted as illustrated in the schematic in Fig 3.5 (a). Before deposition, 5 cycles of trimethylaluminum (TMA) precursor were pulsed to utilize the in situ self-cleaning effect that reduces the interfacial III-V native oxides [61, 62]. A high-k material with large dielectric constant gives a good capacitive coupling to the gate electrode and therefore HfO_2 was used. An interfacial Al_2O_3 is used as a barrier due to its proven good interface to III-V materials and its large bandgap making highly scaled Equivalent Oxide Thickness (EOT) possible. Fig 3.5 shows the transfer curves along with the gate current (I_{GS}) for two devices with different EOT developed during this

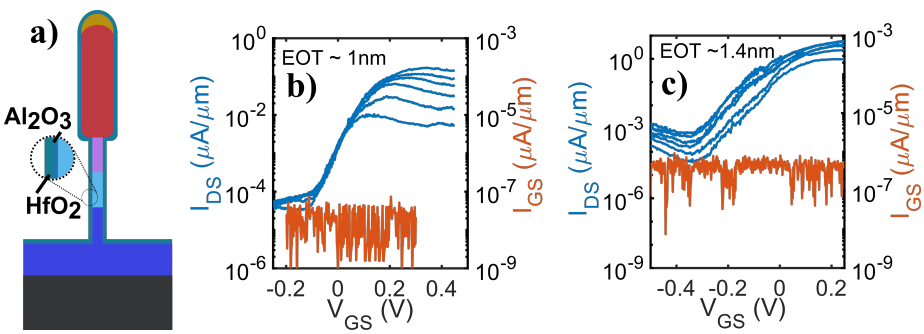

Figure 3.5: (a) Bilayer gate oxide stack shown as a zoom-in from the nanowire device fabrication process. The effect of EOT scaling on the device characteristics considering the I_{OFF} and I_{GS} are evaluated from TFET devices with (b) EOT 1.4 nm and (c) EOT 1 nm. A significant reduction in I_{GS} and I_{OFF} is observed resulting in improved S from 46 mV/dec to 41 mV/dec.

thesis. The values of I_{GS} are close to the noise floor of the measurement equipment in both cases suggesting that there is still room for gate oxide scaling. Improved gate control by scaling the EOT also leads to reduced DIBL as observed from the transfer curves. The improvement in S of the TFET devices from 46 mV/dec to 41 mV/dec due to high-k scaling together with drain underlap can be seen from the plot and from Paper I.

Finally in the gate stack fabrication process is the deposition of gate metal by sputtering W. The placement of the metal edge is crucial especially for a TFET device in which case the ideal gate position would be at the tunnel junction as shown in Fig 3.6 (a). The grading of the junction in most cases resulted in an increase or decrease in the thickness of the nanowire as seen in Fig 3.6 (b) which assisted in the gate alignment. A resist etch back process was used for gate length definition for all samples fabricated in this thesis. After W sputtering, a thick S1800 was spin coated followed by RIE to define the length followed by W dry etching with SF_6:Ar. The defined resist thickness further gets reduced by 30-50 nm during the W etch resulting in a gate placement below the tunnel junction. This can result in a non-gated intrinsic channel (Fig 3.6 (c)) acting as a potential barrier and the TFET losing its purpose and acting as a MOSFET instead. Hence to be safe, the gate was usually defined above the tunnel junction (Fig 3.6 (d)) even though such a placement could lead to source depletion.

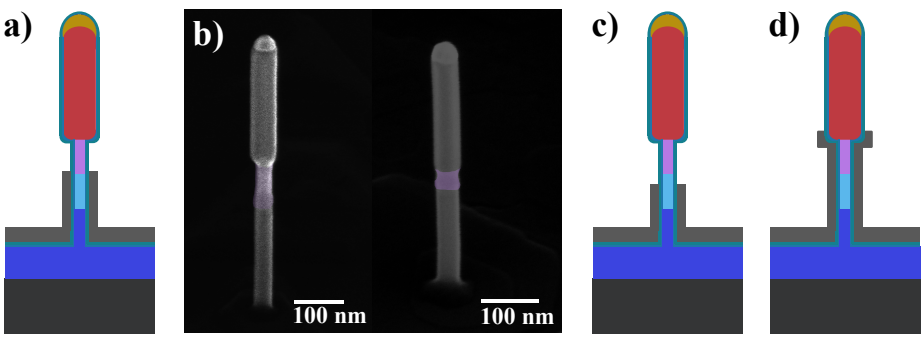

Figure 3.6: (a) Schematic of a TFET device illustrating the ideal position of gate metal edge (b) SEM images of two nanowires highlighted with a locally altered thickness at the junction. Schematic of a TFET device with gate (c) underlapping the channel and (d) overlapping the source.

3.3 IMPROVING OFF-STATE LEAKAGE - SPACER ENGINEERING

The static leakage currents in the off-state of a TFET device can be attributed mainly to the ambipolar conduction at the drain-channel tunnel junction as

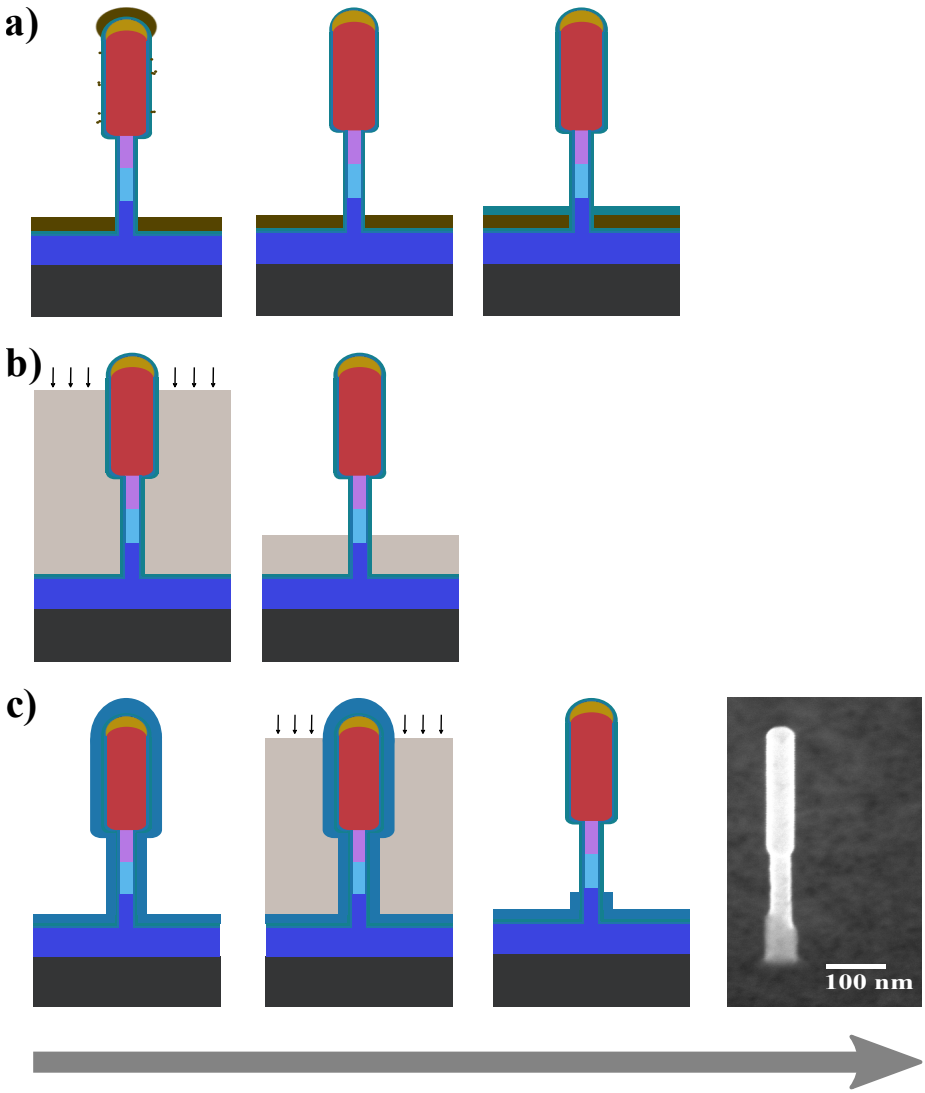

Figure 3.7: Schematic illustration of the fabrication process flow of various spacer technologies employed in this thesis work. (a) Evaporated SiO_x leaving behind flakes on the nanowire sidewalls which is removed with HF followed by extra ALD deposition. (b) Spin coated resist etched back to desired thickness using O_2 plasma. (c) ALD deposited Al_2O_3 defined using resist etch back and HF etching.

described in Fig 2.2 (b) in section 2.1. This can be suppressed by reducing the gate control of the channel-drain heterojunction using bottom spacer engineering as in Paper I and III. Furthermore, the gate oxide alone cannot provide enough isolation between the metal contacts due to the large contact pad area and hence incorporating a low-k spacer material is required to avoid a short. A few different spacer materials as illustrated in the schematics in Fig 3.7 were studied in this thesis to understand and improve the device behavior.

A thermally evaporated SiO_x spacer provides good isolation properties with its low-k value and is also easy to fabricate. The thickness of the material is controlled during deposition and does not require post-evaporation length definition. However, the 15 nm thick SiO_x evaporated resulted in deposition of flakes on the sidewall of the nanowire which required wet chemical etching to be removed. Such an etch usually affected the underlying HfO_2 of the bilayer Al_2O_3/HfO_2 gate oxide resulting in uncertainties in high-k layer thickness and EOT and hence an extra 2nm HfO_2 ALD always had to be deposited as a compensation.

To overcome this, an organic spacer of S1800 that is spin coated and permanently baked was adopted. The thickness of the organic spacer was defined using O_2 plasma RIE as described in Fig 3.7 (b) using the etch back process to create a gate drain underlap of 25 nm as presented in Paper I helping suppress ambipolarity. However, the resist etches faster at the edges of the sample resulting in non-uniform thickness over the sample. To

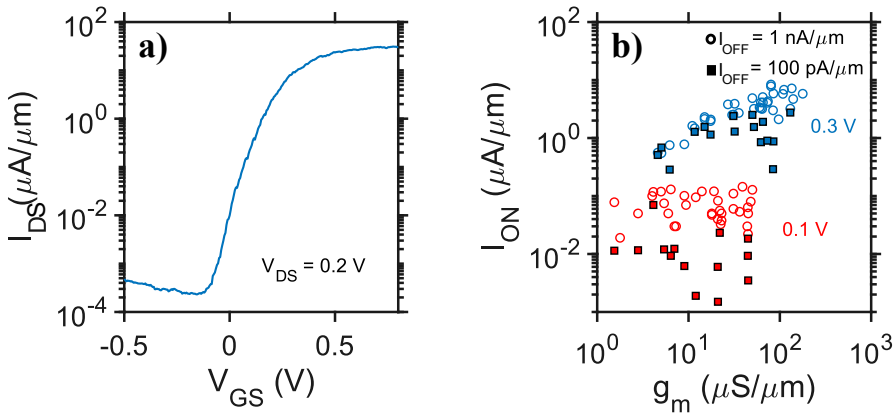

Figure 3.8: (a) Transfer characteristics of a TFET device with suppressed ambipolarity using an Al_2O_3 field plate. (b) g_m vs I_{ON} of 15 devices from the same sample at I_{OFF} of 1 nA/μm and 100 pA/μm showing the capabilities of the devices for low-power logic.

improve the device yield, sacrificial S1800 coated pieces had to be used to circumvent this effect. Despite their benefits, organic spacers suffer from moisture accumulation resulting in charge trapping. This deteriorates the device performance over time and requires frequent annealing to achieve reproducable results. In addition, the hard baking temperature of the resist limits the temperature of further processes in the device fabrication.

A more stable alternative is an Al_2O_3 spacer that is thick enough to reduce the capacitive coupling between the contact pads. An ALD deposited spacer of 10 nm thickness was utilized in this thesis work (Paper II and III) to serve a dual purpose both as a spacer and as a field plate at the drain side bottom segment as shown in Fig 3.7 (c). A field plate is a device structure used commonly in high-power FETs to engineer the electric field [68, 69]. By increasing the thickness of the dielectric close to the drain-end, the gate coupling reduces drastically around the field plate suppressing the ambipolar conduction at the drain-side junction and resulting in reduced off-state as shown in Fig 3.8. The achievable minimum current reaches 100 pA/μm extending the capabilities of the discussed devices for low-power logic applications (Paper V). The developed Al_2O_3 spacer was also used for the PMOS devices to improve the DIBL (Paper V). The suppressed off-state in the PMOS can be seen from Fig 3.9 where the demonstrated devices exhibit the lowest I_{MIN} among the benchmarked devices despite their short gate length (L_G) of 60 nm.

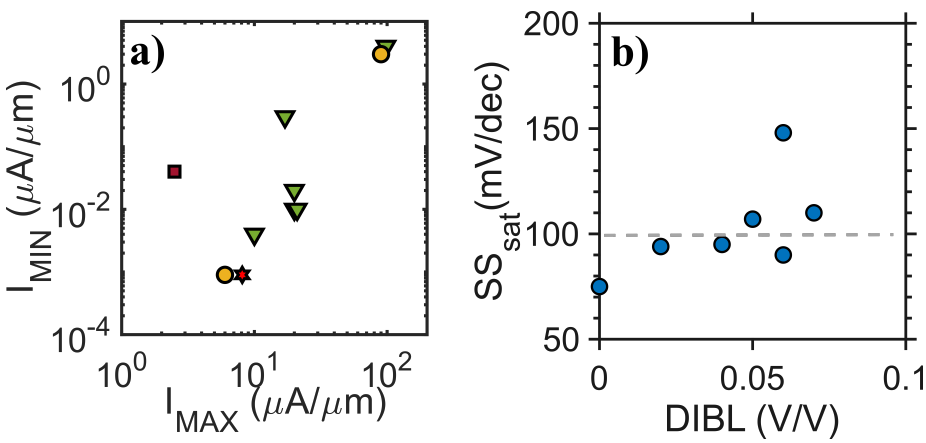

Figure 3.9: (a) Benchmarking of I_{MIN} of the PMOS developed during this thesis with state-of-the-art III-V PMOS. The red star corresponds to this work, green triangles are other vertical nanowire devices [50–52, 63–65], yellow circles are FinFETs [49, 66] and brown squares are wafer bonded devices [67]. (b) Evaluation of the gate control of the PMOS using 8 devices showing negligible DIBL and sub-100 mV/dec switching.

3.4 DEVICE RESISTANCE

Transistor performance is limited by extrinsic parasitic resistances due to heterojunction band non-optimal alignment, poor interface to the metal contact pads, large non-contacted segment, and insufficient doping. The various resistances inherent to the electrical performance of a vertical nanowire FET are depicted in Fig 3.10. Among the types of FETs studied in this thesis, the large R_{on} observed for TFET can be attributed to the resistance at the tunnel junction as the devices exhibit a transmission probability of 0.02 (Paper VI). This suggests that an optimum band alignment is crucial to extracting the full potential of the chosen material for TFET operation. On the other hand, the observed low currents of the PMOS in Fig 3.9 (a) could be due to the large contact and access resistance due to non-optimum dopant concentrations and non-ohmic metal contacts [70]. Improving the on-state performance by reducing the device resistance without increasing the off-state leakage is necessary and so a conscious device design that finds the best trade-off is important. An effort towards finding the optimum is discussed in the following subsections.

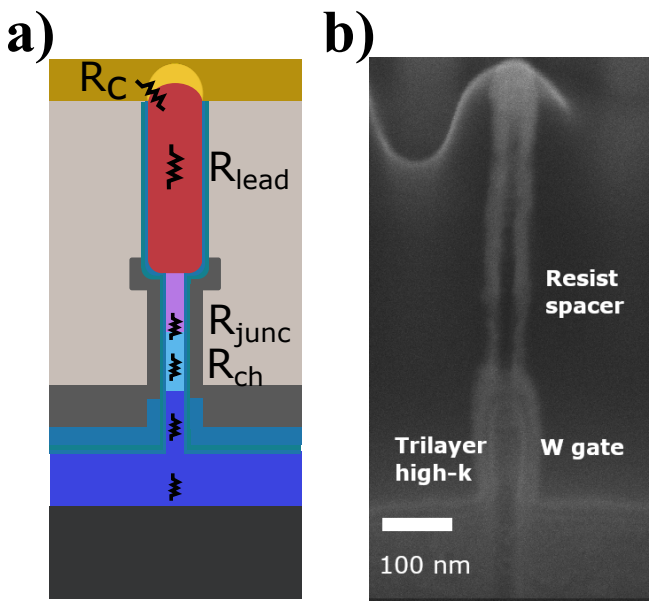

Figure 3.10: (a) Illustration of the resistances associated with a nanowire FET device including the parasitic and intrinsic components. (b) Cross-sectional SEM image of a TFET for comparison to (a)

3.4.1 HETEROJUNCTION ENGINEERING

Variations of the composition of the source segment help vary the band line-up at the tunnel junction [71, 72]. In this thesis, a systematic experimental analysis was conducted as stated in Table 3.1 to get insight into the influence of the critical nanowire growth parameters such as As composition, In pulsing and temperature on the band alignment and electrical characteristics of InAs/InGaAsSb/GaSb TFETs. Such a study helped fine-tune the tunnel barrier based on the application requirements to obtain specific S, g_{m}, I_{ON}, and $g_{\mathrm{m}}/I_{\mathrm{DS}}$ as discussed in Paper II.

Table 3.1: Sample list used in the evaluation of the nanowire growth parameters of a TFET. As composition, In pulsing and growth temperature correspond to the InGaAsSb source segment.

Sample	As composition	Temperature	In pulsing
A	0.64	460	5
B	0.70	430	5
C	0.80	460	5
D	0.92	460	5
E	0.70	439	5
F	0.70	448	5
G	0.70	430	3
H	0.70	430	4
I	0.70	430	5
J	0.70	430	6
K	0.70	430	7

The compositional variation induces lattice mismatch that can result in strained source segment significantly affecting the device performance. The difference in I_{ON} for different growth temperatures was negligible. However, the devices grown at 430°C could demonstrate a slight steeper switching. Fig 3.11 shows the band edge alignment at the tunnel junction for samples A-D with varied As composition. A band alignment that provides a narrow tunnel barrier enhancing the transmission probability and increasing the g_{m} would in turn act as a leakage path in the off-state due to the same thin barrier. Hence tuning the band lineup that balances the tradeoff between the on- and off-state is important. As described in Paper II, the As composition of 0.7 and In

pulsing of 5s provided the best balance between S and g_m and hence Sample B was found to be a good baseline growth for digital logic applications. For applications requiring higher current levels, Sample D with a little higher but still sub-60 mV/dec S could act as a baseline.

3.4.2 CONTACT ENGINEERING

Antimonide based transistors suffer from poor ohmic contacts due to inefficient removal of native oxide and high sensitivity/reactivity to most wet chemicals [49]. GaSb and InGaAsSb segments are present in this work in both the TFET and PMOS as source and drain segments, respectively. In addition, the TFETs could suffer from high drain resistance due to thinning of the InAs drain along with the channel during digital etching. Since increasing the drain doping to bypass this issue could increase ambipolar conduction, efforts were focused on maintaining the as-grown diameter of the InAs drain segment.

A W socket developed at the bottom of the bare nanowire is seen in Fig 3.12 using a similar technique as for the Al_2O_3 bottom spacer described in Fig 3.7 (c). Such a process involves RIE and O_2 plasma cleaning afterwards to remove the byproducts from etching that lead to rough and highly oxidized nanowire sidewalls resulting in uneven etching of the channel during digital etching. The problems faced could also be due to the W socket contributing to metal assisted chemical etch. Due to these issues, the socket process was abandoned. An alternative to W can be an ALD deposited Al_2O_3 socket that does not require any plasma etching. In either case, defining the socket exactly to the doped half of the InAs segment is challenging as there is no physical differentiation observed between the doped and undoped segments of the nanowire.

To reduce the top drain access resistance in PMOS, a core-shell structure with highly doped shell was adopted along with gate last fabrication process [73]. The metal cap also acts as a protective layer for the highly reactive Sb-

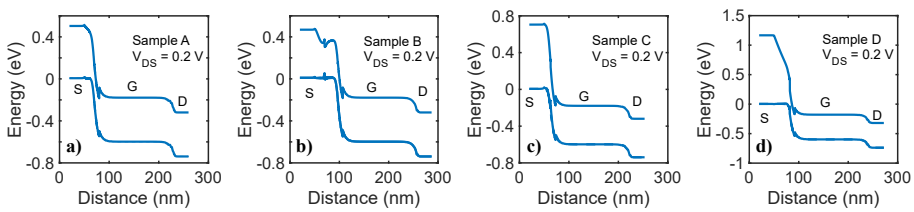

Figure 3.11: Band edge simulations using bulk parameters for sample (a) A, (b) B, (c) C and (d) D at V_{DS}= 0.2 V. Note the thin tunnel barrier for the highest As composition sample D.

segments. The schematic and SEM images of a nanowire with W top contact is shown in Fig 3.12. The process flow for top metal definition is similar to the process detailed for core-shell vertical transistors in the next section.

3.5 HYBRID DEVICE DESIGN

As described in section 3.1, different Au dot diameters were patterned throughout the sample die providing nanowires of various lengths and diameters. Utilizing a core-shell nanowire configuration and tapping into these dimensional variations, hybrid multi-platform sample dies were developed as proof of concept during this thesis. These consisted of single nanowire devices that function as only PMOS or both as PMOS and n-type TFET or as only n-type TFET as shown in Fig 3.13 depending on the position of the shell edge. A shell edge far from the InAs/InGaAsSb junction resulted in gating of a long segment of the intrinsic InGaAsSb segment providing PMOS operation (Fig 3.13 (b)). A shell edge defined close to the tunnel junction but overlapping the InGaAsSb segment gave gating of a short segment of the intrinsic InGaAsSb resulting in PMOS+nTFET operation depending on bias. A shell defined very close to the tunnel junction provided nTFET only operation.

Reconfigurable FET (R-FET), which configures a single device based on the bias polarity for both n-type and p-type operation, is an emerging field of

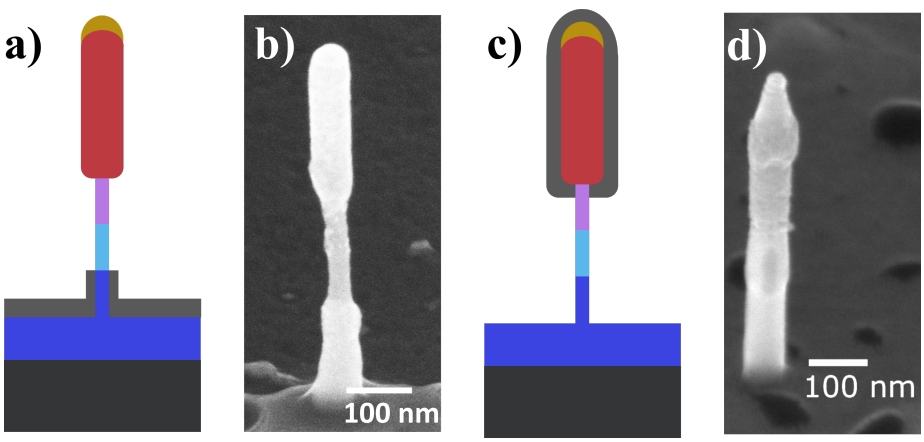

Figure 3.12: (a) Schematic of W socket at the drain segment to protect diameter thinning during digital etching of the channel. (b) SEM image of a digitally etched nanowire post W socket. (c) Schematic and (d) SEM image of the top W metal acting as a contact for source (TFET) or drain (PMOS) to reduce the access resistance.

research to combat the problems associated with power efficiency, device footprint and hardware security [74, 75]. Several R-FETs have been demonstrated based on both top-down and bottom-up nanowires with planar devices and dual gated Schottky junctions [76, 77]. To scale down the device footprint further at reduced device complexity, vertical single nanowire and single gate R-FET is demonstrated in this thesis. The process flow starting from the as-grown nanowires leading up to the placement of the shell is described in detail in Fig 3.14 along with SEM images that provide snippets of the real device. A more detailed account of the same can be found in Appendix B. As grown core-shell nanowires were covered with a sacrificial Al_2O_3 of 10 nm thickness deposited by ALD at 120°C. This layer protects the nanowire surface from plasma in the subsequent processes. The position of the shell edge was defined using an S1800 resist etch back process. When the thickness of the resist was defined, the sacrificial layer was removed with HF and a W top metal was sputtered. The resist used in this process limited any high temperature metal depositions and hence ALD TiN preferred as a protective layer on top of W could not be deposited. The W was removed from the planar surface by anisotropic etching in Inductively Coupled Plasma-RIE (ICP-RIE) using SF_6:N_2. Subsequently, the resist and the sacrificial Al_2O_3 were removed from below the shell edge.

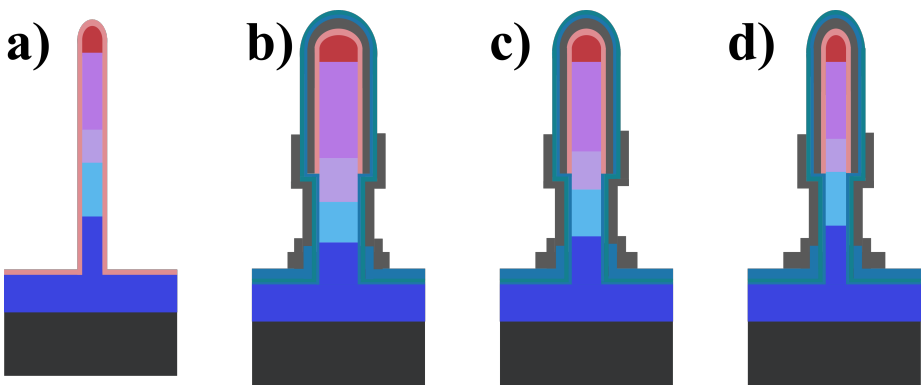

Figure 3.13: (a) As-grown core-shell nanowire. The length of the segments vary based on the Au dot diameter. (b), (c) and (d) illustrate the length variation of the different nanowire segments with respect to the Au dot size facilitating gate placements at (b) the intrinsic InGaAsSb segment far from the junction, (c) the intrinsic InGaAsSb segment close to the junction and (d) the tunnel junction.

3.6 CRITICAL STEPS - VERTICAL DEVICE PROCESS

The vertical nanowire transistor fabrication process has several critical process steps especially due to the small scale at which the devices are produced. A

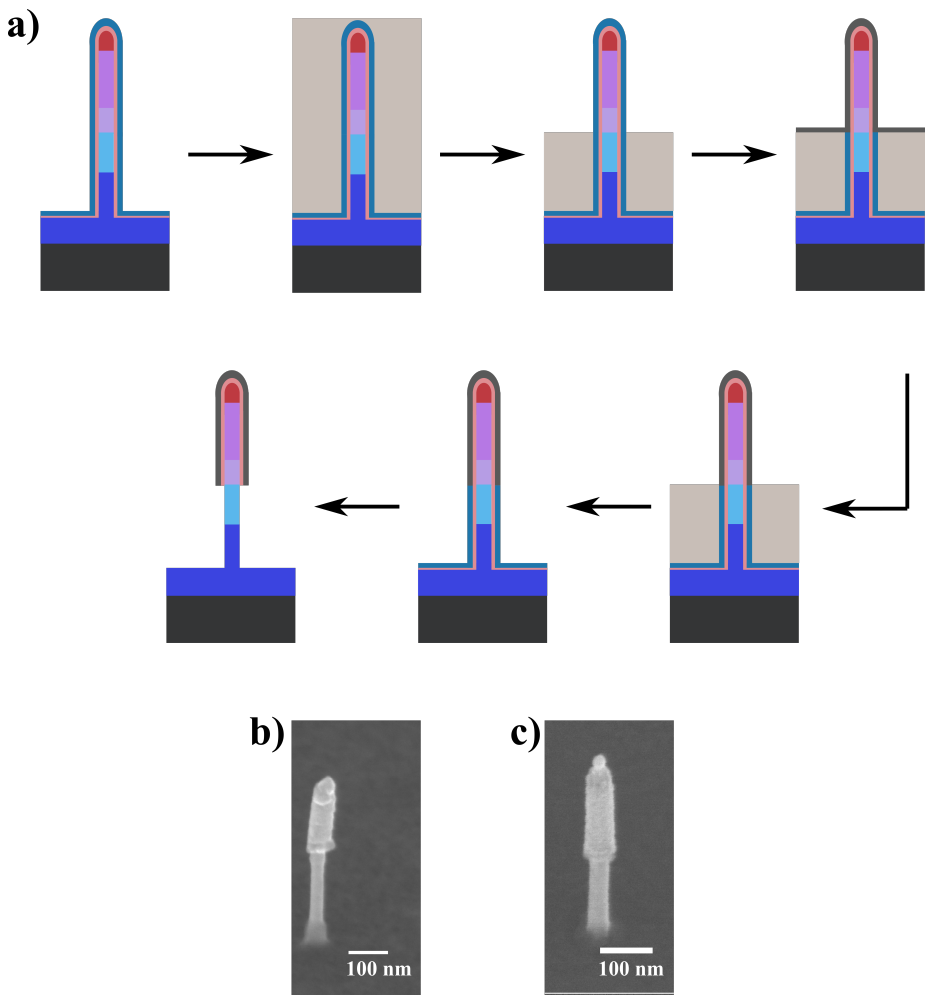

Figure 3.14: (a) Fabrication process flow for a core-shell nanowire TFET. (i) Al_2O_3 sacrificial layer (ii) Resist spin coating (iii) RIE resist etch back (iv) Al_2O_3 etching and W sputtering (v) Anisotropic W etch (vi) Resist removal (vii) Sacrifical layer removal. SEM images with the top metal enclosed shell defined at (b) the intrinsic InGaAsSb segement and (c) close to the tunnel junction.

summary of the most important factors to pay attention to during device processing recognized from experience are listed below.

- Digital etching – The aspect ratio (Length:Diameter) of the nanowire is crucial for the minimum achievable diameter without breaking the nanowires. A safe aspect ratio for the particular nanowire structure used in this thesis work would be 30:1. Wires with segments of different diameters as seen with the thinner InAs and thicker GaSb regions as used in this thesis need additional care as described in section 3.2.1.
- Bottom spacer – The under-etching of Al_2O_3 during HF etching needs to be calibrated. Etching Al_2O_3 with a thin resist to obtain a short Al_2O_3 field plate could lead to a potential short between the contact pads due to under- etching.
- Gate definition – A sputtered W metal of poor surface quality or with strain can result in delamination or cracking of the W film. The byproducts from the dry etching of such a film tend to be hard to remove.
- Top spacer – The top spacer definition is followed by the gate oxide removal from the top of the nanowire using HF 1:400. During this process, an under etching of the high-k layer further below the resist layer of about 50-100 nm is expected. Hence the top spacer must be defined as high as possible to the top of the nanowire to allow room for the under-etch. This is a highly critical step in the whole device process that could lead to potential short of contact pads.
- Metallization – Ni/Au of 10/150 nm is used as contact pads for gate, source and drain segments. After metal sputtering, UV lithography is used to define the pads followed by lift-off. If the lift-off is delayed after the deposition, there is possibility of Ni alloying with the semiconductor resulting in an unetched metal alloy layer.

4

Electrical Characterization

In this chapter, the electrical performance of the three different types of devices n-TFET, p-MOSFET and R-FET developed during this thesis work will be discussed. InAs/InGaAsSb/GaSb vertical nanowires form the baseline for all the technology platforms. Through the process developments mentioned in the previous chapter, several improvements in device performance have been achieved such as the steepest TFETs with high I_{ON}, steep switching PMOS, and multi-use single nanowire devices. In addition to the standard device characterization used to extract the digital and analog metrics, other kinds of device characterizations helpful in gaining physical insights of the device operation are discussed in this chapter. Such a fundamental understanding is crucial to exploit the resources efficiently and upgrade the devices.

4.1 DEFECTS

As mentioned briefly in section 2.1, the performance of FETs is degraded greatly by the defects/traps located at the oxide interface, heterojunction interface and border traps within the bulk of the oxide due to the large surface to volume ratio of the materials used [19]. Traps can act as leakage paths degrading mostly the off- state of the device. There are techniques to mask the effect of the traps during measurement to provide a hint of the intrinsic capabilities of the FET. For example, pulsed measurements where voltage pulses with short pulse widths can be used for biasing the transistors thereby suppressing the traps with longer capture times [31].

4.1.1 OXIDE BORDER TRAPS

Among the different leakage mechanisms through the gate oxide, carriers escaping due to tunneling can be suppressed by increasing the thickness of the gate oxide layer. On the other hand, trap-assisted tunneling mechanisms are harder to control as they depend on material quality. The high-k oxide quality can be assessed by evaluating the border trap density (N_{bt}). One of the techniques used for N_{bt} extraction is the low frequency noise (LFN) measurement as shown in Fig 4.1 for a core-shell PMOS device developed during this thesis. Traps in the oxide can charge and discharge continuously exchanging carriers to the channel causing fluctuations in the surface potential and the flat-band voltage (V_{fb}) seen as noise in I_{DS}. This noise due to variation in the number of carriers is called the number fluctuations and the resulting fluctuations in the mobility due to changes in scattering due to number fluctuations is called correlated mobility fluctuations. A detailed description of the low frequency noise can be found in [78] for further reading.

The measured noise spectral density in Fig 4.1 (a) is independent of gate bias at all measured frequencies suggesting a large series resistance. By multiplying the noise power spectral density (S_{I_D}) with the factor ${V_{GS}}^2/{I_{DS}}^4$, the resistance noise spectral density (S_R) was obtained as seen in Fig 4.1 (b) from which the noise that is independent of V_{GS} due to series resistance was subtracted to get the intrinsic device noise. Such an analysis could provide insight into the existence of bad contacts as well as the intrinsic transport mechanism. 2D TMD materials that are known to suffer from poor ohmic contacts have used the above technique extensively to analyze their device characteristics [79]. The McWhorter model describing the number fluctuations fits well with the measured noise providing a minimum N_{bt} $10^{19} cm^{-3} eV^{-1}$

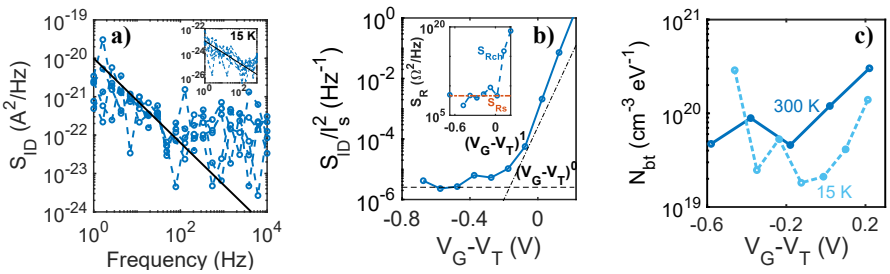

Figure 4.1: (a) Noise current power spectral density (S_{I_D}) as a function of frequency for varying V_{GS}. Inset shows the measurements at 15 K. (b) Normalized current noise as a function of the overdrive voltage. Inset shows the noise resistance power spectral density (S_R) for the channel (S_{Rch}) and the series resistance (S_{Rs}). (c) Border trap density at 300 K and 15 K.

at 300 K and 15 K as shown in Fig 4.1 (c). The N_{bt} reaches its minimum at a similar overdrive voltage (V_{GS}- V_T) for n- and p-type TFETs and MOSFETs that use the same gate oxide. This conclusion is based on comparison to devices developed within the research group during previous works published in [80] suggesting a uniform trap distribution within the high-k.

4.1.2 BAND TAILS

The traps associated with the nanowire arise from irregularities in the crystal structure during growth. The material disorder, impurities, strain etc., can result in a density of states (DOS) tail that decays exponentially into the bandgap resulting in the blurring of the band edges as illustrated in the schematic in Fig 4.2. These extended DOS could act as leakage paths in the off-state as described in section 2.1 worsening the slope.

A high doped source with a near broken heterostructure is crucial for narrow tunnel junction in a TFET. However, a very high doping can result in band tails [81, 82] that bring the exponential tail of the Fermi distribution into the tunneling path thereby degrading the off- state as shown in Fig 4.2 (b). On the other hand, a too low doping can result in the depletion of carriers in the source segment that is overlapped by the gate metal resulting in two slope regions in the transfer characteristics [83]. The right balance between doping and precise gate placement at the heterojunction is challenging to achieve. Efforts to mitigate the dopant-induced band tails has been attempted previously in [84] by introducing the doping of the source segment 20 nm away from the tunnel junction. This approach, though resulted in an order of

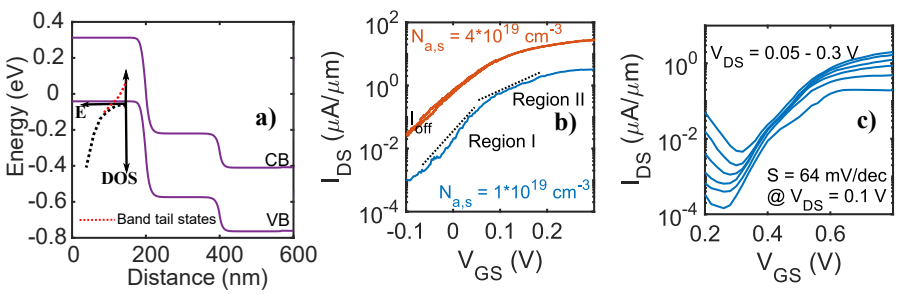

Figure 4.2: (a) Band diagram of a TFET in the on- state illustrating the effect of band tail density of states (DOS). The black dotted lines correspond the the DOS of the valence band and the red dotted lines extending into the bandgap correspond to the band tail DOS. (b) Transfer characteristics of highly doped and lowly doped TFET devices depicting the effects of source depletion (c) Transfer characteristics of a core-shell TFET with poor S, I_{ON} and I_{OFF}.

magnitude reduced I_{OFF} and steeper S , suffered from poor I_{ON} . To improve the on-state, TFET with a core-shell InGaAsSb-GaAsSb nanowire structure was developed during this thesis work with doping moved 120 nm further away from the tunnel junction in the core and 2x increased doping in the shell [85]. However, the resulting TFET in Fig 4.2 (c) demonstrated inferior performance to their predecessors which could be due to the non-optimal shell composition and the critical shell positioning that failed to achieve the desired band bending at the tunnel junction. The effect of band tails on the TFET device performance is further studied extensively in this thesis work using low temperature characterization, the inferences of which are discussed in Paper IV.

4.2 LOW TEMPERATURE/CRYOGENICS

At low temperatures, dopants in the semiconductor material freeze out reducing the trap density and increasing the mobility. Hence, operating transistors at low temperatures provides performance improvements and reduced noise levels useful as control and read-out electronics [86]. To understand the limitations of classical electronics at low temperatures, characterization techniques that measure the physics of carrier transport are necessary. A thorough investigation of the low temperature behavior of TFETs is presented in Paper IV.

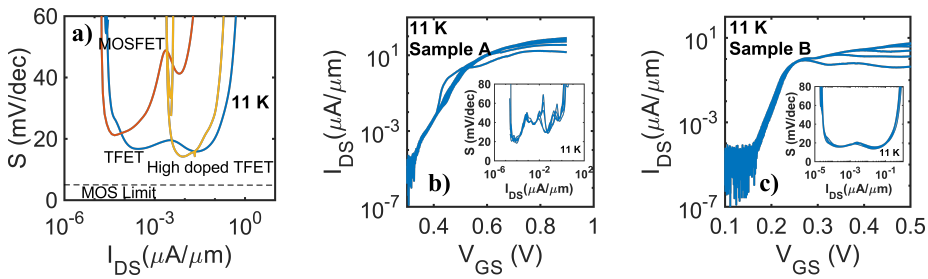

Figure 4.3: (a) The S behavior at 11 K for devices with different conductions mechanisms (nTFET, PMOS) and high doping concentration all reach a minimum value well above the MOS limit. (b) and (c) Transfer characteristics at 11 K of Sample A and B, respectively showing signs of quantization. The insets are the corresponding I_{DS} vs S plots.

4.2.1 SLOPE SATURATION

The theoretical limit of the subthreshold swing for a MOSFET is temperature dependent as given by $S(T)$ = m $\ln(10)$ $k_B T/q$. However, a FET measured at cryogenic temperatures usually demonstrates a non-ideal S which tends to saturate below a specific temperature to at least one order of magnitude higher than the limit. This phenomenon is common to all FETs processed during this thesis work irrespective of their structure and technology platform as seen in Fig 4.3 (a).

The research community initially attributed the observed characteristics entirely to interface traps close to the band edges. However, increasing the interface trap density to fit to the excess S resulted in unrealistic values exceeding the free carrier density of silicon suggesting D_{it} is not the only degrader of the slope. Recently, Bohuslavskyi et al. modelled the cryogenic saturation of S considering an exponential band tail in the density of states [87]. Beckers et al. revised the above model by incorporating the possibility of additional intrinsic mechanisms such as electron-phonon scattering, crystalline periodicity etc. as also responsible for the blurred band edges [88].

In this regard, samples produced during this thesis work reveal several slope regions as seen in the transfer characteristics in Fig 4.3 (b) and (c) at low temperatures which could be attributed to the effect of quantization in the source and channel regions. From previous studies on InAs/InGaAsSb heterojunctions published within the group, the band alignment has been seen to form a triangular well on the source side close to the tunnel junction [19]. The band offset between the wurtzite and zinc blende segments of the InAs channel has also been shown to create a triangular well. Hence both source and channel quantization may contribute to the observed features. Sample A showing several features of kinks in the subthreshold region of the transfer curve gives a higher S saturation value with the minimum S achieved only over a narrow current range. On the other hand, Sample B with several peaks observed only beyond the threshold voltage demonstrates a more constant S over a large current range suitable for circuit implementations. The features blur out with increasing temperature due to thermal broadening of the sub-bands in the source and channel and are hence not observed for room temperature measurements [89]. From this analysis, it can be concluded that though quantization does not drastically affect the S saturation value, it affects the operating range of a device limiting its applicability and hence this effect cannot be neglected. However, the kinks observed close to the off-state of the device could be due to contribution from individual trap states. Hence a more elaborate model to catch the effects of quantization and traps separately from the low temperature measurements is required.

4.2.2 BARRIER HEIGHT

The band structure of the fabricated devices needs to be experimentally evaluated to understand if the obtained band alignment is the same as intended. This assessment is crucial especially for TFETs where the existence of a potential barrier due to poor doping or misaligned metal contacts could lead to a MOSFET, controlled by thermionic emission connected in series with a tunnel junction, instead of a TFET [90]. The barrier height for current transport can be evaluated by studying the temperature dependence of the device current using Arrhenius plots from low as well as high temperature characterization as discussed in Paper I. A ballistic 1D transport model was adopted for the extraction of barrier height for all the samples in this thesis work [91]. Applying this technique in Paper I helped identify the existence of a large potential barrier at the drain-side of the gate underlapped TFET revealing the disadvantages of using a gate-underlap to suppress ambipolarity in TFETs. A similar approach was adopted in evaluating the band structure of the core-shell PMOS in Paper V. This analysis suggested that the V_{DS} dependence in the off- state indicates a non-optimal drain-side doping. Thus, by utilizing the above technique, it is possible to obtain an in-depth understanding of the nanowire growth as well as the device architecture.

4.3 RECONFIGURABLE DEVICES

For a small Au dot size and a given supply of the precursor material, the length of the nanowire increases with a similar volume as for a larger Au dot size. This results in the variation in length of the InAs segment w.r.t the Au diameter as seen in Fig 4.4 (a). At small diameter scales, the chemical potential of the precursor in the seed particle increases resulting in a reduction of material incorporation and decreased growth rate. This phenomenon known as Gibbs-Thomson effect is predominant in the growth of III-Sb nanowires resulting in a shorter InGaAsSb segment at small Au diameters [92].

All nanowires utilized in this thesis work had a similar diameter to length dependence of the nanowire segments. By designing the sample with different Au dot sizes and taking advantage of the variation in the length of the segments, regions on the die with PMOS-only devices, PMOS+ n-type TFET devices and TFET-only devices were developed using the fabrication process flow described in section 3.5. The band bending suitable for a PMOS-only and PMOS+NTFET operation is illustrated in Fig 4.4 (b) & (c), respectively. Note the difference in the gate placement for the two operations. The PMOS-only devices (Fig 4.4 (d)) exhibit good off-state and S while the poor I_{ON} can be attributed to the intrinsic segment of the source and the

low doping of the drain. For devices demonstrating both p- and n-type conduction (Fig 4.4 (e) & (f)), PMOS exhibits poor I_{OFF} probably due to leakage from tunneling from drain to channel as the tunnel barrier in this case is narrow. The TFET also demonstrates poor S and I_{ON} mainly due to InGaAsSb homojunction acting as a tunnel junction with insufficient source doping. Note that the source and drain terminals have been interchanged between the two FET types presented. This demonstration is a proof-of-concept showcasing the possibilities of the particular device architecture but further extensive improvements in performance and device configuration are necessary for its application.

4.4 BENCHMARKING

Different approaches are undertaken during this thesis work to improve the performance particular to the needs of the low-power applications such as

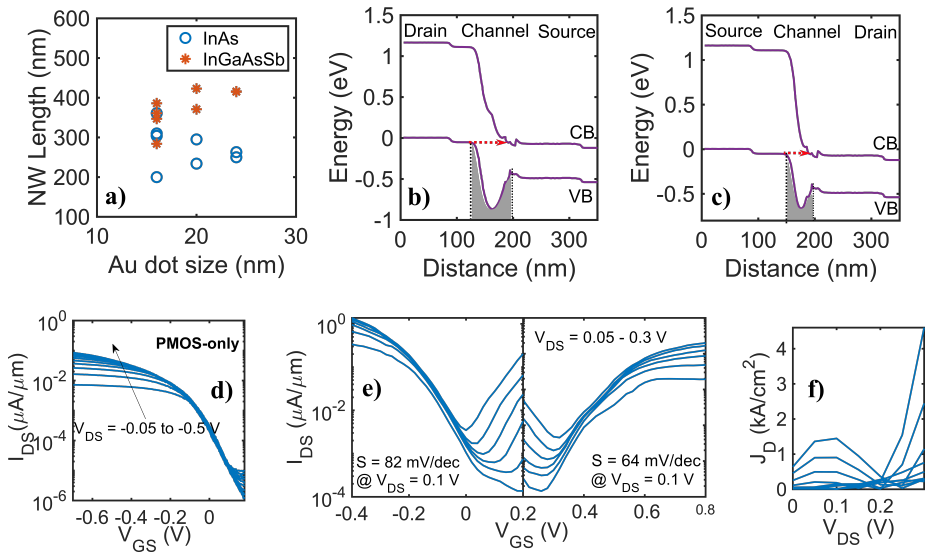

Figure 4.4: (a) The effect of the Au dot size on the length of the bottom InAs and top InGaAsSb segments of the nanowire. The InAs segment shortens while InGaAsSb segment gets longer with increasing Au diameter. (b) Band diagram of a core-shell nanowire demonstrating the band alignment suitable for (c) PMOS-only and (d) PMOS+ n-type TFET operations. Note that the S/D terminals are interchanged. Transfer characteristics of a device that exhibited (e) only PMOS behavior and (f) both PMOS and TFET behavior. (g) NDR characteristics measured confirming the TFET operation.

IoT discussed in section 1.1. In this regard sample matrices with nanowire growth variations and device design alterations were developed as described in chapter 3. The I_{ON}, I_{OFF} and S were the three main parameters targeted for improvement. The contribution of this thesis work to the research field of III-V NTFET and PMOS devices is summarized as benchmark plots highlighting the best performances achieved (Fig 4.6 and Fig 4.7).

To get an overview of the improvements achieved in the TFET device performance during this thesis, the work is categorized based on process development into different generations (Fig 4.5). For TFETs, the first generation focused on suppressing the ambipolar conduction and improving the off-state leakage currents. This involved replacing the SiO_x bottom spacer with resist spacer to realize a gate-drain underlap configuration. Despite achieving the intended reduction in I_{OFF}, the I_{ON} suffered due to the underlap (Paper I). The second generation of process development focused on improving the on-state performance while still suppressing the ambipolarity. This was achieved by varying the arsenic composition of the source while using a

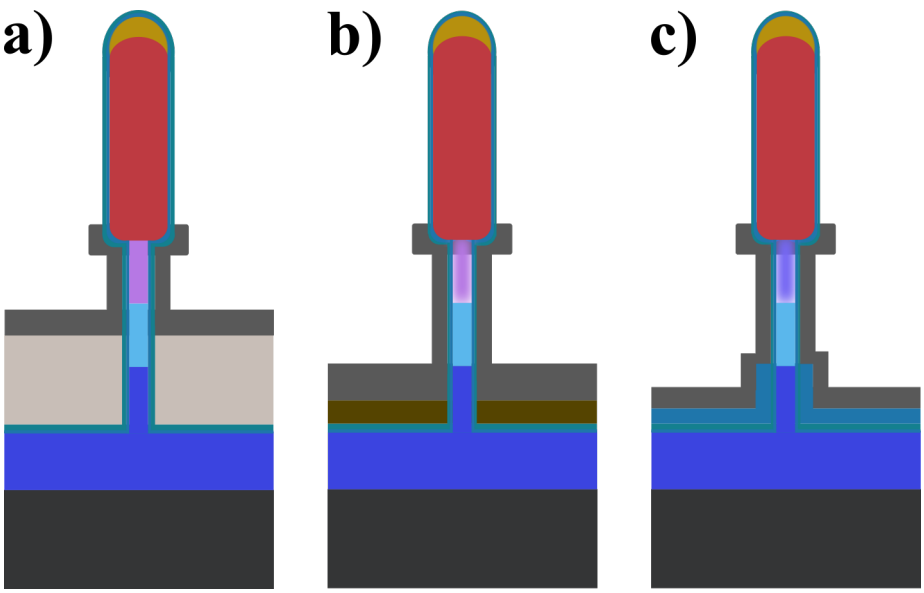

Figure 4.5: Schematic illustrations of the different generations of TFET devices developed during this thesis. (a) Device with organic spacer and a gate-drain underlap aiming to suppress I_{OFF}. (b) Device with reduced EOT, SiO_x spacer and varying arsenic composition in the quaternary source segment. (c) Device with Al_2O_3 bottom spacer field plate and varying indium composition in the quaternary source segment.

SiO_x bottom spacer (Paper II). The third generation focused on improving the performance further and achieving a steeper S which was accomplished by finding the optimum composition for indium at the source and using a

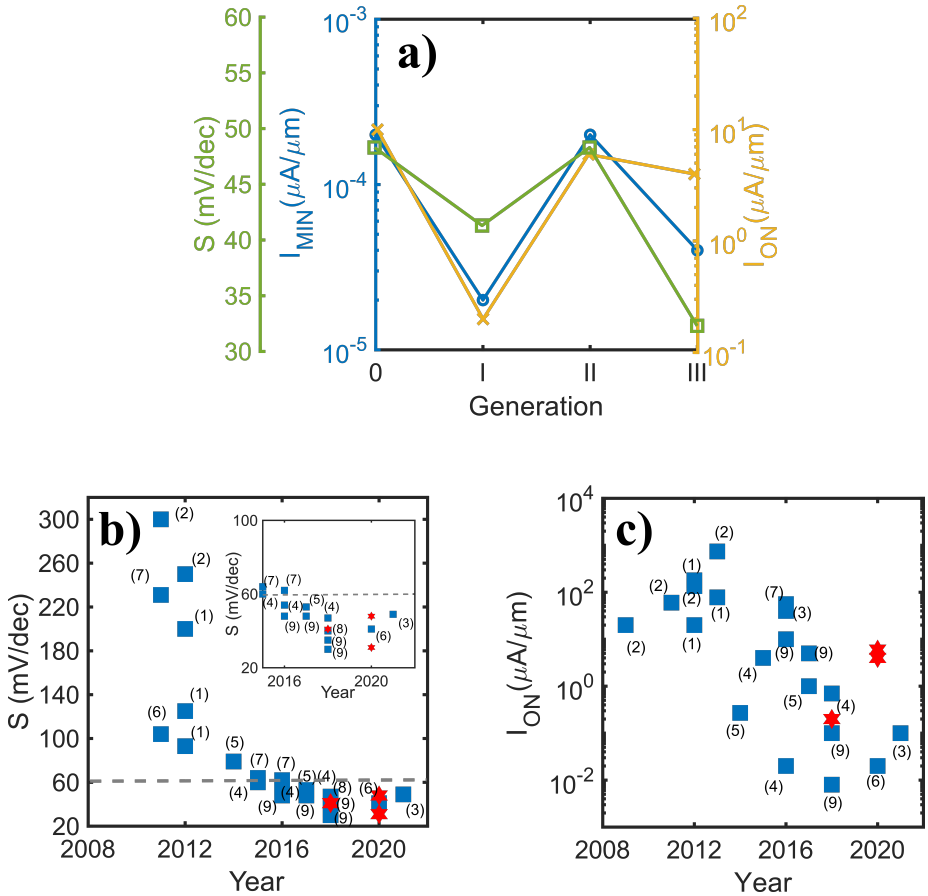

Figure 4.6: (a) The performance of the different generations of the TFETs developed during this project. Generation 0 implies the starting point of this project [39]. I_{ON} suffered in Generation I while I_{MIN} suffered in Generation II. A balance in performance had been achieved with Generation III. (b) S and (c) I_{ON} of the TFETs from this work (red stars) benchmarked against other III-V TFETs from the literature. Inset of (b) shows the zoomed plot. The numbers represent the research groups that reported the corresponding devices: (1) Notre Dame [27, 28, 93–95] (2) Penn state [29, 31, 96] (3) IBM [36, 97, 98] (4) IMEC [35,99,100] (5) MIT [34,101] (6) Hokkaido [37,102] (7) Tokyo [32,33,103] (8) TSMC [38] (9) Lund [39,84,104]

high-k bottom spacer that acted as a field plate (Paper III). Apart from the above highlighted devices, several intermediate samples were involved in the methodical study that paved the way towards upgrading each mentioned generation. In addition, core-shell TFETs were developed to study the impact of dopant induced defects on the TFET characteristics particularly at cryogenic temperatures.

The improvement in S with generations is evident from Fig 4.6 (a) while the I_{ON} has been maintained without drastic degradation. Generation 0 signifies the starting point for this thesis project [39]. The final generation demonstrated devices with sub-40 mV/dec switching with I_{OFF} 10x lower than Generation 0 and I_{ON} reduced only by 0.5x. The different generations are also benchmarked in Fig 4.6 (b) and (c) against the other III-V devices discussed in the state-of-the-art in section 2.3. Though devices developed before 2014 could reach high current levels, they unfortunately struggled to deliver steep switching. After 2015, more sub-60 mV/dec devices had been demonstrated with [39] delivering the best performance. This thesis work has worked towards reducing the S further without compromising the I_{ON} as shown in Fig 4.6 (c).

For PMOS, the device generation involved improving the gate electrostatics by moving from a more Sb-rich channel commonly adopted in the community to an InGaAsSb quarternary channel(Paper V). The outcome of this generation was an improved on/off ratio and a first demonstration of sub-100 mV/dec S (Fig 4.7) compared to the state-of-the art III-V PMOS discussed in section 2.3.

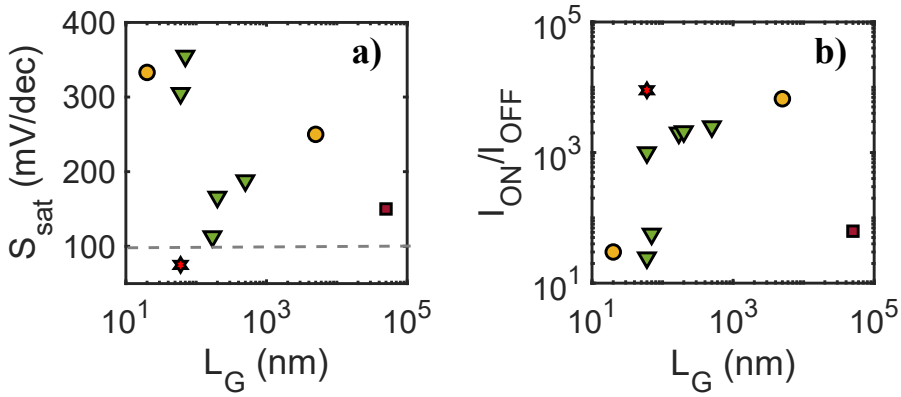

Figure 4.7: (a) Benchmarking of the PMOS device from this work (red star) against other III-V PMOS reported in literature. The green triangles are other vertical nanowire devices [50–52, 63–65], yellow circles are FinFETs [49, 66], and brown squares are wafer bonded devices [67].

Future work could focus on reducing the access resistance by engineering the dopants in the shell and the InAs drain while still maintaining the achieved S and I_{OFF}. Another option worth studying is the device performance by using the same core nanowire structure but without the shell to see the capabilities of the chosen channel.

5

Summary and Outlook

TRANSISTORS that can improve the energy efficiency of electronics have been explored in this thesis work using vertical InAs/InGaAsSb/GaSb heterostructure nanowires integrated on a Si substrate. Improvements in heterojunction band lineup (Paper II) and transistor device design (Paper I, Paper III) has helped achieve, to the best of our knowledge, the highest drive currents (I_{ON} = 4 μA/μm) for a sub-40 mV/dec (S = 32 mV/dec) TFET at a low operating voltage (V_{DS} = 0.3 V) and off- current (I_{OFF} = 1 nA/μm) with minimum current (I_{MIN} = 100 pA/μm). However, further improvements in device performance as stated in section 2.3 is needed for TFETs to find application in electronic devices.

When the TFET reaches such competitiveness at V_{DS} = 0.3 V, they can enable a reduction of the supply voltage by 2.3x from the current commercially available FinFET technology which could provide a 5.4x lower power consumption. Applications requiring low power and small devices such as in Internet of Medical Things (IoMT) can then benefit from this novel technology. We estimate that an Apple Watch offering continuous health monitoring that has a battery life of 18 hours using a 7nm FinFET platform if transferred to the TFET platform can operate with a battery life of 4 days. A portable glucose monitoring device, when connected for data transmission, loses 25-60% of its battery power which can then be reduced to 5-12% when the operating voltage is reduced with the presented technology. This could potentially increase the number of tests that can be performed, and data transmitted from the device before requiring recharging.

Although these steep slope devices demonstrate great potential for low power applications satisfying the requirement for standby power dissipation and low voltage operation, the achieved I_{ON} is, however, still about two orders of magnitude lower than that required for commercial use. Although sys-

tematic variations of the nanowire growth conditions were performed during this thesis work to understand the capabilities of the InAs/InGaAsSb/GaSb tunnel junction, further growth studies which includes variation in doping concentration could help identify the optimum band alignment to reach the required currents. However, past attempts to improve the current levels by increasing the source doping and engineering the band alignment by varying the source composition has in most cases resulted in degrading the off-state performance of the devices. A path forward worth detailed studying is the core-shell TFETs, the first generation of device fabrication process for which has been developed during this thesis. The gate-last process developed for these TFET structures could also help to understand if the contact resistance from the top of the nanowire was degrading R_{on} and I_{ON}.

The InGaAsSb channel PMOS studied during this project can be a promising material option for III-V p-type transistors and optimizing the doping in the nanowire structure is a straightforward step in the future to improve the currents. Short L_G below 60 nm have very rarely been attempted among the III-V PMOS reported due to their already high leakage currents. The better gate control observed from the InAs/InGaAsSb/GaSb PMOS provides an opportunity to scale L_G which could further improve the on-state performance. However, more work on improving the contacts to the Sb- segments and assessing the oxide-semiconductor interface quality is required to extract the full potential of this material structure.

The hybrid p- and n-type devices attempted in this work using a vertical core-shell nanowire and a single gate has demonstrated possibility to achieve reconfigurability at reduced footprint. However, the developed process needs to be extended to a dual gate structure in order to suppress the leakage currents. More detailed measurements and device modeling are required to understand the device functionality and to design application specific unit cells.

Though a lot of developments have happened in the field of III-V FETs in the past five years, several questions still remain. If a novel technology and a novel material system is to penetrate the semiconductor industry, it must demonstrate significant benefits not only from a performance standpoint but also economically to convince industry integration. Substantial efforts are necessary from the scientific community to accomplish this transformation, however the results achieved so far give hope that it would not be too long before we find these transistors in our day-to-day electronic devices.

Bibliography

[1] G. Fagas, J. P. Gallagher, L. Gammaitoni, and D. J. Paul, "Energy Challenges for ICT," *ICT - Energy Concepts for Energy Efficiency and Sustainability*, pp. 1–36, 2017.

[2] S. Lange, J. Pohl, and T. Santarius, "Digitalization and energy consumption. Does ICT reduce energy demand?" *Ecological economics*, vol. 176, p. 106760, 2020. doi: 10.1016/j.ecolecon.2020.106760

[3] P. Wang, P. Zhong, M. Yu, Y. Pu, S. Zhang, and P. Yu, "Trends in energy consumption under the multi-stage development of ICT: Evidence in China from 2001 to 2030," *Energy Reports*, vol. 8, pp. 8981–8995, 2022. doi: 10.1016/j.egyr.2022.07.003

[4] Z. Abbas and M. Olivieri, "Impact of technology scaling on leakage power in nano-scale bulk CMOS digital standard cells," *Microelectronics Journal*, vol. 45, no. 2, pp. 179–195, 2014. doi: https://doi.org/10.1016/j.mejo.2013.10.013

[5] R. Xie, P. Montanini, K. Akarvardar, N. Tripathi, B. Haran, S. Johnson, T. Hook, B. Hamieh, D. Corliss, J. Wang *et al.*, "A 7nm FinFET technology featuring EUV patterning and dual strained high mobility channels," IEEE. IEEE International Electron Devices Meeting (IEDM), 2016. doi: 10.1109/IEDM.2016.7838334 pp. 2–7.

[6] C. H. Jan, U. Bhattacharya, R. Brain, S. J. Choi, G. Curello, G. Gupta, W. Hafez, M. Jang, M. Kang, K. Komeyli *et al.*, "A 22nm SoC platform technology featuring 3-D tri-gate and high-k/metal gate, optimized for ultra low power, high performance and high density SoC applications." IEEE International Electron Devices Meeting (IEDM), 2012. doi: 10.1109/IEDM.2012.6478969

[7] H. Mertens, R. Ritzenthaler, A. Hikavyy, M. S. Kim, Z. Tao, K. Wostyn, S. A. Chew, A. D. Keersgieter, G. Mannaert, E. Rosseel *et al.*, "Gate-All-Around MOSFETs based on vertically stacked horizontal Si nanowires in a replacement metal gate process on bulk Si substrates." IEEE Symposium on VLSI Technology, 2016. doi: 10.1109/VLSIT.2016.7573416 pp. 1–2.

[8] N. Loubet, T. Hook, P. Montanini, C. W. Yeung, S. Kanakasabapathy, M. Guillom, T. Yamashita, J. Zhang, X. Miao, J. Wang *et al.*, "Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET." IEEE Symposium on VLSI Technology, 2017. doi: 10.23919/VLSIT.2017.7998183 pp. T230–T231.

[9] H. Jagannathan, B. Anderson, C. Sohn, G. Tsutsui, K.-I. Seo, and H. Bu, "Vertical-Transport Nanosheet Technology for CMOS Scaling beyond Lateral-Transport Devices." IEEE International Electron Devices Meeting (IEDM), 2021. doi: 10.1109/IEDM19574.2021.9720561 pp. 557–560.

[10] "IEEE IRDS More Moore," 2021.

[11] J. A. D. Alamo, "Nanometre-scale electronics with III-V compound semiconductors," *Nature*, vol. 479, pp. 317–323, 2011. doi: 10.1038/nature10677

[12] A. Nainani, B. R. Bennett, J. Brad Boos, M. G. Ancona, and K. C. Saraswat, "Enhancing hole mobility in III-V semiconductors," *Journal of Applied Physics*, vol. 111, no. 10, p. 103706, 2012.

[13] S. Natarajan, M. Agostinelli, S. Akbar, M. Bost, A. Bowonder, V. Chikarmane, S. Chouksey, A. Dasgupta, K. Fischer, Q. Fu *et al.*, "A 14nm logic technology featuring 2nd-generation FinFET, air-gapped interconnects, self-aligned double patterning and a 0.0588 μm2 SRAM cell size." IEEE International Electron Devices Meeting (IEDM), 2015. doi: 10.1109/IEDM.2014.7046976 pp. 3.7.1–3.7.3.

[14] A. M. Ionescu, T. Rosca, C. Alper, E. Polytechnique, and F. D. Lausanne, "Steep Slope Transistors for Quantum Computing," *2018 IEEE 2nd Electron Devices Technology and Manufacturing Conference (EDTM)*, vol. 1, pp. 56–58, 2018.

[15] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, pp. 329–337, 2011. doi: 10.1038/nature10679

[16] L. Esaki, "New Phenomenon in Narrow Germanium p-n junction," *Phys. Rev.*, vol. 109, pp. 603–604, Jan 1958. doi: 10.1103/PhysRev.109.603

[17] J. Knoch, "Optimizing tunnel FET performance - Impact of device structure, transistor dimensions and choice of material." IEEE International Symposium on VLSI Technology, Systems, and Applications, 2009. doi: 10.1109/VTSA.2009.5159285 pp. 45–46.

[18] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2095–2110, 2010. doi: 10.1109/JPROC.2010.2070470

[19] E. Memisevic, M. Hellenbrand, E. Lind, A. R. Persson, S. Sant, A. Schenk, J. Svensson, R. Wallenberg, and L.-E. Wernersson, "Individual Defects in InAs/InGaAsSb/GaSb Nanowire Tunnel Field-Effect Transistors Operating below 60 mV/decade," *Nano Letters*, vol. 17, pp. 4373–4380, 2017. doi: 10.1021/acs.nanolett.7b01455

[20] Q. T. Zhao, S. Richter, C. Schulte-Braucks, L. Knoll, S. Blaeser, G. V. Luong, S. Trellenkamp, A. Schafer, A. Tiedemann, J. M. Hartmann *et al.*, "Strained Si and SiGe nanowire tunnel FETs for logic and analog applications," *IEEE Journal of the Electron Devices Society*, vol. 3, pp. 103–114, 2015. doi: 10.1109/JEDS.2015.2400371

[21] F. Silveira, D. Flandre, and P. G. Jespers, "A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 1314–1319, 1996. doi: 10.1109/4.535416

[22] W. G. Vandenberghe, A. S. Verhulst, B. SorÃl'e, W. Magnus, G. Groeseneken, Q. Smets, M. Heyns, and M. V. Fischetti, "Figure of merit for and identification of sub-60 mV/decade devices," *Applied Physics Letters*, vol. 102, 2013. doi: 10.1063/1.4773521

[23] L. D. Michielis, L. Lattanzio, and A. M. Ionescu, "Understanding the superlinear onset of tunnel-fet output characteristic," *IEEE Electron Device Letters*, vol. 33, pp. 1523–1525, 2012. doi: 10.1109/LED.2012.2212175

[24] J. Appenzeller, Y. M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube field-effect transistors," *Physical Review Letters*, vol. 93, 2004. doi: 10.1103/PhysRevLett.93.196805

[25] C. Convertino, C. B. Zota, H. Schmid, A. M. Ionescu, and K. E. Moselund, "III-V heterostructure tunnel field-effect transistor," *Journal of Physics Condensed Matter*, vol. 30, 2018. doi: 10.1088/1361-648X/aac5b4

[26] L. Knoll, Q.-T. Zhao, A. Nichau, S. Trellenkamp, S. Richter, A. Schafer, D. Esseni, L. Selmi, K. K. Bourdelle, and S. Mantl, "Inverters With Strained Si Nanowire Complementary Tunnel Field-Effect Transistors," *IEEE Electron Device Letters*, vol. 34, pp. 813–815, 2013. doi: 10.1109/LED.2013.2258652

[27] G. Zhou, Y. Lu, R. Li, Q. Zhang, Q. Liu, T. Vasen, H. Zhu, J. M. Kuo, T. Kosel, M. Wistey *et al.*, "InGaAs/InP tunnel FETs with a subthreshold swing of 93 mV/dec and I_{ON}/I_{OFF} ratio near 10^6," *IEEE Electron Device Letters*, vol. 33, pp. 782–784, 2012. doi: 10.1109/LED.2012.2189546

[28] R. Li, Y. Lu, G. Zhou, Q. Liu, S. D. Chae, T. Vasen, W. S. Hwang, Q. Zhang, P. Fay, T. Kosel *et al.*, "AlGaSb/InAs tunnel field-effect transistor with on-current of 78 μA/μm at 0.5 V," *IEEE Electron Device Letters*, pp. 363–365, 2012. doi: 10.1109/LED.2011.2179915

[29] S. Mookerjea, D. Mohata, R. Krishnan, J. Singh, A. Vallett, A. Ali, T. Mayer, V. Narayanan, D. Schlom, A. Liu *et al.*, "Experimental demonstration of 100nm channel length In0.53Ga 0.47As-based vertical interband tunnel field effect transistors (TFETs) for ultra low-power logic and SRAM applications." IEEE International Electron Devices Meeting (IEDM), 2009. doi: 10.1109/IEDM.2009.5424355

[30] D. Mohata, B. Rajamohanan, T. Mayer, M. Hudait, J. Fastenau, D. Lubyshev, A. W. Liu, and S. Datta, "Barrier-engineered arsenide-antimonide heterojunction tunnel FETs with enhanced drive current," *IEEE Electron Device Letters*, vol. 33, pp. 1568–1570, 2012. doi: 10.1109/LED.2012.2213333

[31] R. Bijesh, H. Liu, H. Madan, D. Mohata, W. Li, N. V. Nguyen, D. Gundlach, C. A. Richter, J. Maier, K. Wang *et al.*, "Demonstration of In0.9Ga0.1As/GaAs0.18Sb0.82 near broken-gap tunnel FET with I_{ON}=740 μA/μm, G_M=70 μS/μm and gigahertz switching performance at V_{DS}=0.5V." IEEE International Electron Devices Meeting (IEDM), 2013. doi: 10.1109/IEDM.2013.6724708 pp. 28.2.1–28.2.4.

[32] R. Iida, S. H. Kim, M. Yokoyama, N. Taoka, S. H. Lee, M. Takenaka, and S. Takagi, "Planar-type In0.53G 0.47As channel band-to-band tunneling metal-oxide-semiconductor field-effect transistors," *Journal of Applied Physics*, vol. 110, 2011. doi: 10.1063/1.3668120

[33] M. Noguchi, S. Kim, M. Yokoyama, O. Ichikawa, T. Osada, M. Hata, M. Takenaka, and S. Takagi, "High I_{on}/I_{off} and low subthreshold slope planar-type InGaAs tunnel field effect transistors with Zn-diffused source junctions," *Journal of Applied Physics*, vol. 118, pp. 045 712.1–045 712.15, 2015. doi: 10.1063/1.4927265

[34] X. Zhao, A. Vardi, and J. A. del Alamo, "Sub-Thermal Subthreshold Characteristics in Top-Down InGaAs/InAs Heterojunction Vertical Nanowire Tunnel FETs," *IEEE Electron Device Letters*, vol. 38, pp. 855–858, 7 2017. doi: 10.1109/LED.2017.2702612

[35] A. Alian, S. E. Kazzi, A. Verhulst, A. Milenin, N. Pinna, T. Ivanov, D. Lin, D. Mocuta, and N. Collaert, "Record 47 mV/dec top-down vertical nanowire InGaAs/GaAsSb tunnel FETs." IEEE Symposium on VLSI Technology, 2018. doi: 10.1109/VLSIT.2018.8510619 pp. 133–134.

[36] K. E. Moselund, H. Schmid, C. Bessire, M. T. Bjork, H. Ghoneim, and H. Riel, "InAs-Si nanowire heterojunction tunnel FETs," *IEEE Electron Device Letters*, vol. 33, pp. 1453–1455, 2012. doi: 10.1109/LED.2012.2206789

[37] K. Tomioka, H. Gamo, J. Motohisa, and T. Fukui, "Vertical gate-all-around tunnel FETs using InGaAs nanowire/Si with core-multishell structure." IEEE International Electron Devices Meeting (IEDM), 2020. doi: 10.1109/IEDM13553.2020.9371991 pp. 21.1.1–21.1.4.

[38] T. Vasen, P. Ramvall, A. Afzalian, G. Doornbos, M. Holland, C. Thelander, K. A. Dick, L. E. Wernersson, and M. Passlack, "Vertical Gate-All-Around Nanowire GaSb-InAs Core-Shell n-Type Tunnel FETs," *Nature Scientific Reports*, vol. 9, pp. 1–9, 1 2019. doi: 10.1038/s41598-018-36549-z

[39] E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind, and L. E. Wernersson, "Vertical InAs/GaAsSb/GaSb tunneling field-effect transistor on Si with S = 48 mV/decade and I_{on} = 10 μa/μm for I_{off} = 1 nA/μm at V_{DS} = 0.3 V." IEEE International Electron Devices Meeting (IEDM), 2017. doi: 10.1109/IEDM.2016.7838450 pp. 19.1.1–19.1.4.

[40] M. Heyns, A. Alian, G. Brammertz, M. Caymax, Y. C. Chang, L. K. Chu, B. D. Jaeger, G. Eneman, F. Gencarelli, G. Groeseneken *et al.*, "Advancing CMOS beyond the Si roadmap with Ge and III/V devices." IEEE International Electron Devices Meeting (IEDM), 2011. doi: 10.1109/IEDM.2011.6131543 pp. 13.1.1–13.1.4.

[41] Y. Kamata, "High-k/Ge MOSFETs for future nanoelectronics," *Elsevier Materials today*, vol. 11, pp. 30–38, 2008.

[42] L. Witters, H. Arimura, F. Sebaai, A. Hikavyy, A. P. Milenin, R. Loo, A. D. Keersgieter, G. Eneman, T. Schram, K. Wostyn *et al.*, "Strained Germanium Gate-All-Around pMOS Device Demonstration Using Selective Wire Release Etch Prior to Replacement Metal Gate Deposition," *IEEE Transactions on Electron Devices*, vol. 64, pp. 4587–4593, 11 2017. doi: 10.1109/TED.2017.2756671

[43] E. Capogreco, L. Witters, H. Arimura, F. Sebaai, C. Porret, A. Hikavyy, R. Loo, A. P. Milenin, G. Eneman, P. Favia *et al.*, "First demonstration of vertically stacked gate-all-around highly strained germanium nanowire pFETs," *IEEE Transactions on Electron Devices*, vol. 65, pp. 5145–5150, 2018. doi: 10.1109/TED.2018.2871595

[44] W. Rachmady, "300mm Heterogeneous 3D Integration of Record Performance Layer Transfer Germanium PMOS with Silicon NMOS for Low Power High Performance Logic Applications." IEEE Internation Electron Devices Meeting (IEDM), 2019. doi: 10.1109/IEDM19573.2019.8993626 pp. 29.7.1–29.7.4.

[45] M. Radosavljevic, T. Ashley, A. Andreev, S. D. Coomber, G. Dewey, M. T. Emeny, M. Fearn, D. G. Hayes, K. P. Hilton, M. K. Hudait *et al.*, "High-performance 40nm gate length InSb P-channel compressively strained quantum well field effect transistors for low-power (V_{CC}=0.5V) logic applications." IEEE International Electron Devices Meeting (IEDM), 2008. doi: 10.1109/IEDM.2008.4796798 pp. 1–4.

[46] B. R. Bennett, M. G. Ancona, J. B. Boos, and B. V. Shanabrook, "Mobility enhancement in strained p-InGaSb quantum wells," *Applied Physics Letters*, vol. 91, pp. 042 104.1– 042 104.3, 2007. doi: 10.1063/1.2762279

[47] J. Nah, H. Fang, C. Wang, K. Takei, M. H. Lee, E. Plis, S. Krishna, and A. Javey, "III-V complementary metal-oxide-semiconductor electronics on silicon substrates," *Nano Letters*, vol. 12, pp. 3592–3595, 2012. doi: 10.1021/nl301254z

[48] M. Yokoyama, H. Yokoyama, M. Takenaka, and S. Takagi, "InGaSb-on-insulator p-channel metal-oxide-semiconductor field-effect transistors on Si fabricated by direct wafer bonding," *Journal of Applied Physics*, vol. 125, pp. 114 501.1–114 501.9, 2019. doi: 10.1063/1.5049518

[49] W. Lu, I. P. Roh, D.-M. Geum, S.-H. Kim, J. D. Song, L. Kong, and J. A. del Alamo, "10-nm Fin-width InGaSb p-channel self-aligned FinFETs using antimonide-compatible digital etch." IEEE International Electron Devices Meeting (IEDM), 2017. doi: 10.1109/IEDM.2017.8268412. ISBN 978-1-5386-3559-9 pp. 17.7.1–17.7.4.

[50] A. Jonsson, J. Svensson, E. Lind, and L. E. Wernersson, "Gate-Length Dependence of Vertical GaSb Nanowire p-MOSFETs on Si," *IEEE Transactions on Electron Devices*, vol. 67, pp. 4118–4122, 2020. doi: 10.1109/TED.2020.3012126

[51] Z. Zhu, A. Jonsson, Y. P. Liu, J. Svensson, R. Timm, and L. E. Wernersson, "Improved Electrostatics through Digital Etch Schemes in Vertical GaSb Nanowire p-MOSFETs on Si," *ACS Applied Electronic Materials*, vol. 4, pp. 531–538, 2022. doi: 10.1021/acsaelm.1c01134

[52] A. Jonsson, J. Svensson, and L. E. Wemersson, "Balanced Drive Currents in 10-20 nm Diameter Nanowire All-III-V CMOS on Si." IEEE International Electron Devices Meeting (IEDM), 2019. doi: 10.1109/IEDM.2018.8614685. ISBN 9781728119878. ISSN 01631918 pp. 39.3.1–39.3.4.

[53] M. W. Larsson, J. B. Wagner, M. Wallin, P. Hakansson, L. E. Froberg, L. Samuelson, and L. R. Wallenberg, "Strain mapping in free-standing heterostructured wurtzite InAs/InP nanowires," *Nanotechnology*, vol. 18, pp. 1–8, 2007. doi: 10.1088/0957-4484/18/1/015504

[54] A. Greene, S. Madisetti, P. Nagaiah, M. Yakimov, V. Tokranov, R. Moore, and S. Oktyabrsky, "Improvement of the GaSb/Al 2O 3 interface using a thin InAs surface layer," *Solid-State Electronics*, vol. 78, pp. 56–61, 2012. doi: 10.1016/j.sse.2012.05.049

[55] P. Caroff, M. E. Messing, B. M. Borg, K. A. Dick, K. Deppert, and L. E. Wernersson, "InSb heterostructure nanowires: MOVPE growth under extreme lattice mismatch," *Nanotechnology*, vol. 20, pp. 1–7, 2009. doi: 10.1088/0957-4484/20/49/495606

[56] J. D. Christesen, C. W. Pinion, X. Zhang, J. R. McBride, and J. F. Cahoon, "Encoding abrupt and uniform dopant profiles in vapor-liquid-solid nanowires by suppressing the reservoir effect of the liquid catalyst," *ACS Nano*, vol. 8, pp. 11 790–11 798, 11 2014. doi: 10.1021/nn505404y

[57] P. Xie, Y. Hu, Y. Fang, J. Huang, and C. M. Lieber, "Diameter-dependent dopant location in silicon and germanium nanowires," *Proceedings of the National Academy of Sciences*, vol. 106, no. 36, pp. 15 254–15 258, 2009. doi: 10.1073/pnas.0906943106

[58] M. T. Bjork, H. Schmid, J. Knoch, H. Riel, and W. Riess, "Donor deactivation in silicon nanostructures," *Nature nanotechnology*, vol. 4, no. 2, pp. 103–107, 2009. doi: 10.1038/nnano.2008.400

[59] M. Hale, S. Yi, J. Sexton, A. Kummel, and M. Passlack, "Scanning tunneling microscopy and spectroscopy of gallium oxide deposition and oxidation on GaAs(001)-c(2$\times$ 8)/(2$\times$ 4)," *The Journal of Chemical Physics*, vol. 119, no. 13, pp. 6719–6728, 2003.

[60] J. Robertson and B. Falabretti, "Band offsets of high K gate oxides on III-V semiconductors," *Journal of Applied Physics*, vol. 100, no. 1, p. 014111, 2006. doi: 10.1063/1.2213170

[61] C. L. Hinkle, A. M. Sonnet, E. M. Vogel, S. McDonnell, G. J. Hughes, M. Milojevic, B. Lee, F. S. Aguirre-Tostado, K. J. Choi, H. C. Kim *et al.*, "GaAs interfacial self-cleaning by atomic layer deposition," *Applied Physics Letters*, vol. 92, pp. 071 901.1–071 901.3, 2008. doi: 10.1063/1.2883956

[62] R. Timm, A. Fian, M. Hjort, C. Thelander, E. Lind, J. N. Andersen, L. E. Wernersson, and A. Mikkelsen, "Reduction of native oxides on InAs by atomic layer deposited Al2O3 and HfO2," *Applied Physics Letters*, vol. 97, pp. 132 904.1–132 904.3, 2010. doi: 10.1063/1.3495776

[63] A. Jonsson, J. Svensson, and L. E. Wernersson, "A self-aligned gate-last process applied to All-III-V CMOS on Si," *IEEE Electron Device Letters*, vol. 39, pp. 935–938, 2018. doi: 10.1109/LED.2018.2837676

[64] Z. Zhu, J. Svensson, A. Jonsson, and L. Wernersson, "Performance enhancement of GaSb vertical nanowire p-type MOSFETs on Si by rapid thermal annealing," *Nanotechnology*, vol. 33, no. 7, pp. 1–10, 2022. doi: 10.1088/1361-6528/ac3689

[65] K. H. Goh, K. H. Tan, S. Yadav, Annie, S. F. Yoon, G. Liang, X. Gong, and Y. C. Yeo, "Gate-all-around CMOS (InAs n-FET and GaSb p-FET) based on vertically-stacked nanowires on a Si platform, enabled by extremely-thin buffer layer technology and common gate stack and contact modules." IEEE International Electron Devices Meeting (IEDM), 2015. doi: 10.1109/IEDM.2015.7409704 pp. 15.4.1–15.4.4.

[66] Z. Yuan, A. Kumar, C. Y. Chen, A. Nainani, B. R. Bennett, J. B. Boos, and K. C. Saraswat, "Antimonide-based heterostructure p-channel MOSFETs with Ni-alloy source/drain," *IEEE Electron Device Letters*, vol. 34, pp. 1367–1369, 2013. doi: 10.1109/LED.2013.2280615

[67] M. Yokoyama, H. Yokoyama, M. Takenaka, and S. Takagi, "III-V single structure CMOS by using ultrathin body InAs/GaSb-OI channels on Si," *IEEE Symposium on VLSI Technology*, vol. 5, pp. 1–2, 2014. doi: 10.1109/VLSIT.2014.6894350

[68] H. Xing, Y. Dora, A. Chini, S. Heikman, S. Keller, and U. K. Mishra, "High breakdown voltage AlGaN-GaN HEMTs achieved by multiple field plates," *IEEE Electron Device Letters*, vol. 25, pp. 161–163, 2004. doi: 10.1109/LED.2004.824845

[69] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, "Suppression of dynamic on-resistance increase and gate charge measurements in high-voltage GaN-HEMTs with optimized field-plate structure," *IEEE Transactions on Electron Devices*, vol. 54, pp. 1825–1830, 2007. doi: 10.1109/TED.2007.901150

[70] K. Nishi, M. Yokoyama, S. Kim, H. Yokoyama, M. Takenaka, and S. Takagi, "Study on electrical properties of metal/GaSb junctions using metal-GaSb alloys," *Journal of Applied Physics*, vol. 115, pp. 034 515.1–034 515.7, 2014. doi: 10.1063/1.4862486

[71] J. Knoch and J. Appenzeller, "Modeling of high-performance p-type IIIV heterojunction tunnel FETs," *IEEE Electron Devices Letters*, vol. 31, pp. 305–307, 2010. doi: 10.1109/LED.2010.2041180

[72] A. S. Verhulst, W. G. Vandenberghe, K. Maex, and G. Groeseneken, "Boosting the on-current of a n -channel nanowire tunnel field-effect transistor by source material optimization," *Journal of Applied Physics*, vol. 104, pp. 064 514.1–064 514.10, 2008. doi: 10.1063/1.2981088

[73] M. Berg, O. P. Kilpi, K. M. Persson, J. Svensson, M. Hellenbrand, E. Lind, and L. E. Wernersson, "Electrical characterization and modeling of gate-last vertical InAs nanowire MOSFETs on Si," *IEEE Electron Device Letters*, vol. 37, pp. 966–969, 2016. doi: 10.1109/LED.2016.2581918

[74] T. Mikolajick, G. Galderisi, M. Simon, S. Rai, A. Kumar, A. Heinzig, W. M. Weber, and J. Trommer, "20 Years of reconfigurable field-effect transistors: From concepts to future applications," *Solid-State Electronics*, vol. 186, pp. 1–4, 2021. doi: 10.1016/j.sse.2021.108036

[75] P. Wu, D. Reis, X. S. Hu, and J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics*, vol. 4, pp. 45–53, 2021. doi: 10.1038/s41928-020-00511-7

[76] N. Oliva, J. Backman, L. Capua, M. Cavalieri, M. Luisier, and A. M. Ionescu, "WSe2/SnSe2 vdW heterojunction Tunnel FET with sub-thermionic characteristic and MOSFET co-integrated on same WSe2 flake," *npj 2D Materials and Applications*, vol. 4, pp. 1–8, 2020. doi: 10.1038/s41699-020-0142-2

[77] M. Simon, B. Liang, D. Fischer, M. Knaut, A. Tahn, T. Mikolajick, and W. M. Weber, "Top-Down Fabricated Reconfigurable FET with Two Symmetric and High-Current On-States," *IEEE Electron Device Letters*, vol. 41, pp. 1110–1113, 2020. doi: 10.1109/LED.2020.2997319

[78] M. von Haartman and M. Ostling, *Low Frequency Noise in Advanced MOS Devices*. Springer, 2007. ISBN 9781402059278

[79] J. Kwon, A. Prakash, S. R. Das, and D. B. Janes, "Correlating Electronic Transport and 1/ f Noise in MoSe2 Field-Effect Transistors," *Physical Review Applied*, vol. 10, pp. 064 029.1–064 029.14, 2018. doi: 10.1103/PhysRevApplied.10.064029

[80] M. Hellenbrand, O. P. Kilpi, J. Svensson, E. Lind, and L. E. Wernersson, "Low-frequency noise in nanowire and planar III-V MOSFETs," *Microelectronic Engineering*, vol. 215, pp. 1–5, 2019. doi: 10.1016/j.mee.2019.110986

[81] P. V. Mieghem, "Theory of band tails in heavily doped semiconductors," *Reviews of Modern Physics*, vol. 64, pp. 755–793, 1992. doi: 10.1103/RevModPhys.64.755

[82] M. A. Khayer and R. K. Lake, "Effects of band-tails on the subthreshold characteristics of nanowire band-to-band tunneling transistors," *Journal of Applied Physics*, vol. 110, pp. 074 508.1–074 508.6, 2011. doi: 10.1063/1.3642954

[83] C. Anghel, A. Gupta, A. Amara, S. Member, and A. Vladimirescu, "30-nm tunnel fet with improved performance and reduced ambipolar current," *IEEE Transactions on Electron Devices*, vol. 58, pp. 1649–1654, 2011. doi: 10.1109/TED.2011.2128320

[84] E. Memisevic, J. Svensson, E. Lind, and L.-E. Wernersson, "Impact of source doping on the performance of vertical InAs/InGaAsSb/GaSb nanowire tunneling field-effect transistors," *Nanotechnology*, vol. 29, p. 435201, 2018. doi: 10.1088/1361-6528/aad949

[85] J. L. Boland, S. Conesa-Boj, P. Parkinson, G. Tutuncuoglu, F. Matteini, D. Ruffer, A. Casadei, F. Amaduzzi, F. Jabeen, C. L. Davies *et al.*, "Modulation doping of GaAs/AlGaAs core-shell nanowires with effective defect passivation and high electron mobility," *Nano Letters*, vol. 15, pp. 1336–1342, 2015. doi: 10.1021/nl504566t

[86] S. J. Pauka, K. Das, R. Kalra, A. Moini, Y. Yang, M. Trainer, A. Bousquet, C. Cantaloube, N. Dick, G. C. Gardner *et al.*, "A cryogenic CMOS chip for generating control signals for multiple qubits," *Nature Electronics*, vol. 4, pp. 64–70, 1 2021. doi: 10.1038/s41928-020-00528-y

[87] H. Bohuslavskyi, A. G. Jansen, S. Barraud, V. Barral, M. CassÃľ, L. L. Guevel, X. Jehl, L. Hutin, B. Bertrand, G. Billiot *et al.*, "Cryogenic subthreshold swing saturation in fd-soi mosfets described with band broadening," *IEEE Electron Device Letters*, vol. 40, pp. 784–787, 5 2019. doi: 10.1109/LED.2019.2903111

[88] A. Beckers, F. Jazaeri, and C. Enz, "Theoretical limit of low temperature subthreshold swing in field-effect transistors," *IEEE Electron Device Letters*, vol. 41, pp. 276–279, 2 2020. doi: 10.1109/LED.2019.2963379

[89] C. B. Zota, D. Lindgren, L. E. Wernersson, and E. Lind, "Quantized Conduction and High Mobility in Selectively Grown InxGa1-xAs Nanowires," *ACS Nano*, vol. 9, pp. 9892–9897, 2015. doi: 10.1021/acsnano.5b03318

[90] F. Giannazzo, G. Fisichella, A. Piazza, S. D. Franco, G. Greco, S. Agnello, and F. Roccaforte, "Impact of contact resistance on the electrical properties of MoS2 transistors at practical operating temperatures," *Beilstein Journal of Nanotechnology*, vol. 8, pp. 254–263, 2017. doi: 10.3762/bjnano.8.28

[91] A. Rahman, J. Guo, S. Datta, and M. S. Lundstrom, "Theory of ballistic nanotransistors," *IEEE Transactions on Electron Devices*, vol. 50, no. 9, pp. 1853–1864, 2003. doi: 10.1109/TED.2003.815366

[92] M. Ek, B. M. Borg, J. Johansson, and K. A. Dick, "Diameter limitation in growth of III-Sb-containing nanowire heterostructures," *ACS Nano*, vol. 7, pp. 3668–3675, 2013. doi: 10.1021/nn400684p

[93] G. Zhou, R. Li, T. Vasen, M. Qi, S. Chae, Y. Lu, Q. Zhang, H. Zhu, J.-M. Kuo, T. Kosel *et al.*, "Novel gate-recessed vertical InAs/GaSb TFETs with record high I_{ON} of 180 μA/μm at V_{DS} = 0.5 V." IEEE International Electron Devices Meeting, 2012. doi: 10.1109/IEDM.2012.6479154 pp. 32.6.1–32.6.4.

[94] G. Zhou, Y. Lu, R. Li, Q. Zhang, W. Hwang, Q. Liu, T. Vasen, H. Zhu, J. Kuo, S. Koswatta *et al.*, "Self-aligned InAs/Al0.45Ga0.55Sb vertical tunnel FETs," in *69th Device Research Conference*, 2011. doi: 10.1109/DRC.2011.5994499 pp. 205–206.

[95] R. Li, Y. Lu, S. D. Chae, G. Zhou, Q. Liu, C. Chen, M. Shahriar Rahman, T. Vasen, Q. Zhang, P. Fay *et al.*, "InAs/AlGaSb heterojunction tunnel field-effect transistor with tunnelling in-line with the gate field," *physica status solidi c*, vol. 9, no. 2, pp. 389–392, 2012.

[96] D. K. Mohata, R. Bijesh, Y. Zhu, M. K. Hudait, R. Southwick, Z. Chbili, D. Gundlach, J. Suehle, J. M. Fastenau, D. Loubychev *et al.*, "Demonstration of improved heteroepitaxy, scaled gate stack and reduced interface states enabling heterojunction tunnel FETs with high drive current and high on-off ratio." IEEE Symposium on VLSI Technology, 2012. doi: 10.1109/VLSIT.2012.6242457 pp. 53–54.

[97] D. Cutaia, K. E. Moselund, H. Schmid, M. Borg, A. Olziersky, and H. Riel, "Complementary III-V heterojunction lateral NW Tunnel FET technology on Si." IEEE Symposium on VLSI Technology, 2016. doi: 10.1109/VLSIT.2016.7573444 pp. 1–2.

[98] C. Convertino, C. B. Zota, H. Schmid, D. Caimi, L. Czornomaz, A. M. Ionescu, and K. E. Moselund, "A hybrid III-V tunnel FET and MOSFET technology platform integrated on silicon," *Nature Electronics*, vol. 4, pp. 162–170, 2021. doi: 10.1038/s41928-020-00531-3

[99] A. Alian, J. Franco, A. Vandooren, Y. Mols, A. Verhulst, S. E. Kazzi, R. Rooyackers, D. Verreck, Q. Smets, A. Mocuta *et al.*, "Record performance InGaAs homo-junction TFET with superior SS reliability over MOSFET." IEEE International Electron Devices Meeting (IEDM), 2015. doi: 10.1109/IEDM.2015.7409811 pp. 31.7.1–31.7.4.

[100] A. Alian, Y. Mols, C. C. M. Bordallo, D. Verreck, A. Verhulst, A. Vandooren, R. Rooyackers, P. G. D. Agopian, J. A. Martino, A. Thean *et al.*, "InGaAs tunnel FET with sub-nanometer EOT and sub-60 mV/dec subthreshold swing at room temperature," *Applied Physics Letters*, vol. 109, p. 243502, 2016. doi: 10.1063/1.4971830

[101] X. Zhao, A. Vardi, and J. A. del Alamo, "InGaAs/InAs heterojunction vertical nanowire tunnel fets fabricated by a top-down approach." IEEE International Electron Devices Meeting (IEDM), 2014. doi: 10.1109/IEDM.2014.7047108 pp. 25.5.1–25.5.4.

[102] K. Tomioka and T. Fukui, "Tunnel field-effect transistor using InAs nanowire/Si heterojunction," *Applied Physics Letters*, vol. 98, p. 083114, 2011. doi: 10.1063/1.3558729

[103] D. H. Ahn, S. Ji, M. Takenaka, and S. Takagi, "Performance improvement of InxGa1-xAs Tunnel FETs with Quantum Well and EOT scaling," in *2016 IEEE Symposium on VLSI Technology*, 2016. doi: 10.1109/VLSIT.2016.7573443 pp. 1–2.

[104] E. Memisevic, J. Svensson, E. Lind, and L. E. Wernersson, "Vertical Nanowire TFETs with Channel Diameter Down to 10 nm and Point S_{MIN} of 35 mV/Decade," *IEEE Electron Device Letters*, vol. 39, pp. 1089–1091, 2018. doi: 10.1109/LED.2018.2836862

APPENDICES

A

Fabrication of Vertical Nanowire Field-Effect Transistor

ALL nanowire growth in this thesis work must be accredited to Dr. Johannes Svensson and Zhongyunshen Zhu. The samples were fabricated on a lightly p-doped 1 cm^2 Si substrates with an epitaxially grown 260 nm thick Sn-doped n^{++}InAs buffer layer. The Au-seed particles were patterned using EBL followed by metal deposition and lift-off. At the time of this thesis the above process step was perfomed at Chalmers University. InAs/InGaAsSb/GaSb heterostructure vertical nanowires were grown using Sn for n-doping the InAs segment and Zn for doping the Sb-segments. Detailed information and data regarding growth can be obtained from the above mentioned growers. The following text describes the details of the process steps involved in the fabrication of vertical nanowire transistors.

SAMPLE CLEANING BEFORE NANOWIRE GROWTH

The 4-inch Au-patterned wafer from Chalmers is protected with photoresist before dicing it into 1 cm^2 sample dies which must then be cleaned before nanowire growth.

- Clean the sample in acetone at 50°C for 15 min.
- Transfer the sample to a beaker with fresh acetone and place in ultrasonic power bath for 10 min.
- Rinse the sample in fresh acetone followed by IPA.
- Clean the sample using O_2 plasma ashing in Plasma Preen with metal cage for 15 s at 5 mbar.

DIGITAL ETCHING

- Inspect the grown nanowires in the SEM.
- To etch the InAs segment:
  - Oxidize the nanowire using O_3 at 50°C for 5 min.
  - Wet-etch the sample in citric acid for 30 s.
  - Rinse in H_2O for 30 s.
  - Rinse in IPA for 30 s.
- To etch the InGaAsSb segment:
  - Oxidize the nanowire using O_2 atmosphere within the ozone cleaner at room temperature.
  - Wet-etch the sample in pre-mixed HCl:IPA 1:10 for 30 s.
  - Rinse in IPA for 30 s.
- Monitor the thickness of the nanowire in SEM between the etch cycles.

GATE OXIDE AND BOTTOM SPACER DEPOSITION

- Load the sample into the ALD Savannah immediately after the last digital etch cycle.
- Surface cleaning using 5 cycles TMAl.
- Deposit 5 cycles of Al_2O_3 at 300°C.
- Deposit 27 cycles of HfO_2 at 120°C.
- Deposit 100 cycles of Al_2O_3 at 120°C.
- Monitor in SEM to confirm deposition thickness.

BOTTOM SPACER DEFINITION

- Spin coat the sample with S1813 photoresist at 60 s, 4000 rpm.
- Hard-bake the resist on a hotplate at 120°C for 15 min.
- Etch S1813 in RIE-Trion using O_2 plasma at 15 sccm, 300 mTorr and 50 W to the desired length of the spacer. Etch rate is ideally 0.7 nm/s and vary depending on chamber conditions.
- Monitor in SEM at constant intervals for the desired length.
- Wet-etch Al_2O_3 in HF 1:400 for 25 s.
- Remove resist by rinsing in acetone followed by IPA.

GATE FORMATION

- Sputter 30 nm W in AJA Orion at 16 sccm Ar-flow and 100 W DC power with rotation.
- Gate length definition:
  - Spin coat the sample with S1813 photoresist at 60 s, 4000 rpm.
  - Hard-bake the resist on a hotplate at 120°C for 15 min.
  - Etch S1813 in RIE-Trion using O_2 plasma at 15 sccm, 300 mTorr and 50 W to the desired length of the spacer.
  - Monitor in SEM at constant intervals for the desired length.
  - Etch W in RIE-Trion using SF_6:Ar at 45/10 sccm, 140 W and 185 mTorr for 45 s.
  - Remove etch residues in Plasma Preen using O_2 plasma ashing for 30 s.
  - Remove resist by rinsing in acetone followed by IPA.
- Gate pad definition
  - Spin coat the sample with S1813 photoresist at 60 s, 4000 rpm.
  - Soft-bake the resist on a hotplate at 115°C for 90 s.
  - Pattern the gate pad using UV lithography for 5 s.
  - Stir the sample in MF 319 developer for 60-70 s.
  - Rinse in H_2O.
  - Hard-bake resist on hotplate at 120°C for 15 min.
  - Etch W in RIE-Trion using SF_6:Ar at 45/10 sccm, 140 W and 185 mTorr for 45 s.
  - Remove etch residues in Plasma Preen using O_2 plasma ashing for 30 s.
  - Remove resist by rinsing in acetone followed by IPA.

TOP SPACER FORMATION

- Spin coat the sample with S1813 photoresist at 60 s, 4000 rpm.
- Permanent-bake the resist on a hotplate at 200°C for 25 min.
- Etch S1813 in RIE-Trion using O_2 plasma at 15 sccm, 300 mTorr and 50 W to the desired length of the spacer.
- Monitor in SEM at constant intervals for the desired length.

VIA-HOLE FORMATION FOR CONTACT PADS

- Spin coat the sample with S1813 photoresist at 60 s, 4000 rpm.

- Soft-bake the resist on a hotplate at 115°C for 90 s.
- Pattern the gate and drain via-holes using UV lithography for 5 s.
- Stir the sample in MF 319 developer for 60-70 s.
- Rinse in H_2O.
- Hard-bake resist on hotplate at 120°C for 15 min.
- Etch the top spacer in the via-holes in RIE-Trion using O_2 plasma at 15 sccm, 300 mTorr and 50 W.
- Remove resist by rinsing in acetone followed by IPA.
- Spin coat the sample with S1813 photoresist at 60 s, 4000 rpm.
- Soft-bake the resist on a hotplate at 115°C for 90 s.
- Pattern the drain via-hole using UV lithography for 5 s.
- Stir the sample in MF 319 developer for 60-70 s.
- Rinse in H_2O.
- Hard-bake resist on hotplate at 120°C for 15 min.
- Remove the trilayer high-k oxide in the via-hole using HF 1:400 for 3 min 45 s.
- Remove resist by rinsing in acetone followed by IPA.

TOP CONTACT

- Remove the bilayer high-k oxide on top of the nanowire using HF 1:400 for 3 min 20 s.
- Load the sample immediately into the sputter AJA Orion deposition chamber.
- Sputter 10nm Ni at 9 sccm Ar-flow and 100 W DC power with rotation.
- Sputter 150 nm Au at 9 sccm Ar-flow and 100 W DC power with rotation.
- Spin coat the sample with S1813 photoresist at 60 s, 4000 rpm.
- Soft-bake the resist on a hotplate at 115°C for 90 s.
- Pattern the contact pads using UV lithography for 5 s.
- Stir the sample in MF 319 developer for 60-70 s.
- Rinse in H_2O.
- Hard-bake resist on hotplate at 120°C for 15 min.
- Wet-etch Au using KI-based etchant for 15-20 s.
- Wet-etch Ni using 1:2.5:2.5:5 CH_3COOH:HNO_3:H_2SO_4:H_2O for 40 s.
- Remove resist by rinsing in acetone followed by IPA.

B

Fabrication of Core-Shell Vertical Nanowire Field-Effect Transistors

This appendix contains the process steps specific to fabrication of transistor from core-shell vertical nanowire. Only those steps different from the standard process described in Appendix A is discussed here. The first step in fabricating with a core-shell nanowire is to define the shell edge and top metal to the top segment of the nanowire, the details of which are as follows.

- Deposit 100 cycles of Al_2O_3 sacrificial layer at 120°C using ALD-Savannah.
- Spin coat the sample with S1813 photoresist at 60 s, 4000 rpm.
- Hard-bake the resist on a hotplate at 120°C for 15 min.
- Etch S1813 in RIE-Trion using O_2 plasma at 15 sccm, 300 mTorr and 50 W to the desired length of the spacer.
- Monitor in SEM at constant intervals for the desired length.
- Wet-etch Al_2O_3 in HF 1:400 for 25 s.
- Sputter 30 nm W in AJA Orion at 16 sccm Ar-flow and 100 W DC power with rotation.
- Etch the planar W layer in ICP-RIE using 25:20 sccm SF_6:N_2 with ICP power 300 W and RF power 30 W at 5 mTorr.
- Remove etch residues in Plasma Preen using O_2 plasma ashing for 30 s.
- Remove resist by rinsing in acetone followed by IPA.
- Remove Al_2O_3 sacrificial layer from the bottom segment of the nanowire by etching in HF 1:400 for 25 s.

Following the above steps, the process flow described in Appendix A can be continued to fabricate the transistors.