Infrared Photodetectors based on InSb and InAs Nanostructures via Heterogeneous Integration-Rapid Melt Growth and Template Assisted Selective Epitaxy

Menon, Heera

2023

Infrared Photodetectors based on InSb and InAs Nanostructures via Heterogeneous Integration

Rapid Melt Growth and Template Assisted Selective Epitaxy

HEERA MENON
DEPARTMENT OF ELECTRICAL AND INFORMATION TECHNOLOGY
FACULTY OF ENGINEERING | LTH | LUND UNIVERSITY

Infrared Photodetectors based on InSb and InAs Nanostructures via Heterogeneous Integration

Rapid Melt Growth and Template Assisted Selective Epitaxy

Doctoral Thesis

Heera Menon

Thesis Supervisor:
Assoc. Prof. Mattias Borg

LUND UNIVERSITY

Department of Electrical and Information Technology
Lund, June 2023

Academic thesis for the degree of Doctor of Philosophy, which, by due permission of the Faculty of Engineering at Lund University, will be publicly defended on Friday, 09 June 2023, at 9:15 a.m. in lecture hall E:1406, Department of Electrical and Information Technology, Ole Römers Väg 3, 223 63 Lund, Sweden. The thesis will be defended in English.

The Faculty Opponent will be Bernardette Kunert, Principal Scientist from Imec.

Organization:
LUND UNIVERSITY
Department of Electrical and
Information Technology
Ole Römers Väg 3
223 63 Lund
Sweden

Author:
Heera Menon

Document Type:
DOCTORAL THESIS

Date of Issue:
May 2023

Sponsoring Organisation(s):
Swedish Foundation for Strategic Research (SSF)
Crafoord Foundation
Royal Physiographic Society of Lund
NanoLund

Title:
Infrared Photodetectors based on InSb and InAs Nanostructures via Heterogeneous Integration-
Rapid Melt Growth and Template Assisted Selective Epitaxy

Abstract:
Monolithic heterogeneous integration of III-V semiconductors with the contemporary Si Complementary Metal Oxide Semiconductor (CMOS) technology has instigated a wide range of possibilities and functionalities in the semiconductor industry, in the field of digital circuits, optical sensors, light emitters, and high-frequency communication devices. However, the integration of III-V semiconductors is not trivial due to the differences in lattice parameters, polarity, and thermal expansion coefficient. This thesis explores two integration techniques to form III-V nanostructures with potential applications in the infrared detection field.
The first technique implemented in this thesis work is the Rapid Melt Growth technique. InSb, which has a large lattice mismatch (19%) to Si, is used to demonstrate the RMG integration technique. A flash lamp with a millisecond annealing technique is utilized to melt and recrystallize amorphous InSb material to form a single crystalline material. The development of the fabrication process and the experimental results for obtaining a single crystalline InSb-on-insulator from a Si seed area through the RMG process are presented. Electron Back Scatter Diffraction (EBSD) technique was employed to understand the crystal quality, orientation, and defects in the RMG InSb nanostructures. The InSb nanostructures have a resistivity of 10 mΩ cm, similar to the VLS-grown InSb nanowires. Mobility ranging from 3490 - 877 cm^2/ V sec was extracted through Hall and Van der Pauw measurements. Finally, we report the first monolithic integrated InSb nanostructure photodetector on Si through the RMG process. Detailed optical and electrical characterization of the device, including the spectrally resolved photocurrent and the temperature-dependent dark current, is studied. The thesis presents an InSb photodetector with a stable photodetector with a responsivity of 0.5 A/W at 16 nW illumination and millisecond time response.
The second integration technique implemented in this thesis work is Template Assisted Selective Epitaxy. Here, the versatility of TASE technique to integrate InAs nanowires on W metal seed is demonstrated. This technique enables the feasibility of integrating III-V semiconductors to back -end of the line integration with Si CMOS technology. EBSD technique was utilized to study and obtain the statistics on the single crystalline InAs nanowires grown from different diameter templates. We also demonstrate the possibility of achieving an nBn InAs detector using TASE on W approach. This technique is a promising step towards developing high operating temperature (HOT) monolithic integrated mid-infrared detectors. Thus, the results of this thesis provide the perspective into two viable CMOS-compatible III-V integration techniques that could be utilized for photodetector applications at a reduced cost.

Keywords:
Rapid Melt Growth, Template Assisted Selective Epitaxy, InAs, InSb, EBSD, Photodetector

Classification System and/or Index Terms
e.g. Electronic Engineering, Nano Technology

Language:
English

Supplementary Bibliographical Information:
–

ISBN (printed):
978-91-8039-721-6

Key title and ISSN:
Series of Licentiate and Doctoral Theses; 1654-790X, No. 158

ISBN (digital):
978-91-8039-722-3

Recipient's Notes:

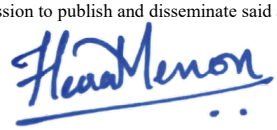
Number of Pages: 181

Price:

Security Classification:
Unclassified

General Permissions:

I, the undersigned, being the copyright owner and author of the above-mentioned thesis and its abstract, hereby grant to all reference sources permission to publish and disseminate said abstract.

Signature: *Heera Menon*  *Date:* 09 May 2023

Infrared Photodetectors based on InSb and InAs Nanostructures via Heterogeneous Integration

Rapid Melt Growth and Template Assisted Selective Epitaxy

Doctoral Thesis

Heera Menon

LUND
UNIVERSITY

Department of Electrical and
Information Technology
Lund, June 2023

Heera Menon
Department of Electrical and Information Technology
Lund University
Ole Römers Väg 3, 223 63 Lund, Sweden

Series of Licentiate and Doctoral Thesis
ISSN 1654-790X, No.158.
ISBN 978-91-8039-721-6 (print)
ISBN 978-91-8039-722-3 (electronic)

Cover image: Pattern generated using EBSD Z map of RMG single crystal InSb

Printed by Tryckeriet in E-huset, Lund University, Lund, Sweden.

To my Anu, who has inspired and encouraged me to chase my dreams.

To my parents, who have raised me to who I am today and for being a constant pillar of support.

Abstract

Monolithic heterogeneous integration of III-V semiconductors with the contemporary Si Complementary Metal Oxide Semiconductor (CMOS) technology has instigated a wide range of possibilities and functionalities in the semiconductor industry, in the field of digital circuits, optical sensors, light emitters, and high-frequency communication devices. However, the integration of III-V semiconductors is not trivial due to the differences in lattice parameters, polarity, and thermal expansion coefficient. This thesis explores two integration techniques to form III-V nanostructures with potential applications in the infrared detection field.

The first technique implemented in this thesis work is the Rapid Melt Growth technique. InSb, which has a large lattice mismatch (19 %) to Si, is used to demonstrate the RMG integration technique. A flash lamp with a millisecond annealing technique is utilized to melt and recrystallize amorphous InSb material to form a single crystalline material. The development of the fabrication process and the experimental results for obtaining a single crystalline InSb-on-insulator from a Si seed area through the RMG process are presented. Electron Back Scatter Diffraction (EBSD) technique was employed to understand the crystal quality, orientation, and defects in the RMG InSb nanostructures. The InSb nanostructures have a resistivity of 10 mΩ cm, similar to the VLS-grown InSb nanowires. Mobility ranging from 3490 - 877 cm^2/ V sec was extracted through Hall and Van der Pauw measurements. Finally, we report the first monolithic integrated InSb nanostructure photodetector on Si through the RMG process. Detailed optical and electrical characterization of the device, including the spectrally resolved photocurrent and the temperature-dependent dark current, is studied. The thesis presents an InSb photodetector with a stable photodetector with a responsivity of 0.5 A/W at 16 nW illumination and millisecond time response.

The second integration technique implemented in this thesis work is Template Assisted Selective Epitaxy. Here, the versatility of TASE technique to integrate InAs nanowires on W metal seed is demonstrated. This technique enables the feasibility of integrating III-V semiconductors to back -end of the line integration with Si CMOS technology. EBSD technique was

utilized to study and obtain the statistics on the single crystalline InAs nanowires grown from different diameter templates. We also demonstrate the possibility of achieving an nBn InAs detector using TASE on W approach. This technique is a promising step towards developing high operating temperature (HOT) monolithic integrated mid-infrared detectors. Thus, the results of this thesis provide the perspective into two viable CMOS-compatible III-V integration techniques that could be utilized for photodetector applications at a reduced cost.

Popular Science Article

Infrared radiation is an electromagnetic wave in a wavelength region longer than the visible light wavelength. All kinds of objects emit infrared radiation, which is invisible to the human eye. For example, a human body at 37 °C radiates infrared energy. One would require a material sensitive to infrared radiation to detect it. Infrared detection is used in several applications in science, communication, medicine, agriculture, industry, military, and remote sensing from space. For instance, in the optical communication system, infrared radiation is used to measure the light intensity from the lasers. They are used in flame monitors to detect light from flames. They are used to detect automobile exhaust gases like carbon monoxide (CO) and carbon dioxide (CO_2), emission control gases like CO and nitrogen dioxide (NO_2), and fuel leakage gases like methane (CH_4). Infrared imaging systems can be used to detect seawater pollution by oil. Scientific applications where water resources, currents, and volcanoes can be studied using infrared radiation. Infrared imaging diagnosis in the medical field and night vision cameras use infrared imaging detection systems.

The commercialized state-of-the-art material for infrared detectors is mercury cadmium telluride (HgCdTe or MCT). The detection range can be varied significantly by tuning the cadmium content in MCT. However, MCT detectors are costly, and the Restriction of Hazardous Substances (RoHS) of the European Union regulates the allowed concentration of mercury and cadmium in electronic devices. Hence, the researchers are looking into alternative materials for infrared detection. Furthermore, the III-V semiconductors do not contain RoHS-restricted substances; therefore, they can be fabricated from infrared photodetectors.

Silicon (Si) semiconductor is the base of any electronic devices and growing III-V semiconductors on Si (monolithic heterogeneous integration) would effectively reduce the cost of manufacturing infrared detectors. In addition, such an integration technique would reduce the size of detector elements, increase the number of detector elements incorporated in a chip and thus improve the performance of the infrared detector. This thesis demonstrates two integration techniques of III-V semiconductors – Rapid Melt Growth (RMG) and Template Assisted Selective Epitaxy technique (TASE).

Indium Antimony (InSb), a III-V semiconductor, is used to demonstrate the fabrication of high-quality InSb on Si using the RMG technique. In the RMG technique, an amorphous InSb (low electrical conductivity) is deposited on a stack containing Si single crystalline (high electrical conductivity) and an insulating material layer (IL1). Next, InSb is made to contact the Si through a small opening. The InSb is then covered by an insulating layer (IL2). The final stack of materials containing Si, IL1, InSb and IL2 is heated to the melting point of InSb, causing the InSb to melt and subsequently cool. On cooling, the melt encounters the Si through the nanometer opening and grows into a single crystalline InSb. This single crystalline InSb is then fabricated into an infrared detector, and the properties and performance of the detector are studied.

Indium Arsenide (InAs), another III-V semiconductor, is used to demonstrate the growth of single crystalline InAs on metallic surfaces using the TASE technique. In TASE technique, vapors of Indium (In) and Arsenic (As) raw materials are used to grow nanowires inside a hollow nanotube fabricated using an insulating material. The nanotube's bottom is exposed to a metallic surface. The atoms from the vapors get collected at this metallic surface, creating a single crystalline InAs nanowire. A barrier detector can be fabricated by introducing another material inside the InAs nanowire. The InAs nanowire and the barrier detector's material and electrical properties are also studied.

Overall, the research demonstrates the possibility of integrating single crystalline InSb and InAs on Si and metallic surfaces using RMG and TASE techniques. In addition, the insights gained from this study would be valuable for future infrared detection systems.

Acknowledgments

The five years of my Ph.D. journey have been a roller coaster ride filled with emotions of all kinds, hard work, struggles, perseverance, and successes. The journey wouldn't be complete without sharing my gratitude towards each of you who have been a part of this journey. Firstly, I would like to thank my main supervisor Mattias Borg for believing in me and providing this learning opportunity. I have always respected your guidance and support and have been inspired by your hard work and encouragement throughout my Ph.D. journey. Your upright comments during our weekly meetings and in the manuscripts have pushed me to think independently and have carved a confident researcher in me. I am deeply indebted to you. Your invaluable insights and feedback have been instrumental in shaping this thesis.

I would also like to extend my thanks to my co-supervisors, Lars-Erik Wernersson and Johannes Svensson, for their valuable contributions and expertise. Johannes, you have always kept your doors open for endless discussions and doubts of mine, and I am grateful to have had such insightful conversations with you. Lars-Erik, I have always admired your people and leadership skills. I am grateful for the valuable advice and guidance you have given me.

I enjoyed meeting and getting acquainted with a few interesting characters during this journey. Stefan and Sam, you have been my great friends, and our time spent together has always helped me in distress. I hope this is just the beginning of our friendship era. Abhinaya and Pradheebha, you were a great source of comfort during this journey. I will miss our time together, having endless conversations, and I hope we stay in contact. Gautham and Navya, thank you for all the impromptu badminton sessions and for staying late in the lab with me, even during the weekends, whenever I needed a lab buddy. I also would like to thank Sebastian, Olli-Pekka, Fredrik, Markus, Adam, Karl-Magnus, Lasse, Anton, Saketh, Zhongyunshen, Marcus, Hannes, Ben, Philipp, Anette, Patrik, Andre, Louise for being kind and supportive colleagues and for all the interesting conversations during our lunch breaks. Robin, I have always enjoyed our scientific discussions inside and outside the lab and thank you for all your support with the TEM lamella preparation. I would also like to thank all my colleagues for creating a good work

atmosphere and sharing their opinions and experience when needed – Erik, Lars, Daniel, Mats, Niklas, Ngoc, Alexandros, and Johan. Thanks to the personnel at the administration department- Stefan, Linda, Erik Jonsson, Erik Gothe, Elisabeth Nordström, and Elisabeth Ohlsson for all your help on any administrative matter.

I want to acknowledge all collaborators (Matthew Steer, Anna, Nick, Hossein, Håkan, Crispin, Sebastian, and Jonas) in my thesis work for their support and assistance. Their willingness to share their knowledge and skills has greatly enriched my experience and facilitated the progress of this research. I would also like to express my gratitude towards all the engineers and technicians in the Lund Nano lab for their constant efforts in tool operations and maintenance. Thank you, Mariusz, George, Emil, Håkan, Dmitry, Sarah, Alex, Elvedin, Peter, Anders, and Natalia, for all the help you provided when I had difficulties in the lab.

I would also like to express my heartfelt appreciation to my family, whose unwavering love, encouragement, and support have been the bedrock of my academic and personal journey. Their sacrifices and understanding have enabled me to pursue my dreams and achieve this significant milestone. Finally, and most importantly, I would like to thank my husband, Anoop, for his constant support, patience, and understanding throughout this journey. His encouragement and unconditional love have been a continuous source of inspiration and motivation.

Contents

Preface

This thesis is the culmination of five years of work in the Electromagnetics & Nanoelectronics division at the Department of Electrical and Information Technology at Lund University. The work was supervised by Associate Professor Mattias Borg (main supervisor), Dr. Johannes Svensson (assistant supervisor), and Professor Lars-Erik Wernersson (assistant supervisor).

Structure of the thesis

The thesis is divided into three main parts. The first section presents a background on the various challenges of heterogeneous integration techniques, different types of integration techniques, and a brief discussion on infrared detectors. Following this section, the research on the RMG of InSb is presented along with the results of the first monolithic integrated InSb photodetector on Si. The figure of merits, such as the spectral response, responsivity, and response time of the photodetector, is investigated in this chapter. The third section will explore the results of the InAs TASE on W metal, where the crystallinity of the InAs is studied in detail using EBSD. The orientation relationship between the nucleated InAs and the underlying W seed is also investigated. Finally, the initial promising results of the InAs barrier detectors are also presented.

Introduction

The main body of the thesis consists of the publications appended in the back. The Introduction provides a more comprehensive view than the very focused publications and ties their work together. The Introduction is intended to be understandable for aspiring researchers with a master's degree in physics or a related subject.

Appendix

Thermodynamic modeling of RMG process

This section provides a detailed description of the thermodynamic modeling of the RMG process conducted.

Papers

The papers forming the main body of the thesis are reproduced in the back and listed in the following.

It should be noted that our collaborators at Glasgow university and EPFL carried out the growth technique of MBE. The optical characterization was done by our collaborators at Halmstad University.

Included Papers

The following form is the main body of this thesis, and the respective published or draft versions are appended in the back.

Paper I

Improved quality of InSb-on-insulator microstructures by flash annealing into melt, **Heera Menon**, Lasse Södergren, Robin Athle, Jonas Johansson, Matthew Steer, Iain Thayne, and Mattias Borg. *Nanotechnology*, 2021, **32**, 165602

I wrote the paper, fabricated the sample, and did material characterization, electrical characterization, and data analysis.

Paper II

Fabrication of single-crystalline InSb-on-insulator by rapid melt growth, **Heera Menon**, Nicholas Paul Morgan, Crispin Hetherington, Robin Athle, Matthew Steer, Iain Thayne, Anna Fontcuberta i Morral, and Mattias Borg. *Phys. Status Solidi A*, 2022, **219**, 1 —8

I wrote the paper, fabricated the samples, did material characterization, did electrical characterization, and did data analysis.

Paper III

Monolithic InSb nanostructure photodetectors on Si using rapid melt growth, **Heera Menon**, Hossein Jeddi, Nicholas Paul Morgan, Anna Fontcuberta i Morral, Håkan Pettersson and Mattias Borg, *Nanoscale Adv.***,** 2023,**5**, 1152-1162

I wrote the paper, fabricated the devices, did material characterization, did electrical characterization and did all the data analysis involved in the project.

Paper IV

Three-Dimensional Integration of InAs Nanowires by Template-Assisted Selective Epitaxy on Tungsten, Johannes Svensson [*], Patrik Olausson, **Heera Menon**, Sebastian Lehmann, Erik Lind, Mattias Borg, *Nano Lett.*-under revision

I was actively involved in discussions regarding growth, processing, and discussions regarding the data, did the EBSD measurements and analysis throughout the project, did EDX measurements, prepared TEM lamella, and was actively involved in discussions regarding the TEM data. I also took part in writing the paper.

Related Work

The following publications are not included in the thesis, but a list of studies I was involved in is presented. The work is divided into peer-reviewed journal papers and conference contributions.

Journal Papers

Paper V

Effects of TiN Top Electrode Texturing on Ferroelectricity in $Hf_{1-x}Zr_xO2$*,* Robin Athle, Anton E. O. Persson, Austin Irish, **Heera Menon**, Rainer Timm, and Mattias Borg, *ACS Applied Materials & Interfaces.,2021,* 13, 9, p. 11089-11095 7 p.

I did the EDS measurement and analysis.

Paper VI

Cubic, hexagonal and tetragonal FeGex phases (x = 1, 1.5, 2): Raman spectroscopy and magnetic properties, Anna Kúkoľová, Mirjana Dimitrievska, Alexander. P. Litvinchuk, Santhanu Panikar Ramanandan, Nicolas Tappy, **Heera Menon**, Mattias Borg, Dirk Grundler and Anna Fontcuberta i Morral, 2021 Oct 7, *CrystEngComm.* 23, 37, p. 6506-6517 12 p.

I helped with FLA experiments and SEM imaging in the Lund Nano Lab clean room.

Paper VII

Directed Self-Assembly for Dense Vertical III–V Nanowires on Si and Implications for Gate All-Around Deposition Anette Löfstrand, Reza Jafari Jam, Johannes Svensson, Adam Jönsson, **Heera Menon**, Daniel Jacobsson, Lars-Erik Wernersson, Ivan Maximov, 2022, *Advanced Electronic Materials*. 8, 9, 2101388.

I did EDS measurement and analysis.

Conference contributions

Paper VIII

Template-Assisted Selective Epitaxy of InAs on W, Johannes Svensson, Patrik Olausson, **Heera Menon**, Erik Lind and Mattias Borg, 2022*, Compound Semiconductor Week, CSW 2022.*

I was actively involved in discussions regarding growth, processing, and discussions regarding the data, did the EBSD measurements and analysis throughout the project, did EDX measurements, prepared TEM lamella, and was actively involved in discussions regarding the TEM data.

Paper IX

Integration of InSb-on-Insulator Microstructures on Si by Flash Annealing into Melt, **Heera Menon**, Nicholas Paul Morgan, Crispin Hetherington, Robin Athle, Matthew Steer, Iain Thayne, Anna Fontcuberta i Morral, and Mattias Borg, *2021 Compound Semiconductor Week, CSW 2021.*

I fabricated the samples, did material characterization, did electrical characterization, did data analysis and presented the work at the conference via an oral presentation.

Paper X

Integration of InSb on Si by Rapid Melt Growth, **Heera Menon**, Matthew Steer, Iain Thayne, Johannes Svensson, Lars-Erik Wernersson and Mattias Borg, 2019, 21st International Vacuum Congress, IVC-21 2019.

I fabricated the sample, did material characterization, electrical characterization, and data analysis and presented the research work at the conference via oral presentation.

Acronyms and Symbols

Here, important acronyms, abbreviations, chemical formulas, and physical quantities are listed, which are recurring throughout the thesis. Some parameters, which only occur in a narrow context, are intentionally omitted; some parameters are used in multiple ways, but the context is always explicitly clarified in the corresponding text.

Acronyms and Abbreviations

APB	Anti Phase Boundary
APD	Anti-Phase Domain
ART	Aspect Ratio Trapping
BOE	Buffered Oxide Etch
CB	Conduction Band
CCD	Charge Coupled Device
CMOS	Complementary metal oxide semiconductor
EBL	Electron Beam Lithography
EBSD	Electron Backscatter Diffraction
EBSP	Electron Backscatter Diffraction Pattern
EDS	Energy Dispersive Spectroscopy
ELO	Epitaxial Lateral Overgrowth
FLA	Flash Lamp Annealing

FPA	Focal Plane Array
FTIR	Fourier Transform Infrared Spectroscopy
HRTEM	High-Resolution Transmission Electron Microscopy
IC	Integrated Circuits
ICP-PECVD	Inductively Coupled Olasma Enhanced Chemical Vapor Deposition
ICP-RIE	Inductively Coupled Reactive Ion Etching
IPF	Inverse Pole Figure
IR	Infrared
MBE	Molecular Beam Epitaxy
MCT	Mercury Cadmium Telluride
MOVPE	Metal Organic Vapor Phase Epitaxy
MWIR	Mid Wavelength Infrared
NEP	Noise Equivalent Power
NETD	Noise Equivalent Temperature Difference
NWs	Nanowires
R	Responsivity
RMG	Rapid Melt Growth
ROIC	Read Out Integrated Circuit

RTA	Rapid Thermal Annealing
SAG	Selective Area Growth
SEM	Scanning Electron Microscope
SRH	Shockley Read Hall
TASE	Template Assisted Selective Epitaxy
TDDs	Threading Dislocation Density
TDs	Threading Dislocations
VB	Valence Band
XRR	X-ray Reflectometry

Physical Quantities and Chemical Formulas

μ	Mobility
Al_2O_3	Aluiminium Oxide
CH_4	Methane
CHF_3	Trifluoro Methane
E_c	Conduction Band Energy
E_g	Bandgap
E_v	Valence Band Energy
Ge	Germanium
$Hg_{1-x}Cd_xTe$	Mercury Cadmium Telluride

HMDS	Hexamethyldisilane
InAs	Indium Arsenide
InSb	Indium Antimony
K	Extinction Coefficient
m_c	Electron Effective Mass
m_v	Hole Effective Mass
N_2	Nitrogen
$Pb_{1-x}Sn_xTe$	Lead Tin Telluride
Si	Silicon
Si_3N_4	Silicon Nitride
SiH_4	Silane
SiO_2	Silicon Dioxide
α	Absorption Coefficient
λ	Wavelength
ν	Frequency

INTRODUCTION

1

Background

1.1 Infrared Detection- Background

The history of heat detection dates back to the 17th century when Herschel demonstrated the existence of radiation beyond the visible red spectrum using glass thermometers[1]. The most critical development of infrared (IR) detectors was initiated with thermal detectors such as thermocouples, thermopiles, Golay cells, bolometers, and pyroelectric detectors. These detectors operate at room temperatures and are used extensively even today, but their drawbacks are their relative insensitivity and slow response times (ms for current bolometers[2]). These drawbacks propelled research toward semiconductor photon detectors. Since then, numerous studies and developments have focused on intrinsic and extrinsic semiconductor infrared material systems. One of the most important phases of semiconductor IR detector research occurred between the late 1960s and 1970 when a linear array of one hundred compound semiconductor $Pb_{1-x}Sn_xTe$ and $Hg_{1-x}Cd_xTe$ (MCT) detector elements were demonstrated. Then began the research towards the large detector arrays aiming for a one-to-one correspondence between the detector elements and the electronic addressing circuits[3].

The detector image elements (also called pixels) located at the focal plane of the imaging system are commonly referred to as the focal plane array (FPA), and it is the key constituent in an IR instrument. Inventions and developments of CCD drives and Si complementary metal oxide semiconductor (CMOS) technology significantly impacted the development of FPAs. For example, if 64 x 64 pixels were available in the 1980s, now it is about 10^8 pixels[3]. Larger array formats would require shrinking the pixel size, which improves the system's resolution and reliability. Complex epitaxial structures have enabled efficient FPA design, but the fourth-generation IR system, with a target of a high pixel count of $>10^8$, still has technological challenges to overcome.

IR FPAs need to connect an IR-sensitive semiconductor structure with a complex CMOS read-out-integrated circuit (ROIC) for each pixel and thus are very well suited for 3D integration. Two common FPA chip fabrication approaches are hybrid and monolithic[3] (Fig 1.1). The former is the

conventional approach, where the detector is optimized separately and integrated on top of the ROIC chip using flip-chip bonding. The achievable interconnect density limits the pixel density in this case. In the latter case, the detector and the read-out circuit are realized in a single monolithic component. This approach reduces the number of processing steps and costs and improves the system's overall efficiency. The current IR FPA technology, below 10 µm pixels, is aligned and hybridized efficiently[4,5]. However, it will be very difficult to achieve pixel sizes less than 5µm due to the extreme challenges of aligning the two chips. Instead, this could be enabled by a thin monolithically integrated absorption layer directly onto the ROIC to achieve pixel sizes in the range of 1-5µm.

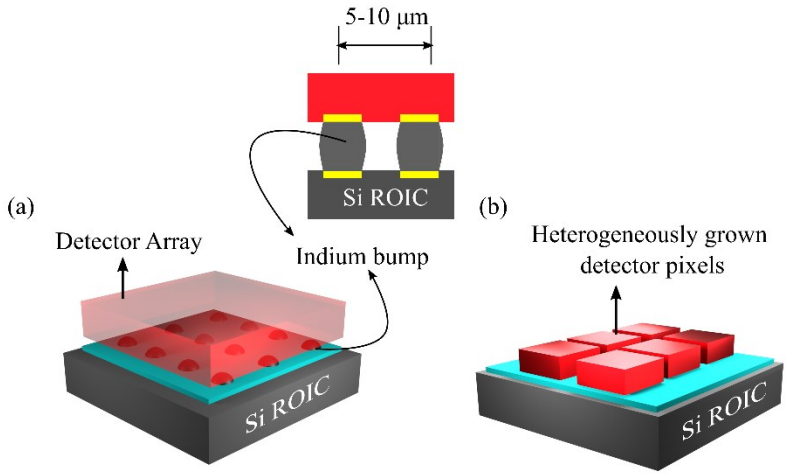


Figure 1.1 Schematic illustrating (a) FPA chip using conventional hybrid process (b) Heterogeneous monolithic integration of detector elements on Si.

MCT FPAs dominate the current IR photodetector for mid-wavelength infrared radiation (MWIR) applications. These detectors can be used for a wide range of IR wavelengths by tuning the cadmium content in the material. Although MCT detectors demonstrate unparalleled device performances such as high detectivity (~10^{12} cmHz$^{1/2}$ W^{-1}), high quantum efficiency (> 70%), and fast response time (ns), they are limited by high cost, array size, low operating temperature, and material fragility[6]. Moreover, the Restriction of Hazardous Substances (RoHS) of the European Union regulates mercury

and cadmium concentrations and only permits the use of MCT with temporary exemptions[7]. On the other hand, III-V materials are more robust when compared to MCT, have high uniformity, and are stable. Furthermore, III-V material semiconductor photodetectors are RoHS compatible. They are easy to process and offer a cost-effective advantage over MCT detectors. The most promising competitor to MCT IR detectors is III-V type II superlattices such as InAs/GaSb and InAs/InAsSb[8,9] and InSb IR technology[10–13]. However, all these detectors still use hybridization of III-V semiconductors with Si processors using indium bonding.

The bonding process is limited by the maximum thermal budget of the CMOS wafer. The maximum thermal budget of the CMOS wafer is estimated to be 425 °C for 2-6 hours or 400 °C for 8-10 hours [14]. Additionally, significant stress can be produced in the detector's active region due to the thermal expansion mismatch and the difference between the bonding and cryogenic operating temperatures. One solution to overcome the issues related to bonding and alignment issues for pixel elements <5 µm will be to implement 3D integrated monolithic heterogeneous IR detectors on the Si CMOS platform.

1.2 3D Heterointegration

3D integration technologies enable packing diverse functionalities into small form factor systems that require ultra-fine interconnects and interfaces. There are three main approaches to implementing 3D integration to achieve multiple diverse functionalities: 3D stacking of ICs/wafers, 3D integrated packaging, and 3D monolithic IC integration [15].

In 3D- stacking of IC dies, wafers, and packages are created by vertical stacking of die-on-die, die-on-wafer, wafer-on-wafer, package-on-package (PoP), or a combination of multiple stacking techniques through bonding techniques. For instance, PoP is enabled by wire bonding and flip-chip bonding. In the case of die-on-die and wafer-on-wafer integration, bonding and through silicon via (TSV) interconnects are used for integration. Fig 1.2 (a-c) illustrates the PoP, die-on-die, and wafer-on-wafer integration technique[16].

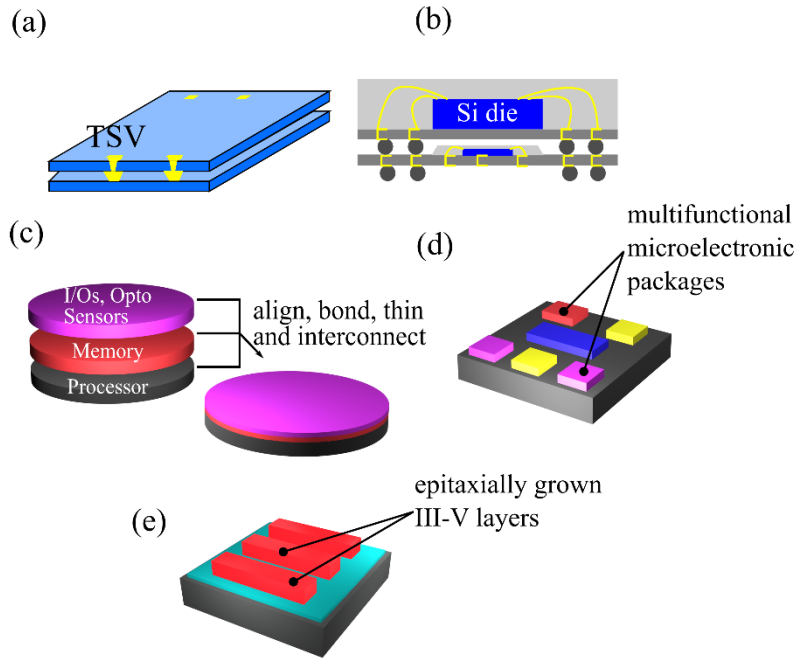


Figure 1.2 a) Die-on-Die integration b) package-on-package integration c) wafer-on-wafer integration d) 3D integration packaging (System on Package) e) 3D monolithic integration.

3D integrated packaging (Fig 1.2d) realizes all the system functions on an ultra-miniaturized, multi-functional, and high-performance micro-electronics package by integrating passive and active components into a single package substrate. It provided miniaturization of a system by substrate integration with high-density I/Os, micro vias, and embedded components. A higher number of active dies can be embedded into the thinner package substrate. This technique provides high reliability with low cost[17].

In 3D monolithic IC integration (Fig 1.2e), devices using different technologies are integrated monolithically on a single semiconductor wafer. This technique enables lower power consumption and high-speed operations when compared to using separate circuits. In addition, the material properties of compound semiconductors can be used to fabricate electrical and opto electronic devices and can be integrated with the Si system. One of the first 'True' 3D integrated devices was reported by Kazior et al., where InP HBT

devices were heterogeneously integrated adjacent to a CMOS transistor on a Si wafer[18]. Monolithic 3D hetero integration of III-V semiconductors is reviewed in detail in Chapter 2.

This thesis demonstrates the monolithic integration of infrared photodetector with the Si and W metal. The integration techniques used in this thesis– Rapid Melt Growth (RMG) and Template Assisted Selective Epitaxy (TASE) are described in Chapters 2, 5, and 6.

1.3 InSb and InAs Properties

1.3.1 Electronic Band Structure

The origin of the electronic band structure can be illustrated using the Kronig-Penney model (Fig 1.3) in approximating a 1D periodic rectangular barrier potential. The solution to the Schrödinger equation in this type of periodic potential gives rise to energy bands with a traveling wave solution and forbidden bands with an exponential decaying solution.

If we consider the energy-momentum relation following wave mechanics,

$$E = \frac{mv^2}{2} \tag{1.1}$$

where v is the velocity, the electron momentum p = mv, and the k space vector is given by $k=2\pi/h$. Thus, rewriting the electron energy in k space for one dimension.

$$E = \frac{\hbar^2 k^2}{2m_0} \tag{1.2}$$

Thus, the E-k relation for a free electron is a simple parabola.

Figure 1.4 a-b shows the band structure of the indirect bandgap of Si and the direct bandgap of InSb. The E-k relation at the bottom of the conduction band (CB) is approximated by

$$E_c = E_g + \frac{\hbar^2}{2m_c}(k_x{}^2 + k_y{}^2 + k_z{}^2) \tag{1.3}$$

$$E_v = -\frac{\hbar^2}{2m_v}(k_x{}^2 + k_y{}^2 + k_z{}^2) \tag{1.4}$$

$$E_g = E_c - E_v \tag{1.5}$$

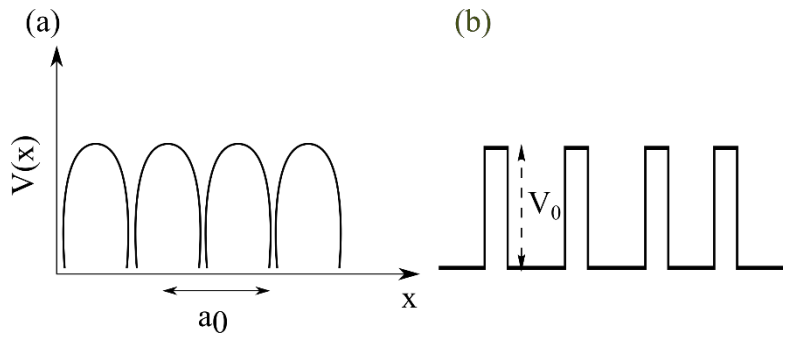


Figure 1.3 (a) Crystal-lattice potential with lattice constant a_0 (b) Idealized rectangular barrier potential used in Kronig-Penney model.

where E_c is the energy of the bottom of the CB, E_v is the energy of the bottom of the VB, and E_g is the bandgap (direct or indirect). The influence of ions in the motion of electrons in the conduction band is given by m_c, which is referred to as the effective mass of the electron. A similar expression can also be derived for the valence band, where m_v represents the holes' effective mass. The effective mass depends on the material's crystal structure and the electron's direction of travel in nonisometric crystals.

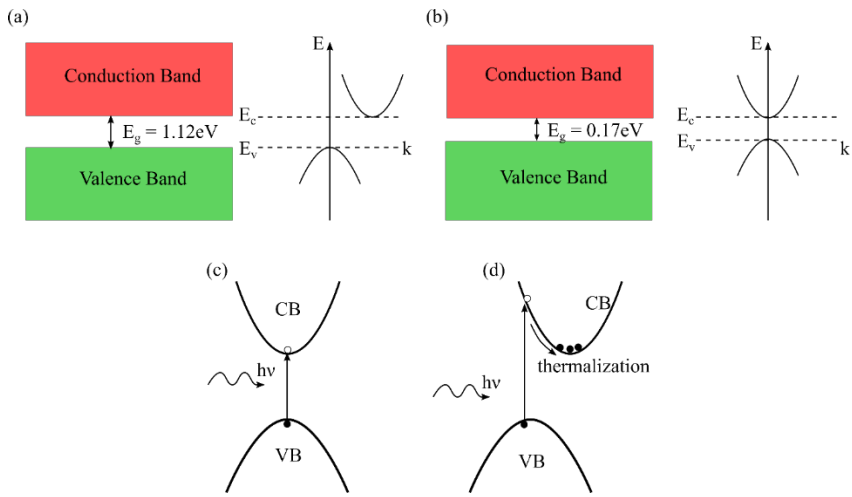


Figure 1.4 Cross-sectional E-K diagram of (a) Si and (b) InSb. Absorption in c) direct d) indirect bandgap semiconductors

In all regular crystals, the maximum of the valence band is located at the Γ point where an electron has zero momentum. A direct bandgap semiconductor is a semiconductor for which the conduction band minimum is also located at the Γ point. In direct bandgap semiconductors, an electron in the conduction band can transfer into the valence band by emitting a photon with the same energy as the band gap E_g. In the same way, an electron in the valence band can absorb a photon with energy at least equal to E_g to transfer from the valence band into the conduction band (Fig 1.4c). On the other hand, semiconductors such as Si whose conduction band minima and valence band maxima do not correspond to the same value of the wavenumber are called indirect bandgap semiconductors. In indirect bandgap semiconductors, photon emission is unlikely. This is because the transition from near bottom of the conduction band to near bottom of the valence band requires a momentum exchange. However, the momentum can be conserved by phonon participation. On the other hand, photon absorption can occur in indirect bandgap semiconductors (Fig 1.4d). This usually happens in two steps where an electron is first excited to a high energy level in the conduction band, which then quickly relaxes through the thermalization process by transferring momentum to phonons. Therefore, this requires the emission/absorption of a phonon to/from the crystal lattice and is less efficient compared to a direct optical transition.

1.3.2 Cutoff Wavelength

The energy ($E = h\nu$), where ν is frequency and h is Planck's constant, of the incident photon and the wavelength are related as

$$\lambda = \frac{1.24}{E}\ \mu m \tag{1.6}$$

Suppose the incident photon has energy greater than the bandgap of a semiconductor; in that case, an electron is excited from the valence band to the conduction band, causing a generation of an electron-hole pair (EHP). The excess energy ($h\nu$-E_g) is dissipated as heat in the semiconductor.

If the wavelength of the incident beam is longer than the critical wavelength (i.e., $h\nu < E_g$), the photo response decreases abruptly as there is no available target state for the electron to transfer to. This critical wavelength corresponds to the bandgap of a semiconductor (in the case of an intrinsic detector). For example, the bandgap of InSb at 77 K is 0.22 eV, corresponding to a wavelength of 5.6 μm. If the InSb is bombarded with

longer wavelength photons, these photons will pass through the InSb detector undetected. However, InSb would efficiently absorb photons with shorter wavelengths. The wavelength at which the photo response decreases abruptly is called the cutoff wavelength. The band gap in most semiconductors is temperature dependent, and so is the cutoff wavelength. For InSb, the cutoff wavelength is 5.6 μm at 77 K.

The spectral region where the material changes from relatively transparent ($hv<E_g$) to strong absorption($hv>E_g$) is referred to as the absorption edge. Direct bandgap semiconductors have an abrupt absorption edge compared to indirect bandgap semiconductors. The weaker absorption above the absorption edge in indirect semiconductors is due to the requirement for a phonon-assisted indirect transition, which is less probable at low temperatures when phonons are scarce. In extrinsic detectors in which doping has been introduced to create localized states near the conduction band edge, the absorption efficiency will be limited by the concentration of these localized states[19].

1.3.3 Absorption Coefficient

A semiconductor material's absorption coefficient (α) represents the wavelength-dependent average penetration depth of a photon into the material before it is absorbed. Understanding the α of different materials is crucial as it will impact the geometrical design of the photodetector. For instance, if a material has a low absorption coefficient, light will penetrate far into the material before it is absorbed. On the other hand, if the material is too thin, it will appear transparent to that wavelength.

If a semiconductor is illuminated by a photon flux intensity I_0 at x= 0, then the emerging photon flux at a distance x is given by

$$I(x) = I_0 e^{-\alpha x} \tag{1.7}$$

where α is the absorption coefficient. This indicates the intensity of the photon flux decreases exponentially within a distance x through the semiconductor.

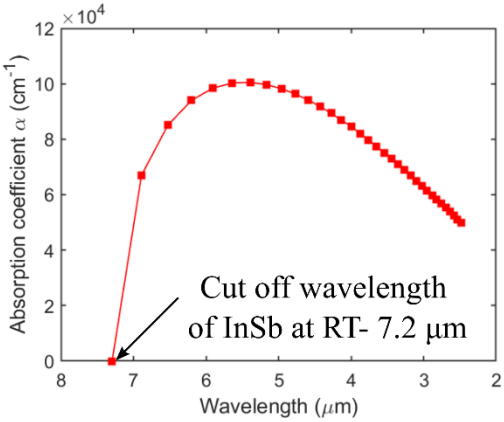


Figure 1.5 Calculated absorption coefficient as a function of wavelength. The calculation is based on the equation for the absorption coefficient for band-to-band transition given in [19].

The characterization of α as a function of wavelength aids in predicting the optical behavior of the semiconductor material. The absorption coefficient is related to wavelength as

$$\alpha = \frac{4\pi K}{\lambda} \tag{1.8}$$

where K is the extinction coefficient, and λ is the wavelength[20]. Figure 1.5 shows the calculated absorption coefficient for InSb, highlighting the cutoff wavelength of InSb at RT.

1.4 Aim of the Thesis

This research study aims to demonstrate the monolithic 3D integration of III-V materials such as InSb and InAs onto heterogeneous substrates such as Si and W metal; characterize and apply these nanostructures for infrared photodetection.

The first part of the thesis focuses on integrating InSb-on-insulator devices on Si substrates using the Rapid Melt Growth technique. Chapter 3 provides an overview of this technique and a survey of the previous works in RMG. A detailed description of the fabrication process, thermodynamic consideration for the RMG process, and the results are presented in Chapter 5. The work involves a significant material characterization, and the descriptions of the techniques used are provided in Chapter 4. The

heterogenous integrated InSb is used to fabricate a metal-semiconductor-metal infrared photodetector, whose characteristics are discussed in Chapter 5.

The second part of the thesis focuses on the direct growth of vertical InAs nanowires on W metallic substrates via template-assisted selective epitaxy. The overview of this research work and the analysis of the same is given in Chapter 6. In addition, the progress towards fabricating an InAs nBn barrier detector for the infrared regime (2-3 μm) using this material is also presented in Chapter 6.

2

Heterogeneous III-V Integration

Si-based CMOS technology is the fundamental building block in contemporary digital electronics. It is a mature technology that has dominated over the years due to the high availability of Si, relatively good electron transport properties, and low-defective Si/SiO_2 interface, allowing for reliable devices to be made at scale. On the other hand, applications in optoelectronics and high-frequency communication III-V semiconductors have superior properties owing to their direct bandgap and high electron mobility. However, the raw materials that make up the common III-V semiconductors (Ga, In, Sb) are scarce, and it has been challenging to make defect-free III-V wafers larger than six inches in diameter which increases the manufacturing cost. Therefore, the hetero integration of III-Vs with Si technology has been widely studied to leverage the benefits of both Si and III-V materials.

There are several approaches developed over the years to integrate good quality III-V materials with minimum defects on Si. These techniques include wafer bonding, buffer layer growth, aspect ratio trapping, VLS nanowire growth, and selective area growth of nanowires. This chapter presents an overview of the challenges of III-V integration with Si and some of the well-studied integration techniques as a background to the description of the integration techniques used in this thesis: Rapid Melt Growth and Template Assisted Selective Epitaxy.

2.1 Challenges of III-V Heterogeneous Integration

The heterogeneous integration of III-V is a promising field; however, it is accompanied by a few challenges. Obtaining a defect-free single crystal through an integration technique is not trivial. The main challenges are lattice mismatch, thermal mismatch, and the polarity difference between the III-V material and Si. These challenges and issues during the integration of III-V on Si are briefly discussed in this section.

2.1.1 Lattice Mismatch

Lattice mismatch occurs when two crystals with different lattice parameters (a_0) are combined during heterogeneous integration. For example, Si exhibits a diamond crystal structure with a lattice parameter of 5.4 Å, and InSb has a zinc blende structure with a lattice parameter of 6.4 Å. When combined, the unit cells at the interface are either compressed or elongated due to the lattice mismatch. The lattice mismatch (misfit) is given by:

$$f = \frac{a_L - a_S}{a_S} \tag{2.1}$$

Where a_L is the lattice parameter of the layer and a_S is the lattice constant of the substrate. For the Si-InSb system, the lattice mismatch is 19 %. The effect of lattice mismatch when $a_L > a_S$ is presented in Fig 2.1a. In this case, the layer is compressed in the lateral direction leading to elongation in the axial direction[21].

2.1.2 Thermal Mismatch

Heteroepitaxial growth is always performed at temperatures far above room temperature to provide sufficient mobility for the adatoms on the growth surface. Since the Si substrate and the III-V materials have different thermal expansion coefficients, thermal stress will be induced while cooling to room temperature. Thermal stress may result in wafer bowing or even thermal cracks in the sample[22,23].

2.1.3 Anti-Phase Boundaries

The crystal structure of Si is nonpolar, indicating no difference between the <111> directions. On the other hand, III-V semiconductors are polar in nature. Therefore, the growth of polar semiconductors on non-polar substrates may result in Anti Phase Domains (APD) formation. During the initial stages of the growth, the III-V nucleations will align at their random [011] direction to <011> direction in Si. The regions with different [011] orientations will grow to form APDs and be bounded by Anti Phase Boundaries (APBs)[22,23].

2.1.4 Dislocations

Dislocations are a type of line defect virtually present in any crystal. When two different semiconductor layers are combined, the strained epitaxial layer may relax by introducing misfit dislocations. To reduce the compressive or

tensile strain in an epilayer, the introduction or omission of the lattice is favorable. The dislocation line can neither begin nor end at the surface; therefore, dislocations from the substrate are replicated in the layer to form threading dislocations[21].

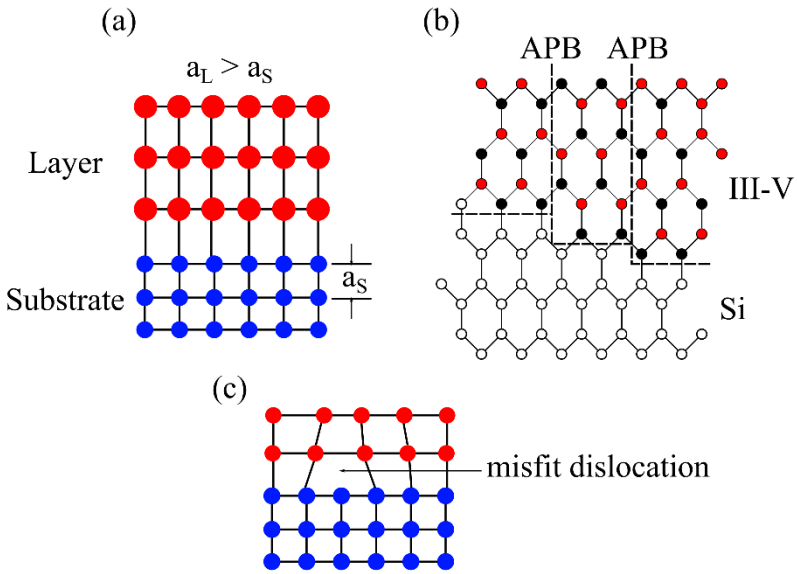


Figure 2.1 a) Compressively strained layer in the lateral direction due to lattice mismatch b) Formation of Antiphase boundaries at single steps in Si (adapted from Ref 15) c) Representation of misfit dislocation.

2.2 Common Heterogeneous integration Techniques

2.2.1 Buffer Layer Growth

The most straightforward way to integrate III-V semiconductors on Si is to directly grow a thin film of III-V material onto a Si substrate. However, due to the large lattice mismatch and difference in polarity between the III-V material and the substrate, defects generated from the interface cause misfit and threading dislocations in the grown III-V layer. These defects will

degrade the epitaxial material's properties, so they are avoided by growing thick buffer layers (μm in case of uniform buffer layers) between the Si substrate and the top (device) layer. These buffer layers reduce the defects in the device layer by annihilating dislocations within the thick buffer layer. Dislocations that meet can be annihilated by the formation of dislocation loops that do not progress further upwards in the growing crystal. It is observed that the dislocation density is inversely proportional to the layer thickness because of the annihilation of the dislocations[24].

Several additional buffer layer techniques have been extensively studied, such as the Si buffer layer[25], two-step growth, graded buffer layers, and superlattices. Two-step growth, for example, in GaAs/Si[26,27] and InP/Si[28] systems, is initiated with a low-temperature nucleation growth step, which leads to a thin and rough layer. This is followed by annealing to smoothen the layer and growth at higher temperatures to grow a buffer layer containing fewer defects. Studies have also reported using intermediate buffer layers by inserting other materials (whose lattice constants and thermal expansion coefficient are similar to Si) between the Si and III-V layers[29,30]. However, the threading dislocation density (TDDs) in both techniques produces ~ 10^8 cm^{-2}.

Graded buffers are also reported to be used for strain relaxations[31]. Continuous or stepwise changes in the lattice constant of the material inside the buffer layer form these buffer layers. The tuning of the lattice constant is done by tuning the composition of the material. As a result, strain relaxation in graded buffer layers is more efficient than uniform buffer layers, and therefore graded buffer layer offers a significant reduction in TDDs[32].

In the case of strained layer superlattices (SLSs), multilayer structures with alternating compressive and tensile strains are formed. SLS has been widely studied in GaAs/Si heteroepitaxy using InGaAs/GaAs, InAlAs/GaAs strained layers[33,34]. If the thickness of each SLS layer is less than a certain critical thickness, the elastic strains are contained within each SLS layer. The strains in the superlattice will cause the bending of the dislocation line, which favors the annihilation of the dislocation. Overall, buffer layer growth is associated with high cost due to the growth of additional thick epitaxial layers. Furthermore, the technique does not suppress the antiphase domains and might lead to cracks in III-V layers due to the buildup of thermal strain.

2.2.2 Selective Area Growth

The Selective Area Growth (SAG) technique was first developed and used for Si-ICs in the 1960s[35]. It is a template method that involves epitaxial growth and lithography approach. In this technique, templates fabricated from oxide or nitride cover most of the substrate except for small, patterned openings. At high temperatures, the adatoms arriving on the mask see the template surface, which is not energetically favorable for nucleation; therefore, the adatoms diffuse on the surface. This leads to growth within the openings of the mask. Taush and Lapierre, and Rai Choudhury investigated initial studies on SAG GaAs[36,37]. Jones and Lau reported one of the early reports on lithography-defined SAG GaAs[38]. Later on, this technique was further developed into the epitaxial lateral overgrowth (ELO) technique which is briefly discussed in the next section. Nowadays, the SAG approach is used to grow III-V nanowires (NWs)[39]. The main disadvantage of this technique is that it requires a high growth temperature to prevent the growth on the template mask to get good selectivity.

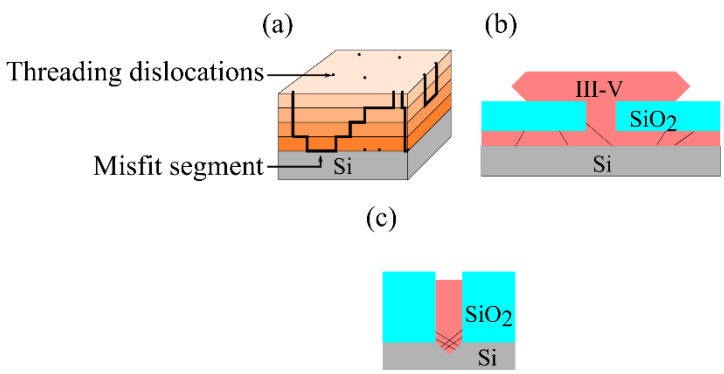


Figure 2.2 Schematic illustration for a) graded buffer layer growth b) epitaxial lateral overgrowth c) aspect ratio trapping.

2.2.3 Epitaxial Lateral Overgrowth

Epitaxial lateral overgrowth (ELO) is a technique based on selective area growth (SAG) and is used to inhibit the propagation of the threading dislocations of the III-V epitaxial layers. This technique first uses metal-organic vapor phase epitaxy (MOVPE) or molecular beam epitaxy (MBE) to

grow a thin III-V film on Si substrates. This layer acts as a seed layer (buffer layer) for the ELO growth and has a high density of dislocations produced due to the lattice mismatch with Si. Then, a SiO_2 layer is deposited, and trenches down to the III-V seed layer are formed by lithography and etching. The exposed III-V surfaces within these openings will act as the nucleation sites for the second III-V epitaxial growth, which fills the trenches and grows out on top of the mask (Fig 2.2b). By tuning the growth parameters, lateral growth is promoted such that the materials from each trench can grow together, leading to a complete film on top of the mask. As a result, most threading dislocations (TDs) are blocked at the bottom of the SiO_2 mask and thus confined in the seed layer. As a result, only a small fraction of the defects propagate through the openings into the top III-V layer. Outside of the trench regions, the quality of the laterally grown III-V material can thus be very high. For instance, a study on ELO GaN by MOCVD reports the reduction of TDD by 3-4 orders of magnitude when compared to bulk growth of GaN grown by MOCVD[40]. Several studies have reported this technique on GaAs and InP on Si systems[41–43]. The studies have explored different aspects of the ELO technique, such as the ELO growth condition optimization[44], investigation of ELO layer dimension with growth temperature[45], and lateral and vertical growth rate with mask stripe orientation[46]. The ELOG technique has also been explored for optoelectronic applications such as AlN LEDs[47], GaN lasers[47] and GaAsP/Si-based solar cells[48]. Various studies have also reported ELO of InP on Si for enabling photonic integrated circuits with Si CMOS[49,50]. The drawbacks of these techniques are the presence of voids above the mask, the high density of defect levels in the trench region, and defects created by merging lateral growth fronts.

2.2.4 Aspect Ratio Trapping

Aspect ratio trapping (ART) is an evolution of the buffer layer method and ELO to improve further the quality of the III-V heteroepitaxial films grown on Si. This technique involves forming high aspect ratio trenches in silicon oxide or similar dielectric material on top of the Si substrate (Fig 2.2c), into which selective epitaxy occurs. Compared to ELO, the trenches have a much larger height than width, and the growth process ends soon after the material grows out of the trench and does not merge into a complete film on top of the mask. Instead, each structure is used as an individual device. The core idea in ART is that defects originating from the III-V – Si interface will terminate at the sidewalls of the high aspect ratio trenches so that the material

at the top of the trench is relatively defect free. ART relies on the fact that threading dislocations and stacking fault defects tend to glide on {111} crystal planes which on Si (001) substrates are inclined [51,52]. One remaining drawback of ART is that APB along {110} planes and {111} planar defects along the trench direction are not naturally confined and may thread all the way to the top of the trench. Mitigating these defects requires considerable effort and skill. For example, the bottom shape of the trenches can be engineered to create a double-step formation using a thin Ge buffer layer to solve the formation of APB when integrating III-V on (001) oriented Si substrate[53]. The study on ART with GaAs on Si has highlighted the effect of different shapes of bottom trenches on the defect reduction process and shown that a V-shaped bottom trench results in the lowest defect density[54]. Thus, by confining the defects at the bottom of the trenches, high-quality crystals can be utilized for high-performing electronic and optical devices[55–57].

High-performance Ge devices and III-V devices fabricated from shallow trenches isolation (STI) templates using the ART technique have been previously reported. Waldron et al. demonstrated the first fully integrated InGaAs n MOSFET by ART technique[58]. Recently, GaAs/InGaP heterojunction bipolar transistors using STI templates were shown on a 300 mm Si substrate for 5G and mm-wave applications[59]. The ART technique has also implemented optoelectronic devices such as lasers and photodetectors. Wan et al. reported an on-chip InAs/InGaAs quantum dot waveguide photodetector with an internal responsivity of 0.9 A/W[60]. A monolithically integrated InGaAs/GaAs multi-quantum well waveguide photodetector illustrated an internal responsivity of 0.65 A/W[61]. GaAs/InGaAs quantum well lasers have also been demonstrated with ART technique[62].

2.3 Template-Assisted Selective Epitaxy

Template-assisted selective epitaxy (TASE) is a technique that can be viewed as derived from ART that utilizes SAG inside tubular oxide structures (template) to achieve heteroepitaxy of III-V nanomaterials on Si[63]. TASE was first developed at IBM's Zurich Lab and was first used to realize vertical InAs nanowires on Si substrates with a multitude of crystal orientations while not having to adjust the same growth parameters.[64]. In this study, templates were formed by covering sacrificial Si nanowires with SiO_2 and then etching back the Si to form nanotubes containing a Si seed surface at the bottom. The

Si seed acted as a starting point for nucleation and thereby initiated the growth of the InAs, which grow to fill out the space of the nanotube. The process requires a long diffusion length of the precursor molecules to reach into the entire template cavity without risking nucleation on its inner walls, and therefore, a growth technique such as MOCVD is best suited for TASE.

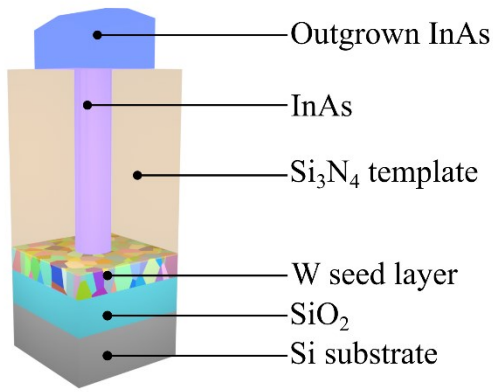


Figure 2.3 Illustration of the schematic of the final structure in a TASE process for growing InAs from a W seed layer.

Misfit dislocations, threading dislocations, and APBs are major challenges faced during integrating III-V materials with Si due to the large lattice mismatch, thermal mismatch, and polarity differences between the materials. Buffer layers, ELO and ART, are used to repress these defects to different degrees. However, in these methods, the approach to repress APBs is to maximize nucleation density at the onset of film growth to self-terminate the APBs early in the film. However, in TASE, the approach is the opposite; here, the conditions are tuned to only have a single nucleation event in each template tube. This is guaranteed by reducing the dimensions of the mask opening to an area much smaller than the precursor diffusion length such that once a nucleation event occurs, it will consume all additional material arriving at the seed area.

TASE process was first demonstrated for vertical structures, focusing on InAs nanowires and InAs-InSb heterostructures[65,66]. Later the TASE process was extended with horizontal and stacked templates with complex shapes. By opening templates in sequential growth runs, extremely dense integration of GaSb and InAs nanostructures could be realized, allowing for fully III-V

CMOS[67]. TASE has also been used to realize state-of-the-art nanosheet transistors[68],photodiodes[69] and lasers[70], and the technique is now used in several labs[70–72]. However, twin defects and stacking faults are commonly observed defects in TASE grown structures[68,73]. Other drawbacks of the technique are slow growth rate[74] and limitation to dimensions of the structures by a few microns.

2.4 Rapid Melt Growth

Rapid Melt Growth (RMG) is a monolithic heterogeneous integration technique pioneered by the Plummer group at Standford University in 2005[75]. This technique was developed for high-quality Ge-on-insulator (GOI) films on Si substrates and allows for much larger structures to be made compared to both ART and TASE.

In the RMG technique (Fig 2.4), an amorphous target material (i.e., Ge or III-V) is structured and confined within a micro-crucible and then exposed to a rapid thermal anneal above its melting point such that the material melts within the crucible. The target material would contact the substrate via a small opening, while most of the material otherwise resides on top of an insulating dielectric layer. The opening is generally referred to as the seed area. Upon cooling, the melted phase recrystallizes, starting from the seed area, and epitaxially grows from the seed area and propagates to the end of the patterned structure. The "necking" caused by the narrow region and change of direction close to the seed confines dislocations and stacking faults to the area close to the seed, allowing the rest of the crystal to be of high quality. The RMG technique can be viewed as being derived from the Czochralski growth technique, used for macroscopic growth of large single crystals from a liquid melt, but at the microscale: The three key elements of the Czochralski growth method also exists in RMG, i.e., 1) a crystalline seed that provides a template for the epitaxial growth from 2) a liquid melt that supplies material for the solidification process, and then finally, 3) a necking mechanism which traps defects and allows for very large defect-free crystals to be grown. For Si crystals, these can be 300 mm in diameter and more than a meter long. Therefore, materials grown using the Czochralski method are also potential candidates for RMG.

RMG was first introduced to produce high-quality GOI crystals. To achieve single crystalline Ge, it is important that crystallization is initiated on the seed area and afterward only occurs on the solid Ge surface and not on the

inner walls of the crucible (unseeded nucleation). It was reported that a temperature window exists where the epitaxial growth rate of Ge seeded by the Si substrate dominated over the unseeded nucleation. The process window lies closer to the melting point of Ge. There were several studies on how different undercooling could result in different grain sizes of Ge. Liu et al. demonstrated a 20 µm single crystalline Ge region with the same orientation as the Si substrates using the RMG process and reported the possibility of obtaining single crystals longer than 20 µm without any random nucleation[76]. This propelled the research towards wide and ultra-long GOI crystals using RMG[77–81]. For instance, Hashimoto et al. demonstrated 40 µm long single crystal Ge wires[77], whereas Miyao et al. reported 400 µm long and 2-5 µm wide Ge stripes using RMG[80]. Finally, with the development of hexagonal mesh patterns (Ge strips comprising of crossing strips), large area crystalline Ge networks (500*250 μm^2) were implemented[82].

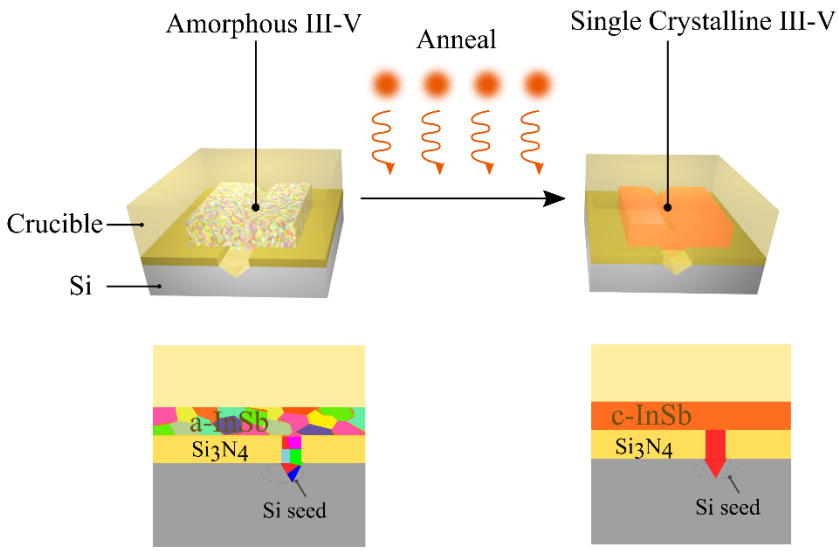


Figure 2.4 Schematic illustration of the RMG process

The literature on RMG studies has also highlighted the achievability of defect-free single crystalline structures. In the RMG process, the dislocations and stacking faults that appear due to lattice mismatch between Si and the Ge at the interface of Si-Ge tend to terminate at the top of the Ge film above

the seed area, while the remainder of the Ge film will be defect free[76]. However, the Ge crystals tend to exhibit a twist/rotation along the long axis of the crystal. This phenomenon has been widely reported, and the dependence of cooling rate and melting temperature on lattice rotation of Ge crystals have been studied[83,84]. Details of this phenomenon will be later discussed in Chapter 5.

More recently, RMG has also been used in more material systems than Ge. For example, stochiometric III-V semiconductors with congruent melting temperatures like GaAs, and GaSb[85], binary alloys like SiGe[86], and ternary semiconductors like InGaAs[87] have been successfully demonstrated. A large miscibility gap exists in the case of alloys such as SiGe. The large liquidus-solidus gap indicates that on cooling, the first solid formed from SiGe liquid will have lower Ge content while it increases along the length of the structure. As a result, laterally graded SiGe films are formed using the RMG process[88]. In the case of ternary semiconductors such as InGaAs, whose melting point lies closer to Si, a large amount of Si dissolves from the seed into the melt, creating Si islands within the InGaAs crystals that have been reported[89].

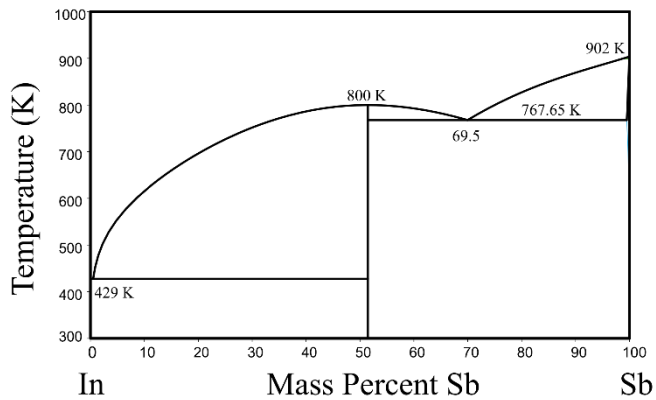


Figure 2.5 Phase diagram of InSb

In this work, we apply RMG to InSb, which has the highest lattice mismatch (19 %) to Si among the III-Vs. InSb is a binary stoichiometric III-V compound semiconductor, and the phase diagram of InSb (Fig 2.5) is characterized by two eutectic points that occur at In- InSb (0.7 %) and Sb-InSb (69.5 wt % Sb). InSb melts and solidifies congruently, indicating that

when the material melts, the liquid and solid phases will have a congruent (same) composition. At the congruent temperature, there is no segregation between the liquid-solid interface during the crystal growth. Furthermore, even with a minor deviation from In:Sb (1:1) in the melt would still be able to produce stoichiometric single crystals.

3

Infrared Detectors

Infrared radiation is a region in the electromagnetic spectrum whose wavelength ranges from 770 nm to 1 mm. Depending on their temperature, all objects emit electromagnetic radiation with energy in this range, called *radiative heat*. The history of heat radiation detectors dates back to the 17th century when Herschel demonstrated the existence of radiation beyond the visible red spectrum using glass thermometers. Since then, numerous studies and developments have focused on infrared radiation, detectors, and emitters. A broad classification of the infrared spectrum is as follows:

- Near-infrared (NIR, 770 nm - 3 μm)
- Mid wavelength infrared (MWIR, 3 - 5 μm)
- Long wavelength infrared (LWIR, 8 - 14 μm)
- Far infrared (FIR, 16 μm - 1 mm)

The main applications of NIR include optical communication, reflectography, surveillance, and optical coherence tomography. In addition, MWIR and LWIR are, to a large degree, used for military surveillance applications, environmental monitoring, and medical screening, whereas FIR is used in astronomy, long-wavelength heaters, and medical therapy[90,91].

Most infrared detectors can be classified into thermal detectors and photon detectors. In this chapter, we briefly discuss these types of IR detectors and the important parameters to consider while analyzing the performance of IR detectors.

3.1 Thermal Detectors

The schematic of a thermal detector is shown in Fig 3.1. When infrared radiation is incident on a material, the absorbed radiation changes the temperature of the material, and the temperature change is measured electrically using a temperature-dependent mechanism such as thermoelectric voltage, resistance, or pyroelectric voltage[92]. The two most commonly used thermal detectors are bolometers and pyroelectric detectors. In the case of bolometers, the change in the heated material's electrical resistance is detected, whereas, in pyroelectric detectors, a change in internal polarization upon heating is detected.

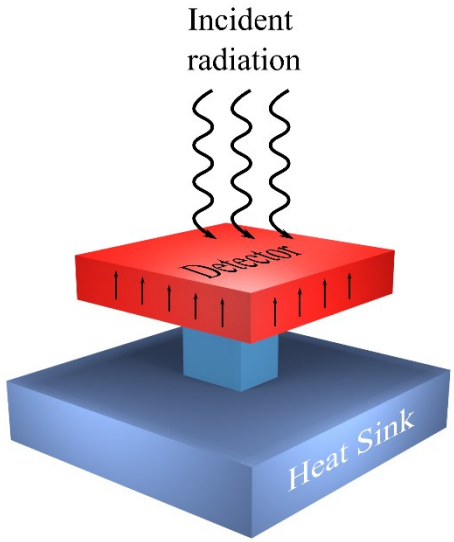


Figure 3.1 Schematic of pyroelectric thermal detector

Thermal detectors generally operate at room temperature, unlike photon detectors, even for far infrared detection. The thermal effects depend on the radiative power and are independent of the wavelength of the radiation. Due to that, the detectors rely on an intermediate process (heating) between radiation and electrical signal, the signal may be lost in the process (heat dissipation), and additional noise would be added, making these detectors relatively insensitive. In addition, long thermal time constants slow the detection speed at best a few 100 Hz, but they are cheap and easy to use[3]. In the last decade, however, there has been enormous development in the field of thermal detectors. Recent studies on micromachined silicon bolometers and pyroelectric detector arrays show promising results in the development of thermal imagers[2,5].

3.2 Photon Detectors

In a photon detector, the absorbed radiation triggers an electronic transition within the materials, which is then observed as an electrical output. All types of semiconductor-based IR detectors fall into this category. The basic excitation processes in these detectors involve a transition of an electron from

the valence band to the conduction band (A, intrinsic absorption), from a dopant level to a conduction band/valence band (B, extrinsic absorption), or from a free carrier in the conduction band (C, free carrier absorption). Photon detectors exhibit selective wavelength dependence in contrast to thermal detectors. As seen in Fig 3.2, the spectral response increases gradually until a cut-off wavelength at which the response quickly drops. The cut-off wavelength is generally specified as a wavelength at which the detectors responsivity falls by 50% of the peak responsivity.

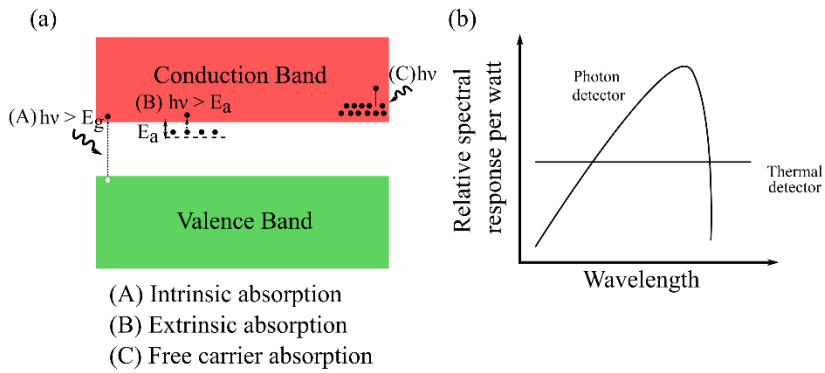


Figure 3.2 (a) Excitation process in bulk semiconductors (b) Relative response time for a thermal and photon detector

Photon detectors generally exhibit a good signal-to-noise ratio and have fast response times. However, they often need to be cooled to a cryogenic temperature to reduce the thermally induced electronic transitions, which would otherwise mask the optically generated signal. Such cooling requirements make these IR systems bulky, expensive, and inconvenient to use.

The photon detectors can be classified into intrinsic, extrinsic, and photo emissive detectors, according to the nature of the radiation interaction and electronic transition. Furthermore, depending on the structure of the photon detector, they can be further divided into photoconductors, p-n junction photodiodes, nBn detectors, metal-insulator-semiconductor (MIS) photodiodes, and Schottky barrier photodiodes. This thesis explores photoconductors and nBn detectors and will be discussed in detail below.

3.2.1 Photoconductor

In its simplest form, a photoconductor is a semiconductor, generally a thin film or bulk form contacted by metal at the two ends (Fig 3.3). When IR radiation illuminates this semiconductor, an electron-hole pair is generated, thereby increasing the semiconductor material's charge carrier concentration and conductivity. Photoconductors are classified as intrinsic detectors if the excitation is from the valence to the conduction band. On the other hand, if the excitation is into the conduction band from impurity states within the band, they are called extrinsic detectors.

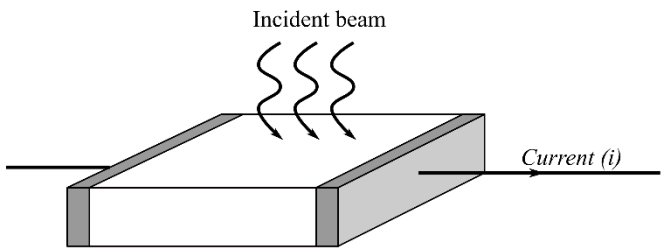


Figure 3.3 Schematic of a photoconductor

The current produced from a photoconductor is given by:

$$i = \frac{\eta q G_p P}{h\nu} \tag{3.1}$$

$$G_p = \frac{\tau_r}{\tau_t} \tag{3.2}$$

where η is the quantum efficiency (number of electron-hole pairs created for each incident photon), and P is the radiation power. G_p is the photoconductive gain, which is given by the ratio of carrier lifetime until recombination (τ_r) and the time for the carrier to transit to the electrode (τ_t). As equations 3.1 and 3.2 show, a photoconductor may have finite gain. This can be understood by the following. An incident photon flux with energy higher than the semiconductor's bandgap generates an electron-hole pair. The generated electron is swept quickly into the positively biased electrode

because of its higher mobility than the hole. A new electron immediately replaces this electron from the other electrode to maintain charge neutrality. This process continues until the hole has been collected, resulting in a photoconductive gain. Even though these types of detectors would provide high responsivity, they lack response time due to the long lifetime of the carriers. Additionally, these detectors have high dark current, require electrical bias for operation, and are associated with non-uniformity in the detector element when operated at lower temperatures due to the recombination mechanism at the electrical contacts.

3.2.2 nBn photodetector

An nBn detector is a barrier detector consisting of a semiconductor heterostructure in which a large band gap-depleted barrier layer separates an n-type absorbing layer and an n-type contact layer (Fig 3.4 b-c)[93]. The barrier layer blocks the transport of the majority carrier type (electrons in the case of nBn) and allows an unimpeded flow of the minority carriers. Therefore, the barrier in an nBn detector should be engineered meticulously to have nearly zero valence band offset (VBO) and large conduction band offset (CBO). In addition, for the majority carrier dark current to be blocked and minority carriers to flow toward the contact (cathode), it is essential to have the barrier located near the contact layer and away from the optical absorber. The thickness of the absorbing layer should be roughly equivalent to the absorption length of the device to maximize absorption efficiency, and the barrier layer must be thick enough to suppress electron tunneling.

A significant disadvantage of a photon detector, especially for long wavelength infrared radiations, is that the background (dark) current produced due to the thermally excited carriers becomes significant compared to the photocurrent, which is detrimental to the detectivity. There are three main contributors to the dark current:

- Diffusion current associated with Auger or radiative processes (I_{diff})
- The surface current associated with conduction via states on the surface of the device (I_{surf})
- Shockley-Read-Hall (SRH) current (I_{SRH})- A current associated with the thermal excitation and recombination of the carriers that occur in the depletion region of a p-n junction. The defect or impurity centers in the depletion region, which form a different

energy level within the forbidden energy gap, could also trigger SRH currents.

The diffusion current is the primary source of dark current in an nBn photodetector. The diffusion current is expressed as:

$$I_{diff} \propto \frac{q{n_i}^2}{N_d \tau_{diff}} AL \tag{3.3}$$

$${n_i}^2 \propto T^3 \exp\left(\frac{-E_g}{k_B T}\right) \tag{3.4}$$

$$I_{diff} \propto T^3 \exp\left(\frac{-E_g}{k_B T}\right) \tag{3.5}$$

where τ_{diff} is the carrier lifetime, N_d is the n-type doping, n_i is the intrinsic carrier concentration, and L is the width of the neutral region.

The surface leakage current is approximately temperature independent and has an ohmic current-voltage relationship. This current is mainly due to the surface charges that form an n-type layer that covers the narrow band gap semiconductor regardless of its doping. Therefore, proper passivation of the device by native oxides may reduce the surface leakage current and surface recombinations.

The primary source of dark current in a cooled photodiode is the SRH current. In a conventional p-n junction, the diffusion of the majority of charge carriers across the junction creates a space charge region that is depleted of free charge carriers. This diffusion continues until the electric field created from the depletion region is large enough to inhibit the diffusion of the charge carriers. In thermal equilibrium, the fermi level is uniform throughout the device and can act as the center for the SRH current, which is one of the main contributors to the dark current (Fig 3.4 a).

$$I_{SRH} = q \frac{W_{dep} n_i A}{2\tau_0} \tag{3.6}$$

$$n_i \propto T^{\frac{3}{2}} \exp\left(\frac{-E_g}{2k_B T}\right) \tag{3.7}$$

$$I_{SRH} \propto T^{\frac{3}{2}} \exp\left(\frac{-E_g}{2k_B T}\right) \tag{3.8}$$

where W_{dep} is the width of the depletion region, and τ_0 is the electron-hole lifetimes.

The key to minimizing the SRH current is to remove the fermi level from the middle of the band gap. By introducing a wide bandgap barrier layer in between an n-type absorbing and contact layer, the fermi level position can be varied from the middle of the band gap. Effectively, the dark current associated with the SRH process and the surface leakage current is reduced by this device architecture. As a result, it exhibits a higher signal-to-noise ratio enabling the detector to operate at higher temperatures when compared to conventional diodes.

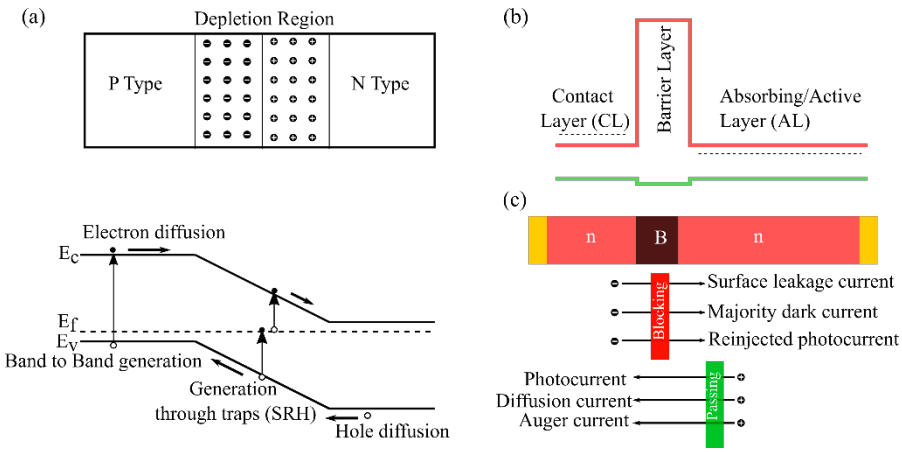


Figure 3.4 (a) p-n junction and band diagram illustrating the SRH process(b) Band diagram of nBn detector (c) schematic of nBn detector illustrating the current components which are blocked and passed in the presence of the barrier.

3.3 Figures-of-Merit

To analyze, quantify and adequately compare the performance of the IR photodetectors, it is essential to understand their figures of merit. The figure of merits of the detectors describes the signal-to-noise ratio and the signal from the detector in terms of the power of the incident radiation and the wavelength. The work of defining suitable figures-of-merit for IR photodetectors was first initiated in the year of 1950s by Jones[94]. The widely

used figures-of-merit are spectral response, responsivity, noise equivalent power (NEP), detectivity, frequency response, response time and time constant, and noise equivalent temperature difference (NETD).

(i) Spectral response:

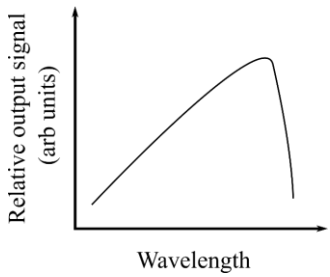


Figure 3.5 Spectral response of a photodetector

The spectral response (Fig 3.5) gives information about how the detector changes its output signal in response to changes in the wavelength of the input signal[95]. The vertical scale can either be the rate of arrival photons per unit wavelength interval or unit incident radiant power per unit wavelength. The latter is commonly used for infrared detectors.

(ii) Responsivity:

The responsivity *R* gives information about the signal gain of the detector[96]. It is defined as the output signal (typically voltage or current) of the detector produced in response to a given incident power on the detector. Responsivity is given by

$$R = \frac{I_{ph}}{\mathrm{P}*\mathrm{A}} \tag{3.9}$$

where I_{ph} is the photocurrent, P denotes the incident power density, and A is the effective illuminated area. The usual units of responsivity for infrared detectors are either V/W or A/W. Although responsivity gives a good indication of the fundamental performance of the IR detector, it does not provide information about the intrinsic noise in the device and, thus the sensitivity of the detector. For instance, due to high noise levels, a detector with high R might still be unable to detect low-intensity IR radiation signals

or distinguish between IR sources of closer intensities. Therefore, it is important to also rely on other figures of merits in addition to responsivity.

(iii) Noise equivalent power:

The *NEP* is defined as the radiant power incident on the detector that produces a signal equal to the root mean square of the detector noise. It is a measure of the minimum radiant flux that the detector can measure. A low value of *NEP* would mean better sensitivity of the detector. The following equation can describe it:

$$NEP = \frac{I_N}{R*\sqrt{\Delta f}} \tag{3.10}$$

where I_N is the rms noise current (voltage) measured within the required bandwidth. If the noise amplitude is frequency independent, the noise spectral density will have an inverse dependence on the square root of frequency. The unit of *NEP* is, therefore, W Hz $^{-1}$. The *NE*P value could be misinterpreted if the frequency is not specified, and therefore measured *NEP* values should always be represented either in full operational bandwidth or 1-Hz bandwidth.

(iv) Detectivity:

The detectivity of defined as the reciprocal of the *NEP* and is a measure of the signal-to-noise ratio per unit of radiant power.

$$D = \frac{1}{NEP} \tag{3.11}$$

The root mean square of the detector noise is proportional to the area of the detector A_d, indicating that both *NEP* and detectivity are functions of the device geometry. Thus, one can define a normalized detectivity of the detector by considering A_d, which is called the specific detectivity D^*.

$$D^* = \frac{(A_d*\Delta f)^{\frac{1}{2}}}{NEP} \tag{3.12}$$

Therefore, D^* is defined as the detector output signal-to-noise ratio at 1 Watt of input IR radiation normalized to the detector with unit area and unit bandwidth. A high value of detectivity would indicate that the detector can detect even low signal amplitudes.

(v) Response Time and Time constants:

The response time and the time constants of the detector are extracted from the response of the detector when illuminated with pulsed radiation.

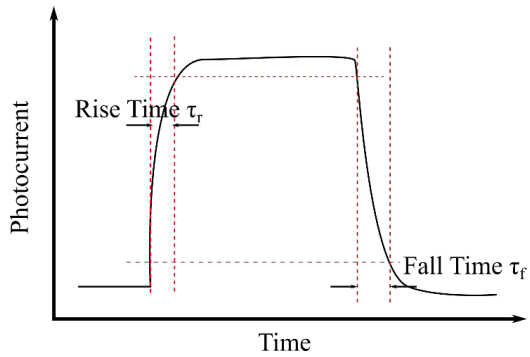


Figure 3.6 Illustration of the response time of a photodetector when illuminated with a pulsed optical beam

When a pulsed optical beam is an incident on the detector sample, a photocurrent is generated, and the response time is calculated as either the rise or fall time required for the output current to change from 10% to 90% of the final current value or vice versa (Fig 3.6). The response time depends on two factors: the RC constant of the detector circuit and the transit time of the slowest type of generated charge carriers, i.e., the holes[97]. The carriers' transit time indicates the time required to collect the carriers at the electrodes. The transit time of the photodetector is given by:

$$\tau_{transit} = \frac{L^2}{\mu_{drift} E} \tag{3.13}$$

where μ is the mobility of the carriers, L is the electrode spacing, and E is the applied bias[98–100]. The transit time thus depends on the carrier mobility and the electrode spacing.

The second factor limiting the response time could be the time constant of the detector equivalent circuit(τ_{RC}). For a photoconductor is given by:

$$\tau_{RC} = (R_L + R_s) C_p \tag{3.14}$$

where R_L is the load resistance, R_s is the series resistance, and C_p is the parasitic capacitance.

The presence of surface and trap states can also affect the response time of the photodetector. When a light is incident on the detector, excess holes and electrons are generated. As a consequence, two fermi levels are generated. As the intensity of the light increases, these quasi-fermi levels move either to the conduction band and valence band, creating an increased number of trap states into recombination centers. These trap states prolong the lifetime of the photoexcited carriers as these trap states are first filled up to reach maximum and then contribute to the steady photocurrent[101,102].

4

Process and Characterization Methods

This chapter introduces key processing and characterization methods used throughout this thesis work. First, the flash annealing technique utilized for the RMG process is described in detail. Following this, the material characterization tools, such as electron backscatter diffraction and energy dispersive spectroscopy, along with the description of the optical characterization technique of Fourier transform infrared spectroscopy, are provided in this chapter.

4.1 Flash Lamp Annealing

Thermal annealing techniques are an integral part of the semiconductor processing industry and are generally used to relieve stress in Si, reduce defects and activate dopants. Challenges evoked by the scaling of the CMOS devices now require a technique that minimizes the diffusion of the dopant impurity into the device area[103,104]. Flash lamp annealing is a technique that uses arrays of flash lamps to produce pulses of intense light in the range of 10 µs-100 ms. The energy is provided by Xe flash lamps which emit a broad spectrum of light with maximum intensity in the violet spectral region

To understand the concept of annealing and the temperature distribution in a material, it is vital to discuss a few thermodynamic values related to it. Thermal diffusivity (D_{th}) describes how quickly heat conduction occurs in a material and is given by

$$D_{th} = \frac{\lambda_T}{\rho C_p} \tag{4.1}$$

where λ_T is the thermal conductivity, ρ is the mass density, and C_p is the specific heat capacity. The thermal response time (τ_{th}) is given by:

$$\tau_{th} = \frac{s^2}{D_{th}} \tag{4.2}$$

where *s* is the thermal diffusion length which is practically the characteristic length of interest. For instance, it can be either the width of the doping profile or the wafer thickness. For Si, the thermal diffusivity is 0.9 cm^2s^{-1} at RT and 0.09 cm^2s^{-1} at 1600K. This indicates that the thermal response time will be in the range of 3 to 30 ms for a Si wafer of thickness 525 µm. In rapid thermal annealing (RTA), the annealing time (1-100 s) is longer than the τ_{th} for Si, and during the annealing process, both the front side and backside of the wafer are at the same temperature. Whereas FLA has an annealing time of 10 µs-100 ms and is in the same range of $\tau_{th,}$ and hence only a narrow region close to the surface is annealed to a maximum temperature, and there is a decaying temperature profile towards the backside of the sample.

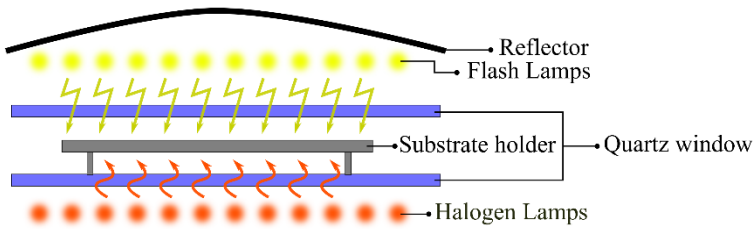


Figure 4.1 Schematic of FLA tool with backside preheating by halogen lamps and flash lamp array on the top.

Figure 4.1 shows a basic schematic of an FLA tool. It consists of a process chamber with a substrate holder, quartz windows protecting the lamps, a bank of Xe flash lamps, a bank of halogen lamps used for preheating the sample if required, and a reflector that directs the light towards the substrate. Quartz windows are used to protect the lamps against potential material evaporated from the sample and to protect the sample and pump in case of lamp explosion. The flash lamps are triggered by a pulse-forming network consisting of large capacitors and coils, which determine the flash pulse's shape and duration. Pulse intensity and duration are the critical parameters of an FLA. The typical values of the pulse times vary from 0.1 ms - 20 ms, with the energy density variation from 10-100 J/cm^2. Depending on whether the flash pulse is short or long, the backside temperature is closer to RT or the surface temperature. For a long pulse time, FLA can turn into an RTA-type process, and for a very short time, there is a possibility that FLA can turn into a laser annealing-type process.

4.2 Electron Backscatter Diffraction

Electron backscatter diffraction (EBSD) is a characterization technique used to acquire information about individual grain orientation, local texture, point-to-point orientation correlation, and phase identification of individual grains[105]. This technique extracts the orientation information from the electron backscatter diffraction patterns (EBSP) formed on a phosphor screen when the stationary column of electrons illuminates the steeply inclined crystalline sample in a scanning electron microscope (SEM).

The EBSP was first reported in 1954 by Alam, Blackman & Pashley. They referred to the pattern as a high-angle Kikuchi pattern, which was recorded on an electron-sensitive film. Later in the 1970s, they were recorded on a fluorescent phosphor screen placed inside an SEM chamber. They were photographed directly from the screen, and analysis was based on this photograph. Modern EBSD tools have a fully automated system where EBSPs are captured on a fluorescent phosphor and imaged live by a camera while the patterns are indexed automatically.

The experimental setup of an EBSD system is shown in Fig 4.2. EBSD is usually used in conjunction with a scanning electron microscope, where an electron beam is focused on a small area. The electrons interact with the sample, and a fraction of these are diffracted due to the arrangement of the atoms in a crystal. Some of the backscattered electrons collide with a fluorescent phosphor screen, which is about 1-2 cm away from the sample holder. The phosphor screen is parallel to the electron beam and the stage's tilt axis. A sensitive CCD camera is used for viewing the diffraction pattern on the phosphorous screen. A tilted geometry of the sample is preferred to obtain the maximum number of backscattered electrons. When the diffracted electrons intersect the phosphor screen, they produce pairs of lines. Each pair of lines is known as the Kikuchi lines, and the diffraction pattern is referred to as the Kikuchi diffraction pattern. The phosphor screen is parallel to the electron beam and the stage's tilt axis. A sensitive CCD camera is used for viewing the diffraction pattern on the phosphorous screen.

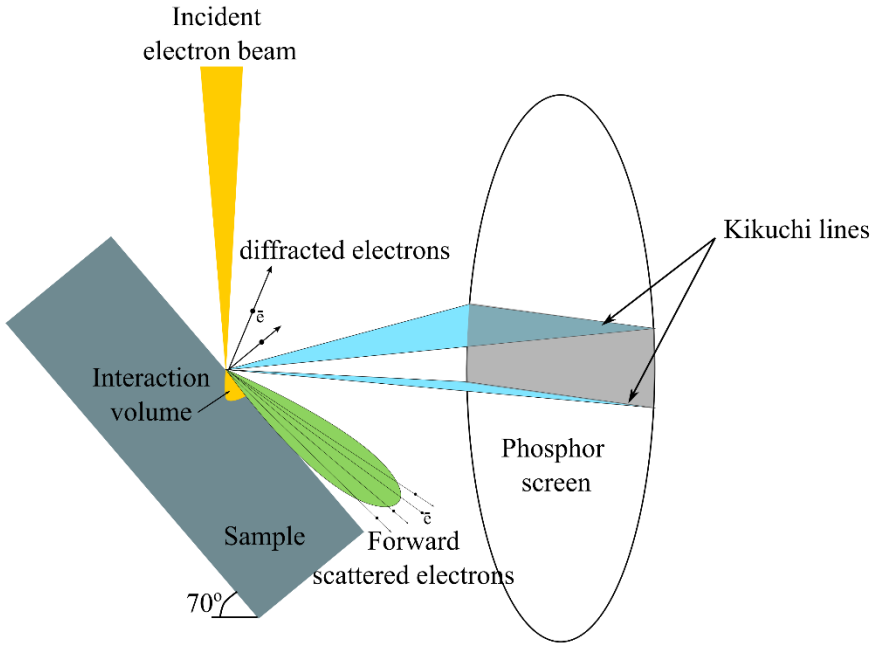


Figure 4.2 Schematic illustrating the EBSD setup.

4.2.1 Formation of EBSP

As the electron beam enters the sample, the electrons are subjected initially to a diffuse inelastic scattering of electrons in all directions. The atomic plane of the material is thus exposed to electrons in all directions. Some of the electrons satisfy Bragg's Law.

$$n\lambda = 2d_{hkl}sin\theta_B$$

Where λ is the electron's wavelength, and θ_B is the Bragg angle. The electrons that impinge the crystal's parallel planes and satisfy the Braggs condition will scatter elastically and form two cones of diffracted electrons ($-\theta_B$ and θ_B). The pair of cones are essentially hyperbola recorded on the screen. Since the Bragg angle is small (0.5 -2°) and the opening angle of the cones is (90- θ_B), the hyperbolas appear as two straight lines known as Kikuchi lines. A particular crystal plane in the crystal gives rise to a pair of Kikuchi lines. The Kikuchi bands intersect at locations known as the zone axes, which indicate the actual crystallographic direction within a unit cell of a crystal.

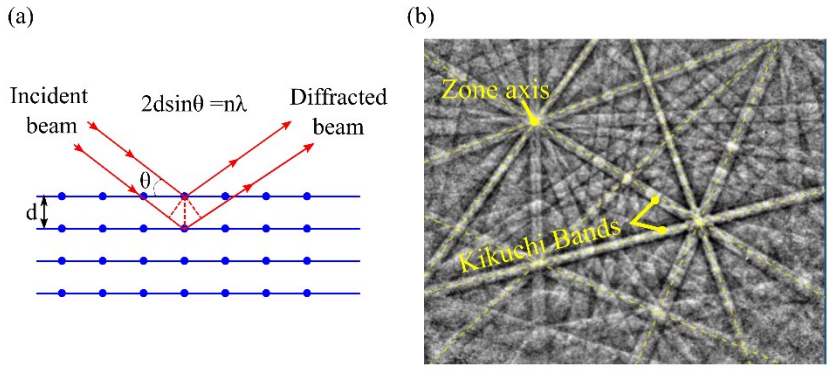


Figure 4.3 a) Schematic illustration of Bragg's Law b) EBSD generated Kikuchi pattern of InSb wafer indicating the Kikuchi bands and one of the zone axis.

The intensity of each band relative to the intensity of other bands is extracted using a structure factor F_{hkl}. This is a key parameter for processing Miller Indices of the bands in EBSPs. As the figure above shows, The EBSPs contain many Kikuchi bands formed at different angles and positions. To extract the band positions, the Hough Transform[106] is used. Using the Hough transform, the center of the bands can (i.e., the center line) can be extracted, and thus the band position. Note that every point in the EBSP is a pixel and is associated with a coordinate (x,y). The Hough transform technique converts every pixel into *Hough space* (illustrated in Fig 4.4). For example, here, points 1,2, and 3 would correspond to different pixels on a band center line. Each point is converted into a sinusoidal curve that intersects in Hough space. The intersected point gives the position of the band. Once the bands are detected and indexed, the algorithm then compares the detected band geometry with the known crystallographic information of the sample. As a result, the crystallographic phase and orientation are determined.

The sample must be tilted to a high angle to maximize the fraction of the backscatter electrons. Typically, the backscatter electrons that form the EBSP originate from a small volume below the specimen. The depth of volume is about 20 nm for 20 kV accelerating voltage. Therefore, the sample's surface is crucial for the quality of the EBSP obtained.

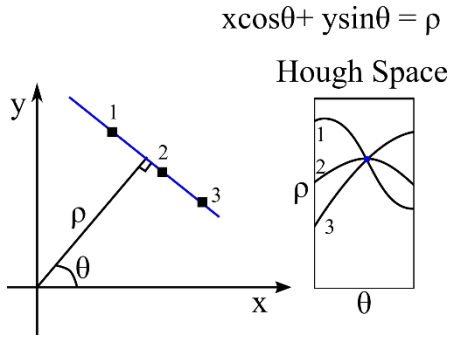


Figure 4.4 Schematic representation of Hough Transformation implemented in EBSPs

Tilt angles between 60-85° give good contrast for the Kikuchi patterns. However, at 85°, the electron beam spot is elongated along the sample, resulting in diffuse patterns. A good compromise is to use 70° to obtain good Kikuchi bands. Due to the sample tilting, the spatial resolution parallel to the tilt axis is better than perpendicular to the tilt axis. Usually, the resolution perpendicular to the tilt axis is three times the resolution parallel to the tilt axis when the tilt angle is 70°, and the factor is 5.7 times when the tilt angle is 80°. In regard to the accuracy of the measurement technique (how well the orientations are measured with respect to the reference frame) is generally quite poor, as the accuracy of the measurement could be affected by the EBSD setup and how the sample is cut and placed in the holder. However, the angular precision of the measurement is high and is close to 0.5°

4.2.2 Display and Interpretation of EBSD Data

(i) Inverse pole figure

The Inverse Pole Figure (IPF) shows the prevalence of crystallographic planes in an EBSD data set along one of the sample's cartesian (x, y, z) axes as a stereographic projection. Here, each crystallographic orientation is displayed as a single point. Figure 4.5 shows an IPF plot for the sample normal direction (z-direction). In the example, only one crystal plane is observed, and it is close to the [001] direction. In case the sample is a cubic material, it would mean that the (001) plane is almost parallel to the sample surface.

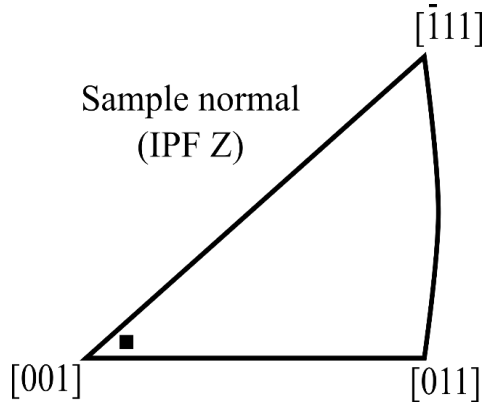


Figure 4.5 Inverse pole figure plotted for sample normal (IPF Z), which displays the orientation of a crystal direction with respect to the normal.

(ii) Inverse pole figure map

By assigning a color to each direction in the stereographic triangle, an orientation map can be created from the EBSD data by mapping the orientation of each pixel in the data by the appropriate color key from the IPF.

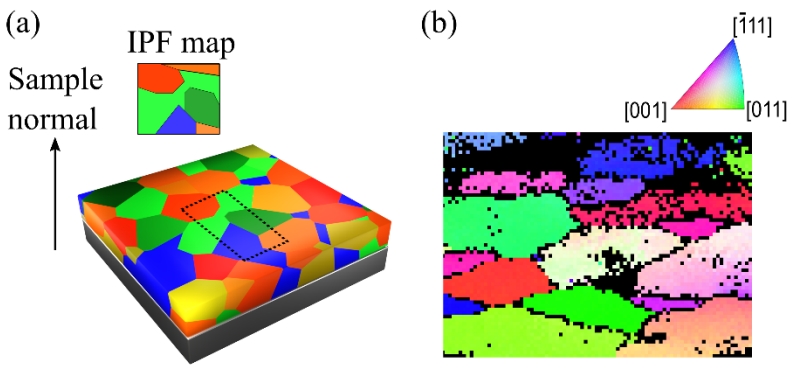


Figure 4.6 (a) Schematic illustration of crystal orientation indicated using a color variation. (b) EBSD generated an IPF map showing grains with different orientations according to the orientation color key.

For instance, Fig 4.6 b shows an actual measured IPF map of a W (Tungsten) thin film in the z-direction, indicating the position of the grains and their different orientations. The black regions separating two grains appear

because the software could not reliably index the pixels to a specific crystal orientation due to overlapping signals from the two grains and can be viewed as representing grain boundaries.

4.3 Energy Dispersive Spectroscopy

Energy dispersive spectroscopy (EDS) is a method used in conjunction with scanning electron microscope (SEM) or scanning transmission electron microscope (STEM), where a focused electron beam is used to produce x-ray signals from the materials which can be analyzed to enable elemental mapping of the sample[105]. Figure 4.7 shows a schematic diagram of the inner atomic shells and how characteristic x-rays are produced. An incident electron can interact with the atom to expel an electron from an inner shell, creating a vacancy that is filled by a transition of another electron from an outer shell into the vacant position. In this process, characteristic energy, depending on the shell structure of the atom, is released in the form of X-rays. The resultant photon energy is in the range of a few to several keV and is thus specific to each element.

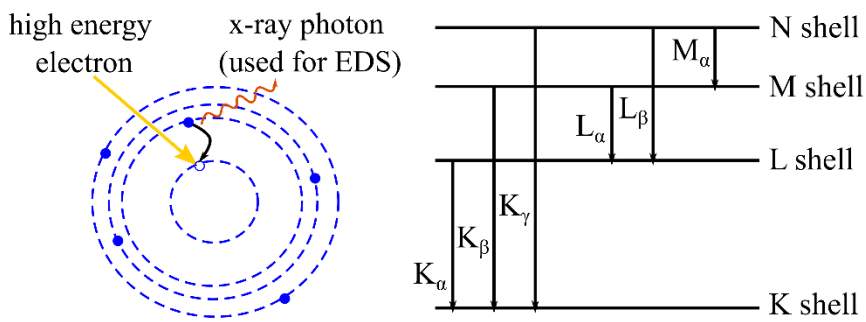


Figure 4.7 Schematic illustrating x-ray generation used in EDS.

During characterizing nanostructures, it is important to consider the region from which the X-rays are generated from the sample. The sample's interaction volume and the X-ray generation region can be controlled by adjusting the acceleration voltage. Low acceleration voltage would result in a small interaction volume, and smaller features of the sample can be detected. Note that the interaction volume would vary from sample to sample. But, the general rule of thumb is to use a low acceleration voltage to

obtain low interaction volume. It is also important to remember that the reduced acceleration voltage should be high enough to excite the required characteristic X-ray from the sample.

4.4 Fourier Transform Infrared Spectroscopy

Fourier transform infrared spectroscopy is a technique that measures the spectrally resolved absorption, transmission, and photocurrent with a high signal-to-noise ratio. The method utilizes the interferogram formed by the interference of two light beams to extract the infrared spectrum.

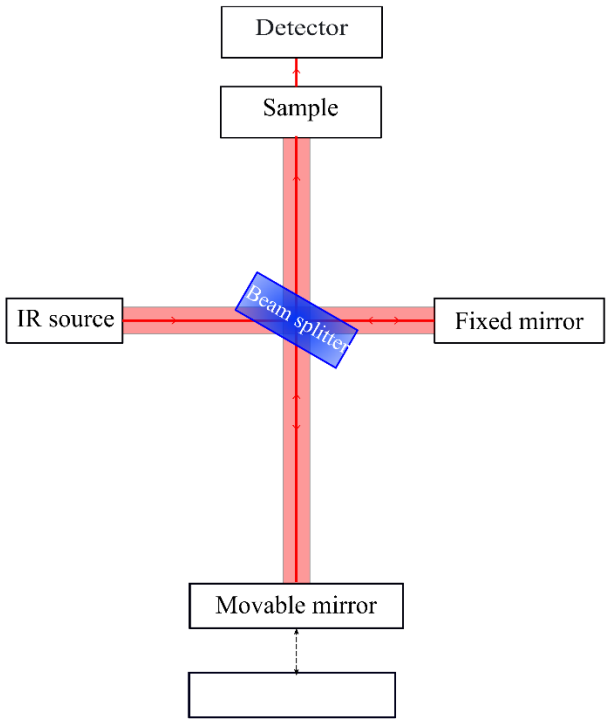


Figure 4.8 Simple schematic illustration of FTIR setup

The typical FTIR spectrometer consists of an IR light source, a Michelson interferometer, a sample compartment, a detector, and an amplifier. The light source generates a beam that bombards the sample after passing through the interferometer. The interferometer splits the beam into two using a beam

splitter. The beam splitter is a semitransparent mirror that transmits half of the beam striking it and reflects the other half. The beam transmitted through the beam splitter hits the fixed mirror, and the reflected beam reaches a movable mirror. The fixed and movable mirrors reflect the light beam back to the beam splitter, where it is combined to form a modulated beam comprising all wavelengths. The beam is then focused onto the sample, which in our case, is mounted in a cryostat integrated into the sample compartment of the FTIR setup. The sample itself is used as a detector. The beam produces a modulated photocurrent from the sample, which is amplified by a fast current-voltage amplifier. The interferogram consists of the modulated output voltage, and the mirror position is then converted to a spectrally resolved photocurrent by using Fourier transform algorithm.

The photocurrent measurements in this work were carried out using the FTIR model Vertex 80v from Bruker. The spectrometer has a pulse tube closed-cycle cryostat (Janis PTSHI-950-FTIR) for measurements down to 5 K. A MIR source with a KBr beam splitter was used for our samples.

5

InSb-on-insulator by RMG

This chapter describes and discusses the thesis results on InSb-on-insulator synthesis by the RMG method. It consists of four main sections; a general description of the fabrication process along with the discussion regarding the observed fabrication challenges; thermodynamical modeling giving insights into the feasibility of using InSb for the RMG process; electrical and material characterization of the rapid melt-grown samples; realization of an InSb-on-insulator metal semiconductor metal photodetector.

5.1. Fabrication Process

The fabrication process to realize the InSb-on-insulator microstructures is divided into four major steps and discussed in the following.

(a) Seed Area Patterning: The fabrication process was initiated on full three-inch Si (100) as the starting substrate. This is covered by a thin (40 nm) Si_3N_4 layer, deposited using inductively coupled plasma-enhanced chemical vapor deposition (ICP-PECVD) using SiH_4 and N_2 precursors at 250 °C. The Si_3N_4 layer will act as the electrically insulating and separating layer between the InSb and Si, and it was chosen due to its resistance to the wet etching chemistries used later in the process. First, the Si_3N_4 layer is patterned with long narrow trenches to prepare for the formation of the seed area (nano-sized opening into the Si substrate). For this, electron beam lithography (EBL) using a positive resist (AR-P 6200.09) was used, and the trenches were dry-etched using CHF_3:N_2-based inductively coupled reactive ion etching (ICP-RIE). Following this, a V-groove is formed in the Si exposed in the trenches by using a heated TMAH 25% etch. This step is introduced for two reasons; firstly, the appearance of the V-groove can be verified by SEM and verifies that the trench etch step was deep enough. Secondly, the etch ensures that the Si surface is clean and free of dry-etch induced damage which may otherwise interfere with the nucleation of crystalline InSb on the surface. After this step, the wafers were sent to our collaborators (the University of Glasgow or EPFL) for deposition of an amorphous layer of InSb (1:1), either 30 nm or 120 nm thick using molecular beam epitaxy (MBE) (Fig 5.1 a-d).

It is essential to ensure that the interface between the deposited amorphous InSb material and the Si substrate is pristine and undamaged. Therefore, the rapid oxidation of Si surfaces in the air is challenging. In addition, the native oxide, even if very thin, may prevent epitaxial InSb growth. It was, therefore, crucial that the native oxide was removed using a BOE or HF wet etch directly prior to loading the sample into the vacuum of the MBE chamber. Even so, any delay could negatively impact the yield of this step, which made it important to collaborate with MBE growers with experience in III-V heteroepitaxy on Si.

(b) Patterning of InSb: Now, the seed area is fully formed, enclosing the Si V groove and the amorphous InSb layer. InSb is sensitive to hydroxide-based chemicals. They tend to get etched by resist removers and buffered oxide etch and therefore need to be protected from subsequent processing steps. Hence, the InSb layer is covered with a thin (3 nm) Al_2O_3 layer by atomic layer deposition to protect it from subsequent processing. The 3-inch Si wafer was diced at this stage to 10*8 mm samples to perform further processing steps. By having a long seed area trench, were now had the flexibility to desired InSb structures with good alignment to the seed area. The InSb was then patterned into structures with dimensions 10 µm long and with different widths (200 nm-1µm) with EBL using a negative resist (ARN 7250.17). Severe adhesion problems were observed when this resist was used on the Al_2O_3 surface; therefore, to improve the adhesion of the resists, the samples were treated in an HMDS oven at 110 °C for 5 min. The patterned InSb structures were then etched using $CH_4/H_2/Ar$ chemistry in ICP-RIE at 110 °C. The etch step was conducted at higher temperatures to assist the desorption of the byproduct trimethylindium from the sample surface. Following the dry etch step, the resist was removed using acetone and isopropanol and prolonged oxygen plasma (30 min) to ensure there were no organic residues on the sample. The Al_2O_3 protective layer on InSb prevents it from getting oxidized during this step.

(c) Micro crucible deposition: Once the InSb is patterned, the structures need to be covered with a thick dielectric layer (also referred to as a capping layer) to hold the structures' shape and prevent leakage of the material during the annealing process. The material quality and the thickness of the dielectric layer have a crucial role in the RMG process. In this work, ICPCVD SiO_2 and Si_3N_4 were two options for the capping layer. X-ray reflectometry measurement (XRR) and BOE etch tests were used to determine the best

possible capping layer for the RMG process. With SiO_2 as the capping layer, significant leakage of the InSb material was observed after the annealing process. This is attributed to the low density of SiO_2 films. On the other hand, Si_3N_4 is an efficient diffusion barrier and results in less material leakage. But, the quality of the ICPCVD deposited Si_3N_4 is not dense on the step structures or the vertical surface, thus leading to leakage at the edges of the InSb structures. To mitigate this issue, we first deposit a conformal Al_2O_3 layer which would act as an intermediate capping layer before the Si_3N_4 layer. The thickness of the Al_2O_3 layer should be 10 nm. Layers thicker than 10 nm would lead to crystallization of the Al_2O_3 layer at random surfaces, which is hard to etch away without damaging the InSb underneath.

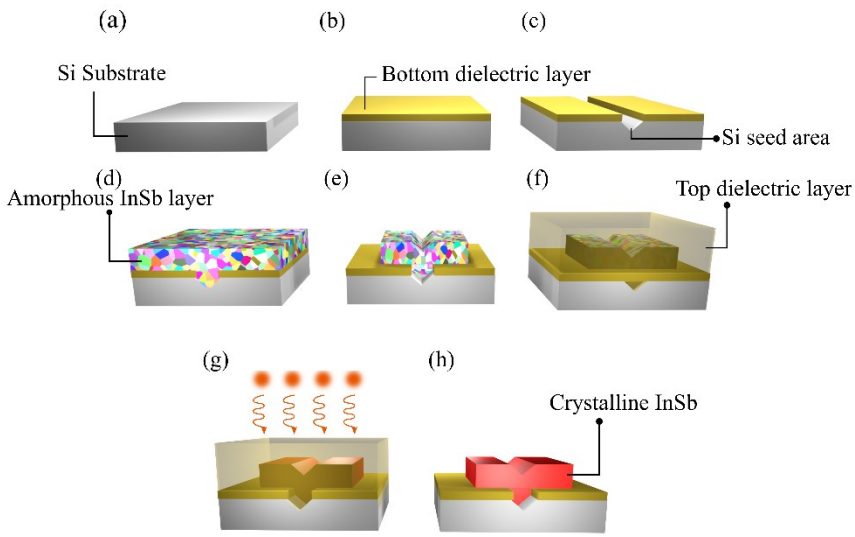


Figure 5.1 Schematic illustration of RMG process a) Si (001) substrate b) Deposition of bottom dielectric (PECVD Si_3N_4 layer) c) Si_3N_4 and seed area patterning d) Deposition of amorphous InSb using MBE e) Patterning of InSb c) Capping of the InSb using a top Si_3N_4 dielectric layer g) Flash annealing of the sample leading to the formation of single crystalline InSb h) Removal of Si_3N_4 revealing the single crystalline InSb

(Note: It is vital that the micro crucible must be able to hold the melted target material without any leakage. A conformal deposition is not always

necessary if the crucible can provide good sidewall coverage. In this work, the ICPCVD deposited Si_3N_4 has poor sidewall coverage, and therefore, a thin layer of Al_2O_3 was used before Si_3N_4 deposition to overcome the leakage of material when annealed. The stack containing the bottom Si_3N_4 layer, Al_2O_3 intermediate capping layer, and top Si_3N_4 capping layer is referred to as the micro crucible.)

(d) Thermal Annealing: After the capping of the InSb structures, InSb is annealed above the melting point using FLA. The sample is preheated to 335 °C and pulsed with 1.5 ms of white light with 19.5 J cm^{-2} energy density. This work prefers FLA over rapid thermal annealing (RTP) for two reasons. Firstly, in the RTP annealing process, the InSb is held in a liquid state for a longer time when compared to FLA, and thus causes the formation of voids in InSb structures due to the diffusion of In and Sb into the crucible during the annealing process. The FLA, on the other hand, mitigates this issue due to the millisecond annealing time. Secondly, FLA is more CMOS compatible as the preheating temperature is below 400 °C, and the annealing is completed in milliseconds without affecting the underlying Si.

The melting temperature has a key role in the RMG process. If the annealing temperature is less than the melting temperature of InSb, InSb will not melt, and there will be no rapid growth. InSb will remain in an amorphous state. The main requirement for rapid melt growth is that the material should be in a melt state. Annealing temperatures greater than the melting point may affect the thermal mismatch. For ternary semiconductors and alloys, annealing temperature must be selected carefully as an increase in annealing temperature could increase the Si diffusion into the melt. Since the InSb melting point is low, we do not have to consider the problem of Si interdiffusion.

(e) Removal of Micro Crucible: Following the flash annealing of the InSb structures, the capping layer is removed. The capping layer should be such that it can be easily removed after the annealing step. Since InSb is etched by BOE (1:10) and HF, wet etching of the Si_3N_4 cannot be adopted. Therefore, the Si_3N_4 capping layer is removed with reactive ion etching (RIE) using SF_6 and O_2 chemistry. Following this, Al_2O_3 intermediate layer is partially etched using BOE (1:30), leaving 5 nm of Al_2O_3 on top of InSb, which serves as a passivation layer for the crystalline InSb. Once the crucible is removed, the annealed target material is characterized using a scanning

electron microscope, electron backscatter diffraction, and electrical characterization.

5.2 Thermodynamic Modelling for RMG InSb

To understand the crystal growth process in RMG, it is essential to understand the thermodynamics involved using the macroscopic quantities. To this end, I have applied the thermodynamic model introduced by Liu et al. [107] to the RMG of InSb.

RMG is similar to liquid phase epitaxial growth in that the main phases involved in an RMG process are the liquid and crystalline solid. When the material is annealed and cooled down, nucleation of the solid phase from the melt is driven by the undercooling of the liquid. If the cooling process is extremely fast, there may not have been time for nucleation, and the liquid will be frozen, resulting in amorphous material. At more reasonable cooling speeds, thermodynamic driving forces are in play, and to understand these, we must investigate the classical theory of nucleation. APPENDIX provides an in-depth discussion of all the equations and concepts used in this section.

Parameters required for crystallization.

The crystallization process involves two key concepts: the driving force for crystallization and atomic motion. To understand the crystallization process, we consider the classical nucleation theory.

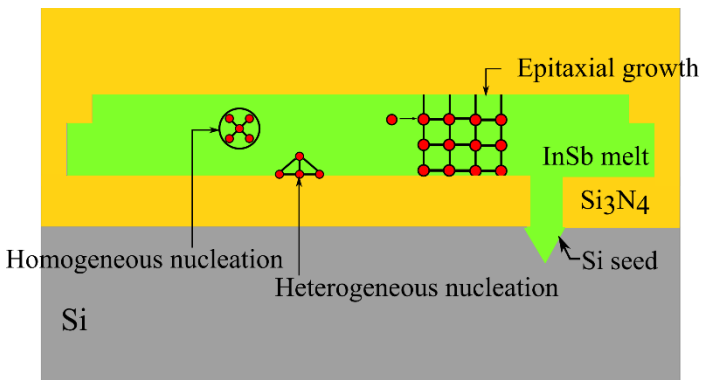


Figure 5.2 Schematic illustration of random nucleation (homogeneous and heterogeneous) and epitaxial growth front.

The growth of the crystalline layer happens when it is initiated by a nucleation process. Once a stable nucleus is formed, the crystal grows. There are two types of nucleation according to the classical nucleation theory: homogeneous and heterogeneous nucleation. In homogeneous nucleation, nucleation occurs spontaneously and randomly in a homogenous initial phase. In heterogeneous nucleation, the nucleus is formed at a preferential site (foreign particles, walls of the container, or other interfaces). An in-depth discussion on this section is available in APPENDIX. Nucleation can occur in three places, homogeneously inside the melt, heterogeneously on the inside walls of the crucible, or on the Si seed surface where we want it (Fig 5.2). The first step is to calculate the critical radius of the nucleus and the critical free energy for the formation of the nucleus using eq I.9 and eq I.10 (in APPENDIX). The driving force for crystallization can be extrapolated from eq (I.6) in terms of J/atom unit as:

$$\Delta G_A = \frac{\Delta H_F \Delta T}{N_{av} T_m} \tag{5.1}$$

Where N_{av} is Avogadro's constant, for InSb, the enthalpy of fusion ΔH_F = 47.73 kJ/mol[108], and the melting temperature T_m is 800 K. Once the driving force ΔG_A is calculated, the next important parameters to determine are the liquid-solid interface energy, the activation energy ΔG_M' for the atomic jump from liquid to solid[109], and the atomic jump frequency. The interface energy is calculated following the equations of Turnbull[110], and the value obtained is 0.152 J/m^2. The self-diffusion activation energy of the liquid InSb is not trivial to find. A theoretical and experimental value of liquid InSb activation energy was reported by Wu et[111]. These values correspond to 0.2 eV and 0.3 eV. For our simulation, we assume a range from 0.1 eV - 0.3 eV. The activation energy of 0.1 eV corresponds to 1.76*10^{-20} J for each atom, and for 0.3 eV corresponds to 4.8*10^{-20} J for each atom. The calculations below correspond to ΔG_M = 1.76 *10^{-20} J for each atom. Finally, the value of the atomic jump frequency is assumed to be a standard 1 *10^{12} Hz. With these parameters, the homogeneous nucleation rate can be determined (eq I.14 APPENDIX).

Moving on, to calculate the heterogeneous nucleation rate, the next critical parameter is the contact angle of InSb with the crucible wall. This parameter significantly influences the heterogeneous nucleation rate, and it is challenging to get the exact contact angle value. However, there are a few reports of the contact angle of semiconductors on oxides. For example, InSb on SiO_2 has a contact angle of 110°, whereas GaAs has a very similar contact

angle of 115° on SiO_2 and a contact angle of 111° for Al_2O_3 surfaces[112]. Interestingly, the contact angle of Ga droplets on GaAs substrates under high vacuum ranges from 90 -130° for different crystalline surfaces. Therefore, for our model, we assume the contact angle of InSb to be in the range of 90 -110° is reasonable since the heterogeneous nucleation starts at larger undercooling at larger angles. It should be noted that no references on the contact angle between InSb and Si_3N_4 were obtained; therefore, a contact angle of 90° is assumed for the heterogeneous nucleation calculations on Si_3N_4 surfaces.

Once all the key parameters are known, we can calculate the growth velocity, homogeneous and heterogeneous nucleation rate. Figure 5.3 a-b illustrates the heterogeneous and homogeneous nucleation rate with temperature. The magnitude of the growth velocity is in the same order of magnitude as reported for the Ge RMG process by Liu et al. The onset of the heterogenous nucleation rate is at a higher temperature than the homogeneous nucleation rate since heterogeneous nucleation requires smaller undercooling when compared to homogeneous nucleation. Also, it is worth noting that the magnitude of the heterogenous nucleation rate is higher than the homogeneous nucleation rate. Figure 5.3 c shows the plot of growth velocity as a function of temperature together with the homogeneous and heterogeneous nucleation rates for the undercooled InSb with dimensions 0.03*1*5 µm on Si_3N_4 as the bottom insulator. The growth rate is in the order of m/sec, meaning the epitaxial growth starting from the seed area can dominate over the random nucleation during the crystallization period. The process window for the epitaxial growth is between 343 °C and 526 °C, resulting in a maximum undercooling of ΔT_m = 184 °C. In this discussion of growth velocity for RMG, the nucleation of InSb crystal at the Si-InSb interface in the seed window is neglected, and only the formation of InSb layers on InSb crystal is considered. The growth rate is in the range of m/sec within the process window, and it is thus sufficient to grow crystals of tens of microns in size for both the rapid thermal annealing process (seconds of cooling time) and flash annealing process (with milli second cooling time).

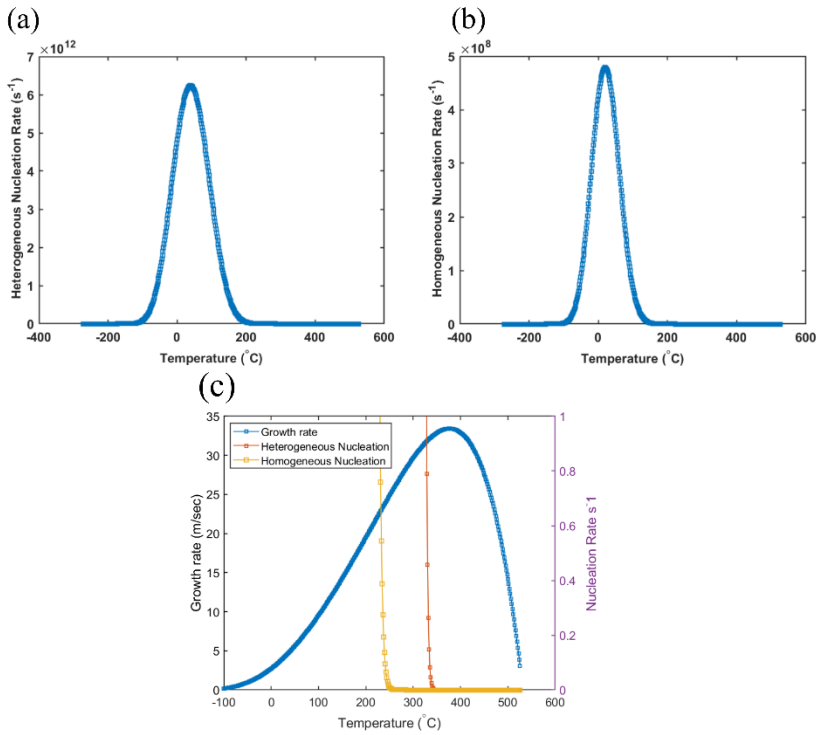


Figure 5.3 Nucleation rate variation with temperature for InSb (a) Heterogeneous nucleation on Si_3N_4 (b) Homogeneous nucleation (c) Variation of the growth rate of InSb crystal with temperature

5.3 Crystallography

EBSD, SEM, HRTEM, and micro-Raman spectroscopy were used to characterize InSb crystals. EBSD was the primary technique to investigate the single crystallinity and orientation of the melt-grown InSb crystals. TEM characterization offers excellent spatial resolution, high precision orientation measurement, and high sensitivity to strain; however, it cannot be used for gathering statistical data, as it requires complicated and tedious sample preparation, and only a limited sample area can be investigated. In contrast, with EBSD, the orientation and single crystalline material statistics can be collected using many devices.

5.3.1 EBSD analysis of InSb structures:

Figure 5.4 shows the inverse pole crystal orientation map of InSb in all three directions obtained using the EBSD method. In this example, the crystal grown from the Si seed has the same orientation as that of the Si at the beginning of the seed area. The straight vertical line indicates the seed area, and the horizontal structure is the crystalline InSb. Additionally, the presence of randomly nucleated crystals within the InSb structure is not present, indicating the single crystallinity of the InSb structure.

The information regarding the crystal orientations and defects, such as lattice rotation and twin defects, can be extracted from the crystallographic maps of InSb structures and are described in the upcoming sections.

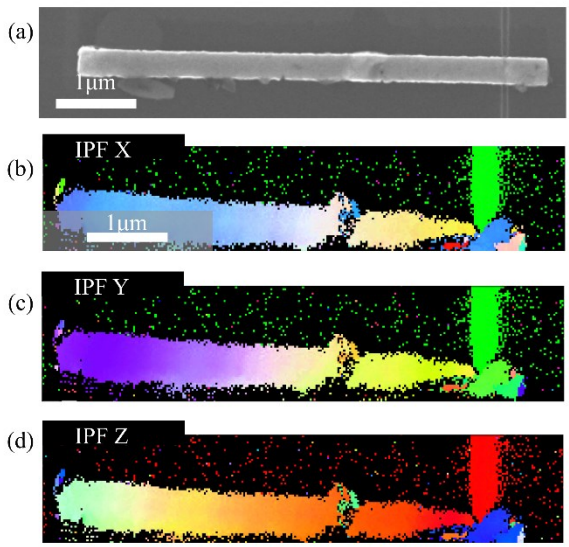


Figure 5.4 a) SEM image of the EBSD scanned InSb structure after flash annealing and removal of the dielectric layer. IPF crystal orientation maps of 5µm long InSb structure in b) X direction, c) Y direction, and d) Z direction.

(i) Analysis of Lattice Rotation in RMG InSb

A commonly reported crystallographic defect in rapid melt-grown structures is lattice rotation. EBSD provides a visual representation of the lattice rotation/ twist that can happen during the melt growth process. In this

example, the crystal grown from the Si seed has the orientation closer to the Si seed orientation. However, towards the middle of the InSb structure, the gradual development of a color change is visible (Fig 5.5 b). This gradual difference represents a twist of the InSb crystal along the growth direction, and here we further discuss the twist and lattice rotation appearing in RMG crystals.

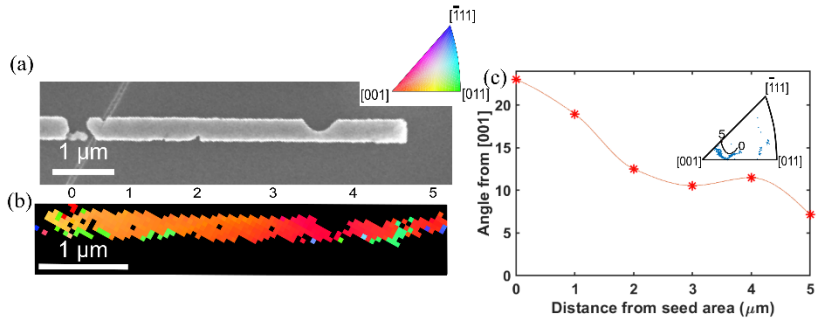


Figure 5.5 a) SEM image of lattice rotated InSb crystal b) EBSD IPF Z map illustrating the lattice rotation c) Misorientation angle with respect to seed orientation along the length of the crystal. Inset showing the lattice rotation in the stereographic projection using inverse pole figure.

Several studies have reported the possible driving forces for lattice rotation in RMG. For example, Toko et al. demonstrated the growth of lattice rotated Ge crystal from Si (111) seed to (100) orientation[113,114]. The study concluded that the rotation occurred to minimize the interface energy between the SiO_2 crucible and Ge as the (100) surface had the minimum surface energy. Another study reported by Tweet et al. explained the increase in lattice twist in the melt growth crystal with the increase in excess annealing temperature above melting[115]. Wen et al. observed Ge lattice rotation directly related to the cooling rate during the annealing process[116]. They concluded that with a higher cooling rate, a steeper temperature gradient at the growth front results in a higher thermal strain, producing lattice rotations in the Ge crystal.

Furthermore, Tanaka et al. have observed lattice rotation in RMG SiGe. The study reported the presence of lattice rotation when the Si concentration gradient is greater than 0.1 % /um[117]. Several other research works on RMG have also studied the effect of Si diffusion on lattice rotations[118].

Figure 5.5 c exhibits the lattice rotation of the InSb crystal and the misorientation analysis. The misorientation analysis measures the lattice orientation at the measurement point and the angular distance with the lattice frame at the reference point (seed area). By making this measurement at points along the length of the InSb structure, a misorientation profile representing the lattice's total angular deviation from the seed orientation is obtained. The maximum rotation angle is defined as the maximum deviation from the seed orientation. It can be seen that the orientation stabilizes closer to (001) orientation.

In our work, we speculate that lattice rotation may occur due to the high thermal strain between the liquid-solid interface. For example, in Ge RMG, the thermal conductivity of solid Ge is higher than in liquid Ge; thus, the latent heat produced at the growth front during annealing is effectively carried away by solid Ge. This effect is even more pronounced for InSb, as the thermal conductivity of solid-InSb is almost twice that of liquid-InSb. This difference in thermal conductivity would create a strong temperature gradient at the liquid-solid interface, resulting in high strain. This increased strain, accompanied by a high crystallization rate, could be the reason for the significant lattice rotation observed in our InSb crystals.

(ii) Presence of Twin Defects

A twin defect is a two-dimensional defect that can be recognized in that the crystal plane order appears mirrored along a certain crystal direction. The defect is commonly observed in III-V compounds, notably In-containing compounds such as InSb, InAs, and InP. The probability of twinning is high for materials with atomic bonds that carry a high degree of ionicity(highly ionic in nature, an element has more electrons than the other).

The creation of a twin defect in diamond and zincblende crystal structures is closely related to facet formation and involves the formation of a new atomic layer. This layer is commonly specified by a rotation of the lattice by 60° about <111> axis. Numerous factors can enhance the presence of twin defects during melt growth: temperature instabilities, the presence of impurities, foreign particles on the melt surface, the contact angle with the inner container, and morphological instabilities of the crystallization front.

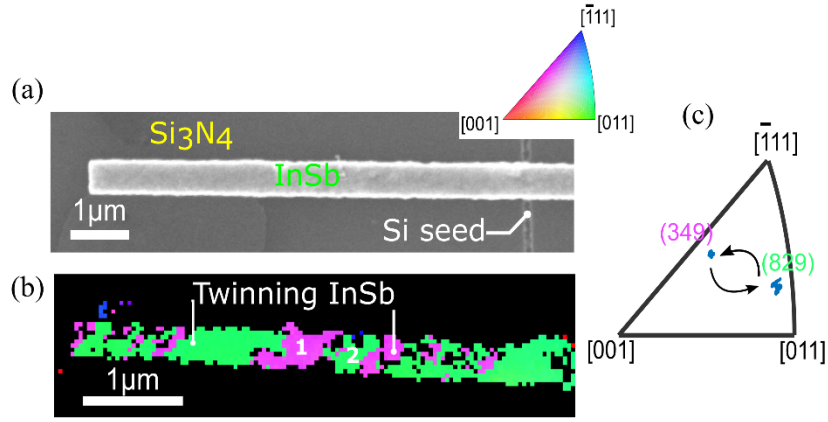


Figure 5.6 a) SEM image of twinning InSb nanostructure b) EBSD IPF Z map illustrating twinning in InSb nanostructure c) inverse pole figure showing the orientation of twin grains in the InSb nanostructure.

Twin defects occur in some of our RMG InSb structures, however, at a relatively low concentration (Fig 5.6). Hulme and Mullin have studied twinning in InSb and reported that In-terminating (111) A direction is more prone to twinning than the Sb-terminated (111) B direction. Growth in (111) A direction would correspond to (111) B edge facet. Thus, a large supercooling and high surface energy of In-terminating facets would result in twinning in InSb crystals. They also reported that facet size, foreign impurities, presence of scum on the melt surface, and met supercooling could be key factors enhancing the twinning in InSb. In our RMG InSb crystals, there was the presence of In droplets in the amorphous InSb layer, indicating that the material was In-rich. This was also confirmed by EDS measurements. Thus, a stochiometric shift in the melt and rough crucible surface could, in our case, could be factors contributing to the disturbance in the growth front resulting in twin defects.

(iii) Epitaxial Relationship

Interestingly, not all the InSb structures indicated an epitaxial relationship with Si at first glance. Therefore, to investigate the crystal orientation relationship between the Si seed and the crystalline InSb, the orientation of 55 InSb nanostructure above the seed area was collected using EBSD. The

collected statistics of the orientations are plotted in the IPF (Fig 5.7) with the intensity of color extending to 5° outside specific orientation.

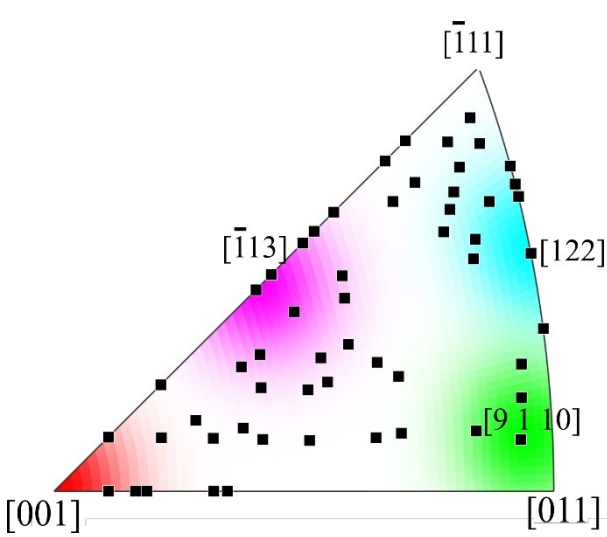


Figure 5.7 Inverse pole figure showing InSb orientations closer to the seed area for 55 structures.

InSb and Si have a high lattice mismatch of 19% which could introduce strain fields at the interface of the InSb melt and Si seed. This could introduce a few degrees of lattice twist, and therefore the spread in the orientations collected is to be expected[119] . However, a cluster of orientation around four specific crystallographic orientations ([001], [113], [9 1 10], and [122]) was observed. [001] orientation represents direct nucleation of InSb melt on the Si [001] plane, indicating an epitaxial relationship. Interestingly, we also find another orientation cluster close to [122], a twin of [001] plane. Twinning and lattice rotations are often observed in the InSb nanostructures have already been discussed in previous sections.

The dominant cluster of orientations is close to [113]. In accordance with previous studies reported by Mori et al., the heteroepitaxy of InSb on V groove Si (001) indicated a 30° rotation around the <111> facets of the V groove. It is observed that such a rotation tends to decrease the lattice mismatch from 19 % to 3.3 %[120,121]. The RMG InSb [001] crystal, if rotated at 30°, would yield an orientation [1 1.3 3.7] that is close to [113]. The twin of this orientation is close to [9 1 10] and is also one of the main clusters in the orientation.

5.4 Electrical Characteristics

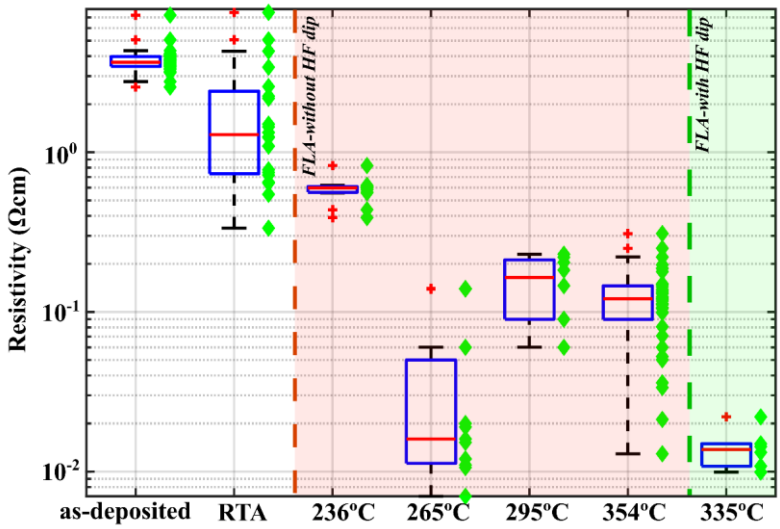


Figure 5.8 Summary of the resistivity of InSb nanostructures annealed using different techniques.

To fully understand the electronic properties of the InSb nanostructure grown by RMG, Ni/Au contacts were evaporated on the devices to make the electrical measurements. Electrical measurement techniques like the Transfer Line Method (TLM), Four probe measurement, Van der Pauw measurement, and Hall measurements were used to obtain the resistivity and the mobility of RMG-grown InSb nanostructures. The resistivity obtained from TLM, Four probe, and Van der Pauw measurements correlated well with each other. Furthermore, the resistivity of the structures was the same regardless of the width of the structures (p=0.001).

Figure 5.8 shows the summary of resistivity extracted from the InSb nanostructures. As-deposited resistivity of InSb refers to the resistivity of the pre-annealed amorphous InSb deposited using MBE. They exhibit the highest mean resistivity of 3.2 Ωcm among all the considerations, which clearly indicates the amorphous nature of the material. As mentioned in the earlier section, both RTA and FLA were utilized to anneal the InSb structures, and a significant difference in the resistivity between both cases

can be observed. RTA-processed InSb structures had a mean resistivity of 1.2 Ωcm, only slightly lower than the amorphous material. In contrast, the resistivity of FLA annealed structures varied very much, from the highest mean value of 0.5 Ωcm (T_{pre}=236 °C) to the lowest mean value of 0.04 Ωcm (T_{pre}=265 °C). These FLA annealed samples (I, II, III, and IV) were polycrystalline due to an interfacial oxide layer between the Si and InSb. Therefore, the variation between devices is rather large, indicating a broad distribution of transport properties, possibly due to a distribution in grain size. Nevertheless, the resistivity of the polycrystalline InSb was, in the best cases, similar to InSb nanowires grown by VLS growth. Single crystalline InSb structures were obtained when the interfacial layer was removed, resulting in less variation between devices and a mean resistivity of only 0.01 Ωcm. Table 5.1 compares the resistivity of InSb nanowires with the RMG InSb.

Table 5.1 Comparison of resistivity of nanowires with RMG InSb nanostructure

Material	Ref	Method	Resistivity (mΩcm)
InSb	[122]	Au seeded InSb NW, MBE	93
InSb	[122]	Au seeded InSb NW, MBE	66
InSb	[122]	Au seeded InSb NW, MBE	45
InSb	[123]	CVD, self-catalyzed growth	100
InSb	[124]	CVD	10
InSb	[125]	Electrochemical	70
InSb	This work	RMG	10

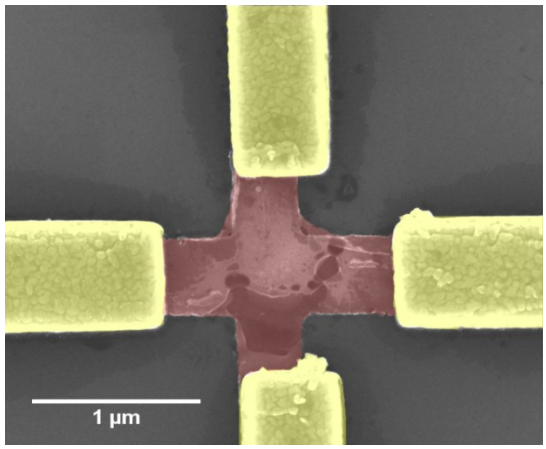


Figure 5.9 SEM image of Hall mobility measured device

Further analysis of the RME InSb was done though Hall and Van der Pauw measurements, through which the electron mobility and the carrier concentration of the InSb nanostructures were extracted in the same geometry. Figure 5.9 shows the SEM image of the contacted InSb hall bar structure, and Table 5.2 summarizes the parameters extracted from the devices.

Table 5.2 Carrier concentration and mobility of InSb nanostructure

Sample	**Carrier Concentration (cm^{-3})**	**Mobility(cm2/Vs)**	**Thickness (nm)**
FLA II	$2.53*10^{17}$	3490	60
FLA V	$6.6*10^{18}$	877	120

The mobility values of the RME InSb are higher than the reported values of InSb nanowires grown using the electrochemical method and CVD[124,125]. However, these values are lower than the bulk InSb. In regards to the thin films, a 0.1 µm InSb thin film grown on GaAs substrate using MBE reportedly has an electron mobility of 1800 cm^2/Vs[126]. RME InSb FLA II sample, in this case, has higher mobility, but in the case of the FLA V sample, it is lower due to a rather high carrier concentration. In addition, the lower value of mobility could be attributed to the higher surface roughness in this case[127,128].

Despite the RMG InSb exhibiting low resistivity and high mobility, these values can still be improved. The low-temperature deposition of amorphous InSb on the bottom dielectric Si_3N_4 has a rough surface, and this surface roughness propagates toward all the layers deposited above the a-InSb layer. As a result, the single crystalline InSb formed after annealing has a surface roughness associated with it. Surface roughness impacts the resistivity of the nanostructure, and they can induce changes to the electronic band structures, which in turn acts as scattering potential, thereby reducing the mobility of the carriers[129,130]. Chemical mechanical polishing (CMP) of a-InSb layers prior to processing could mitigate the issue of surface roughness and thereby could improve the resistivity and mobility of the rapid melt-grown InSb structures.

5.5 Metal-Semiconductor-Metal Photodetector

A metal semiconductor metal single nanostructure InSb photodetector was fabricated via the RMG process. The optical characterization and the figures of merit, such as the detector's responsivity and time response, were measured and discussed in detail in this section.

5.5.1 Spectral Response

The Spectral response is a vital parameter of the detector performance, and here we have used FTIR to obtain the spectrally resolved photocurrent. Figure 5.10 shows the photocurrent response from an area of 500 nm *1.1 µm when illuminated by an IR source at 77 K. The bandgap of InSb at 77 K is 0.23 eV, corresponding to a wavelength of 5.6 µm. A photocurrent peak at this energy level indicates the contribution of the photo responsivity of the detector is from an energy level corresponding to the bandgap of InSb. Interestingly, the onset of the photocurrent peak is redshifted to 0.12 eV, and the photo response abruptly decreases beyond 0.18 eV, resulting in a cut-off wavelength of 6.8 µm. This validates that the InSb detector absorbs wavelengths shorter than its critical wavelength and is transparent to longer wavelengths.

The redshift in the onset could correspond to a band tail (Urbach tail) and bandgap narrowing. These effects could be ascribed due to the interaction of electrons and holes with defects, impurity atoms, lattice disorders, and phonons. It is reported InAs bandgap, electron, and hole effective masses showed a 38% decrease due to biaxial tensile stress. This is in line with the

fact that we observe the presence of significant lattice strain (lattice rotation) along the structure and twin defects. Raman spectroscopy measurements have also corroborated the lattice strain and thus confirm this as a possible reason for the band gap narrowing in the detector (Paper III). Strain-induced band gap narrowing is also reported in many other nanostructures and could be advantageous in some cases.

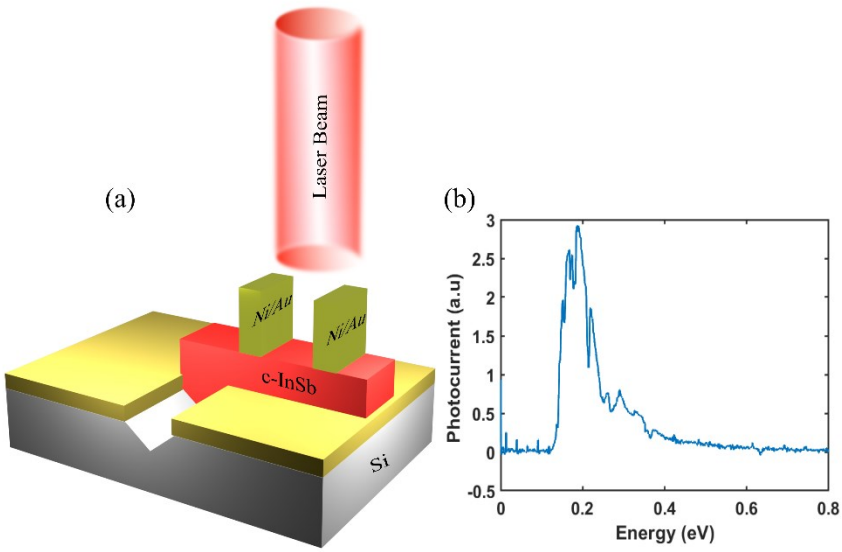


Figure 5.10 a) Schematic of MSM InSb photodetector illuminated by a 1550nm laser beam b) Spectrally resolved photocurrent.

5.5.2 Responsivity

Responsivity measures how many electron-hole pairs are created by incident photons and which are collected by the external circuit. Figure 5.11 a shows the variation in photocurrent with different laser power intensities when a 1550 nm laser is illuminated on the detector. The detector's responsivity can be extracted from the slopes of Fig 5.11 b. The responsivity extracted was 0.5 A/W at 1 V bias for a given illumination area of (0.5*1.1 μm^2) when a power of 16 nW is incident on the device.

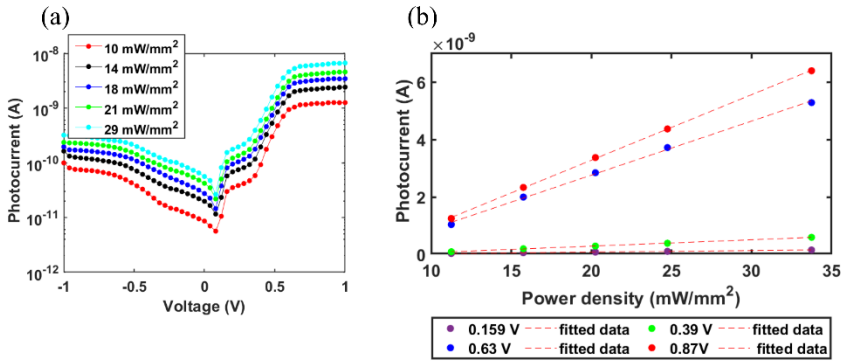


Figure 5.11a) I-V curves under 1550nm illumination with different power densities b) Photocurrent obtained for different power densities for different biases.

To improve the responsivity, we need to maximize the absorption of the incident photons in the semiconductor material. The absorbed photons are a function of reflectivity and the thickness of the semiconductor material. For a given semiconductor material with an incident photon intensity I_0, the absorbed photons are given by $I_0(1-e^{-\alpha d})$, meaning the absorbed photons decay exponentially within the semiconductor material. For our InSb detector, the thickness is 120 nm indicating an absorption of just 20 % for a wavelength of 1550 nm.

Another noteworthy observation of our photodetectors is that there is no anti-reflection (AR) coating on the surface of the semiconductor material. Often, all the incident light is not absorbed within the semiconductor material, a portion of the light is always reflected due to the change in refractive index. For instance, the reflectivity of the surface without a coating is given by:

$$\mathbf{R} = \frac{(\mathbf{n_o}-\mathbf{n_s})^2}{(\mathbf{n_0}+\mathbf{n_s})^2} \tag{5.2}$$

where n_s is the refractive index of the material on the other side of the interface, and n_o is the refractive index of the material of propagation. If we consider the top surface of the RMG InSb photodetector, which includes a thin Al_2O_3 layer, i.e., without an AR coating, 40% of the incident light is reflected from the top surface. Introducing an AR coating on both the detector's top and back surfaces could improve the detector's performance.

Table 5.3 summarizes the characteristics of single InSb NW and nanosheet detectors reported in the literature. These InSb detectors involve a mechanical transfer of the nanosheet or NW onto a Si substrate on which it is processed and contacted. RME InSb detector illustrates monolithic heterogeneous integration of detectors on Si, which is advantageous over other techniques.

Table 5.3 Summary of InSb single nanowire and nanosheet detector performance parameters

Material	Technique	Temp	Power incident	Responsivity (A/W)	Rise time	Ref
InSb nanosheet	MBE	77 K	1.6 nW	14.9	4.2 sec	[131]
InSb nanosheet	MBE	77 K	1 pW	311.5	2.3 msec	[131]
InSb nanowire	Electrochemical	RT	0.49 mW/cm^2	$8.4*10^4$	0.26 sec	[132]
InSb nanostructure	RMG	77 K	16 nW	0.5	65 msec	This work

Finally, we investigate the response time of the InSb detector. The detector's response time is usually limited by RC of the equivalent circuit or the carriers' transit time. However, the capacitance formed in our circuits is in the range of pF, resulting in an RC constant of nanoseconds. This indicates that our detector is not RC limited. In a photoconductor, due to the high electron mobilities, the electrons are captured quickly at the electrodes. This leads to the generation of more carriers until the hole generated is collected at the other end of the electrode. This generally leads to longer carrier recombination time and diffusion time in a photoconductor. In our sample, if we consider the diffusion length to be 1 μm (electrode spacing) and the diffusivity as 22 cm^2/Vs (for holes), the diffusion time results in the range of nanoseconds. However, our detectors have a response time in the range of milliseconds, similar to other NW detectors. Thus, we speculate that the msec range response time of our detector is due to the large surface/volume ratio in the device leading to high surface trap states that can slow down the detector's response.

6

InAs Nanowires on Metal by TASE

Chapter 3 discussed template-assisted selective epitaxy (TASE) on different material systems and its applications in high-speed electronics and optoelectronics. In TASE, generally, III-V is grown from a Si seed inside a lateral or vertical predefined template, which defines the shape of the grown crystal. This chapter will discuss how metals can be utilized as seed areas for the TASE process. Such direct integration on metals, instead of reliance on a crystalline Si substrate, would enable III-V device integration onto a metal layer stack, which could be part of the back end of the line of a Si CMOS chip or a part of a substrate for flexible electronics.

The chapter briefly describes the fabrication process used to prepare the templates for enabling TASE of InAs nanowires onto W metal. Following this section, growth specifics and material characterization of the grown InAs will be discussed. The chapter then concludes with a preliminary demonstration of an InAs barrier detector and its advantages over the InAs photoconductor.

6.1 Fabrication Process

Below is a brief outline of the different steps in the fabrication process of TASE InAs NWs (Fig 6.1):

(a) **Formation of the metallic seed layer and template stack:** To establish the seed layer and template material stack, W was first sputtered on a SiO_2 pre-deposited 2-inch Si wafer. A thin (3-10 nm) Al_2O_3 was deposited using atomic layer deposition (ALD) to act as an etch stop for the later steps. Following this, a 380 nm thick Si_3N_4 film was deposited using ICPCVD with SiH_4 and N_2 precursors at 250°C.

(b) **The patterning of the template:** Once the template stack layers are deposited, EBL is used to define the positions for opening holes in the Si_3N_4 layer. Here AR-P 6200.09 resist was used, but it was found that during the Si_3N_4 etch, the patterns were widened due to resist

thinning, resulting in a tapered geometry of the nanotube templates. Therefore, 30 nm Cr was evaporated above the Si_3N_4 layer and formed a hard mask for the subsequent etch process. Both arrays of nanotube templates with diameters 20, 32, 48, 70, 100, 120 and 300 nm, with three different pitches (500, 1000 and 2000 nm), and single nanotube templates were incorporated in the design. The Cr hard mask was dry etched with ICPRIE using a Cl_2:O_2 chemistry. The AR-P resist was thereafter removed, revealing the Cr hard mask with the openings patterned in it. This was followed by the dry etch of the Si_3N_4 layer using SF_6 and N_2 chemistry. This chemistry was chosen to avoid the formation of chlorofluorocarbons during the prolonged etch of the thick Si_3N_4 layer, typically observed with the common CHF_3-based etch chemistry. Here, the Al_2O_3 layer serves as the etch stop layer for the dry etch step and helps to preserve the W surface from any etch damage. In addition, the Cr mask enables a near-vertical sidewall of 5°, which is crucial to obtain a small diameter nanotube template. Once the nanotube template is formed, the Cr hard mask is removed. This step was followed by the removal of the Al_2O_3 etch stop layer and tungsten oxide layer in the buffered oxide etch before loading the sample in the MOCVD reactor.

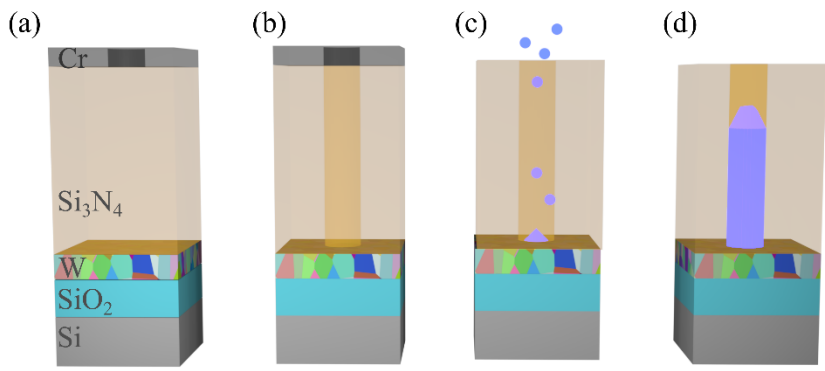


Figure 6.1 Schematic illustration of template fabrication for TASE a) Formation of template openings in Cr hard mask b) Formation of template in Si_3N_4 layer via dry etching c) Nucleation in the template openings during the growth d) InAs nanowire grown inside the Si_3N_4 template.

(c) **Growth of nanowires:** The growth of the nanowires inside the template is carried out using an MOCVD reactor. It is common to use an annealing step at a higher temperature than the growth temperature prior to epitaxial growth in MOVPE to desorb native oxides on the epitaxial substrate, but here this step was excluded to comply with the temperature budget restrictions of BEOL integration. Instead, the reactor temperature was immediately increased to the growth temperature of 450 °C. Trimethylindium (TMIn) and Arsine (AsH_3) were used as the precursors for the InAs nanowire growth.

6.2 InAs Nanowire Growth on W Films

Here the details of the MOVPE process used to grow InAs nanowires on W inside Si_3N_4 nanotube templates are presented. More specifically, the requirements for InAs nucleation, conditions to fill out the nanotubes, and the diameter dependence of the growth process are described in detail.

6.2.1 InAs nucleation on W films

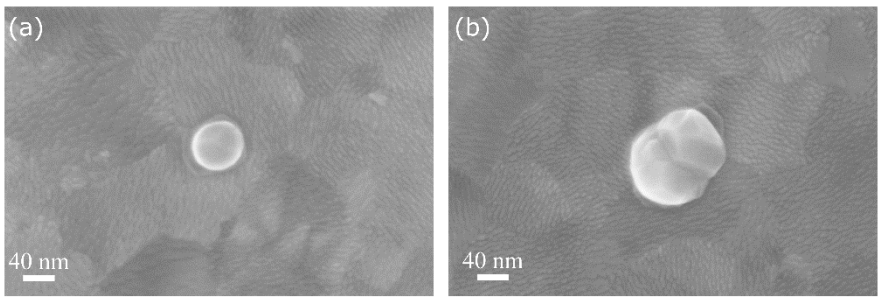


Figure 6.2 InAs crystals after 6 min nucleation on W surface a) 40nm b) 120nm diameter template.

In order to achieve single crystalline InAs nanowire growth, it is critical to control the InAs nucleation events inside the Si_3N_4 template, to avoid InAs nucleation on the inner walls of the nanotube, as well as to ensure that only a single nucleation event occurs on the W film at its bottom. This is critical as the presence of more than one nucleus on the W surface risk leading to polycrystalline growth as the crystalline orientation of each nucleus cannot be controlled and, thus, upon coalescence, will form individual grains of a polycrystal. A pivotal consideration is finding growth conditions that balance the nucleation probability on W compared to the Si_3N_4 template surface. The

nucleation probability must be high enough to ensure single nucleation on the W surface and low enough on the Si_3N_4 surface to avoid nucleation on the inner walls.

Controlling the growth temperature and the V/III ratio could ensure single nucleation events during the growth. The diffusion length of the adatoms typically increases with an increase in growth temperature; thus, a higher growth temperature can ensure that the adatoms reach the bottom of the template surface. Secondly, a low V/III ratio is required for the nucleation to occur. If the group III molar flow is increased beyond a threshold level, there is possibility that the nucleation occurs at the edge of the template mask due to the lower adatom diffusion length.

Importantly, if the W surface is significantly smaller than the adatom diffusion length, then a single nucleus can use the full W surface as a collection area, thus reducing the chemical potential on the surface and, in turn, the risk of subsequent nucleation events. This effect can be observed in Fig 6.2, where tubes smaller than 100 nm in diameter typically only exhibit a single nucleus, indicative of an adatom diffusion length of this length scale or longer.

6.2.2 Conditions to Fill out the Template

In order to fill out the nanotube templates by the growing InAs nanowires, thus the use of the template to decide the shape of the InAs crystal, we found that a two-step growth process is helpful, similar to Kanungo et al.[133] In the first growth step a low V/III ratio (V/III = 20) is used to ensure proper formation of a single nucleus. But with these parameters, the crystal growth is too anisotropic, with a very low growth rate on the {110} planes and a fast growth rate on [111] B[65], and would only partially fill out the template (Fig 6.3). In the second step, we therefore increase the V/III ratio (V/III = 100) to achieve more isotropic growth rates on all major facets, allowing to fill up the template properly.

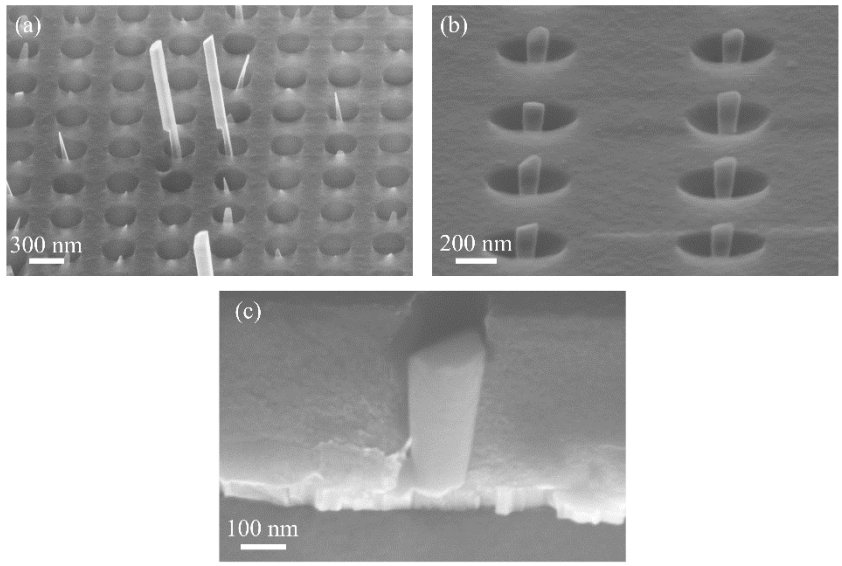


Figure 6.3 SEM image of a) InAs growth using single growth step with low flow and low V/III ratio resulting in partial filling of the template. (b-c) Top view and cross-section of InAs crystals using a two-step growth resulting in complete filling of the template. Note: SEM images are taken from the partial removal of the Si_3N_4 template.

6.2.3 Diameter Dependence of InAs Growth

We studied the dependence of the InAs growth rate on both template diameter, *d*, and pitch between templates arranged in an array. For the smallest diameters, we observe a clear linearly increasing growth rate with increased *d*. In this regime, we also did not see much growth rate variation depending on the pitch. For the larger diameters (>100 nm), we instead see a much weaker growth rate dependence on *d,* while the pitch had a greater effect, with a larger pitch leading also to a higher growth rate (Fig 6.4). The behavior at small diameters can be explained by following the model of Borg et al. [134] who analyzed the mean free path in the vapor of the precursor species and various products of their decomposition. The calculated mean free path was observed to be much longer than the nanotube's inner diameter.

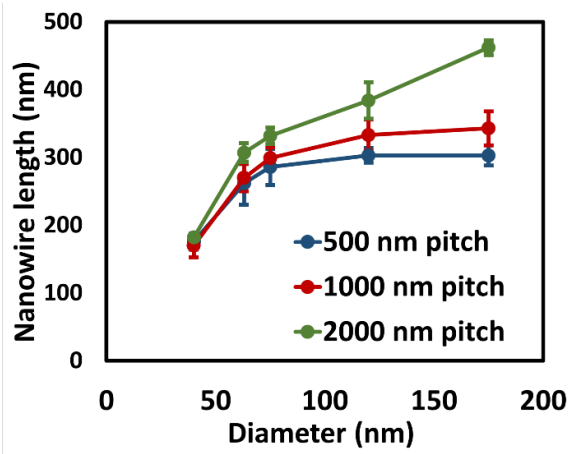


Figure 6.4 InAs nanowire length for different diameter templates and pitches.

When the mean free path between the particle collisions is significantly larger than at least one characteristic spatial dimension of the system, the gas transport regime is referred to as a Knudsen diffusion[135]. The molar flow per area in accordance with Knudsen diffusion in long tubes is given by:

$$\Phi_{Kn}^{i} = \widehat{v_i}\,\frac{\Delta p_i}{3LRT}\,d \qquad (6.1)$$

where $\widehat{v_i}$ is the mean molecular speed of the species i, R is the gas constant, T is the temperature, d is the inner diameter of the template and Δp_i is the pressure difference across the length (L) of the nanotube template. The molar flow per area increases with diameter d; thus, the growth rate will have a linear dependence with d, similar to what we observe also here. Borg et al. did not observe any growth rate dependence on the pitch, while we do for the large diameter regime. This discrepancy can be understood from two differences between our experiments: 1) Our experiments were conducted at a much lower temperature (450 °C) compared to theirs (525 - 600 °C), which will likely increase the contribution of adatom diffusion.

2) There is a significant difference in the template geometry between our case and that of Borg et al., in that they worked with protruding nanotubes for which adatoms would have to first climb up the outer wall of the tube before entering, while in our case they can directly enter from the top of the Si_3N_4 film. In our geometry, therefore, the effective pitch between templates will be shorter than in Borg's geometry, although the distance in the plane of the

substrate is the same. Thus, it is likely that in the large diameter regime where material transport within the templates is fast and not rate-limiting, neighboring templates will compete for growth material, leading to a pitch dependence.

6.3 Structural Characterization of InAs Nanowires

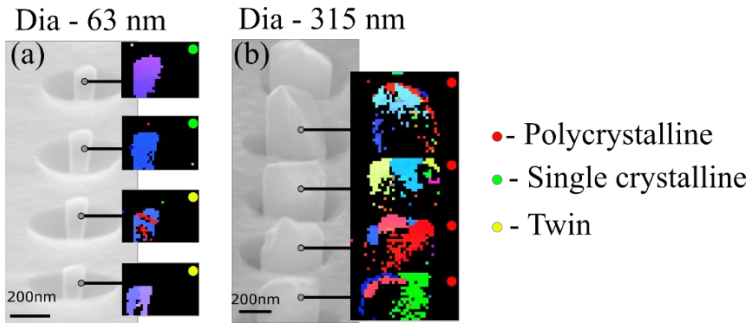


Figure 6.5 EBSD IPF Z orientation map of InAs NW for different nanowires a) 63nm b) 315 nm. The map illustrates the three types of crystals present in the sample – single crystalline, twin, and polycrystalline NWs.

Structural material characterization of InAs NW on W was done using EBSD, SEM, and HRTEM. For this purpose, the Si_3N_4 template was etched away using BOE (1:10) (at least in part) to facilitate measurements. Figure 6.5 illustrates the high-angle SEM images and EBSD orientation maps of InAs NWs with two different diameters after the removal of the template. The relatively high throughput of the EBSD technique allowed us to obtain statistics on the crystallinity of InAs NWs with various diameters which are presented in Paper IV. It was observed that the fraction of polycrystalline NWs increased with the increase in diameter, and for diameters smaller than approximately 63 nm almost all nanowires were single crystalline. This confirms that the probability of more than one nucleation event is higher in larger diameter templates than in smaller templates, with the result of leading to polycrystalline growth. Figure 6.5 shows a 63 nm NW array where all the NWs are single crystalline, although some have occasional twin defects. In contrast, almost all of the wires grown from 315 nm diameter templates are polycrystalline. The single crystallinity as well as presence of stacking faults and twins, were also confirmed using HRTEM (Fig 6.6)

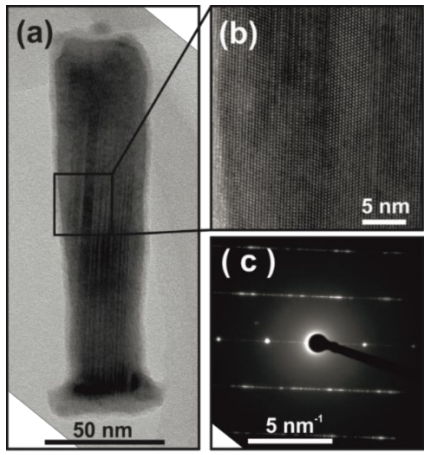


Figure 6.6 HRTEM and SAED pattern of a 40nm InAs NW. The HRTEM indicates the presence of a high density of stacking faults which is also visible through the line streaks in the SAED pattern.

6.3.1 Orientation Relation Between W Grain and InAs

The seed area for the growth of InAs NWs is the sputtered W layer which serves as the basis for nucleation inside the Si_3N_4 template. The W layer is a predominantly α-W phase with grains larger than the smallest template openings in our sample. This is a good indication that we often have only a single or few grains at the bottom of the template.

It is of interest to identify if there is any orientation relation between W and the InAs NWs, indicative of an epitaxial relationship between the two crystals. For this purpose, a sample with InAs grown for only a short nucleation time was investigated with EBSD. The template of this sample was then removed to reveal the InAs crystal and the W grains around it. The InAs and W grains were probed separately, choosing a low acceleration voltage (7 kV optimal) to avoid getting a signal from the W underneath the InAs. Figure 6.7a shows the SEM image of one such investigated InAs crystal, with the positions in which Kikuchi patterns (Fig 6.7 c-g) were collected. Figure 6.7(c-d) shows the Kikuchi pattern generated by the InAs crystal, the similarity of which clearly demonstrates its single crystalline nature. Figure 6.7(e-g) instead shows the Kikuchi pattern generated from the surrounding W grains. It was observed that there were three distinct grains with different orientations in the vicinity of the InAs crystal, either of which may have been where the InAs crystal nucleated.

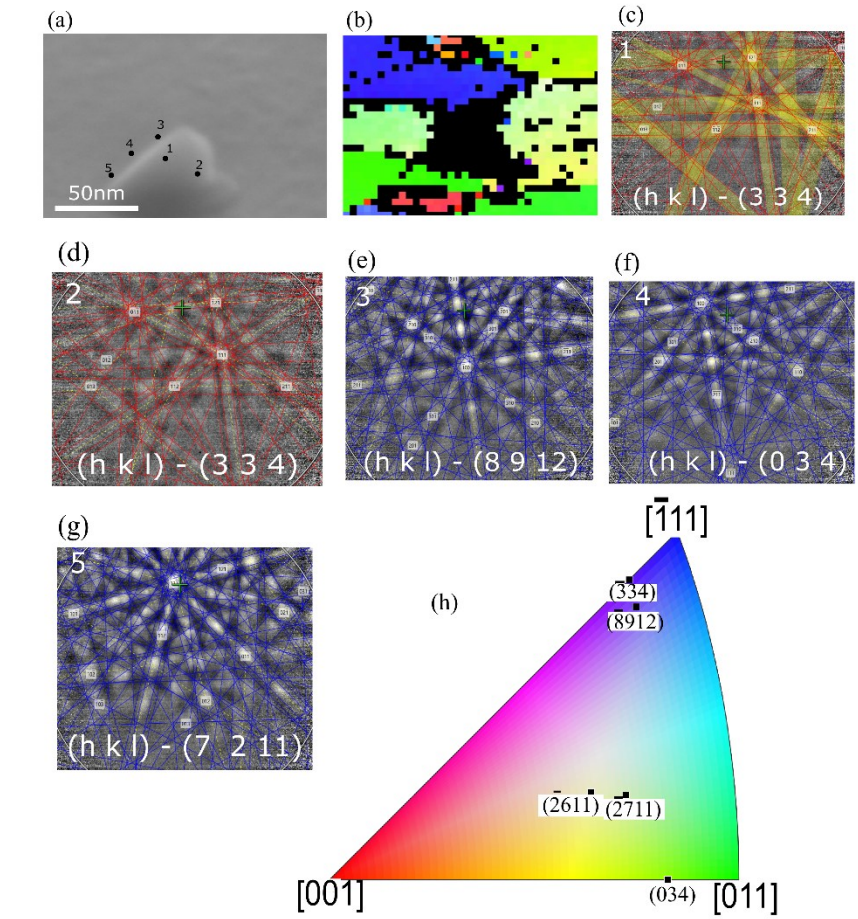


Figure 6.7 a) SEM image of InAs nucleated crystal on W grain b) IPF map of W grains in the vicinity of InAs nucleation(c-d) Kikuchi pattern generated from the InAs crystal (e-g) Kikuchi pattern generated from the W grains (h) Inverse pole figure indicating the orientations of both InAs and W grains.

If we plot these three orientations into an inverse pole figure, we can see that the orientation of W and InAs are not exactly the same. InAs has a (334) orientation out of the plane of the sample, while the three W grains have (8 9 12), (0 3 4), and (7 2 11). However, it is interesting to note that (334) and (8 9 12) lie very close to each other in the inverse pole figure. This could indicate a possibility of epitaxial growth of InAs on the (8 9 12) grain. To

confirm this, we repeated the experiment on other InAs crystals, at present, our data cannot unambiguously confirm such an epitaxial relationship, and we would require more data. However, given the very low signal and weak Kikuchi pattern generated by most of the InAs crystals, obtaining such statistics was considered time-consuming with the current setup and, therefore, not attempted. It will, however, be very interesting for future studies on the topic, as epitaxy between such distinct crystals as W and InAs is seldom observed.

6.4 nBn Photodetector – preliminary results

Conventional photodiodes for infrared detection require to be cooled down to operate with a high signal-to-noise ratio due to the presence of high dark currents in the device. As discussed in Chapter 3, section 3.2.2, an nBn device structure can be used to reduce the dark currents and improve the operating temperatures of the device. In this section, we present the initial measurement results towards an nBn InAs photodetector based on TASE-grown InAs nanowires. An nBn device structure was grown inside the templates fabricated using the same method as mentioned in section 6.1. The InAs contact layer at the bottom of the structure was 100 nm long, a 40 nm long InGaAs barrier layer grown on top of this, and finally, the active layer was grown to fill out the remainder of the template and grown out of the template to form a protruding large active area (protruding NW diameter varies in the range of 200 – 500 nm). To determine the actual effect of the InGaAs barrier, InAs NWs, and InAs barrier structures were contacted to measure the dark currents. The W layer below the structure was used as an ohmic contact to the InAs nanowire. As the top electrode a 10 nm layer of TiN was deposited using ALD to allow good electrical contact without hindering the penetration of infrared radiation onto the active area. This was followed by a thicker second contact layer with Ni/Au electrodes to form measurement pads using a resist lift-off process. Figure 6.8a shows a schematic illustration of the InAs barrier detector structure.

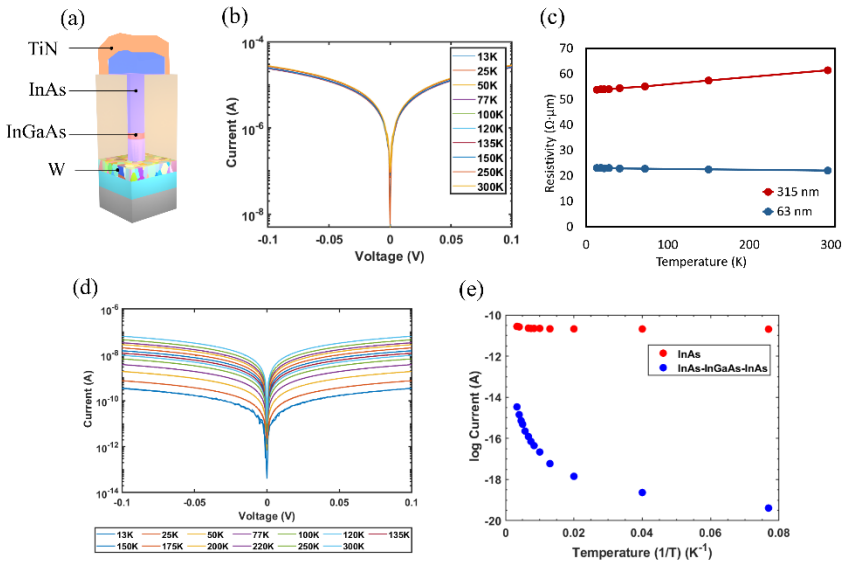


Figure 6.8 a) Schematic of InAs barrier detector b) IV characterization of InAs NW c) Temperature dependence of resistivity of 63 nm and 315 nm InAs NW d) Temperature-dependent IV characterization of 20 nm InAs barrier detector e) Arrhenius plot of InAs and InAs-InGaAs-InAs barrier detector

Temperature-dependent IV characterizations on devices with and without a barrier were performed to understand and study the effect of the barrier inside the InAs NW. Figure 6.8b shows the IV measurement of a 63 nm InAs device without a barrier, and Fig 6.8c shows the resistivity change of 63 nm and 315 nm NWs at different temperatures. The resistivity increases with an increase in diameter which confirms the presence of grain boundaries within larger diameter NWs. However, the InAs NWs exhibit no significant temperature dependence. This could be attributed to Fermi level pinning inside the conduction band, as commonly reported for InAs nanowires[136,137]. These surface states would lead to temperature-independent surface leakage currents. Contrary to the InAs NW device, the InAs barrier detector exhibit significantly lower dark current as well as a stronger temperature dependence(Fig 6.8 d,e). There is a three-order magnitude difference of the dark current between the InAs barrier detector and InAs NW at 150 K.

To determine whether the barrier profoundly affects the dark current, we further analyze the temperature-dependent I-V curve. As previously discussed, the SRH activation energy is $E_g/2$, and the diffusion activation

energy is E_g. However, the activation energy extracted from the Arrhenius plot (ln I vs 1/T) for the temperature range 175 – 300 K (Fig 6.9a) is approximately 0.043 eV and is significantly lower when compared to the previously reported activation energy of the InAs nBn detector.

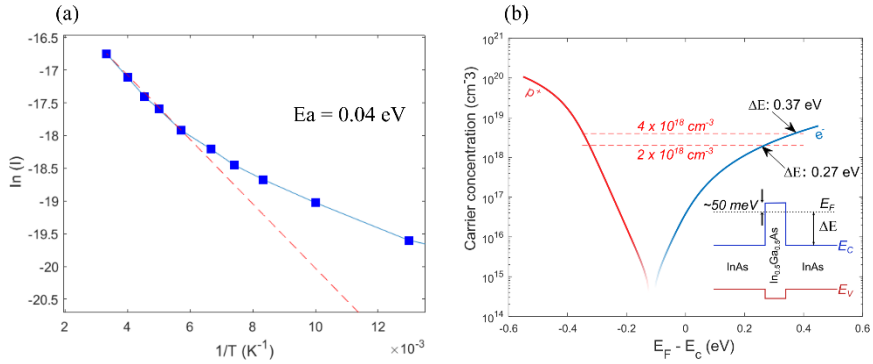


Figure 6.9 a) InAs barrier device Arrhenius plot to extract the activation energy b) Variation of carrier concentration with fermi level position indicating the activation energy for degenerate InAs barrier device.

In our case, the InAs are degenerately doped, indicating that even for InGaAs barrier with 50 % Ga will result in a smaller barrier height with just tens of meV. (Fig 6.9b). This could be the reason why we observe such small activation energy. Furthermore, optical measurements using FTIR, and 1550 nm laser were attempted on the same single nanowire devices and no spectral response and photocurrent was observed for this device geometry. For optimum performance of the nBn detector, future investigation on barrier height, doping concentration and the device geometry and absorber thickness would be beneficial.

7

Conclusion and Outlook

In conclusion, the thesis work aimed to develop and demonstrate integration techniques suitable for realizing monolithically integrated materials and devices for use in infrared detection. Demand for smaller pixel elements in an infrared detection system requires monolithic integrated pixel elements, which could substantially lower the manufacturing cost and be a solution to the alignment issue of sub-10 μm pixel elements in the flip-chip approach. The integration techniques used in this thesis work are Rapid Melt Growth and Template Assisted Selective Epitaxy, which are both Si CMOS-compatible processes and could be a promising way forward for monolithic integrated detector elements. These techniques have previously been studied, and our aim with this thesis was to further develop and demonstrate these techniques for other material systems (InSb for RMG) and on new substrates (W for TASE) suitable for the infrared detection sector.

This thesis can be divided into two main parts, one dedicated to each integration technique of III-V materials – RMG and TASE. Fabrication and growth of InSb (Paper I and Paper II) using RMG has demonstrated single crystalline InSb-on-insulator on Si. Paper III demonstrates, to best of our knowledge, the first monolithically integrated InSb photodetector with a responsivity of 0.5 A/W and spectral response with photocurrent onset near the bandgap of InSb. The versatility of TASE to grow InAs NWs on metallic substrates is demonstrated in Paper IV. The possibility to fabricate a barrier detector using the TASE on W approach is also studied in the thesis. Even though the thesis covers just two integration techniques and their applications in IR photodetectors, some areas could have been explored and studied in more detail. Therefore, as a proposal for future research, examples of some of these topics for further investigation are given below.

RMG is a versatile technique that enables large-area integration of III-V materials with Si and maybe even other substrates. It would be interesting to study how the laser annealing technique could affect length, width, different geometrical patterns, and the defects of grown III-V materials on Si or any other substrates. Furthermore, since laser annealing can be employed on a specific sample area, it would be interesting to explore the possibility of both detector and light-emitting diode III-V materials integrated on the same

substrate. It would also be interesting to study in more detail if the dielectric (bottom and top) thickness affects the lattice rotation observed in the InSb crystals.

Successful integration of InSb photodetector using RMG on Si paved the way for further interesting studies in this area. It has been reported that both SiNx and SiN_x/MgF_2 have good transmissivity (above 60 %) around 4.5-5 μm. One exciting study will be to use these materials as an antireflection coating to improve the detectivity and responsivity of the InSb photodetector. Noise present in the detector is an area that was not explored in the thesis, and it would be beneficial to include noise measurements of the detector for future experiments. These experiments would provide further optimization of the detector performance.

Furthermore, when it comes to research in TASE, many exciting studies are possible. Currently, the device measured were single nanowires. If one could manipulate the device structure, we could improve and extract more performance from the detector. For instance, the device's geometry can be tuned to funnel or T shape to provide a larger absorption area. The barrier composition and position inside the InAs NW can be varied to study the change in dark current levels. Also, given the fact that we see an impact of the absorber doping concentration in the detector performance, it could be interesting to investigate the electrical and optical properties of nBn device based on the absorber doping. Arrays of NWs can also be contacted to extract the figure of merits of the nBn detector.

The rapid advances in the III-V semiconductor and the advent of the barrier detector have led to a new generation of cost effective and high performing IR detectors. Although the integrated materials have a long way to get to the state of the art performing IR detectors, I firmly believe and hope that monolithically integrated IR detectors will be a game changer and will be an important milestone in the generations of the IR detectors to come.

APPENDIX

Thermodynamic Modelling of the RMG process

This section discusses the thermodynamic description of the RMG process using macroscopic quantities. The growth of a crystalline material requires deviation from the equilibrium. The temperature variation at constant pressure between the equilibrium temperature and the controlled temperature can be considered as a deviation from the equilibrium state. For liquid solid equilibrium the undercooling or supercooling $\Delta T = T_m - T$, where T_m is the melting temperature.

The two phases involved in RMG are liquid and crystalline solid. The driving force for the RMG process is the energy difference between the undercooled liquid and the crystalline solid. The formation and growth of solid nuclei leads to crystal formation.

If we are taking the thermodynamics of this process into account, assuming constant pressure, during the crystallization process the Gibbs free energy will decrease.

$$\Delta G = G^l - G^S \tag{I.1}$$

where ΔG is the driving force, G^l is the Gibbs free energy of the liquid and G^S is the Gibbs free energy of the solid. Change in Gibbs free energy at constant pressure in terms of enthalpy difference (ΔH) and entropy difference (ΔS) is given as:

$$\Delta G = \Delta H - T\Delta S \tag{I.2}$$

ΔH and ΔS in terms of a crystallization process are given by:

$$\Delta H = H^l - H^s = \Delta H_F + \int_{T_m}^{T} \Delta C_p dT \tag{I.3}$$

$$\Delta S = S^l - S^s = \Delta S_F + \int_{T_m}^{T} \frac{\Delta C_P}{T} dT \tag{I.4}$$

ΔH_F, ΔS_F, and ΔC_P are the heat of fusion, entropy of fusion and heat capacity at constant pressure

When the material is melted, the system is in equilibrium, i.e., when $T = T_m$, $\Delta G=0$. If we assume that there is no heat capacity difference between the liquid and the solid phases then, at equilibrium

$$\Delta H_F = T_m \Delta S_F \tag{I.5}$$

When the system is away from equilibrium Gibbs free energy change can be written as:

$$\Delta G = \Delta H_F \frac{\Delta T}{T_m} \tag{I.6}$$

where ΔT is the undercooling. This equation is the Turnbull equation[138] for solidification, valid when the undercooling is small.

For crystallization to occur, there are two concepts we have to consider: driving force for crystallization and atomic motion. The driving force for crystallization increases linearly as the undercooling increases whereas the atomic motion increases exponentially with temperature. At low temperatures, even though the driving force is high, the crystallization rate might be very low i.e., the atoms will be frozen to their positions. Therefore, in order to understand the crystallization process, it is important to look into the classical nucleation theory in addition to the thermodynamic driving force.

Classical Nucleation Theory:

Growth of a crystalline layer proceeds by attachment of atoms or molecules to the surface. Growth is initiated by some nucleation; small clusters of particles form nuclei of the solid. Once a nucleus reaches a critical size it stabilizes and the crystal grows. There are two types of nucleation according to the classical nucleation theory: Homogeneous nucleation and heterogeneous nucleation.
In homogeneous nucleation, nucleation occurs spontaneously and randomly in a homogenous initial phase. In heterogenous nucleation, the nucleus is formed at a preferential site (foreign particles, walls of the container or other interfaces).

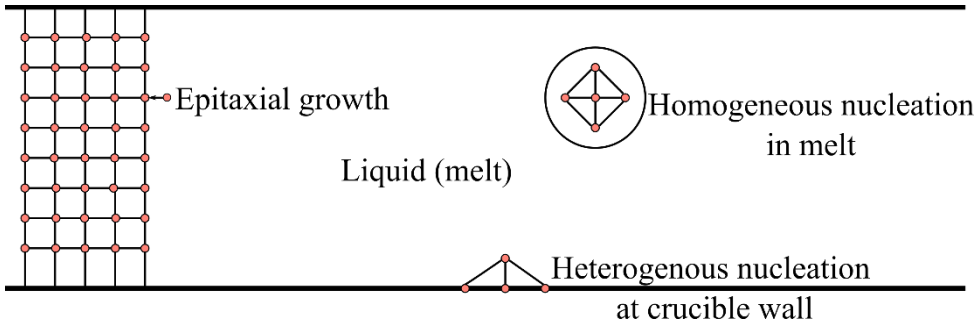


Figure I.A Illustration of three possible crystal growth formation: homogeneous, heterogeneous and epitaxial growth

During nucleation, a new phase with an interface at the boundaries to the initial phase is formed. If the energy released by forming the volume of the new phase is not enough to surpass the cost of creating the new surfaces, nucleation will not proceed. A critical size of the nucleus is therefore required to realize homogeneous nucleation. When a nucleus is formed, there is change in Gibbs free energy (ΔG_N). ΔG_N has two contributions.[21] First, a volume of the new phase is formed, assuming that this phase is the more stable phase at the current temperature the process liberates energy proportional to its volume ($\Delta G_V < 0$). Second, an interface between the new stable phase and the initial metastable phase must be created, surface which typically carry a positive interfacial energy, due to for example dangling chemical bonds. This gives a positive ΔG_S term. For a spherically shaped nucleus,

$$\Delta G_N = -\frac{4}{3}\pi r^3 \Delta G_V + \Delta G_S \quad \text{(I.7)}$$

$$\Delta G_S = 4\pi r^2 \gamma_{ls} \quad \text{(I.8)}$$

where r is the radius of the nucleus and γ_{ls} is the liquid-solid interface energy.

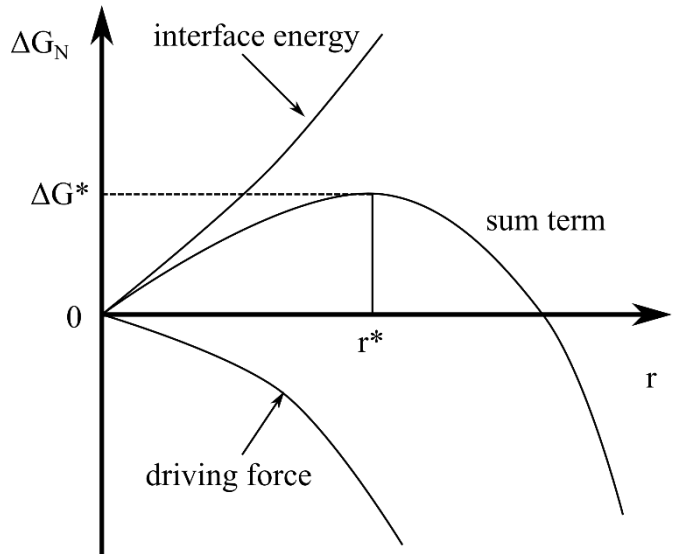


Figure I.B Illustration of radius dependence on the total free energy change corresponding to nucleus formation.

As shown in the Figure I.B, the total energy ΔG_N first increases to a peak value at r^*, and then decreases with the further increase in r. If growth is interrupted while r is smaller than r^*, the nucleus tends to shrink to decrease the total free energy. But when r is greater than r^*, nucleus shrinkage would increase the total energy. At this stage the nucleus is stable. r^* is the critical size of the nucleation and the total energy associated for the formation of this nuclei is called the nucleation barrier and is represented by ΔG^*. This is the energy barrier that the nucleus has to overcome in order to survive as a stable nucleus. The number of atoms in this nucleus with r^* radius is denoted as n^*.

The critical radius r^* and nucleation barrier ΔG_N is given by:

$$r^* = \frac{2\gamma_{ls}}{\Delta G_V} \tag{I.9}$$

$$\Delta G^* = \frac{16\pi {\gamma_{ls}}^3}{3{\Delta G_V}^2} \tag{I.10}$$

The next step is to calculate the nucleation rate. In order to calculate the nucleation rate, it is important to find how many nuclei there are in the undercooled liquid. The population of nuclei is a function of total free energy change or the nuclei size.

The two theories widely used to predict the distribution of the solid particles in the undercooled liquid are Volmer-Weber theory[139] of nucleation and Becker and Döring theory of nucleation[140] In both the theories, the population of particles increases exponentially as the free energy change decreases. We use the Becker and Döring theory (widely used) in which the nuclei population is predicted as

$$Z^* = \frac{N}{n^*}\left(\frac{\Delta G^*}{3\pi kT}\right)^{\frac{1}{2}} \exp\left(-\frac{\Delta G^*}{kT}\right) \quad \text{(I.11)}$$

Where N is the total number of atoms in the system.

Homogeneous Nucleation Rate:

The nucleation rate is given by the number of nuclei that have formed and are about to start growing in an undercooled liquid per unit time. The nucleation rate is the product of number of solid particles, sticking rate and available sites for atomic attachment of those particles. The number of particles can be calculated from the Becker and Döring theory of nucleation. The sticking rate (R) is the rate at which new atoms can attach to the solid particles. The number of available sites can be calculated from the product of surface area A^* of the particle and the area density of the attachment site, σ. Therefore, I_{hom} is given by

$$I_{hom} = R\sigma A^* Z^* \quad \text{(I.12)}$$

where R is dependent on temperature by Arrhenius relationship.

$$R = v_0 \exp\left(-\frac{\Delta G'_M}{kT}\right) \quad \text{(I.13)}$$

where v_0 is the vibration frequency and the $\Delta G'_M$ is the activation energy for an atom to jump across the liquid-solid interface and attach to a new site. Combining I.12 with I.11 and I.13 results in:

$$I_{hom} = \frac{N\sigma A^* v_0}{n^*}\left(\frac{\Delta G^*}{3\pi kT}\right)^{\frac{1}{2}} \exp\left(-\frac{\Delta G'_M}{kT}\right) \exp\left(-\frac{\Delta G^*}{kT}\right) \quad \text{(I.14)}$$

The temperature dependence of the nucleation rate is dominated by the exponential ΔG^* term. But when the temperature is low, the activation energy will play a more prominent role.

Heterogeneous Nucleation and Nucleation Rate:

Heterogeneous nucleation is treated similarly to homogeneous nucleation with the exception that the surface of the nucleus is shared between the solid-liquid interface and an interface to a third material, thus reducing the interface area to the metastable liquid. Therefore, the energy barrier ΔG_N^* is smaller. In the case of RMG, the possible location for the heterogeneous nucleation is from the crucible walls and the seed area.

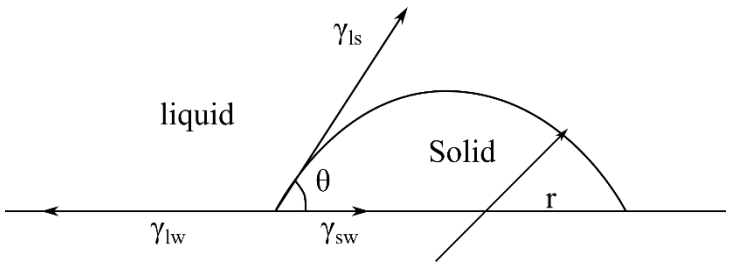


Figure I.C Illustration of solid formed at the interface and the interfacial energies associated with it

Figure (I.C) shows the schematic of heterogeneous nucleation on the crucible wall. Here, the particle takes the form of spherical cap with a wetting angle (contact angle) θ. The radius of the sphere is r. The three different surface/interface energies present during this process are the liquid-solid interface energy γ_{ls}, solid-crucible wall interface energy γ_{sw}, and the liquid-crucible wall interface energy γ_{lw}. Using the Youngs relation for absolute values of energy tension in balance,

$$\gamma_{lw} = \gamma_{sw} + \gamma_{ls}cos\theta \tag{I.15}$$

The volume of the spherical cap is given as:

$$V_s = \frac{1}{3}\pi r^3 S(\theta) \tag{I.16}$$

$$S(\theta) = \frac{1}{4}(2 - 3cos\theta + cos^3\theta) \tag{I.17}$$

where $S(\theta)$ is a geometrical factor depending on the contact angle. The area of the liquid-solid interface and particle-crucible wall interface is given as:

$$A_{ls} = 2\pi r^2(1 - cos\theta) \tag{I.18}$$

$$A_{sw} = \pi r^2 sin^2\theta \tag{I.19}$$

The total Gibbs free energy change for the heterogeneous nucleation will be the sum of energy which drives the phase transition from liquid to solid, creation of new interface with area A_{ls}, and change of interface with area A_{sw} from liquid-crucible wall interface to the solid-crucible wall interface.

$$\Delta G_N = -V_S \Delta G_V + A_{ls}\gamma_{ls} + A_{sw}(\gamma_{sw} - \gamma_{lw}) \tag{I.20}$$

Substituting all the values into Eq. I.20 leads to

$$\Delta G_N = -\frac{1}{3}\pi r^3(2 - 3cos\theta + cos^3\theta)\Delta G_V + \pi r^2 \gamma_{ls}(2 - 3cos\theta + cos^3\theta) \tag{I.21}$$

$$\Delta G_N = (-\frac{4}{3}\pi r^3 \Delta G_V + 4\pi r^2 \gamma_{ls})S(\theta) \tag{I.22}$$

The critical radius is obtained in the same way as for homogeneous nucleation:

$$r^* = \frac{2\gamma_{ls}}{\Delta G_V} \tag{I.23}$$

And the critical energy for heterogenous nucleation is then given by:

$$\Delta G_{hetero}{}^* = \frac{16\pi {\gamma_{ls}}^3}{3{\Delta G_V}^2} \tag{I.24}$$

Heterogeneous nuclei population considering the Becker and Döring nucleation theory is given be:

$$Z_{hetero}{}^* = \frac{\sigma A_w}{n^*}(\frac{\Delta G_{hetero}{}^*}{3\pi kT})^{\frac{1}{2}} \exp(-\frac{\Delta G_{hetero}{}^*}{kT}) \tag{I.25}$$

Where σA_w is the total number of atoms along the crucible wall surface. The heterogeneous nucleation rate will be given by the product of sticking rate (R), the area density σ, the interface area A_{ls} and the nuclei population.

$$I_{Hetero} = \frac{A_w \sigma^2 {A_{ls}}^* v_0}{n^*}(\frac{\Delta G_{hetero}{}^*}{3\pi kT})^{\frac{1}{2}} \exp\left(-\frac{\Delta G_{hetero}{}^*}{kT}\right) \exp(-\frac{\Delta {G_M}'}{kT}) \tag{I.26}$$

Growth velocity:

When a stable nuclei is formed, it will grow with more atoms coming across the liquid – solid interface. There are two possible directions for atoms to move around: sticking to the solid from the liquid or leaving the solid to dissolve in the liquid. Growth happens when the sticking rate is higher than the dissolving rate. The energy barrier for an atom to jump from liquid to solid is equivalent to the activation energy for the jump process, whereas the barrier for an atom to dissolve from solid from the liquid would have an additional energy difference ΔG_d. The jump rate[141] is defined as:

$$R_{l\to s} = n_l a_l v_l \exp\left(-\frac{\Delta G''_M}{kT}\right) \quad \text{(I.27)}$$

$$R_{s\to l} = a_s v_s \exp\left(-\frac{\Delta G''_M + \Delta G_N}{kT}\right) \quad \text{(I.28)}$$

But, at zero driving force, $R_{l\to s} = R_{s\to l}$,

$$a_s v_s = n_l a_l v_l = v_0 \quad \text{(I.29)}$$

The net rate R_N with which the atoms jump from liquid to attach to a site on the solid surface is given by:

$$R_N = R_{l\to s} - R_{s\to l} = v_o \exp\left(-\frac{\Delta G_M''}{kT}\right)\left[1 - \exp\left(-\frac{\Delta G_d}{kT}\right)\right] \quad \text{(I.30)}$$

ΔG_d is the difference between the driving force for the phase transition and the interface energy cost associated with the growth. In RMG, we assume that the growth front is planar and has enough kink sites and ledges at the solid-liquid interface to propel new layer formation. The uniform growth velocity is defined as the product of net jump rate and the distance gained per layer of new atoms.

$$U = a v_0 \exp\left(-\frac{\Delta G_M''}{kT}\right)\left[1 - \exp\left(-\frac{\Delta G_N}{kT}\right)\right] \quad \text{(I.31)}$$

When the undercooling is small ΔG_N is small compared to kT. Therefore, the equation can be simplified to

$$U = a v_0 \frac{\Delta G_N}{kT} \exp\left(-\frac{\Delta G_M''}{kT}\right) \quad \text{(I.32)}$$

Bibliography

1. Langevelde, R. Van, Member, S. & Klaassen, M. Effect of Gate-Field Dependent Mobility Degradation on Distortion Analysis in MOSFET ' s. *IEEE Transactions of Electron Devices* **44**, 2044–2052 (1997).
2. Becker, S. *et al.* Latest pixel size reduction of uncooled IR-FPA at CEA, LETI. in *Electro-Optical and Infrared Systems: Technology and Applications IX* vol. 8541 85410C (SPIE, 2012).
3. Capper, P. & C.T., E. *Infrared Detectors and Emitters: Materials and Devices*. (KLUWER ACADEMIC PUBLISHERS, 2001).
4. Jerram, P. & Beletic, J. Teledyne's high performance infrared detectors for Space missions. in *International Conference on Space Optics* 120 (SPIE-Intl Soc Optical Eng, 2018). doi:10.1117/12.2536040.
5. Huang, E. K. *et al.* Small pixel MWIR sensors for low SWaP applications. in 21 (SPIE-Intl Soc Optical Eng, 2021). doi:10.1117/12.2588774.
6. Lei, W., Antoszewski, J. & Faraone, L. Progress, challenges, and opportunities for HgCdTe infrared materials and detectors. *Appl Phys Rev* **2**, (2015).
7. Raphael Müller *et al.* Thermoelectrically-Cooled InAs/GaSb Type-II Superlattice Detectors as an Alternative to HgCdTe in a Real-Time Mid-Infrared Backscattering Spectroscopy System. *Micromachines (Basel)* **1124**, 11 (2020).
8. Gautam, N. *et al.* Barrier engineered infrared photodetectors based on type-II InAs/GaSb strained layer superlattices. *IEEE J Quantum Electron* **49**, 211–217 (2013).
9. Razeghi, M. *et al.* InAs/InAs 1-x Sb x type-II superlattices for high performance long wavelength infrared detection . in *Infrared Technology and Applications XLII* vol. 9819 981909 (SPIE, 2016).

10. Rogalski, A., Antoszewski, J. & Faraone, L. Third-generation infrared photodetector arrays. *J Appl Phys* **105**, (2009).

11. Gunapala, S. D. *et al.* Toward 16 megapixel focal plane arrays. in *Infrared Systems and Photoelectronic Technology II* vol. 6660 66600E (SPIE, 2007).

12. Gershon, G. *et al.* 3 mega-pixel InSb detector with 10μm pitch. in *Infrared Technology and Applications XXXIX* vol. 8704 870438 (SPIE, 2013).

13. Parrish, W. J., Blackwell, J. D., Paulson, R. C. & Arnold, H. 128 x 128 MWIR InSb focal plane and camera system. in *Infrared and Optoelectronic Materials and Devices* vol. 1512 68–77 (SPIE, 1991).

14. Gurga, A. *et al.* Wafer-scale integration of antimonide-based MWIR FPAs. in *Infrared Technology and Applications XLVII* 29 (SPIE-Intl Soc Optical Eng, 2021). doi:10.1117/12.2588311.

15. Choudhury, D. 3D integration technologies for emerging microsystems. in *IEEE MTT-S International Microwave Symposium Digest* 1–4 (IEEE, 2010). doi:10.1109/MWSYM.2010.5514747.

16. Lu, J. Q. 3-D hyperintegration and packaging technologies for micro-nano systems. *Proceedings of the IEEE* **97**, 18–30 (2009).

17. Rao Tummala, S. R. & Swaminathan, M. *Source : Introduction to System-on-Package (SOP): Miniaturization of the Entire*. www.Digitalengineeringlibrary.com.

18. Liu, W. K. *et al.* Monolithic integration of InP-based transistors on Si substrates using MBE. *J Cryst Growth* **311**, 1979–1983 (2009).

19. Saleh, B. E. A. , & Teich, M. C. ,. SEMICONDUCTOR OPTICS. in *Fundamentals of Photonics* 627–679 (2013).

20. Zimmermann, H. *Integrated Silicon Optoelectronics*. (Springer).

21. Udo W. Pohl. *Epitaxy of Semiconductors- Introduction to Physical Principles*. (Springer Heidelberg New York Dordrecht London, 2012).

22. Demeester, P. *et al.* RELAXED LATTICE-MISMATCHED GROWTH OF IIl-V SEMICONDUCTORS. *Crystal Growth and CharacL* **22**, 53–141 (1991).

23. Park, J. S., Tang, M., Chen, S. & Liu, H. Heteroepitaxial growth of III-V semiconductors on silicon. *Crystals (Basel)* **10**, 1–36 (2020).

24. Liliental-Weber, Z.Sohn & H.-C.Washburn, J. *Structural Defects in Epitaxial III/V Layers*. vol. 38 (1992).

25. Hao, M. *et al.* Characterization and Improvement of GaAs Layers Grown on Si using Ultrathin a-Si Film as a Buffer Layer. *Jpn J Appl Phys* **35**, L960–L963 (1996).

26. Akiyama, M., Kawarada, Y., Ueda, T., Nishi, S. & Kaminishi, K. GROWTH OF HIGH QUALITY GaAs LAYERS ON Si SUBSTRATES BY MOCVD. *J Cryst Growth* **77**, 490–497 (1986).

27. Akiyama, M., Kawarada, Y. & Kaminishi, K. Growth of Single Domain GaAs Layer on(100)-Oriented Si Substrate by MOCVD. *Japanese Journal of Applied Physics Growth of Single Domain GaAs Layer on* **23**, 843 (1984).

28. Yamamoto, A., Uchida, N. & Yamaguchi, M. OPTIMIZATION OF InP/Si HETEROEPITAXIAL GROWTH CONDITIONS USING ORGANOMETALLIC VAPOR PHASE EPITAXY. *J Cryst Growth* **96**, 369–377 (1989).

29. Buzynin, Y. *et al.* GaAs/Ge/Si epitaxial substrates: Development and characteristics. *AIP Adv* **7**, (2017).

30. Nakao, R., Arai, M., Kakitsuka, T. & Matsuo, S. Heteroepitaxial growth of GaAs/Ge buffer layer on Si for metamorphic InGaAs lasers. in *IEICE Transactions on Electronics* vol. E101C 537–544 (Institute of Electronics, Information and Communication, Engineers, IEICE, 2018).

31. Park, J. S., Tang, M., Chen, S. & Liu, H. Heteroepitaxial growth of III-V semiconductors on silicon. *Crystals (Basel)* **10**, 1–36 (2020).

32. Tersoff, J. Dislocations and strain relief in compositionally graded layers. *Appl Phys Lett* **62**, 693–695 (1993).

33. Chen, S. M. *et al.* 1.3 μm InAs/GaAs quantum-dot laser monolithically grown on Si substrates operating over 100°C. *Electron Lett* **50**, 1467–1468 (2014).

34. Fritz, I. J., Gourley, P. L., Dawson, L. R. & Schirber, J. E. Electrical and optical studies of dislocation filtering in InGaAs/GaAs strained-layer superlattices. *Appl Phys Lett* **53**, 1098–1100 (1988).

35. B.D., J. & J.A., B. Selective Epitaxial Deposition of Silicon. *Nature* **195**, 485–486 (1962).

36. Tausch, F. W. & Lapierre, A. G. A novel crystal growth phenomenon: Single crystal GaAs overgrowth onto Silicon dioxide. *J Electrochem Soc* **112**, 706 (1995).

37. Rai-Choudhury, P. Epitaxial Gallium Arsenide from Trimethyl Gallium and Arsine. *J. Electrochem. Soc* **116**, 1745 (1962).

38. Jones, S. H. & May Lau, K. Selective Area Growth of High Quality GaAs by OMCVD Using Native Oxide Masks. *J. Electrochem. Soc* **134**, 3149.

39. Tomioka, K. *et al.* Selective-area growth of III-V nanowires and their applications. *Journal of Materials Research* vol. 26 2127–2141 Preprint at https://doi.org/10.1557/jmr.2011.103 (2011).

40. Marchand, H. *et al.* Atomic force microscopy observation of threading dislocation density reduction in lateral epitaxial overgrowth of gallium nitride by MOCVD. *MRS Internet J. Nitride Semicond. Res* **3**, 3 (1998).

41. B-Y. Tsaur *et al.* Low-dislocation-density GaAs epilayers grown on Ge-coated Si substrates by means of lateral epitaxial overgrowth. *Appl. Phys. Lett* **41**, 347 (1982).

42. Seiichi Sakawa & Tatau Nishinaga. Effect of Si Doping on Epitaxial Lateral Overgrowth of GaAs on GaAs-Coated Si Substrate. *Jpn. J. Appl. Phys.* **31**, L359–L361 (1992).

43. Yoshinori Ujiie & Tatau Nishinaga. Epitaxial Lateral Overgrowth of GaAs on a Si Substrate. *Jpn. J. Appl. Phys* **28**, L337–L339 (1989).

44. Huang, W., Nishinaga, N. T. & Naritsuka, S. Microchannel Epitaxy of GaAs from Parallel and Nonparallel Seeds. *Jpn J Appl Phys* **40**, 5373–5376 (2001).

45. Chang, Y. S., Naritsuka, S. & Nishinaga, T. Optimization of growth condition for wide dislocation-free GaAs on Si substrate by microchannel epitaxy. *J Cryst Growth* **192**, 18–22 (1998).

46. Y.T. Sun*, E. Rodrı́guez Messmer, D. Söderström, D. Jahan & S. Lourdudoss. Temporally resolved selective area growth of InP in the openings off-oriented from [1 1 0] direction. *J Cryst Growth* **225**, 9–15 (2001).

47. Tomiya, S. *et al.* Dislocations in GaN-Based Laser Diodes on Epitaxial Lateral Overgrown GaN Layers. *Physica Status Solidi A Appl Res* **188**, 69–72 (2001).

48. Stromberg, A., Manavaimaran, B., Srinivasan, L., Lourdudoss, S. & Sun, Y. T. Epitaxial lateral overgrowth of GaAsP/Si for tandem solar cell. in *2022 Compound Semiconductor Week, CSW 2022* (Institute of Electrical and Electronics Engineers Inc., 2022). doi:10.1109/CSW55288.2022.9930409.

49. Kataria, H. *et al.* Simple Epitaxial Lateral Overgrowth Process as a Strategy for Photonic Integration on Silicon. *IEEE Journal on Selected Topics in Quantum Electronics* **20**, (2014).

50. Junesand, C., Olsson, F., Xiang, Y., Gau, M. H. & Lourdudoss, S. Heterogeneous integration of indium phosphide on silicon by nano-epitaxial lateral overgrowth. in *Conference Proceedings - International Conference on Indium Phosphide and Related Materials* 59–62 (2009). doi:10.1109/ICIPRM.2009.5012415.

51. J. Z. Li *et al.* Defect reduction of GaAs / Si epitaxy by aspect ratio trapping. *J. Appl. Phys* **103**, 106102 (2008).

52. J.-S. Park, J. Bai, M. C., B. Adekore, M. Carroll & A. Lochtefeld. Defect reduction of selective Ge epitaxy in trenches on Si (001) substrates using aspect ratio trapping. *Appl. Phys. Lett* **90**, 052113 (2007).

53. Wang, G. *et al.* Selective area growth of high quality InP on Si (001) substrates. *Appl Phys Lett* **97**, 121913 (2010).

54. Orzali, T. *et al.* GaAs on Si epitaxy by aspect ratio trapping : Analysis and reduction of defects propagating along the trench direction of defects propagating along the trench direction. *J. Appl. Phys* **118**, 105307 (2015).

55. Waldron, N. *et al.* Replacement fin processing for III-V on Si: From FinFets to nanowires. *Solid State Electron* **115**, 81–91 (2016).

56. B.Kunert *et al.* III / V nano ridge structures for optical applications on patterned 300 mm silicon substrate. *Appl. Phys. Lett* **109**, 091101 (2016).

57. Wang, Z. *et al.* Polytypic InP Nanolaser Monolithically Integrated on (001) Silicon. *Nano Lett* **13**, 5063–5069 (2013).

58. Waldron, N. *et al.* Integration of InGaAs Channel n-MOS Devices on 200mm Si Wafers Using the Aspect-Ratio-Trapping Technique. *ECS Trans* **45**, 115–128 (2012).

59. A. Vais *et al.* First demonstration of III-V HBTs on 300mm Si substrates using nano-ridge engineering. in *IEDM* (IEEE, 2019).

60. Wan, Y. *et al.* Monolithically integrated InAs/InGaAs quantum dot photodetectors on silicon substrates. *Opt Express* **25**, 27715 (2017).

61. Ozdemir, C. I. *et al.* Low Dark Current and High Responsivity 1020nm InGaAs/GaAs Nano-Ridge Waveguide Photodetector Monolithically Integrated on a 300-mm Si Wafer. *Journal of Lightwave Technology* **39**, 5263–5269 (2021).

62. Li, J. Z. *et al.* Monolithic Integration of GaAs/InGaAs Lasers on Virtual Ge Substrates via Aspect-Ratio Trapping. *J Electrochem Soc* **156**, H574 (2009).

63. Borg, M. *et al.* Vertical III − V Nanowire Device Integration on Si(100). *Nano Lett* **14**, 1914–1920 (2014).

64. Pratyush Das Kanungo *et al.* Selective area growth of III – V nanowires and their heterostructures on silicon in a nanotube template : towards monolithic integration of nano-devices. *Nanotechnology* **24**, 225304 (2013).

65. Borg, M. *et al.* Vertical III-V nanowire device integration on Si(100). *Nano Lett* **14**, 1914–1920 (2014).

66. Kanungo, P. Das *et al.* Selective area growth of III-V nanowires and their heterostructures on silicon in a nanotube template: Towards monolithic integration of nano-devices. *Nanotechnology* **24**, (2013).

67. Borg, M. *et al.* High-Mobility GaSb Nanostructures Cointegrated with InAs on Si. *ACS Nano* **11**, 2554–2560 (2017).

68. S. Lee *et al.* High performance InGaAs Gate-All-Around Nanosheet FET on Si Using Template Assisted Selective Epitaxy. in *IEDM* (2018).

69. Wen, P. *et al.* Waveguide coupled III-V photodiodes monolithically integrated on Si. *Nat Commun* **13**, (2022).

70. Yan, Z. *et al.* A monolithic InP/SOI platform for integrated photonics. *Light Sci Appl* **10**, (2021).

71. Khazaka, R. *et al.* Local lateral integration of 16-nm thick Ge nanowires on silicon on insulator substrates. *Appl Phys Lett* **112**, (2018).

72. Šuran Brunelli, S. T. *et al.* Horizontal heterojunction integration via template-Assisted selective epitaxy. *Cryst Growth Des* **19**, 7030–7035 (2019).

73. Borg, M. *et al.* Facet-selective group-III incorporation in InGaAs template assisted selective epitaxy. *Nanotechnology* **30**, (2019).

74. Borg, M., Schmid, H., Moselund, K. E., Cutaia, D. & Riel, H. Mechanisms of template-assisted selective epitaxy of InAs nanowires on Si. *J Appl Phys* **117**, (2015).

75. Liu, Y., Deal, M. D. & Plummer, J. D. High-quality single-crystal Ge on insulator by liquid-phase epitaxy on Si substrates. *Appl Phys Lett* **84**, 2563–2565 (2004).

76. Liu, Y., Deal, M. D. & Plummer, J. D. High-quality single-crystal Ge on insulator by liquid-phase epitaxy on Si substrates. *Appl Phys Lett* **84**, 2563–2565 (2004).

77. Hashimoto, T., Yoshimoto, C., Hosoi, T., Shimura., T. & Watanabe, H. Fabrication of local ge-on-insulator structures by lateral liquid-phase epitaxy: Effect of controlling interface energy between ge and insulators on lateral epitaxial growth. *Applied Physics Express* **2**, (2009).

78. Balakumar, S. *et al.* Fabrication aspects of germanium on insulator from sputtered Ge on Si-substrates. *Electrochemical and Solid-State Letters* **9**, (2006).

79. Feng, J., Liu, Y., Griffin, P. B. & Plummer, J. D. Integration of germanium-on-insulator and silicon MOSFETs on a silicon substrate. *IEEE Electron Device Letters* **27**, 911–913 (2006).

80. Miyao, M. *et al.* High-mobility defect-free Ge single-crystals by rapid melting growth on insulating substrates. in *ICSICT-2010 - 2010 10th IEEE International Conference on Solid-State and Integrated Circuit Technology, Proceedings* 827–830 (2010). doi:10.1109/ICSICT.2010.5667440.

81. Toko, K., Tanaka, T., Ohta, Y., Sadoh, T. & Miyao, M. Defect-free Ge-on-insulator with (100), (110), and (111) orientations by growth-direction-selected rapid-melting growth. *Appl Phys Lett* **97**, (2010).

82. Toko, K. *et al.* Single-crystalline (100) Ge networks on insulators by rapid-melting growth along hexagonal mesh-pattern. *Appl Phys Lett* **98**, (2011).

83. Toko, K., Tanaka, T., Ohta, Y., Sadoh, T. & Miyao, M. Defect-free Ge-on-insulator with (100), (110), and (111) orientations by growth-direction-selected rapid-melting growth. *Appl Phys Lett* **97**, (2010).

84. Tweet, D. J., Lee, J. J., Maa, J. S. & Hsu, S. T. Characterization and reduction of twist in Ge on insulator produced by localized liquid phase epitaxy. *Appl Phys Lett* **87**, 1–3 (2005).

85. Chen, S. L., Griffin, P. B. & Plummer, J. D. Single-crystal GaAs and GaSb on insulator on bulk Si substrates based on rapid melt growth. *IEEE Electron Device Letters* **31**, 597–599 (2010).

86. Matsumura, R., Tojo, Y., Kurosawa, M., Sadoh, T. & Mizushima, I. Growth-rate-dependent laterally graded SiGe profiles on insulator by cooling-rate controlled rapid-melting-growth. **241904**, (2015).

87. Bai, X., Chen, C. Y., Mukherjee, N., Griffin, P. B. & Plummer, J. D. Rapid Melt Growth of Single Crystal InGaAs on Si Substrates. *Advances in Materials Science and Engineering* **2016**, (2016).

88. Koh, H. Y. S., Chen, S. L., Griffin, P. B. & Plummer, J. D. High quality single-crystal laterally graded SiGe on insulator by rapid melt growth. *Electrochemical and Solid-State Letters* **13**, (2010).

89. Bai, X., Chen, C. Y., Mukherjee, N., Griffin, P. B. & Plummer, J. D. Rapid Melt Growth of Single Crystal InGaAs on Si Substrates. *Advances in Materials Science and Engineering* **2016**, (2016).

90. Chen, B. & Chen, Y. Recent Advances in High Speed Photodetectors for eSWIR / MWIR / LWIR Applications. *MDPI Photonics* **8**, (2021).

91. Rogalski, A. Infrared detectors : status and trends. *Prog Quantum Electron* **27**, 59–210 (2003).

92. Rogalski, A., Science, M. & Optoelectronics, I. Infrared thermal detectors versus photon detectors. *Proceedings of SPIE* (1997) doi:10.1117/12.280417.

93. Rogalski, A., Kopytko, M. & Martyniuk, P. Infrared Barrier Photodetectors. *Antimonide-based Infrared Detectors: A New Perspective* 141–184 (2018) doi:10.1117/3.2278814.ch6.

94. Jones, R. C. Performance of Detectors for Visible and Infrared Radiation. *Advances in Electronics and Electron Physics* **5**, 1–96 (1953).

95. R. J. Keyes. *Optical and Infrared Detectors*. *Optica Acta: International Journal of Optics* vol. 28 (Springer, 1981).

96. Panos C. Datskos & Nickolay V. Lavri. Detectors-Figure of of Merit. 349–357 (2014).

97. Goushcha, A. O. & Tabbert, B. On response time of semiconductor photodiodes. *Optical Engineering* **56**, 097101 (2023).

98. Buscema, M. *et al.* Photocurrent generation with two-dimensional van der Waals semiconductors. *Chem. Soc. Rev* **44**, 3691–3718 (2015).

99. Mukhokosi, E. P., Krupanidhi, S. B. & Nanda, K. K. An Extrinsic Approach Toward Achieving Fast Response and Self-Powered Photodetector. *Phys. Status Solidi A* **215**, (2018).

100. Mukhokosi, E. P., Manohar, G. V. S., Nagao, T., Krupanidhi, S. B. & Nanda, K. K. Device Architecture for Visible and Near-Infrared Photodetectors Based on Two-Dimensional SnSe 2 and MoS 2 : A Review. *Micromachines (Basel)* **11**, (2020).

101. Jiang, J. *et al.* Defect Engineering for Modulating the Trap States in 2D Photoconductors. *Advanced Materials* **30**, (2018).

102. Jiang, Y. *et al.* Photoresponse properties of CdSe single-nanoribbon photodetectors. *Adv Funct Mater* **17**, 1795–1800 (2007).

103. Prucnal, S., Rebohle, L. & Skorupa, W. Doping by flash lamp annealing. *Mater Sci Semicond Process* **62**, 115–127 (2017).

104. Lars Rebohle, Slawomir Prucnal & Denise Reichel. *Flash lamp annealing*. vol. 288 (2019).

105. Schwarts, A. J., Kumar, M. & L.Adams, B. *Electron Backscatter Diffraction in Materials Science*. (Springer, 2009).

106. Christian, N., Lassen, K., Christian, N. & Lassen, K. Automated Determination of Crystal Orientations from Electron Backscattering Patterns. (The Technical University of Denmark, 1994).

107. Liu, Y., Deal, M. D. & Plummer, J. D. Rapid Melt Growth of Germanium Crystals with Self-Aligned Microcrucibles on Si Substrates. *J Electrochem Soc* **152**, G688 (2005).

108. Pure Substances. Part4_Compounds from HgH_g to ZnTe_g. in (ed. Lehrstuhl für Theoretische Hüttenkunde, R.-W. T. H. A.) 125–150 (Springer Berlin, Heidelberg). doi:10.1007/10688868_8.

109. Sapkota, G. & Philipose, U. Synthesis of metallic, semiconducting, and semi-metallic nanowires through control of InSb growth parameters. *Semicond Sci Technol* **29**, (2014).

110. Bai, X. M. & Li, M. Calculation of solid-liquid interfacial free energy: A classical nucleation theory based approach. *Journal of Chemical Physics* **124**, (2006).

111. Wu, Y. N., Zhao, G., Liu, C. S. & Zhu, Z. G. Structure and properties of liquid InSb alloy below and above the melting point: Ab initio molecular dynamics simulations. *Journal of Physics Condensed Matter* **18**, 4471–4480 (2006).

112. I.Hartera, P.Dusserrea, T.Duffara, J.-Ph.Nabota & N.Eustathopoulos. Wetting of III- V melts on crucible materials. *J Cryst Growth* **131**, 157–164 (1993).

113. Toko, K., Tanaka, T., Ohta, Y., Sadoh, T. & Miyao, M. Defect-free Ge-on-insulator with (100), (110), and (111) orientations by growth-direction-selected rapid-melting growth. *Appl Phys Lett* **97**, 95–98 (2010).

114. Toko, K., Ohta, Y., Tanaka, T., Sadoh, T. & Miyao, M. Chip-size formation of high-mobility Ge strips on SiN films by cooling rate controlled rapid-melting growth. *Appl Phys Lett* **99**, 1–4 (2011).

115. Tweet, D. J., Lee, J. J., Maa, J. S. & Hsu, S. T. Characterization and reduction of twist in Ge on insulator produced by localized liquid phase epitaxy. *Appl Phys Lett* **87**, 1–3 (2005).

116. Wen, J. J. *et al.* Cooling rate dependent lattice rotation in ge on insulators formed by rapid melt growth. *ECS Solid State Letters* **2**, 73–76 (2013).

117. Tanaka, T., Toko, K., Sadoh, T. & Miyao, M. High quality single-crystalline Ge-rich SiGe on insulator structures by Si-doping controlled rapid melting growth. *Applied Physics Express* **3**, 2–5 (2010).

118. Matsumura, R. *et al.* Growth-rate-dependent laterally graded SiGe profiles on insulator by cooling-rate controlled rapid-melting-growth. *Appl Phys Lett* **101**, (2012).

119. Falub, C. V. *et al.* Perfect crystals grown from imperfect interfaces. *Sci Rep* **3**, 1–6 (2013).

120. Mori, M. *et al.* High quality InSb films grown on Si(111) substrate via InSb Bi-layer. *e-Journal of Surface Science and Nanotechnology* **7**, 145–148 (2009).

121. Mori, M. *et al.* InSb films grown on the V-grooved Si(001) substrate with InSb bilayer. *Phys Procedia* **3**, 1335–1339 (2010).

122. Thelander, C., Caroff, P., Plissard, S. & Dick, K. A. Electrical properties of InAs 1-xSb x and InSb nanowires grown by molecular beam epitaxy. *Appl Phys Lett* **100**, (2012).

123. Sapkota, G. & Philipose, U. Synthesis of metallic, semiconducting, and semi-metallic nanowires through control of InSb growth parameters. *Semicond Sci Technol* **29**, (2014).

124. Wang, Y. *et al.* Field effect transistor based on single crystalline InSb nanowire. *J Mater Chem* **21**, 2459–2462 (2011).

125. Kuo, C. H., Wu, J. M. & Lin, S. J. Room temperature-synthesized vertically aligned InSb nanowires: Electrical transport and field emission characteristics. *Nanoscale Res Lett* **8**, 1–8 (2013).

126. Debnath, M. C., Zhang, T., Roberts, C., Cohen, L. F. & Stradling, R. A. High-mobility InSb thin films on GaAs (0 0 1) substrate grown by the two-step growth process. *J Cryst Growth* **267**, 17–21 (2004).

127. Khanal, D. R. *et al.* Decoupling single nanowire mobilities limited by surface scattering and bulk impurity scattering. *J Appl Phys* **110**, (2011).

128. Ramayya, E. B., Vasileska, D., Goodnick, S. M. & Knezevic, I. Electron mobility in silicon nanowires. *IEEE Trans Nanotechnol* **6**, 113–117 (2007).

129. Wang, F. *et al.* Surface roughness induced electron mobility degradation in InAs nanowires. *Nanotechnology* **24**, (2013).

130. Marom, H. & Eizenberg, M. The effect of surface roughness on the resistivity increase in nanometric dimensions. *J Appl Phys* **99**, (2006).

131. Zhang, S. *et al.* Highly Sensitive InSb Nanosheets Infrared Photodetector Passivated by Ferroelectric Polymer. *Adv Funct Mater* **30**, (2020).

132. Kuo, C. H., Wu, J. M., Lin, S. J. & Chang, W. C. High sensitivity of middle-wavelength infrared photodetectors based on an individual InSb nanowire. *Nanoscale Res Lett* **8**, (2013).

133. Kanungo, P. Das *et al.* Selective area growth of III-V nanowires and their heterostructures on silicon in a nanotube template: Towards monolithic integration of nano-devices. *Nanotechnology* **24**, (2013).

134. Borg, M., Schmid, H., Moselund, K. E., Cutaia, D. & Riel, H. Mechanisms of template-assisted selective epitaxy of InAs nanowires on Si. *J Appl Phys* **117**, (2015).

135. Gruener, S. & Huber, P. Knudsen diffusion in silicon nanochannels. *Phys Rev Lett* **100**, 1–4 (2008).

136. Mead, C. A. & Spitzer, W. Q. FERMI LEVEL POSITION AT SEMICONDUCTOR SURFACES. *Phys Rev Lett* **10**, (1963).

137. Pedrazzani, J. R., Maimon, S. & Wicks, G. W. Use of nBn structures to suppress surface leakage currents in unpassivated InAs infrared photodetectors. *Electron Lett* **44**, 1487–1488 (2008).

138. D.Turnbull. Principles of solidification. in *Thermodynamics in Physical Metallurgy*. 282–306 (1950).

139. M.Volmer & A.Weber. Keimbildung in ubersattigten Losungen. *Zeitschriftfu r Physicalische Chemie* **119**, 277–301 (1926).

140. R.Becker & W.Doring. Kinetische Behandlung der Keimbildung in ubersattigten Dampfen. *Ann. Phys* **24**, 719–752 (1935).

141. P.V. Evans & S.R. Stiffler. *Interfacial atomic transport in the nucleation of crystalline silicon from the melt*. vol. 39 (1991).