Vertical III-V Nanowires For In-Memory Computing

Mamidala, Saketh Ram

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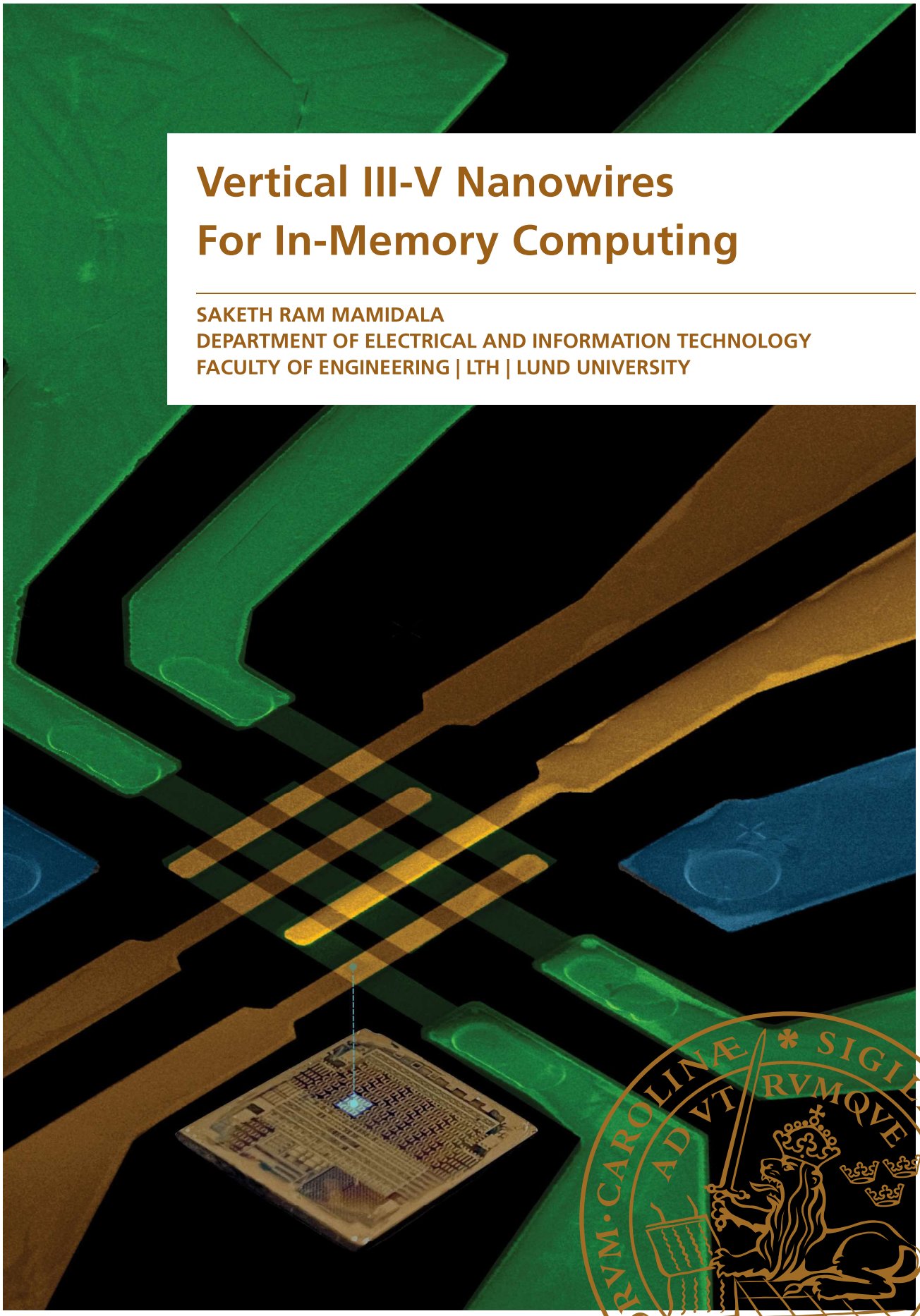

Vertical III-V Nanowires For In-Memory Computing

Doctoral Thesis

Saketh Ram Mamidala

LUND
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Department of Electrical and
Information Technology
Lund, September 2023

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Abstract:
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In this thesis, to achieve a 1T1R cell with a minimal footprint of $4F^2$, a technology platform has been developed to integrate a vertical nanowire GAA MOSFET as a selector device for the RRAM. Firstly, the effect of the geometry (planar to vertical) of the ITO/HfO_2/TiN RRAM cell was studied where low energy switching (0.49 pJ) and high endurance (10^6) were achieved in the vertical configuration. Furthermore, InAs was incorporated as the GAA MOSFET selector channel material to leverage the beneficial transport properties of III-V materials desirable for supply voltage scaling. Finally, an approach was developed wherein InAs is used as the selector channel as well as the RRAM electrode by carefully tuning the InAs native oxides. This thesis also presents low-frequency noise characterization of the RRAM cell as well as the MOSFET to further understand the semiconductor/oxide interface. The vertical 1T1R cell developed in this thesis enables the implementation of Boolean logic operations using a single vertical nanowire while reducing the footprint by 51x when compared to its traditional CMOS counterpart.

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Frontispiece: Fabricated chip housing the vertical gate-all-around 1T1R cells, with the inset showing a zoomed-in scanning electron microscope image of a 4x4 crossbar array present within the chip.

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To *Amma* and *Nanna*

Abstract

In recent times, deep neural networks (DNNs) have demonstrated great potential in various machine learning applications, such as image classification and object detection for autonomous driving. However, increasing the accuracy of DNNs requires scaled, faster, and more energy-efficient hardware, which is limited by the von Neumann architecture where separate memory and computing units lead to a bottleneck in performance. A promising solution to address the von Neumann bottleneck is in-memory computing, which can be achieved by integrating non-volatile memory cells such as RRAMs into dense crossbar arrays. On the hardware side, the 1-transistor-1-resistor (1T1R) configuration has been central to numerous demonstrations of reservoir, in-memory and neuromorphic computing.

In this thesis, to achieve a 1T1R cell with a minimal footprint of $4F^2$, a technology platform has been developed to integrate a vertical nanowire GAA MOSFET as a selector device for the RRAM. Firstly, the effect of the geometry (planar to vertical) of the ITO/HfO_2/TiN RRAM cell was studied where low energy switching (0.49 pJ) and high endurance (10^6) were achieved in the vertical configuration. Furthermore, InAs was incorporated as the GAA MOSFET selector channel material to leverage the beneficial transport properties of III-V materials desirable for supply voltage scaling. Finally, an approach was developed wherein InAs is used as the selector channel as well as the RRAM electrode by carefully tuning the InAs native oxides. This thesis also presents low-frequency noise characterization of the RRAM cell as well as the MOSFET to further understand the semiconductor/oxide interface. The vertical 1T1R cell developed in this thesis enables the implementation

of Boolean logic operations using a single vertical nanowire while reducing the footprint by 51x when compared to its traditional CMOS counterpart.

Popular Science Summary

Answers to complex engineering problems are often found by simply turning to nature. The blade shape of a wind turbine was inspired by the ridges on the pectoral fins of a humpback whale, automobile windshields were inspired by the design of a spider's web to prevent shattering, and wide-field-of-view cameras mimic the vision of aquatic animals. When it comes to computing, a natural comparison drawn is with the biological brain. We know that computers for a given problem, are far superior in terms of calculation speed and precision, but are they energy-efficient? With the rise of artificial intelligence (AI) and data-hungry machine learning, the energy demand on the present computing systems is only increasing.

The fundamental units that build a computer are the processor and memory. The traditional computers we use today are based on the von Neumann architecture, where the memory and processor units are separate. The physical separation poses a severe constraint on further development as the data needs to be constantly shuttled between the two units and is termed the von Neumann bottleneck. The biological brain, on the other hand, can process and store information, making it extremely energy-efficient.

Someone who has taken a basic electronics course can identify the three passive circuit elements: the resistor, the capacitor, and the inductor. There is a fourth fundamental circuit element that was predicted in 1971 and experimentally observed only in 2008: the memristor or the memory resistor. Memristors not only act as storage elements but also enable a new paradigm in computing known as in-memory computing, where the redundancy arising from data traffic can be eliminated.

In this work, we have worked on developing a technology platform for memristors using an unconventional vertical geometry, combining it with a new material system that looks beyond silicon. We also demonstrate basic logic operations that are performed and stored in our energy and area-efficient vertical memristors, without the need to move data between the processor and memory. These memristors are also non-volatile meaning no external power supply is needed for them to remember the programmed state.

AI, while growing at a rapid pace, also asks the question making us rethink: What is the best way to build a computer?

Acknowledgments

REACHING the end of my Ph.D. feels bittersweet, as it marks the end of an incredible chapter filled with cherished memories. To begin with, *Lars-Erik Wernersson*, I am truly grateful to you for giving me this opportunity to work here in Lund. You have been an inspirational mentor, and I look up to your optimism, empathy, and your strategic approach to taking risks.

The guidance provided by my cosupervisors, *Karl-Magnus Persson* and *Johannes Svensson*, has been instrumental in the successful completion of this work. You both have been more than just cosupervisors to me; you have also become cherished friends. *Karl-Magnus*, thank you for teaching me the right way to celebrate every milestone, regardless of its size. *Johannes*, thank you for all the board gaming sessions at your place, concerts, and mid-day walks to buy 'exotic' snacks. Thank you *Mattias Borg* for your valuable input on my first RRAM paper and *Erik Lind* for letting me get a sneak peak of the quantum course. Have to leave on a cliffhanger!

Olli-Pekka Kilpi, thank you for introducing me to the MOSFET fabrication process, Finnish humour and for all the FIFA matches after work. You were definitely the better player. Following the graduation of the previous generation of students/postdocs, I was fortunate to meet another set of passionate and lively students/postdocs: *Ben Nel*, *Hannes Dahlberg*, *André Andersen*, and *Philipp Gribisch*, famously known as the "Cold Swim House" group. You guys made work-life balance challenging for me by significantly raising the fun quotient at work. I will fondly remember our after-work evenings, 5 am ocean dips, cricket discussions, and the eventful hike where *Philipp* nearly set *André's* tent ablaze. I have no doubt that you will continue to carry the same spirit throughout the remaining duration of your PhDs. I would like to extend my gratitude to all the fantastic colleagues within our division for fostering such

a pleasant environment. It has always been a pleasure to find one of you for a cup of coffee and engage in both scientific and non-scientific conversations. Thank you, *Anton Stefan*, *Markus*, *Gautham*, *Adam*, *Anette*, *Lars*, *Abinaya*, *Lasse*, *Heera*, *Fredrik*, *Navya*, *Duc*, *Patrik*, *Robin*, *Louise*, *Sebastian*, *Niklas*, *Alexandros*, *Johan*, *Daniel*, and *Mats*. Special thanks to *André*, *Karthik*, and *Neharika* for helping me out with proof reading and *Marcus* and *Zhongyunshen* for being nice office mates.

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Lund, June 2023

Contents

Preface

This thesis is the culmination of five years of work in the *Electromagnetics and Nanoelectronics* division at Lund University and investigates the possibility of integrating RRAMs on a III-V vertical nanowire technology platform. The work was supervised by Professor *Lars-Erik Wernersson* and co-supervised by Dr. *Karl-Magnus Persson* and Dr. *Johannes Svensson*.

STRUCTURE OF THE THESIS

This thesis is not a monograph but a collection of research papers with an introductory section providing a summary of the research field comprehensible for aspiring researchers with a master's degree in science or engineering degree interested in pursuing similar research.

- **INTRODUCTION**
  The main body of the thesis consists of the publications appended in the back. The Introduction provides a broader view than the very focused publications and ties their work together.

- **APPENDICES**

  A Fabrication flow

  B Virtual source model

- **PAPERS**
  The appended publications form the main body of the thesis and are reproduced in the back and listed in the following.

INCLUDED PAPERS

The following papers form the main body of this thesis and the respective published or draft versions are appended in the back.

Paper I: M. S. Ram, K.-M. Persson, A. Irish, A. Jönsson, R. Timm, and L.-E. Wernersson, "High-density logic-in-memory devices using vertical indium arsenide nanowires on silicon", *Nature Electronics*, vol. 4, pp. 914–920, Dec 2021, doi: 10.1038/s41928-021-00688-5.

► *I carried out the processing of devices, performed electrical measurements and analysis, and wrote the paper.*

Paper II: M. S. Ram, K.-M. Persson, M. Borg, and L.-E. Wernersson, "Low-power resistive memory integrated on III-V vertical nanowire MOSFETs on Silicon", *IEEE Electron Device Letters*, vol. 41, no. 9, pp. 1432–1435, Sept. 2020, doi: 10.1109/LED.2020.3013674.

► *I carried out the processing of devices, performed electrical measurements and analysis, and wrote the paper.*

Paper III: M. S. Ram, J. Svensson, S. Skog, S. Johannesson, and L.-E. Wernersson, "Low-Frequency Noise in Vertical InAs/InGaAs Gate-All-Around MOSFETs at 15 K for Cryogenic Applications", *IEEE Electron Device Letters*, vol. 43, no. 12 pp. 2033–2036, Dec 2022, doi: 10.1109/LED.2022.3216022.

► *I carried out the processing of devices, performed electrical measurements and analysis, and wrote the paper.*

Paper IV: M. S. Ram, J. Svensson, and L.-E. Wernersson, "Effects of Interface Oxidation on Noise Properties and Performance in III-V Vertical Nanowire Memristors", *ACS Applied Materials and Interfaces*, vol. 15, no. 15, pp. 19085–19091, Apr 2023, doi: 10.1038/10.1021/acsami.2c21669.

► *I carried out the processing of devices, performed electrical measurements and analysis, and wrote the paper.*

Paper V: M. S. Ram, K.-M. Persson, and L.-E. Wernersson, "A $4F^2$ Vertical Gate-all-around Nanowire Compute-in-memory Device Integrated in (1T1R) Cross-Point Arrays on Silicon", *IEEE Silicon Nanoelectronics Workshop (SNW)*, pp. 1–2, Sept 2022, doi: 10.1109/SNW56633.2022.9889066.

► *I carried out the processing of devices, performed electrical measurements and analysis, and wrote the paper.*

Paper VI: K.-M. Persson, M. S. Ram, M. Borg, O.-P. Kilpi, and L.-E. Wernersson, "Cross-point arrays with low-power ITO-HfO_2 resistive memory cells integrated on vertical III-V nanowires", *Advanced Electronic Materials*, vol. 6, no. 6 ,pp. 200154, May 2020, doi: 10.1002/aelm.202000154.

► *I assisted with device fabrication, electrical measurements, and the writing of the paper.*

Paper VII: K.-M. Persson, M. S. Ram, and L.-E. Wernersson, "Ultra-scaled AlO_x diffusion barriers for multibit HfO_x RRAM operation", *IEEE Journal of Electron Devices Society*, vol. 9,pp. 564–569, May 2021, doi: 10.1109/JEDS.2021.3079398.

► *I assisted with device fabrication, electrical measurements, and the writing of the paper.*

Paper VIII: M. S. Ram, K.-M. Persson, and L.-E. Wernersson, "Controlling Filament Stability in Scaled Oxides (3 nm) for High Endurance (>10^6) Low Voltage ITO/HfO_2 RRAMs for Future 3D Integration", *IEEE Device Research Conference (DRC), Santa Barbara, CA, USA*, pp. 1–2, Jun 2021, doi: 10.1109/DRC52342.2021.9467131.

► *I performed electrical measurements and analysis, and wrote the paper.*

Paper IX: K.-M. Persson, M. S. Ram, and L.-E. Wernersson, "Investigation of Reverse Filament Formation in ITO/HfO_2-based RRAM", *IEEE Device Research Conference (DRC), Ann Arbor, MI, USA*, pp. 1–2, Mar 2020, doi: 10.1109/DRC46940.2019.9046443.

► *I assisted with device fabrication, electrical measurements, and the writing of the paper.*

Paper X: Z. Yong, M. S. Ram, K.-M. Persson, G.S. Subramanian, L.-E. Wernersson and J. Pan , "The Effect of Deposition Conditions on Heterointerface-Driven Band Alignment and Resistive Switching Properties", *Advanced Electronic Materials*, vol. 8, no. 11 ,pp. 2200220, May 2020, doi.org/10.1002/aelm.202200220.

► *I assisted with device fabrication, electrical measurements, and the writing of the paper.*

Paper XI: Z. Yong, K.-M. Persson, M. S. Ram, G. D'Acunto, Y. Liu, S. Benter, J. Pan, Z. Li, M. Borg, A. Mikkelsen, L.-E. Wernersson and R. Timm , "Tuning oxygen vacancies and resistive switching properties in ultra-thin HfO_2 RRAM via TiN bottom electrode and interface engineering", *Applied Surface Science*, vol. 551, no. 5 ,pp. 149386, June 2021, doi: 10.1016/j.apsusc.2021.149386.

► *I assisted with device fabrication, electrical measurements, and the writing of the paper.*

RELATED WORK

The following publications are not included in the thesis, but summarise related work that I was involved in.

Paper XII: S. Andric, O.-P. Kilpi, M. S. Ram, J. Svensson, E. Lind, and L.-E. Wernersson, "Performance, Analysis, and Modeling of III-V Vertical Nanowire MOSFETs on Si at Higher Voltages", *IEEE Transactions on Electron Devices*, vol. 69, no. 6, pp. 3055–3060, June. 2022, doi: 10.1109/TED.2022.3168241.

Paper XIII: O.-P. Kilpi, S. Andric, J. Svensson, M. S. Ram, E. Lind, and L.-E. Wernersson, "Increased Breakdown Voltage in Vertical Heterostructure III-V Nanowire MOSFETs With a Field Plate", *IEEE Electron Device Letters*, vol. 42, no. 11, pp. 1596–1598, June. 2021, doi: 10.1109/LED.2021.3115022.

Paper XIV: G. Rangasamy, M. S. Ram, L. O. Fhager, and L.-E. Wernersson, "Self-Heating in Gate-All-Around Vertical III-V InAs/InGaAs MOSFETs", *accepted in IEEE Electron Device Letters*

Acronyms and Symbols

Here, important acronyms, abbreviations, and symbols are listed, which are recurring throughout the thesis. Some parameters, which only occur in a narrow context, are intentionally omitted; some parameters are used in more than one way, but the context is always explicitly clarified in the corresponding text. Some (compound) units are provided with prefixes to reflect the most commonly encountered notations in the literature.

ACRONYMS AND ABBREVIATIONS

1T1R	One-transistor-One-resistor
AC	Alternating Current
ALD	Atomic layer deposition
B.E.	Bottom electrode
BOE	Buffered oxide etch
CBRAM	Conductive bridge random access memory
CC	Current compliance
CIM	Compute-in-memory
CMOS	complementary metal-oxide semiconductor
DC	Direct current
DNN	Deep neural network

eNVM	Emerging non-volatile memory
FeRAM	Ferroelectric random access memory
FTJ	Ferroelectric tunnel junction
GAA	Gate-all-around
HRS	High resistive state
LFN	Low frequency noise
LRS	Low resistive state
MAC	Multiply-and-accumulate
MIM	Metal-insulator-metal
MIS	Metal-insulator-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
MOVPE	Metalorganic vapor phase epitaxy
MRAM	Magnetic random access memory
OxRRAM	Oxide resistive random access memory
PEALD	Plasma Enhanced Atomic Layer Deposition
PVD	Physical vapor deposition
RFF	Reverse filament formation
RIE	Reactive-ion etching
RRAM	Resistive random access memory
TALD	Thermal atomic layer deposition
T.E.	Top electrode
UV	Ultraviolet
VLS	Vapor-liquid-solid
XPS	X-ray photoelectron spectroscopy
ZB	Zettabytes

LATIN SYMBOLS

$\mathbf{Al_2O_3}$		Aluminium Oxide
E_F	eV	Fermi Level Energy
E_g	eV	Band Gap
f	Hz	Frequency
I_{SET}	A	Set Current
I_{RESET}	A	Reet Current
I_D	A, mA μm^{-1}	Drain Current, often normalised by the gate width
I_{DS}	A, mA μm^{-1}	Source-to-Drain Current, often normalised by the gate width
I_G	A, mA μm^{-1}	Gate Current, often normalised by the gate width
InAs		Indium Arsenide
I_S	A, mA μm^{-1}	Source Current, often normalised by the gate width
k_B		$\approx 1.381 \times 10^{-23}$ kg m^2 K^{-1} s^{-1}, Boltzmann Constant
L_G	m	Gate Length
m_0		$\approx 9.109 \times 10^{-31}$ kg, Electron Rest Mass
m^*	m_0	Effective Mass
q		$\approx 1.602 \times 10^{-19}$ C, Elemental Charge
V_{FORM}	V	Forming Voltage
V_{SET}	V	Set Voltage
V_{RESET}	V	Reset Voltage
V_{DS}	V	Drain-to-Source Voltage
V_{GD}	V	Gate-to-Drain Voltage

V_{GS}	V	Gate-to-Source Voltage
V_T	V	Threshold Voltage

GREEK SYMBOLS

α	eV^{-1}	Non-Parabolicity Factor
κ		Relative Permittivity
λ		Mean free path

INTRODUCTION

1

Background

"In God we trust. All others must bring data."

W. Edwards Deming

As the field of artificial intelligence continues to evolve rapidly, the volume of data generated and stored is continuously expanding. This expansion has placed considerable strain on the hardware infrastructure built on the traditional von Neumann architecture. As a result, there is a growing need for innovative hardware designs that can efficiently handle the ever-increasing data processing/storage demands. This chapter briefly discusses the current state-of-the-art and introduces the work carried out during this thesis.

1.1 ARTIFICIAL INTELLIGENCE AND THE NEED FOR MEMORY

The advent of metal-oxide-semiconductor-field-effect transistors (MOSFETs) in November 1959 has led to an unimaginable rate of technological advancement in electronic devices. These electronic devices, which house powerful computer chips, can deal with a variety of intelligent tasks. However, the actual data processing instead of taking place inside the electronic device, takes place in large data server farms. These server farms collect and store massive amounts of data which is then used to train machine-learning algorithms for recognizing faces, patterns, voices, etc. Our electronic devices tap into the knowledge stored in the server farms via the cloud [1].

The global datasphere which represents the total data transmission, replication, or reception, is projected to grow to 175 zettabytes, equivalent to 1 trillion gigabytes by 2025. To put this into perspective, downloading this amount of data at a typical speed of 25 Mbps would take 1.8 billion years to complete. Therefore, significant technological advancements in memory solutions must be made to meet the ever-increasing demands for fast data access, throughput, and storage size [2].

1.2 THE VON NEUMANN BOTTLENECK

Today's computer hardware design is based on the von Neumann architecture where the processor and memory are physically separated as illustrated in Figure 1.1. The separation led back-and-forth data movement between the processor and memory leads to unavoidable latency. Despite the significant evolution in computing performance, the unchanged von Neumann architecture forces the high-speed processor to remain idle while it waits to receive data. This fundamental problem is termed as the von Neumann bottleneck [3].

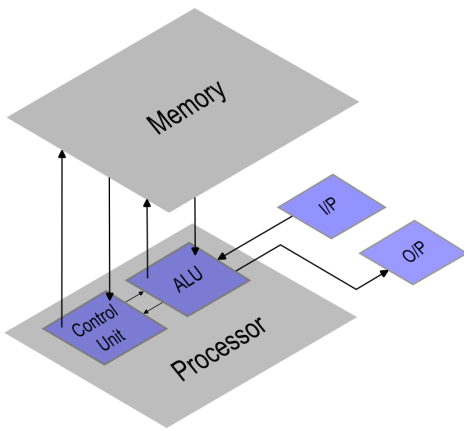

Figure 1.1: Block diagram of the traditional von Neumann architecture.

1.3 IN-MEMORY AND NEUROMORPHIC COMPUTING

A promising solution to overcome the von Neumann bottleneck is In-memory computing. In-memory computing also commonly referred to as compute-in-memory (CIM), logic-in-memory or process-in-memory is an energy-efficient

way where the memory and processing units are combined thereby eliminating the need for data exchange between the two units. This leads to latency reduction combined with increased energy efficiency [4]. Large-scale data processing applications such as deep neural networks (DNNs) are used in machine learning applications such as autonomous driving or image and face detection [5]. The matrix-matrix multiplication is the fundamental operation in DNNs performed using multiply-and-accumulate (MAC).

For MAC operations, a two vector-matrix multiplication ($V_{X\times Y}.G_{X\times Y}$) can be performed using a crossbar array consisting of a memory element and a series transistor at every crosspoint. Figure 1.2 illustrates a crossbar array consisting of 1-transistor-1-resistive memory (1T1R) cells. The vector $G_{X\times Y}$ can locally store the weights used for instance, in DNNs and stream only the vector $V_{X\times Y}$.

$$I = V.G = \sum_{i=1}^{n} (V_i.g_{in})^T \tag{1.1}$$

Emerging memory devices or memristive devices can not only store the weights but also offer information processing capability. The memristors can be made from CMOS-friendly metal oxides, phase-change materials as well as magnetic materials [7].

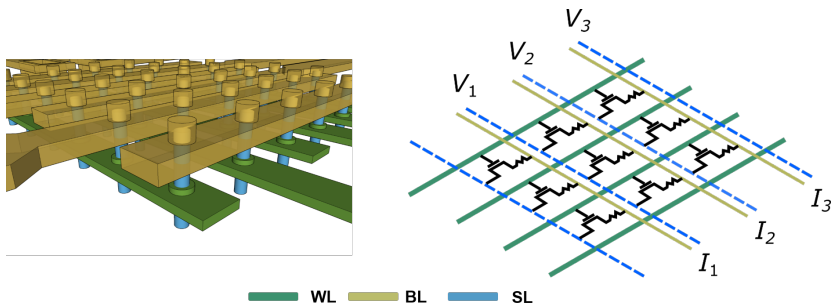

Figure 1.2: Cross-sectional illustration and a circuit representation of a crossbar array consisting of a 1T1R cell at every crosspoint.

1.4 EMERGING NON-VOLATILE MEMORY TECHNOLOGIES

Traditional flash memories are charge based consisting of one transistor (1T) cells. The transistor is used both as an access and storage device. At present, flash memories are used in more than 99 percent of applications. Although, flash memory currently dominates the memory market, the scalability of charge-based devices is challenging. The physical scaling of flash cell dimen-

sions is possible, however, the threshold voltage distribution in the memory array becomes large due to the number of stored electrons reaching statistical limits. The large distributions in scaled charge-based devices can then lead to significant output errors.

The limit to continued scaling of 2D NAND flash devices led to the development of another class of non-volatile memories that are not charge based. This new class of emerging non-volatile memories (eNVMs) includes resistive random access memory (RRAM), ferroelectric random access memory (FeRAM), ferroelectric tunnel junction (FTJ), magnetic memory (MRAM) and more.

To an extent, the problem of having too few charges in 2D NAND flash is to an extent resolved by vertical stacking of memory layers in a 3D NAND implementation. Although 3D NAND has been the current choice to replace 2D NAND, the emerging non-volatile memories as shown in Table 1.1, are continuously being developed as their scalability and low-power consumption are attractive for applications like machine learning. The eNVMs usually have a two-terminal configuration and therefore need an external selector device (eg. Transistor or a diode) when integrated in crossbar arrays.

Table 1.1: State of the art eNVM performance [8]

	FeFET	**FTJ**	**STT-MRAM**	**CBRAM**	**OxRAM**	**Mott**
Feature Size	22 nm	20 nm	22 nm	20 nm	3 nm	110 nm
Cell Area	$4F^2$	-	$9F^2$	$4F^2$	$4F^2$	-
Read current	40 uA/um	0.8 nA	20 uA	100 pA	100 pA	-
W/E time	5 ns	10 ns	3 ns	$<$ 1 ns	85 ps	2 ns
Endurance	10^{12}	10^6	10^{12}	10^{10}	10^{12}	10^2
Retention	10^5s 210°C	3 days 300°C	>10 years	>10 years	>10 years	NA
Write voltage	3.5 V	1.4 V	0.17 V	0.4 V	0.11 V	0.75 V
Read voltage	0.1 V	0.1 V	0.24 V	0.05 V	0.1 V	0.2 V
Write energy	3 fJ	1.2 fJ	30 fJ	0.1 pJ	3.8 fJ	1 fJ

1.5 EMERGING SELECTOR DEVICES AND RE-EXPLORING MOSFET SELECTORS

There has been increasing research interest in pursuing a selector device that does not add memory area overhead and, at the same time, supplies sufficiently high drive current. Primarily due to area constraints, research in developing MOSFET selectors designed to enable RRAM performance has not kept pace and alternate selectors have emerged as listed in Table 1.2 [10]. At the same time 1-transistor-1-resistor(1T1R) based memristor crossbar arrays are being widely used. H. Kim et. al (2021) have used the 1T1R configuration in crossbar arrays for pattern classification [9]. S.-I. Yi et. al (2022) have demonstrated training of deep neural networks to reconstruct braille words using 1T1R crossbar arrays [6]. Y. Zhong et. al (2022) have performed real-time signal processing and demonstrated fully analogue reservoir computing using 1T1R crossbar arrays [3]. The continuous use of 1T1R cells in current key applications serves as an incentive to develop MOSFET selectors favorable for high-density integration.

The gate-all-around (GAA) MOSFETs are promising candidates to extend Moore's law beyond the state-of-the-art finFETs [10]. Moreover, the vertical GAA geometry can accommodate more room for spacer layers and ohmic metal contacts and saves power by 10-15 % in the 7-nm technology node [11]. Figure 1.3 illustrates the MOSFET in a lateral as well as in a vertical GAA configuration. The vertical GAA configuration in a crossbar array would offer power savings and enable integration with eNVMs at a minimal footprint, allowing for increased density. While the vertical geometry offers high-density integration, exploring alternate materials to Silicon can offer the benefits of higher drive currents at lower supply voltages.

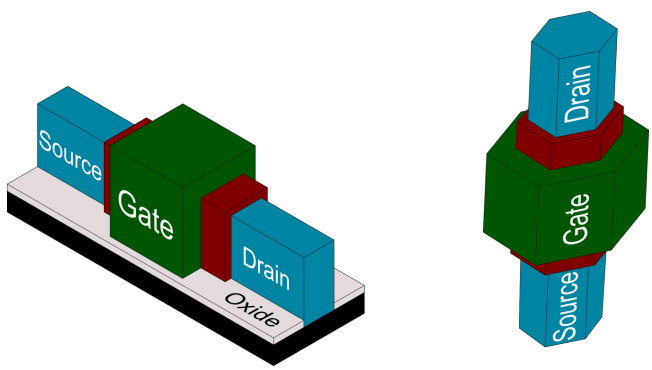

Figure 1.3: Cross-sectional illustration of a lateral and vertical GAA MOSFET architecture.

Table 1.2: Emerging selectors for memory devices [10]

Device Type	Material	Advantage	Challenge
Polysilicon diode	Polysilicon	**High ON/OFF ratio and 3D compatability**	**High thermal budget and increased contact resistance**
Oxide diode	p-NiO_x/n-TiO_x	**Low thermal budget and processing complexity**	**Contact resistance and low ON/OFF ratio**
Mott switch	VO_2, $SmNiO_3$	**Good switching performance**	**Leakage currents, endurance needs improvement and complex material system**
Threshold switch	NbO_x/Pt	**Good switching performance**	**Leakage currents, endurance needs improvement and complex material system**
Tunneling devices	Ni/TiO_2/Ni	**Low thermal budget and processing complexity**	**Needs improved reliability and endurance**
Ionic/Electronic conduction materials	MIEC materials	**Good switching performance**	**Copper accumulation failure**

1.6 RRAM TECHNOLOGY EVOLUTION DURING THIS WORK

This thesis aims to develop a technology platform to integrate vertical nanowire GAA MOSFETs with RRAMs in a 1T1R configuration suitable for in-memory and neuromorphic computing. This thesis gives an introduction to the work carried out to achieve the vertical GAA 1T1R cell and the technology evolution during this work is illustrated in Figure 1.4 and is divided into chapters as follows:

- **Planar RRAMs**
  This chapter covers basics of RRAMs and motivates the material selection for the planar RRAMs used in this work. The fabrication details and the measurements used to evaluate RRAM performance are also described. This chapter serves as an introduction to papers VII - XI. The planar RRAMs correspond to generation 1 in Figure 1.4.
- **Vertical GAA III-V MOSFETs**
  This section familiarizes the reader of the benefits of III-V materials for high-performance vertical GAA MOSFETs and covers the gate-last fabrication process, electrical characterization, and modelling. This chapter serves as an introduction to paper III.
- **Vertical 1T1R**
  This part of the thesis finally covers the transfer of RRAMs onto vertical nanowires. The fabrication flows developed during this work are explained in this chapter. The performance of the resistive memory cell is evaluated post vertical integration. This chapter also serves as an introduction to papers I, II, IV, V, VI. The vertical nanowire RRAMs correspond to generation 2-4 in Figure 1.4.
- **Conclusion and Outlook**
  The results obtained during this work are put into perspective and potential applications are briefly discussed.

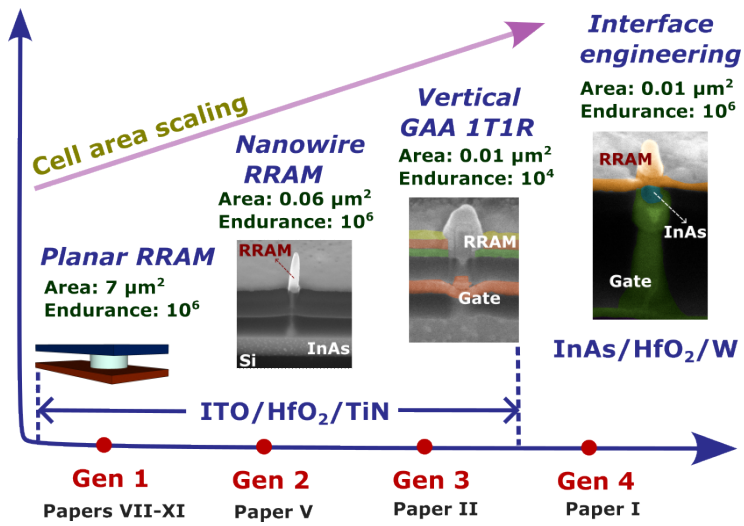

Figure 1.4: Evolution of the vertical GAA 1T1R technology platform.

2

Resistive Random Access Memories (RRAMs)

For implementing RRAMs in a vertical configuration, it is important to evaluate the material stack first in a planar configuration. This chapter lays out RRAM basics and motivates the material selection as it directly influences voltage biasing ranges and electrical performance.

2.1 RRAM FUNDAMENTALS

It was in the 1960s when the resistive switching phenomenon in insulators was observed and reported for the first time when a large bias was applied across the oxide [12]. Interest in resistive switching was revived in the 1990s and 2000s when current hysteresis was observed during bi-directional current-voltage ($I-V$) measurements in perovskite oxides such as $SrTiO_3$ and $SrZrO_3$ [13] [14]. Soon after, industry too got involved in resistive random access memory technology development with Samsung demonstrating a NiO RRAM array completely compatible with CMOS technology in 2004 [15]. Finally in 2008, the concept of the memristor was tied to RRAMs by HP labs in a paper titled 'The missing memristor found' [16]. Since then there have been multiple reports of RRAMs using CMOS-compatible binary oxides such as CuO_x, ZrO_x, AlO_x, HfO_x, etc [17] [18] [19] [20].

In general, RRAMs can be classified into two types. The two types of RRAM are differentiated by their conductive filaments, with one type using oxygen vacancies and is known as oxide-based RRAM (OxRRAM), and the other type using metal atoms and is referred to as conductive-bridge RAM (CBRAM). Although the underlying physics of switching in CBRAM is different due to metal ion migration, the CBRAM shares common device characteristics and array design considerations as the OxRRAM.

In this thesis, OxRRAM is referred to as RRAM as the focus is on oxygen vacancy-based resistive switching. The typical cross-sectional illustration of a metal-insulator-metal (MIM) RRAM stack is shown in Figure 2.1 (a) where a thin oxide layer is sandwiched between two metal electrodes. In RRAMs, the ”SET” process indicates the switching event from the high-resistive state (HRS) to the low-resistive state (LRS). On the other hand, the switching event from the LRS to the HRS is called the ”RESET” process. For pristine RRAM samples, in order to make them switchable an initial ”FORMING” step is carried out. During the FORMING step, a relatively large bias is applied due to the initial resistance of the stack being very high.

RRAMs can further be classified into two different categories based on their modes of operation: unipolar and bipolar. The switching characteristics of a

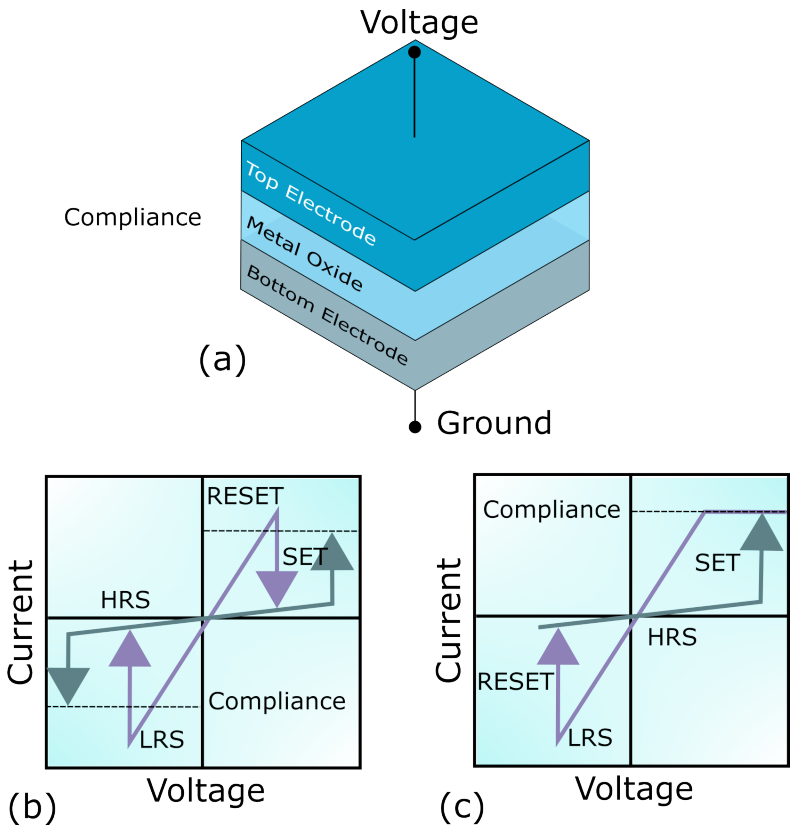

Figure 2.1: (a) Cross-sectional illustration of a MIM-RRAM stack, I-V characteristics showing (b) Unipolar mode switching and (c) Bipolar mode switching.

unipolar RRAM are illustrated in Figure 2.1 (b) where the switching depends on the applied voltage amplitude and not the polarity. On the other hand, in bipolar switching, as illustrated in Figure 2.1 (c), the switching depends on the applied voltage polarity. This means that the SET/RESET processes occur at reversed polarity.

As the FORMING/SET processes involve a soft breakdown of the dielectric, it is crucial to enforce current compliance (CC) to prevent permanent dielectric breakdown. A CC can be applied by the semiconductor parameter analyzer during chip testing but for practical applications, it is recommended to have a current limiting device (MOSFET, diode, or a resistor) in series with the RRAM. After the RRAM write operation, the data from the RRAM can be read by applying a small READ voltage to identify whether the RRAM is in the LRS or HRS. It is important for the READ voltage to be significantly smaller than the SET/RESET voltage to not disturb the current RRAM state.

The SET and RESET operations induce the migration of oxygen vacancies which results in modifying the shape and size of the conductive filament. The oxygen vacancy-based conductive filament is formed during the FORMING operation. During the RESET operation when a negative bias is applied on the RRAM top electrode, the oxygen vacancies migrate towards the T.E resulting in a partial rupture of the conductive filament as illustrated in Figure 2.2. The ruptured gap in the conductive filament has a high resistance and switches the RRAM into the high-resistive state. The RESET transition has

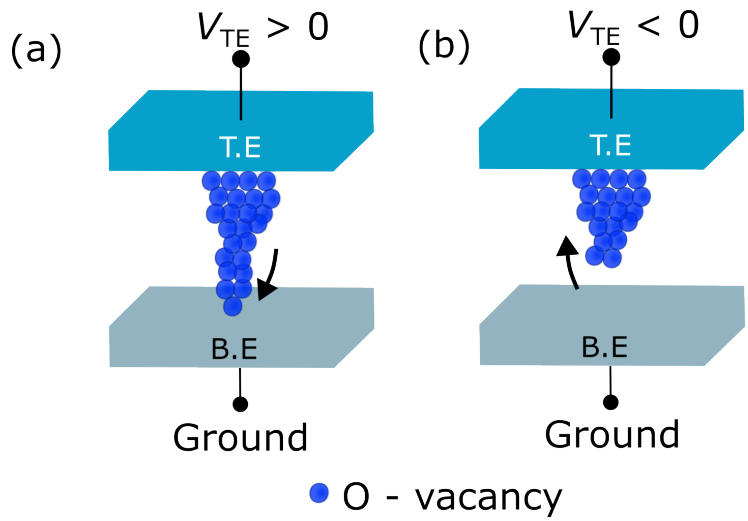

Figure 2.2: Cross-sectional illustration of a MIM-RRAM showing the movement of oxygen vacancies during (a) SET and (b) RESET.

been analytically modeled by Ambrogio et. al [21] and can be written as

$$\frac{d\Delta}{dt} = Ae^{-\frac{E_A - \alpha qV}{KT}} \tag{2.1}$$

where E_A is the activation energy for vacancy migration, α is a coefficient for barrier lowering, V is the voltage drop across the ruptured gap, k is the Boltzmann constant, T is the local temperature and A is a preexponential coefficient.

Similarly, when a positive bias is applied on the RRAM top electrode, the oxygen vacancies migrate towards the RRAM bottom electrode filling the ruptured gap with oxygen vacancies as illustrated in Figure 2.2 (a). This results in a continuous conductive filament and switches the RRAM into the low-resistive state. Similar to the RESET operation, the SET operation can also be described using an analytical model and can be written as

$$\frac{d\phi}{dt} = Ae^{-\frac{E_A - \alpha qV}{KT}} \tag{2.2}$$

where ϕ is the diameter of the conductive filament. The switching modes of the RRAM are significantly influenced by the choice of electrode materials. This means that even when the switching oxide is the same, using different metal electrodes can result in different switching modes. From this, it can be noted that the switching mode is not an inherent property of the oxide material, but is rather determined by both the oxide material and the electrode/oxide interfaces. Typically, using an inert or less reactive metal like Pt for both the top and bottom electrodes results in the unipolar switching mode. However, by substituting one of the electrodes with oxidizable materials which can scavenge oxygen like Ti, the bipolar switching mode can be achieved. A commonly used stack in TiN/metal/oxide/TiN and oxygen-scavenging metals like Ti, Hf, Al, etc. can be used to scavenge oxygen. Due to the relatively higher energy consumption in unipolar RRAMs due to higher RESET currents and variability, we focus on bipolar RRAMs in this thesis.

2.2 BOTTOM ELECTRODE CONSIDERATION

Noble metals such as Au and Pt are more commonly used as the B.E. than easily oxidizable metals such as Ti and Cu. This is because noble metals tend to gather less oxygen from the atmosphere if the sample is not in vacuum between B.E. and switching oxide deposition. However, in the industry, the use of noble metals may not be feasible due to their high cost and etching issues [22].

For eventual compatibility with industry pilot lines, metals such as TiN or TaN are desired instead of noble metals. TiN is popularly used as a B.E.

for RRAMs because of its compatibility with Si-CMOS, inertness, relatively large work function, and can be selectively etched. However, it is known that TiN can gather oxygen and act as an oxygen reservoir leading to oxidation of the TiN B.E. The formation of TiO_x and TiO_yN_z can strongly affect resistive switching characteristics of the RRAM and therefore is important to study the B.E./dielectric interface.

In the next section, the effect of different deposition techniques like ALD and sputtering on the surface of TiN B.E. will be discussed as they can impact resistive switching properties.

2.2.1 SPUTTERED TIN VS. ALD TIN

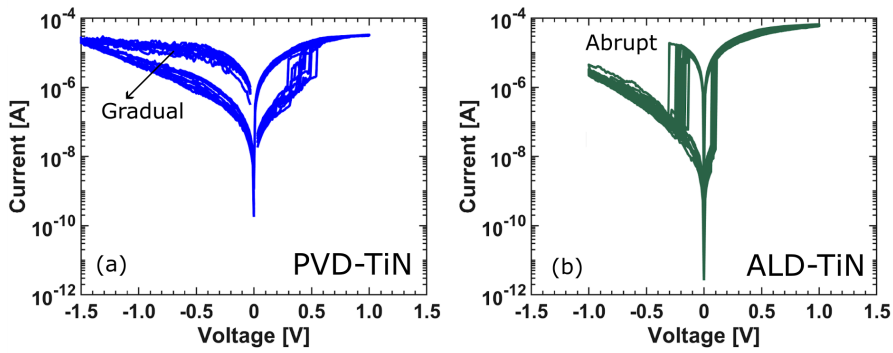

Figure 2.3: IV characteristics of the ITO/HfO_2/TiN RRAM for (a) PVD-TiN and (b) ALD-TiN

To study the effect of the deposition technique of TiN on the RRAM switching properties, two RRAM stacks labelled as Sample A and Sample B with different B.E. were fabricated where the B.E. was deposited using PVD/sputtering and ALD as shown in Table 2.1. The choice of indium tin

Table 2.1: Fabricated RRAM stacks

	T.E.	**Oxide**	**B.E.**
Sample A	ITO	HfO_2	TiN (PVD)
Sample B	ITO	HfO_2	TiN (ALD)

oxide (ITO) as the RRAM T.E. will be discussed in the next section. Electrical DC $I-V$ characteristics of sample A and sample B shown in Figure 2.3 clearly show a difference in switching properties depending on the deposition technique used for the B.E.

The gradual switching behavior combined with the reduced memory window for Sample A indicates that there is a larger conductive base at the B.E. interface as shown in Figure 2.4 (a). This is due to a larger concentration of oxygen vacancies present at the TiN interface when deposited using sputtering. The XPS measurements carried out at Max IV, Lund presented in Paper XI also suggest that HfO_x layer in the HfO_x/PVD-TiN (Sample A) is oxygen deficient when compared to HfO_x/ALD-TiN (Sample B). This may be due to the PVD-TiN being more defective with many grain boundaries causing oxygen scavenging from the HfO_x layer. The increase in surface roughness for the PVD-TiN was confirmed with AFM where the root mean square surface roughness was measured to be 10.0 $\AA$ and for ALD-TiN to be 3.0 $\AA$. The XPS findings also revealed the presence of a thicker TiO_2 overlayer in Sample B which may slow down oxygen scavenging from the HfO_x layer.

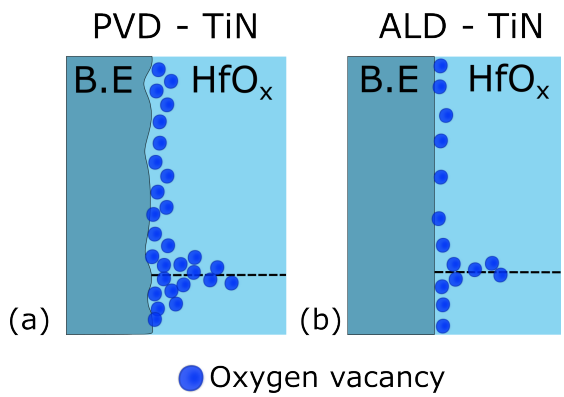

Figure 2.4: (a) Cross-sectional illustration of the B.E./HfO_x interface for (a) PVD-TiN and (b) ALD-TiN.

2.3 SWITCHING OXIDE AND TOP ELECTRODE CONSIDERATION

HfO_2, despite being widely used in industry in transistor gate stacks, is also very attractive for use in RRAMs as the resistive switching (RS) oxide. HfO_2 does not have any stable substoichiometric oxides which helps conserve the number of oxygen vacancies during resistive switching [23]. RRAM endurance values as high as 10^{10} have been demonstrated in RRAM stacks with HfO_2 as the RS oxide [24].

Titanium (Ti) is a commoly used T.E. as mentioned earlier in this chapter, but in this work Indium-Tin-Oxide (ITO) is used as the RRAM T.E. Using ITO as the T.E. for RRAMs has two benefits:

1. Lower switching voltages: In literature, ITO/HfO_2-based RRAMs have demonstrated switching voltages of sub-0.6 V which are lower compared to standard RRAM stacks such as TiN/HfO_2/Ti/TiN [25] [26]. The lower switching voltages are due to the oxidation/reduction reactions taking place near the ITO electrode as shown in Equations 2.3 and 2.4 [28].

$$O^{2-} + Sn^{4+} \rightarrow Sn^{2+} + O_2 \tag{2.3}$$

$$O^{2-} \rightarrow V_O^{2+} + \frac{1}{2}O_2 + 2e^- \tag{2.4}$$

2. Self-compliance ability: Self-compliance in ITO is induced because of the formation of a Schottky barrier at the ITO/HfO_2 interface [29]. The barrier is formed during the filament formation or the SET process where oxygen is driven towards the ITO T.E. where the oxygen reacts with tin and forms tin-oxide. The presence of the local Schottky barrier helps to stabilize the LRS by protecting the RRAM from current overshooting. The difference between self-compliance and parameter analyzer (B1500A) imposed current compliance can be seen in a standard SET operation as shown in Figure 2.5.

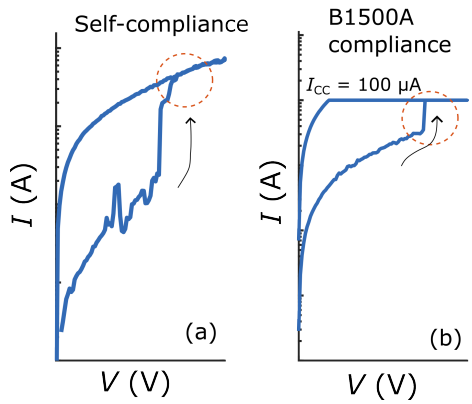

Figure 2.5: (a) SET operation illustrating self-compliance (b) SET operation illustrating a current compliance, I_{CC} of 100μA forced by the parameter analyzer.

2.4 RRAM FABRICATION

The planar RRAM is fabricated on a silicon substrate with a 200 nm-thick thermally grown SiO_2. The RRAM is not fabricated directly on the silicon substrate because the presence of the 200 nm-thick SiO_2 lowers the surface roughness which helps reduce the cell-to-cell variability. Figure 2.6 illustrates the process flow with the help of cross-sectional schematics of the RRAM at different process stages.

First, the 30 nm-thick TiN for the RRAM B.E. is deposited using PEALD at 250°C with a tetrakis dimethylamino-titanium (TDMA-Ti) precursor. An N_2 remote plasma with a power of 300 W is used for 5 minutes per cycle. The B.E. is patterned using UV-lithography and then etched by RIE using an SF_6/N_2 plasma. For the RRAM switching oxide, a 3.3 nm-thick HfO_2 layer is deposited using PEALD. The HfO_2 layer is deposited using a tetrakisethylmethylamido-hafnium (TEMA-Hf) precursor at 200°C with an O_2-plasma of power 300 W and flow of 40 sccm. To isolate the contact pads from the substrate, an organic spacer (S18-resist) is spin-coated and then hard-baked at 200°C. For the RRAM area definition, 3 μm wide openings are patterned in the spacer layer using UV-lithography. For the RRAM T.E., 20 nm-thick ITO is deposited using sputtering with an Ar flow rate of 9 sccm

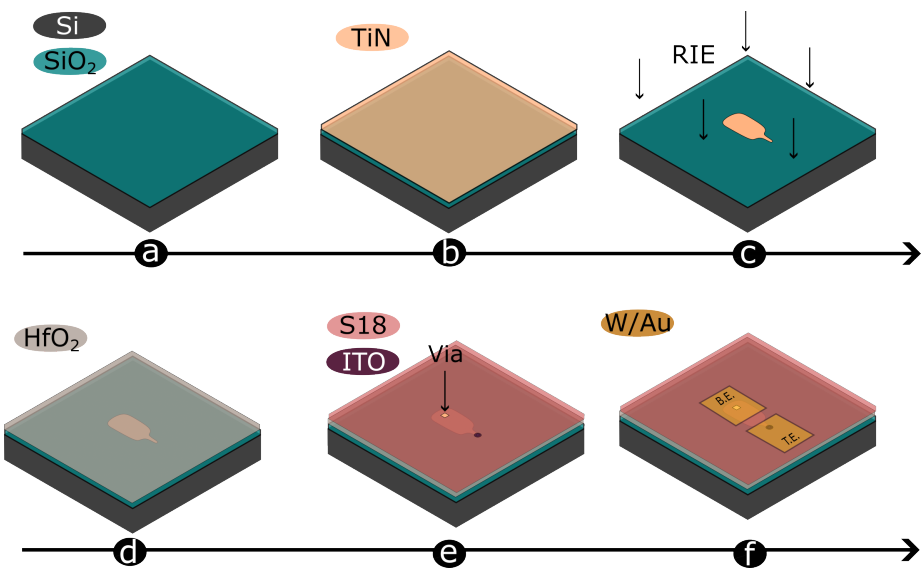

Figure 2.6: Cross-sectional illustration of the process flow for fabricating a planar ITO/HfO_2/TiN RRAM.

and an RF power of 50 W. The ITO RRAM T.E. is then patterned using UV-lithohraphy and is etched using RIE in Cl/Ar plasma.

Before depositing the contact pads for probing, vias are patterned and opened down to the TiN layer by first etching the resist spacer and then HfO_2 using a BOE wet etch. Finally for the contact pads, W/Au are deposited with thicknesses 40/60 nm and then defined using UV-lithography and etching.

2.5 ELECTRICAL CHARACTERIZATION

2.5.1 PULSED CHARACTERIZATION FOR ENDURANCE

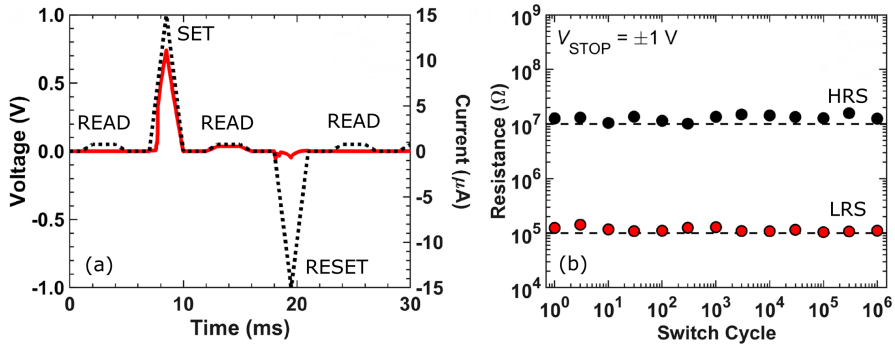

Figure 2.7: (a) Applied voltage pulse train and measured current (b) Endurance measurement showing upto 10^6 write cycles for the ITO/HfO_2/TiN RRAM with ALD-TiN.

For practical applications it is important to evaluate the endurance of the RRAM using pulsed characterization. DC characterization is often performed for initial performance validation to get an idea of the switching mechanism, switching voltages and the memory window. As we learnt that the ALD- TiN RRAM which consisted of the stack TiN/HfO_2/ITO had a tight switching distribution and a large memory window, pulsed endurance measurements were performed on the same.

The applied voltage pulse train and the corresponding measured current are shown in Figure 2.7 (a). The applied voltage pulse train consists of a READ, SET, READ, RESET and READ. A programming pulse of 3 ms was used as the measurement was limited by the parasitic load stemming from the external transistor used to obtain a 1T1R configuration. Therefore, an integrated transistor instead of an external transistor would be enable faster pulsing due to reduced parasitics.

The above-described pulse train was applied to the $TiN/HfO_2/ITO$ RRAM stack where an endurance of 10^6 switching cycles was measured as shown in Figure 2.7 (b). During the 10^6 switching cycles, no degradation of resistance states was observed and a memory window of 100x was consistently maintained. Triangular programming voltage pulses of $\pm$ 1.0 V were applied. Although depending on the application a higher endurance may be desired, an endurance of at least 10^5 cycles has been shown to be sufficient to run deep learning applications [30].

2.5.2 MULTI-BIT OPERATION AND RETENTION

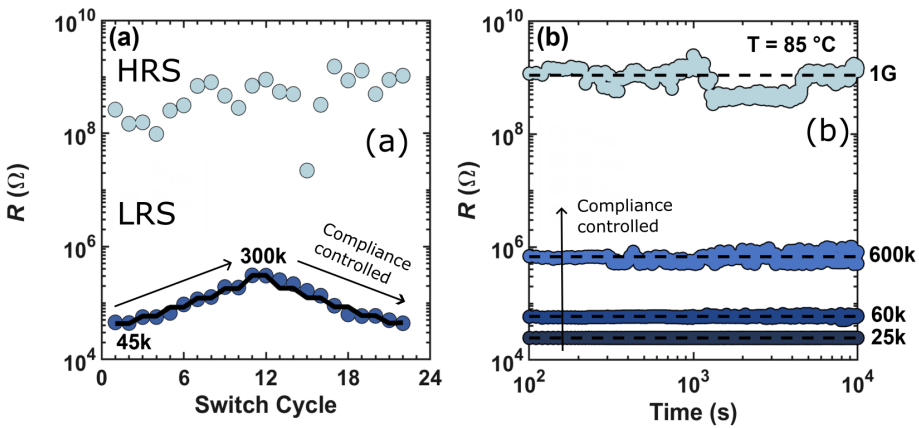

Figure 2.8: (a) Compliance current controlled resistance modulation (b) Retention measurement for 4 resistance states.

Although. RRAMs are extremely scalable and can be integrated densely in crossbar arrays, the density can further be increased by enabling the multi-bit operation of individual RRAM cells. Several studies have reported that introducing an AlO_x layer as a diffusion barrier can enhance switching performance and enable multi-bit or more than the traditional 2-bit operation. In some studies, the introduction of the AlO_x layer resulted in multi-bit operation by having an analog dependence on the RESET voltage magnitude or the number of RESET pulses applied [31] [32] [33] [34] [35].

In paper VII, we have studied the effect of introducing ultra-thin (0.5 nm-thick) AlO_x diffusion barriers at different interfaces of HfO_x. The introduction of AlO_x layers on B.E and T.E. interface allows for better control of the oxygen vacancy filament. In Paper VII, with the help of energy band diagrams

it is explained that, having the barrier at the B.E. interface is beneficial for suppressing RFF. Whereas, the barrier at the T.E. interface reduces the vacancy concentration at that interface changes the filament shape to be more cylindrical than conical. Therefore, the AlO_x barrier layers prevent in parasitic filament overgrowth which is not desirable for high endurance. Contrary to some studies where multi-bit operation was performed by controlling the programming voltage, Figure 2.8 demonstrates the possibility of modulating the low resistive state by changing the transistor compliance current. An external transistor was used to obtain the 1T1R configuration and the selector/transistor gate was used to adjust the compliance current. This method of controlling the resistance state is less sensitive to losses in a large memory array as the low resistance state is independent of the magnitude of programming voltage.

2.5.3 REVERSE FILAMENT FORMATION (RFF)

For achieving high endurance it is important to understand the failure mechanisms of the RRAM as well. A significant failure mechanism that limits RRAM endurance is the reformation of the conductive filament during the RESET process [36]. This failure mechanism is referred to as RFF in this thesis. Therefore, it is very important to maintain a safe margin between the RESET voltage and the RFF voltage to prevent switching failure. An example of RFF for the ITO/HfO_x/TiN RRAM after the 1st RESET is shown in Figure 2.9 (a).

The RFF margin can be improved by modifying the electrode and oxide material deposition conditions. The probability of RFF is higher if there is a larger concentration of oxygen vacancies present near the B.E./oxide interface. The RFF margin can be improved by using either an ALD-TiN B.E or by depositing the HfO_x switching oxide using TALD and not PEALD as discussed in paper X and paper XI.

It is also possible to improve the RFF margin by introducing a diffusion barrier layer for example Al_2O_3 at B.E./oxide interface which would suppress any oxygen vacancy supply from the B.E. as discussed in Paper IX.

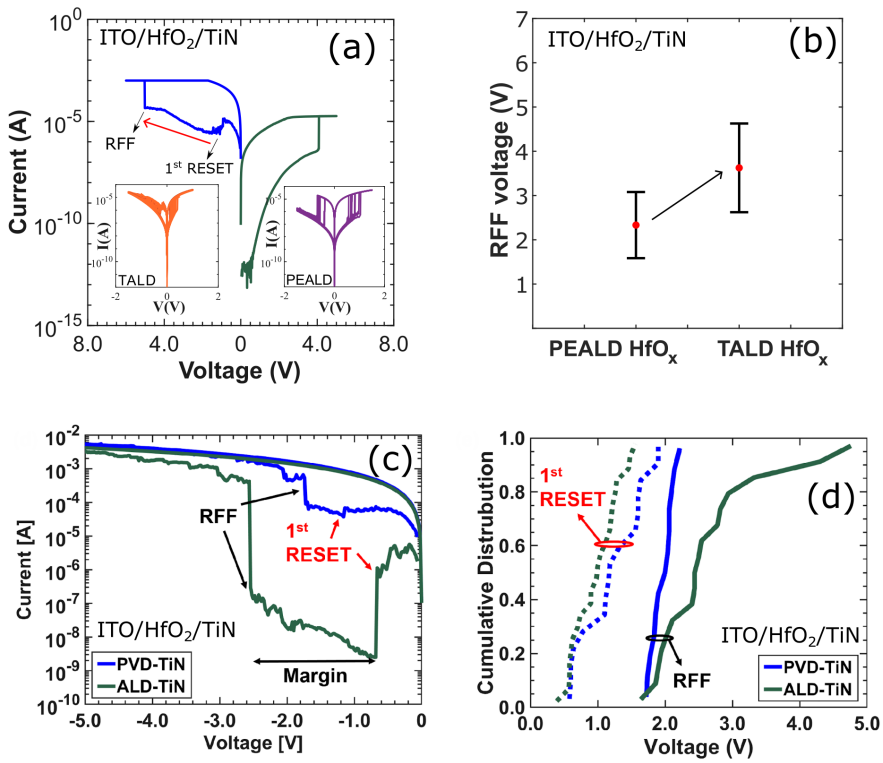

Figure 2.9: (a) $I-V$ characteristics of the ITO/HfO_2/TiN RRAM showing the 1st RESET and the onset of RFF (b) Distribution of the RFF voltages for PEALD and TALD HfO_x (c)IV characteristics of the ITO/HfO_2/TiN RRAM showing the RFF margin for PVD-TiN and ALD-TiN (d) CDF plots for RFF voltages for PVD-TiN and ALD-TiN.

3

Vertical Nanowire III-V GAA-MOSFETs

As this thesis aims to develop a vertical 1T1R cell that implements a high-performance GAA MOSFET selector, this chapter will focus on GAA MOSFETs. Previously, the vertical InAs/InGaAs MOSFET has demonstrated record performance when fabricated using the gate-last process [37]. In this chapter, the gate-last process will be described and the process modules which were optimized will be discussed.

3.1 BASIC MOSFET OPERATION

The fundamental principle of operation for a MOSFET involves controlling the current between its source and drain terminals using a voltage applied to the gate terminal. Ideally, there is no current flowing into or out of the gate. The gate oxide enables the gate terminal to control the channel by isolating the gate metal from the gate oxide. The cross-sectional planar MOSFET structure along with the operating principle illustrated using energy band diagrams are shown in Figure 3.1. In an n-type bulk MOSFET, the source and drain contacts are created by highly n-doped regions implanted into a p-doped substrate. Without an applied voltage (V_{GS}) between the gate and source, the resulting band structure forms an energy barrier in the channel that prevents the majority of electrons from crossing it as illustrated in Figure 3.1 (b). Consequently, no current flows between the source and drain, as the MOSFET is in its OFF-state. When a positive V_{GS} is applied, the energy barrier in the channel is lowered due to the electric field created via the gate oxide. As V_{GS} increases, more electrons can overcome the barrier, when a sufficiently large voltage (V_{DS}) between the source and drain is applied. As the source-to-drain current (I_{DS}) increases, the MOSFET transitions into the ON-state as

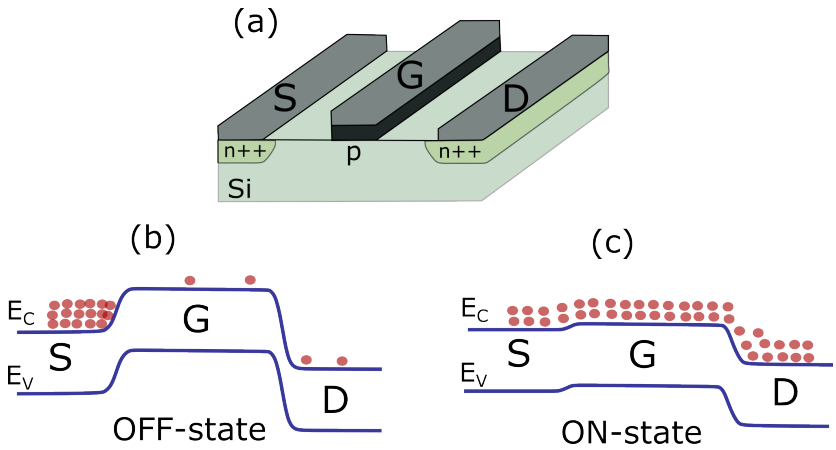

Figure 3.1: (a) Cross-sectional illustration of a planar MOSFET (b) Energy band diagram for the MOSFET in the OFF-state (c) Energy band diagram for the MOSFET in the ON-state.

illustrated in Figure 3.1 (c). The threshold voltage is the voltage above which the MOSFET is in the ON-state and below which is in the OFF-state.

3.2 GATE-LAST PROCESS

The vertical MOSFET process used in this work is based on the gate-last process developed at Lund University which offers reduced access resistance compared to the gate-first process [40]. Gate-first vertical MOSFETs have an ungated area that gives rise to increased access resistance. This section describes the gate-last process and a detailed process flow is given in the appendix.

Figure 3.2 illustrates with the help of cross-sectional schematics the key steps of the gate-last process. First, a 300 nm-thick InAs buffer layer is grown on Si using metal-organic chemical vapor deposition (MOCVD). The vertical nanowires intended to form a core-shell structure are then grown using vapor-liquid-solid (VLS) growth from EBL-patterned gold particles. The nanowire after growth is illustrated in Figure 3.2 (a).

For placement of the MOSFET drain contact, a 400 nm-thick HSQ film is spin-coated and baked. The thickness/height of the HSQ film is then defined using EBL by varying the dose [41]. A dose test is performed before the actual run to extract the dose needed to correctly align the HSQ height to the nanowire segment where the doped region begins. After HSQ definition, a 20 nm-thick Mo followed by 1.5 nm-thick TiN is deposited using sputtering and

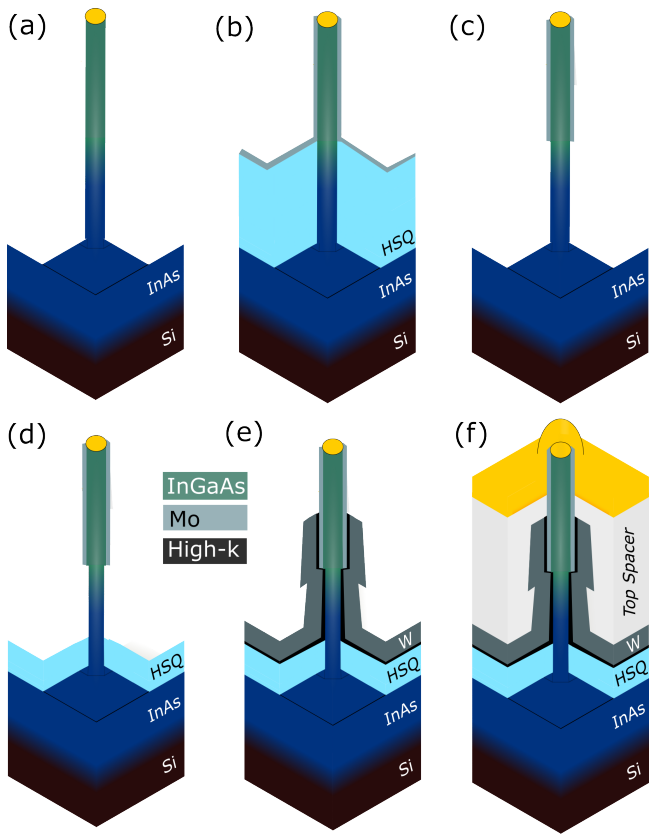

Figure 3.2: Cross-sectional illustration of the key steps in the process flow to fabricate a vertical GAA InAs/InGaAs MOSFET.

ALD respectively as illustrated in Figure 3.2 (b). To etch the metal on lateral surfaces only, anisotropic reactive ion etching is used and then the sacrificial HSQ layer is stripped away. After this step, the metal only remains on the nanowire sidewalls as illustrated in Figure 3.2c. The recipe developed to etch the drain metal is explained in the next section. For the bottom spacer, a 400 nm-thick HSQ is spin-coated and baked as shown in Figure 3.2d. The bottom spacer thickness can be controlled using the EBL dose which in turn defines the MOSFET gate length which will be explained in the subsequent sections. As the bottom spacer and the drain top metal mask the MOSFET contact regions, the doped shell around the channel can be locally etched by using a digital etch process. For the digital etch, the channel surface is first oxidized using ozone, and the oxide is then etched using an HCl:IPA mixture.

For the gate dielectric, an Al_2O_3/HfO_2 bilayer is deposited using ALD. The gate metal comprises of a 1.5 nm-thick TiN layer followed by 60 nm-thick W as shown in Figure 3.2 (e) The device is then completed by depositing the top spacer and metalizing contacts as illustrated in Figure 3.2 (f).

3.2.1 TOP METAL/DRAIN CONTACT OPTIMIZATION

Having an ohmic contact is key when designing MOSFETs aimed towards reducing contact resistance. In previous demonstrations, W/TiN and Mo/TiN have been shown to form good contacts with vertical nanowires [41] [42]. A record low access resistance in vertical MOSFETs was also achieved using the gate-last process [37]. In previous demonstrations, anisotropic etching was achieved using an $SF_6/C_4F_8/Ar$ chemistry. However, due to a change in the RIE tool in the Lund Nanolab, the etch process was redeveloped. Anisotropic etching in this work was achieved using an SF_6/N_2 recipe instead. C_4F_8 was replaced by N_2 as similar etch results could be obtained with minimal etch residues on the sample surface and nanowire sidewalls.

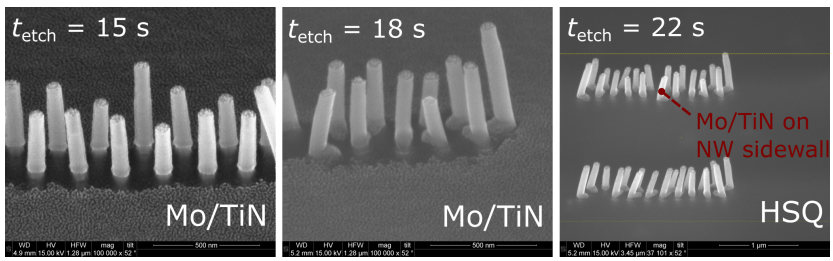

Figure 3.3: SEM images of a vertical InAs/InGaAs nanowire array showing the etch time required to completely remove Mo/TiN from the lateral surfaces so that the HSQ layer is completely exposed.

Figure 3.3 shows that an etch time (t_{etch}) of 22 s is sufficient to remove Mo/TiN (20 nm/1.5 nm) from the lateral surfaces. These results were obtained by varying ICP and RF powers as well as SF_6/N_2 flow rates. The final etch parameters obtained are given in Table 3.1.

Table 3.1: Mo/TiN Etch Parameters

ICP Power	**RF Power**	**SF_6 flow rate**	**N_2 flow rate**	**Pressure**	**Etch time**
700 W	30 W	25 sccm	25 sccm	5 mTorr	22 s

3.2.2 SPACER CONTROL

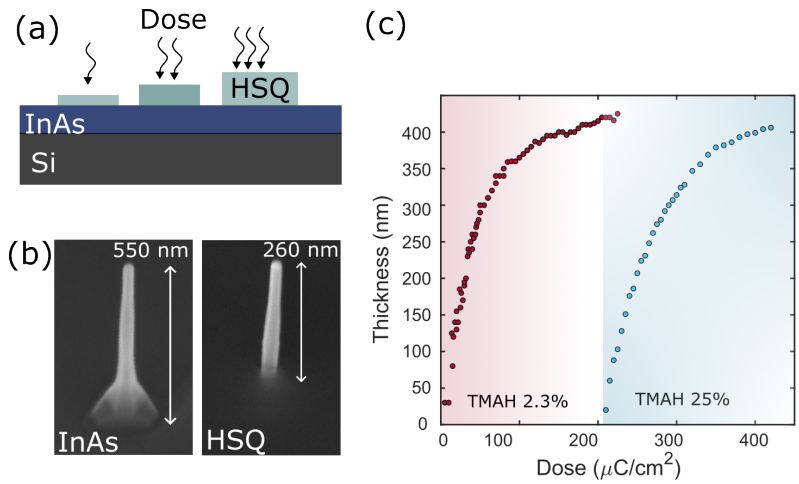

Figure 3.4: (a) Cross-sectional illustration of HSQ pads on InAs defined using EBL (b) SEM images of InAs/InGaAs nanowire before and after HSQ height definition (c) Contrast curves for HSQ development with 2 different TMAH concentrations.

Spacer control is key to achieving precise placement of the gate stack and controlling the gate length. To reduce process complexity, the same high-k that is used for the gate oxide can be used as the bottom spacer [38], [39]. Albeit the ease in processing, using the gate oxide as a spacer will lead to increased gate-to-source capacitance which is not desirable for high-performance RF MOSFETs. Some examples of spacers in more advanced structures include PECVD Si_3N_4, ALD SiO_2, and EBL-defined hydrogen-silsesquioxane (HSQ) [43] [44] [45] [46]. As the ALD and PECVD deposited spacers need to be selectively etched away from the nanowire sidewalls, an EBL-defined HSQ spacer is used in this work. The electron beam-sensitive HSQ resist (Fox-15) turns into SiO_2 after curing which has a good thermal budget and is also mechanically stable. The thickness of the HSQ spacer after spinning is 400 nm-thick and can be precisely controlled by the EBL dose as shown in Figures 3.4. The HSQ spacer also forms an even surface next to the nanowire which is beneficial for the deposition of the subsequent gate stack layers. A TMAH-based developer is commonly used. Typically, 25% TMAH is used which is considered very hazardous and moving to a lower TMAH percentage would help minimize user risk. From experimental tests, we observed that HSQ could also be developed using a commonly used developer, MF319 which only contains 2.3% TMAH. Additionally, it can be

noted that using MF319 also moves the contrast curve towards lower EBL doses as shown in Figure 3.4c which can significantly reduce EBL exposure times.

3.2.3 GATE STACK

Precise HSQ thickness control using EBL for top metal definition and bottom spacer allows obtaining physical gate lengths in the range as small as 15-20 nm. Figure 3.5 shows the SEM images after high-k deposition where different gate lengths on the same sample can be obtained by locally varying the EBL dose.

For III-V MOSFETs such as In(Ga)As, multiple oxides like Al_2O_3, HfO_2 and ZrO_2 have been demonstrated [47] [48] [49] [50]. For our vertical nanowire MOSFETs we use a bilayer consisting of Al_2O_3/HfO_2 as the gate dielectric. The Al_2O_3/HfO_2 gate dielectric is deposited using ALD where 10 cycles at 300°C is used for Al_2O_3 and 40 cycles at 120°C is used for HfO_2. The mentioned ALD deposition of the dielectric results in an equivalent oxide thickness (EOT) of 1.5 nm. As interface oxides of InAs are detrimental for MOSFET performance, Al_2O_3 forms a good interface with InAs. The InAs is also pre-dosed with a TMA precursor for surface passivation [51].

For the gate metal, first a 2 nm-thick TiN is deposited using PEALD for better sidewall surface coverage compared to metal deposition using sputtering. It has also been observed that sputtering causes more damage to the oxide surface due to physical bombardment [52]. The ALD TiN is then followed by a sputter deposition of a 60 nm-thick W layer.

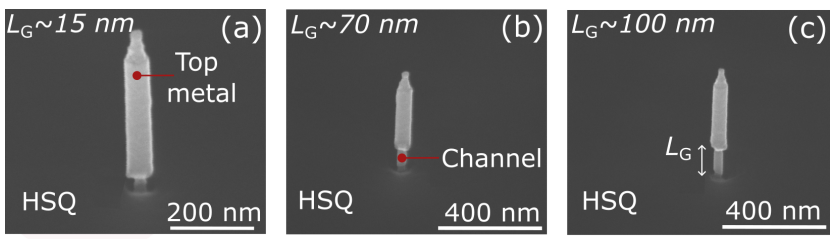

Figure 3.5: SEM images of the InAs/InGaAs MOSFET showing the possibility of obtaining different gate lengths by controlling the bottom spacer (HSQ) thickness where (a) L_G = 15 nm (b) L_G = 70 nm (c) L_G = 100 nm.

3.3 CHARACTERIZATION

3.3.1 ELECTRICAL CHARACTERIZATION AND VIRUAL SOURCE MODELLING

Direct current (DC) measurements are used to evaluate typical performance metrics like transconductance (g_m) and ON-resistance (R_{ON}). Figure 3.6 shows the transfer and output characteristics of the InAs/InGaAs GAA MOSFET fabricated using the gate-last process. With a $g_m \sim 1.4$ mS/μm and $R_{ON} = 550$ $\Omega\mu$m at a gate length of 70 nm, the fabricated InAs/InGaAs GAA MOSFET has a similar performance when compared to reported state-of-the-art III-V vertical MOSFETs [41]. From the perspective of developing a 1T1R cell, the InAs/InGaAs GAA MOSFET can drive the RRAM cell with sufficient current for reliable switching even at a low supply voltage, V_{DS} of 0.5 V.

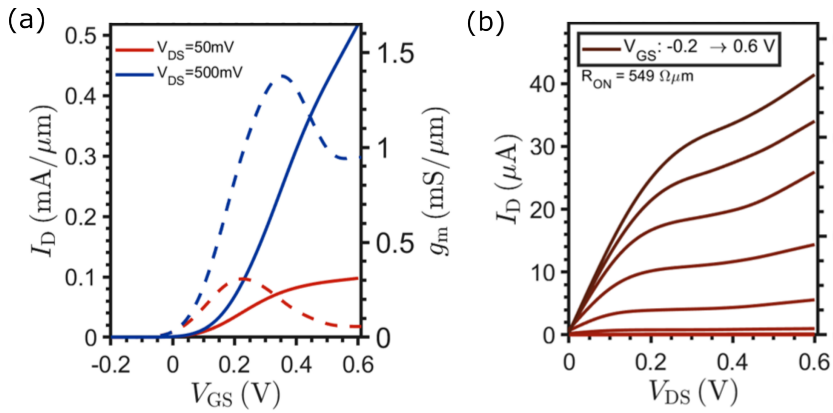

Figure 3.6: (a)Transfer and (b) output characteristics of the vertical InAs/InGaAs GAA MOSFET with a gate length of 70 nm and nanowire diameter of 27 nm.

To extract useful parameters such as access resistance, mobility and injection velocity, the virtual source model (MVS 2.0.0) is used to model and fit to measured data [53] [54]. The physics-based MVS 2.0.0 describes the transport in quasi-ballistic transistors and is based on the Laundauer scattering theory. In the virtual source model, the current, I_D is given by equation 3.1

$$\frac{I_D}{W} = Q_{xo}.v_{xo}.F_{sat} \tag{3.1}$$

Where Q_{x0} is the charge at the barrier top which is considered as the virtual source point, v_{x0} is the injection velocity and F_{sat} is an empirical function used to account for the current transition from saturation to linear with change in V_{DS}.

F_{sat} and V_{dsat} are described using equations 3.2 and 3.3.

$$F_{sat} = \frac{\frac{v_{ds}}{v_{dsat}}}{(1 + (\frac{v_{ds}}{v_{dsat}})^{\beta})^{\frac{1}{\beta}}} \tag{3.2}$$

$$V_{dsat} = \frac{v_T.\lambda}{\mu_{eff}}.(\frac{1}{T_{lin}}).((\frac{T_{sat}}{2 - T_{sat}})f_1) \tag{3.3}$$

where V_{dsat} is the saturation voltage, β is an empirical parameter to control the current transition from linear to saturation region, T_{lin} and T_{sat} are the transmission coefficients and μ_{eff} is the effective mobility. Figure 3.7 shows the modelled characteristics (solid red line) along with the measured data (black circles). The fitting parameters are stated in the appendix.

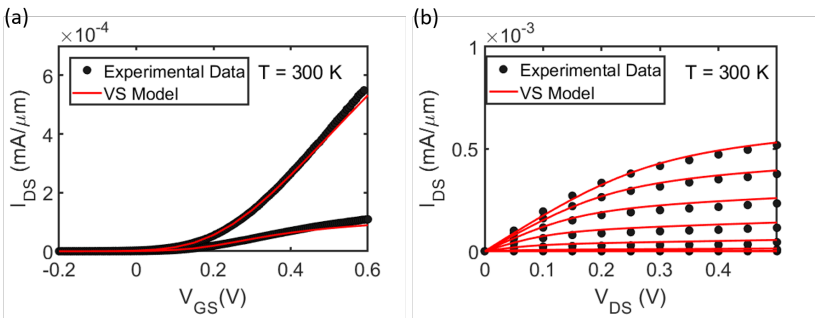

Figure 3.7: Measured and virtual source modelled (a) transfer and (b) output characteristics of a vertical InAs/InGaAs GAA MOSFET.

The virtual source model which is in good agreement with experimental data is used to extract parameters such as mobility for device evaluation.

3.3.2 EFFECT OF STACKING FAULTS ON MEAN FREE PATH

Vertical InAs nanowires grown under growth conditions used in this work typically have a wurtzite crystal structure. However, in previous reports, it has been seen with transmission electron micrography that the introduction of Ga forms a zincblende segment at the InAs/InGaAs junction. The crystal structure change also introduces stacking faults in the nanowire drain region [55]. It is also known that the presence of a single stacking fault in the MOSFET channel region can degrade performance due to reduced mean free path caused by carrier scattering [56]. Therefore, it was important to check if the presence of stacking faults in the drain region in our MOSFETs were leading to mobility degradation.

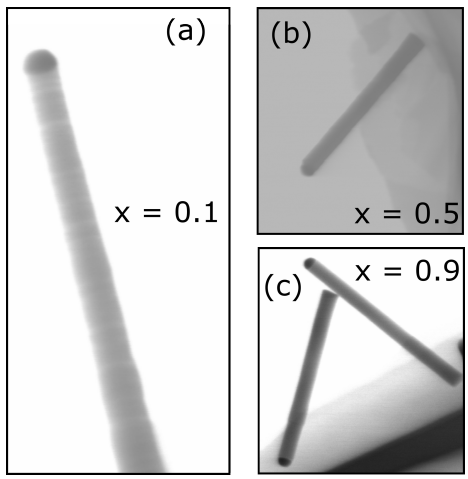

Figure 3.8: STEM images of InAs/InGaAs nanowires with increasing indium concentration.

In literature it has also been shown that a higher temperature and a lower V/III ratio can result in a low stacking fault density and gives less shell growth [57]. To modify the previously used growth parameters, the growth temperature was increased from 460°C to 490°C and V/III ratio was lowered from 21 to 4. Figure 3.8 shows STEM images of the nanowire grown at 490°C but with varying In compositions. It was observed that for the lowest In composition of 0.1, stacking faults were clearly present as can be noted from Figure 3.8 (a). Whereas for an In concentration of 0.5 and higher, no visible stacking faults were observed as can be noted from Figure 3.8 (b) and (c).

To study the effect of stacking faults on the mean free path for the new growth, the gate-length of the MOSFETs on the same sample was varied from 15 nm to 180 nm. The gate-length scaling was done by keeping the bottom HSQ spacer height constant while the top metal was moved by varying EBL doses as described in the previous section. The bottom spacer height is not varied in order to have the same source resistance across the sample (R_S). The resulting MOSFETs with L_G between 70 nm - 100 nm have comparable ON-resistance to previously used growth recipe (R_{ON}) as shown in Figure 3.9 (b). When operated in the quasi-ballistic regime, the transconductance (g_m) and transmission (T) are given by

$$g_m = T.g_{m_{ballistic}} \tag{3.4}$$

$$T = \frac{\lambda}{\lambda + L_G} \tag{3.5}$$

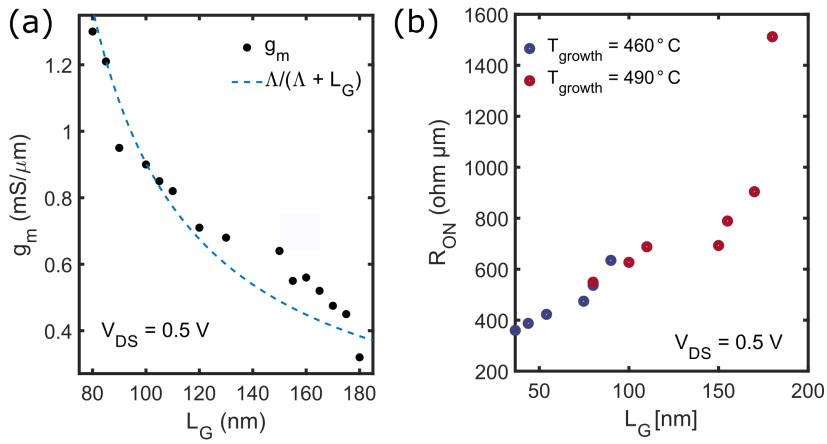

Figure 3.9: (a) Effect of g_m on gate length scaling where the dashed line represents the fitted transmission, T (b) Effect of R_{ON} on gate length scaling for two different growth temperatures.

where λ is the mean free path and L_G is the gate-length. By fitting T to the experimental data as shown in Figure 3.9 (a), $\lambda \sim 41$ nm. From the previous study when growth temperature was 460°C and stacking faults were clearly observed, the mean free path was $\lambda = 35 \pm 15$ nm [41]. These results indicate that the presence of stacking faults in the high field drain region do not affect the mean free path significantly.

3.3.3 PROSPECT FOR CRYOGENIC MEMORY APPLICATIONS

With rapid advancements in quantum electronics and quantum computing, cryogenic data storage is crucial for the development of these systems to become more scalable and practical [58]. Therefore, we looked into the performance of vertical InAs/InGaAs MOSFETs when operated at lower temperatures.

LOW-FREQUENCY NOISE

Figure 3.10 (a) shows the transfer characteristics of an InAs/InGaAs MOSFET where ripples in current can be observed throughout the curve. These ripples arise due to different forms of noise. Thermal noise ($S_I = 4K_BT/R$) and shot noise ($S_I = 2qI$) sources are present in all electrical devices but are frequency independent. In addition to these two noise sources, another significant source of noise arises from the oxide defects/traps that also result in current

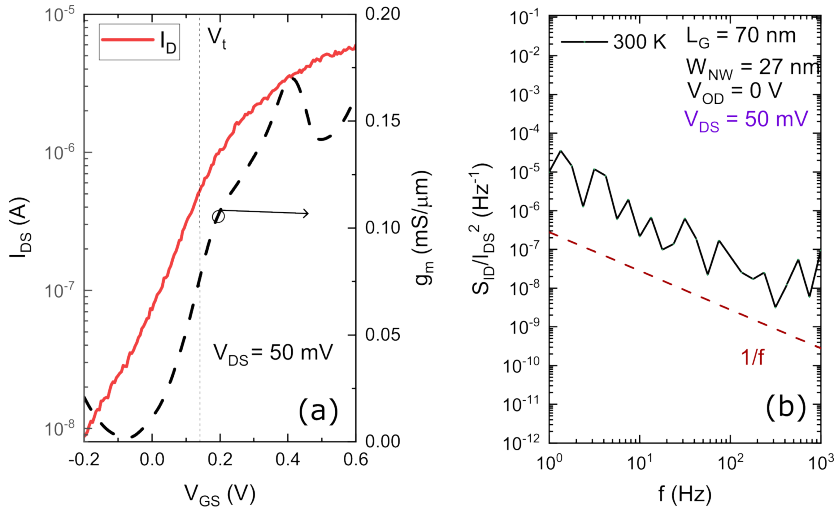

Figure 3.10: (a) Transfer characteristics of an InAs/InGaAs MOSFET measured at T= 300 K (b) Drain current noise spectral density (S_{ID}) plotted vs. frequency showing $1/f$ behaviour.

hysteresis. The noise originating from oxide traps is often summarized as low-frequency noise (LFN).

In 1957, A. L. McWhorter introduced a model that is widely used to describe the occurrence of low-frequency noise (LFN) resulting from oxide traps [60]. A comprehensive explanation of low-frequency noise, including recent advancements since 1957, can be found in [61]. Due to the $1/f$ dependence of the current noise spectral density, as can be observed in Figure 3.10 (b), this type of noise is also referred to as $1/f$ noise. The $1/f$ noise is detrimental to circuits, for e.g. mixer circuits where the noise can get mixed with the actual signal.

Paper III discusses the low-temperature $1/f$ noise characterization of vertical InAs/InGaAs MOSFETs. $1/f$ noise or low-frequency noise (LFN) is a dominant source of noise in modern electronic circuits as well as in qubits used for quantum computing [59] [62]. When the InAs/InGaAs MOSFET is operated at a temperature of 15 K, the steep subthreshold slope (SS) of 36 mV/dec along with a reduction in low-frequency noise may prove beneficial when used as a memory selector at lower temperatures [63].

Figure 3.11 (a) shows the DC switching characteristics for the first 100 cycles of a planar RRAM measured at 14 K with the same material stack discussed in

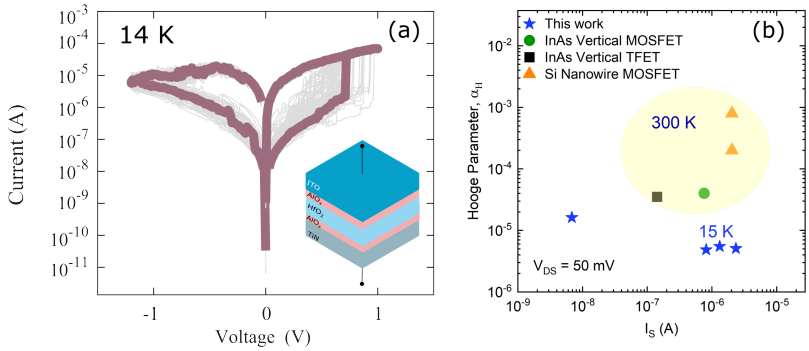

Figure 3.11: (a) $I-V$ characteristics of a stand-alone ITO/Oxide/TiN RRAM measured at 14 K (b) Calculated Hooge parameter for the InAs/InGaAs MOSFET at 15 K compared to room temperature for other nanowire MOSFET technologies.

the previous chapter. Moreover, in the InAs/InGaAs MOSFET, the reduction of the material dependant Hooge parameter (α_H) which describes the electron-phonon scattering in the channel is attributed to reduced surface scattering at 15 K due to freezing out of interface traps. The Hooge parameter is calculated using Equation 3.6 [64] [65] [66].

$$\frac{S_{ID}}{I_S^2} = \frac{q\mu_{eff}\alpha_H V_{DS}}{L_G^2 f I_S} \tag{3.6}$$

Figure 3.11 (b) compares the calculated Hooge parameter for the InAs/In-

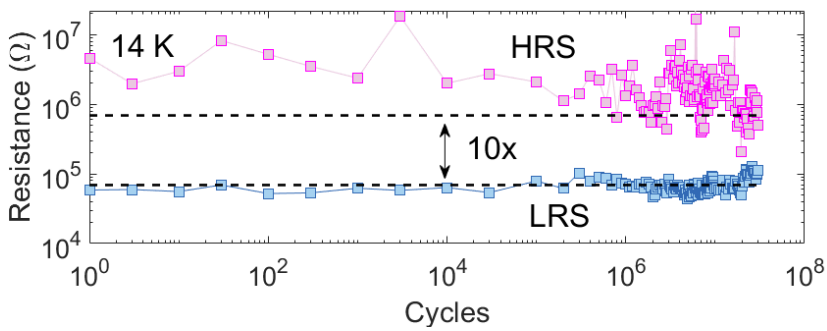

Figure 3.12: Endurance for the ITO/Oxide/TiN RRAM measured at 14 K with $t_{pulse} = 100\mu s$.

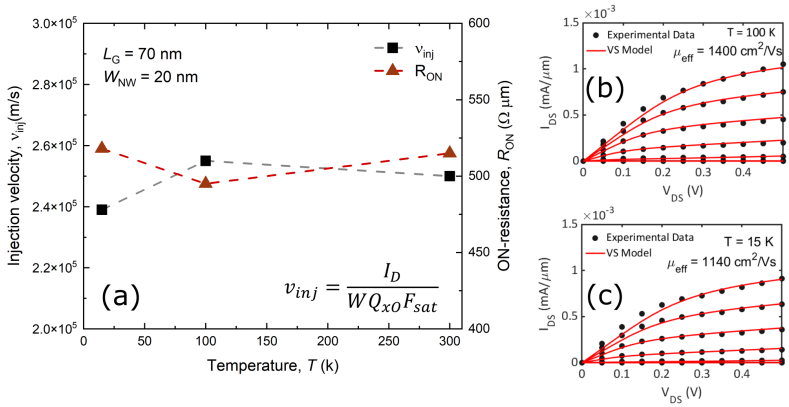

Figure 3.13: (a)Effect of temperature on injection velocity and ON-resistance for the vertical GAA InAs/InGaAs MOSFET (b) Output characteristics of the InAs/InGaAs MOSFET measured at 100 K (c) Output characteristics of the InAs/InGaAs MOSFET measured at 15 K where the solid line is the VS model.

GaAs MOSFET at 15 K versus other reported nanowire MOSFETs at room temperature.

An endurance measured to be $> 10^7$ with a memory window of $10\times$ for the planar ITO/oxide/TiN RRAM at 14 K is also a positive indicator for RRAMs to be used in cryogenic circuits. The endurance measured at 14 K is shown in Figure 3.12.

Figure 3.13 shows the effect of temperature on MOSFET parameters extracted using the virtual source model such as ON-resistance, mobility, and injection velocity. The knowledge of the vertical nanowire MOSFET parameter change with temperature is useful when designing a 1T1R cell aimed towards cryogenic applications.

4

Vertical Nanowire GAA-1T1R

As transistors are aggressively scaled down, various short-channel effects, including drain-induced barrier lowering (DIBL), threshold voltage roll-off, and velocity saturation, start to degrade transistor performance. To enhance the gate's electrostatic control over the channel, double or triple gates, such as finFETs, are employed at scaled nodes. Additionally, the use of gate-all-around (GAA) MOSFETs further improves the suppression of short-channel effects by wrapping the channel with the gate from all sides. The vertical GAA MOSFETs due to their increased power

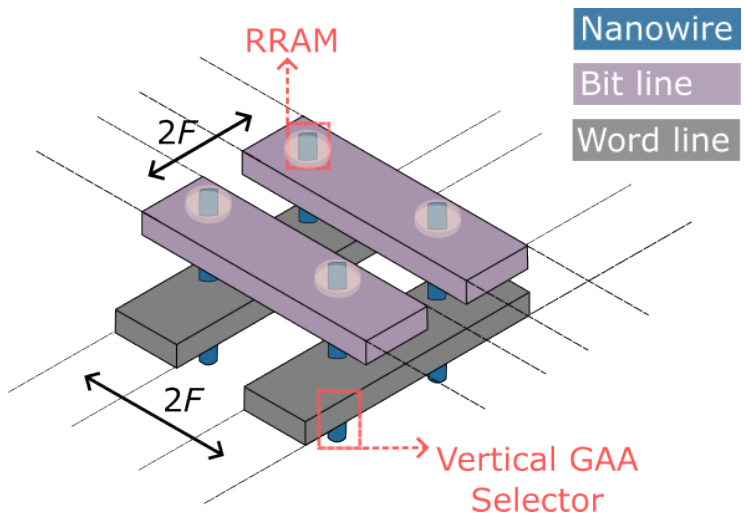

Figure 4.1: Crossbar array illustration of vertical GAA 1T1R cells with a cell footprint of $4F^2$.

saving and high-density integration capability are ideal candidates to be used in memory crossbar arrays. In crossbar arrays, the minimum feature size (F) is half the minimal distance between the centers of two metal lines. As illustrated in Figure 4.1, the vertical GAA MOSFET when implemented as a selector in crossbar arrays allows for RRAM integration with a minimal footprint of $4F^2$. Whereas, a planar finFET has a footprint of $6F^2$ which would limit the density of the crossbar array.

Micron, a key industry developer of memory technologies, has also identified a lack of scalable selectors as one of the main impediments to using RRAMs for mass storage. The researchers from Micron have raised the concern of supply voltage scaling too becoming increasingly difficult which is needed for low-power memory operation [67].

To the best of our knowledge, there are not many experimental reports demonstrating the 1T1R configuration using the vertical GAA MOSFET as a selector. In 2013 and 2014, Z. Fang et. al. and B. Chen et al. demonstrated successful RRAM integration with vertical Si nanopillar GAA MOSFETs [68] [69]. The reported Si-based vertical GAA MOSFET selectors reported in the literature are shown in Table 4.1.

The results, although encouraging, face certain limitations such as: 1) Limited endurance 2) High RRAM switching voltages and 3) High saturation voltage of Si MOSFET.

The use of III-V materials could aid in scaling down the supply voltage while achieving sufficient current densities, which are currently constrained in Silicon-based MOSFET selectors.

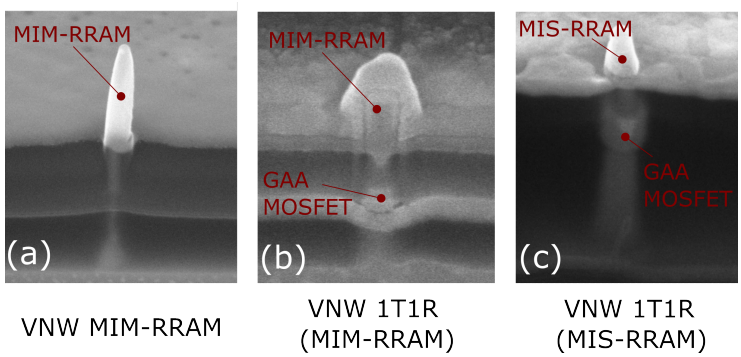

Figure 4.2: Cross-sectional SEM images of (a) VNW MIM-RRAM which was further developed to (b) VNW GAA 1T1R MIM-RRAM and the (c) VNW GAA 1T1R MIS-RRAM.

Table 4.1: Vertical GAA MOSFET based 1T1R demonstrations

	[68]	**[69]**	**[70]**	**Paper II**	**Paper I**
Channel	Si	Si	Si	InAs	InAs
Geometry	GAA Nanopillar	GAA Nanopillar	GAA Nanopillar	GAA Nanowire	GAA Nanowire
V_{SET}/V_{RESET} (V) - DC	2.5/-1.08	2.0/-0.5	2.5/-1.08	0.3/-0.4	0.2/-0.8
Endurance (cycles)	200	20	10^5	10^4	10^6
Retention (s)	2×10^3 (RT)	-	3×10^4 (85°C)	-	10^4 (85°C)
MOSFET Saturation Voltage (V)	> 1.5	> 1.5	> 1.5	0.5	0.5

In this chapter, the experimental realization of the VNW 1T1R cell is described. The effect of geometry change from planar to vertical nanowire on the RRAM performance is also evaluated prior to the integration of the MOSFET selector. The cross-sectional SEM images of the VNW 1R and the subsequent VNW 1T1R with a metal-insulator-metal (MIM) and metal-insulator-semiconductor (MIS) configuration are shown in Figure 4.2.

4.1 VERTICAL NANOWIRE MIM-RRAM (1R)

4.1.1 FABRICATION

The InAs vertical nanowire (VNW) used for housing the RRAM cell is grown from a 300 nm-thick InAs buffer layer on a Si substrate. InAs VNWs as shown in Figure 4.3 (a) were grown using the Vapor-Liquid-Solid (VLS) method in MOVPE where Au dots were first defined by electron beam lithography (EBL). In the process used for high performance III-V vertical MOSFETs, hydrogen silsesquioxane (HSQ) is used as the bottom spacer to reduce the gate-to-source capacitance (C_{gs}). To emulate the MOSFET process in [37], an HSQ bottom spacer is spin-coated as illustrated in Figure 4.3 (b). In this case, the 400 nm-thick bottom spacer separates the RRAM bottom electrode (B.E.) and the substrate. The thickness of the HSQ layer can be defined by varying the dose of the EBL exposure. For the RRAM B.E., TiN is deposited using PEALD

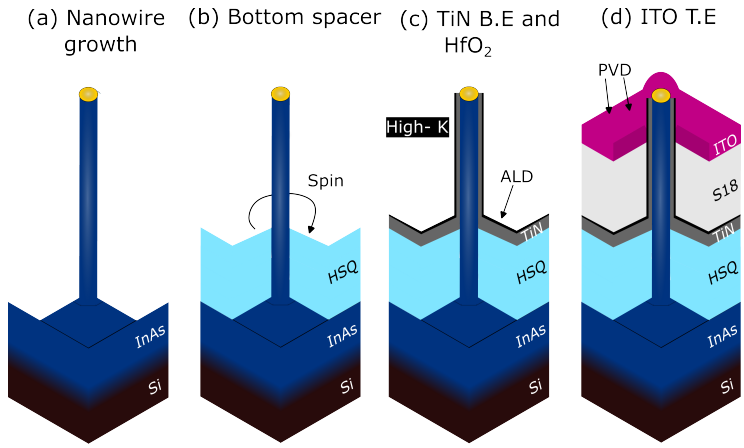

Figure 4.3: Cross-sectional illustration of the key steps in the process flow to fabricate a vertical nanowire MIM-RRAM.

at 250°C with a Tetrakis(dimethylamido)titanium (TDMAT) precursor and a N_2 plasma. The B.E. contact is then defined by photolithography followed SF_6/N_2 based reactive-ion etching as illustrated in Figure 4.3 (c).

The 4 nm-thick HfO_2 RRAM switching oxide is deposited by PEALD using a Tetrakis(ethylmethylamido)hafnium precursor at 200°C. For the top spacer, (S1813-resist) is spin-coated and then permanently baked at 200°C. The RRAM area is defined by a resist etch-back using an O_2 plasma to expose the top 400 nm of the nanowire top segment.

For the RRAM T.E., a 40 nm-thick ITO followed by a 40 nm-thick Au for probing is sputtered. The above-mentioned electrode thicknesses are the lateral thicknesses. The thickness on the nanowire sidewalls is approximately $1/3^{rd}$ of the lateral thickness. The metal electrode is then patterned and defined using UV-lithography followed by a lift-off process. A cross-sectional SEM image of the completed VNW-RRAM is shown in Figure 4.2 (d).

4.1.2 PERFORMANCE

Paper VI discusses the measurements on the VNW MIM-RRAM in detail. The $I-V$ switching characteristics for the ITO/HfO_2/TiN RRAM integrated on a vertical nanowire are shown in Figure 4.4 (a). Figure 4.4 (b) shows the effect of switching oxide thickness scaling on the forming voltage for the planar and nanowire RRAMs (ITO/HfO_2/TiN). The VNW MIM-RRAM consisting of the material stack at similar oxide thicknesses when compared to the planar RRAM exhibits a higher forming voltage. The increase in forming voltage when decreasing the cell area by about 100x is expected. This is due to having

less number of defects in a smaller area which in turn reduces the probability of filament formation [71] [72].

Apart from the increase in forming voltage, the performance of the wrap-

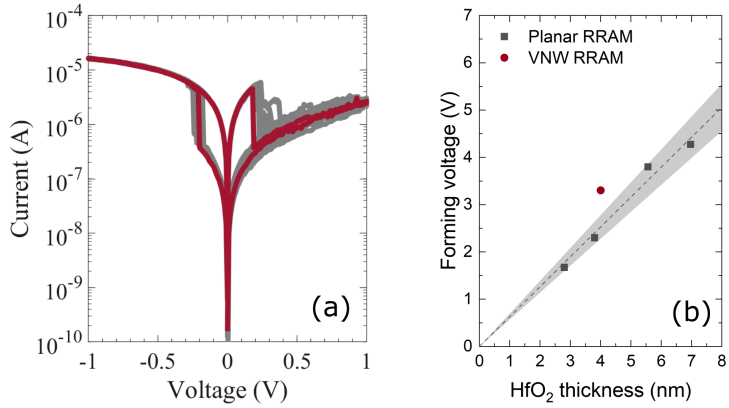

Figure 4.4: (a) Switching $I-V$ characteristics of the VNW MIM-RRAM (b) Effect of the oxide thickness on the forming voltage.

around VNW-MIM ITO/HfO_2/TiN RRAM is retained when compared to its planar counterpart. The performance metrics comparing the two geometries are shown in Table 4.2.

Table 4.2: Effect of geometry on RRAM performance

Geometry	**Area (μm^2)**	**t_{ox} (nm)**	**V_{FORM} (V)**	**V_{SET} (V)**	**V_{RESET} (V)**	**Memory Window**	**Endurance**
Planar (MIM)	7	3.3	3.7	0.4	0.4	>100x	10^6
Nanowire (MIM)	0.06	4	3.3	0.3	0.3	>100x	10^6

4.2 VERTICAL GAA 1T1R WITH MIM-RRAM

As the 100x area reduction achieved by geometry transfer from planar to wrap-around vertical nanowire did not impact the switching performance

negatively, a gate-all-around MOSFET selector is realized on the same nanowire.

4.2.1 FABRICATION

The key steps for the fabrication of the III-V VNW-1T1R is shown in Figure 4.5. The 1T1R devices are fabricated on a p-type Si substrate on which an InAs buffer layer is first grown using MOVPE. The nanowires are then grown using the same method as described in the previous section for the III-V VNW MIM-RRAM. The only difference now is that the nanowire top segment where the RRAM is housed (MOSFET drain) is highly doped InGaAs. The introduction of Ga on the drain side introduces a wider bandgap to reduce the OFF-state leakage current [73]. Similar growth was also used by Kilpi et al [41].

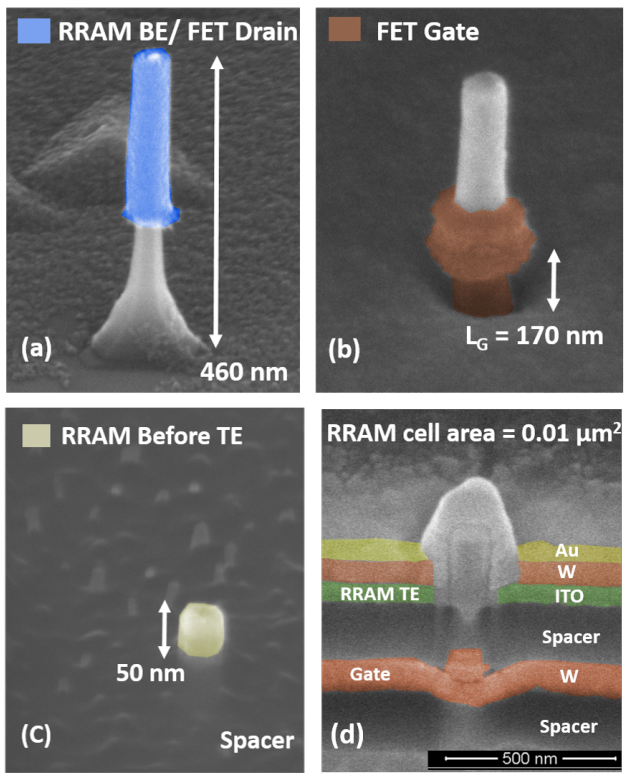

Figure 4.5: SEM images of the key steps in the process flow to fabricate a vertical GAA 1T1R with a MIM-RRAM.

It should be noted that for the III-V VNW 1T1R, the RRAM B.E. and MOSFET drain contact is the same which reduces process complexity and maintains material compatibility. For the RRAM B.E./MOSFET drain, a 400 nm-thick hydrogen silsesquioxane (HSQ) film is spin-coated and EBL is used to define the height. Next, a 20 nm-thick Mo layer is sputtered followed by ALD deposition of 15 nm-thick TiN. For the RRAM B.E./MOSFET drain to remain only on the nanowire sidewalls, RIE is used to anisotropically etch the horizontal metal layer. The HSQ layer used to define the metal height is then removed using a BOE wet etch. A SEM image of the III-V VNW 1T1R post-RRAM B.E./MOSFET drain definition is shown in Figure 4.5 (a).

The GAA-MOSFET gate length (L_G) is defined to be 170 nm using HSQ height control by EBL. A gate-last process is also used by M. Berg et al. [44]. Before putting on the gate stack, the highly doped shell is removed by using a digital etch process. For the gate stack, first the gate dielectric consisting of an Al_2O_3/HfO_2 bilayer is deposited using TALD. The thickness of the gate dielectric is 4 nm which corresponds to an EOT of 1.5 nm. The gate metal consisting of a 2 nm-thick TiN followed by a 60 nm-thick W is deposited using ALD and sputtering respectively. A SEM image of the III-V VNW 1T1R post-gate stack deposition is shown in Figure 4.5 (b).

For the wrap-around RRAM cell definition, the bilayer gate dielectric is selectively removed from the top segment of the nanowire which is defined by a resist etch-back. The 2.8 nm-thick RRAM switching oxide is deposited using PEALD at 200°C with similar conditions described in the previous section. To separate the GAA-MOSFET gate from the RRAM, S1813 resist spacer was spin-coated at baked at 200°C. The RRAM cell area can be defined by thinning the spacer layer as shown in Figure 4.5 (c) where 50 nm of the nanowire top segment is exposed. The 30 nm-thick ITO RRAM top electrode is deposited and patterned similarly as explained in the previous section. A cross-sectional SEM image of the completed 1T1R is shown in Figure 4.5 (d).

4.2.2 PERFORMANCE

Paper II discusses the measurements on the GAA 1T1R MIM-RRAM. The electrical characteristics of the vertical GAA 1T1R are measured by first forming the ITO/HfO_2/TiN RRAM. A positive bias (V_{DS}) is applied to the RRAM T.E. while the GAA-MOSFET is in the ON-state. The relatively larger bandgap of the InGaAs drain compared to the InAs source is also beneficial during the higher voltages applied during the forming process. The RRAM switching performance of the integrated RRAM is summarized in Table 4.3 where it can be seen that the performance is retained even after selector integration. Figure 4.6 (a) and (b) show the RRAM switching characteristics and the GAA-MOSFET output characteristics with effective current modulation. The

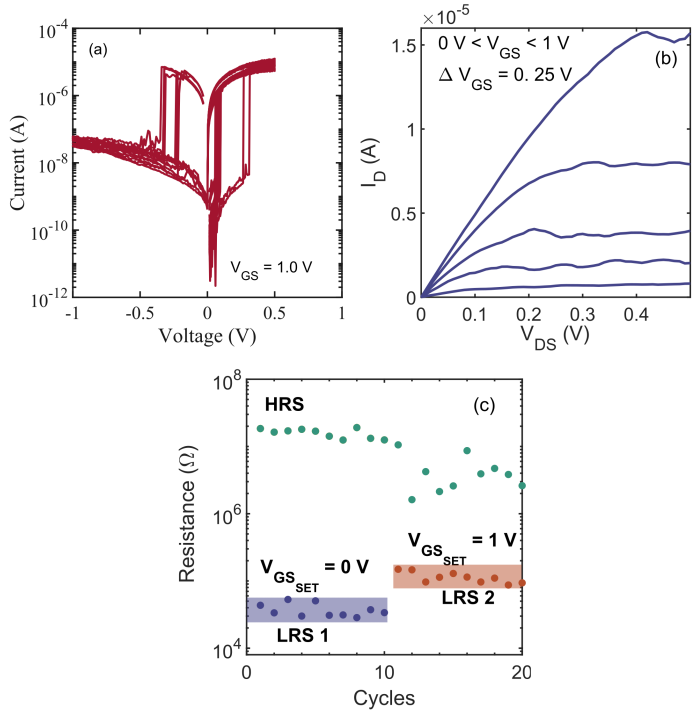

Figure 4.6: (a)$I-V$ switching characteristics of the integrated MIM-RRAM (b) Output characteristics of the vertical GAA MOSFET selector (c) Two distinct LRS levels achieved by changing the selector gate voltage.

selector gate can also be used to change the compliance current during the SET operation which can enable more than one state by controlling the LRS as shown in Figure 4.6 (c).

4.3 VERTICAL GAA 1T1R WITH MIS-RRAM

4.3.1 FABRICATION

The process schematic for fabricating the vertical GAA 1T1R where the RRAM stack consists of InAs/HfO_2/W is shown in Figure 4.7. As explained in previous sections, the vertical InAs nanowires are grown using MOVPE with the help of VLS growth. For the VLS growth, Au seed particles were defined using EBL. For the MIS structure, the previously used ITO metal electrode is now replaced by the InAs nanowire itself. The VNW is intended to act

Table 4.3: Effect of geometry on RRAM performance

Geometry	Area (μm^2)	t_{ox} (nm)	V_{FORM} (V)	V_{SET} (V)	V_{RESET} (V)	Memory Window	Endurance
Planar (MIM)	7	3.3	3.7	0.4	0.4	>100x	10^6
Nanowire (MIM)	0.06	4	3.3	0.3	0.3	>100x	10^6
GAA 1T1R (MIM)	0.01	2.8	3.1	0.3	0.4	>500x	10^4

as the RRAM T.E. as well as the selector MOSFET channel. As no separate drain metal electrode is used, a sacrificial SiO_2 layer is deposited to cap the top segment of the nanowire. This is first done by spin-coating and baking S1813 followed by an O_2 resist etch back so that only the top segment of the nanowire is exposed. The SiO_2 layer is then deposited using PEALD and anisotropically etched using RIE with an SF_6/N_2 chemistry. After this step, the SiO_2 layer only remains on the nanowire sidewalls as illustrated in Figure 4.7 (b). Once the top segment of the nanowire is protected, the highly doped shell in the MOSFET channel region is removed using a digital etch process.

For the gate stack, first an Al_2O_3/HfO_2 bilayer which is 7 nm-thick is deposited using thermal ALD. The gate metal which consists of a 2 nm-thick TiN and a 60 nm-thick W layer is deposited using ALD and sputtering.

A gate length of 200 nm was defined by a resist etch back followed by RIE of the gate metal. Before the RRAM oxide deposition, the gate dielectric and the SiO_2 cap present at the top segment of the nanowire is selectively removed using a BOE or HF 1:100 solution. For the RRAM oxide, 2.8 nm-thick HfO_2 is deposited using PEALD and the first 10 ALD cycles are used to oxidize the $InAs/HfO_2$ interface with a plasma length (t_{plasma} =80 s). S1813 is used as the top spacer to separate the gate stack from the RRAM stack and is etched back using an O_2 plasma till the top segment of the nanowire is exposed. The RRAM B.E., W is deposited and patterned using sputtering and photolithography.

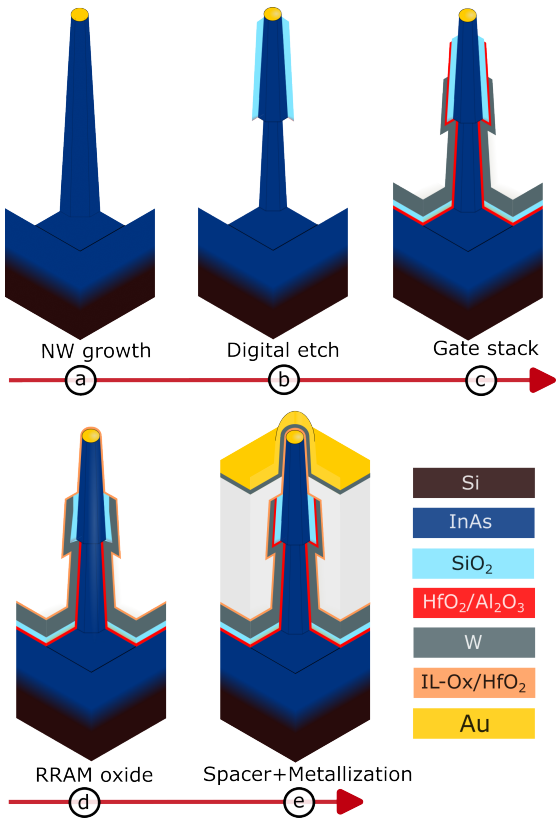

Figure 4.7: Cross-sectional illustration of the key steps in the process flow to fabricate a vertical GAA 1T1R with a MIS-RRAM.

4.3.2 PERFORMANCE

Paper I discusses the measurements on the GAA 1T1R MIS-RRAM in detail and Table 4.4 summarizes the performance . The switching $I-V$ characteristics for the InAs/IL-oxide/W integrated in a 1T1R cell is shown in Figure 4.8. The voltage ranges allowed by the fabricated 1T1R cell can allow integration of other promising RRAM oxides such as TaO_x and Al_2O_3 [74] [75].

4.4 III-V/HIGH-K INTERFACE CONTROL

The fabricated III-V vertical GAA 1T1R cell has good resistive switching properties as well as efficient current modulation offered via the selector gate. Although the selector gate stack (InAs/High-k/TiN+W) and the RRAM

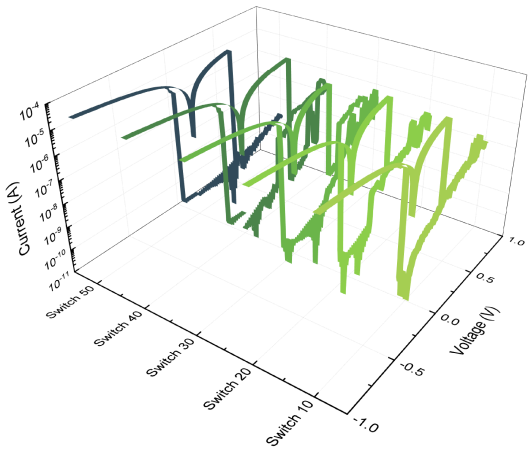

Figure 4.8: $I - V$ switching characteristics of the integrated MIS-RRAM.

Table 4.4: Effect of geometry on RRAM performance

Geometry	**Area (μm^2)**	**t_{ox} (nm)**	**V_{FORM} (V)**	**V_{SET} (V)**	**V_{RESET} (V)**	**Memory Window**	**Endurance**
Planar (MIM)	7	3.3	3.7	0.4	0.4	>100x	10^6
Nanowire (MIM)	0.06	4	3.3	0.3	0.3	>100x	10^6
GAA 1T1R (MIM)	0.01	2.8	3.1	0.3	0.4	>500x	10^4
GAA 1T1R (MIS)	0.01	2.8	3.0	0.2	0.8	10^4	10^6

stack (InAs/IL-oxide/high-k/ W) are similar, the InAs/high-k interface and the process conditions are different as follows:

1. Before depositing the selector gate oxide, the InAs native oxides are removed. The removal of interface oxides enables stable MOSFET performance due to the reduction of interface traps.

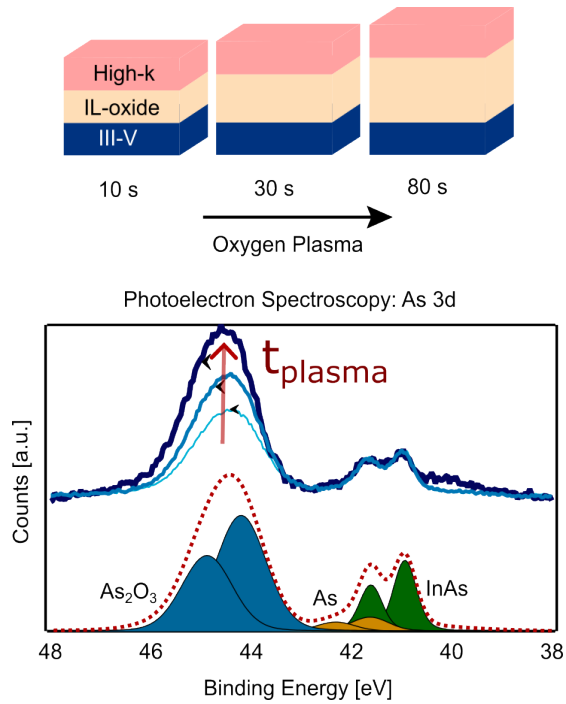

Figure 4.9: Dedicated planar samples where the IL-oxide growth was controlled using the oxygen plasma length duration during PEALD deposition of HfO_2 where the growth of the IL-oxide was verified using XPS measurements.

2. For the RRAM oxide, the InAs surface is first oxidized by exposing InAs to an oxygen plasma for 80 s so that a balanced interlayer oxide (IL-oxide) is created which was found to improve RRAM performance. The resulting dual oxide layer configuration is shown in Figure 4.9. The IL-oxide thickness is controlled by the pulse length (t_{plasma}) during PEALD which was also confirmed using XPS measurements carried out at the Max IV synchrotron facility in Lund.

4.5 VERTICAL NANOWIRE NAND GATE

In addition to the data storage capabilities of RRAMs, they have also been shown to perform logical operations. A way of realizing basic logic capabilities is to demonstrate the "universal gate," which is the NAND gate. By utilizing the NAND gate in a combinational circuit, any logic operation can

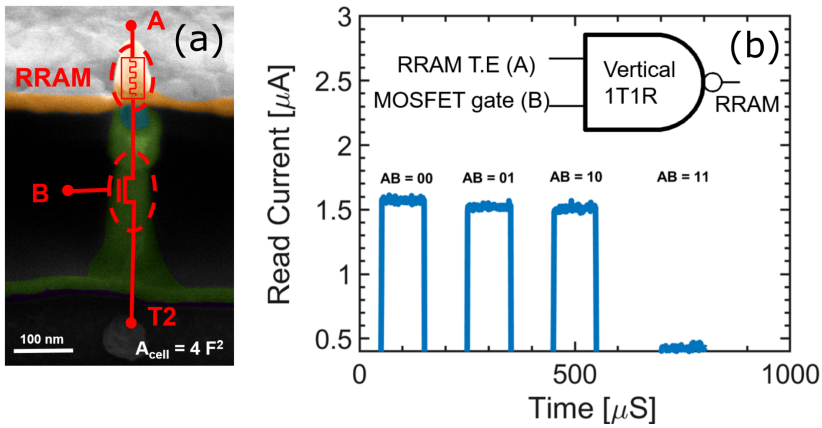

Figure 4.10: (a) Schematic illustrating the use of a GAA 1T1R cell as a NAND gate (b) The truth table of a NAND gate obtained by applying voltage pulses to terminal A and B of vertical nanowire.

be achieved. The logic capabilities of the universal NAND gate have been previously demonstrated in other studies [76] [77].

In this work, a measurement scheme as descibed in Paper I is used to replicate the truth table of NAND gate. Figure 4.10 briefly shows how a boolean NAND gate can be implemented on a vertical nanowire 1T1R at a footprint of $4F^2$. Whereas, a conventional tranistor based NAND gate occupies a footprint of $200F^2$.

This work presents a vertical GAA 1T1R cell that provides a scalable solution, overcoming limitations imposed by the conventional transistor footprint.

5

Summary and Outlook

Over the course of this thesis, a comprehensive understanding has been developed for the integration of resistive random access memories with III-V vertical nanowire gate-all-around MOSFETs. In this work, to the best of our knowledge, a vertical 1T1R cell with the highest reported switching endurance for a GAA vertical 1T1R cell is fabricated. Figure 5.1 compares the switching endurance of the vertical 1T1R cell with other commonly used selector technologies. While the planar 1T1R and 1S1R currently exhibit higher reported endurances, their footprint is relatively large. The results obtained in this thesis demonstrates a way to realize a vertical 1T1R cell with good performance at a minimal footprint, making it advantageous for dense crossbar array integration.

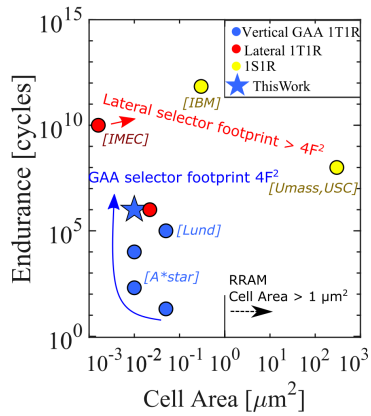

Figure 5.1: Benchmarking endurance vs. cell area [78].

To summarize this thesis; first, RRAMs and MOSFETs were individually realized and characterized. The effect of the geometry (planar to vertical) of the ITO/HfO_2/TiN RRAM cell was studied where low power switching and high endurance were preserved in the vertical configuration. Moreover, InAs was used as the channel material for the GAA MOSFET selector to harness the advantageous transport properties of III-V materials, which are desirable for scaling the supply voltage. Additionally, an approach was developed, utilizing InAs as both the selector channel and the RRAM electrode, achieved by engineering the InAs native oxides.

This thesis also presents low-frequency noise characterization of both the RRAM cell and the MOSFET, with the aim of gaining further insights into the oxide/semiconductor interface. The vertical 1T1R cell developed in this work allows for the implementation of Boolean logic operations using a single vertical nanowire while reducing the footprint by a factor of 51 compared to the traditional CMOS counterpart.

As a proposition for future research, it would be interesting to modify the RRAM material stack in order to enable analog switching behavior. This modification could enhance the attractiveness of the technology and align it more closely with neuromorphic applications. While the voltage ranges for the demonstrated analog RRAMs are compatible with our reported 1T1R structure, an actual demonstration would serve as an important initial step [79] [80].

With the growing interest in cryogenic applications, especially in the context of quantum computing advancements and electronics for space, it becomes intriguing to demonstrate neuromorphic computing/compute-in-memory capabilities at cryogenic temperatures.

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APPENDICES

A

Fabrication Recipes

In this appendix, the fabrication flows used in this thesis are described in detail.

VERTICAL 1T1R MIM-RRAM

NANOWIRE GROWTH

Nanowire growth reference: 3100 CCS. InAs/InGaAs Wires were grown by Johannes Svensson.

TOP METAL FABRICATION

- Remove Fox-15 (HSQ) from freezer and wait till it reaches room temperature (30 minutes)
- Sample prebake (2 min 150°C on the hotplate)
- Spin coat HSQ (60s at 3000 RPM)
- Clean backside followed by Postbake (2 min 200°C on the hotplate)
- EBL exposure (Perform dose test before on InAs test sample)
- HSQ development in 25% TMAH and transfer to DI water followed by microscope inspection
- Native oxide removal (HCl:IPA for 30s)
- 20 nm Mo sputtering with Ar flow 12 sccm
- 15 nm TiN using PEALD at 250°C
- Anisotropic Mo/TiN RIE Apex (SF_6, N_2) for 22 s (Inspect in microscope to make sure metal is removed)

- HSQ removal using BOE 1:10 for 20 s (Without stirring the sample to avoid risk of collapsing nanowires)
- SEM inspection

BOTTOM SPACER

- Remove Fox-15 (HSQ) from freezer and wait till it reaches room temperature (30 minutes)
- Sample prebake (2 min 150°C on the hotplate)
- Spin coat HSQ (60s at 3000 RPM)
- Clean backside followed by Postbake (2 min 200°C on the hotplate)
- EBL exposure (Perform dose test before on InAs test sample)
- HSQ development in 25% TMAH for 60s and transfer to DI water
- SEM inspection

DIGITAL ETCH AND HIGH-K DEPOSITION

Digital etch:

- 5 min O_3 oxidation at 50°C
- 20s HCl:IPA (No stirring, move when bubbles cover the surface roughly after 15 s) and move sample to IPA beaker
- SEM inspection and repeat process till target diameter is achieved

High-k deposition:

- Surface cleaning with 10 cycles TMA at 300°C in Savannah ALD
- 6 cycles Al_2O_3 at 300°C using TMA and H_20
- 36 cycles HfO_2 at 120°C using TDMAHf and H_2O

GATE DEFINITION AND GATE PAD PATTERNING

The height of the gate is defined by thinning down the resist and etching the gate-metal. It is important to ensure that there is a small overlap of the gate metal with the top metal contact to avoid ungated area.
Gate definition:

- 2 nm TiN using PEALD
- 60 nm W sputtering with Ar flow of 16 sccm
- Prebake 2 min at 115°C
- Spin coat S1813 resist (60 s at 4000 rpm)
- Postbake 15 min at 120°C
- Thinning resist (O_2 RIE at 300 m Torr in Trion)
- Gate-metal etch (SF_6 and Ar RIE in Trion at 185 mTorr)
- O_2 plasma residual removal

- S1813 resist removal in acetone and then transfer to IPA

Gate pad patterning:

- Prebake 2 min at 115 C
- Spin coat S1813 resist (60 s at 4000 rpm)
- Softbake 90 s at 120 C
- Soft UV define gate pad
- S1813 development (MF319 90 s) and transfer to DI water
- Postbake 15 min at 120 C
- W etch (SF_6 and Ar RIE in Trion at 185 mTorr)
- O_2 plasma residual removal
- S1813 resist removal in acetone and then transfer to IPA

RRAM OXIDE AND SECOND SPACER

- Repeat resist thinning step and BOE etch to remove gate-oxide from the top 50 nm-100 nm of the wire
- 26 cycles HfO_2 at 200°C using PEALD (Fiji).
- Prebake 2 min at 115°C
- Spin coat S1813 resist (60 s at 4000 rpm)
- Postbake 40 min at 200°C
- Thinning resist till desired height of nanowire (50nm-100 nm) is exposed (O_2 RIE at 300 m Torr in Trion, etch rate 0.65-0.70 nm/s)

RRAM T.E. AND FINAL METALLIZATION

RRAM T.E.:

- Sputter 30 nm ITO.
- Prebake 2 min at 115°C
- Spin coat S1813 resist (60 s at 4000 rpm)
- Softbake 90 s at 120°C
- Soft UV ITO disc structure / Lift-off also available in mask design
- S1813 development (MF319 90 s) and transfer to DI water
- ITO etch using Cl_2 and Ar (Etch rate 100 nm/sec).
- O_2 plasma residual removal
- S1813 resist removal in acetone and then transfer to IPA

Open vias:

- Prebake 2 min at 115°C
- Spin coat S1813 resist (60 s at 4000 rpm)
- Softbake 90 s at 120°C
- Soft UV gate and source vias.

- S1813 development (MF319 90 s) and transfer to DI water
- Open the vias (O_2 RIE at 300 mTorr in Trion)
- Remove HSQ (1-100 HF) about 1 min 30 s, inspect in microscope

Contact pads:

- Sputter contact (40 nm W and 100 nm Au)
- Prebake 2 min at 115°C
- Spin coat S1813 resist (60 s at 4000 rpm)
- Softbake 90 s at 120°C
- Soft UV contact pads.
- S1813 development (MF319 90 s) and transfer to DI water
- Postbake 15 min at 120°C
- Etch Au (KI based wet etch) - Optical inspection after 15 s and add 5 s and repeat to avoid overetching close to nanowires.
- W etch (SF_6 and Ar RIE in Trion at 185 mTorr, 45 s etches about 60 nm)
- S1813 resist removal in acetone and then transfer to IPA

VERTICAL 1T1R MIS-RRAM

NANOWIRE GROWTH

Nanowire growth reference: 3356 CCS. InAs wires were grown by Johannes Svensson.

SIO_2 CAP

As the InAs nanowire is used as the RRAM electrode, no top metal is deposited. Instead, a sacrificial SiO_2 cap is used to protect the RRAM segment of the wire from digital etching.

- Prebake 2 min at 115°C
- Spin coat S1813 resist (60 s at 4000 rpm)
- Postbake 15 min at 120°C
- Resist thinning to expose the top segment of the wire (O_2 RIE at 300 mTorr in Trion)
- 100 cycles SiO_2 at 200°C using PEALD (fiji)
- Anisotropic SiO_2 etch in Apex (SF_6, N_2)
- S1813 removal using acetone
- SEM inspection

BOTTOM SPACER AND DIGITAL ETCH

Bottom spacer:

- 200 cycles Al_2O_3 at 120°C using TMA and H_20
- Prebake 2 min at 115°C
- Spin coat S1813 resist (60 s at 4000 rpm)
- Postbake 15 min at 120°C
- Resist thinning till the just the foot of the nanowire is covered (O_2 RIE at 300 mTorr in Trion)
- Etch Al_2O_3 from the nanowires using HF 1:100 or BOE. Calibrate etch rate on planar sample.
- S1813 removal using acetone

Digital etch:

- 5 min O_3 oxidation at 50°C
- 20s HCl:IPA (No stirring, move when bubbles cover the surface roughly after 15 s) and move sample to IPA beaker
- SEM inspection and repeat process till target diameter is achieved

HIGH-K DEPOSITION AND GATE DEFINITION

High-k:

- Surface cleaning with 10 cycles TMA at 300°C in Savannah ALD
- 6 cycles Al_2O_3 at 300°C using TMA and H_20
- 50 cycles HfO_2 at 120°C using TDMAHf and H_2O

Gate definition:

- 2 nm TiN using PEALD
- 60 nm W sputtering with Ar flow of 16 sccm
- Prebake 2 min at 115°C
- Spin coat S1813 resist (60 s at 4000 rpm)
- Postbake 15 min at 120°C
- Thinning resist (O_2 RIE at 300 m Torr in Trion)
- Gate-metal etch (SF_6 and Ar RIE in Trion at 185 mTorr)
- O_2 plasma residual removal
- S1813 resist removal in acetone and then transfer to IPA

Gate pad patterning:

- Prebake 2 min at 115 C
- Spin coat S1813 resist (60 s at 4000 rpm)
- Softbake 90 s at 120 C
- Soft UV define gate pad
- S1813 development (MF319 90 s) and transfer to DI water
- Postbake 15 min at 120 C
- W etch (SF_6 and Ar RIE in Trion at 185 mTorr)
- O_2 plasma residual removal

- S1813 resist removal in acetone and then transfer to IPA

RRAM OXIDE AND SECOND SPACER

- Repeat resist thinning step and BOE etch to remove the SiO_2 cap from the top 50 nm-100 nm of the wire
- 26 cycles HfO_2 at 200°C using PEALD with $_{tplasma}$ = 80 s (Fiji).
- Prebake 2 min at 115°C
- Spin coat S1813 resist (60 s at 4000 rpm)
- Postbake 40 min at 200°C
- Thinning resist till desired height of nanowire (50nm-100 nm) is exposed (O_2 RIE at 300 m Torr in Trion, etch rate 0.65-0.70 nm/s)

RRAM T.E. AND FINAL METALLIZATION

The RRAM T.E. in this structure is W which will be deposited as the final metallization step. Open vias:

- Prebake 2 min at 115°C
- Spin coat S1813 resist (60 s at 4000 rpm)
- Softbake 90 s at 120°C
- Soft UV gate and source vias.
- S1813 development (MF319 90 s) and transfer to DI water
- Open the vias (O_2 RIE at 300 mTorr in Trion)
- Remove HSQ (1-100 HF) about 1 min 30 s, inspect in microscope

Contact pads:

- Sputter contact (40 nm W and 100 nm Au)
- Prebake 2 min at 115°C
- Spin coat S1813 resist (60 s at 4000 rpm)
- Softbake 90 s at 120°C
- Soft UV contact pads.
- S1813 development (MF319 90 s) and transfer to DI water
- Postbake 15 min at 120°C
- Etch Au (KI based wet etch) - Optical inspection after 15 s and add 5 s and repeat to avoid overetching close to nanowires.
- W etch (SF_6 and Ar RIE in Trion at 185 mTorr, 45 s etches about 60 nm)
- S1813 resist removal in acetone and then transfer to IPA

B

Virtual Source Model

The virtual source model is one way of extracting MOSFET parameters such as access resistance, injection velocity, mobility, etc. As a starting point

- The model can be downloaded from:
  Rakheja, S. Antoniadis, D. (2015). MVS Nanotransistor Model. (Version 2.0.0). nanoHUB. doi:10.4231/D3416T10C.
- Load experimental data (transfer and output characteristics) and normalize current by taking into account the number of nanowires and the wire circumference.
- Other information needed before fitting: Gate length (L_G), inversion capacitance (C_{inv}), drain-induced barrier lowering (DIBL), equivalent oxide thickness (EOT) and threshold voltage. (For reference, the following values were used in this work L_G = 70 nm, C_{inv} = 0.1003 F/m^2, DIBL = 0.075 V/V , EOT = 1.5 nm)
- Enter the emperical fitting parametes α and β for fitting the transition from the MOSFET linear region to saturation region. The following values were used in this work for reference:

Table B.1: Input parameters

$T(K)$	α	β
15	2.5	1.1
100	2.5	1.6
300	2.5	1.6

- Mobility and access resistance were used as fitting parameters to obtain best possible fit to the experimental transfer and output characteristics. An example after the fitting is shown in Figure B.1.

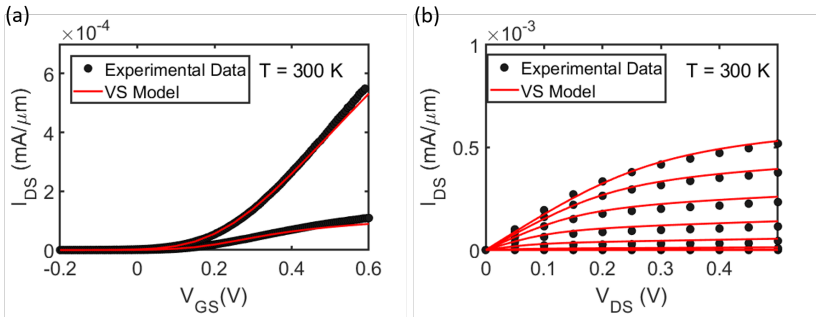

Figure B.1: Measured and virtual source modelled transfer and output characteristics of a vertical InAs/InGaAs GAA MOSFET.

- The obtained parameters in this work for measurements carried out at three different temperatures:

Table B.2: Output after fitting

$T(K)$	$\mu_{app}(cm^2/Vs)$	$v_{inj}(m/s)$	$R_s + R_d(\Omega\mu m)$
15	1100	2.39×10^5	358.8
100	1400	2.55×10^5	356.8
300	1300	2.5×10^5	355.6