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Vertical III-V Nanowire Transistors for Low-Power Logic and Reconfigurable Applications

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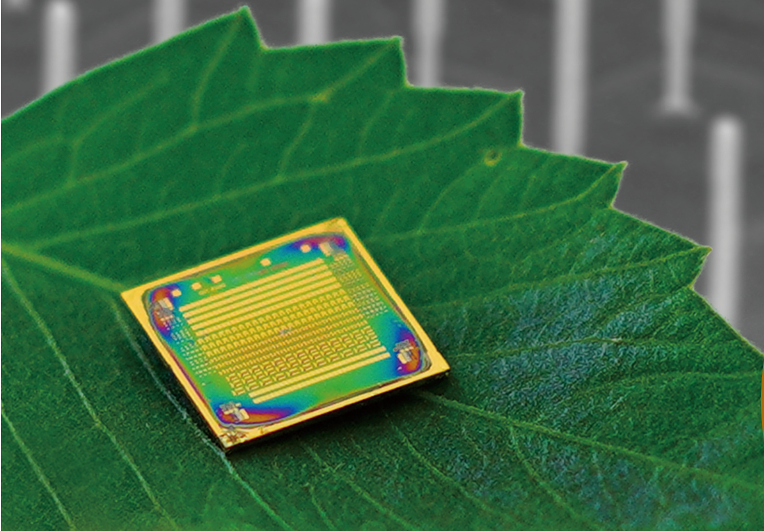

Vertical III-V Nanowire Transistors for Low-Power Logic and Reconfigurable Applications

Doctoral Thesis

Zhongyunshen Zhu

LUND
UNIVERSITY

Department of Electrical and
Information Technology
Lund, October 2023

Academic thesis for the degree of Doctor of Philosophy, which, by due permission of the Faculty of Engineering at Lund University, will be publicly defended on Friday, 13 October, 2023, at 9:15 a.m. in lecture hall E:1406, Department of Electrical and Information Technology, Ole Römers Väg 3, 223 63 Lund, Sweden. The thesis will be defended in English.

The Faculty Opponent will be Professor *Kirsten Moselund*, from *Paul Scherrer Institute* and *EPFL*.

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Vertical III-V Nanowire Transistors for Low-Power Logic and Reconfigurable Applications

Abstract:
With rapid increase in energy consumption of electronics used in our daily life, the building blocks — transistors — need to work in a way that has high energy efficiency and functional density to meet the demand of further scaling. III-V channel combined with vertical nanowire gate-all-around (GAA) device architecture is a promising alternative to conventional Si transistors due to its excellent electrical properties in the channel and electrostatic control across the gate oxide in addition to reduced footprint. Based on this platform, two major objectives of this thesis are included: 1) to improve the performance of III-V p-type metal-oxide-semiconductor field-effect transistors (MOSFETs) and tunnel FETs (TFETs) for low-power digital applications; 2) to integrate HfO_2-based ferroelectric gate onto III-V FETs (FeFETs) and TFETs (ferro-TFETs) to enable reconfigurable operation for high functional density.

The key bottleneck for all-III-V CMOS is its p-type MOSFETs (p-FETs) which are mainly made of GaSb or InGaSb. Rich surface states of III-Sb materials not only lead to decreased effective channel mobility due to more scattering, but also deteriorate the electrostatics. In this thesis, several approaches to improve p-FET performance have been explored. One strategy is to enhance the hole mobility by introducing compressive strain into III-Sb channel. For the first time, a high and uniform compressive strain near 1% along the transport direction has been achieved in downscaled GaSb nanowires by growing and engineering GaSb-GaAsSb core-shell structure, aiming for potential hole mobility enhancement. In addition, surface passivation using digital etch has been developed to improve the electrostatics with subthreshold swing (SS) down to 107 mV/dec. Moreover, the on-state performance including on-current (I_{on}) and transconductance (g_m) have been enhanced by ~50% using annealing with H_2-based forming gas. Lastly, a novel p-FET structure with (In)GaAsSb channel has been developed and further improved off-state performance with SS = 71 mV/dec, which is the lowest value among all reported III-V p-FETs.

Despite subthermionic operation, TFETs usually suffer from low drive current as well as the current operating below 60 mV/dec (I_{60}). The second focus of this thesis is to fine-tune the InAs/(In)GaAsSb heterostructure tunnel junction and the doping in the source segment during epitaxy. As a result, a substantially increased I_{60} (> 1 μA/μm) and I_{on} up to 40 μA/μm at source-drain bias of 0.5 V have been achieved, reaching a record compared to other reported TFETs.

Finally, emerging ferroelectric oxide based on Zr-doped HfO_2 (HZO) has been successfully integrated onto III-V vertical nanowire transistors to form FeFETs and ferro-TFETs with GAA architecture. The corresponding electrical performance and reliability have been carefully characterized with both DC and pulsed *I-V* measurements. The unique band-to-band tunneling in InAs/(In)GaAsSb/GaSb heterostructure TFET creates an ultrashort effective channel, leading to detection of localized potential variation induced by single domains and defects in nanoscale ferroelectric HZO without physical gate-length scaling. By introducing gate/source overlap structure in the ferro-TFET, non-volatile reconfigurable signal modulation with multiple modes including signal transmission, phase shift, frequency doubling, and mixing has been achieved in a single device with low drive voltage and only ~0.01 μm^2 footprint, thus increasing both functional density and energy efficiency.

Keywords:
III-V Nanowires, MOSFET, TFET, Ferroelectrics, Reconfigurable.

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Department of Electrical and
Information Technology
Lund, October 2023

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Frontispiece: A semiconductor chip made from nanowire transistors rests on a leaf.

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Abstract

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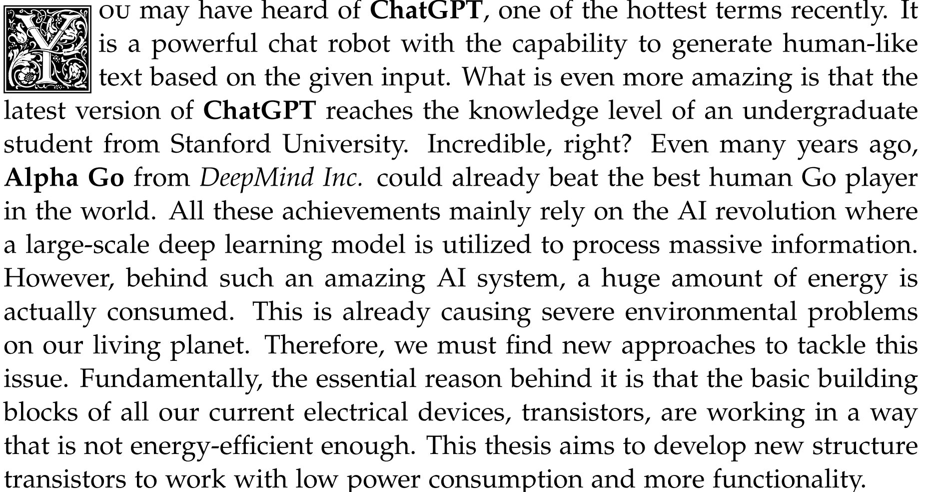
Popular Science Summary



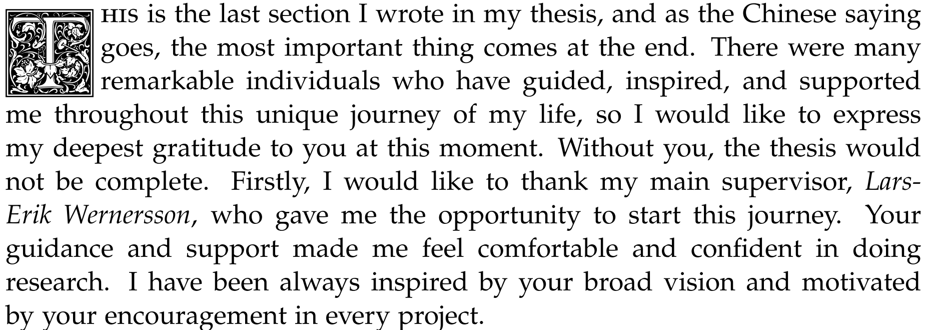
You may have heard of **ChatGPT**, one of the hottest terms recently. It is a powerful chat robot with the capability to generate human-like text based on the given input. What is even more amazing is that the latest version of **ChatGPT** reaches the knowledge level of an undergraduate student from Stanford University. Incredible, right? Even many years ago, **Alpha Go** from *DeepMind Inc.* could already beat the best human Go player in the world. All these achievements mainly rely on the AI revolution where a large-scale deep learning model is utilized to process massive information. However, behind such an amazing AI system, a huge amount of energy is actually consumed. This is already causing severe environmental problems on our living planet. Therefore, we must find new approaches to tackle this issue. Fundamentally, the essential reason behind it is that the basic building blocks of all our current electrical devices, transistors, are working in a way that is not energy-efficient enough. This thesis aims to develop new structure transistors to work with low power consumption and more functionality.

The transistors are essentially a switch that can be turned on and off by an electrode called gate. It is pretty like the water-tap (gate) which controls whether the water flowing (current flow in transistors) out or not. The on- and off-state of the transistor are encoded as binary data of "0" and "1", respectively. When putting millions or even billions of transistors (e.g. A16 chip in iPhone 14 contains 16 billion transistors) together in a specific way, they can do extremely complicated computations that are almost impossible for the human brain. To package such a dense system, transistors need to be very tiny, which can reach around 10 nm regime, a size about 5000

times thinner than human hair. Unfortunately, the leakage current when you switch off the transistor increases with the size downscaling, leading to a large amount of energy wasted. This will also heat up the system, which then significantly affects the performance.

In this thesis, we attempt to develop transistors with new structures that can operate at low power conditions. We basically combine three aspects to realize this. First, a vertical nanowire is used to reduce the footprint yet bring the transistor size scaling to the vertical direction. In this 3D architecture, you can expect a larger transistor out of the plane but remaining a small planar area. Therefore, the leakage can be well suppressed while a high package density can be still achieved. Second, we change the transistor material from silicon to III-V compound semiconductors which are alloys of group-III and V elements in the periodic table. These materials show better electrical performance compared to silicon. Therefore, lower supplied voltage can be used to achieve the same performance as silicon transistors which dominate in most electronics. Based on these two points, combining lower leakage current and supplied voltage results in lower power consumption. Moreover, we have taken one step forward to add more functionality into one transistor so that it can do the work that several transistors used to do (just imagine that you have a fancy multi-level adjustable showerhead). This is achieved by integrating new materials called ferroelectrics onto our III-V vertical nanowire transistors. As a result, either the number of transistors is reduced but with the same functions, or more functions are realized but with the same number of transistors. Thus, the power consumption can be lowered without compromising the performance. We believe that our study on such a transistor structure will trigger more potential applications for systems requiring energy efficiency, such as AI chips and IoT devices.

Acknowledgments



THIS is the last section I wrote in my thesis, and as the Chinese saying goes, the most important thing comes at the end. There were many remarkable individuals who have guided, inspired, and supported me throughout this unique journey of my life, so I would like to express my deepest gratitude to you at this moment. Without you, the thesis would not be complete. Firstly, I would like to thank my main supervisor, *Lars-Erik Wernersson*, who gave me the opportunity to start this journey. Your guidance and support made me feel comfortable and confident in doing research. I have been always inspired by your broad vision and motivated by your encouragement in every project.

I also want to thank my second supervisor, *Johannes Svensson*. Thank you for leading me to the lab and teaching me the growth hand by hand. I appreciate very much that you always said "Yes" when I asked you "Do you have time to discuss?" and patiently answered my sometimes even stupid questions. You are definitely more than only a supervisor to me.

A big thanks to those who gave me special help and inspiration during my PhD research. Thank you, *Anton Persson*, I enjoyed a lot with you for fantastic exploration of the first ferroelectric transistors here in Lund. Thank you, *Gautham Rangasamy* and *Abinaya Krishnaraja*, those great discussions made me learn a lot about TFETs. *Adam Jönsson*, thank you for introducing me to the vertical processing step by step. *Robin Atle*, thank you for your incredible assistance in making beautiful FIB images of the nanowires. Thank you, *Erik Lind*, for your great discussions about TFET physics and constructive inputs in the first ferro-TFET paper.

I would also like to extend my gratitude to all the remarkable colleagues within the division who made the work environment not only vibrant but also relaxing with full of fun. I will never forget the moments we spent

together from lab to office, from fika to innebandy. So a great thanks goes to you, *Marcus, Saketh, Phillipp, André, Hannes, Karthik, Ben, Ngoc Duc, Heera, Lars, Mattias, Anette, Navya, Patrik, Louise, Lasse, Markus, Fredrik, Karl-Magnus, Stefan, Sebastian, Olli-Pekka, Paula, Niklas, Daniel, Mats, Johan, Andrea*, and *Alexandros*. A special thanks to *André, Gautham*, and *Guoda* for proofreading of this thesis. Beyond the department, I want to thank *Yen-Po* and *Rainer* from the Physics Department, and *Axel* from the Chemistry Department for providing excellent material characterizations in our collaborations.

Furthermore, I want to thank all the engineers and technicians in both *NanoLund* and *EIT* lab. My thesis wouldn't be possible to be completed without your tremendous help. A special thank you to *Sebastian Lehmann* and *Sungyoun Ju* for your professional maintenance of the growth machine so that I could grow samples in an expected way.

I thank all my friends in Sweden and in China. You made my life far from boring. Thank you, *Guoda*, for your generous assistance in our several relocations and for playing Pingpong with me after work. Thank you, *Shang*, for having wonderful experiences together over the years and I believe there will be more to come.

Finally, I would like to thank my family for your unconditional love and forever support in my entire life. My deepest appreciation goes to *Yuyu*, who has been always supportive and understanding throughout this journey. Your patience and wisdom in life have influenced me to be a better person. Living thousands of miles away from my hometown and family is not easy, but you make me feel at home wherever I am.

Lund, Sept. 2023

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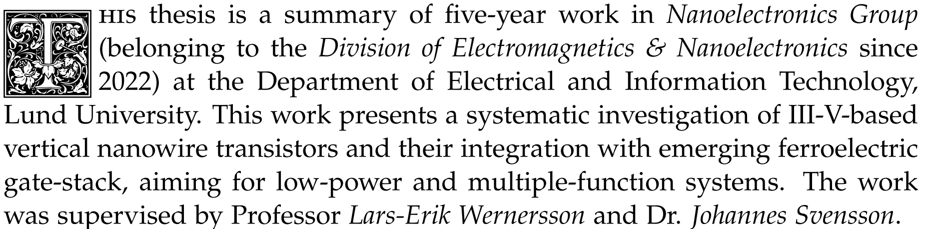
Preface


THIS thesis is a summary of five-year work in *Nanoelectronics Group* (belonging to the *Division of Electromagnetics & Nanoelectronics* since 2022) at the Department of Electrical and Information Technology, Lund University. This work presents a systematic investigation of III-V-based vertical nanowire transistors and their integration with emerging ferroelectric gate-stack, aiming for low-power and multiple-function systems. The work was supervised by Professor *Lars-Erik Wernersson* and Dr. *Johannes Svensson*.

STRUCTURE OF THE THESIS

This is a thesis with a collection of research papers, including an introductory section providing a summary of the research field. The appended publications together with the introduction are comprehensible for aspiring researchers with a master's degree interested in pursuing similar research topics.

- **INTRODUCTION**
  The Introduction provides a broad and comprehensive view of the included publications and combines related work together. The Introduction is intended to be comprehensible for aspiring readers with a Master's degree in physics, electrical engineering, or a related subject.

- **APPENDICES**
  - **A Nanowire Epitaxy Recipes**
    Appendix A provides details of nanowire growth procedures by MOVPE.
  - **B Fabrication Steps of Vertical Nanowire Transistors**
    Appendix B provides detailed steps of vertical device fabrication included in this thesis.

- **PAPERS**
  The papers forming the main body of the thesis are reproduced in the back and listed in the following.

INCLUDED PAPERS

The following published papers form the main body of this thesis and are appended at the back of the thesis.

Paper I: Z. ZHU, J. SVENSSON, A. R. PERSSON, R. WALLENBERG, A. V. GROMOV, AND L.-E. WERNERSSON, "Compressively-strained GaSb nanowires with core-shell heterostructures", *Nano Research*, vol. 13, no. 9, pp. 2517–2524, Jun. 2020, doi: 10.1007/s12274-020-2889-3.

▶ *I performed the nanowire growth, sample preparation for TEM and μ-Raman characterizations, data analysis, and wrote the paper.*

Paper II: Z. ZHU, A. JÖNSSON, Y.-P. LIU, J. SVENSSON, R. TIMM, AND L.-E. WERNERSSON, "Improved Electrostatics through Digital Etch Schemes in Vertical GaSb Nanowire p-MOSFETs on Si", *ACS Applied Electronic Materials*, vol. 4, no. 1, pp. 531–538, Jan. 2022, doi: 10.1021/acsaelm.1c01134.

▶ *I performed the nanowire growth, part of sample fabrication, part of electrical measurements, and wrote the paper.*

Paper III: Z. ZHU, J. SVENSSON, A. JÖNSSON, AND L.-E. WERNERSSON, "Performance enhancement of GaSb vertical nanowire p-type MOSFETs on Si by rapid thermal annealing", *Nanotechnology*, vol. 33, no. 7, pp. 075202, Nov. 2021, doi: 10.1088/1361-6528/ac3689.

▶ *I performed the nanowire growth, sample fabrication, part of electrical measurements, and wrote the paper.*

Paper IV: A. E. O. PERSSON, Z. ZHU, AND L.-E. WERNERSSON, "Integration of Ferroelectric $Hf_xZr_{1-x}O_2$ on Vertical III-V Nanowire Gate-All-Around FETs on Silicon", *IEEE Electron Device Letters*, vol. 43, no. 6, pp. 854–857, Jun. 2022, doi: 10.1109/LED.2022.3171597.

▶ *I performed the nanowire growth, part of sample fabrication, and part of electrical measurements.*

Paper V: Z. ZHU, A. E. O. PERSSON, AND L.-E. WERNERSSON, "Sensing single domains and individual defects in scaled ferroelectrics", *Science Advances*, vol. 9, no. 5, pp. eade7098, Feb. 2023, doi: 10.1126/sciadv.ade7098.

▶ *I performed the nanowire growth, part of sample fabrication, part of electrical measurements, and wrote the paper.*

Paper VI: Z. ZHU, A. E. O. PERSSON, AND L.-E. WERNERSSON, "Reconfigurable Signal Modulation in a Ferroelectric Tunnel Field-Effect Transistor.", *Nature Communications*, vol. 14, no. 1, pp. 2530, May. 2023, doi: 10.1038/s41467-023-38242-w.

▶ *I performed the nanowire growth, part of sample fabrication, part of electrical measurements, and wrote the paper.*

Paper VII: A. KRISHNARAJA, Z. ZHU, J. SVENSSON, AND L.-E. WERNERSSON, "Low-power, Self-aligned Vertical InGaAsSb NW PMOS with S < 100 mV/dec.", *IEEE Electron Device Letters*, vol. 44, no. 7, pp. 1064–1067, Jul. 2023, doi: 10.1109/LED.2023.3277917.

▶ *I partly designed the device structure and performed the nanowire growth.*

Paper VIII: G. RANGASAMY, Z. ZHU, AND L.-E. WERNERSSON, "High Current Density Vertical Nanowire TFETs with $I_{60} > 1\ \mu A/\mu m$.", *IEEE Access*, vol. 11, pp. 95692–95696, Aug. 2023, doi: 10.1109/ACCESS.2023.3310253.

▶ *I partly designed the device structure and performed the nanowire growth and modeling.*

RELATED WORK

The following publications and manuscripts in preparation are not included in this thesis, but summarize related work that I was involved in.

Paper ix: G. RANGASAMY, Z. ZHU, L. O. FHAGER, AND L.-E. WERNERSSON, "TFET Circuit Configurations Operating Below 60 mV/dec", *IEEE Transactions on Nanotechnology*, (2022, Under Review)

Paper x: G. RANGASAMY, Z. ZHU, L. O. FHAGER, AND L.-E. WERNERSSON, "g_m/I_d Analysis of Vertical Nanowire III–V TFETs", *Electronics Letters*, (Sept. 2023, accepted)

Paper xi: A. KRISHNARAJA, J. SVENSSON, E. MEMISEVIC, Z. ZHU, A. R. PERSSON, E. LIND, L. R. WALLENBERG, AND L.-E. WERNERSSON, "Tuning of source material for InAs/InGaAsSb/GaSb application-specific vertical nanowire tunnel FETs", *ACS Applied Electronic Materials*, vol. 2, no. 9, pp. 2882–2887, Sep. 2020, doi: 10.1021/acsaelm.0c00521.

Paper xii: A. Krishnaraja, J. Svensson, Z. Zhu, and L.-E. Wernersson, "Tunnel Field-Effect Transistor Operation at Different Temperature Regimes", *Applied Physics Letters*, (2023, In Revision)

Paper xiii: D. Dzhigaevc, J. Svensson, A. Krishnaraja, Z. Zhu, Z. Ren, Y. Liu, S. Kalbfleisch, A. Björling, F. Lenrick, Z. I. Balogh, S. Hammarberg, J. Wallentin, R. Timm, L.-E. Wernersson, and A. Mikkelsen, "Strain mapping inside an individual processed vertical nanowire transistor using scanning X-ray nanodiffraction", *Nanoscale*, vol. 12, no. 27, pp. 14487–14493, Jun. 2020, doi: 10.1039/D0NR02260H.

Acronyms and Symbols

Here, important acronyms, abbreviations, and symbols are listed, which are recurring throughout the thesis. Some parameters, which only occur in a narrow context, are intentionally omitted; some parameters are used in more than one way, but the context is always explicitly clarified in the corresponding text. Some (compound) units are provided with prefixes to reflect the most commonly encountered notations in the literature.

ACRONYMS AND ABBREVIATIONS

3D Three Dimensional
5G Fifth-Generation Technology Standard for Broadband Cellular Networks

AC Alternating Current
AI Artificial Intelligence
ALD Atomic Layer Deposition

BEOL Back-End-of-Line
BOE Buffered Oxide Etchant
BTBT Band-to-Band Tunneling

CMOS Complementary Metal-Oxide-Semiconductor

DC Direct Current
DE Digital Etch
DI Deionized

EBL	Electron-Beam Lithography
FeFET	Ferroelectric Field-Effect Transistor
FEOL	Front-End-of-Line
GAA	Gate-All-Around
IC	Integrated circuit
ICP	Inductively Coupled Plasma
IoT	Internet-of-Things
IPA	Isopropyl Alcohol
MFS	Metal-Ferroelectric-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MOVPE	Metal-Organic Vapor-Phase Epitaxy
MW	Memory Window
NAND	Not And
NDR	Negative Differential Resistance
NTC	Negative Transconductance
PUND	Positive-Up Negative-Down
RIE	Reactive-Ion Etch
RRAM	Resistive Random-Access Memory
RTA	Rapid Thermal Annealing
SEM	Scanning Electron Microscopy
TEM	Transmission Electron Microscopy
UV	Ultraviolet
WZ	Wurtzite
XEDS	Energy-dispersive X-ray spectroscopy
XPS	X-ray Photoelectron Spectroscopy
XRD	X-Ray Diffraction
ZB	Zink-Blende

LATIN SYMBOLS

Al_2O_3		Aluminium Oxide
AsH_3		Arsine
C_{ox}	F/m	Gate Oxide Capacitance
d	m	Nanowire Diameter, subscript indicates the specific object
D_{it}	$eV^{-1}cm^{-2}$	Interface Trap Density
E_g	eV	Band Gap
E_C	eV	Conduction Band Edge
$E_{F,D}$	eV	Fermi Level Energy at the Drain
$E_{F,S}$	eV	Fermi Level Energy at the Source
E_V	eV	Valence Band Edge
f	Hz	Frequency, subscript indicates the specific case
GaAsSb		Gallium Arsenide Antimonide
GaSb		Gallium Antimonide
g_m	S, $\mu S\,\mu m^{-1}$	Transconductance, often normalised by the gate width
$g_{m,peak}$	S, $\mu S\,\mu m^{-1}$	Peak Transconductance, often normalised by the gate width
HfO_2		Hafnium Oxide
HZO		Hafnium Zirconium Oxide (Zirconium-doped Hafnium Oxide)
I_D	A, $\mu A\,\mu m^{-1}$	Drain Current, often normalised by the gate width
I_{off}	A, $\mu A\,\mu m^{-1}$	Off-Current, often normalised by the gate width
I_{on}	A, $\mu A\,\mu m^{-1}$	On-Current, often normalised by the gate width
InAs		Indium Arsenide
InAsSb		Indium Arsenide Antimonide
InGaAsSb		Indium Gallium Arsenide Antimonide
k_B		$\approx 1.381 \times 10^{-23}$ kg m^2 K^{-1} s^{-1}, Boltzmann Constant
L_g	m	Gate Length

m_0	kg	$\approx 9.109 \times 10^{-31}$ kg, Electron Rest Mass
m^*	m_0	Effective Mass
q	C	$\approx 1.602 \times 10^{-19}$ C, Elemental Charge
R_{on}	$\Omega\,\mu$m	On Resistance, often normalised by the gate width
SS	mV/dec	Subthreshold Swing
t	s	Time, subscript indicates the specific case
T	K, °C	Temperature
V_D	V	Drain Bias
V_{DS}	V	Drain-to-Source Voltage
V_G	V	Gate Bias, here equivalent to Gate-to-Source Voltage (V_{GS})
V_{OV}	V	Overdrive Voltage, $V_G - V_T$
V_S	V	Source Bias
V_T	V	Threshold Voltage

GREEK SYMBOLS

α	eV^{-1}	Exponential Coefficient Associated with the Material Properties
κ		Relative Permittivity
φ_S	V	Surface Potential
$\tau_{e/c}$	s	Time constant of single electron emission/capture (e/c)

INTRODUCTION

1 Background

"Opposites are not contradictory but complementary."

— Niels Bohr

transistor is a device in which the conduction between two electrodes can be controlled by its third electrode. Since this unique device was first invented in 1947 at Bell Laboratories, the era of semiconductor electronics has been opened and has remarkably changed our daily life. According to the Semiconductor Industry Association (SIA), sales in the global semiconductor industry reached $574.1 billion in 2022, marking the highest annual total to date and a 3.3% increase from 2021 [1] due to the continuously strong demand in the market particularly in consumer electronics and electrical vehicles driven by emerging technologies mainly including IoT, cloud computing, 5G network, and AI. When amazed by the capability of modern electronics, a huge amount of power consumed by data computing and storage has become a big concern in industry. For instance, over the past few years, the energy consumption in large data centers has been on the rise, increasing by 10-30% annually, due to the significant increase in workloads being processed [2]. Therefore, many measures including optimizing the thermal management and hardware architecture have been taken to improve the energy efficiency. As the essential building block for microelectronics, the development of a single transistor with improved performance and reduced power consumption is crucial to directly impact circuits and further systems. In fact, back to 1980s, with the same regard on the power consumption, Si bipolar transistors which used to be the mainstream in the early stage of

integrated circuits (ICs) were replaced by CMOS technology where both n-type and p-type MOSFET are connected in a certain way. In the following decades, MOSFETs have dominated the digital circuits and enabled very large-scale integrated (VLSI) circuits owing to their high scalability and energy efficiency.

In this chapter, we will generally go through the basic history of MOSFET architectures, the potential and challenges for III-V transistors and their integration with emerging technologies. The key motivation and contribution of this thesis will be briefly addressed. We mainly discuss MOSFETs in the entire thesis when mentioning transistors without specification.

1.1 TRANSISTOR ARCHITECTURE: PAST, PRESENT, AND FUTURE

Dennard's scaling indicates that shrinking transistor size allows high density package in the same chip area and lowers the operating voltage, thereby reducing power consumption and the cost per transistor [3]. By consuming less energy per switching event per transistor, it is possible to fit more logic gates into the IC, resulting in faster switching speed while keeping the same power budget.

In 1965, the founder of Intel, Gordon Moore, predicted that the transistor density would be doubled every 2 years based on the aggressive scaling of the geometry. This so-called Moore's law was proved to exactly fit the industrial roadmap of transistor scaling in planar MOSFETs whose structure is presented in Fig 1.1a. In such a device, a planar channel along with a high-permittivity (high-κ) dielectric and metal gate is used to control the current flow injected from the source to the drain which is typically highly doped. However, when miniaturizing towards 22 nm or downward, the electrostatics over the MOS structure degrades dramatically, deteriorating the switching behavior and skyrocketing the power dissipation. This led to inhibition in further gate-length downscaling. The invention of FinFET saved the continuation of Moore's law by using a fin as the channel with a tri-gate to improve the electrostatic control of the transistor (Fig. 1.1b). This architecture is still used in most of electronics requiring advanced technology nodes, including CPUs in laptops and smart phones. Figure 1.2 shows the excellent extension of Moore's law and reduced switching energy with FinFET architecture. Gate-all-around (GAA) geometry with a wrapped gate surrounding the channel is regarded to give the best electrostatics for the transistor. Nanosheets with LGAA structure (Fig. 1.1c) has been demonstrated for the next technology node beyond 3 nm (Fig. 1.2). By vertically stacking multiple layers of nanosheets, the transistor performance can be enhanced [4]. The same architecture can be extrapolated to complementary FETs (CFETs)

with vertically stacking both n- and p-type MOSFETs (Fig. 1.1d), which have been demonstrated experimentally [5] for 3D IC. In accordance with IEEE International Roadmap for Device and Systems (IRDS) 2022 [6], the CFET structure can possibly extend Moore's law to 0.5-nm equivalent technology node in 2037, leading to attojoule switching energy per transistor as indicated in Fig. 1.2. Compared to lateral FETs, further scaling of footprint can be achieved in vertical GAA (VGAA) nanowire/nanosheet FET (Fig. 1.1e) which allows independent optimization of gate-length and spacer width to possibly minimize the device area [7].

1.2 III-V SEMICONDUCTOR: OPPORTUNITY AND CHALLENGE

In MOSFETs, high carrier mobility in the channel is desirable to increase the current at the drain side (I_D) and a higher I_D results in a higher operating frequency. III-V compound semiconductors (an alloy with group-III and group-IV elements) are one of the potential candidates that may replace Si as the channel of MOSFETs due to their superior electrical properties (see Table 1.1) such as high mobility and injection velocity [9]. Given this III-Vs have been widely explored in high frequency applications. For instance, GaAs-based heterojunction bipolar transistors (HBTs) have been already commercially available for power amplifiers in wireless communications [10] and InAs-based high electron mobility transistors (HEMTs) have reached a cutoff frequency up to 628 GHz [11]. Furthermore, with the rapid revolution in quantum computers using superconducting or spin qubits as the quantum circuits, III-V-based MOSFETs [12] and HEMTs [13] have also shown tremendous attraction with fast switching for peripheral modules of signal readout at cryogenic temperatures.

In digital applications, it is difficult to take the most advantage of both electron and hole mobility in a single III-V material, leading to challenges in competing with Si CMOS. Nevertheless, as noted in Table 1.1, InAs and GaSb are almost lattice-matched and have the highest electron and hole mobility, respectively. Many efforts have been made to co-integrate InAs n-MOSFET (n-FET) and GaSb p-MOSFET (p-FET) for CMOS logic gates. So far, various device architectures including planar InAs/GaSb on Si box [14], LGAA nanowires [15], VGAA monolithic InAs/GaSb co-integration [16, 17] have been reported. Although arsenide-based n-FETs can well outperform their Si counterparts, antimonide-based p-FETs are still far below the expectation, resulting in unmatched performance. There are two major challenges constraining the development of high-performance antimonide-based p-FETs. First, ohmic contact with low resistance is still lacking for antimonides, which hinders further enhancement of the drive current in the on-state. Some recent

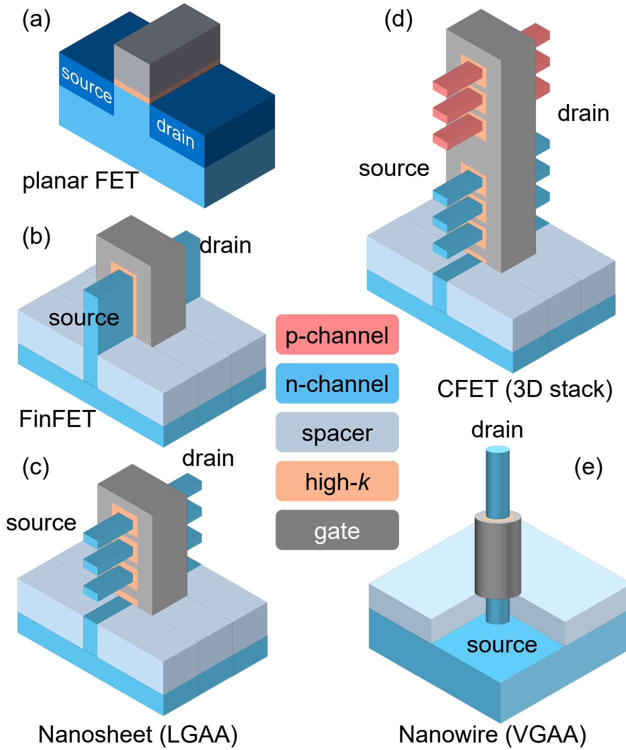


Figure 1.1: Evolution of MOSFET architecture with footprint scaling. (a) Planar high-κ metal-gate (HKMG) MOSFET. The dielectric with high permittivity such as HfO_2 combined with metal gate electrode is used for improving the electrostatic control beyond SiO_2/poly-Si gate-stack. (b) FinFET has been utilized beyond 22-nm node and has boosted the transistor performance. A tri-gate is used for retaining electrostatics with gate-length scaling. (c) LGAA configuration with nanosheets is considered as the device architecture of the technology nodes beyond 5 nm to improve the electrostatic confinement. (d) Continuous scaling for higher transistor density, CFETs with 3D stack of n- and p-type nanosheet FETs can be used. (e) VGAA nanowire FETs can further scale the pitch between gates which is a limit of lateral FETs. This VGAA architecture may continue the Moore's law beyond 2040.

efforts such as capping III-Sb with p-type InAsSb thin layer [18] and alloying Ni into antimonide source and drain by annealing [19] have been investigated to improve the contact resistance. Second, high-quality high-κ oxide/III-Sb interface is lacking. As seen in Table 1.1, a high interface trap density typically exists in GaSb due to rich oxide states at the surface [20], causing

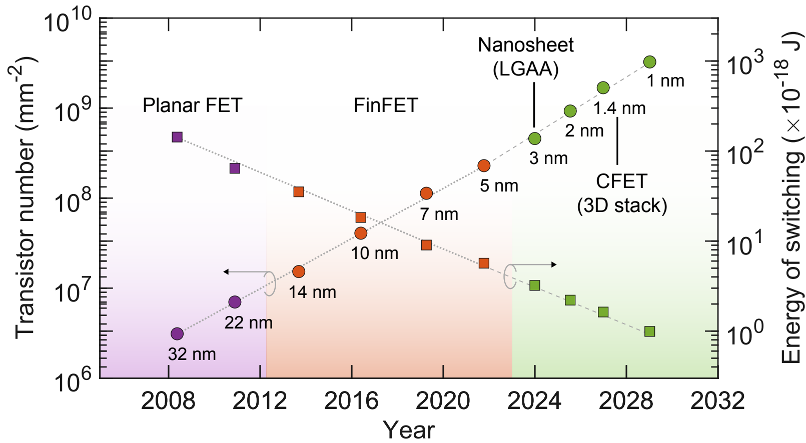


Figure 1.2: MOSFET scaling can still follow Moore's law nicely with future hyper scaling technologies. The energy of per switching per transistor can be further reduced towards atto-joule regime. Data are from Ref. [8].

a detrimental electrostatic control for MOSFETs. As a result, the effective hole mobility in GaSb MOSFETs is only one tenth ($\sim$100 cm^2/Vs) [21] of its bulk value (Table 1.1). In scaled nanowire MOSFETs, higher surface-volume ratio could introduce more surface scattering to the channel, leading to even lower mobility ($\sim$70 cm^2/Vs) [22]. This limits the switching behavior when further downscaling the device. Recently, an unconventional approach using template-assisted selective epitaxy, a high hall-effect hole mobility of $\sim$760 cm^2/Vs has been achieved in an ultra-scaled dimension down to 20 nm [23], close to the bulk value although no MOSFETs have been fabricated.

In line with the goal of energy efficiency, novel device concepts beyond CMOS technology have been investigated recently. Steep-slope transistors are a promising device variant that allows transistors to switch on/off using a voltage swing below the physical limit of conventional MOSFETs. TFETs whose transport mechanism relies on band-to-band tunneling (BTBT) are one of these steep-slope devices [26, 27], aiming for low-power circuits and systems such as IoT and biosensors. Among many semiconductors, III-V heterostructures stand out for this type of devices due to their rich alloy combinations in optimization of band alignment for tunnel junction [28, 29], thereby being additional opportunity for future III-V based electronics.

Table 1.1: Comparison of Si and common III-V materials with various parameters at 300 K: lattice constant (a_0), electron (μ_e) and hole mobility (μ_h), interface trap density (D_{it}), and thermal conductivity (k_{th}, data from Ref. [24]). Lattice and mobility data are from Ref. [25].

material	a_0 (Å)	μ_e (cm^2/Vs)	μ_h (cm^2/Vs)	D_{it} level[a] (eV/cm^2)	k_{th} (W/mK)
Si	5.43	1400	450	$\sim 10^{10}$	145
GaAs	5.65	8500	400	$\sim 10^{12}$	44
InAs	6.06	13000	500	$\sim 10^{12}$	27
GaSb	6.09	3000	1000	$\sim 10^{13}$	33

[a] Typical order of magnitude regardless interface treatment.

1.3 HETEROGENEOUS INTEGRATION

By following the geometrical scaling (shrinking size) and the equivalent scaling (strained Si, HKMG, and non-planar FETs), advanced electronics will enter a hyper-scaling era through future innovations at different levels including from materials and devices to systems [30], enabling possible avenue to continue Moore's law beyond the physical dimension of a single transistor.

One of the key approaches is heterogeneous integration where various technological platforms are assembled in a dense way to realize diverse functionalities while keeping the total area. At the system level, multi-die integration technology (Fig. 1.3a) offers a possible way to interconnect different function chips on one platform rather than separately packaging them, enabling a low-cost, low-power, and low-latency system [31]. To further increase the package density as well as to maximize the performance of different technologies (e.g. Si CMOS for logic while III-V HEMTs for RF component) on a one IC wafer, 3D vertically stacked integration (Fig. 1.3b) has been proposed and demonstrated using bonding technique which can mitigate the monolithic integration of III-V on Si due to the large mismatch in lattice constant and thermal expansion (see a_0 and k_{th} in Table 1.1) [32].

At the device level, integration of memory cells directly into a computing device (e.g. MOSFET) has been under intensive investigation for brain-inspired or in-memory computation due to the high potential to break through the bottle-neck of conventional von Neumann architectures which physically separate the computing and memory chips thus being latency- and energy-inefficient. Depending on the practical purpose and the technical approach, there are typically two integration schemes of memory cells on a

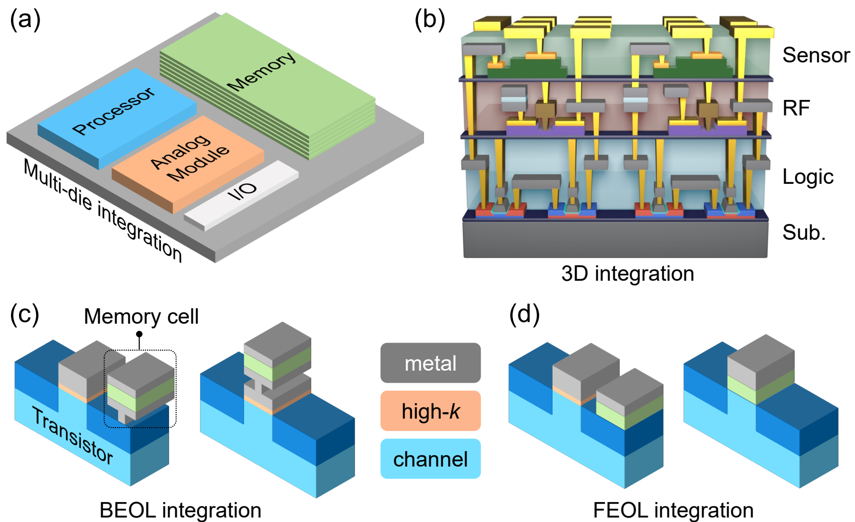


Figure 1.3: Schematics of potential heterogeneous integration at different levels. (a) A multi-die system with all die-to-die interconnections on the same package wafer. (b) 3D IC integration of different function dies in a vertical direction, thus shrinking the package area. Device-level in-memory computing unit with (c) BEOL and (d) FEOL integration.

transistor: on the drain or on the gate. Moreover, the memory cell can be integrated after the computing devices (e.g. CMOS) are fabricated (BEOL, see Fig. 1.3c) or directly integrated during the computing device fabrication process (FEOL, see Fig. 1.3d). Recently, the rapid development of non-volatile memories based on diverse materials such as ferroelectrics, resistive oxides, and phase-change materials has boosted the research of in-memory computing [30].

An energy- and area-efficient hardware architecture for artificial neural networks (ANN) is crossbar arrays with massive multiply-and-accumulate (MAC) operations in parallel, enabling high-speed matrix-based computations. In this regard, a VGAA device structure with both logic and memory in one nanowire is preferred to achieve the theoretical minimum feature size of one cell. Given this a high-density VGAA-nanowire-based device has been recently reported by using a nanowire transistor as a selector to activate the FEOL-integrated RRAM cell and an NAND logic gate has also been implemented in the same structure, thereby realizing in-memory computing [33]. Specifically, part of this thesis aims for integrating HfO_2-based ferroelectric gate-stack onto a III-V nanowire platform (Paper IV, V &

VI) to add reconfigurability into conventional transistors, thus realizing high functional diversity in a single device.

2

Transistor Fundamentals

HE general work principles and key concerns of III-V vertical nanowire MOSFET, TFETs, and FeFETs will be discussed in this chapter. Note that a detailed discussion of ferroelectric material and device physics is out of the scope of this thesis.

2.1 BASICS OF MOSFETS AND TFETS

In a n-type MOSFET as shown in Fig. 2.1a, the source and drain are highly n-type doped with a Fermi level ($E_{F,S}$ or $E_{F,D}$) close or higher than the conduction band edge (E_C), leading to high electron concentration (obeying Fermi-Dirac distribution, $f(E)$). A source-drain bias (V_{DS}) is applied to create an electrical field for electrons to flow from the source to the drain. The channel between the source and drain is like the traffic lights which allow (on-state, $V_G > V_T$) or block (off-state, $V_G < V_T$) the electron flow by setting the height of the energy barrier through a gate voltage (V_G) across the MOS structure. In the case of p-FETs, the source and drain are p-type doped, thus the corresponding E_F close to the valence band edge (E_V). For III-V materials, group IV elements such as C, Si, and Sn are commonly used as the dopant since they can be either donors (n-type) or acceptors (p-type) depending on which site (group-III or group-V) in the crystal is replaced [34].

Unlike MOSFETs where charge carriers are thermally injected over a barrier, interband tunneling, or BTBT, is the primary injection mechanism in TFETs in which a gated p-i-n structure typically exists (Fig. 2.1b). By controlling the band bending in the unintentionally doped channel via V_G, TFETs can be switched on and off abruptly. In the off-state of a n-type TFET (Fig. 2.1b), the $E_{F,S}$ is located below the channel E_C, and thus BTBT is suppressed, resulting

in a low off-state current (I_{off}). In the on-state when applying a larger V_G, the E_C in the channel is pulled down to the position below the source E_V so that many vacancies above the channel E_C are available for electrons to tunnel, leading to strong BTBT and increased tunneling current.

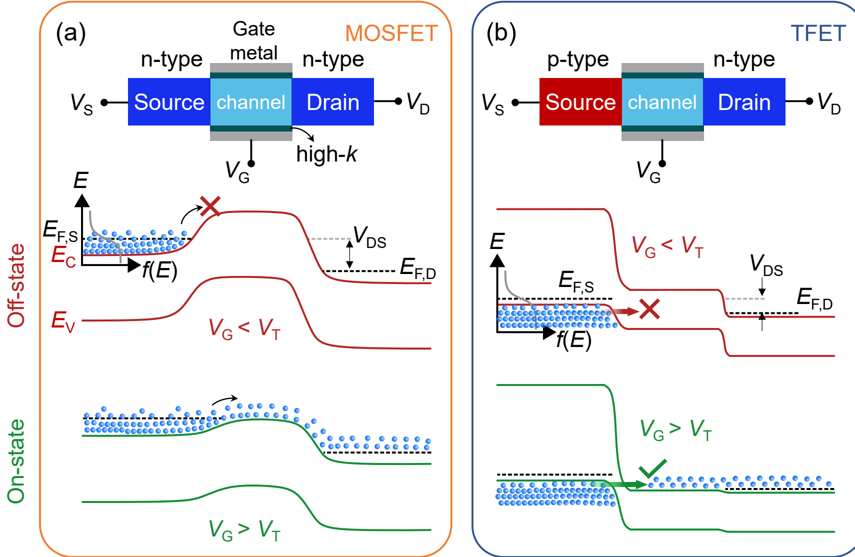


Figure 2.1: Basic mechanism from the perspective of band diagram in (a) MOSFETs and (b) TFETs. The main difference between the two device structures is that only one type of doping (either n- or p-type) is needed for source and drain in MOSFETs while a p-i-n structure is conventionally used for TFETs. In the off-state of MOSFETs, E_C of the channel is much lower than $E_{F,S}$, so the electrons barely cross the barrier to the drain; in the on-state, the energy barrier is lower enough and $E_{F,S}$ is above the channel E_C so that electrons can freely flow to the drain. In the case of TFETs, electrons can tunnel from the source to the channel through the tunneling barrier only when the channel E_C is lower than $E_{F,S}$. The schematics denote the ideal cross-section of GAA nanowire transistors.

2.1.1 METRICS OF TRANSISTOR PERFORMANCE

The current collected from the drain side (I_D) is the essential metric when evaluating the performance of a transistor. The relationship of I_D and the voltage applied to the three terminals can reflect the intrinsic properties of the device. Two major characteristics named transfer characteristic ($I_D - V_G$) and output characteristic ($I_D - V_{DS}$) are illustrated in Fig. 2.2 a and b, respectively, deriving many key performance metrics that are discussed below.

- On- and off-current: I_{on} and I_{off}
  I_{on} and I_{off} are commonly defined as the minimum and maximum I_{D} in the voltage span of a certain V_{DS} in the transfer curve (Fig. 2.2a), respectively. The ratio between I_{on} and I_{off} is called on-off current ratio ($I_{\mathrm{on}}/I_{\mathrm{off}}$), which is expected as large as possible to distinguish the on- and off-state within a small V_{G}. A typical assessment of transistor performance made from various technologies is to compare their I_{on} at the same I_{off} and V_{DS}. In industry, I_{off} is usually application-dependent. For instance, in the low-power system an $I_{\mathrm{off}} = 5$ nA/μm is required to lower the static power dissipation according to the specification under low operation power (LOP) condition [35].

- Threshold voltage: V_{T}
  V_{T} is the critical voltage that distinguishes the on- and off-state (Fig. 2.2a). Many factors such as temperature, channel size, and dielectric thickness affect V_{T} of a transistor. The difference between V_{G} and V_{T} is called overdrive voltage ($V_{\mathrm{OV}} = V_{\mathrm{G}} - V_{\mathrm{T}}$).

- Subthreshold swing: SS
  SS is defined as how much voltage needs to change I_{D} by one order of magnitude in the subthreshold region (Fig. 2.2a) with the expression given by,

$$\mathrm{SS} = \frac{\partial V_{\mathrm{G}}}{\partial log(I_{\mathrm{D}})} = \ln(10)\frac{k_{\mathrm{B}}T}{q}(1 + \frac{C_{\mathrm{dep}}}{C_{\mathrm{ox}}}) \geq \ln(10)\frac{k_{\mathrm{B}}T}{q} \approx 60\,\mathrm{mV/dec}\,(300\,\mathrm{K}) \tag{2.1}$$

  where k_{B} is the Boltzmann constant, T the temperature, q the electron charge, C_{dep} and C_{ox} the depleted and the gate oxide capacitance, respectively. SS mainly describes the steepness of the switching, thereby depending on the electrostatic control over the MOS capacitor. As Eq. (2.1) points out, the minimum SS at room temperature (300 K) of a conventional MOSFET is limited to 60 mV/dec due to the thermal injection of the carrier. However, SS can be further reduced below this limit in TFETs where the BTBT governs the carrier transport. As seen in Fig. 2.1b, the bandgap of the source cuts off the band tail of $f(E)$, thereby filtering out the high-energy electrons. This well suppresses the thermionic leakage in the off-state compared to MOSFETs. Consequently, a larger $I_{\mathrm{on}}/I_{\mathrm{off}}$ can be (ideally) achieved in TFETs with the same V_{G} swing. In other words, a smaller V_{G} swing is needed in TFETs than in MOSFETs to switch the current to the same level, thus lowering the power consumption.

- Transconductance: g_{m}
  $g_{\mathrm{m}} = \partial I_{\mathrm{D}}/\partial V_{\mathrm{G}}$ is defined as the linear slope in the transfer curve shown in

Fig. 2.2a, representing the efficiency of gate modulation of the transistor. The maximum value of g_m ($g_{m,peak}$) is an important metric that effectively influences f_T and the maximum oscillation frequency (f_{max}) in the RF performance of a transistor. A high g_m also means a larger gain through a transistor as it relates the input (V_G) and the output signal (I_D). Thus, g_m is also crucial for amplifiers and logic gates.

- On-resistance: R_{on}
  R_{on} is typically the reciprocal of the largest slope of $I_D - V_{DS}$ relation in the output characteristic as shown in Fig. 2.2b and is the total series resistance in the on-state consisting of contact resistance (R_c), access resistance of both the source and drain side (R_{acc}), and the channel resistance (R_{ch}) as the inset shows. Therefore, the reduction in any component of the resistance can lower R_{on}, resulting in an improved on-state performance.

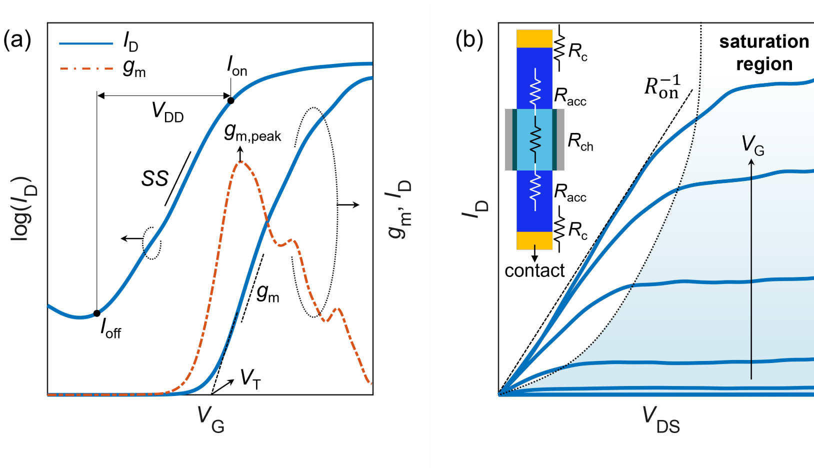


Figure 2.2: Typical performance metrics in MOSFETs. (a) Transfer characteristics. (b) Output characteristics with good saturation region. The inset illustrates all the components of (R_{on}). The color codes are identical to Fig. 2.1a

Other metrics such as output conductance ($g_d = \partial I_D / \partial V_{DS}$ reflects the transistor ideality in the saturation region of the output characteristic, see Fig. 2.2b) are also important but not highly relevant, and hence deep discussion of those metrics is out of the scope in this thesis.

2.1.2 INTERFACE TRAPS

As discussed in Chapter 1, D_{it} is considerably higher at the III-V/oxide interface as compared to Si since there is no suitable native oxide that can be used as dielectric like Si/SiO_2 in III-V materials. The surface of III-V materials may thus be oxidized or contaminated in the unvacuumed environment before depositing the gate oxide, leading to surface states due to imperfection. For example, faulty III-V bonds or dangling bonds can cause interface traps with the energies above E_C of InAs [36]. Also, the imperfection of gate oxide such as oxygen vacancies can generate interface defects with energies either above E_C and below E_C of III-V materials [37], being detrimental to n- or p-channel. As the gate oxide is typically amorphous, interface traps are expected to have distributions as a function of energy states. For instance, Fig. 2.3a shows the D_{it} distribution as the trap energy level (E_{tr}) with respect to E_C in the intrinsic InAs nanowires.

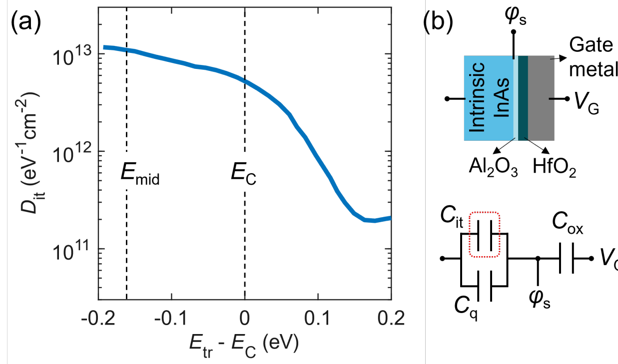


Figure 2.3: (a) A representative D_{it} distribution of intrinsic InAs nanowires extracted by *C-V* measurements from Ref. [38]. (b) Schematic of the InAs/Al_2O_3/HfO_2/metal MOS structure and the corresponding capacitance model.

The existence of interface defects is considered as an extra charging event, which can be modeled as a paralleled capacitance ($C_{it} = qD_{it}$) with the quantum capacitance (C_q), and then in series with the gate-oxide capacitance (C_{ox}), see Fig. 2.3b. Hence, the surface potential φ_s can be written as the voltage division of V_G and then SS can be related to D_{it} as below,

$$\text{SS} = \ln(10)\frac{k_B T}{q}(1 + \frac{C_q + qD_{it}}{C_{ox}}), \tag{2.2}$$

reflecting that SS linearly depends on D_{it}. As shown in Fig. 2.4, SS evidently degrades when the transistor has higher D_{it}.

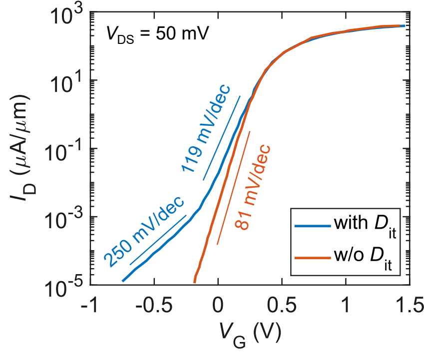


Figure 2.4: The impact of D_{it} on the simulated transfer characteristics of an InGaAs MOSFET. Data are from Ref. [39]. The SS degrades with presence of high D_{it} ($\sim 10^{13}$ $eV^{-1}cm^{-2}$) due to the donor-like interface defects.

Numerous investigations have aimed to suppress D_{it} or displace them beyond the energy range that is operated in MOSFETs. Various methods of III-V surface passivation via certain chemicals by wet etching [40] or using forming gas [41] while annealing has been suggested to decrease D_{it} and improve SS. Additionally, the self-cleaning phenomenon during the ALD process with inserting an Al_2O_3 interfacial layer at high growth temperature between III-V channel and HfO_2 high-κ has been detected [42], and thus such bilayer Al_2O_3/HfO_2 (1 nm/3 nm) high-κ is used for transistor fabrication in this thesis.

As discussed before, GaSb has a large number of surface oxide states due to its thick native oxide easily growing even during the air [43]. One of the main goal of this thesis is to improve the quality of GaSb/gate-oxide interface using different ways (see Chapter 4), lowering SS and I_{off} to enhance the switching performance in III-V p-FETs.

2.1.3 NEGATIVE DIFFERENTIAL RESISTANCE

When reversely biasing the source and drain (common drain configuration, $V_{SD} > 0$) in a TFET, a featured negative differential resistance (NDR) can be generally observed (Fig. 2.5), being evidence of tunneling junction within the device. This effect has been also studied well in Esaki diodes which is a reversely-biased p-n junction [44, 45]. Figures 2.5b–e elucidate the cause of this phenomenon. By gradually sweeping V_{SD}, the band edges at the source move down and enlarge the tunneling window (difference between $E_{F,S}$ and $E_{F,D}$, see Fig. 2.5b–c). This increases the tunneling current until E_V at the source aligns E_C at the channel reaching the peak current at $V_{SD} = V_P$.

Further increasing V_{SD}, the tunneling path is prohibited, and the current decreases (Fig. 2.5d), leading to an NDR region (Fig. 2.5a). When source bands are lowered enough so that carriers are able to thermally overcome the energy barrier (Fig. 2.5e), the current substantially increases again. Therefore, a current peak and valley are typically observed and their ratio (PVCR) is defined as a metric to evaluate the quality of the tunnel junction. However, NDR effect is unnecessary to be seen in all TFETs and depends on the structure design and material selection [46].

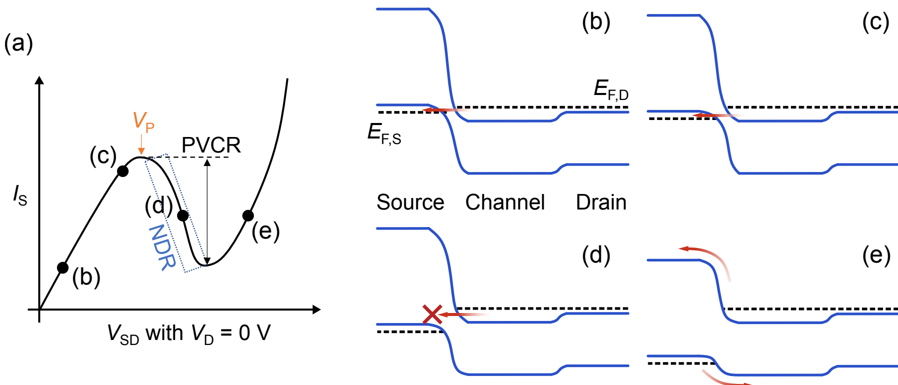


Figure 2.5: NDR effect in TFETs. (a) NDR *I*-*V* curve of a TFET at a fixed V_G. V_P is the corresponding voltage at the current peak and the peak-valley current ratio (PVCR) typically describes how strong the NDR effect is. (b–e) Schematics of band diagrams at different V_{SD} indicated in (a).

2.1.4 NEGATIVE TRANSCONDUCTANCE

In heterostructure TFETs, the gate placement is critical. Earlier work has shown that aligning the gate position overlaying more with the source segment (see Fig. 2.6a) gives lower I_D due to the strong source depletion [47, 48], leading to a small region with negative transconductance (NTC). This phenomenon can be explained by the band diagram in Fig. 2.6c–f where the bands of gate-overlapped source segment move down at high V_G, leading to the prohibition of BTBT, thus lowering the current. By intentionally modifying the source doping and increasing the overlapped region, even strong NTC can be achieved [49] and a parabola-shaped symmetric transfer is then obtained with equally large positive and negative g_m (Fig. 2.6b). Although from the performance perspective of TFETs, the presence of NTC is undesirable, many recent investigations with wide range of materials [50–52] have suggested wide potentials with NTC for multi-valued logic gates [52,53],

artificial synapses [50], and frequency doubling [54, 55], which may expand the application of using TFETs in a different way. We, in this thesis explore, this NTC feature in III-V TFETs for its application in signal modulation by carefully designing the gate/source overlap structure.

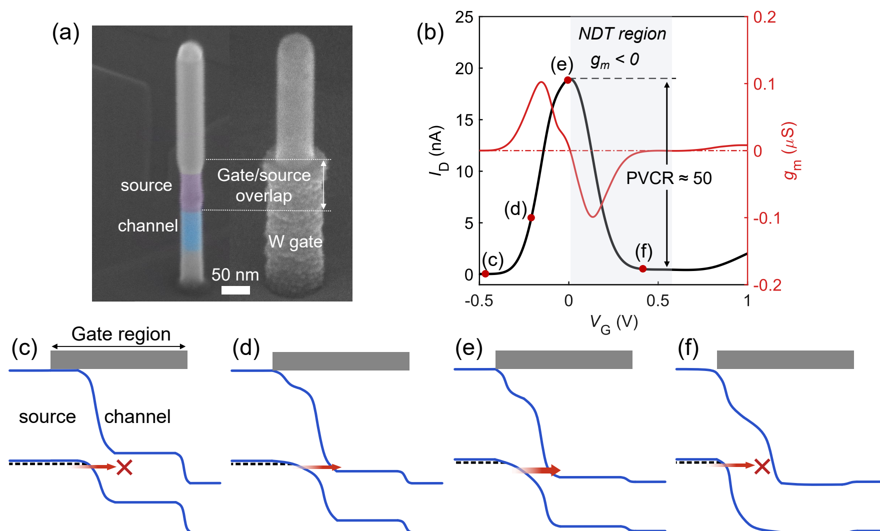


Figure 2.6: NTC in gate/source overlapped TFETs. (a) SEM image of a nanowire TFET post growth and during the fabrication after gate-length definition with gate/source overlap. (b) Representative transfer characteristic with strong NTC effect. A high PVCR of ∼50 is obtained in this device. (c–f) Schematics of band diagram at various V_G indicated in (a).

2.2 FERROELECTRIC FETS

Ferroelectrics are materials with spontaneous electric polarization, which can be utilized for non-volatile memories and neuromorphic devices. Ferroelectric FETs (FeFETs) are a class of FETs that replace the dielectric gate-oxide with ferroelectric material in conventional MOSFETs. The first FeFET was proposed in 1963 by using triglycine sulphate as the ferroelectric gate insulator [56] and then had been under high interest in research and industry. However, the continuous development of FeFETs was constrained by the low compatibility with IC manufacturing, challenging scalability, and unstable performance. The discovery of ferroelectricity in doped HfO_2 [57] has then changed this situation and triggered a rethink of FeFETs. As we discussed in Chapter 1, non-ferroelectric HfO_2 has been already used in industrial Si MOSFETs as a

high-κ dielectric, so HfO_2-based ferroelectrics are completely compatible with CMOS technology. Recently, robust ferroelectricity in ultra-thin HfO_2-based films has been found [58, 59], in line with the trend of scalability of future electronics, leading to high promise for further studies of HfO_2-based FeFETs. In this thesis, we mainly focus on the integration of Zr-doped HfO_2 (HZO) ferroelectric gate-stack on III-V vertical nanowire transistors as FeFETs rather than an in-depth discussion of HZO ferroelectrics.

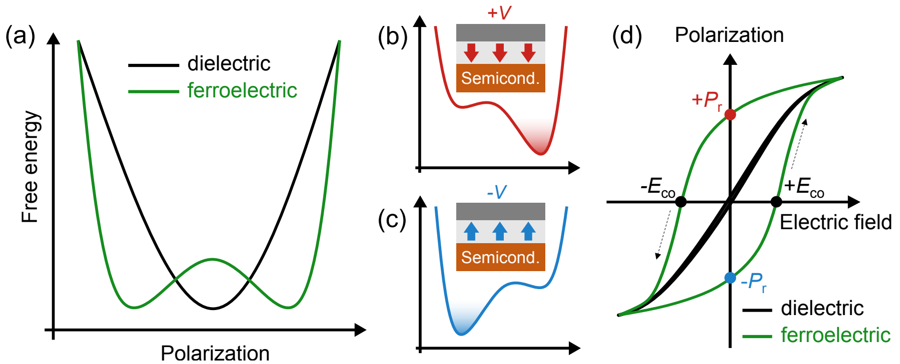


Figure 2.7: (a) A double-well energy landscape of ferroelectrics as a function of electric polarization. (b–c) Two polarization states can be achieved by applying corresponding external voltages ($\pm V$) at the ferroelectric MOS structure. Semiconductor is denoted by Semicond. (d) $P - E$ hysteresis in dielectrics and ferroelectrics. P_r is defined by the macroscopic polarization when no external electric field is applied while E_{co} is the electric field at $P_r = 0$ macroscopically [60]. The arrows indicate a counterclockwise sweeping direction.

2.2.1 REMANENT POLARIZATION

In amorphous dielectric materials, the lowest free energy is stabilized at zero polarization due to the isotropic nature as indicated in Fig. 2.7a. In contrast, ferroelectrics have two thermally stable lowest free energy point (double-well energy landscape) at different polarization states (Fig. 2.7a) due to the phase transitions during crystallization processing (e.g. rapid thermal annealing) in doped HfO_2 such as HZO [61]. The key element in FeFETs is the ferroelectric MOS structure in which the polarization switching can be controlled by applying an external electric field (voltage) as shown in Fig. 2.7b–c, leading to only one free energy minimum with one dominated polarization. The relationship between polarization and the applied electric field is shown in Fig. 2.7d where a representative polarization-field ($P - E$) hysteresis exists

in ferroelectrics. This hysteresis is a conventional measurement for proving the ferroelectricity in the tested material and gives fundamental parameters such as remanent polarization (P_r) and coercive field (E_{co}) as indicated in Fig. 2.7d. A widely used technique to obtain this loop is to measure $P-V$ curve from time-dependent current response from sequential positive and negative triangle voltage pulses. To avoid the leakage current confusing the result, a more advanced method called positive-up-negative-down (PUND) measurement has been demonstrated [62]. As it is commonly used nowadays for ferroelectrics, in-depth description of this measurement is excluded in this thesis.

2.2.2 MEMORY WINDOW AND RECONFIGURABILITY

The basic operation of a FeFET with a common source configuration is shown in Fig. 2.8. The gate electrode in FeFETs can either write and read the state (Fig. 2.8a). In the writing process, a voltage pulse ($\pm V_P$) is applied to the gate while the drain and source are grounded (Fig. 2.8b). The pulse width (t_{pulse}) is typically in the range of nanosecond (ns) to microsecond (μs) depending on the amplitude, in accordance with the nucleation-limited switching (NLS) model which fits well with the polycrystalline HfO_2-based ferroelectrics [61]. Recently, even faster switching down to picosecond can be achieved in ferroelectrics [63], indicating potentially lower energy in data writing. The polarization in the ferroelectric gate can be reconfigured after writing (Fig. 2.8c) and retains due to the non-volatility. In the reading process, a relatively small voltage range is swept at the gate with certain V_{DS} (Fig. 2.8b), avoiding destruction in the polarization state. As illustrated in Fig. 2.8c, two opposite polar directions in the gate oxide lead to a V_T shift when measuring the transfer characteristic of FeFETs, creating a voltage memory window (MW) between these two states: low-V_T and high-V_T state. This MW is an essential parameter for FeFETs used as non-volatile memories and reconfigurable devices that have two or more switchable V_T states. Many factors such as E_{co}, film thickness, and the interface will affect the magnitude of the MW [64, 65].

Additionally, the reliability of MW in FeFETs is crucial as it determines the ability of the device how well to retain its dipolar functionality over repeated writing cycles (endurance) and time after switching the polarization (retention time). Compared to other memory technological platforms, FeFETs have considerably long retention time with possible extrapolation over 10 years at 85 °C [66], thereby being promising as candidates for non-volatile memory. However, due to the natural switching mechanism, bulk charge trapping and detrapping are generated in the ferroelectric layer, resulting in MW shrinking over writing cycles [67, 68]. Moreover, for conventional Si

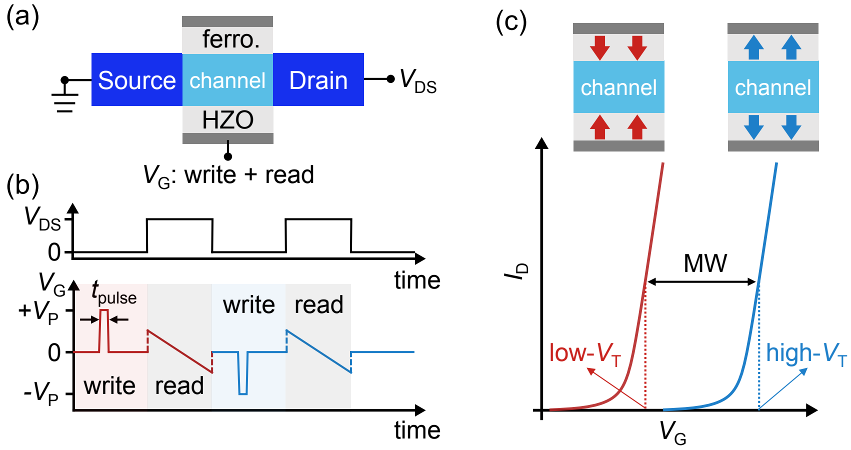
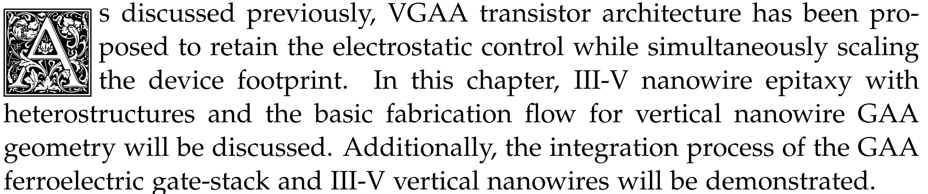


Figure 2.8: (a) Cross-sectional schematic of a nanowire FeFET. Both the write and read voltages are applied to the gate electrode. Ferroelectric is denoted by ferro. (b) A typical voltage pulse scheme of the FeFET write-and-read operation. (c) Transfer characteristics of a FeFET in two polarization states which are defined as low-V_T and low-V_T states. The difference between two V_T is the MW of the FeFET.

FeFETs, the thin native SiO_2 interlayer causes breakdown after certain cycling operations leading to device failure and limits the endurance to 10^4–10^6 [69]. Several strategies including interlayer engineering [69, 70], optimizing the writing scheme ([69], Paper IV), and high-pressure annealing [71] have been reported to increase the endurance up to 10^{10}. It is still in this early stage for FeFETs based on III-V channels, and an endurance of $\sim 10^4$–10^6 in the III-V/ferroelectric MOS structure has been achieved (Paper IV), which is lower than that of Si FeFETs. This can be attributed to the high defect density at the III-V/gate-oxide interface after the rapid thermal annealing (RTA) process (see Chapter 3 for details). However, recent work has suggested that using localized flash lamp annealing can lower the defects at the interface [72], thereby being potential to improve the endurance of III-V FeFETs.

3

Device fabrication



As discussed previously, VGAA transistor architecture has been proposed to retain the electrostatic control while simultaneously scaling the device footprint. In this chapter, III-V nanowire epitaxy with heterostructures and the basic fabrication flow for vertical nanowire GAA geometry will be discussed. Additionally, the integration process of the GAA ferroelectric gate-stack and III-V vertical nanowires will be demonstrated.

3.1 NANOWIRE EPITAXY

To achieve VGAA transistors, vertical nanowire geometry is desired and can be mainly formed by top-down etch from planar film epitaxy or bottom-up vertical epitaxy. The former approach gives an abrupt interface when it comes to heterostructures and controllable doping profiles. However, the large lattice mismatch between III-V and Si makes this method challenging to fabricate transistors on Si [9]. Therefore, most III-V VGAA transistors based on top-down etched nanowires were reported on non-Si wafers [73–75]. Moreover, the top-down etching might introduce sidewall roughness and contamination. On the other hand, bottom-up nanowire growth such as selective area epitaxy and catalyst-assisted vapor-liquid-solid (VLS) growth can provide high-quality sidewall surfaces and well release the strain induced by lattice mismatch from the heterostructure interface, enabling to grow III-V nanowires directly on Si [76, 77]. In this thesis, VLS is used for all nanowire growth.

3.1.1 VAPOR-LIQUID-SOLID GROWTH

The Au particles are typically used as the catalyst for VLS growth since Au can alloy with most materials. In this section, the epitaxy process with three nanowire structures (see Fig. 3.1) involved in the thesis will be mainly discussed, and all the nanowire growth is performed by MOVPE in a close-coupled showerhead system 18313 at a pressure of 100 mbar and a total flow of 8000 sccm. The nanowire epitaxy details are in **Appendix A**.

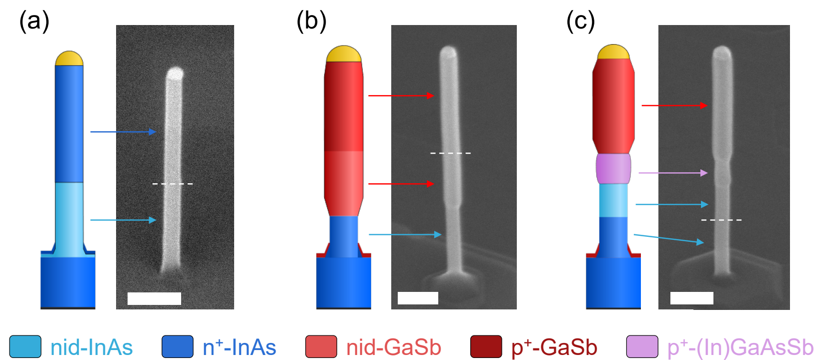


Figure 3.1: Schematics and corresponding SEM images of vertical nanowires for different devices. (a) InAs n-type MOSFETs. (b) GaSb p-type MOSFETs with a highly n-type doped InAs stem, nid-GaSb as the channel, and p-type doped GaSb as the drain; (c) InAs/(In)GaAsSb/GaSb TFETs. The scale bars are 100 nm. It has been proved that the introduction of a quaternary segment with (In)GaAsSb acting as the source for the tunnel junction can effectively reduce the tunneling in the off-state by creating a staggered band alignment with InAs channel [28]. Similar to the GaSb p-MOSFET, the p-doped GaSb is grown for the top contact.

Figure 3.2 shows the basic VLS growth scheme of our InAs nanowires with non-intentionally doped (nid) and n-type doped segments on the bottom and top, respectively, for n-FETs. As shown in Fig. 3.2a, the Au particles with desirable size (typically d_{Au} = 16–28 nm) and interval (pitch) are first prepatterned by EBL on the InAs/Si(111) substrate which consists of a ∼260-nm-thick highly doped InAs buffer layer grown on the commercial Si substrate. Next, when the growth conditions such as temperature, vapor pressure and source flow of the precursors reach the target, the InAs nanowire growth starts by supplying TMIn and AsH_3 which then decompose to In and As vapor molecules, respectively. At this moment illustrated in Fig. 3.2b, Au catalyst becomes liquid, and absorbs the vapor phase of the applied materials, leading to quicker nucleation and growth at the liquid-solid interface than at the solid

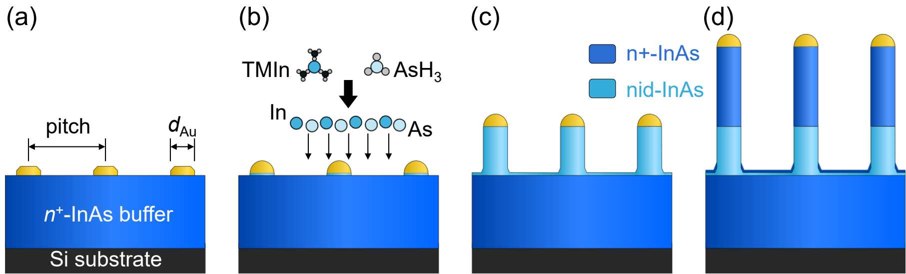


Figure 3.2: InAs Nanowire growth with VLS process. (a) EBL-defined solid Au particles before the growth. (b) InAs nucleation and growth at the liquid-solid interface via absorbing vapors decomposed by precursors. (c) nid-InAs nanowire growth with thin planar growth. (d) n-type doped InAs growth.

surface. As a result, the nanowire growth dominates with thin planar growth as shown in Fig. 3.2c. Figure 3.2d shows the n-doped InAs nanowire growth for the top contact segment by incorporating n-type dopant such as Sn during the growth.

3.1.2 CHALLENGES IN THIN GaSb NANOWIRES

The growth of GaSb nanowires differs from InAs. Although high-mobility GaSb nanowires were reported by direct growth with surfactant-assisted CVD approach [78], the growth orientation and dimension of those nanowires seem uncontrollable, thereby limiting the fabrication of VGAA p-FETs. In the conventional VLS process, GaSb nanowires are challenging to grow directly on the planar surface due to the difficult nucleation [79]. Therefore, a stem is usually utilized to initialize the GaSb growth in most of the reports though it is unnecessary for our device structure. Additionally, unlike InAs nanowires which usually have WZ phase with random switching between WZ and ZB phase, GaSb nanowires typically have pure ZB crystal structure, thereby excluding the emergence of stacking faults. Third, due to the Gibbs-Thomson effect, GaSb nanowires hardly nucleate and grow on the thin stem [80]. Figure 3.3 shows the comparison of GaSb growth on InAs stems with different diameters. It is also noticeable in Fig. 3.3b that GaSb is thicker than the InAs stem. This mainly results from the increased size of Au particles as both Ga and Sb are introduced into the reactor and have high incorporating concentration with Au at equilibrium [81]. Moreover, the V/III ratio in GaSb nanowire growth is critical. A large V/III ratio with a high TMSb molar fraction usually leads to significant additional radial growth on GaSb sidewall facets. Due to the long diffusion length on ZB {110} side facets of antimonide

nanowires, a homogeneous radial growth is observed in GaSb nanowires (Fig. 3.4). To suppress this overgrowth, a roughly balanced molar fraction of both TMGa and TMSb is typically used (V/III ratio is close to 1).

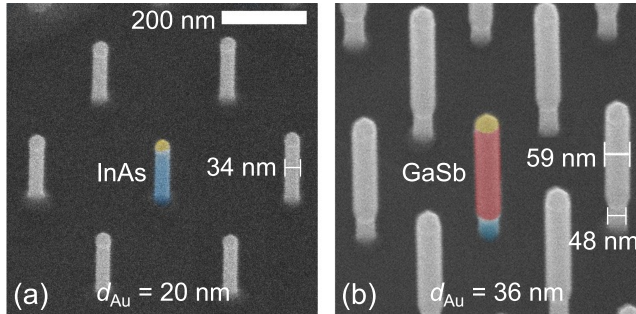


Figure 3.3: SEM images of GaSb Nanowire growth on InAs stem with different diameters in the same sample. (a) InAs stem with 20-nm Au particle. (b) InAs stem with 36-nm Au particle. Between two cases, GaSb only nucleate and grow on the InAs stem with d_{Au} = 36 nm.

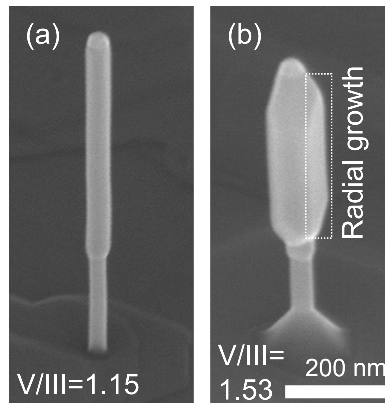


Figure 3.4: SEM images of GaSb nanowire overgrowth. (a) Without radial overgrowth. The GaSb nanowire has a similar diameter as the Au particle. (b) With significant radial overgrowth, leading to a larger diameter of the nanowire than that of the Au particle.

3.1.3 HETEROJUNCTION ENGINEERING IN TFETS

Heterostructure TFETs are sensitive to epitaxy as BTBT is spatially confined within a very short distance across the tunnel junction. Thus, slight modifica-

tion at the heterojunction can substantially change the performance. In Paper VIII, the TFET growth has been fine-tuned to realize a significant increase in I_D at SS = 60 mV/dec. The main optimization in growth is to delay the introduction of Ga and Zn dopant into the source segment, resulting in a longer unintentionally doped InAsSb segment which has a narrower bandgap than InAs. Due to the doping delay, the majority of the tunneling occurs at the p-(In)GaAsSb/nid-InAsSb interface, leading to a larger energy window for tunneling compared to that of InAs channel according to the band diagram in Fig. 3.5. Combined with that the carrier effective mass in InAsSb is smaller than that in InAs, the tunneling current thereby would increase, resulting in a higher I_{on} (Paper VIII).

3.2 STRAIN EFFECT IN GaSb-RELATED NANOWIRES

Strain, a mechanical property of materials, is very commonly observed in semiconductors and plays a critical role in electrical properties of transistors such as mobility [9]. The origin of strain in MOSFETs is technology and device-dependent. For instance, strain can come from the lattice-mismatched heterostructures during epitaxy and the intrinsic stress in the deposited film such as metals and spacers during device fabrication. In earlier Si CMOS technology nodes, the channel mobility has been enhanced from the strain induced by both the selectively epitaxial SiGe source/drain segment due to the lattice mismatch with Si channel and the high-stress SiN_x capping layers [82]. These techniques allow tensile strain introduced into n-FETs

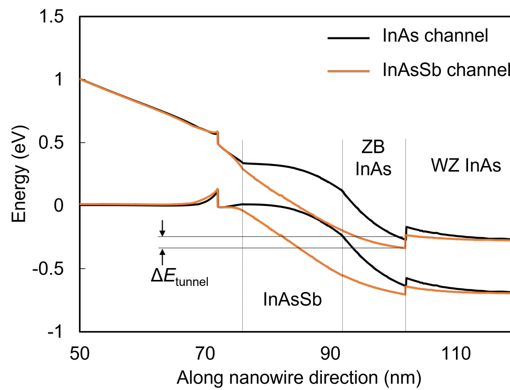


Figure 3.5: Band diagram simulation of heterojunction TFETs with InAsSb channel compared to InAs channel. ΔE_{tunnel} indicates a larger energy window for tunneling in the case of InAsSb channel.

while compressive strain into p-FETs, thus improving both electron and hole mobility of the channel, respectively. For example, by using the strain engineering, IBM's 7-nm FinFETs have shown 1.6 GPa stress in both n-FET and p-FET channel, leading to significant enhancement of effective drain current [83].

For III-V semiconductors, compared to their n-type counterparts, p-FETs have much lower mobility (see Table 1.1). However, by introducing compressive strain in III-V antimonides, the hole mobility used for p-channel materials can be further improved, thereby being possible to balance the p-FET performance with n-FETs. Many previous investigations including lattice-mismatched heterostructure epitaxy [84,85] and process-induced SiN_x stressor on the channel [86] have shown the enhancement of hole mobility and g_m in the planar transistors. In vertical nanowire structures, a core-shell structure (radial heterostructure) can accommodate more residual strain compared to the axial heterostructure. The simulation result in Fig. 3.6 shows that the strain is evenly distributed in the nanowire in the core-shell structure while localizes only near the interface in the axial heterostructure due to the large aspect ratio. Therefore, to introduce sufficient compressive strain into the entire channel for a p-type nanowire device (e.g. GaSb p-FETs), the core-shell geometry is desired.

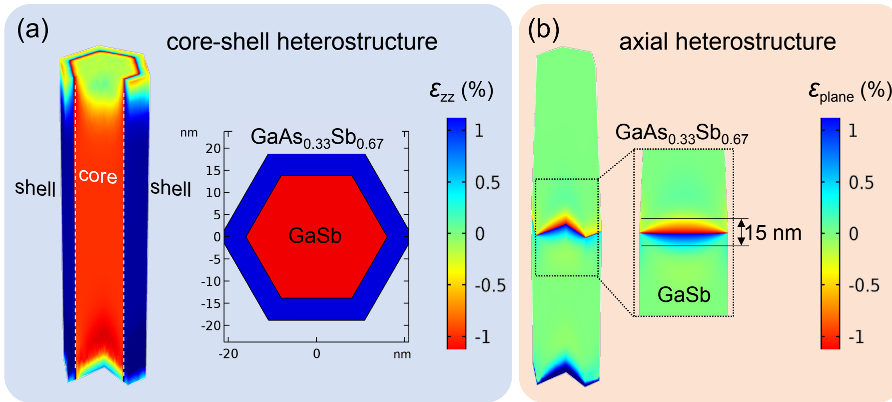


Figure 3.6: Strain simulation using finite-element methods. Axial strain (ε_{zz}) distribution in (a) GaSb-GaAsSb core-shell nanowires and (b) in-plane strain (ε_{plane}) in axial GaSb/GaAsSb heterostructure nanowires. The strain in the core-shell structure is almost constant while attenuates quickly along the nanowire (only confined within ∼15 nm) in the axial heterostructure.

Paper I demonstrates compressively-strained GaSb nanowires achieved by growing GaSb-GaAsSb core-shell structures as GaAsSb ternary alloy has a smaller lattice constant than that of GaSb. Figures 3.7a–c present the SEM

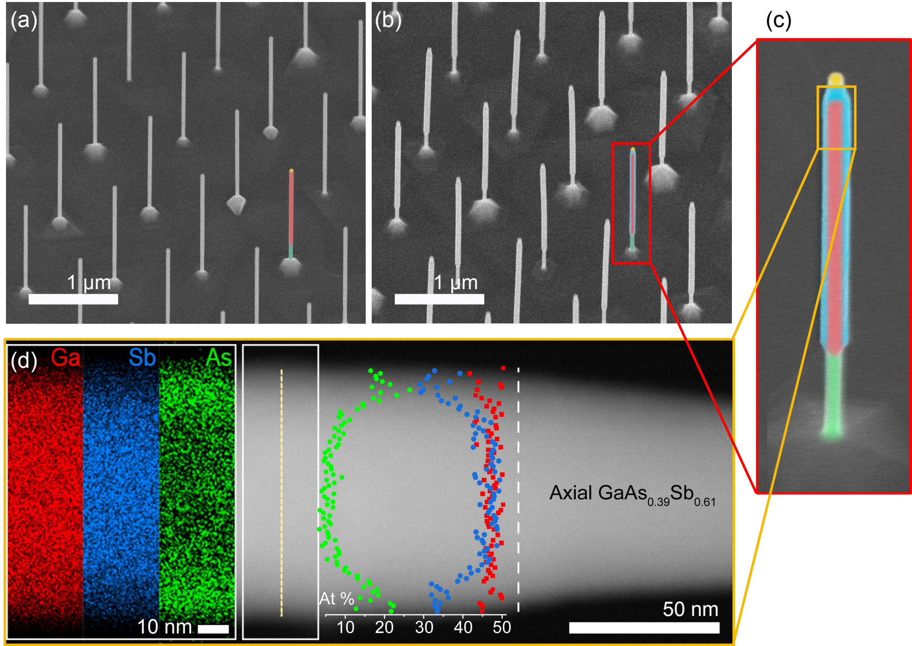


Figure 3.7: Structural morphology of GaSb-GaAsSb core-shell nanowires. SEM image of (a) bare GaSb nanowire arrays and (b) GaSb-GaAsSb core-shell nanowire arrays with magnified single nanowire in (c). False-color codes: green for InAs, red for GaSb, and blue for GaAsSb shell. (d) Elemental distribution and atomic compositions from TEM-XEDS mapping (left white box) and linescan (yellow dashed line) in the core-shell nanowire, respectively. The result shows almost identical x_{As} = 0.4 in both the shell and the axial GaAsSb.

image of bare GaSb nanowires and GaSb-GaAsSb core-shell nanowires, respectively. The TEM and XEDS result in Fig. 3.7d confirms the As composition (x_{As}) of GaAsSb in both the shell and the inevitably grown axial GaAsSb. With varying both the shell thickness (t_{shell}) and the x_{As} in the GaAsSb shell, axial strain values along the nanowire direction (ε_{zz}) in the GaSb core are obtained by the XRD measurements (see Fig. 3.8a) in which an evident right shift of the GaSb peak indicates a smaller lattice constant of the GaSb core in the nanowire growth direction according to the Bragg's law. Figures 3.8b–c summarize the results of ε_{zz} with varying t_{shell} and x_{As}. The maximum ε_{zz} of –0.92% in the GaSb core has been achieved with a 9.2-nm-thick $\mathrm{GaAs_{0.33}Sb_{0.67}}$ shell. This value is close to –1% uniaxial strain which was theoretically predicted to reduce the hole effective mass of GaSb [111] orientation by about

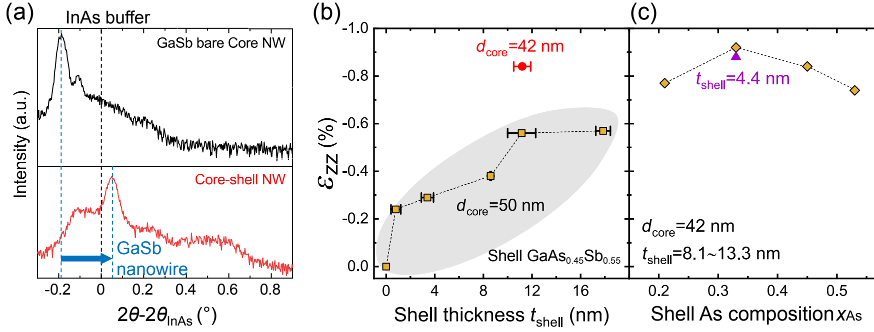


Figure 3.8: Axial strain as a function of t_{shell} and x_{As} obtained by XRD measurements. (a) XRD spectrum with (111) $\omega/2\theta$ scans (see Paper I) of bare GaSb nanowire (top) and GaSb-$GaAs_{0.33}Sb_{0.67}$ core-shell nanowire with core diameter (d_{core}) of 42 nm and t_{shell} = 9.2 nm. The right shift of GaSb peak signal indicates compressive strain along [111] (nanowire growth direction) in the GaSb core. (b) and (c) are the axial strain ε_{zz} with varying t_{shell} and x_{As}, respectively.

7 times compared to the unstrained case [87], leading to further mobility enhancement. In fact, uniaxial compressive strain in the GaSb nanowire may have more attractive potential for advanced transistor architecture such as GAA MOSFETs where a thin channel is preferable. Additionally, compared to biaxial compressive strain in the planar strained GaSb films, uniaxial compressive strain provides more enhancement in hole mobility for p-type channel MOSFETs [9]. The theoretical results showed that the hole mobility in GaSb is almost doubled with 2% compressive biaxial strain while 3–4 times higher with the same amount of uniaxial strain [88]. Therefore, the core-shell structure presented in Paper I provides a potential approach to achieve high uniaxial strain along the channel direction in GaSb nanowire for high-mobility p-FETs.

For the axial III-V heterostructures such as InAs/GaSb and TFET nanowire structures, the strain only exists within a confined region close to the interface (Fig. 3.6), thereby negligibly affecting the electrical properties. However, for heterostructure nanowire TFETs in which the BTBT process determining the drive current is spatially confined at the interface, the strain may still significantly influence the tunneling current [89] by changing the band structures and effective mass [90,91]. For such an ultra-scaled region down to only a few nanometers, strain characterization using lab-based XRD setup is challenging. Despite the complex measurement scheme and low spatial resolution, the strain distribution in an individual InAs/GaSb nanowire TFET has been

mapped by using synchrotron-accelerated fast scanning X-ray nanodiffraction [92], which provides a possible way for nanostructure strain characterization.

3.3 FABRICATION PROCESS FOR VERTICAL NANOWIRE TRANSISTORS

In this section, the process flow of the vertical nanowire transistors will be presented briefly. The details of each step in the processing are included in **Appendix B**.

3.3.1 BASIC PROCESS FLOW

A basic gate-first process flow of vertical nanowire transistors is provided and discussed in this subsection as shown in Figs. 3.9a–f with an example of GaSb p-FETs. Almost identical processing is utilized for other types of nanowire transistors such as TFETs in this thesis. Figure 3.9g shows the layout of a final single nanowire device with three terminals for probing. The corresponding magnified SEM image of Ni/Au-coated nanowire transistor is presented in Fig. 3.9h. Other slightly different variants of gate-first vertical processing including using a polymer as the second spacer (Paper II) and skipping the first spacer (Paper IV&VI) can also be utilized for specific purposes.

3.3.2 DIGITAL ETCH ON NANOWIRES

DE is a selective etch technique that can controllably thin down the nanowire diameter by alternating the process of surface oxidation and wet etching of the oxides as illustrated in Fig. 3.10. This is a critical step to achieve ultra-thin channel diameter for VGAA nanowire FETs for improved electrostatic control of the gate. Additionally, DE provides a surface pretreatment prior high-κ deposition, further improving the channel-oxide interface quality, thus reducing SS. With this technique, scaled channel diameters have been demonstrated in vertical nanowire InGaAs n-FETs with SS of 70 mV/dec [73] and InAs/InGaAsSb/GaSb TFETs with SS = 35 mV/dec [93]. Typically, oxygen plasma or ozone is selected for surface oxidation for arsenide materials such as InAs and InGaAs and various acids can be used as wet etchant for III-V oxides. Almost the same etch rate of $\sim$1 nm/cyc. and nanowire diameter down to $\sim$10 nm were obtained in each DE scheme for InAs [94] and InGaAs [73]. For TFETs, water-based citric acid is usually used to selectively etch InAs oxides from GaSb oxides so that thick GaSb still remains with large area for the top contact.

The performance of antimonides-based p-FETs is usually inhibited by the poor electrostatics originating from the high level of interface and border traps (see Table 1.1). Therefore, it is important to develop a suitable DE scheme

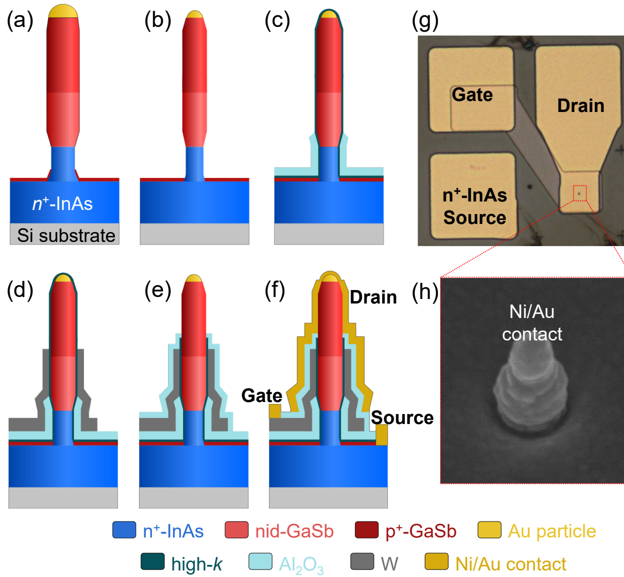


Figure 3.9: Vertical nanowire process of GaSb p-FETs. Schematics of critical fabrication steps: (a) Nanowires post epitaxy; (b) The nanowire device after DE which removes the oxides on the nanowire sidewalls and shrinks the channel diameter; (c) High-κ and first spacer (Al_2O_3) deposition by ALD. The height of the first spacer is defined by S1813 photoresist mask and back-etch process using oxygen plasma in RIE setup; (d) After W gate sputtering, the gate length gate pads are defined by the same process in (c) and the excessive W is dry etched by SF_6:Ar in RIE; (e) ALD-deposited second Al_2O_3 spacer is used to isolate the drain and the gate. The same back-etch process is used to control the height of this spacer; (f) Via exposure and contact metallization (10-nm Ni/200-nm Au by sputtering) finalize the device fabrication. (g) The top-view optical image of a single nanowire transistor. (h) SEM image of the final nanowire device with Ni/Au contact metal on the surface.

for III-Sb p-FETs to benefit further from its high hole mobility. However, previous study from *Lu et. al.* has shown that the above oxidizing agents (ozone and oxygen plasma) are too aggressive for III-Sb, leading to forming high order of Sb oxides like Sb_2O_5 which is almost impossible to be fully etched in most acids [95]. The authors suggested a DE scheme using a more gentle oxidizer like pure O_2 atmosphere combined with 10% HCl:IPA etch for 30 s as the etching process. By using this alcohol-based HCl DE method, a controllable DE rate and thin channel diameter down to 16 nm has been achieved [94]. Nevertheless, SS in Sb-based p-FETs still needs to further improve as compared to its n-type counterparts.

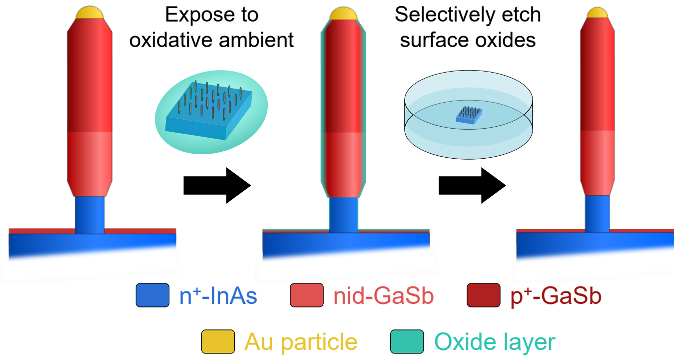


Figure 3.10: Schematics of the 1-cycle DE process of Vertical GaSb nanowires. For GaSb, exposure in O_2 ambient is enough to generate GaSb oxides on the nanowire sidewalls. Different acids such as HCl and HF can be used for wet etching of GaSb oxide layer.

In Paper II, two DE schemes for GaSb nanowire channel using different etching chemicals have been investigated and compared. Apart from alcohol-based HCl (HCl:IPA), water-based BOE is for the first time introduced as the DE process for GaSb device. As shown in Fig. 3.11, in contrast with the case of HCl:IPA 1:10, BOE 30:1 also exhibits a stable and controllable etching rate within about 7 cycles. By repeatedly performing DE process, the GaSb nanowire diameter gradually reduces in both cases. Noticeably, the nanowires start breaking off in BOE DE after 7 cycles while they maintain a great mechanical yield in the case of HCl:IPA. The reason behind this can be that alcohol-based acids have lower surface tension than water-based acids [96], leading to broken nanowires during wet etching or the following rinse step. Although the mechanical yield is lower after 7 cycles than in the case of HCl:IPA, using BOE may still benefit by simplifying the Sb-based process integrated on Si technology without introducing new chemical etchant as BOE is commonly used in the Si-based CMOS process.

The corresponding statistical results of the GaSb nanowire array in two DE schemes along with results of InGaSb nanowires from literature are compared in Fig. 3.12. The increase of etching time in BOE (40 s *vs*. 30 s) does not change the etch rate, confirming that the etching stops when the oxides are fully removed with 30 s. In all cases, the etch rate during the first 3 cycles remains similar (~1.2 nm/cyc.) and almost identical to that of III-As nanowires. The average etch rate is ~1 nm/cyc. in BOE while ~1.2 nm/cyc. in HCl:IPA for both GaSb and InGaSb. The etching almost saturates after 5 cycles in HCl:IPA and 7 cycles in BOE. In the gate-first vertical process, DE is the first fabrication

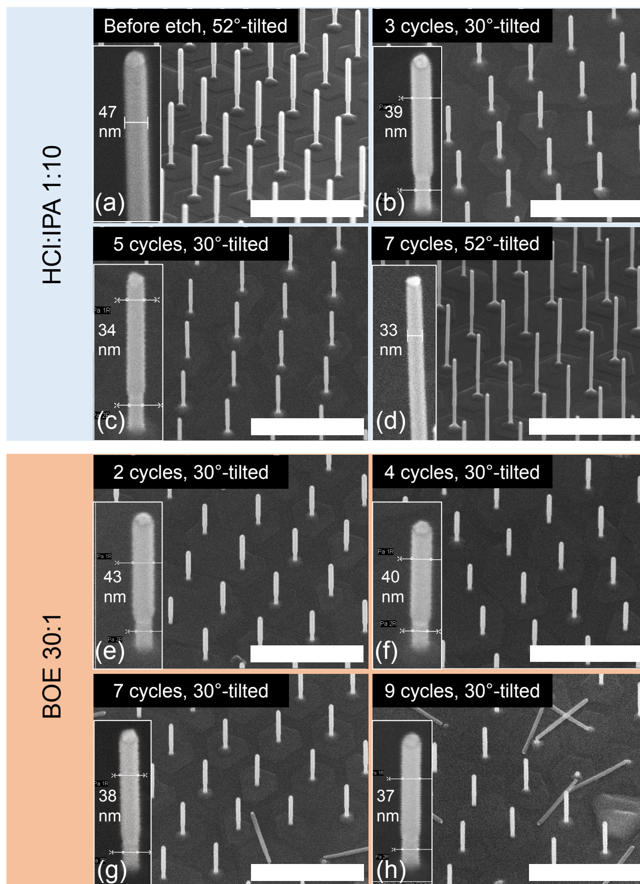


Figure 3.11: (a) SEM image of nanowires before DE. A sequential etch experiment with different numbers of DE cycles in (b-d) HCl:IPA 1:10 and (e-h) BOE 30:1, respectively, performed in two samples with a GaSb nanowire array. The insets show a single nanowire in the array. The scale bars are 1 μm.

step and thus the etch rate in this study is comparable. However, the etch rate in the gate-last process could be very different due to the potential change of the nanowire surface state after many processing steps.

To further explore the ability of surface oxide removal with two DE schemes, XPS measurements on GaSb substrates with different surface states were employed (Fig. 3.13). The results in Fig. 3.13 show that both HCl:IPA and BOE can significantly remove oxides of GaSb surface. Particularly, a strong reduction of Sb oxides after DE with either HCl:IPA or BOE is observed as shown in Figs. 3.13d–f, which may lead to improved electrostatics in

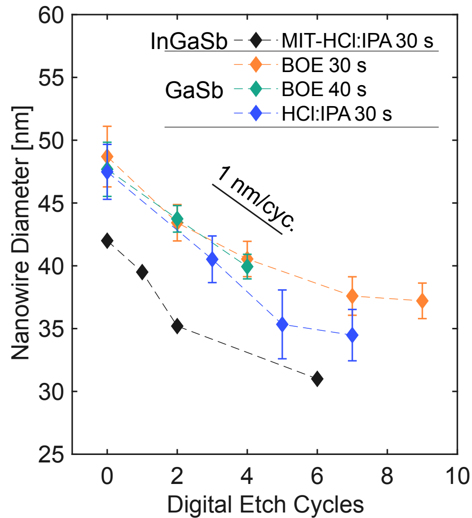


Figure 3.12: Average nanowire diameters from the GaSb nanowire array (as indicated in Fig. 3.11) as a function of DE cycles to determine the etch rate in various wet etch situations. The black diamond data of InGaSb nanowires is from Ref. [73]. O_2 ambient is used for surface oxidation in all cases. The error bars denote the standard deviation.

GaSb p-FETs with both DE schemes. The main difference from XPS results between the two cases is that Ga oxide states such as Ga_2O_3 and Ga_2O are less suppressed by BOE etching as compared to that of HCl:IPA as indicated by Fig. 3.13b–c, which can be a reason that higher SS are observed in GaSb p-FETs with BOE DE compared to that with HCl:IPA DE (see Chapter 4 for details).

3.3.3 GATE-LAST PROCESS

Gate-last process provides the opportunity for self-aligned channels for vertical nanowire FETs in which the device fabrication is initialized with the source and drain contacts and finalized with the gate-stack formation. In this case, the gate length can be accurately and intrinsically defined by the opening between the source and drain contacts, which ideally removes the access resistance. For vertical InAs/InGaAs nanowire FETs, a thin highly doped shell is grown for better contact [97] but needs to be removed for the channel region. In this case, the gate-last process allows selective DE employed only on the channel region as the source and drain are protected. As a result, a

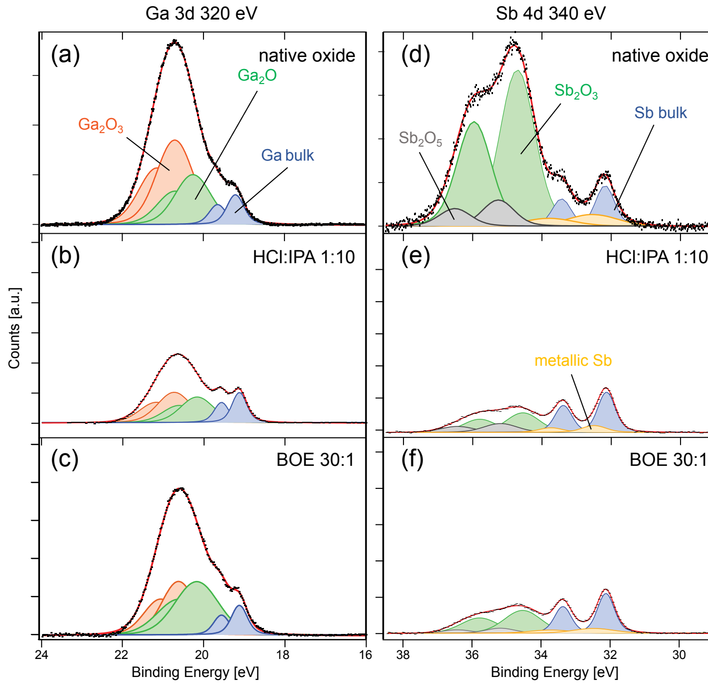


Figure 3.13: Synchrotron-based XPS results of (a–c) Ga 3d and (d–f) Sb 4d core levels obtained from GaSb substrates with different surface states: (a,d) no surface pretreatment with native oxides; (b,e) post HCl:IPA 1:10 etching followed by ALD-deposited Al_2O_3 protection layer; (c,f) post BOE 30:1 etching followed by ALD-deposited Al_2O_3 protection layer. The intensity of each spectrum is normalized to the peak heights of the Ga bulk and Sb bulk components for visualization.

thin channel and a thick top segment in the nanowire for improved contact can be simultaneously achieved. In addition, the gate-last process enables higher scalability for short channel devices with precise control of $L_g < 100$ nm [77]. By using this process, an ultrathin GaSb p-channel down to 16 nm has been obtained [94], which can overcome the diameter limitation in the VLS growth due to Gibbs-Thomas effect [80].

A thin doped InAs(Sb) shell grown on GaSb nanowire sidewalls can improve the top contact this core-shell configuration has a lower resistance than bare GaSb nanowire [98]. Figure 3.14a illustrates the key fabrication flow until gate-stack formation in the gate-last process for GaSb p-FETs. Unlike our previous self-aligned process for GaSb transistors [17,99], all inorganic spacers

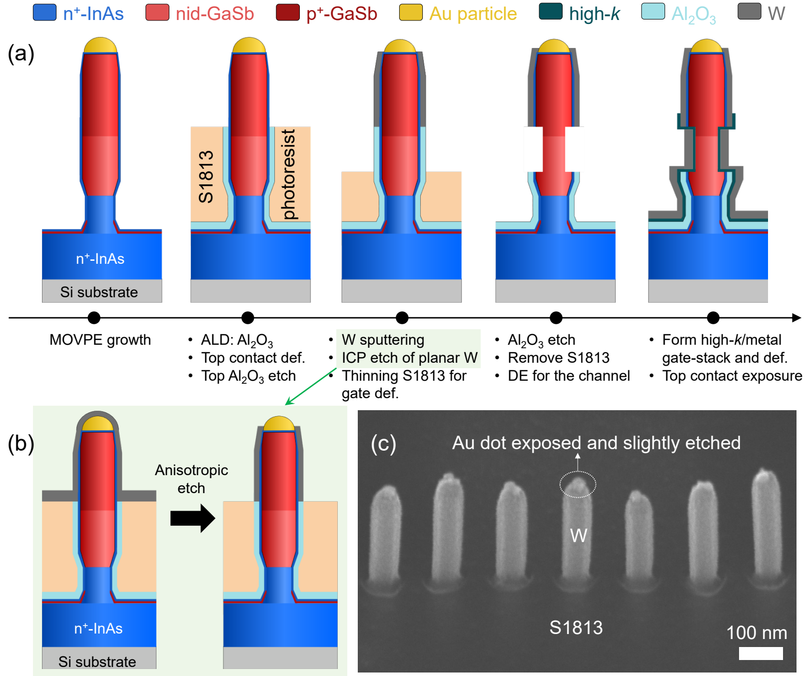


Figure 3.14: (a) Schematics of initial steps in the gate-last process (the following fabrication steps are identical to the gate-first process as shown in Fig. 3.9) Def. denotes definition. (b) Detailed step of anisotropic ICP etch of planar W film. (c) SEM image of one GaSb nanowire row after planar W etch with a clean photoresist (S1813) surface.

enable the post-fabrication RTA (Paper III) for the devices to further enhance the performance (see Chapter 4). Another major difference compared to our earlier gate-last process is that we replace the EBL step with UV lithography to define the top contact length by using back-etch of S1813. Hard-baked S1813 also enables high-quality W film sputtering (Fig. 3.14b). ICP is then utilized to only anisotropically etch the planar W while remaining the W on the nanowire sidewalls (Fig. 3.14b). This is practically realizable due to the high etch rate of W in SF_6:N_2 gas ambient with very low reactor pressure of 5 Torr. In our specific case, a clean planar surface of S1813 but W on the top of the nanowire sidewalls has been achieved (Fig. 3.14c). It is also noticeable that the Au dot is exposed on top of nanowires and slightly etched during the ICP dry etch due to the high etch along the vertical direction.

The fabricated GaSb nanowire p-FETs with the gate-last process have a L_g of ∼80 nm and a thin channel diameter of ∼35 nm by using 3 cycles of DE

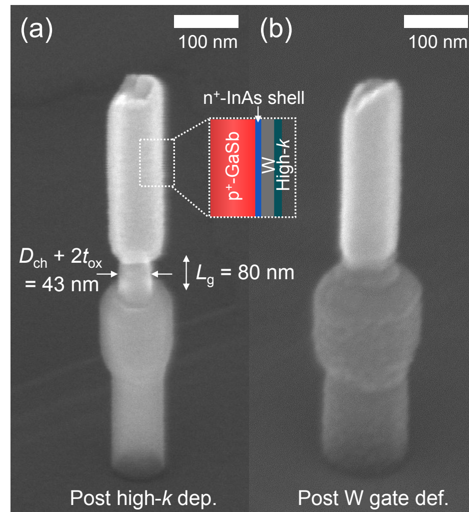


Figure 3.15: SEM images of a single nanowire GaSb p-FET with InAs(Sb) shell during the gate-last process (a) post high-κ deposition and (b) post W gate definition. The real channel diameter (D_{ch}) can be determined by knowing the high-κ thickness (t_{ox}) from the reference planar sample measured by ellipsometer. Here, 43 nm is measured in SEM and t_{ox} = 4 nm for Al_2O_3/HfO_2 bilayer high-κ.

after exposing the channel region (Fig. 3.15a). Meanwhile, a thick nanowire segment with InAs shell is kept for a better top contact as shown in Fig. 3.15. To fully remove the InAs shell in the channel, the first cycle of DE in this case was carried out in an ozone ambient at 50 °C to oxidize the InAs surface. This results in a much higher etch rate in HCl:IPA than that for samples being only exposed to the oxygen, which could be attributed to that the ozone penetrates the thin InAs shell and significantly oxidizes the GaSb core. Most of the samples discussed in this thesis were fabricated by gate-first process which is simple and straightforward since the aggressive downscaling of the channel is beyond the main goal of the thesis.

3.4 FERROELECTRIC GATE-STACK INTEGRATION

Integration of HZO ferroelectric gate-stack with III-V channel materials is the key to the fabrication of III-V vertical nanowire FeFETs and ferro-TFETs. Similar as the Al_2O_3/HfO_2 high-κ, HZO film is usually grown by thermal ALD. The most common approach to achieve ferroelectricity in HZO films is using RTA to partially crystallize the film into an orthorhombic phase which is

believed to mainly contribute to the ferroelectricity formation (see processing flow in Fig. 3.16a–d). Compared to Si, III-V arsenides and antimonides have lower thermal stability and thus may reduce the crystal quality during RTA process at high annealing temperatures. Figures 3.16e–h show the morphological influence of the ferro-TFETs at different annealing temperatures with N_2 ambient for 30 s. The SEM results indicate that the nanowires can survive at the temperatures up to 500 °C. Further increasing the temperature, the Au particle seems to become liquid phase and migrate from the top to the sidewalls during annealing at 550 °C (Fig. 3.16g) and even catalyze the nanowire growth from the sidewalls at 600 °C (Fig. 3.16h). Therefore, achieving ferroelectric HZO films yet reducing the annealing temperature is critical for HZO-based III-V FeFETs and ferro-TFETs.

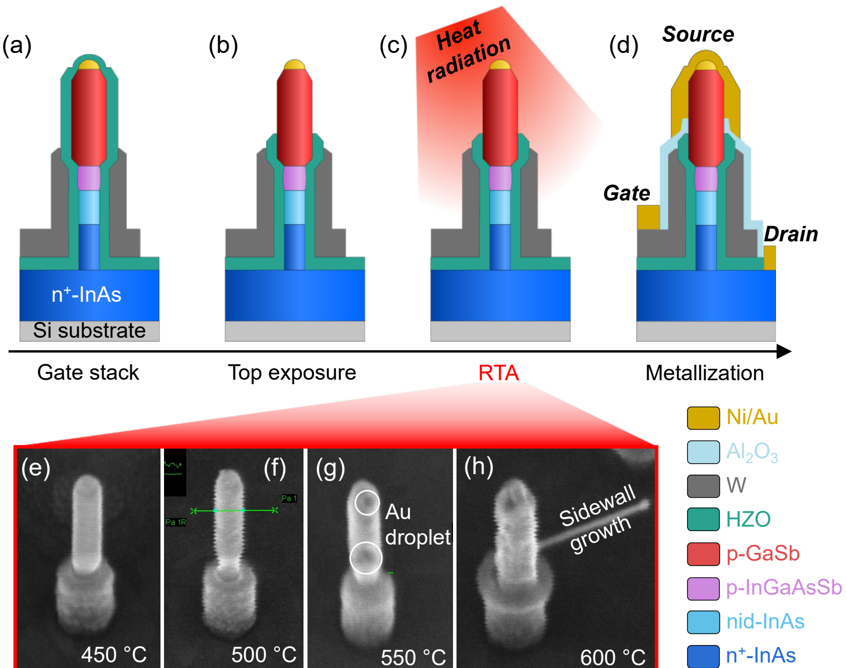


Figure 3.16: (a–d) Critical steps of vertical ferro-TFET fabrication. Here, the bottom spacer was skipped to enable the electrical test for verification of ferroelectricity post RTA. (e–h) SEM images of ferro-TFETs post top HZO etching when sequentially increasing the annealing temperature in RTA process. Presented single nanowires are not the same one.

Based on results obtained via SEM, it was determined that an annealing temperature below 500 °C is preferred for HZO crystallization during ferro-

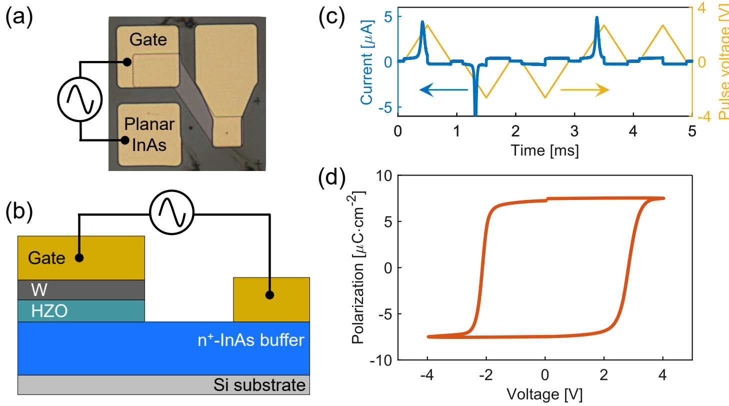


Figure 3.17: PUND measurements of planar ferroelectric MOS structure on the ferro-TFET sample after RTA at 450 °C. (a) Top-view optical image of the measurement scheme on one ferro-TFET device. (b) Side-view schematic of (a). (c) Voltage pulse scheme and corresponding sensed current in the PUND measurement. (d) Extracted ferroelectric polarization-voltage hysteresis of the planar MFS structure on the ferro-TFET.

TFET processing. As a result, 450 °C was chosen as the initial annealing temperature for this process. To verify if the sample turns ferroelectric, the PUND measurement of the planar W/HZO/InAs structure on the ferro-TFET sample after annealing at 450 °C was performed as shown in Fig. 3.17a–b. The experimental result in Fig. 3.17c–d showed evident ferroelectric hysteresis in the typical polarization-voltage relationship which was achieved by the ferroelectric current. Although the remanent polarization is lower than those obtained at higher annealing temperature which usually can reach > 20 μC·cm^{-2}, the charge change in the HZO gate oxide originating from the ferroelectric polarization is sufficient for such a nanoscale channel to have apparent V_T shift in our final nanowire ferro-TFET device (see Chapter 5). Lower annealing temperature such as 400 °C has been also examined but no ferroelectricity was obtained from the same HZO film.

4

Electrical measurements and results

AIN results of electrical characterization in III-V vertical nanowire transistors including p-type MOSFETs, TFETs, FeFETs, and ferro-TFETs will be presented in this chapter. We will also discuss and benchmark the corresponding performance with reported works in the literature.

4.1 III-V NANOWIRE P-FETS

All III-V CMOS technology is mainly impeded by the p-type III-Sb MOSFETs as addressed in Chapter 1, which results in very unbalanced performance compared to their n-type counterparts. Here, we demonstrate the performance enhancement of III-V p-FETs with different approaches.

4.1.1 CHANNEL SURFACE PRETREATMENT

III-Sb materials are typically sensitive and very rapidly oxidized even in the air [73]. In Chapter 3, two DE schemes for GaSb nanowires have been discussed and both can act as a great oxide removal. In Paper II, we fabricated GaSb p-FETs by implementing these two DE schemes (HCl:IPA and BOE). The corresponding transfer characteristic from two representative devices (Fig. 4.1a) with either HCl:IPA or BOE surface pretreatment prior to high-κ deposition are compared. The results show almost identical I_{on} and maximum I_{D} while a remarkably reduced I_{off} for the device with DE in HCl:IPA, which leads to a $\times 5$ increase in $I_{\mathrm{on}}/I_{\mathrm{off}}$ and improved SS in the case of HCl:IPA etching. These observations imply that HCl:IPA removes more oxide states on the GaSb nanowire surface in contrast with the situation of using BOE. This is in consistency with the XPS results shown in Fig. 3.13. The statistical

results show that the performance in the on-state such as peak g_m (Fig. 4.1b) is almost the same in two cases. The variations may come from slightly different nanowire length during the growth and the processing variability. Compared to DE in BOE, an increased I_{on}/I_{off} and decreased SS_{min} in Figs 4.1c–d are achieved by DE in HCl:IPA, in agreement with the result in Fig. 4.1a. Although DE with HCl:IPA exhibits overall better performance, using BOE for surface pretreatment can also remove most of the surface oxide states (Fig. 3.13) and generally provides improved SS and I_{off} compared to previously reported III-Sb transistors. With regard to the integration of III-V with Si technology, BOE could be more compatible and thus simplifying the chemical selection during the processing scheme.

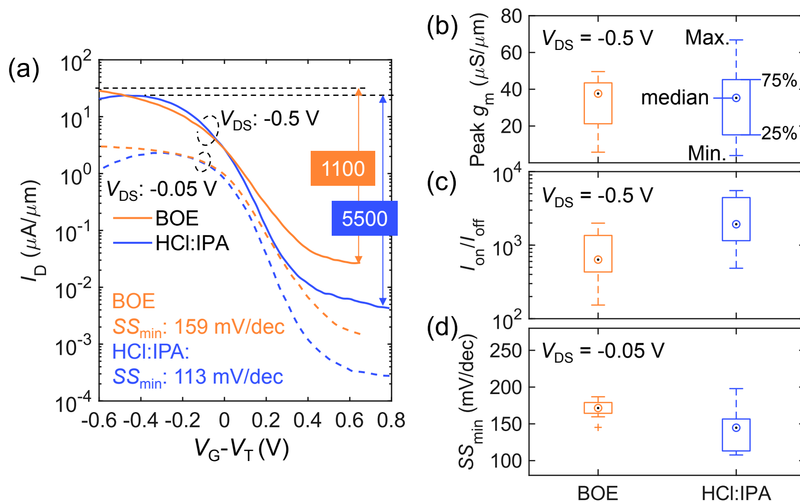
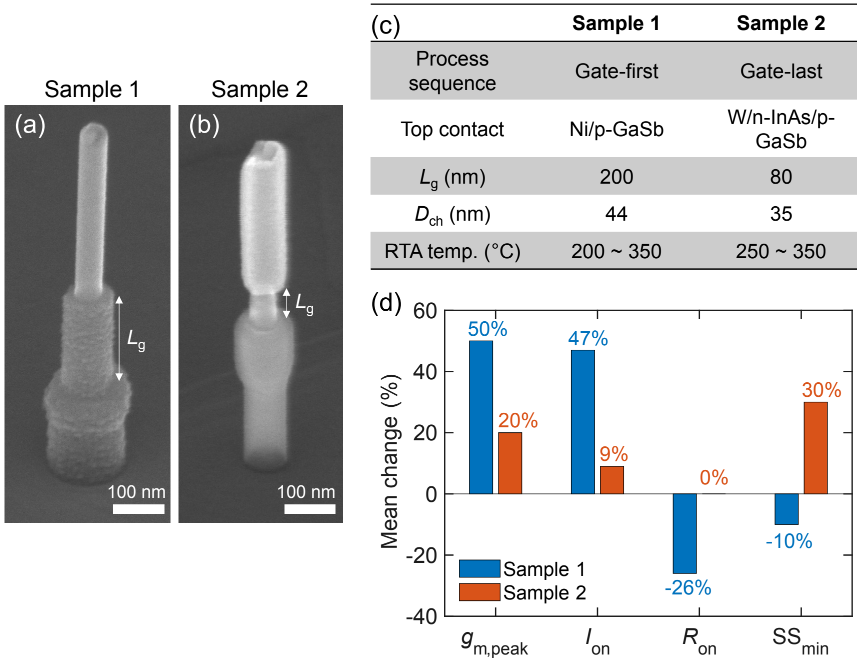


Figure 4.1: (a) Transfer characteristic of the representative single nanowire device from two samples with almost identical dimension but different channel surface pretreatment. The I_{on}/I_{off} is defined as the maximum value within ΔV_G = 1.2 V (the same for the following). Statistical result with boxplots including (b) peak g_m, (c) I_{on}/I_{off}, and (d) SS_{min} based on over 10 devices in two samples.

4.1.2 ANNEALING WITH FORMING GAS

For MOSFETs, RTA process has been demonstrated to passivate the interface between channel and the gate oxide in a forming gas (H_2/N_2 mixed gas) ambient [40,100] and improve the metal/semiconductor contact [101,102]. As discussed previously, the major challenges for III-Sb p-FETs lie on the MOS interface and the contact. Therefore, RTA could provide a possible approach

to further enhance the transistor performance. The influences of annealing on GaSb-based long-channel ($L_g > 5$ μm) planar transistors [21, 103] and Ni-GaSb contact resistance [104] have been reported. In Paper III, the RTA investigation of GaSb p-FETs was extended to VGAA nanowire structures, which for the first time demonstrated the post-fabrication annealing effects on such a nanoscale GaSb device. Figures 4.2a–c describe and summarize the device information from two fabricated samples with different L_g and top contact. The gate-last process enables a short channel with $L_g = 80$ nm and different top contact configuration with W/n-InAs shell/p-GaSb. It thus allows us to examine the annealing effects on different device structures.



(c)	Sample 1	Sample 2
Process sequence	Gate-first	Gate-last
Top contact	Ni/p-GaSb	W/n-InAs/p-GaSb
L_g (nm)	200	80
D_{ch} (nm)	44	35
RTA temp. (°C)	200 ~ 350	250 ~ 350

Figure 4.2: SEM image of a single nanowire GaSb p-FET from (a) sample 1 (after L_g definition) and (b) sample 2 (after high-κ deposition), respectively. (c) Details of two samples in RTA study. (d) Summary of the RTA effects on the key metrics of two samples by comparing the difference before and after RTA at 300 °C based on the mean value change of 28 devices in each sample.

The typical performance metrics were compared at different annealing temperatures for both samples and it is concluded that 300 °C is the optimal annealing temperature due to the best overall performance. With respect to as-fabricated performance, the statistical results after annealing at 300 °C in Fig. 4.2d show that the on-state performance (I_{on} and $g_{m,peak}$) is improved

after annealing in both samples while SS_{min} behaves differently. For sample 1, a noticeable reduction of R_{on} can account for the enhancement of on-state performance. This may originate from the improvement in the top contact of Ni/p-GaSb in which more Ni can alloy with GaSb during annealing thus promoting the contact quality. Moreover, the presence of forming gas, especially H_2, during annealing can passivate the channel interface by recombining with oxygen vacancies, potentially leading to lower D_{it}, which further shrinks SS_{min}. Such improvement of electrostatic control also results in better gate modulation in a way and therefore increases $g_{m,peak}$. For sample 2 with shorter L_g and complicated top contact, our results indicate that a higher thermal stability exists in the W/n-InAs/p-GaSb top contact when annealing at 300 °C as compared to Ni/p-GaSb, thereby causing negligible change of R_{on} in average. This is perhaps attributed to the non-alloy property of W, resembling Mo [74]. Despite an invariant mean value of R_{on}, there is still a slight change in individual devices where those with reduced R_{on}, the $g_{m,peak}$ increase linearly depends on the reduction in R_{on}. Therefore, the reduction of R_{on} could be the unique contribution to the $g_{m,peak}$ increase, yet leads to less improvement in percentage of $g_{m,peak}$ for sample 2 as compared to sample 1. Meanwhile, mean value of SS_{min} deteriorates dramatically after annealing. The reason could be that the gate-last process required many additional steps prior to the gate-oxide formation may introduce potential contamination which might later activate more interface traps during RTA process.

4.1.3 (In)GaAsSb CHANNEL

To mitigate the challenges posed in binary Sb-based p-type MOSFETs, a new device structure with (In)GaAsSb channel and p-type doped GaAsSb thin shell as the top contact has been explored in Paper VII (see Fig. 4.3a). Here, gate-last process was applied to keep the top contact with shell while the channel with only the (In)GaAsSb core. The corresponding transfer characteristic in Fig. 4.3b exhibits negligible DIBL and SS_{min} down to 71 mV/dec, indicating an excellent electrostatic control in the device. The I_{off} down to 1 nA/μm and $I_{on}/I_{off} > 10^4$ suggests a significant improvement off-state performance compared to GaSb channel p-FETs. Therefore, although the maximum I_D in the on-state is only 10 μA/μm, the I_{on} at I_{off} in the range of 1$\sim$100 nA/μm with V_{DS} = 0.5 V is higher than most of the reported III-V p-FETs [15,95,99,105], which allows this (In)GaAsSb channel p-FETs to work suitably in low-power systems. Nevertheless, further improvements of on-state performance can be realized by increasing the doping level of n-type InAs source and engineering the strain in the nanowire heterostructures.

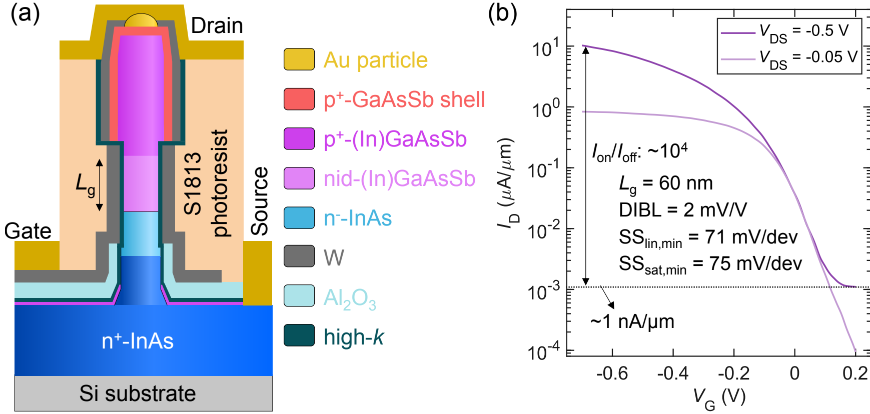


Figure 4.3: (a) Schematic of an (In)GaAsSb channel vertical nanowire p-FET with $L_g = 60$ nm. (b) Representative transfer characteristic of a single nanowire device.

4.1.4 BENCHMARKING

To present the impact of our achievements on III-V p-FETs, we benchmark the key device performance including $g_{m,peak}$, SS_{min}, and I_{on}/I_{off} as a function of L_g against other reported III-V p-FETs with various device architectures in Fig. 4.4 and Fig. 4.5. The results indicate that the fabricated GaSb p-type devices in this thesis have balanced on- and off- performance compared to the state-of-the-art III-V p-FETs. In the sub-micrometer channel regime, our devices with both GaSb and (In)GaAsSb channel exhibit the record values in terms of SS and I_{on}/I_{off} among other III-V p-FETs, exhibiting high potential for low-power applications. With the demonstrated surface pretreatment method and RTA process as well as new device channel, further downscaling in VGAA nanowire FETs and engineering of doping and strain may provide more performance enhancement for balanced III-V CMOS technologies.

4.2 InAsSb CHANNEL NANOWIRE TFETS

Owing to the flexibility of structure design using III-V materials for heterojunction by band engineering, III-V TFETs have shown device performance with sub-thermionic operation [28, 29] and substantially improved on-state performance in contrast with homojunction or Si-based TFETs [26, 109]. In Paper VIII, we have carefully modified the heterostructure at the tunnel junction to realize the major tunneling process occurring with InAsSb channel

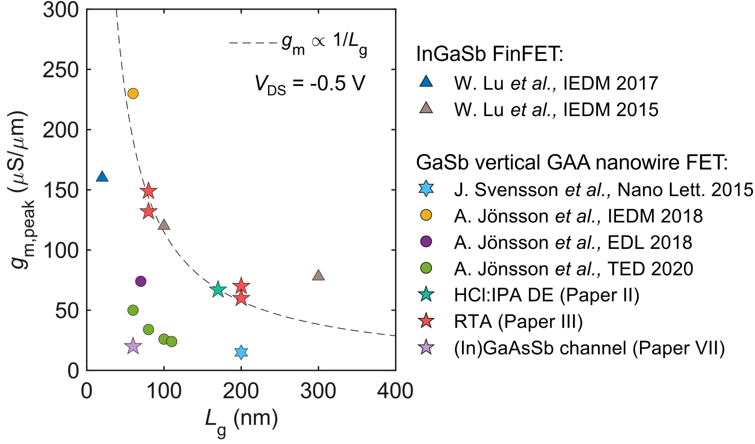


Figure 4.4: Benchmarking of III-V p-FETs with $L_g < 500$ nm by $g_{m,peak}$ vs. L_g. III-V nanowire p-FETs presented in this thesis outperform most of the devices from our earlier reports [16,17,99], in line with the state-of-the-art III-Sb p-type transistors [94] with fitting the scaling trend based on drift diffusion physics ($g_{m,peak} \sim 1/L_g$) well.

as discussed in Chapter 3. A record I_{60} (maximum I_D operating below 60 mV/dec) up to 1.3 μA/μm (Fig. 4.6a) has been achieved, meeting the requirements for circuit design based on TFETs [110]. Moreover, about 3 orders of magnitude of I_D can operate below 60 mV/dev at $V_{DS} = 0.2$ V in our device. Compared to the state-of-the-art TFET reported in IEDM-2016 [28], the result in this work shows > 4 times higher I_{60} and $\sim$30 times higher I_D with SS_{min} at $V_{DS} = 0.5$ V (Fig. 4.6a). Additionally, I_{60} is $\sim$3 times higher even at $V_{DS} = 0.2$ V than that at $V_{DS} = 0.2$ V in our previous work, meaning that a huge reduction in power consumption can be achieved in the new TFETs.

Among other recently reported TFETs with state-of-the-art on-state performance and SS < 60 mV/dec, the presented InAsSb channel TFETs reveal an substantial performance enhancement towards the best corner (Fig. 4.6b). For typical source-drain bias at 0.3 V, we have also showed the record metrics in both $g_{m,peak}$ and I_{60}, demonstrating a great promise for future low-power applications.

4.3 III-V NANOWIRE FEFETS

Due to the high electron mobility and injection velocity, InAs is a great candidate as a III-V n-channel material. The integration of ferroelectric HZO

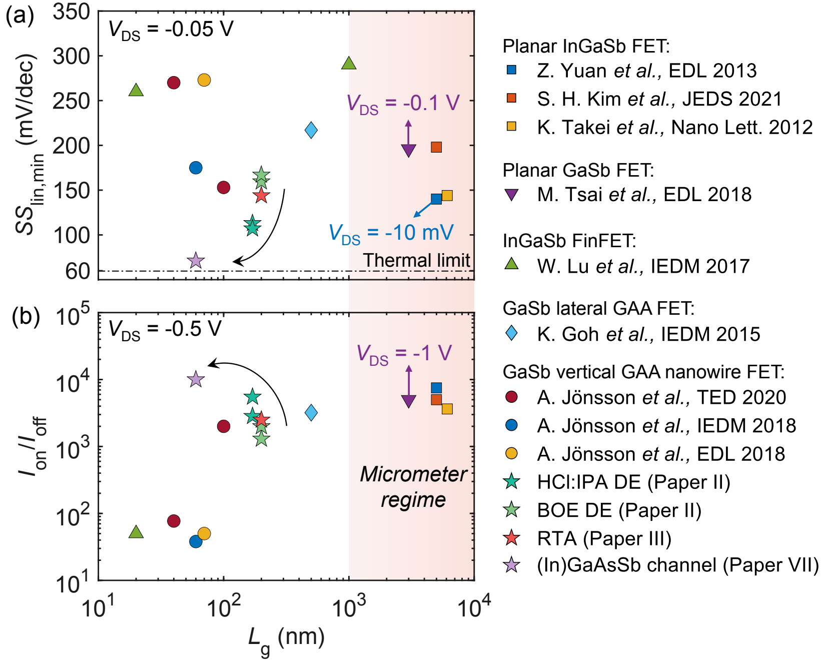


Figure 4.5: Benchmarking of III-V p-FETs by (a) $SS_{lin,min}$ and (b) I_{on}/I_{off} vs. L_g. The results achieved in this thesis reveal high competitiveness among other state-of-the-art III-V p-FETs with various device structures including planar FETs [104,106–108], FinFETs [95], LGAA FETs [15], and VGAA nanowire FETs [17,94,99]. The I_{on}/I_{off} is determined by the maximum value of V_G sweep range in specific technologies benchmarked in the figure. For our devices, I_{on}/I_{off} is determined by within $\Delta V_G < 1.5$ V. The arrow shows the trend of our approaches to gradually improve the device performance in SS and I_{on}/I_{off}.

gate on such III-V platform thus becomes critical to extend the functionality of a single transistor. In Paper IV, the first vertical nanowire III-V GAA FeFET consisting of an InAs channel and a ferroelectric HZO gate-stack has been demonstrated. The pristine transfer characteristics at various V_{DS} (Fig. 4.7a) show a comparable performance with I_{on} over 200 μA/μm, and SS down to 113 mV/dec, in line with state-of-the-art gate-first nanowire InAs transistors [113, 114]. Moreover, a small value of DIBL has been obtained, indicating a great electrostatic control in the InAs FeFET, benefiting from GAA geometry. All the above confirm that the integration processing does not degrade the transistor performance.

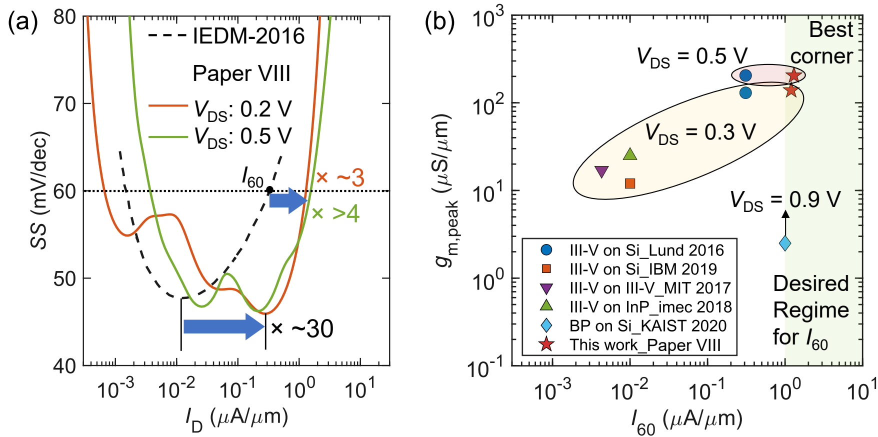


Figure 4.6: (a) SS as a function of I_D compared to state-of-the-art TFET in Ref. [28]. (b) Benchmarking of our InAsSb channel TFET against other reported TFETs with different technologies [28, 46, 75, 111, 112]. This work shows the device has not only an improved I_{60} but also a considerably high $g_{m,peak}$ = 205 μS/μm compared to other TFETs.

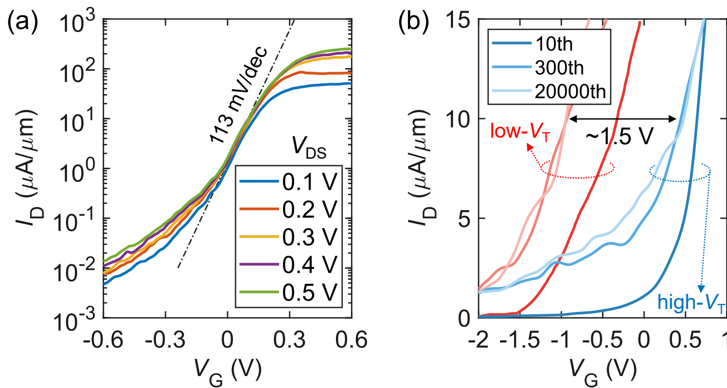


Figure 4.7: (a) Pristine transfer characteristics of the InAs FeFET at various V_{DS}. (b) Transfer characteristics of the InAs FeFET in the low-V_T and high-V_T state after 10, 300, and 20000 cycles of ferroelectric switching.

Typical transfer characteristics with ferroelectric hysteresis (measured after setting the low- or high-V_T state by applying V_P of 5 V/100 ns to the gate) of ~1.5 V was demonstrated even after 20000 switching cycles in Fig. 4.7b, suggesting a comparable endurance as in other III-V ferroelectric devices

[115,116]. The FeFET had an abrupt HZO breakdown when further employing polarization switches, which can be explained by the large planar area of ferroelectric MOS structure existing in the device (see Paper IV). A developed process scheme with a thick bottom spacer between the planar n-InAs and the gate may further improve the device endurance. Although the performance needs to be further enhanced compared to state-of-the-art Si-based FeFETs which typically showed an endurance of 10^6 cycles but up to over 10^{10} cycles with interfacial engineering [69], this proof-of-concept device indicates the potential of integrating GAA ferroelectric gate on vertical nanowire III-V platform for future applications in reconfigurable RF- and mm-wave field.

4.4 III-V NANOWIRE FERRO-TFETS

The nanowire ferro-TFET (Fig. 4.8a) is initially characterized in the pristine state before any ferroelectric switching, showing a subthermionic operation with negligible hysteresis at different V_{DS} (Fig. 4.8b). This confirms the successful integration of HZO on TFET with no evident degradation observed. The reconfigurability is verified by a state-of-the-art MW > 2 V, close to the theoretical limit with similar thickness [65]. Notably, a degradation of average SS and higher I_{off} in two states are observed after switching, which could be due to more charge trapping being involved.

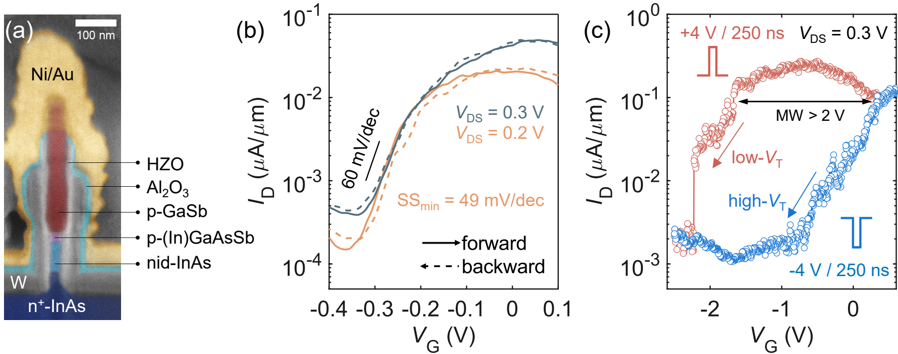


Figure 4.8: (a) Cross-sectional SEM image of a fabricated nanowire ferro-TFET. (b) Pristine transfer characteristics of the ferro-TFET with subthermionic operation with $SS_{min} = 49$ mV/dec. (c) Transfer characteristics after ferroelectric switching with two polarization states: low- and high-V_T state, reconfigured by ±4 V, respectively. The arrows indicate V_G sweeping direction.

4.4.1 RELIABILITY

Endurance and retention time are considered as two major metrics for the reliability of a memory device and have been characterized. It is found that the readout scheme influence the V_T value and thus the endurance of ferro-TFETs. A more stable V_T is obtained when applying the pulsed bias (Fig. 4.9b) for reading the state out after ferroelectric switching as compared to the case with DC bias (Fig. 4.9a), in which V_T is negatively shifted in both states while the MW degrades due to the more V_T shift in the high-V_T state over cycling. As a result, the pulsed *I-V* gives a higher endurance as V_T is almost invariant for the first ∼3000 cycles. The possible reason is that the pulsed *I-V* with faster reading process compared to the DC *I-V* measurement may mitigate the influence from charge trapping. Furthermore, the retention time of the ferro-TFET shown in Fig. 4.9c indicates that the MW slightly shrinks and stabilizes to ∼0.7 V for over at least 10^4 s at room temperature, with potential extrapolation up to over 10 years.

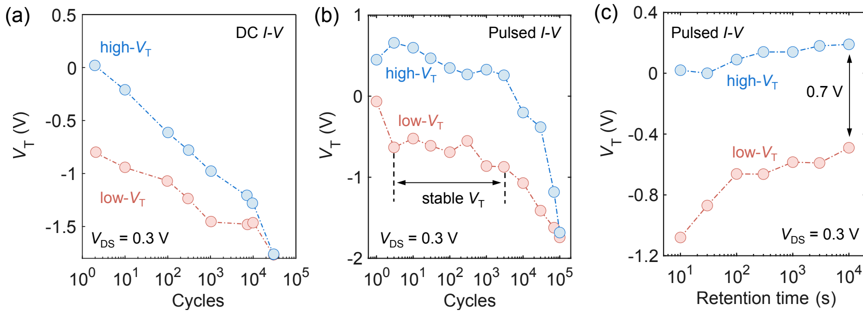


Figure 4.9: V_T as a function of ferroelectric switching cycles in different read schemes: (a) with DC *I-V* and (b) with pulsed *I-V*. A more stable V_T with higher endurance ($> 10^5$) has been observed with pulsed *I-V* readout scheme. (c) V_T as a function of retention time, indicating no MW degradation after the ferroelectric switching for at least 10^4 s.

4.4.2 INDIVIDUAL DEFECTS IN FERROELECTRIC HZO

In ultrascaled MOSFETs, the number of individual defects in the gate oxide can be limited to a small value. As a result, the potential variation induced by charge trapping/detrapping from a single defect can be visualized as I_D fluctuation in the transfer characteristic [117]. Such phenomenon can also occur in heterostructure TFETs in which the BTBT is very spatially confined and thus create a short effective channel [118]. In Paper V, similar current peaks due to individual charge trapping are observed in ferro-TFET before

and after ferroelectric switching (Fig. 4.10a). When applying a fixed V_G at which the current peak appears for sufficient time, the individual trap(s) can frequently interact with the carrier in the channel. Consequently, the charge capture/emission occurs via tunneling between oxide and the channel, resulting in two distinct current levels over time, as seen in Fig. 4.10b. This time-dependent current fluctuation is called *Random Telegram Noise* (RTN).

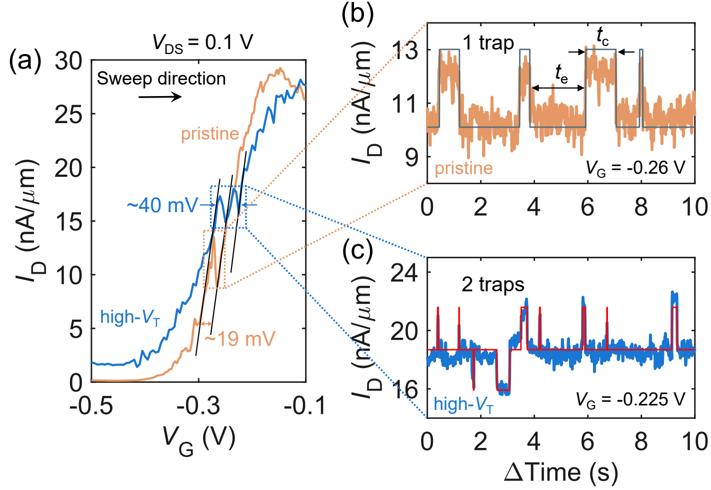


Figure 4.10: Individual defects with RTN. (a) Transfer characteristics before (pristine) and after ferroelectric switching in the high-V_T state. Excerpt of the corresponding RTN measurement (b) before and (c) after ferroelectric switching at similar I_D with indicated V_G. Two current levels were observed in the pristine case while three current levels in the case after switching. The indicated $t_{c/e}$ denotes the capture/emission time of a trap.

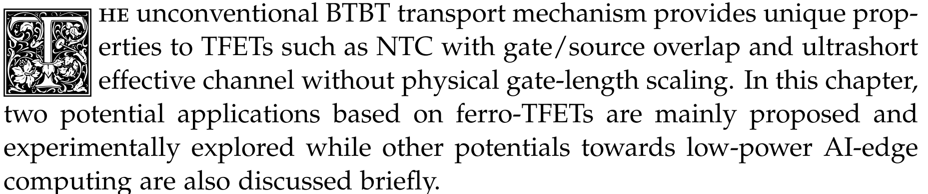
When the trapped charge is emitted to the channel and contributes to the transport process, a higher I_D is obtained. On the contrary, when the trap captures a charge from the channel, I_D decreases. The probability of charge capture/emission is defined as $1/\tau_{c/e}$ where $\tau_{c/e}$ is the characteristic capture/emission time constant which is obtained by fitting the time distribution in the high/low current level with an exponential function $f(t_{c/e}) = \tau_{c/e}^{-1}\exp(-t_{c/e}/\tau_{c/e})$. By repeating the RTN measurements at various V_G, a set of τ_c and τ_e can be obtained. If assuming all the traps are charged below the Fermi level of the channel ($E_{F,ch}$), one can determine that the trap energy level aligns with $E_{F,ch}$ at the condition of $\tau_c = \tau_e$ (see Paper V).

After the ferroelectric switching, three-current-level RTN is obtained at fixed V_G in Fig. 4.10c. This can be interpreted as one more trap is activated

due to the ferroelectric switching process, in agreement with the corresponding transfer curve where two peaks appear in Fig. 4.10a. Compared to the width of V_G shift ($\sim$19 mV) due to the current peak before switching, the one after switching shows almost exactly doubled value ($\sim$40 mV), confirming two individual defects involved. Further evidence in another device shows that more traps are generated after ferroelectric switching cycle by cycle but the width of the current peak maintains an integer multiple of $\sim$19 mV. The continuous generation of new individual traps with switching cycles may originate from the imperfection in thermally ALD-deposited HZO film and the degraded semiconductor/oxide interface after RTA process.

5

Applications of ferro-TFETs



THE unconventional BTBT transport mechanism provides unique properties to TFETs such as NTC with gate/source overlap and ultrashort effective channel without physical gate-length scaling. In this chapter, two potential applications based on ferro-TFETs are mainly proposed and experimentally explored while other potentials towards low-power AI-edge computing are also discussed briefly.

5.1 SINGLE DOMAIN DETECTION

Detection of single domain switching in scaled ferroelectric materials provides a way to for understand the fundamental limits and domain dynamics of ferroelectronics. Downscaling the channel length of a FeFET to the size of a single domain in the ferroelectric gate has been demonstrated as an electrical method to sense the single domain switching with abrupt V_T shift in the FeFETs [119].

5.1.1 EFFECTIVE SHORT CHANNEL IN TFETs

In accordance with the Wentzel-Kramers-Brillouin (WKB) approximation, the on-state transmission probability exponentially depends on the electric field ε along the tunnelling direction [109, 120], which approximately has inverse proportion with the electrostatic scaling length λ ($\varepsilon \sim 1/\lambda$). Therefore, the BTBT process (or the tunneling current) is extremely sensitive to the region within λ (Fig. 5.1a) although a long physical L_g is typically used in TFETs to mitigate the source-drain tunneling thereby improving the off-state performance [120].

For nanowire GAA FETs, the channel diameter (d_{ch}), the gate oxide thickness (t_{ox}), and the corresponding relative permittivity ϵ_{ch} and ϵ_{ox} can influence λ [121] which can be given as below by an analytical model based on 1D modified Poisson equation for electrostatics solving for III-V TFETs [122]:

$$\lambda = \sqrt{(\epsilon_{ch}/4\epsilon_{ox})t_{ox}d_{ch}}, \; d_{ch}/2 \gg t_{ox}. \tag{5.1}$$

In Paper V, $t_{ox} = t_{HZO} = 13$ nm which can be translated to the equivalent oxide thickness (EOT) of 1.4 nm by using the coaxial capacitance model and considering the channel as a cylinder for C_{ox}. Thus, this fulfils the condition $d_{ch}/2 \gg t_{ox}$, and λ is calculated to 5.7 nm with $d_{InAs} = 23$ nm (Fig. 5.1b), which is considerably shorter than the grain size in HZO film (typically similar as the film thickness, i.e., 13 nm [123]). This means that the potential variation within λ contributes the most to the tunneling current. For example in Fig. 5.1a, domain B which is the closest to the heterojunction has the highest electrostatic controllability for tunneling. Thus, the tunneling current of the ferro-TFET is only sensitive to the polarization of domain B rather than the other domains (A, C, or D). By further downscaling the channel diameter and the ferroelectric film, a domain with size towards sub-nanometer can be sensed by the ferro-TFET in principle (Fig. 5.1b). Therefore, TFETs can provide an electrical method to potentially sense the single domain switching in ultrascaled ferroelectrics without physical L_g miniaturization.

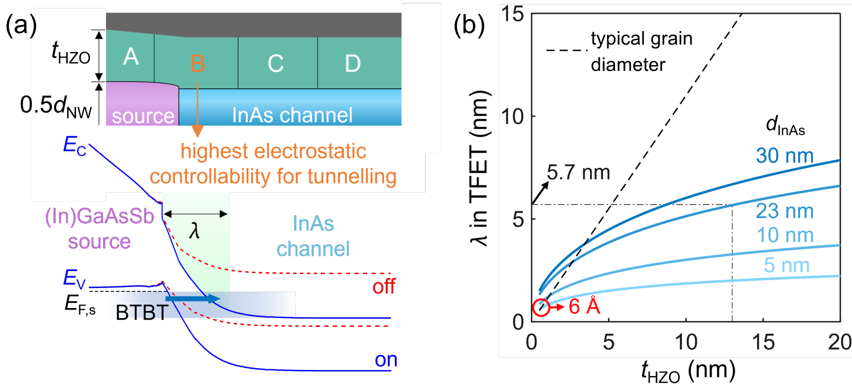


Figure 5.1: (a) Schematic of the gate-stack and the corresponding band diagram in the tunnel junction region of the ferro-TFET. A, B, C, and D denote single ferroelectric domains. (b) λ scaling as a function of t_{HZO}.

5.1.2 CHARACTERIZATION OF SINGLE DOMAIN SWITCHING

Electrical verification of single domain switching is experimentally implemented in both DC and pulsed *I-V* measurement. The first evidence is observed in DC-swept transfer characteristic in the low-V_T state where a super-steep region appears (Fig. 5.2a). This can be interpreted as the polarization of a single domain switched when V_G reaches the coercive voltage during the DC sweep, which has been found also in ultrascaled FeFETs [124]. As discussed, the domain closest to the tunnel junction can govern the tunneling current and thus when its polarization is switched from *DOWN* to *UP*, the current can be abruptly reduced due to BTBT prohibition (see diagram in Fig. 5.2b). As a result, a super-steep region with ultralow SS can be achieved (Fig. 5.2b). To validate the single domain switching, a measurement scheme that can separate the ferroelectric switching and charge trapping has been designed and elaborated in Paper V.

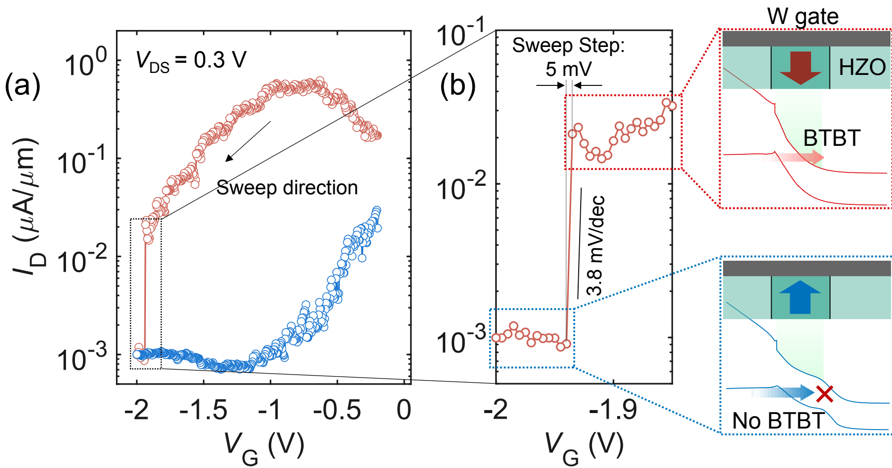


Figure 5.2: Super steep switching in ferro-TFETs with DC *I-V* reading scheme. (a) Transfer characteristics of two polarization states by applying V_P with ±4 V/250 ns. (b) Zoom-in super-steep region of the transfer curve in the low-V_T state with corresponding schematics indicating two polarization states and band diagrams.

To further confirm the single domain switching in ferro-TFETs, pulsed *I-V* measurements with progressively increasing pulse width (t_{pulse}) of the writing scheme (inset of Fig. 5.3a) are carried out. The pulsed *I-V* read scheme can avoid the super-steep switching while reading out the state due to the fast voltage pulse [124]. Unlike FeFETs with long channels [125], an abrupt V_T

shift rather than analog change is observed (Fig. 5.3a) at various V_P, in line with other reported short-channel FeFETs [119].

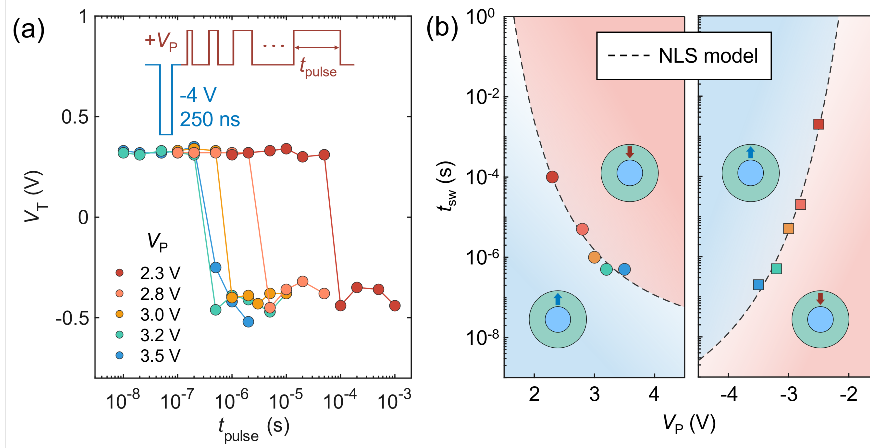


Figure 5.3: Pulsed I-V measurements of single domain switching. (a) V_T with varying t_{pulse} of the pulse scheme (inset) at different V_P. (b) The extracted required switching time t_{sw} as a function of pulse amplitude V_P, fitting well with the nucleation-limited switching model. Two polarization states are separated by the region with different colors and the schematic of the ferro-TFET cross-section (inset).

In thin ALD-deposited ferroelectric HZO films, the nucleation process takes longer than the domain wall (DW) migration as the distance that DWs can move is very limited. Hence, the nucleation-limited switching (NLS) model is more suitable to describe the switching dynamics in thin polycrystalline ferroelectric films [61,119]. Although the individual domains might be single crystal, the DW migration is still limited by the small grain size. Based on the above, the NLS model is utilized to investigate the switching dynamics in ferro-TFETs, which typically gives a relation of required switching time (t_{sw}) and the applied V_P:

$$t_{sw} = t_0 \exp\left(\frac{\alpha}{k_B T} \frac{1}{V_P^2}\right) \tag{5.2}$$

where t_0, α, k_B, and T denote minimum nucleation/switching time, the exponential coefficient associated with the material properties, Boltzmann constant, and temperature, respectively. The result in Fig. 5.3b indicates NLS model fitting well with the t_{sw}-V_P relation in ferro-TFETs.

5.2 RECONFIGURABLE SIGNAL MODULATION

Adding reconfigurability to analog devices and circuits gains interests because of the increase in functionality per unit area in such area- and power-hungry system, which may eventually reduce the cost due to the low-power and simplified circuit design. Recently, ambipolar transistors combined with either back-gate [126] or ferroelectric gate-stack [125] have been demonstrated for desired single-transistor reconfigurable analog signal modulation. This section demonstrates a new type of reconfigurable transistors based on ferro-TFETs for analog application with reduced supply voltage and device area as compared to other reported device architectures with the same functionality.

5.2.1 RECONFIGURABLE NTC

As discussed in Chapter 2, a parabolic transfer characteristic with NTC can be obtained in TFETs by using gate/source overlap structure. Such NTC feature remains when integrating with HZO ferroelectric gate-stack, realizing reconfigurable NTC in ferro-TFET as shown in Fig. 5.4. The slightly uneven peak current in the two states may be caused by the different impact from the gate polarization on the source and channel region. This perhaps further change the factors which determine the maximum tunneling current, such as the height and width of the tunnel barrier, and the density-of-states in the source segment.

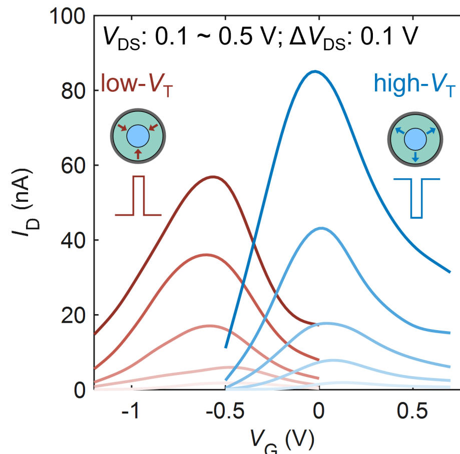


Figure 5.4: Transfer characteristics with NTC in the gate/source overlapped ferro-TFET under two polarization states .

5.2.2 PROGRAMMABLE MODULATION MODES

By properly programming the ferroelectric gate in the ferro-TFET, low- and high-V_T state can be achieved as illustrated in Fig. 5.5, leading to reconfigurable signal modulation without changing the DC offset of the input analog signal. This simplifies the operation scheme compared to conventional cases [127]. In the high-V_T state, the input signal (v_{in}) operates in the positive g_m branch of the transfer curve and thus signal follower can be achieved; whereas in the low-V_T state, v_{in} oscillates near the current peak, and thus each semi-cycle of (A–B–C or C–D–E) leads to a full cycle (A–B–C) in the output waveform of I_D, realizing frequency doubling. In Paper VI, such reconfigurable signal modulation has been demonstrated in a single ferro-TFET and also implemented in a simple circuit with a pull-down load resistor (R) as shown in Fig. 5.6. Moreover, other signal reconfigurable signal modulation including 180°-phase shifter and frequency mixer (with two frequencies summed in the input signal) can be achieved in the same ferro-TFET (Paper VI).

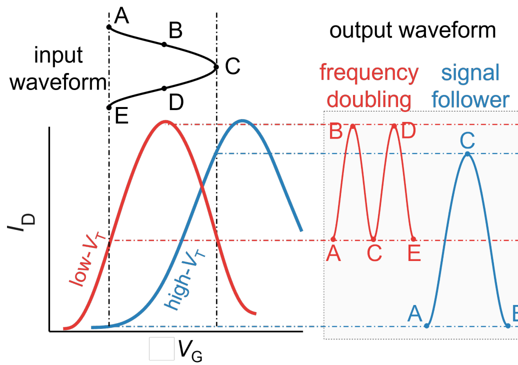


Figure 5.5: Working principle for reconfigurable signal modulation in the ferro-TFET. Either signal follower or frequency doubling can be realized under different polarization states.

Compared to conventional CMOS-based frequency doublers or mixers where a large device/circuit area and high drive voltage are typically needed, the demonstrated single ferro-TFET solution benefits from its significantly reduced footprint and drive voltage while remaining high spectral purity with above 90% power concentrating on the desired frequencies (Paper VI), leading to high area and energy efficiency. Meanwhile, the reconfigurability in the device by integrating the ferroelectric gate increases the functionality of a single transistor, in line with the future hyper-scaling strategy.

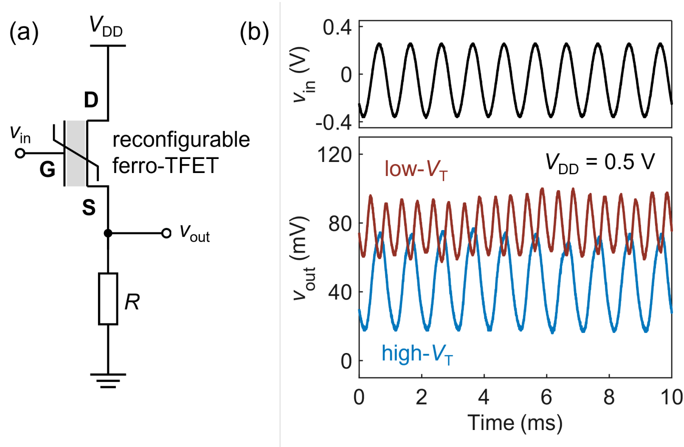


Figure 5.6: Experimental demonstration of reconfigurable signal modulation with a single ferro-TFET. (a) The schematic of measurement circuit for output voltage (V_{out}) waveform. The load resistor $R_L = 8$ MΩ. (b) Transient V_{in}-V_{out} waveform in two different signal modulation modes.

5.3 OTHER POTENTIAL APPLICATIONS

The reconfigurable NTC behavior can be further extrapolated for reconfigurable FETs in which the polarity (n- or p-type) can be switched. Within the certain operation region of V_G (e.g., –0.6 to 0.2 V in Fig. 5.4), the low-V_T state exhibits p-type feature while the high-V_T state shows n-type. This reconfigurable polarity in ferro-TFETs can be used for hardware security where the true function of the transistor is hidden to avoid reverse engineering [128], and XNOR operation in self-activated in-memory computing [129]. In addition, the single domain switching in ferro-TFETs may lead to a probability-based switching model which is useful in hardware-based true random number generators [130]. Although the performance including endurance and I_{on}/I_{off} after ferroelectric switching needs to be further improved, the major advantages of using ferro-TFETs for the above applications are the low power operation and high density package with vertical nanowire geometry, which are critical concerns for future electronics.

6

Summary and Outlook

This thesis has investigated the strategies to improve the performance of vertical GAA III-V nanowire transistors mainly focusing on III-Sb-based p-FETs and heterostructure TFETs. Besides, the integration of HfO_2-based ferroelectric gate-stack on vertical III-V nanowire FETs and TFETs with GAA device architecture has been, for the first time, demonstrated. Further study on III-V ferro-TFETs including fundamental device physics and potential reconfigurable applications has been explored. The performance achieved by these devices holds great promise for low-power logic and reconfigurable applications.

Given various device functions, the papers appended in the end of this thesis can be classified as the following: 1) III-V p-FETs (Paper I–III, VII); 2) III-V heterostructure TFETs (Paper VIII); 3) III-V FeFETs and ferro-TFETs (Paper IV–VI). The contribution of this thesis mainly covers the design and modeling of new device structures and the development of fabrication schemes to enhance performance. The elaborated summary in different devices is discussed below:

III-V p-FETs

In Paper I, a GaSb-GaAsSb core-shell nanowire structure has been demonstrated and an axial compressive strain up to 0.92% in the GaSb core along the transport direction in the nanowire has been achieved by carefully engineering the As composition and thickness of the GaAsSb shell. Such high axial compressive strain potentially leads to enhancement of hole mobility in GaSb, thus improving the p-FET performance.

In Paper II and III, two processing approaches including using DE scheme as channel surface pretreatment and post-fabricated RTA have been applied

to GaSb vertical nanowire p-FETs, respectively. By employing the alcohol-based HCl as the DE etchant (Paper II), improved quality of channel surface with suppression of both Ga and Sb oxide states was achieved, which was confirmed by XPS characterization. The corresponding transistors exhibited SS down to 107 mV/dec, lower than that in other reported GaSb p-FETs. Moreover, the on-state performance including $g_{\mathrm{m,peak}}$ (up to 150 μS/μm) and I_{on} (up to $\sim$100 μA/μm) has been enhanced by $\sim$ 50% after RTA in a forming gas ambient at 300 °C with various L_{g} (Paper III).

In Paper VII, a novel device structure with (In)GaAsSb channel has been demonstrated for further improving the off-state performance in p-FETs with SS down to 71 mV/dec, which is the lowest SS among all reported III-V p-FETs. The I_{off} was reduced down to 1 nA/μm at $V_{\mathrm{DS}} = 0.5$ V, which meets the requirement of low-power circuit applications. Due to the excellent electrostatic control, the corresponding I_{on} at $I_{\mathrm{off}} = 1$ nA/μm reached 3 μA/μm with $I_{\mathrm{on}}/I_{\mathrm{off}} = 3000$ with V_{DD} swing of 0.5 V.

III-V Heterostructure TFETs

In Paper VIII, by fine-tuning the heterostructure at the tunnel junction, vertical nanowire TFETs with a new device structure have been grown and fabricated. The electrical results showed a substantial improvement in I_{60} which reached a record value with $> 1\mu$A/μm. In addition, a high $g_{\mathrm{m,peak}}$ >200 μS/μm as well as a low SS down to 43 mV/dec have been achieved in the same device. These metrics indicate that the performance of III-V heterostructure TFETs can be enhanced by carefully designing the structure and still attractive for future low-power applications.

III-V FeFETs and ferro-TFETs

In Paper IV, the first demonstration of HZO ferroelectric gate-stack integrating on vertical InAs nanowire MOSFETs has been shown as the proof-of-concept experimental verification of III-V vertical GAA FeFETs. A stable memory window of $\sim$1.5 V for about 10^4 switching cycles and long retention time with extrapolation up to 10 years have been achieved in the device.

In Paper V, further investigation based on the same integration processing from InAs FeFETs, ferro-TFETs have been demonstrated with steep slope (49 mV/dec) in the pristine state and a great memory window >2 V between two ferroelectric states. This ferro-TFET can also sense the single domain switching in the ultra-scaled ferroelectric film due to its BTBT mechanism. Furthermore, in Paper VI, unique near-parabolic transfer characteristic due to the gate/source overlap structure in ferro-TFETs has been shown for analog

signal modulation with reconfigurability originating from the ferroelectric polarization in the gate-stack. This potentially provides a novel device variant for high-density, low-power, and multiple-function analog/mix signal circuits.

Outlook for ferro-TFETs

The unique properties existing in ferro-TFETs unveil many promising applications. Therefore, further investigations on such devices could be of tremendous interests. On one hand, further exploration of device physics such as ferroelectric switching dynamics at various temperatures and low-frequency noise behavior in ferro-TFETs is critical for understanding the interference between charge trapping and ferroelectric switching at nanoscale device level. On the other hand, structure modification including scaling of the thickness and Zr composition in HZO film and the effects of inter-layer between HZO and the channel can be further investigated. The above two research paths may generate new understanding of this device, thus providing unexpected applications for different systems.

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APPENDICES

A

Nanowire Epitaxy Recipes

In this appendix, detailed steps of nanowire growth by MOVPE will be provided. The recipes mainly cover the growth for InAs/(In)GaAsSb/GaSb nanowire TFETs which include the growth of InAs nanowire n-MOSFETs and GaSb nanowire p-MOSFET (basically the same structure but without the middle quaternary segment). The shell growth details in GaSb-GaAsSb core-shell nanowires (Paper I) will be also included. A cleaning process with HCl gas is typically needed after Sb-involved growth. Due to the nanowire growth initialization with InAs, an InAs cover run is also used prior to the desired nanowire growth. The details of these preparation process, however, will not be included in in this appendix.

Growth recipe for InAs/(In)GaAsSb/GaSb nanowires

- **General reactor settings**
  1. Reactor pressure: 100 mbar;
  2. Total flow: 8000 sccm.
- **InAs nanowire growth**
  1. Pregrowth annealing at 481 °C in AsH_3 with molar fraction of $X_{AsH_3} = 2.5 \times 10^{-3}$ for 5 min;
  2. Set growth temperature at 461 °C;
  3. Set precursor flows of the growth: $X_{TMIn} = 6.1 \times 10^{-6}$, $X_{AsH_3} = 1.25 \times 10^{-4}$, $X_{TESn} = 3.1 \times 10^{-5}$;
  4. Switch AsH_3 to the growth flow and open TMIn and TESn;
  5. Grow Sn-doped InAs nanowire for 100 s;
  6. Close TESn to grow undoped InAs nanowire for 40 s.

- **(In)GaAsSb nanowire growth**
    1. Close TMIn and change AsH_3 flow to $X_{AsH_3} = 2.5 \times 10^{-3}$ to purge In from Au droplets for 3 min;
    2. Close AsH_3 and simultaneously open TMIn for 5 s;
    3. Close TMIn but simultaneously open AsH_3 with $X_{AsH_3} = 2.72 \times 10^{-5}$ and TMSb with $X_{TMSb} = 1.3 \times 10^{-4}$ for 8 s;
    4. Open TMGa with $X_{TMGa} = 4.9 \times 10^{-5}$ and DEZn with $X_{DEZn} = 1.7 \times 10^{-5}$ for 25 s (here Zn/Ga = 0.35, but can be varying according to the demand).

- **GaSb nanowire growth**
    1. Set growth temperature to 515 °C and TMSb flow to $X_{TMSb} = 6.5 \times 10^{-5}$ in 3 min;
    2. Close AsH_3 to grow Zn-doped GaSb nanowire while heating up;
    3. When the temperature reaches the target (515 °C), continue to grow GaSb for 420 s.

- **Cooling down**
    1. Close all precursors and steadily cool down the reactor in AsH_3 until 300 °C;
    2. Reset all the parameters and cool down the system to 50 °C.

GaAsSb shell growth in GaSb-GaAsSb core-shell nanowires

Due to almost identical core structure to the previous growth scheme but without (In)GaAsSb segment or dopants, the recipe below starts with the only shell growth.

- **Settings of growth parameters**
    1. Growth temperature: 515 °C;
    2. Precursor flow: $X_{TMGa} = 4.9 \times 10^{-5}$, $X_{TMSb} = 7.76 \times 10^{-5}$, $X_{AsH_3} = 1.88 \times 10^{-5}$. Here, the flow of TMSb and AsH_3 is adjustable to achieve desired composition;
- **Growth procedure**
    1. Close TMGa and TMSb;
    2. Lower TMSb flow for the shell growth in 20 s;
    3. Wait 30 s for stabilization of TMSb flow;
    4. Open TMGa, TMSb, and AsH_3 for the shell growth for desired time;
    5. Close all precursors and cool down the system;
    6. Reset all the parameters.

B Fabrication Steps of Vertical Nanowire Transistors

This appendix contains details of vertical processing steps for nanowire transistors excluding the growth, mainly including two schemes: 1) gate-first and 2) gate-last process. A slightly different version based on gate-first process for ferro-TFETs is also provided mainly focusing on the HZO etch and RTA steps.

Gate-first processing

For GaSb p-MOFETs and TFETs with all inorganic spacers (without shell):

- **High-κ and first spacer formation**
  1. Oxidize the sample in O_2 ambient at 50 °C for 8 min;
  2. Wet etch in HCl:IPA (1:10) (or BOE 30:1) for 30 s and rinse in IPA (or DI water) for 1 min;
  3. Sequentially deposit 5-cycle Al_2O_3 at 300 °C, 27-cycle HfO_2 at 120 °C, and 200-cycle Al_2O_3 at 120 °C by ALD to form the high-κ and first spacer;
  4. Bake on the hot plate at 120 °C for 2 min;
  5. Spincoat s1813 at 4000 rpm for 1 min ;
  6. Bake on the hot plate at 120 °C for 15 min with lid;
  7. RIE dry etch s1813 in O_2 plasma with RF power of 75 or 50 W until the desired thickness which can be verified in SEM;
  8. Wet etch Al_2O_3 in BOE 30:1 for 35 s (etch rate: 0.6 nm/s) and rinse in DI water for 1 min.
- **Gate length and gate pad definition**
  1. Sputter 60-nm W with DC power of 100 W and Ar flow of 16 sccm;
  2. Bake on the hot plate at 120 °C for 2 min;

3. Spincoat s1813 at 4000 rpm for 1 min ;
4. Bake on the hot plate at 120 °C for 15 min with lid;
5. RIE dry etch s1813 in O_2 plasma with RF power of 75 or 50 W until the desired thickness which can be verified in SEM;
6. RIE dry etch sidewall W in SF_6/Ar plasma with total pressure of 185 Torr;
7. Clean the sample with O_2 plasma for 45 s;
8. Remove s1813 using Acetone at 65 °C for 5 min and rinse in IPA;
9. Bake on the hot plate at 115 °C for 2 min;
10. Spincoat s1813 at 4000 rpm for 1 min ;
11. Bake on the hot plate at 115 °C for 90 s;
12. Expose in soft-UV light for 4.5 s with designed gate pad pattern;
13. Develop in MF319 for 80 s and rinse in DI water for 1 min;
14. Bake on the hot plate at 120 °C for 15 min with lid;
15. RIE dry etch planar W in SF_6/Ar plasma with total pressure of 185 Torr;
16. Clean the sample with O_2 plasma for 45 s.

- **High-κ length definition and top spacer**
  1. Bake on the hot plate at 120 °C for 2 min;
  2. Spincoat s1813 at 4000 rpm for 1 min ;
  3. Bake on the hot plate at 120 °C for 15 min with lid;
  4. RIE dry etch s1813 in O_2 plasma with RF power of 75 or 50 W until the desired thickness which can be verified in SEM;
  5. Wet etch 3-nm HfO_2 in HF 1:400 for 215 s and rinse in DI water for 1 min;
  6. Remove s1813 using Acetone at 65 °C for 5 min and rinse in IPA;
  7. Deposit 110-cycle Al_2O_3 at 120 °C in ALD for the top spacer.

- **Via opening**
  1. Bake on the hot plate at 115 °C for 2 min;
  2. Spincoat s1813 at 4000 rpm for 1 min ;
  3. Bake on the hot plate at 115 °C for 90 s;
  4. Expose in soft-UV light for 5.5 s with designed pattern of vias;
  5. Develop in MF319 for 80 s and rinse in DI water for 1 min;
  6. Bake on the hot plate at 120 °C for 15 min with lid;
  7. Wet etch in HF 1:400 for 315 s (etch rate for Al_2O_3: 0.3 nm/s) and rinse in DI water for 1 min;
  8. Remove s1813 using Acetone at 65 °C for 5 min and rinse in IPA.

- **Top contact definition and metallization**

1. Bake on the hot plate at 120 °C for 2 min;
2. Spincoat s1813 at 4000 rpm for 1 min ;
3. Bake on the hot plate at 120 °C for 15 min with lid;
4. RIE dry etch s1813 in O_2 plasma with RF power of 75 or 50 W until the desired thickness which can be verified in SEM;
5. Wet etch Al_2O_3 in BOE 30:1 for 25 s and rinse in DI water for 1 min;
6. Remove s1813 using Acetone at 65 °C for 5 min, rinse in IPA;
7. Sputter 10-nm/200-nm Ni/Au with DC power of 100 W and Ar flow of 9 sccm;
8. Bake on the hot plate at 115 °C for 2 min;
9. Spincoat s1813 at 4000 rpm for 1 min ;
10. Bake on the hot plate at 115 °C for 90 s;
11. Expose in soft-UV light for 5 s with designed pattern of metal pads;
12. Develop in MF319 for 80 s and rinse in DI water for 1 min;
13. Bake on the hot plate at 120 °C for 15 min with lid;
14. Clean the sample with O_2 plasma for 45 s;
15. Wet etch Au in $KI:I_2:H_2O$ (1:2:17) for 25 s and rinse in DI water;
16. Remove s1813 using Acetone at 65 °C for 5 min and rinse in IPA;
17. Clean the sample with O_2 plasma for 30 s;
18. Wet etch Ni in $CH_3COOH:HNO_3:H_2SO_4:H_2O$ (2.5:2.5:1:15) for 100 s and rinse in DI water.

For InAs FeFETs and ferro-TFET, the processing is almost identical but slightly modified to adapt to HZO etch and crystallization for ferroelectricity. The difference is that crystallized HZO cannot be etched by HF while amorphous HZO can be etched by HF.

- **Bottom contact via opening and HZO etch**
  1. Bake on the hot plate at 115 °C for 2 min;
  2. Spincoat s1813 at 4000 rpm for 1 min ;
  3. Bake on the hot plate at 115 °C for 90 s;
  4. Expose in soft-UV light for 5.5 s with designed pattern of bottom contact vias;
  5. Develop in MF319 for 80 s and rinse in DI water for 1 min;
  6. Bake on the hot plate at 120 °C for 15 min with lid;
  7. Wet etch in HF 1:400 for 20 min and rinse in DI water for 1 min;
  8. Remove s1813 using Acetone at 65 °C for 5 min and rinse in IPA.
- **Sidewall HZO etch and RTA for HZO crystallization**

1. Bake on the hot plate at 120 °C for 2 min;
2. Spincoat s1813 at 4000 rpm for 1 min ;
3. Bake on the hot plate at 120 °C for 15 min with lid;
4. RIE dry etch s1813 in O_2 plasma with RF power of 75 or 50 W for HZO height definition to expose the top contact region;
5. Wet etch nanowire sidewall HZO in HF 1:400 for 12 min and rinse in DI water for 1 min;
6. Remove s1813 using Acetone at 65 °C for 5 min and rinse in IPA;
7. RTA at 450–550 °C in N_2 ambient for 30 s.

After that, the following steps are the same as the above gate-first processing.

Gate-last processing

For GaSb and (In)GaAsSb-channel p-MOFETs with thin shell, gate-last processing is used, starting with the top contact (which are given as below) and the rest steps are the same as the above gate-first processing.

- **Top contact and DE of the channel**
  1. Deposit 200-cycle Al_2O_3 at 120 °C by ALD as protection layer;
  2. Bake on the hot plate at 120 °C for 2 min;
  3. Spincoat s1813 at 4000 rpm for 1 min ;
  4. Bake on the hot plate at 120 °C for 15 min with lid;
  5. RIE dry etch s1813 in O_2 plasma with RF power of 75 or 50 W for top contact definition;
  6. Wet etch exposed Al_2O_3 in BOE 30:1 for 35 s and rinse in DI water for 1 min;
  7. Sputter 30-nm W with DC power of 100 W and Ar flow of 16 sccm;
  8. ICP-RIE dry etch planar W for 65 s in SF_6/N_2 with RF power of 300 W and pressure of 5 Torr;
  9. RIE dry etch s1813 in O_2 plasma with RF power of 50 W for 100 s;
  10. Wet etch Al_2O_3 in BOE 30:1 for 35 s and rinse in DI water for 1 min;
  11. Remove s1813 using Acetone at 65 °C for 5 min and rinse in IPA;
  12. Wet etch in HCl:IPA (1:10) for 30 s and rinse in IPA for 1 min;
  13. Oxidize in O_3 ambient at 50 °C for 30 s;
  14. Wet etch the entire shell and oxide layer of the channel in HCl:IPA (1:10) for 30 s and rinse in IPA for 1 min;
  15. Sequentially deposit 5-cycle Al_2O_3 at 300 °C and 27-cycle HfO_2 at 120 °C by ALD to form the high-κ;
  16. Sputter 60-nm W with DC power of 100 W and Ar flow of 16 sccm.