Reconfigurable Receiver Front-Ends for Advanced Telecommunication Technologies

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Reconfigurable Receiver Front-Ends for Advanced Telecommunication Technologies

Doctoral Thesis

Iman Ghotbi

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Title: Reconfigurable Receiver Front-Ends for Advanced Telecommunication Technologies

Abstract:

The exponential growth of converging technologies, including augmented reality, autonomous vehicles, machine-to-machine and machine-to-human interactions, biomedical and environmental sensory systems, and artificial intelligence, is driving the need for robust infrastructural systems capable of handling vast data volumes between end users and service providers. This demand has prompted a significant evolution in wireless communication, with 5G and subsequent generations requiring exponentially improved spectral and energy efficiency compared to their predecessors. Achieving this entails intricate strategies such as advanced digital modulations, broader channel bandwidths, complex spectrum sharing, and carrier aggregation scenarios. A particularly challenging aspect arises in the form of non-contiguous aggregation of up to six carrier components across the frequency range 1 (FR1). This necessitates receiver front-ends to effectively reject out-of-band (OOB) interferences while maintaining high-performance in-band (IB) operation. Reconfigurability becomes pivotal in such dynamic environments, where frequency resource allocation, signal strength, and interference levels continuously change. Software-defined radios (SDRs) and cognitive radios (CRs) emerge as solutions, with direct RF-sampling receivers offering a suitable architecture in which the frequency translation is entirely performed in digital domain to avoid analog mixing issues. Moreover, direct RF-sampling receivers facilitate spectrum observation, which is crucial to identify free zones, and detect interferences.

Acoustic and distributed filters offer impressive dynamic range and sharp roll-off characteristics, but their bulkiness and lack of electronic adjustment capabilities limit their practicality. Active filters, on the other hand, present opportunities for integration in advanced CMOS technology, addressing size constraints and providing versatile programmability. However, concerns about power consumption, noise generation, and linearity in active filters require careful consideration.

This thesis primarily focuses on the design and implementation of a low-voltage, low-power RFFE tailored for direct sampling receivers in 5G FR1 applications. The RFFE consists of a balun low-noise amplifier (LNA), a Q-enhanced filter, and a programmable gain amplifier (PGA). The balun-LNA employs noise cancellation, current reuse, and g_m boosting for wideband gain and input impedance matching. Leveraging FD-SOI technology allows for programmable gain and linearity via body biasing. The LNA's operational state ranges between high-performance and high-tolerance modes, which are apt for sensitivity and blocking tests, respectively. The Q-enhanced filter adopts noise-cancelling, current-reuse, and programmable G_m-cells to realize a fourth-order response using two resonators. The fourth-order filter response is achieved by subtracting the individual response of these resonators. Compared to cascaded and magnetically coupled fourth-order filters, this technique maintains the large dynamic range of second-order resonators. Fabricated in 22-nm FD-SOI technology, the RFFE achieves 1%-40% fractional bandwidth (FBW) adjustability from 1.7 GHz to 6.4 GHz, 4.6 dB noise figure (NF) and an OOB third-order intermodulation intercept point (IIP3) of 22 dBm. Furthermore, concerning the implementation uncertainties and potential variations of temperature and supply voltage, design margins have been considered and a hybrid calibration scheme is introduced. A combination of on-chip and off-chip calibration based on noise response is employed to effectively adjust the quality factors, G_m-cells, and resonance frequencies, ensuring desired bandpass response. To optimize and accelerate the calibration process, a reinforcement learning (RL) agent is used.

Anticipating future trends, the concept of the Q-enhanced filter extends to a multiple-mode filter for 6G upper mid-band applications. Covering the frequency range from 8 to 20 GHz, this RFFE can be configured as a fourth-order dual-band filter, two bandpass filters (BPFs) with an OOB notch, or a BPF with an IB notch. In cognitive radios, the filter's transmission zeros can be positioned with respect to the carrier frequencies of interfering signals to yield over 50 dB blocker rejection.

Key words: 5G, Receiver, Filter, Low-noise amplifier, FD-SOI, Calibration.

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Iman Ghotbi

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Furthermore, concerning the implementation uncertainties and potential variations of temperature and supply voltage, design margins have been considered and a hybrid calibration scheme is introduced. A combination of on-chip and off-chip calibration schemes is employed to effectively adjust the quality factors, G_m-cells, and resonance frequencies, ensuring desired bandpass response. To optimize and accelerate the calibration process, a reinforcement learning (RL) agent is utilized.

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Popular Science Summary

Have you ever found yourself in a stadium surrounded by a boisterous crowd, the noise so deafening that you and your friend constantly had to ask, "What did you say?" If you've experienced this, you know that such a scenario temporarily impairs your ability to communicate. You must wait for the cacophony to subside before your words can be heard again. But what if you and your friend possessed a superpower enabling you to create an exclusive communication channel in the air, isolated from the surrounding clamor? With this power, you could converse effortlessly, undeterred by the strongest background noises—a communication immune to interference.

If you are intrigued by the notion that this thesis will bestow upon you such a remarkable ability, I must regrettably inform you otherwise. Despite the author's fondness for science fiction, this research does not concern a groundbreaking invention like a silent channel in the air between two people, impervious to external noise.

Instead, our focus lies in enhancing the functionality of your cellphones. Just as you've struggled amidst the clamor of a stadium, theater, or other crowded places, your cellphone has also grappled with maintaining connections and delivering high-quality multimedia experiences. Perhaps you've uploaded numerous high-resolution photos to your social media, streamed a major event in glorious 4K, or simply aimed to share precious moments with a distant loved one. Now, envisage a few years ahead—when you desire your cellphone to immerse you in a 3D augmented reality, allowing real-time, multi-angled views of a football goal, transcending your physical location. Furthermore, remember that you're not alone in these endeavors; tens of thousands of others in the same place are concurrently engaged in similar activities. The huge amount of data requiring simultaneous transmission is staggering, isn't it?

Ironically yet fittingly, your cellphone encounters its own version of the "What did you say?" predicament that you've faced with your friend. Just as your communication has faltered due to simultaneous and conflicting voices, your cellphone may grapple with diminished performance owing to devices competing

for the same spatial, temporal, and frequency resources. However, unlike you and your friend, your cellphone is allowed only a single "pardon me" in every ten thousand conversations. Clearly, this presents a daunting challenge.

How can our cellphones maintain seamless, high-speed communication amid formidable interference? Drawing parallels with our initial analogy, we are presented with two choices: the first is to elevate our voice until it drowns out all others—an impractical and vocal-cord-taxing proposition! The same holds true for cellphones; boosting their signal strength above competing interferences is unfeasible, leading to rapid battery depletion or even explosions.

Alternatively, we could suppress other voices as they reach our ears—a wishful notion, but one not currently attainable for humans. Yet, with the marvels of semiconductor technology, our cellphones can be endowed with the capability to reject unwanted signals.

In pursuit of this, our research is centered on designing selective filters to quell interferences, thereby achieving a communication that's clear, high-speed, and energy-efficient. These filters possess adaptability, adjusting based on operational conditions, including varying interference power levels. The significance of this implementation, apart from its versatility, is that it is suitable for modern wideband telecommunication technologies like 5G and beyond, enhancing their performance and ensuring seamless connectivity.

Preface

This thesis represents the culmination of my research as a doctoral student in the field of radio frequency circuit design at the division of *Integrated Electronic Systems*. The primary focus of this endeavor lies in the development of broadband, reconfigurable, and energy-efficient receiver front-ends using advanced CMOS technology.

The thesis is structured into two parts. Part I, titled "Introduction," provides an overview of the research subject, including its use-cases, background, and motivations, followed by a glimpse into potential future research directions. Part II consists of five original scientific publications that highlight the significance of the research. The following list outlines these papers along with my contributions to each:

Paper I

I. Ghotbi, B. Behmanesh, M. Törmänen, "A Wideband Balun-LNA for Sub-6-GHz 5G NR with Multi-Mode Operation in 22-nm FD-SOI," in *Proc. 20th IEEE Interregional NEWCAS Conference (NEWCAS)*, Quebec City, QC, Canada, 2022, pp. 94-98.
Personal contributions: I proposed the structure of the LNA, conducted schematic simulations and designed the layout. I took the role of the main author and presented the paper at the conference as well.

Paper II

I. Ghotbi, B. Behmanesh, M. Törmänen, "A 1.7-6.4 GHz fourth-order RF filter with 1-40% fractional bandwidth in 22-nm FDSOI," in *Proc*. *IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Taipei, Taiwan, 2022, pp. 1-3.
Personal contributions: I devised the novel circuit topology, performed schematic simulations, designed the layout, and carried out measurements. I also authored the paper and delivered its presentation at the conference.

Paper III

I. Ghotbi, B. Behmanesh, M. Törmänen, "A Reconfigurable RF Filter with 1-40% Fractional Bandwidth for 5G FR1 Receivers," in *IEEE Solid-State Circuits Letters*, vol. 6, pp. 97-100, 2023.
Personal contributions: I designed and characterized the chip and wrote the paper.

Paper IV

I. Ghotbi, B. Behmanesh, M. Törmänen, "Broadband RF Front-End Featuring a Reconfigurable Q-Enhanced Filter for Upper Mid-Band 6G Receivers," in *Proc. 21st IEEE Interregional NEWCAS Conference (NEWCAS)*, Edinburgh, United Kingdom, 2023, pp. 1-5.
Personal contributions: I innovated the structure of the multi-mode front-end, formulated its operation mathematically, designed both the schematic and layout, and performed simulation works. I authored and presented the paper as well.

Paper V

I. Ghotbi, B. Behmanesh, M. Törmänen, "Wideband programmable RF front-end for 5G direct sampling receivers," submitted.
Personal contributions: I undertook the role of chip designer and conducted characterizations. Furthermore, I developed circuit analysis, proposed the calibration scheme, and wrote the paper.

Acknowledgments

As I stand at the end of this chapter of my long (and seemingly never-ending!) academic journey, I am profoundly grateful to the entire EIT family for their unwavering commitment to fostering a culture of academic freedom and respect. Without your continuous presence and support, the rollercoaster of successes and challenges I have navigated would have derailed long ago!

My supervisors, you have been a harmonious team. Markus Törmänen, my main supervisor, I truly appreciate your supportive and patient guidance. Baktash Behmanesh, my co-supervisor, I am fortunate to have your sharp insights on my work. Thank you both for being attentive and insightful mentors.

I want to extend my warm thanks to Henrik Sjöland, Pietro Andreani, Stefan Andersson, Lars Sundström, Florent Torres, Mohammed Abdulaziz, Therese Forsberg, and Jonas Lindstrand for their technical expertise, which greatly enriched this research endeavor. Also, I would like to thank Fredrik Tufvesson for leading the Massive MIMO Technology and Applications project, which provided sponsorship for this research in collaboration with Ericsson AB.

If I've managed to turn my ideas into practical reality, if we now have functional silicon, it owes much to the exceptional lab management of Sirvan Abdollahpour. Also, the patient guidance and training I received from Göran Jönsson, Andreas Johansson, Lars Ohlsson Fhager, Stefan Andric, and Peter Herrder were vital in teaching me the art of measurement.

Long Before the measurements, I needed functional servers, reliable networks, and up-to-date software to simulate my ideas. Erik Jonsson and Stefan Molund, your tireless dedication ensured everything ran seamlessly. Thank you both for your invaluable efforts!

My sincere appreciation to Oban[1], the unsung hero of our research team. Through late nights and countless tasks – writing, graphics, simulations, and more – you have been the backbone of my work. You have been a trusty ally, almost never letting me down!

[1] Just to clarify, I'm talking about my PC - not anything or anyone else!

Daniel Sjöberg, Joachim Rodrigues, and Stefan Höst, your kindness on that freezing morning as you stood with international students in opposition to changes in migration laws will forever be etched on my heart. Your compassionate leadership and your human touch are truly appreciated.

I would like to express my deep gratitude to Migrationsverket and the unforeseen impact of COVID-19. Your combined efforts, in their own unique way, helped me preserve my entire passion and excitement for this defense event by preventing me from physically attending any conference throughout my PhD journey.

Research thrives in a calm and stress-free working environment, a place where the mind can be focused, free from concerns about finances and paperwork. Elisabeth Nordström, Linda Bienen, Elisabeth Ohlsson, and Erik Göthe, your dedication has created such an environment for all of us. Thank you.

Over these five years, I have had the privilege of working alongside a remarkable group of colleagues. Masoud Nouripayam, your profound insights, extensive knowledge, generosity, sociable nature, and unwavering humanitarian spirit have been truly inspiring. I've gained so much from our interactions, and the path of learning with you is boundless. Rikard Gannedahl, your intellect and gentleness have been a constant source of inspiration. Hamid Karrari, your friendly and genuine nature has enriched this journey. Masoud Attari (MJ), your sharp criticism of everything kept us on our toes. Lucas Ferreira, your boundless enthusiasm and liveliness brought a sense of joy to our work. And Arturo Prieto, your patience and silent reflections during our Persian conversations, even as we occasionally ignored you, did not go unnoticed — you even picked up some Persian along the way!

I would also like to express my gratitude to Mojtaba Mahdavi, Mohammadhassan Safavi, and Mahdi Rezayati Charan. Our conversations have been enlightening, and I'm thankful for the knowledge and companionship you have shared.

Throughout my educational journey, I've had the privilege of learning from a multitude of exceptional teachers, each contributing a unique piece to the puzzle that shaped this thesis. My gratitude extends to all my teachers. In particular, I wish to highlight the profound impact of two individuals in my life, Mrs. Sedaghat and Mr. Hossein Shafiei.

I feel incredibly fortunate to have found a circle of friends who generously share love and compassion in my new home, Sweden. Thank you, Naghmeh, Behshid, Baktash, and Masoud. And a special thank you to my long-time friend, Fariborz.

I am deeply grateful for my parents, who diligently prepared everything necessary for my personal and academic growth, who respected my choices, and nurtured in me a profound appreciation for life and liberty. I love you both.

And, finally, I extend my thanks to you, my reader. These words would have no purpose without your presence.

Iman Ghotbi
Lund, Nov. 2023

List of Acronyms and Abbreviations

3GPP	Third Generation Partnership Project
4G	Fourth generation
5G	Fifth generation
6G	Sixth generation
AAF	Anti-aliasing filter
ACS	Adjacent channel selectivity
ADC	Analog-to-digital converter
AFE	Analog front-end
AI	Artificial intelligence
AlN	Aluminum nitride
AR	Augmented reality
BAW	Bulk acoustic wave
BEOL	Back end of line
BER	Bit error rate
BG	Back gate
BLER	Block error rate
BOX	Buried oxide
BPF	Band-pass filter
BS	Base station
BVD	Butterworth-Van Dyke
CA	Carrier aggregation
CBW	Channel bandwidth
CC	Component carrier
CG	Common gate
CMRR	Common-mode rejection ratio

CR	Cognitive radio
CS	Common source
CW	Continuous wave
DAC	Digital-to-analog converter
DC	Dual connectivity
DCS	Digital channel selection
DDC	Digital down-conversion
DFAD	Digital frequency and amplitude detector
DFD	Digital frequency detector
DFE	Digital front-end
DL	Downlink
DR	Dynamic range
DSP	Digital signal processing
DSS	Dynamic spectrum sharing
DUT	Device under test
EE	Energy efficiency
eMBB	Enhanced mobile broadband
ENOB	Effective number of bits
FBW	Fractional bandwidth
FD	Full duplex
FDSOI	Fully depleted silicon on insulator
FDD	Frequency-division multiplexing
FEOL	Front end of line
FFT	Fast Fourier transform
FoM	Figure of merit
FR1	Frequency range 1
FR2	Frequency range 2
GFDM	Generalized frequency-division multiplexing
Gsps	Giga sample per second
IB	In-band
IBB	In-band blocking
IEEE	Institute of electrical and electronics engineers
IF	Intermediate frequency
IMD	Intermodulation distortion
IoE	Internet of everything
IoT	Internet of things
IP2	Second-order intercept point
IP3	Third-order intercept point

IRF	Image-reject filter
IRR	Image rejection ratio
ISI	Inter-symbol interference
ISM	Industrial, scientific, and medical
LDE	Layout-dependent effects
LNA	Low-noise amplifier
LO	Local oscillator
LPF	Low-pass filter
LTI	Linear time-invariant
MaMi	Massive MIMO
Mbps	Mega bit per second
MIMO	Multiple-input multiple-output
ML	Machine Learning
mMTC	Massive machine-type communication
MOL	Middle of line
NCO	Numerically controlled oscillator
NF	Noise figure
NFET	N-type field-effect transistors
NLTI	Nonlinear time-invariant
NR	New radio
NSD	Noise spectral density
OFDM	Orthogonal frequency-division multiplexing
OOB	Out of band
OSR	Oversampling ratio
OTA	Operational transconductance amplifier
PA	Power amplifier
PAPR	Peak-to-average power ratio
PCB	Printed circuit board
PE	Power efficiency
PFET	P-type field-effect transistors
PGA	Programmable gain amplifier
PLL	Phase-locked loop
PN	Phase noise
PSRR	Power supply rejection ratio
PU	Primary user
PVT	Process, voltage, and temperature
QAM	Quadrature amplitude modulation

RB	Resource block
RE	Resource element
RF	Radio frequency
RFFE	Radio-frequency front-end
RL	Reinforcement learning
RX	Receiver
S/H	Sample and hold
SAR	Successive approximation register
SAW	Surface acoustic wave
SCS	Subcarrier spacing
SDR	Software-defined radio
SE	Spectral efficiency
SFDR	Spurious-free dynamic range
SI	Self-interference
SINR	Signal-to-interference-plus-noise ratio
SL	Sidelink
SNDR	Signal-to-noise-and-distortion ratio
SNR	Signal-to-noise ratio
SoC	System on chip
SOI	Silicon on insulator
SU	Secondary user
TDD	Time-division duplexing
TI	Time-interleaved
TL	Transmission line
TRX	Transceiver
TX	Transmitter
UE	User equipment
UL	Uplink
URLLC	Ultra-reliable low-latency communication
VCO	Voltage-controlled oscillator
WSN	Wireless sensor network
XR	Extended reality

Contents

Abstract ..... **iii**

Popular Science Summary ..... **v**

Preface ..... **vii**

Acknowledgments ..... **ix**

Acronyms, Abbreviations and Symbols ..... **xi**

Part I Introduction **1**

Chapter 1 Motivation and Scope **3**

1.1 A World of Connected Systems 4

1.2 Intensified Trade-Offs in Integrated RF Design 7

1.3 Pursuit of Resilience and Sustainability 10

1.4 Research Rationale and Objectives 11

1.5 Thesis Outline 12

Chapter 2 Receiver Design Challenges in 5G and Beyond **15**

2.1 Architecture, Spectrum, and Signals of 5G 16

2.2 Frequency Allocation Techniques 21

2.2.1 Carrier Aggregation 21

2.2.2 Dual Connectivity 24

2.2.3 Dynamic Spectrum Sharing 25

2.2.4 SL and SL-Assisted Transmissions 27

2.3 5G Receiver Requirements 28

2.3.1 Sensitivity and Dynamic Range Requirements 28

2.3.2 Linearity Requirements 30

2.3.3 Necessity of Multiple Mode Operation 36

2.4 Receivers Architectures for Multi-Band Operation 37
2.4.1 Homodyne, Low-IF, and Double-Conversion Receivers 38
2.4.2 Digital-IF Receivers 42
2.4.3 Direct RF-Sampling Receivers 44
2.5 Thesis Contribution 53

Chapter 3 Broadband Low-Noise Amplifiers **55**
3.1 LNA Performance Metrics 56
3.2 Bandwidth Extension 60
3.3 Noise Cancellation 64
3.5 Power Efficiency Enhancement 67
3.5 Linearization Techniques 69
3.6 Gain Programmability 71
3.7 Balun-LNAs 74
3.8 Thesis Contribution 75

Chapter 4 RF Filters **77**
4.1 Specifications of RF Filters 77
4.2 Passive RF Filters 81
4.2.1 Acoustic Filters 81
4.2.2 Distributed-Element Filters 83
4.3 Active RF Filters 84
4.3.1 G_m-C Filters 84
4.3.2 N-Path Filters 87
4.3.3 Q-Enhanced Filters 90
4.4 Uncertainties and Calibration 95
4.4.1 Effects of PVT Variations on Q-Enhanced Filter 95
4.4.2 Calibration Schemes 96
4.5 Measurement and Verification 99
4.5.1 Noise and gain measurements 100
4.5.2 Linearity measurements 100
4.6 Thesis Contribution 102

Chapter 5 Conclusions and Outlook **105**

Bibliography **107**

Part II Included Papers **127**

A Wideband Balun-LNA for Sub-6-GHz 5G NR with Multi-Mode Operation in 22-nm FD-SOI **131**

I. Introduction 132
II. Proposed Architecture 133
III. Circuit Analysis and Design Considerations 134
IV. Post-Layout Simulation Results 137
V. Conclusions 141

A 1.7-6.4 GHz fourth-order RF filter with 1-40% fractional bandwidth in 22-nm FDSOI **145**

A Reconfigurable RF Filter with 1-40% Fractional Bandwidth for 5G FR1 Receivers **155**
I. Introduction 156
II. Proposed Circuit Topology 156
III. Measurement Results 159
IV. Conclusion 163

Broadband RF Front-End Featuring a Reconfigurable Q-Enhanced Filter for Upper Mid-Band 6G Receivers **167**
I. Introduction 168
II. Reconfigurable Q-Enhanced Filter 169
III. Circuit Architecture 171
IV. Post-Layout Simulation Results 172
V. Conclusions 174

A Reconfigurable RF Front-End for 5G Direct Sampling Receivers with an Optimized Calibration Scheme **181**
1. Introduction 182
2. Front-end architecture and circuit analysis 183
2.1. Reconfigurable balun-LNA 183
2.2. Q-enhanced filter 184
2.3. PGA and output buffer 189
3. System-level simulation results 190
4. Experimental results 192
5. Calibration Scheme 194
5. Conclusions 198

Part I

Introduction

Chapter 1

Motivation and Scope

On October 22nd, 2022, at Der Große Stern, Berlin, my camera pointed skyward, focused on the statue of Victoria. It smoothly captured all the way down along The Victory Column and became fixated on the vast crowd gathered in the street circle. Their collective chants for liberty and equality filled the air. I believed I was livestreaming a momentous event of the Iranian diaspora. However, my excitement waned when I realized my phone had lost its connection almost from the outset of recording. Everyone there encountered the same unfortunate fate, as each person experienced the loss of connectivity. Each person sought to share their firsthand experience of the event through stories, images, and videos, yet thousands of gigabytes of data remained stranded in phone memories, unable to reach the outside world. The hunt for connectivity began, with data demand so unbearably high that the entire area plunged into darkness, cut off from the global digital landscape. However, this network outage was short-lived. Soon enough, the light returned, and we were reintegrated into the interconnected world of the 2020s, where constant connectivity is expected —uninterrupted and accessible anytime, anywhere. This thesis presents a number of research achievements in the field of electronic circuit design, aiming to enhance the reliability, efficiency, and adaptability of mobile receivers in congested areas.

The opening chapter provides an overview of the socio-technical context in which the research has been conducted. It explores the driving use-cases, technology enablers, and evolving trends of advanced telecommunication networks. In addition, it examines the advantages and disadvantages of semiconductor scaling for analog/RF design. Sustainability considerations and potential contributions to societal resilience are also discussed in relation to the subject matter of the thesis. The chapter concludes by outlining the goals of the research and presenting the structure of the thesis.

1.1 A World of Connected Systems

Over the past decade, a number of super exponentially flourishing technologies have emerged, and the transition phase between waves of destructive innovation has shortened [1]. From computing to transportation, from material science to telecommunication, from sensors to healthcare, in all fields of science and technology we have been observing a great deal of advancement. Many of these techno-scientific developments are convergent, meaning the outcomes of one speed up the surge of the other, and vice versa. For example, an enabling technology in the healthcare sector might be the driving force for advancements in nanoscience. All together, these technologies are shaping a vibrant world in front of our eyes while opening opportunities for well-being that would be unimaginable in the beginning of this millennium. Some examples of these cutting-edge use-cases are:

- Augmented reality (AR) and extended reality (XR) are drastically changing our experience of learning, shopping, travelling, communicating, etc. As an instance, no need to regret for missing Linkin Park live in concerts, maybe you get lucky to see their 3D avatars on stage someday, as we recently witnessed ABBA's XR concert in London [2]. Resurrection might become a recreational reality!
- Autonomous vehicles are on the streets now and advanced driver assistance systems (ADAS) are considered an essential part of modern automobiles. Vehicle-to-vehicle (V2V) connection is needed to enhance safety and optimize urban transportation [3].
- Video-on-demand (VoD), live-streamed multimedia, and high-quality video/audio contents of social media constitute a large portion of our daily data consumption. Exploring TikTok for an hour consumes roughly 840 MB of data [4].
- Video conferencing, which used to be a costly way of communication, has become ubiquitous especially since the COVID-19 pandemic. Holographic telepresence and 3D presentation of industrial prototypes and educational materials are envisaged to be in use [5, 6].
- Remote robotic-aided surgery, telerehabilitation, human-to-machine interface, drug delivery and electrical stimulation bioimplants are a few examples of advanced use-cases in the healthcare sector [7]. Wireless sensor networks (WSN) and wearable electronic gadgets will be used to capture vital signals in real-time from patients, specifically for elderly, high-risk patients, and patients under postoperative care [7].
- Massively distributed wireless sensors, accessible through the concept of internet-of-things (IoT), are deployed for monitoring environmental parameters and plantation, alerting forest fire, facilitating underwater research, analyzing sewage, and enhancing agricultural yield [3].

- Environment-aware traffic lights, online speed monitoring gauges and vehicle counting systems are examples of means to realize optimally managed transportation in smart cities [3]. Wirelessly controlled appliances in smart homes, industry 4.0 robots in manufacturing and warehousing, and smart grids are other examples of currently in-use systems enabled by machine-to-machine (M2M) communication [6].
- Unmanned aerial vehicles (UAV), in civil field, are and will be used for transportation of people and goods, traffic monitoring, agricultural and environmental purposes, filmmaking, relaying of data transmission for remote locations, and rescue operations in occasions of emergency [8].
- Ultra realistic interactive sport and interpersonal online gaming are going to offer extremely high-quality multisensory entertainment [6, 9].

The list above can go on and on with pieces of a colorful map of technology, a portrait of an ambitious world, in which ultimately everything is going to be connected. However, extreme datafication and digitalization of everything is impossible without transmitting and handling enormous amounts of data by means of giant telecommunication networks. Depending on use-cases and distribution of processing between edge and cloud, these networks must fulfill the requirements of coverage, data rate, latency, security, spectral efficiency (SE), and power efficiency (PE). These networks are the underlying infrastructural cornerstone for materializing the abovementioned driving technologies (Figure 1.1).

As a response to this ever-growing demand for connectivity, telecommunication networks have evolved generation after generation. The fifth generation of wireless technology (5G) is expanding and projected to take over previous generations by 2027 in terms of the transferred mobile data traffic and the number of subscriptions [10]. In 5G, the services provided by the network can be categorized as: 1) Enhanced Mobile Broadband (eMBB) targeting wide area coverage and high data rate applications, 2) Massive Machine-Type Communication (mMTC) enabling Internet-of-Everything (IoE) by giving access to a multitude of devices, and

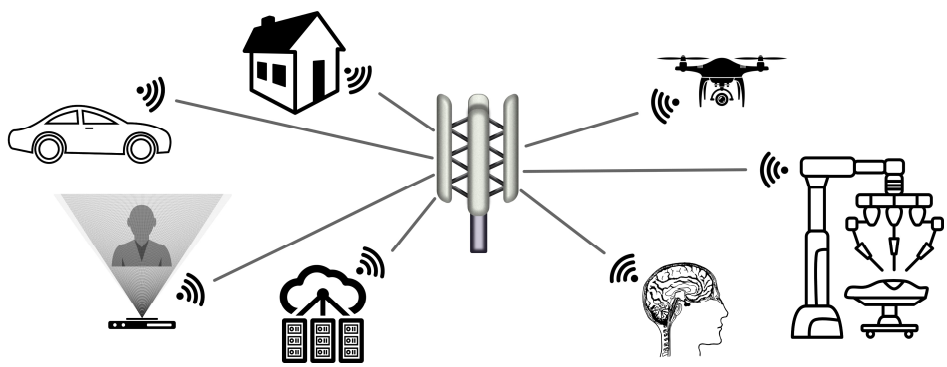

Figure 1.1: Use-cases of 5G and beyond.

3) Ultra-Reliable Low-Latency Communication (URLLC) supporting time-critical use-cases such as automotive and human-machine interface [3].

As shown in Figure 1.2(a), 5G has been deployed since 2018 – the year this PhD project started – and now, it provides 23.5% of global mobile data traffic. It is anticipated that considerable surge of using XR and AR will increase mobile data traffic by a factor of 2.3 by 2026 [10]. In 2019, only 2% of population had access to 5G, now this number has reached 48% and by 2027, 84% population coverage is expected (Figure 1.2(b)) [10].

In 2018, smartphones constituted the majority of connected devices with a share of 48%. It can be seen in Figure 1.2(c) that only five years later, a threefold increase in the number of IoT devices made them the largest group of subscribers [10]. It should be noted that despite smartphones, which demand high data-rate and wideband communication links to process and deliver "big data", IoT devices typically require narrowband channels for a couple of seconds to transfer "small data" which they have measured [6]. From another perspective, while the human population imposes an upper bound for the number of smartphones, there is no ceiling to stop skyrocketing number of IoT devices.

Figure 1.3(d) highlights the transition phase from 4G to 5G. It is projected that 5G will complete its commercialization process by 2029 [10]. However, it could barely be the end of wireless technology evolution. The utilization of artificial

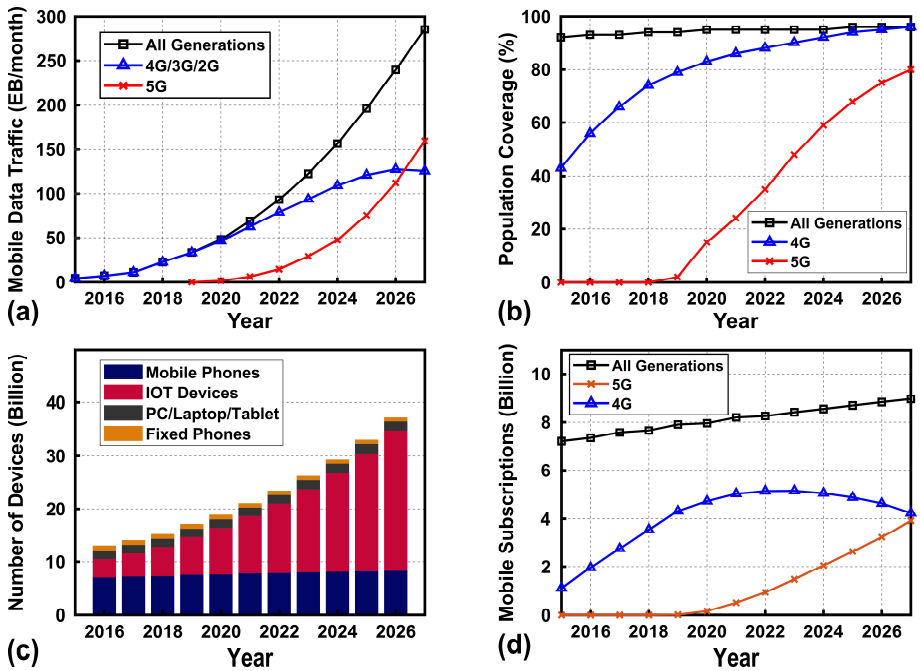

Figure 1.2: Trends of developments in wireless technology: (a) Data traffic. (b) Population coverage. (c) Number of connected devices. (d) Number of mobile subscriptions [10].

intelligence (AI) and machine learning (ML) appears to have a transformative impact on the applications of telecommunication networks, exponentially increasing the demand for high-speed, wide-coverage data transmission. Therefore, it is projected that the introduction of the next generation (6G) will occur approximately by 2030. Moreover, groundwork for its vision, examination of its requirements, and research in network protocols and software/hardware implementations are already underway [6]. Initial studies suggest that to effectively address the requirements, the average data rate per user needs to escalate from 1 Gbps in 5G to 1 Tbps in 6G, while the connection density must experience a tenfold increase, from 10^6 to 10^7 per square kilometer [9]. In Chapter 2, we will delve deeper into the performance targets of 5G and 6G. We will focus on various frequency allocation techniques and coexistence scenarios which are being considered for deployment in these technologies.

1.2 Intensified Trade-Offs in Integrated RF Design

The semiconductor industry has a pivotal role in materializing processing and transmission capabilities of telecommunication networks. We can find electronic chips in all types of connected devices, from low-power IoT sensors to low-latency electronic radars in vehicles, and all integrated systems within smartphones, indeed. Without advancements in design and fabrication of high-speed digital processors and memories, multi-Gsps data converters, and reconfigurable broadband RF/mm-wave front-ends, rollout of 5G and emergence of the world of connected systems would be impossible.

Ever-advancing quality of our digital experiences are attained through a continual enhancement of performance and efficiency in digital processors, which must handle ever-growing matrix calculations. These processors are mainly manufactured in CMOS technology. High-speed signal processing requires low-delay on-chip communication, meaning smaller gate capacitance of transistors. Since the value of the parasitic capacitances is directly correlated with the transistor's physical dimensions, downsizing of transistors speeds up computations. Moreover, reducing the minimum possible manufacturable size of transistors (i.e., feature size) enables more compact designs and higher processing capacity per unit area of silicon. Hence, CMOS technology is destined to being constantly downscaled. While technology scaling is driven by digital demands, i.e., higher integration density, faster switches, and lower leakage currents, analog/RF design does not always benefit from scaling. Nonetheless, to preserve signal integrity in connection between RF and digital domains, avoid reflections and inter-symbol interference (ISI), and reduce complexity and cost of integration and packaging, RF/mm-wave transceivers are commonly embedded in a single system-on-chip

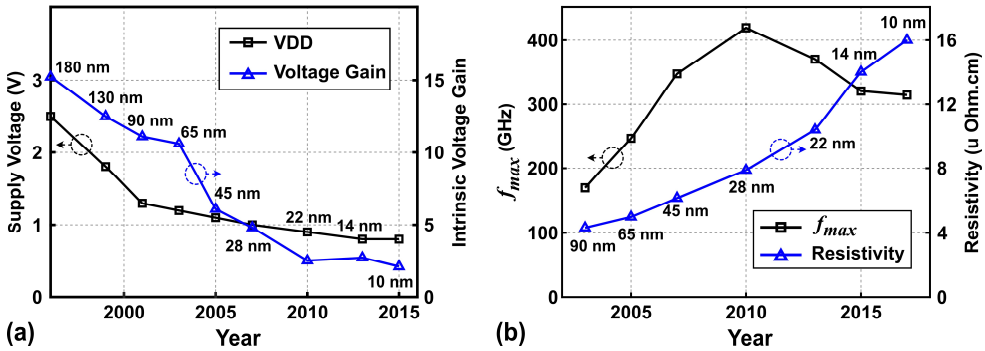

Figure 1.3: Trends of (a) supply voltage and intrinsic voltage gain, and (b) maximum oscillation frequency and Cu resistivity across CMOS technology nodes [11-20].

(SoC) fabricated in a cutting-edge CMOS technology. In other words, RF circuits and systems must be tailored to mitigate the downsides of scaling and harness the strengths of new technologies. In general, scaling has exacerbated the well-known, challenging trade-offs between RF design goals, including power consumption, voltage/power gain, bandwidth, noise performance, linearity, and chip area. In this regard, several important characteristics of nanometer-scale CMOS technologies and their impact on RF design are highlighted below:

- As depicted in Figure 1.3(a), thinner gate oxide in advanced CMOS technologies has led to a reduction in the supply voltage (V_{DD}); i.e., lower than 1 V for 32 nm process and subsequent nodes. However, the threshold voltage has not scaled down proportionately. Consequently, the linear operational region of transistors has been more restricted than earlier sub-micron technology nodes. In RF transceivers, this limitation manifests as more pronounced intermodulation products, gain compression, and harmonic distortion.
- Intrinsic gain (g_m/g_{ds}) of the core transistors has been constantly decreasing, from 15 in 180 nm technology node to below 5 in 32 nm and beyond. As a result, for high gain amplifier design, the size of transistors should be increased and stacked structures should be used which limit the maximum achievable bandwidth.
- Historically, the substantial reduction in the size of front-end-of-line (FEOL) parasitic capacitors in downscaled technology nodes used to drive a rapid increase in both the transit frequency (f_T) and the maximum oscillation frequency (f_{max}). However, this trend has reached a saturation point. As shown in Figure 1.3(b), we have observed marginal or no improvements in f_{max} for technology nodes beyond 45 nm. This phenomenon can be attributed to the presence of larger inter-metal capacitors and increased resistance in the interconnects of the middle-of-

line (MOL) and back-end-of-line (BEOL) [21, 22]. As a result, scaling down the physical dimensions of the FEOL does not necessarily lead to an increase in the operating frequency anymore.

- For the sake of higher integration density, the cross section of metal layers, contact and vias is also scaled down which intensifies surface scattering and grain boundary scattering effect [18, 21]. Therefore, the effective resistivity of Cu interconnects has been drastically increasing and this trend is projected to continue at a high rate (Figure 1.3(b)). It means that RC delays, phase shifts, generated noise, and power dissipation of interconnects alongside other layout-dependent effects (LDEs) must be considered in the design flow and extensive R+ C + CC parasitic extraction is required.
- In 45 nm node and beyond, reduction of the gate oxide thickness has exacerbated the tunnelling current [14]. This phenomenon can be modeled as a gate resistance (R_G) which is not negligible anymore. This resistance limits noise performance of low-noise amplifiers (LNAs), matching bandwidth, and power efficiency of power amplifiers (PAs).
- Smaller feature size, smaller device pitch, and thinner metal layers in recent technologies have troubled heat conduction. As a result, self-heating has become an important factor in sizing devices and layout of circuits [15]. In comparison between bulk CMOS and silicon on insulator (SOI) technologies, the latter suffers more severely from self-heating. Among SOI technologies though, fully depleted (FD) SOI has a superior maximum current density as the thin buried oxide (BOX) layer has higher heat conductivity than its thick counterpart in other SOI technologies [17].
- Short-channel and narrow-channel effects are more prominent in deeply downscaled technology nodes, resulting in increased variations in the threshold voltage (V_{th}) [22]. However, in FD-SOI technology, where the bulk is isolated from the channel by a BOX layer and no additional junction design is required, V_{th} variations are mitigated, offering improved reliability compared to bulk CMOS technology [12].
- The underlying substrate of transmission lines and inductors plays a crucial role in determining the effective quality factor of these passive components. Additionally, the resistivity and linearity of the substrate both affect the level of self-interference, crosstalk, and high-frequency leakage within the chip [12, 23]. Low-resistivity substrates, typically employed for digital implementations, can degrade RF performance. To address this issue, special treatments and substrate doping profiles are applied to increase resistivity beneath RF components [14, 23], thereby increasing the quality factor of passive structures. This necessitates more intricate layout considerations in compact designs, where also coupling to other passive structures and active components can influence the performance.

To summarize, advanced CMOS technologies provide nanometer-scaled, power-efficient, and high-speed transistors. However, MOL/BEOL layers and substrate can produce noticeable delay and noise, while dissipating a large amount of power. Additionally, V_{DD} scaling has limited the headroom voltage of amplifiers and makes circuits susceptible to nonlinear effects. Moreover, it is crucial to effectively address device mismatch, process variations, and self-heating at all levels of design.

1.3 Pursuit of Resilience and Sustainability

Considering the broader implications, the progress of wireless technology greatly contributes to the well-being of humanity and the sustainable development of societies. It facilitates widespread access to the internet, knowledge, educational resources, and healthcare services [3, 9]. This empowers individuals to exercise their fundamental right to freedom of expression while creating a more equitable society and fostering a democratic societal order [24]. The significance of these advancements has become particularly apparent during the COVID-19 pandemic, where access to remote services has become indispensable. In envisioned scenarios of future sustainable societies, including the collaborative economy [25], the pivotal role of digitalization and information networks as a prerequisite for resource sharing and alleviated spatial limitations is emphasized.

In the context of greenhouse gas emissions and their environmental consequences, smart cities and optimized transportation enabled by telecommunication networks can make a significant impact on reducing fuel consumption and, consequently, CO_2 emissions. However, it should be noted that these networks themselves contribute to 7-10% of global energy consumption [26]. Despite the anticipated 10 to 100-fold increase in energy efficiency with the advent of 5G networks, the exponential growth in data demand raises concerns about the overall energy consumption of these networks. In particular, a multiband 5G base station can consume more than 20 kW at peak data traffic [27]. To address this concern, the utilization of power-efficient and reconfigurable circuits and systems, coupled with a holistic approach towards co-optimizing network protocols and modulation schemes, can help mitigate carbon footprint of telecommunications networks [26].

Narrowing down our discussion, in RF circuit design for 5G and beyond, it is crucial to prioritize sustainability by minimizing material usage during manufacturing and maximizing spectrum efficiency and energy efficiency during operation. The amount of material used depends on factors such as chip area, bonding and packaging processes, and soldering techniques. Employing compact designs and conducting thoughtful modular layout and floor planning can help minimize material waste.

To enhance spectrum efficiency, it is necessary to incorporate wideband and multi-band circuits. It is important to note that frequency allocation regulations vary geographically. Therefore, the inclusion of programmable circuits and software-defined radio (SDR), which support multiple frequency bands and standards and allow for circuit reuse, can reduce manufacturing costs and use of material.

Furthermore, the minimization of power consumption and the implementation of power-saving modes should be key considerations in transceiver design. It is worth emphasizing the importance of ensuring network access for all end-users, particularly in congested urban areas. Therefore, meeting both resilience and sustainability requirements simultaneously can pose a challenging task, necessitating a degree of reconfigurability in RF circuits and systems.

By carefully addressing these sustainability-related factors in integrated RF circuit design, we can move towards more environmentally friendly and efficient wireless systems that prioritize resource conservation, spectrum utilization, energy efficiency, and network accessibility.

1.4 Research Rationale and Objectives

Considering the demanding requirements of receiver front-ends for 5G/6G applications and the RF design challenges posed by advanced CMOS technologies, as depicted in Figure 1.4, it becomes of utmost importance to:

- Thoroughly investigate various receiver architectures to gain a comprehensive understanding of their capabilities and limitations in the reception of wideband multi-carrier signals in the ever-evolving wireless networks.

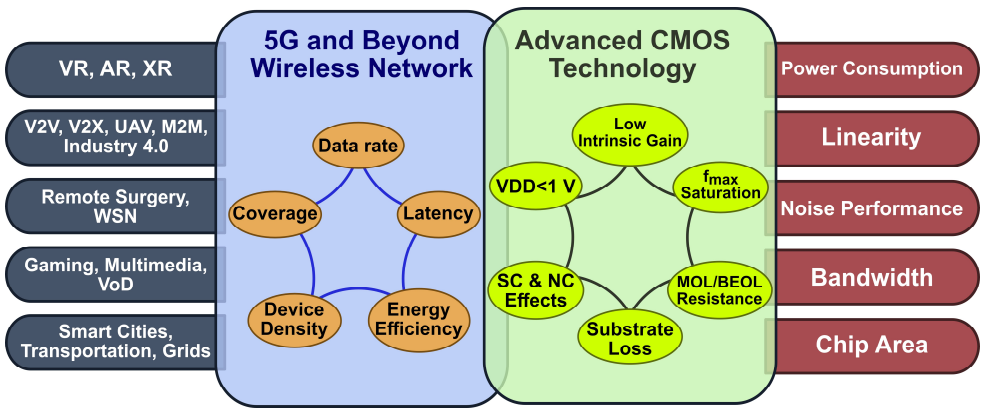

Figure 1.4: Summary of research challenges and objectives.

- Conduct an exploration of broadband LNA designs, assessing their tolerance to blockers and sensitivity in rigorous tests.
- Examine integrated RF filter solutions, while addressing the hurdles in achieving sufficiently low power consumption.
- Highlight the necessity for multi-mode and reconfigurable front-ends, enabling the realization of software-defined and cognitive (spectrum-aware) radios.
- Explore the potential of harnessing the strengths of advanced CMOS technology in switching and digital processing to mitigate its weaknesses in RF performance.

Aligned with this rationale, the primary objectives of this thesis are:

- To integrate reconfigurable elements into LNAs and RF filters, enabling RF front-ends to meet both sensitivity and blocker tolerance requirements and achieve high dynamic range.
- To propose low-voltage and low-power solutions by leveraging a combination of digitally-assisted circuits, analog power-saving techniques, and the unique features of FD-SOI technology.
- To introduce efficient calibration techniques and automatic tuning approaches to mitigate uncertainties and maintain optimal performance.

1.5 Thesis Outline

The Introduction part of the thesis is organized into five chapters, with the aim of presenting an overview of the challenges faced in receiver design for 5G and beyond applications. Within these chapters, we delve into various solutions at different levels of design, offering insights into innovative system architectures and circuit topologies. Our investigation underscores the pivotal role of reconfigurable RF front-ends, demonstrating how cutting-edge CMOS technologies enable this essential feature. The Introduction part serves as a bridge between the foundational knowledge in the field of electronic circuit design and the subsequent part of the thesis, which comprises the research papers.

Chapter 2 provides an in-depth exploration of the requirements and challenges in designing receivers for 5G networks. It describes the complexities arising from spectrum allocation techniques, with a particular focus on blockers. Additionally, various receiver architectures are analyzed, weighing their advantages and disadvantages. The chapter culminates in a detailed study of direct RF-sampling receivers, examining their properties and evaluating their strengths and weaknesses.

Chapter 3 is dedicated to outlining different circuit techniques employed in state-of-the-art broadband LNAs. Special emphasis is placed on noise-cancelling and

power-saving techniques, highlighting their effectiveness in achieving superior performance.

Moving on to Chapter 4, the focus shifts to RF filter design. The chapter introduces key filter parameters and explores their applications in receiver front-ends. Specifically, the discussion revolves around G_m-C and N-path filters, addressing their design challenges such as excessive power consumption at high frequencies. Moreover, Q-enhanced filters are introduced, and previous research works in this domain are reviewed. Subsequently, we discuss the impact of uncertainties stemming from fluctuations in power supply, variations in temperature, and inherent manufacturing imperfections on Q-enhanced filters. We underscore the necessity of calibration and explore various calibration techniques, including the use of reinforcement-learning (RL) in formulating an optimal policy for an efficient calibration process. The chapter culminates in an overview of measurement techniques and test scenarios that have been employed to evaluate the front-end's performance.

Finally, Chapter 5 concludes the Introduction part by summarizing the accomplishments and contributions of the thesis, while offering insights and recommendations for future research works.

Chapter 2

Receiver Design Challenges in 5G and Beyond

In 1992, J. Mitola III published a widely recognized paper on the evolution of SDR in which he foresaw the necessity, challenges, and opportunities of digitally programmable radios [28]. Mitola identified the rapid digitalization trend in the communication industry and the transition from special-purpose analog hardware solutions to flexible digital implementations. He concluded that placing ADC as close to the antenna as possible and defining radio functions in software were key characteristics of software radios [29]. The objective was to introduce an adaptive radio capable of changing its operational mode for optimal power consumption, service availability, or signal quality [28]. However, Mitola acknowledged the significant challenges in realizing such an ambitious idea. He highlighted the limitations in bandwidth, sampling rate, and dynamic range of ADCs, particularly when expanding the SDR concept to frequencies above 1 GHz [28]. At that time, optoelectronic RF sampling circuits and ultra-fast sample-and-holds in GaAs technology were among the most promising solutions to address the ADC issues [28]. However, manufacturability and integration difficulties postponed the practical implementation of high frequency SDRs. Mitola also emphasized the need for breakthroughs in multiband antennas, wideband RF front-ends (RFFEs), and RF filters with high out-of-band (OOB) rejection to meet the demands of SDR [30]. Almost a decade later, Mitola and Maguire introduced the concept of cognitive radio (CR), adding intelligence to SDRs. While the authors did not name their newly born technology themselves and Mitola found the term “cognitive radio” somewhat misleading [31], they aimed to develop radios that are aware of the spectrum, location, environment, and network, and capable of automatic adaptation to changes in these parameters [32]. A CR was intended to automatically select radio bands and

operating modes to fulfill user requirements at specific spatiotemporal status [33]. The goal is to utilize the radio spectrum more efficiently. Nevertheless, Mitola and Maguire modestly acknowledged that *"significant memory, computational resources, and communication bandwidth are needed for cognitive radios, so this technology might not be deployable for some time… this goal may be very far off … the present research is therefore offered as a mere baby step in a potentially interesting research direction"* [32].

We had to wait for two decades until CMOS technology achieved satisfactory switching performance for implementing Gsps ADCs and ultra-broadband RFFEs. The alignment between the employed techniques to enhance spectral efficiency (SE) and energy efficiency (EE) in 5G and beyond with SDRs and CRs is not a mere coincidence. It signifies a deliberate integration of these approaches, demonstrating a strategic fit between the goals and capabilities of SDRs and CRs with the requirements of SE and EE optimization in advanced wireless communication systems. However, it does not imply that all challenges have been resolved and that advanced semiconductor devices have been able to address all the performance bottlenecks. There are still several critical issues that need to be addressed, such as noise, interference, image rejection, aliasing, spectrum observation, and more. These challenges require continued investigation and innovation, taking incremental "baby steps" towards finding effective solutions in circuit design. In this chapter, we explore the features of 5G technology, the challenges it poses for receiver design, and various receiver architectures. We also examine RF sampling receivers as a viable implementation and explore their requirements through realistic examples.

2.1 Architecture, Spectrum, and Signals of 5G

As mentioned in Chapter 1, the merit of wireless technologies from generation to generation can be measured in three main aspects: coverage, available data rate, and reliability. With that regard, Table 2.1 compares the performance targets of 4G, 5G New Radio (NR), and 6G (predicted).

To be capable of boosting coverage tenfold and providing connectivity for a multitude of user equipment (UE) in a reliable and efficient fashion, 5G has a

Table 2.1: Comparison of performance targets across wireless technology generations [35]-[37].

Performance Metrics	4G	5G	6G
Peak data rate (Gbps)	0.1	20	1000
User available data rate (Mbps)	10	100	1000
Connectivity density (devices / square km)	10^5	10^6	10^7
Maximum Channel Bandwidth (MHz)	20	100 (FR1)	160 (FR1)
Spectral Efficiency (bps/Hz)	10	30	100

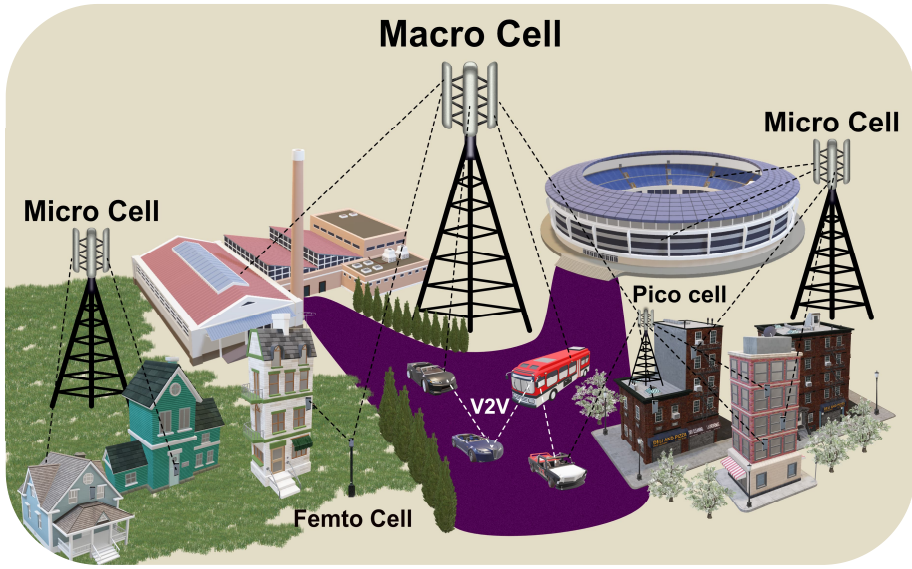

Figure 2.1: Use-cases, communication links, and base stations in 5G network.

hierarchical structure of base stations (BS) and three types of transmission links. As shown in Figure 2.1, we can categorize BSs into four groups: Macro Cells, Micro Cells, Pico Cells, and Femto Cells. In the Third Generation Partnership Project (3GPP) classification of BSs, the Macro and Micro cells are called NR Wide-Area (WA) BS and NR Medium-Range (MR) BS, respectively, while both Pico and Femto cells are placed in the same category called NR Local-Area (LA) BS [34].

Table 2.2 makes a comparison between these four categories. From the top to the bottom of this pyramid, for covering a wider area and reducing the path loss, lower carrier frequencies are used. Macro cells are required to have the best noise performance, while Pico cells need to be highly tolerant to interfering signals because they are typically used in congested urban areas and not at height on the tower.

In 5G, three main types of signaling are considered based on the receiver, transmitter, and the direction of data transmission. Uplink (UL) signal is transmitted

Table 2.2: Attributes of various types of 5G base stations [38], [39].

Attribute	Macro Cell	Micro Cell	Pico Cell	Femto Cell
Number of connected users	>2000	100~2000	30~100	1~30
Cell radius (km)	8~30	0.2~2	0.1~0.2	0.01~0.1
Transmitted power (dBm)	>40	30~40	20~30	0~20
Minimum coupling loss (dB)	70	53	45	<45
Minimum BS to UE distance (m)	35	5	2	<2

by a UE and received by a BS. This signal is typically low-power and narrowband. Downlink (DL) signal moves in the opposite direction and carries most of the high data-rate traffic. The third type is called sidelink (SL), referring to direct communication between vehicles and devices in device-to-device (D2D) and vehicle-to-everything (V2X) services.

Frequency allocation to these three types of signaling and management of resources in the network must be done in a way to minimize collisions and to maintain the reliability of the system. Moreover, in a network where all UEs can potentially possess a part of frequency spectrum and propagate their signals, the magnitude of aggregated interference can significantly vary time to time and location to location, requiring spectrum-aware receivers to be seamlessly adjusted in response [40].

To achieve tenfold increase of the data rate compared to 4G, as formulated by Shannon in Equation 2.1 [41], either larger bandwidths (BW) must be allocated to 5G signals or the signal to noise power ratio ($SNR=S/N$) of the communication link must be improved.

$$C = BW.\log_2\left(1+\frac{S}{N}\right) \tag{2.1}$$

While SNR enhancement is performed mostly through coding, channel characterization, spatial multiplexing, beamforming, and digital processing [42, 43], increasing the total available bandwidth necessitates various frequency allocation techniques, utilizing unlicensed and unused bands (white spaces), and reframing crowded parts of the spectrum [44]. Figure 2.2 shows the 5G spectrum which is divided in two frequency ranges according to 3GPP's Release 17 [34]:

1. **Frequency Range 1 (FR1) (410 to 7125 MHz):** Frequency resources below 1 GHz (Low Bands) have been used by all previous generations and are shared with TV broadcasting and meteorological satellites [45]. The 5G bands within this sub-range are used for low data rate SL or long-distance DL/UL and frequency-division multiplexing (FDD) is mainly deployed [34]. The range from 1 to 2.6 GHz (Mid Bands 1) has been used for cellular communications since advent of 2G. This range is the most crowded part of the spectrum and there are numerous sources of interference, among them the best known is the ISM radio band at 2.4 GHz [45] where n40 and n41 exist; the only bands within Mid Bands 1 that support 100 MHz channel bandwidth (CBW). Mid Bands 1 are primarily considered for wideband low-latency SLs as well as medium bandwidth DL/ULs. The next sub-range within FR1, Mid Bands 2, includes less coexistent wireless standards and has been considered for cellular communication since the introduction of 4G. Within Mid Bands 2, several broad bands (n77, n79, n46, and n96) are allocated to 5G, supporting 100 MHz CBW for high data rate DL signals. As differentiated by colors in Figure 2.2, the transceivers operating within this sub-range use time-division duplexing (TDD) [34].

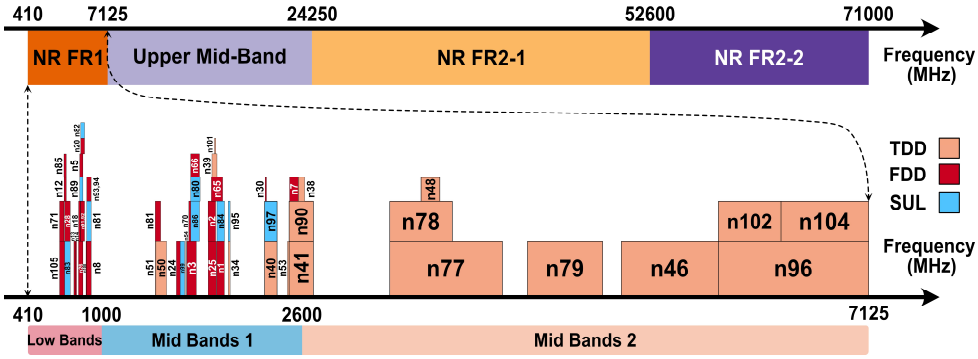

Figure 2.2: 5G spectrum.

2. **Frequency Range 2 (FR2) (24.25 to 71 GHz):** This mm-wave frequency range of 5G is assigned to short-range ultra-high data rate and reliable communication links. Due to remarkable propagation loss at these frequencies, only Pico and Femto cells use these frequency blocks. Beamforming, signal generation, power efficiency and ultra-wideband operation are the main receiver design challenges within FR2. However, the number of interfering signals is less, and the level of interferers are normally lower than FR1, so mm-wave receivers have relaxed linearity requirements compared to FR1 receivers.

In addition to FR1 and FR2, Figure 2.2 shows a frequency span between these two labelled Upper Mid-Band [46]. It is also called centimetric range in some publications [47]. Within this range, IEEE K_u and K bands primarily are used for satellite communication [45], but considering envisioned 400 MHz CBW in 6G, reframing and partitioning of this range is in progress [46].

Along with increasing CBW and utilizing higher carrier frequencies, to achieve the required SE, high order digital modulation schemes are employed in 5G in which each symbol represents M bits, increasing the effective bandwidth and maximum data rate. Quadrature amplitude modulation (2^M-QAM) is the main scheme used for this purpose and 256-QAM is the highest order considered for FR1 signals [34]. However, the more complex modulation schemes lead to more sensitivity to noise, thus posing more stringent requirements on the receiver noise performance. For example, Figure 2.3 shows the uncoded bit error rate (BER) versus bit to noise ratio (E_b/N_0) across QAM modulations and corresponding constellation diagrams. The difference between E_b/N_0 and SNR values in subplots of Figure 2.3 stems from the fact that

$$SNR = \frac{E_s}{N} = \frac{E_b}{N}\log_2(M) \tag{2.2}$$

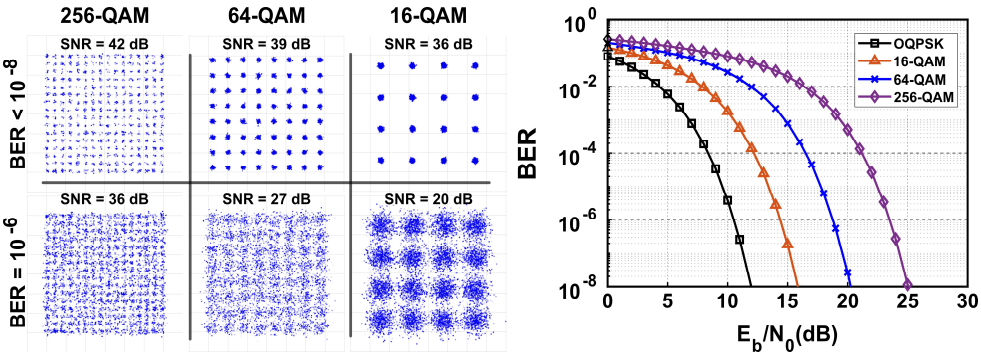

Figure 2.3: Constellation diagram and BER of high-order digital modulation schemes.

In eMBB applications, BER<10^{-6} is often acceptable [8]. With that threshold, it can be seen from constellation diagrams that the received SNR is required to be larger than 36 dB for 256-QAM, while 20 dB SNR is enough for 16-QAM. Maintaining acceptable noise performance of receivers while they are exposed to strong interfering signals is crucial to enable high-order modulations, otherwise the BS must settle for lower modulation orders which results in degraded SE. Moreover, it is worth mentioning that more complex modulation schemes generate larger peak-to-average power ratio (PAPR), which must be considered in the transceiver (TRX) link budget for both RX and TX, especially affecting PA in the TX [48].

Multiple-input multiple-output (MIMO) signaling is another feature of 5G technology which contributes to SE enhancement. An array of antennas on the UE device [43, 49, 50] and a massive number of antennas in BS [9] provide additional gain by employing diversity techniques [42], thereby increasing SNR and capacity. Massive MIMO (MaMi) can also be used to reduce interference and OOB propagation [42]. However, these two techniques require different configurations and cannot be performed simultaneously. Therefore, if we configure MIMO system for a better SNR, the large number of propagating antennas at BS might render mutual interference which needs to be considered in BS receiver design. Moreover, the utilization of massive antenna arrays necessitates a more densely packed arrangement of transceivers for each antenna unit, thereby demanding compact and integrated solutions.

Since the focus of this thesis is on the RFFEs of receivers for 5G NR FR1 communication, the rest of this chapter is dedicated to the techniques commonly deployed for increasing SE in this frequency range. Particularly, we briefly overview several frequency allocation techniques which increase total effective bandwidth. We also assume that beamforming and MIMO processing are conducted in the digital domain.

2.2 Frequency Allocation Techniques

Before introducing the major frequency allocation techniques, it is important to clarify the definitions of certain concepts in the context of frequency management. The 5G NR transceivers employ Orthogonal Frequency Division Multiplexing (OFDM) in which a data stream is divided among several subchannels (subcarriers) in the frequency domain, with each subchannel carrying a symbol at a dedicated time slot. These subchannels are commonly referred to as resource elements (RE) in the physical layer of communication systems. In 5G FR1, 12 consecutive subcarriers construct a resource block (RB) in the frequency domain, and the subcarrier spacing (SCS) is dynamically chosen from 15, 30, or 60 kHz [34]. A NR channel is composed of 24 to 275 RBs, and guard bands are required between each pair of adjacent channels, although they can be asymmetric. As a result, the channel bandwidth can be determined by

$$CBW = Number\ of\ RBs\ \times 12 \times SCS + GBW \tag{2.3}$$

where GBW represents the total bandwidth of guard bands. In 5G, unlike previous generations, the REs within an RB can be assigned to different time slots, providing greater flexibility in time/frequency resource management [34], thereby enhancing both SE and EE.

Furthermore, it is anticipated that fully developed 5G systems and future generations of wireless technology will adopt Generalized Frequency Division Multiplexing (GFDM) to reduce OOB emission and enhance SE, even though it introduces additional implementation complexity [51].

In the following, we will focus on five key strategies adopted to enhance SE and expand bandwidth in 5G networks. We will also examine the complexities and challenges these approaches introduce in the context of receiver design.

2.2.1 Carrier Aggregation

In Carrier Aggregation (CA) scenarios, two or more NR channels are simultaneously utilized to establish a wideband link, primarily for eMBB use-cases. Each aggregated channel is called a component carrier (CC). Figure 2.4 illustrates three modes of CA:

1- **Contiguous Intra-Band CA:** CCs belong to a single band and are adjacent to each other. This mode allows for assigning a wide frequency slot within a single band to a particular communication link.
2- **Non-Contiguous Intra-Band CA:** CCs belong to a single band, but they are discontinuous and distributed across the band.
3- **Inter-Band CA:** At least one CC belongs to a different band than others.

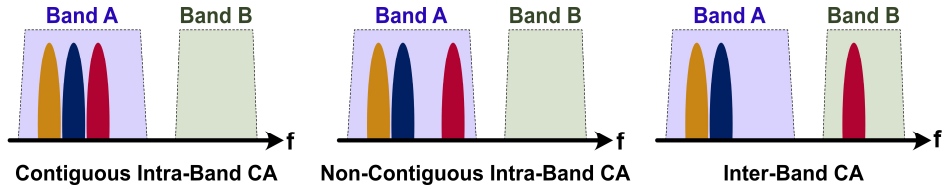

Figure 2.4: Three types of carrier aggregation.

As per the latest 5G technical specifications frozen in 3GPP's Release 17, the current limit allows for the aggregation of up to 16 CCs with a constraint on the total bandwidth, set at a maximum of 400 MHz in FR1. Furthermore, the 3GPP has introduced combinations of two to six bands for inter-band CA, enabling simultaneous FDD and TDD communication links [34]. However, it is anticipated that these numbers will increase as 5G technology progresses towards full maturity.

The growing number of aggregated carriers across a wide frequency range gives rise to a multitude of practical challenges for receiver implementation. In non-contiguous CA, expanding the reception bandwidth of the radio is a commonly adopted solution. However, in cases of non-contiguous and inter-band CA, the implementation often necessitates numerous parallel receiver and transmitter paths on a single chip [52].

State-of-the-art integrated transceivers supporting CA and MIMO configurations already employ over 20 RX paths with this number expected to continue increasing [53]. Without architectural innovations, the power consumption and chip area of such direct conversion transceivers will soon exceed manageable limits [52]. However, power, bandwidth and area are not the sole concerns arising from these complex scenarios. Here, we highlight a few of these challenges:

- **TX-to-RX leakage:** When multiple transceivers are simultaneously active, operating in both FDD and TDD modes, the aggregated leakage from all TX paths received by each RX path can lead to desensitization. In FDD mode, the TX-RX isolation depends on the frequency spacing between RX and TX carriers. In the case of inter-band CA involving the bands A and B, it is possible that the RX frequency of the band A is closer to the TX frequency of the band B than to its own TX frequency, making it more difficult to isolate RX_A from the interference originating from TX_B, as compared to its normal self-interference (SI) [53]. For instance, in the case of 4CC CA involving n1, n3, n7, and n38 shown in Figure 2.5(a), the leakage from n3 TX can compress the gain of n1 RX and degrade its sensitivity. Furthermore, in this combination, n38 is adjacent to n7 TX. Since n38 operates in TDD mode, a high roll-off band-select filter is required at the input of n38 RX. Addressing these concerns necessitates duplexers with a TX-RX isolation larger than 55 dB and receivers capable of withstanding SI as high as 0 dBm [54].

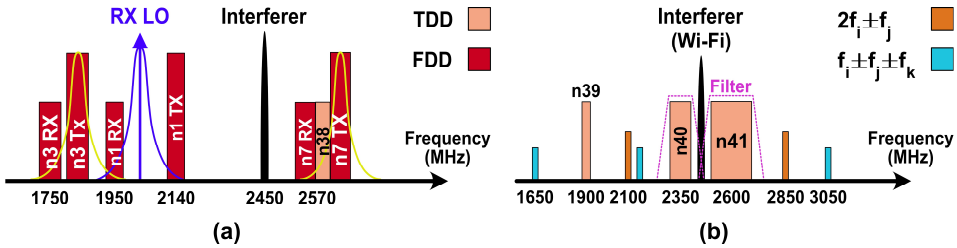

Figure 2.5: Examples of receiver challenges in CA and co-existence scenarios.

- **LO leakage:** The leakage power from in-band local oscillators (LO), along with the harmonics of OOB LOs can exacerbate DC offset of RX chains [53]. Moreover, the phase noise (PN) of LO modulates the TX leakage, thereby degrading the effectiveness of SI cancellation techniques [54]. Figure 2.5(a) shows the extended skirt of LO/TX PN into adjacent bands.
- **Complex image rejection:** The distribution of aggregated bands can introduce challenges in achieving acceptable image rejection, especially in digital intermediate frequency (digital-IF) implementations where an LO is employed to down-convert the higher-frequency bands before digitizing all bands together [53].
- **Intensified role of second-order nonlinearities:** In a single-carrier transceiver, the impact of second-order intermodulation distortions (IMDs) is typically considered to be significantly lower compared to third-order IMDs since they fall far out of band and are substantially attenuated by the filters in the RX chain. However, when multiple carrier frequencies are involved, the significance of second-order IMDs can no longer be disregarded, as they may become in-band distortions for other RX bands [53].
- **LO-LO spurs:** The crosstalk between LO interconnects, leakage between phase-locked loops (PLLs), nonlinearities, and reciprocal mixing can generate intermodulation products between LOs and their harmonics. This interference can appear across the entire band-of-interest, resulting in the down-conversion of interfering signals or SI to the baseband [54].
- **Co-existent interference signals:** Numerous external sources propagate signals within the same part of frequency spectrum, and in a wideband multi-carrier system, there is a higher likelihood of these interferers being in close proximity to the desired signals [54]. Consequently, filtering out this interference becomes more challenging. The LO leakage, LO-LO spurs, or LO harmonics can down-convert these signals. For example, in Figure 2.5(b), a Wi-Fi signal appears between two aggregated bands (n40 and n41). To effectively reject this interference and capture the desired wideband signals within n40 and n41, high-order band-pass/band-stop RF filters are required.

- **Passive intermodulation (PIM) products:** The simultaneous emission of multiple high-power signals generates cross-modulations in the internal components of the transceiver modules, including switches and filters, as well as surrounding objects such as connectors, cables, antennas, and metal surfaces. This SI adversely affects the SNR and dynamic range of the receiver. Since the magnitude of PIMs depends on the power of transmitted signals, the impact of this type of SI is particularly notable at base stations [55].

Two commonly employed techniques in 4G/5G base stations to handle these challenges are Maximum Power Reduction (MPR) and Maximum Sensitivity Degradation (MSD) [55]. However, these approaches come with trade-offs: MPR sacrifices coverage, while MSD compromises SE. To overcome these issues and uphold high data rates, 5G receivers must incorporate highly reconfigurable and interference-tolerant front-ends featuring analog and digital SI cancelling subsystems, RF filters with enhanced OOB rejection capabilities, and PLLs with a lower phase noise compared to previous generations.

2.2.2 Dual Connectivity

In Chapter 1, we have discussed gradual and evolutionary deployment of 5G. During the initial stages, when 5G BSs are not yet ubiquitous, there can be coverage gaps that result in sudden disconnections for UEs [56]. This issue becomes more pronounced during handovers when UEs are in motion. Additionally, for global roaming purposes, UEs must be backward compatible, meaning they need to support the waveforms and frequency bands of legacy 2G/3G/4G networks [57].

To reduce the interruption time while handover occurs, to maintain high data rate, and to optimize the utilization of infrastructure and spectrum [56], 3GPP have defined three connectivity modes: 1) Long-Term Evolution (LTE) operation where the UE is only connected to a 4G BS, 2) Non-Standalone (NSA) LTE+NR in which multiple links are established between the UE and both LTE and NR BSs, and 3) Standalone (SA) NR where only 5G BSs serve UEs [58]. Among these options, NSA, which is also called Evolved Universal Mobile Telecommunications Service Terrestrial Radio Access (E-UTRA) NR Dual Connectivity (EN-DC), offers several advantages:

- **Seamless handover:** UEs have simultaneous access to both LTE and NR networks, reducing the probability of service disruptions [56].
- **Enhanced peak data rate and SE:** Data can be split into multiple streams and transmitted through several links, which are then are aggregated at the UE. This, combined with CA and MIMO techniques, improves the peak data rate and SE [56, 57].

- **Throughput maintenance:** mm-wave links can provide ultra-high data rates. However, due to high isotropic pathloss, blockage from surrounding objects, attenuation caused by foliage, and sensitivity to moisture, these links are prone to highly dynamic channel conditions. In scenarios with low signal to interference plus noise ratio (SINR) for FR2 NR links, an auxiliary LTE link can maintain throughput at an acceptable level [56].
- **Latency improvement:** mm-wave channels pose challenges for handovers, and traditional standalone networks may not respond quickly enough. In an NSA architecture, LTE links can collect channel measurements, enabling better characterization of channel dynamics and faster handovers [59].
- **Frequency reuse:** Underutilized 4G frequency bands at a specific spatiotemporal coordinate can be employed in CA configurations to enhance SE and data rate [56].

However, the benefits of EN-DC come with increased complexities in transceiver design. Similar to CA, EN-DC requires multiple, independent, simultaneously activated RX/TX paths, which can lead to SI and OOB emission violations due to intermodulation products [58]. One particularly challenging instance of EN-DC is the aggregation of EUTRA B41 and NR n41 bands. These TDD bands share the same part of spectrum around 2.5 GHz, which renders them susceptible to potential interference from signals in the 2.4 GHz ISM band [58].

To make enough isolation between these paths, conventional RFFE architectures require multiple surface acoustic wave (SAW) filters and external on-board components, resulting in increased costs and dimentions. Moreover, in the use-cases like video streaming, the power consumption of concurrent radios in NSA mode is more than double compared to SA 5G operation [56]. Furthermore, the realization of the frequency reuse advantage in EN-DC relies on the deployment of CRs.

2.2.3 Dynamic Spectrum Sharing

Spectrum scarcity is a prevailing challenge in the telecommunications industry, characterized by limited availability, high costs, and uneven utilization. Licensed bands, despite being allocated for specific purposes, often remain occupied for less than 5% of the time at a particular location. In contrast, unlicensed bands are significantly congested [60]. To address this issue, dynamic spectrum sharing (DSS) has emerged as a method to maximize spectrum utilization by enabling secondary users (SUs) to transmit data in unused parts of the spectrum known as spectrum holes, while ensuring minimal impact on the communication performance of primary users (PUs) [61]. The allocation of frequencies in DSS is dynamic and varies based on location and availability.

Two general spectrum access methods are commonly employed. In the overlay/underlay mode, SUs are granted permission to share the spectrum simultaneously with PUs, as long as the SINR of the PUs remains above a specified

threshold. Conversely, in the interleaved scenario, PU spectrum access is guaranteed, and SUs are allowed access to the spectrum only if it is available. The interleaved approach minimizes the risk of collisions between PUs and SUs, as well as the interference caused by SUs to PUs. However, it requires SUs to periodically sense the spectrum and determine the activity of PUs [60]. Consequently, SUs need to be equipped with CRs to detect spectrum holes and identify the suitable channels for transmission [62].

In the context of 5G networks, Pico Cells deployed in ultra-dense areas could greatly benefit from DSS. Various frequency allocations and aggregation policies are being considered to optimize spectrum usage. For instance, the C-band (3.4 to 3.8 GHz) has potential for sharing with satellite systems, offering an opportunity to enhance spectrum utilization [61]. Additionally, the TV white spaces (TVWS) within the VHF and UHF bands (470 to 790 MHz) are an underutilized resource that can be leveraged in DSS scenarios [62]. In a coexistence scenario, NR nodes acting as SUs can have access to the licensed LTE B40 (2.3 to 2.4 GHz), unlicensed 2.4 GHz ISM band (Wi-Fi), and TVWS [62]. The decision to grant access to an SU can be made in a centralized manner, known as spectrum harvesting, where spectrum sensors provide measurement data to a central NR service provider responsible for assigning spectrum to SUs [61]. Alternatively, access can be determined in a distributed manner, where SUs locally sense the spectrum and make individual decisions on transmission [62].

The implementation of 5G NR receivers capable of effectively supporting DSS presents several challenges that require careful consideration and solutions. These challenges include:

1. **Wideband, fast, and high dynamic range spectrum sensing:** To operate in coexistent PU networks, SUs must possess the capability to accurately measure the emitted power across wide channels and different frequency bands. This entails the need for wideband spectrum sensing techniques that can handle the dynamic nature of the spectrum occupancy [60]. Additionally, the varying power levels of different primary users, such as Wi-Fi, LTE, satellite, and TV broadcasting, require SUs to have a high dynamic range in their sensing capabilities [62, 63]. It is also crucial for SUs to perform fast local spectrum measurements and quickly switch between different frequency bands as the spectrum utilization and location of PUs and SUs are constantly changing. However, it is important to note that these requirements can potentially lead to increased power consumption in CR of SUs [60].
2. **Control communications with unlicensed PUs:** In order to effectively manage interference levels and cooperatively optimize DSS in a given time and location, NR SUs need to establish control communications with unlicensed primary users, such as Wi-Fi networks. This communication is necessary to delicately control the interference caused by SUs to Wi-Fi PUs and ensure efficient spectrum sharing [62].

3. **SU-to-SU interference:** In distributed decision-making mechanisms, where SUs autonomously access the available spectrum, the spatial correlation of access opportunities can lead to a significant aggregated interference between NR SUs coexisting in the same location. Therefore, it becomes essential to define interference tolerance requirements and develop interference management techniques to mitigate the impact of SU-to-SU interference in DSS scenarios [63].

2.2.4 SL and SL-Assisted Transmissions

SL communications play a crucial role in 5G networks, serving three key purposes. Firstly, they enable direct data transfer in V2V and D2D scenarios, allowing for localized data processing without the delay associated with transmitting data through BS [64]. Secondly, SL facilitates cooperative relay networks among in-coverage UEs, providing network access for out-of-coverage UEs or when connection with the BS encounters failure [65]. This functionality is commonly known as proximity-based services (ProSe) [66]. Thirdly, SL can establish standalone networks between UEs in emergency situations or natural disasters when the cellular network infrastructure is unavailable [67].

SL resource allocation can be achieved through either centralized or distributed approaches [67]. In the autonomous scenario, each UE needs to sense the availability of candidate resources and determine if they are free or occupied. This involves measuring the total signal power in sub-channels and comparing it to a predetermined threshold. In congested areas, where spectrum congestion is prevalent, UEs must adaptively increase the threshold and identify the most collision-free options [67]. This demands high sensitivity and resolution in spectrum sensing, along with quick measurement capabilities due to the short sensing and selection window [67].

In addition to the need for environment and spectrum awareness, which calls for low-power design, receivers that support SL for URLLC use cases are preferred to be full-duplex (FD) [64]. FD operation allows for simultaneous transmission and sensing, enabling adaptive resource allocation and minimizing the probability of collisions and severe distortion. However, implementing FD introduces challenges related to isolation between RX and TX paths and addressing TX-to-RX SI [64].

It is worth noting that in congested urban areas, where numerous connected devices utilize SL for local communication, the aggregated interference for other UEs, including eMBB users, increases. This highlights the need for better interference rejection capabilities in these devices [67].

2.3 5G Receiver Requirements

The linearity and noise performance of RF receivers are crucial factors in determining their compliance with wireless protocol regulations. To assess whether a receiver meets the rigorous requirements of 5G networks, the 3GPP has established a series of test scenarios and benchmarking metrics for UEs and BSs. In the following subsections, we will explore two categories of verification measures that aim to define the desired levels of receiver linearity and noise performance.

A receiver undergoes testing to obtain approval based on specific conditions involving the desired signal, interferences, and added noise. The test aims to ensure that the communication throughput remains above a certain threshold, often greater than 95% of the maximum achievable value, for a specific reference configuration of CBW, OFDM SCS, and signal modulation [34]. The throughput refers to the successful bit rate, representing the amount of data successfully received in one second. To measure this metric, another parameter called the block error rate (BLER) is typically evaluated first. BLER is defined as:

$$BLER = \frac{num\ of\ NACKs}{(num\ of\ ACKs + NACKS)} \tag{2.4}$$

where NACKs are the number of failed blocks and ACKs are the number of successful blocks. Subsequently, the throughput can be calculated from:

$$Throughput\ [\text{bps}] = (1 - BLER) \times \frac{Bits\ per\ Block}{Transmit\ Time\ per\ Block} \tag{2.5}$$

2.3.1 Sensitivity and Dynamic Range Requirements

In a receiver, various components contribute to the generation of noise, which in turn reduces the input signal-to-noise ratio (SNR_{in}). Consequently, the practical output SNR (SNR_{out}) is always lower than SNR_{in}. The noise figure (NF) is a metric that quantifies this decrease in SNR [68]:

$$NF(dB) = SNR_{in}(dB) - SNR_{out}(dB) \tag{2.6}$$

The noise floor of a receiver refers to the integrated noise power within the channel bandwidth. This noise, as formulated by Equation 2.7, comprises the input thermal noise and the input-referred noise generated by the receiver [68].

$$Noise\ Floor = 10\log_{10}(k_B T \times CBW) + NF \tag{2.7}$$

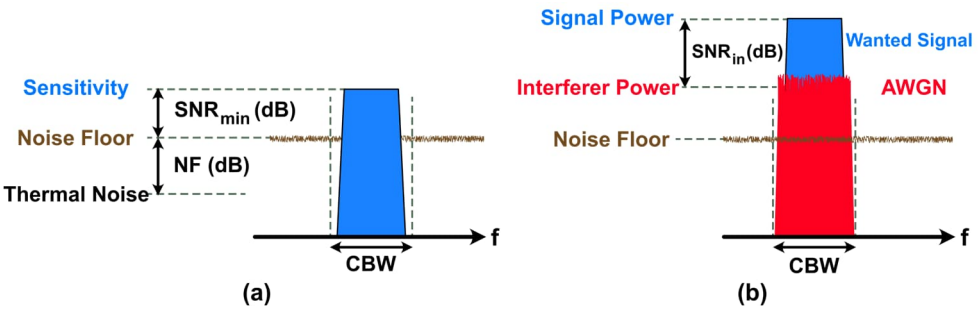

Figure 2.6: (a) Sensitivity and (b) dynamic range test scenarios.

where k_B is the Boltzmann constant, and T is the absolute temperature.

The sensitivity of a receiver refers to the minimum power level required for a desired signal to be successfully received. As mentioned in Section 2.1, each modulated signal requires a minimum SNR (SNR_{min}) for proper detection and decoding. Figure 2.6(a) illustrates the relationship between the sensitivity level (P_{sen}), NF, and SNR_{min}, which can be expressed as follows [68]:

$$P_{sen} = 10\log_{10}(k_B T \times CBW) + NF + SNR_{min} \tag{2.8}$$

In accordance with this equation and the sensitivity levels specified by the 3GPP for NR UE [34] and various NR BSs [39], the maximum acceptable NF at the room temperature (i.e., T=300°K) can be determined as presented in Table 2.3. It is important to note that these calculations incorporate a MIMO diversity gain of 6 dB and 3 dB for BSs and UE, respectively [42]. Wide-area BSs receive severely faded and attenuated UL signals from long distances; therefore, they must have the lowest sensitivity level. In contrast local-area BSs are closer to UEs allowing for a more relaxed sensitivity requirement.

Dynamic range (DR) is another key performance metric of receivers, defined as the range of input power levels over which the receiver can capture and detect desired signals. As mentioned earlier, the minimum input level is determined by the noise floor. On the other hand, the receiver's supply voltage, technology, and circuit architecture restrict the maximum power level, known as full-scale power (P_{FS}).

Table 2.3: Sensitivity levels, maximum acceptable NF, and required dynamic range of NR receivers.

Type of Receiver	Sensitivity level (dBm)	NF_{max} (dB)	Maximum IL (dB)	Minimum DR (dB)
Wide-area BS	-95.7	5.1	5.3	-
Medium-range BS	-90.7	10.1	5.6	-
Local-area BS	-87.7	13.1	5.3	-
UE[1]	-86.5	11	-	64.4

CBW = 100 MHz, SCS = 60 kHz, SNR_{min} = -1 dB, [1] calculated for n41 band.

However, due to nonlinearity effects, impairments and mismatches, the noise performance of receivers degrades in the presence of large signals and strong interferers. Consequently, there is a loss in the full-scale power and a practical back-off margin must be considered. This margin is referred to as implementation loss (*IL*) [48]. Hence, the dynamic range can be given by

$$DR = P_{FS} - IL - Noise\ Floor \tag{2.9}$$

In the 3GPP receiver requirements for BSs, a test illustrated in Figure 2.6(b) is considered to ensure that *IL* remains below an acceptable threshold. In this test an additive white Gaussian noise (AWGN) interfering signal is applied in the same channel alongside a 16-QAM NR signal [34]. The *IL* must be low enough to maintain the throughput above 95% of its maximum achievable value. For UEs, the 3GPP has clearly specified the maximum input level. Using Equation 2.9 and the values of SNR_{in} from the specifications, we can derive the required *DR* or *IL* of receivers as presented in Table 2.3.

2.3.2 Linearity Requirements

Amplifiers, filters, data converters, and other building blocks of receivers are constructed using inherently nonlinear electronic components such as transistors, diodes, and MOS capacitors. Thus, receivers behave differently when subjected to small or large input signals. While local linearization can be adopted for small signal fluctuations around an operating point, a general nonlinear model must be employed for design and simulations when dealing with large signals.

For a memoryless nonlinear time-invariant (NLTI) system, the mathematical relationship between the input (x) and output (y) can be represented using Taylor expansion as follows:

$$y = \sum_{k=0}^{\infty} \alpha_k x^k = a_0 + a_1 x + a_2 x^2 + a_3 x^3 + \cdots \tag{2.10}$$

When the input consists of a single-tone signal, a nonlinear system produces harmonics and experiences gain compression, where the fundamental gain decreases with increasing input amplitude, eventually leading to output saturation.

For an input with N constituent signals (including desired signals, aggregated channels, and interferers), the relationship can be written as:

$$y = \sum_{k=0}^{\infty} \alpha_k x^k = \sum_{k=0}^{\infty} \alpha_k \left(\sum_{l=1}^{N} x_l \right)^k \tag{2.11}$$

The two-tone test is a widely adopted method for evaluating the linearity of RF receivers. It involves feeding in two continuous wave (CW) signals, with the same amplitude and a specific frequency spacing, into the receiver, and then tracking the fundamental output and intermodulation products as the amplitude of the CW signals is swept [68]. As demonstrated in Figure 2.7(a), two intercept points are measured and used as performance metrics. The second-order intercept point (IP2) and the third-order intercept point (IP3) indicate the input power levels at which the second-order and third-order intermodulation products (IM2 and IM3) intersect the fundamental output, respectively. These input power levels are denoted as IIP2 and IIP3, while their corresponding output power levels are referred to as OIP2 and OIP3. Using Equation 2.11, IIP2 and IIP3 can be expressed as [68]:

$$IIP_2 = \frac{2\alpha_1}{\alpha_2}, \qquad IIP_3 = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.12}$$

However, in practical measurements, IIP2 and IIP3 cannot be measured directly since the output power saturates before reaching these levels. Hence, linear small-signal trends of fundamental output, IM2 and IM3 are extrapolated to estimate these intercept points.

Additionally, Figure 2.7(a) highlights two other commonly used metrics to benchmark the linearity of receivers. These metrics are the output saturation level (P_{sat}) and the 1-dB compression point (P_{1dB}). P_{sat} corresponds to the output power level at which the receiver's performance reaches saturation. On the other hand, P_{1dB} represents the input power level at which the power gain drops by 1 dB from its small-signal value [68].

In realistic operational scenarios, NR receivers that support CA typically encounter a multiple-tone input signal. Assuming that the input signal consists of N CW signals at N different carrier frequencies, the receiver generates numerous

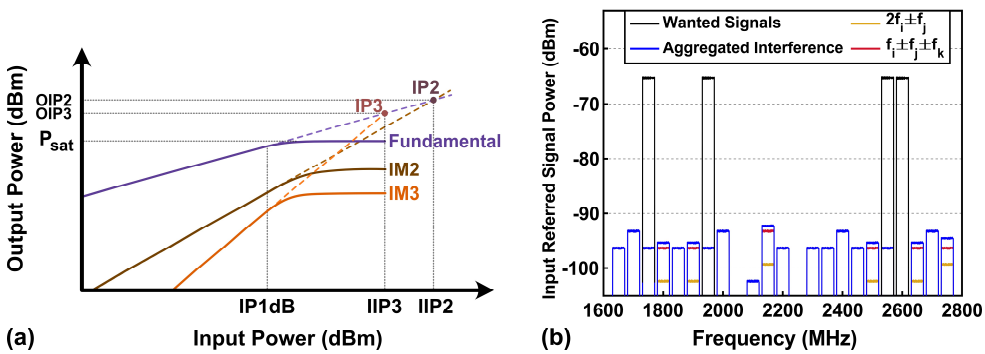

Figure 2.7: (a) Typical input-output characteristic of the fundamental, second-order, and third-order intermodulation products. (b) An example of the aggregated interference.

intermodulation products and harmonics. More precisely, the output spectrum includes frequency components at $\sum_{l=1}^{N} m_l f_l$, where m_l can theoretically be any integer. However, in practical situations, the high-order nonlinear components in Equation 2.11 are considerably weaker than the first three terms, making them negligible for most applications. As a result, assuming N sinusoidal signals at frequencies $f_1, f_2, ..., f_N$ as input, the output spectrum exhibits frequency components as presented in Table 2.4. This table also shows the number of frequency components in each group and their respective amplitudes.

In the case of 4-CC CA and the presence of two in-band interfering signals, a receiver with only third-order nonlinearity ($\alpha_2 = 0$) generates 140 intermodulation products. As illustrated in Figure 2.7(b), a number of these intermodulation products fall within the band-of-interest and, without proper in-band filtering, they can enter the receiver, causing distortion and degrading the throughput. Combining the power of all these in-band intermodulation products results in what is known as the "aggregated interference" [69]. Given the large number of these products distributed across the bandwidth, this aggregated interference can be considered as a degradation of the dynamic range of the receiver, acting similar to a higher noise floor. Furthermore, the strongest frequency component in this spectrum determines the spurious-free dynamic range (SFDR), setting the limit for the receiver's capability to withstand strong unwanted signals, commonly referred to as blockers.

Frequency-Dependent Nonlinearity

The assumption of a memoryless system becomes invalid at high frequencies due to the presence of energy-storing elements like inductors and capacitors in electronic circuits. In other words, the response of a circuit depends not only on its input at the

Table 2.4: Output frequency components of a third-order nonlinear system.

Output Frequency component	Number of components	Amplitude
f_j	N	$\alpha_1 A_j + \frac{3\alpha_3}{4} A_j^3 + \frac{3\alpha_3}{2} A_j \sum_{k \neq j} A_k^2$
$2f_j$	N	$\frac{\alpha_2 A_j^2}{2}$
$f_j \pm f_k$	$N(N\text{-}1)$	$\alpha_2 A_j A_k$
$3f_j$	N	$\frac{\alpha_3}{4} A_j^3$
$2f_j \pm f_k$	$2N(N\text{-}1)$	$\frac{3\alpha_3}{4} A_j^2 A_k$
$f_j \pm f_k \pm f_l$	$4\binom{N}{3}$	$\frac{3\alpha_3}{2} A_j A_k A_l$

current instant but also on all the previous inputs it has received over time. Consequently, the linearity performance metrics become frequency dependent, and the amplitude of intermodulation products varies throughout the bandwidth.

At higher frequencies, the Taylor expansion, which neglects memory effects, leads to inaccurate analytical predictions, especially for even-order intermodulation products [70, 71]. Although the power gain's Taylor expansion for a differential implementation suggests that these products only exist in the presence of a degree of mismatch, considering memory effects at high frequencies reveals that these distortions are generated even for completely matched circuits.

To overcome these limitations, the Volterra series is an analytical tool that replaces the Taylor expansion. Using Volterra series, the output signal is expressed as

$$y = \sum_{k=0}^{\infty} H_k[x] = \sum_{k=0}^{\infty} H_k\left[\sum_{l=1}^{N} x_l\right] \tag{2.13}$$

In this equation $H_k[.]$ represents the k-th order Volterra operator [70]. By translating this equation into frequency domain and using the phasor representation of signals, we can derive the output frequency spectrum. This enables us to express frequency-dependent metrics, such as IIP3, as follows:

$$IIP_3 = \sqrt{\frac{4}{3}\frac{|H_1(f_1)|}{|H_3(f_1, f_1, -f_2)|}} \tag{2.14}$$

where H_1 and H_3 are the frequency domain Volterra kernels [70]. This equation reveals that the IIP3 varies with carrier frequencies, and the intermodulation products at $2f_1$-f_2, $2f_1$+f_2, $2f_2$-f_1, and $2f_2$+f_1 may have different amplitudes. This observation sharply contradicts the predictions of the Taylor expansion, and it aligns more accurately with the experimental findings [71].

Blocking Requirements

Blocking requirements are essential for assessing a receiver's ability to withstand strong interferers while maintaining an acceptable level of throughput. In wireless standards, the power of interfering signals and their corresponding frequency offsets from the desired channel are defined. Based on the interferer's location with respect to the assigned channel, these requirements can be categorized into four groups:

1. **Adjacent channel selectivity (ACS):** As depicted in Figure 2.8(a), the NR interfering signal is present within the adjacent channel, at a frequency offset from the edge of the assigned channel. The ACS determines the required roll-off and order of the channel selection filter (CSF).

2. **In-band blocking (IBB):** In this case, the NR interfering signal exists within the same NR band as the wanted signal. Typically, a margin is considered when defining in-band and OOB regions. For example, the 3GPP has defined the in-band region for bands wider than 100 MHz as extending 60 MHz below the lower edge to 60 MHz above the upper edge of the band [39].
3. **Out-of-band blocking (OBB):** As shown in Figure 2.8(b), in this scenario, a strong CW blocker falls outside the band-of-interest. This requirement determines the characteristics of the band selection filter.
4. **Narrowband blocking (NBB):** This measure evaluates the receiver's ability to resist the presence of a narrowband (CW or single RB) blocker located very close to the edge of the channel. Filtering out such a blocker proves to be considerably difficult. As a result, it is imperative to take this requirement into account when calculating the minimum acceptable compression point and the tolerable margin of NF degradation.

The blocking requirements can be summarized as shown in Figure 2.8(b), with the red profile indicating the average power levels of blockers at various frequency distances from the desired channel. Table 2.5 presents the required blocker levels specified by the 3GPP. From these numbers, several conclusions can be drawn:

1. LA BS receivers, which typically operate in congested areas and indoors, have the most stringent linearity requirements to meet.
2. Assuming 10 dB margin for gain compression and 3 dB PAPR for CW interferers, the part of the receiver chain preceding the band selection filter must have a P_{1dB} higher than -2 dBm.
3. For the part of the receiver chain before the channel selection filter, which includes the band selection filter, the in-band P_{1dB} must be higher than -17,

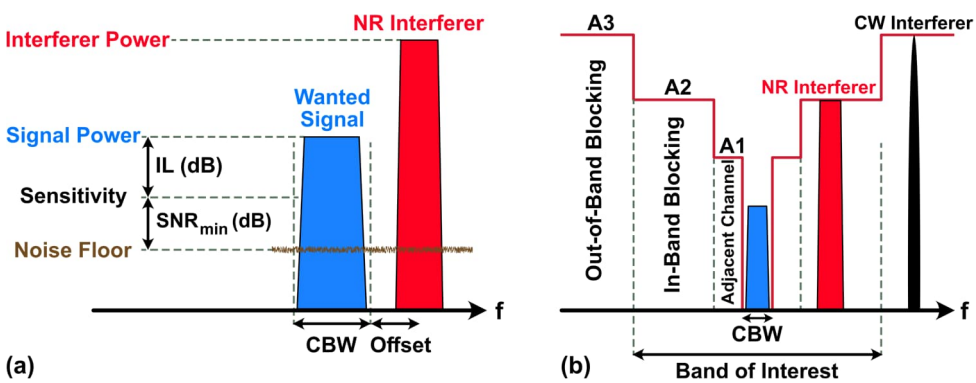

Figure 2.8: Frequency and power level arrangement in linearity test scenarios: (a) Adjacent channel selectivity test. (b) Blocking tests.

Table 2.5: Power levels and frequency offsets in blocking requirements.

Type of Receiver	ACS			IBB			OBB			NBB		
	P_{sig}	A1	Offset	P_{sig}	A3	Offset	P_{sig}	A2	Offset	P_{sig}	P_{int}	Offset
	dBm	dBm	MHz	dBm	dBm	MHz	dBm	dBm	MHz	dBm	dBm	kHz
WA BS	-89.7	-52	9.47	-89.7	-43	30	-89.7	-15	60	-89.7	-49	565
MR BS	-84.7	-47	9.47	-84.7	-38	30	-84.7	-15	60	-84.7	-44	565
LA BS	-81.7	-44	9.47	-81.7	-35	30	-81.7	-15	60	-81.7	-41	565
UE[1]	-72.5	-53.4	2.5	-73.7	-44	12.5	-70.5	-15	85	-70.5	-55	840

CBW = 100 MHz, SCS = 60 kHz, [1] calculated for n41 band.

-20, -25, and -26 dBm for LA BS, MR BS, WA BS, and UE, respectively. The PAPR of NR interfering signal is assumed to be 8 dB [72].

4. The full receiver chain must have an in-channel P_{1dB} of at least -26, -29 -34, and -35.4 dBm for LA BS, MR BS, WA BS, and UE, respectively.
5. The NF degradation of the receiver in the presence of a -15 dBm blocker should not exceed 6 dB to ensure the same throughput as in a blocker-free situation.

Intermodulation Requirements

These requirements establish the minimum intermodulation rejection needed to maintain throughput in the presence of two or more interfering signals with specified power levels and center frequencies. Figure 2.9(a) illustrates the test configuration defined by the 3GPP, where the IM3 of a CW interferer and a NR interfering signals falls within the channel-of-interest. Table 2.6 provides the attributes of these signals. The minimum required in-band IIP3 has been calculated from these data by using the following equation [73].

$$IIP_3 = \frac{2P_{int\_CW} + P_{int\_NR} - \left(P_{sig} - SNR_{min} - IL - M_{PVT}\right)}{2} \qquad (2.15)$$

The values obtained from Equation 2.15 ensure that the third-order intermodulation distortion (IMD_3) remains sufficiently low to achieve the required SNR, while considering the IL and a margin for process-voltage-temperature (PVT) variations (M_{PVT}). In our calculations, we have incorporated a 10 dB margin for *IL* and M_{PVT} combined.

More complex test scenarios are also defined for various CA configurations. For instance, in Figure 2.9(b), the IM3 of an NR interfering signal and one of the desired signals in Band B appears in Band A. These test setups ensure comprehensive evaluation of the receiver's performance in real-world scenarios with multiple interfering signals.

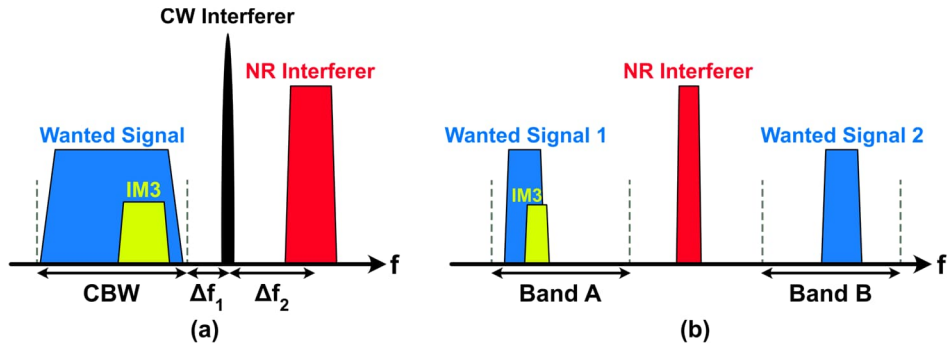

Figure 2.9: Frequency and power level arrangement in intermodulation test scenarios: (a) Two-tone test. (b) CA scenario.

2.3.3 Necessity of Multiple Mode Operation

To successfully pass sensitivity and blocking tests and meet challenging noise and linearity requirements, reconfigurability is a crucial aspect for modern receivers. Figure 2.10 illustrates four different modes of operation for a receiver, depending on the power levels of the desired signal and blocker:

- **Mode 1, high-sensitivity mode:** In this mode, the wanted signal is extremely low-power and the blocker's power is well below the gain compression point. As a result, the receiver is configured for high-performance, high-gain, low-noise operation.
- **Mode 2, highly linear mode:** Here, the wanted signal remains low-power, but the blocker is strong. In this scenario, the receiver may slightly sacrifice NF for enhanced linearity. Compared with Mode 1, a minor degradation in NF is acceptable.
- **Mode 3, high-tolerance mode:** In this mode, both the wanted signal and the blocker are of high amplitude. The receiver must switch to a low-gain, extremely blocker-tolerant configuration, where NF can be compromised for the sake of improved linearity.

Table 2.6: Intermodulation requirements.

Type of NR Receiver	P_{sig} (dBm)	P_{int_cw} (dBm)	P_{int_NR} (dBm)	Δf_1(MHz)	Δf_2(MHz)	$IIP3_{min}$ (dBm)
WA BS	-89.7	-52	-52	7.48	25	-28
MR BS	-84.7	-47	-47	7.48	25	-23
LA BS	-81.7	-44	-44	7.48	25	-20
UE[1]	-70.5	-46	-46	7.5	CBW/2+7.5	-29

CBW = 100 MHz, SCS = 60 kHz, [1] calculated for n41 band.

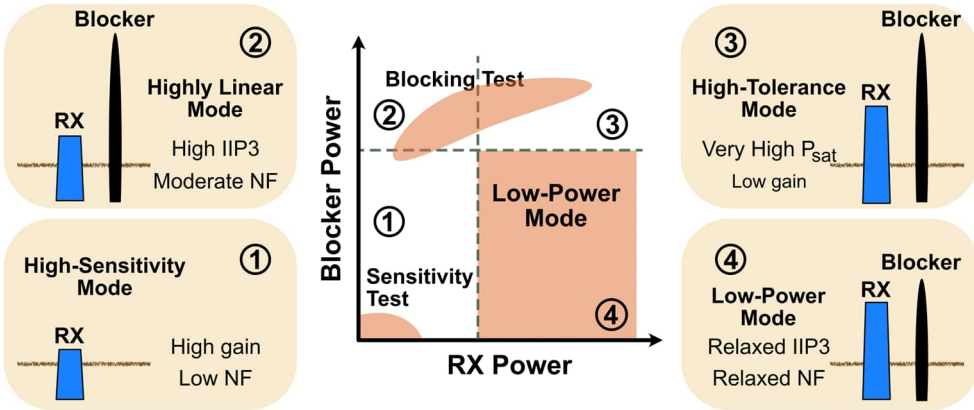

Figure 2.10: Operational modes of a reconfigurable receiver (reproduced from [74]).

- **Mode 4, low-power mode:** In this mode, the power levels of both the wanted signal and the blocker are moderate. Consequently, the receiver can compromise both NF and IIP3 for the purpose of achieving lower power consumption.

2.4 Receivers Architectures for Multi-Band Operation

From an architectural point of view, a wireless receiver serves four essential functions: RF signal conditioning, mixing, sampling, and digitizing. Figure 2.11 demonstrates a generic receiver chain comprising analog, mixed-signal, and digital units. Signal conditioning primarily involves impedance matching, amplification, and band-select filtering, all of which occur in the analog domain. Down-conversion mixing translates RF signals to IF in case of heterodyne, or to baseband in case of homodyne/zero-IF receivers. The sampler acts as the gateway between the continuous-time and discrete-time signal processing domains. Finally, an ADC quantizes analog signals, enabling further processing in the digital domain.

The digital front-end (DFE) utilizes a multitude of complex digital signal processing (DSP) units for various tasks, such as digital channel selection (DCS), digital down-conversion (DDC), demodulation, error minimization, interference cancellation, and spectrum sensing.

In the context of multi-band radios, particularly in the study of receiver architectures that support CA, EN-DC, and DSS, we can classify the state-of-the-art receiver front-ends based on where the frontier between the analog front-end (AFE) and DFE is established. This classification depends on two factors: the frequency at which the signal is sampled and how the task of frequency translation

is shared between the analog, mixed-signal, and digital components. Consequently, we can identify three categories of multi-band receivers:

1. Baseband/low-IF sampling receivers
2. Digital-IF receivers
3. Direct RF-sampling receivers

2.4.1 Homodyne, Low-IF, and Double-Conversion Receivers

In these receivers, the frequency translation is entirely achieved by analog mixers, and the down-converted version of signals is sampled. This approach relaxes the requirements of the ADC design. To implement concurrent multi-band receivers, the most straightforward method is to use multiple narrowband homodyne or Low-IF receiver chains in parallel. Each path is dedicated to a single carrier component. To conserve power consumption and occupied area, the frequency range of the receiver is divided into a few subranges, each containing a group of bands. For instance, [75] considers three subranges within NR FR1. In this implementation, two, seven, and three chains are assigned to low bands (< 1 GHz), mid bands (1.4 to 2.7 GHz), and high bands (> 3.2 GHz), respectively.

Since these paths are optimized for narrowband operation and they are isolated, this implementation can achieve high dynamic range and reliability. However, the high level of parallelization and secondary effects of nonlinearities, parasitic coupling, and leakage, along with high power consumption and large occupied area, create several challenges in realizing efficient integrated versions of this type.

As an example of this category, Figure 2.12 illustrates the architecture of an *m*-path receiver consisting of two antennas and both homodyne and low-IF chains. Paths 1, 2 and 3 share ANT1 to capture three CCs within the band A, while paths 4 to *m* are connected to ANT2, receiving CCs from the band B.

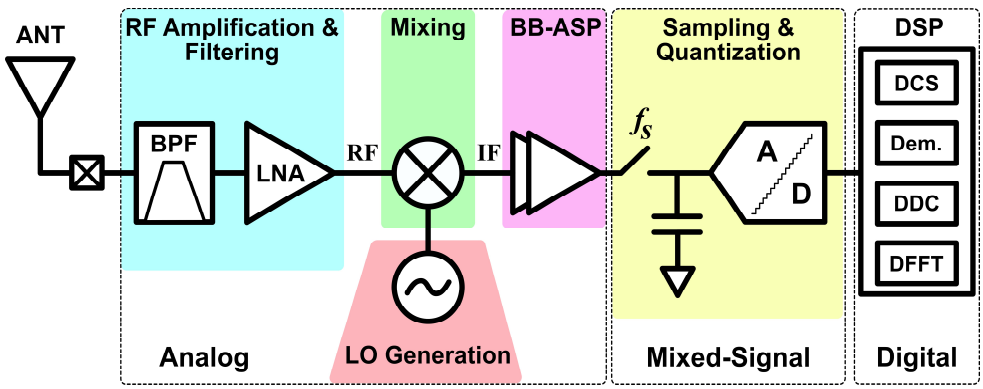

Figure 2.11: Generic architecture of a receiver.

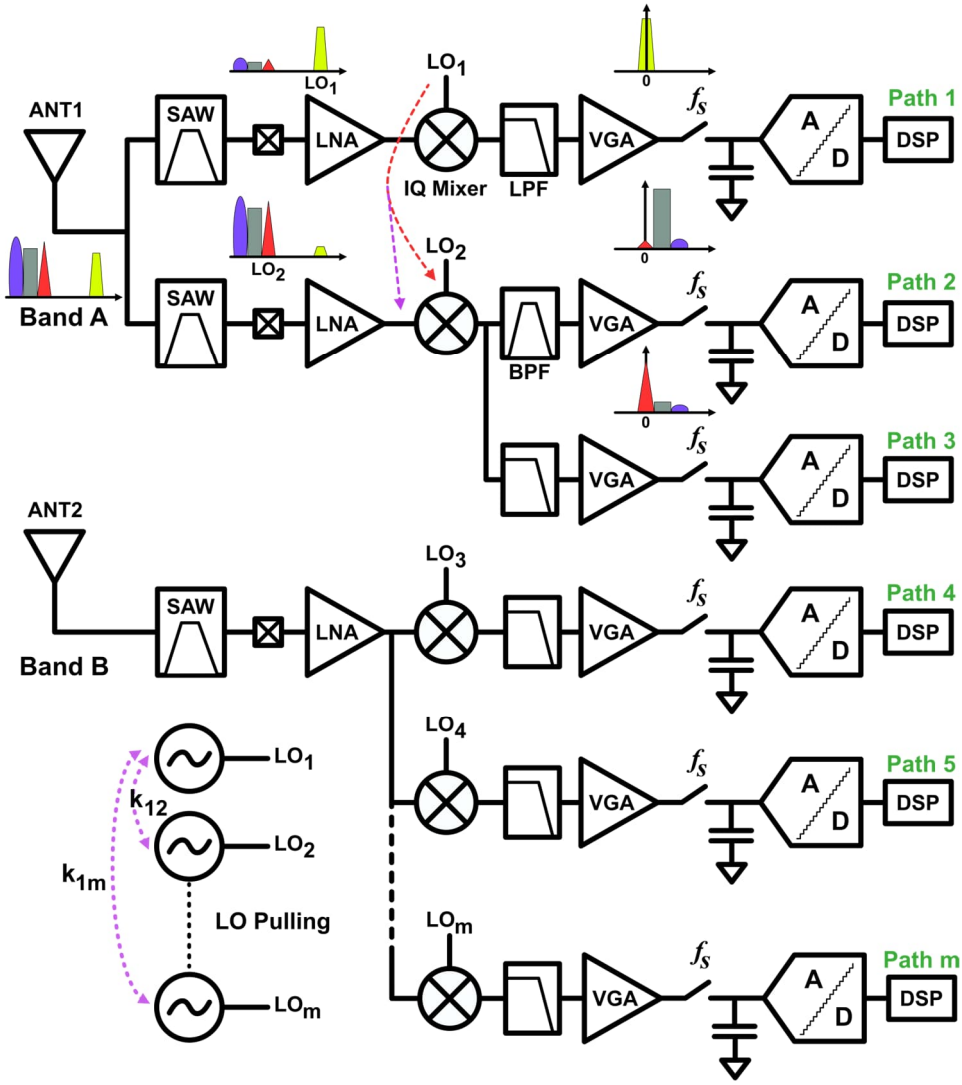

Figure 2.12: Architecture of a multiple-path homodyne/low-IF receiver.

Path 1 is a homodyne chain comprising a band-select SAW filter to reject OOB interferers, an LNA to amplify the desired signal and provide input matching, a mixer to directly down-convert the RF signal to the baseband, a baseband low-pass filter (LPF), a programmable gain amplifier (PGA), and ultimately a Nyquist-rate sampler. Since the efficient implementation of a high-order LPF at the baseband is viable, this chain can successfully filter out the adjacent channels and close-in blockers. However, homodyne receivers suffer from DC offsets generated by LO-

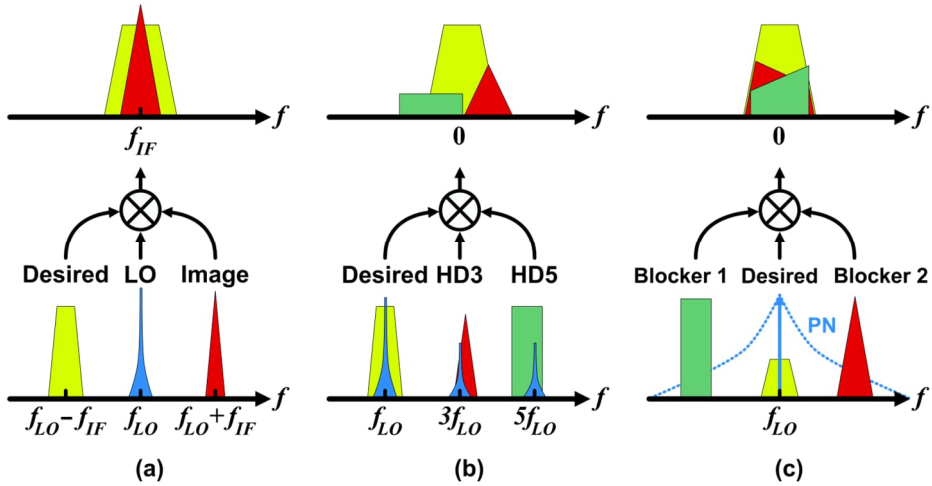

Figure 2.13: (a) Image problem. (b) Harmonic down-conversion. (c) Reciprocal mixing.

to-RF leakage in the mixer, which can saturate baseband stages. In addition, the flicker noise is more pronounced at lower frequencies, limiting the output SNR [48].

Path 2 is a Low-IF receiver chain where the desired RF signal is translated to a few tens of MHz IF. Low-IF receivers are free from DC offset and flicker noise issues, but they face an image problem. As depicted in Figure 2.13(a), both the desired signal and the interfering signal fall at f_{IF} after mixing. Therefore, the image signal must be filtered out before mixing by making use of high-quality factor (high-Q), high-order RF filters, which are challenging to be efficiently realized in integrated solutions [48]. Although quadrature mixers are employed to separate desired and image signals, in this approach, the image rejection ratio (IRR) is prone to phase-amplitude (I-Q) imbalance [48].

Furthermore, in a multi-path receiver, it might be possible to share some parts of the receiver chain between different paths. For example, Path 2 and Path 3 share the antenna, band-select filter, LNA and mixer. Such sharing enables "block down-conversion", which is suitable for contiguous CA [76, 77]. The "block" refers to a couple of adjacent CCs. In this method, the LO frequency is set close to the edge of the block to down-convert all the CCs to the baseband/low-IF together. Then, baseband high-Q LPFs, BPFs, and complex mixers are employed to separate different channels. However, block down-conversion cannot be easily reconfigured for more than three channels or more complicated intra-band and inter-band CA. Moreover, complex baseband signal processing requires multiple feedback loops, which raises stability concerns, limiting the operational bandwidth of the receiver to a few tens of MHz, which does not match wide CBWs of 5G NR signals [78].

Another aspect of multi-path receivers is the parasitic interactions between voltage-controlled oscillators (VCOs) utilized in the LO generation unit and the crosstalk between LO distribution networks. The inter-coupling between VCOs

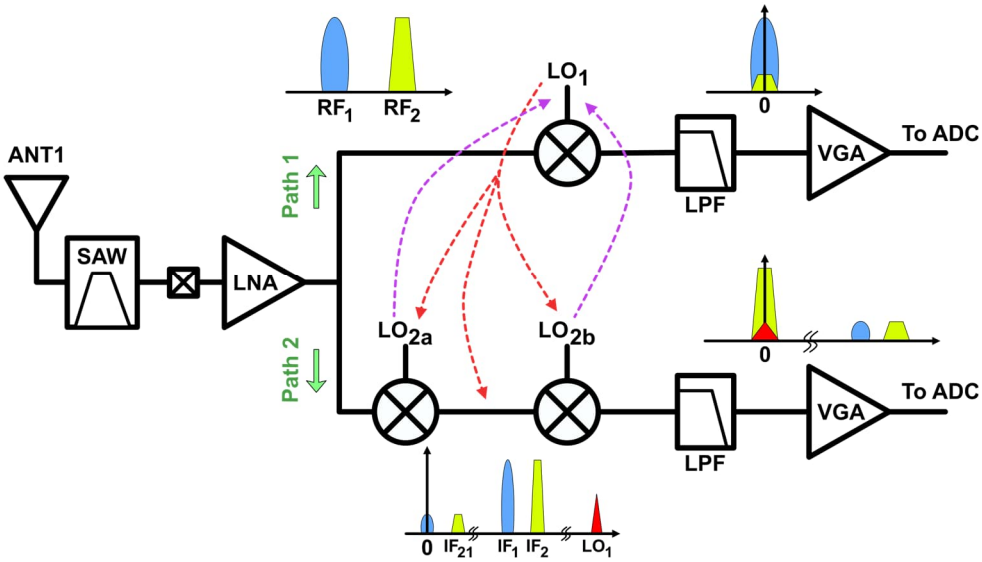

Figure 2.14: Architecture of a dual-path double-conversion/super-heterodyne receiver.

causes the pulling effect, a deviation in LO frequencies that drastically degrades the receiver's performance [79].

Moreover, the intermodulation products of LO signals leaked to the RF and LO ports of mixers introduce in-band interference to the down-converted signal. Specifically, in the congested spectrum of NR FR1, two well-investigated drawbacks of analog mixing play a detrimental role in limiting the received signal to noise and distortion ratio (SNDR). These two mechanisms are harmonic mixing and reciprocal mixing, illustrated in Figure 2.13(b, c). The former refers to mixing with the harmonics of LO signal, and the latter denotes the mixing of close-in blockers with the skirt of the phase noise generated by LO PLLs [68].

To mitigate pulling and intermodulation effects, more complex LO planning has been proposed. The purpose is to widen the frequency spacing between LOs, thereby pushing the IM products out of the desired frequency band and distancing the resonant frequency of VCOs. As an example, Figure 2.14 demonstrates a receiver with homodyne and double-conversion paths [79], where

$$f_{RF1} = f_{LO1}, \qquad f_{RF2} = f_{LO_{2a}} + f_{LO_{2b}} \tag{2.16}$$

By carefully choosing the frequencies of LO_{2a} and LO_{2b}, it is possible to minimize in-band IM distortion. However, from the spectrum plots in this figure, we can see that some distortions still fall at DC. These distortions stem from two main mechanisms: 1) self-mixing of LO signals leaked to another path due to LO-to-LO

and LO-to-RF leakage, and 2) second-order IM between LO_{2a} and LO_{2b} leakage to LO_1 [80].

Furthermore, each double-conversion receiver chain requires two LOs, which complicates layout and doubles power consumption for LO generation and distribution (buffers and dividers). A solution to this could be the deployment of sliding-IF structure in which LO_{2b} is produced by dividing LO_{2a}, hence, one PLL is enough for each path [81]. However, sliding-IF restricts the frequency planning and reconfigurability of the system to operate in a broad frequency range and support a wide variety of BWs and CA scenarios.

Among other superheterodyne and double-conversion architectures, multiple-phase mixing [80], recentering [82], and harmonic recombining [83] are notable. Although these techniques are successful in reducing spurs and pulling effects, they lack enough reconfigurability, and they require numerous PLLs, frequency dividers, and buffers, resulting in excessive power consumption and crosstalk.

2.4.2 Digital-IF Receivers

To enhance power efficiency and address crosstalk issues in multi-path double-conversion receivers, a promising approach involved shifting quadrature mixing and baseband filtering to the digital domain [48]. As depicted in Figure 2.15, an analog mixer down-converts RF signals to a relatively high IF. The second frequency translation to the baseband is then carried out by digital quadrature mixers fed by numerically controlled oscillators (NCOs). Subsequently, the channel selection is performed by using high-order digital CSFs. The number of CCs aggregated in a single band-of-interest determines the number of required digital paths.

By capturing multiple channels at once, a single digital-IF path can perform the tasks of several fully analog chains. Furthermore, through dynamic adjustments in frequency planning, ADC resolution, and bandwidth of the receiver, this design can be reconfigured for various CA combinations, offering superior power efficiency, reduced implementation costs, and effectively mitigating issues like DC offset, TX-to-RX leakages, I/Q mismatch, self-mixing, and flicker noise [84, 85].

Despite these advantages, digital-IF receivers face some challenges and limitations, primarily related to the ADC:

1. **Sampling Rate and Bandwidth:** Digital-IF receivers rely on high-speed ADCs to effectively sample wideband signals. As the receiver's bandwidth increases, the required sampling rate also escalates, leading to higher power consumption and increased complexity. According to the Nyquist sampling theorem, the sampling frequency (f_s) must be greater than the Nyquist rate, expressed as:

$$f_s \geq 2f_{max} \tag{2.17}$$

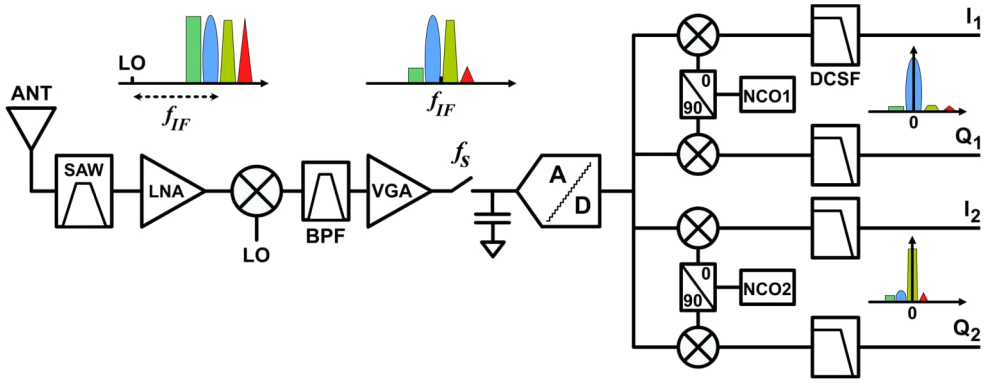

Figure 2.15: Architecture of a digital-IF receiver.

where, f_{max} represents the maximum frequency component of the sampled signals [48]. For instance, in scenarios like 3CC contiguous CA, with a total bandwidth of 300 MHz, the track-and-hold circuit needs at least 300 MHz input bandwidth, and the ADC requires a 600 MHz clock frequency. However, in cases of relatively narrowband channels where the ratio of CBW to f_{IF} is small, the sampling rate can be reduced, and subsampling ADCs can be employed [48], where:

$$f_S \geq 2CBW \tag{2.18}$$

In subsampling, a copy of the desired signal is captured from one of the non-fundamental Nyquist zones. To enable IF subsampling, precise frequency planning is essential. The relationship between the center frequency of the desired signal, the location of potential interferences, the sampling rate, and f_{IF} must be carefully considered to avoid aliasing and SNDR degradation. Maintaining these relationships across all CA scenarios makes the use of the digital-IF architecture challenging and demands widely adjustable LO-PLL and sampling rates [86].

2. **Interference filtering:** In digital-IF receivers, the primary interferences of concern are in-band blockers, TX leakage, image signals, and aliased signals [85]. Although a large IF can alleviate the requirements of the image-reject filter (IRF), aliasing becomes a concern as it can fold IB and OOB blockers onto the desired signal. Consequently, a high-order, high-Q anti-aliasing filter (AAF) at the IF frequency is necessary to be placed before the sampler. This filter plays a crucial role in mitigating noise folding as well [86]. For subsampling ADCs, aliasing is even more pronounced, demanding even sharper bandpass AAFs [48].
3. **Mismatch in interleaved ADCs:** To achieve wideband digitization, parallel sampling is a widely used solution. Time-interleaved ADCs (TI-

ADCs), hybrid filter band (HFB), and quadrature frequency-interleaved ADCs (QFI-ADCs) are a few examples of these multiple-channel data converters [48, 87]. However, these ADCs can generate distortion due to jitter and mismatch in gain, offset, and transfer function. This necessitates the deployment of digital calibration schemes to accurately reconstruct the sampled signals [87].

4. **Noise and dynamic range:** Since close-in blockers and adjacent channels are not sufficiently rejected by either band-select filter or AAF, the ADC requires high dynamic range and low noise performance [48]. Regarding the required ACS and SNR_{out} for 5G NR receivers, the effective number of bits (ENOB) of the ADC requires to be greater than eight. Oversampling can be employed to enhance dynamic range by $10\log_{10}(OSR)$, where OSR denotes the oversampling ratio as expressed below.

$$OSR = \frac{f_s}{2CBW} \tag{2.19}$$

   However, oversampling gain comes at the expense of higher power consumption [85].
5. **Limitations for inter-band CA:** To support inter-band CA scenarios, two approaches can be considered: either increasing the IF and sampling rate in proportion to the total bandwidth of all involved bands or using multiple digital-IF chains in parallel [85]. The former choice reduces the gap between IF and RF frequency, requiring Gsps ADCs, which ultimately eliminates the need for an analog mixer, transforming the digital-IF architecture into a direct-RF sampling receiver, as is discussed in the following section. On the other hand, the latter choice introduces issues of leakage and crosstalk.

It is worth mentioning that among different types of ADCs, bandpass ΔΣ ADCs and time-interleaved successive approximation register (TI-SAR) ADCs are more commonly employed in digital-IF receivers. Bandpass ΔΣ ADCs can combine frequency translation, filtering, and quantization functions [84]. TI-SAR ADCs are favored for low-power, low-voltage applications. Although the thermal noise of TI-SAR ADCs becomes a prominent factor in degrading SNR at high frequencies, the dynamic range requirement can typically be met using oversampling [85].

2.4.3 Direct RF-Sampling Receivers

As discussed in Chapter 1, advanced CMOS technologies have proven to be highly beneficial for digital and switching circuits. The direct RF-sampling architecture is an approach aimed at bringing the digital front-end as close as possible to the antenna, leveraging the advantages of ultra short-channel MOS devices, and

expediting receiver design by means of digital synthesis, power optimization, and place-and-route tools [88].

In our journey from analog homodyne to less-analog digital-IF receivers, we can take a step further towards digital-intensive receivers by eliminating analog mixers. This approach down-converts RF signals to the baseband solely through sampling and digital processing. By doing so, challenges related to image rejection, reciprocal mixing, and harmonic mixing are circumvented, and the multi-band receiver enjoys more versatility [89].

Neglecting secondary effects, a sample and hold (S/H) circuit can be modeled by a switch with an ON-resistance of r_{ON} in series with a sampling capacitor (C_{SH}). Successful reconstruction of the sampled signal requires that the input bandwidth of the S/H (Δf_{in}) be greater than the signal's bandwidth (Δf_{sig}). This condition can be expressed as [89]:

$$\Delta f_{in} = \frac{1}{2\pi C_{SH} r_{ON}} = (1 + |\delta|)\Delta f_{sig} \tag{2.20}$$

where δ is a parameter determined by the desired flatness of the gain and implementation margins. From this equation we observe that to digitize wider channels or contiguous CA of several channels while maintaining noise and power consumption constant, lower r_{ON} is required, implying the use of larger switches. However, the gate capacitor (C_{SW}) of the switch can deteriorate the SFDR of the S/H through charge sharing and clock feedthrough mechanisms. A larger switch has a larger gate capacitance, leading to a trade-off between bandwidth and SFDR of the ADC. Nevertheless, technology scaling can partially relax this trade-off, enabling the realization of sufficiently high dynamic range wideband ADCs. This can be seen from the first-order approximation of the gate capacitor given by [89]:

$$C_{SW} \cong \frac{1}{2\pi r_{ON} f_T} = \frac{(1 + |\delta|)\Delta f_{sig}}{f_T} C_{SH} \tag{2.21}$$

where f_T is the transit frequency of the switch, a characteristic of technology nodes in connection with their speed. Higher-f_T technology nodes allow sampling of larger bandwidths while maintaining the same performance.

Power consumption is another critical performance metric of ADCs, which can be expressed as [89]:

$$P_{ADC} \cong \sum_j \alpha_j C_j V_{dd}^2 f_s \tag{2.22}$$

where the capacitors C_j represent the internal capacitors of switched-capacitor stages, and the coefficients α_j stand for the activity factor in charging/discharging of

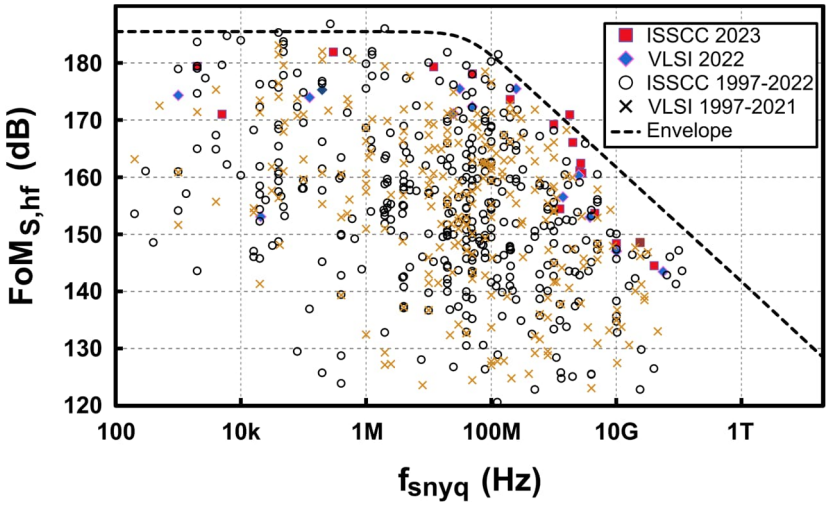

Figure 2.16: ADC performance survey [91].

the capacitors, incorporating the power dissipation in stray capacitances, operational amplifiers, and capacitor. Considering the thermal noise of switched-capacitor circuits as k_BT/C, for the same noise power density, we keep the capacitors constant. Therefore, the power consumption of an ADC can be assumed as a linear function of its sampling rate.

The trade-offs between noise, dynamic range, sampling rate, and power consumption of ADCs are combined in the well-known Schreier's figure of merit ($FoM_{S,hf}$) as follows [90]:

$$FoM_{S,hf} = SNDR + 10\,log\left(\frac{f_s/2}{P_{ADC}}\right) \tag{2.23}$$

By substituting Equation 2.22 into Equation 2.23, we might expect to observe constant $FoM_{S,hf}$ with respect to f_s. However, as shown in Figure 2.16, this FoM declines for the sampling frequencies above 100 MHz, suggesting that technological limitations make the realization of multi-Gsps ADCs challenging. Two of these important limitations are V_{dd} scaling and f_T saturation, which were briefly discussed in Chapter 1.

However, recent advancements in multi-Gsps ADCs implemented in sub-65-nm CMOS technologies have achieved impressive SNDRs greater than 50 dB [92]-[96]. These developments hold great promise for 5G FR1applications.

By employing these high-speed wideband ADCs, it becomes feasible to construct a direct RF-sampling receiver as illustrated in Figure 2.17. In this structure, the input RF signal is amplified by an LNA, and all bands of interest are concurrently processed through parallel branches of filters and PGAs. The filters effectively

reject OOB blockers and noise, while the PGAs equalize the amplitude of the aggregated carriers. Finally, the entire band is digitized at once by an ADC. Subsequent processes, including down-conversion, demodulation, and channel selection, are performed in the digital domain [97].

Indeed, this architecture has demonstrated the potential for low-power, low peak current, low-voltage, and compact implementations [88]. Direct RF-sampling receivers offer higher efficiency in terms of silicon area and energy consumption compared to their multi-path direct/double-conversion counterparts, especially for bandwidths greater than 20 MHz [98]. However, these advantages come at the expense of more challenging frequency planning and filtering in both mixed-signal and analog components to address aliasing and noise folding issues. Particularly in fully integrated receivers, careful gain/noise/power budgeting becomes essential. Investigating these challenges, we first provide an overview of two major sampling strategies: Nyquist-rate sampling and subsampling.

Nyquist-rate sampling

This sampling method, also known as low-pass sampling, involves capturing the entire spectrum of interest within the first Nyquist zone [48]. In other words, the sampling frequency is set to be greater than twice the upper boundary of the frequency range, i.e., $f_s > 2f_H$. For 5G FR1 receivers, a Nyquist-rate ADC with a minimum sampling rate of 14.25 GHz is required.

As depicted in Figure 2.18(a), the subsequent Nyquist zones are situated far away from the desired bands, allowing for the use of a low-pass AAF with relaxed requirements. Furthermore, in 5G FR1 applications, the blockers that may exist in the second Nyquist zone, ranging from 7.125 to 14.25 GHz, are typically sparse and weak. Consequently, aliasing is not a significant concern in this type of receiver.

While BPFs and parallel branches for multi-band reception are still required to attenuate blockers within the first Nyquist zone and reject between-band blockers, the rejection ratio requirements of these filters are comparable to those in multi-path homodyne receivers.

When the receiver shown in Figure 2.17 samples at the Nyquist rate to capture K bands simultaneously, the output noise spectral density (NSD) of the receiver within the n^{th} band ($1<n<K$) can be derived from [99]:

$$S_{N_n,nyq} = \frac{1}{f_{s,nyq}} \sum_{k=1}^{K} P_k G_{p_k} \left(\frac{2z^2}{3L_q^2} + \left(2\pi f_k \sigma_j\right)^2 \right) + k_B T G_{p_n} F_n \qquad (2.24)$$

where $f_{s,nyq}$ represents the sampling frequency, P_k and G_{pk} denote the average signal power and power gain within the k^{th} band, z accounts for clipping error, L_q stands for the number of quantization levels, σ_j represents the standard deviation of jitter, and G_{pn} and F_n denote the power gain and noise factor of the RFFE within the

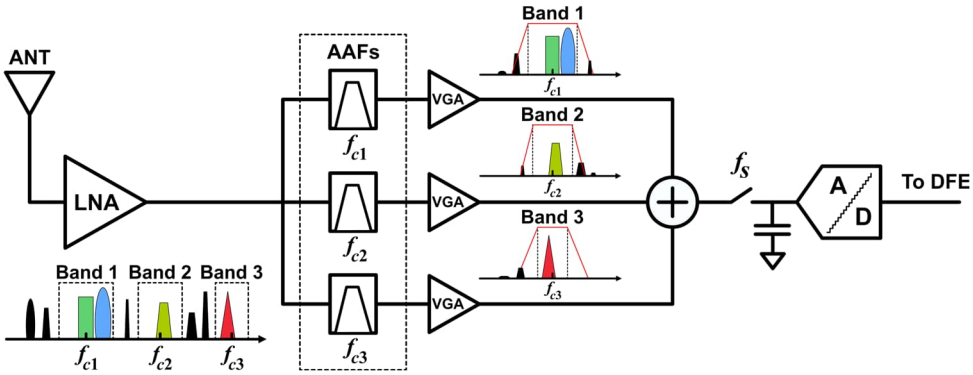

Figure 2.17: Architecture of a direct RF-sampling receiver.

n^{th}-band. In other words, the first term accounts for ADC noise and the second term represents the RFFE noise contribution.

To achieve lower NF, the following strategies can be considered:

1. **Increasing $f_{s,nyq}$:** This involves obtaining a larger oversampling rate, as discussed in the previous section. However, it comes with the cost of additional power consumption in the PLLs, clock dividers, and buffers. Each doubling of the sampling rate poses a 16-fold increase in the VCO's power for the same σ_j [100].
2. **Lowering G_{pk}:** This requires high-Q, high-order BPFs in concurrent branches, which can result in higher power consumption and linearity issues.
3. **Reducing jitter:** This can also be challenging due to the trade-off between jitter and PLL's power consumption. When the PLL's reference induces phase noise, the VCO's power consumption is a function of σ_j^{-4} [100].
4. **Increasing RFFE's in-band gain:** Although this gain (G_{pn}) is set to its maximum in high-sensitivity mode, the gain compression of the RFFE and the DR of the ADC impose an upper bound for it.

In addition to the stringent jitter requirements and complex clocking schemes in Nyquist-rate TI-ADCs, the gain, timing, and transfer function mismatches among sub-ADCs degrade the SFDR. Additional digital correction and extensive calibration are required to reduce the in-band spurs generated by aliasing [101].

As an example of wideband Nyquist-rate ADCs, a 24 GS/s TI-ADC in [92], consisting of 80 sub-ADCs, achieves 46 dB SNDR up to 7.2 GHz. Although implementing such a complex design in a cutting-edge 7-nm technology resulted in only 0.9 mm^2 die area, it consumes 750 mW, with more than 50% contributed by clock dividers, buffers, samplers, and calibration circuits. Jitter causes 47.5% of the noise in this data converter.

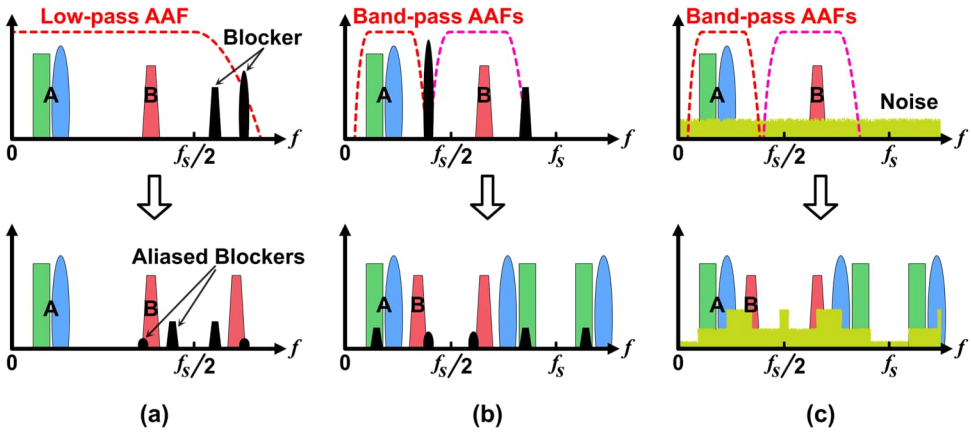

Figure 2.18: Illustration of:
(a) Aliasing in low-pass sampling. (b) Aliasing in band-pass sampling. (c) Noise folding.

Subsampling

Subsampling, also referred to as band-pass sampling, offers a solution to relax the phase noise requirement of TI-ADCs and enables the implementation of low-power designs by digitizing the entire band at a sampling frequency less than the Nyquist rate, i.e., $f_{s,sub} < 2f_H$ [102, 103]. According to the sampling theory, as long as $f_{s,sub}$ is greater than twice the bandwidth of each desired signal, aliasing can be avoided, and the sampled signals can be successfully reconstructed [48].

In a subsampling receiver, the inherent frequency translation feature of the sampling process is utilized, where the sampled signals around the harmonics of $f_{s,sub}$ are down-converted to the first Nyquist zone. For example, if a signal in n77 band with a bandwidth of 100 MHz and a center frequency of 3.7 GHz is sampled by $f_{s,sub}$ = 400 MHz, its down-converted copy falls between 50 and 150 MHz.

However, if the desired signal is located at 3.8 GHz, the low-frequency copy of the signal falls between two Nyquist zones, resulting in aliasing. Therefore, this sampling method requires careful frequency planning. For applications covering a wide range of channel bandwidths and center frequencies (f_c), the sampling frequency needs to be adjustable to ensure that the desired signals fall within only one Nyquist zone. A reasonable strategy is to set the center of down-converted signals to $f_{s,sub}/4$. To achieve this, the sampling frequency must be calculated as [103]:

$$f_{s,sub} = \frac{4f_c}{2l-1} \tag{2.25}$$

where l = 1, 2, 3, …, $\lfloor f_c/BW + 0.5 \rfloor$. The value of l is optimized by considering oversampling gain, aliasing, and noise folding [103]. In the previous example, $f_{s,sub}$ could be 202.6, 608, or 800 MHz for l = 38, 13, and 10, respectively.

Figure 2.18(b) illustrates the effect of aliasing in an inter-band CA scenario. In the presence of strong blockers between the desired bands, sharp roll-off AAFs are required. Otherwise, the aliased versions of these blockers or other concurrent signals in other bands become in-band distortion for the desired channel.

Another challenge of subsampling, known as noise folding, is shown in Figure 2.18(c). It occurs when the input noise spectrum density within higher Nyquist zones is translated to the fundamental zone, raising the in-band noise floor, and degrading the SNDR [88]. In a direct sampling receiver, this input noise refers to the output noise spectrum of the RFFE. Therefore, considering the folding effect, the contribution of the RFFE's noise in the output NSD of the receiver can be written as [99]:

$$S_{N_n,RFFE} = k_B T \left(G_{p_n} F_n + m_{sub} \left(\frac{G_{p_n}}{A_{R_n}} F_{LNA} + G_{p,PGA}(F_{PGA} - 1) \right) \right) \quad (2.26)$$

where, m_{sub} represents the number of times noise folding occurs and can be calculated from $\lfloor 2\, f_H / f_{s,sub} \rfloor$ [99]. A_{Rn} denotes the AAF's OOB rejection ratio and $G_{p,PGA}$ stands for the PGA's power gain. Also, F_{LNA} and F_{PGA} are the noise factors of the LNA and PGA, respectively.

By incorporating the noise contribution of the sampler and quantizer into Equation 2.26, the total output NSD of the receiver can be expressed as [99]:

$$S_{N_{n,sub}} = \frac{1}{f_{s,sub}} \sum_{k=1}^{K} P_k G_{p_k} \left(\frac{2z^2}{3L_q^2} + \left(2\pi f_k \sigma_j\right)^2 \right) + S_{N_n,RFFE} \quad (2.27)$$

From this equation, we can highlight the practical challenges in the implementation of subsampling receivers in comparison to Nyquist-rate sampling receivers:

1. **Higher sensitivity to blockers and OOB signals:** Since $f_{s,sub}$ is often significantly lower than $f_{s,nyq}$, the presence of blockers and OOB signals in multi-band receivers and CA scenarios has a considerably stronger deteriorating effect on the SNDR. In other words, reducing the sampling rate sacrifices the oversampling gain to relax the jitter requirements [99].
2. **High-Q, high-order AAF:** In contrast to Nyquist-rate sampling receivers, subsampling receivers require BPFs with quality factors larger than 100 to effectively reject OOB blockers and to reduce the OOB noise power before folding [88]. Within NR FR1, achieving quality factors greater than 20 is

challenging in CMOS processes due to losses in the metal layers and substrate. Therefore, low-power and low-noise filtering solutions need to be investigated.

3. **Sufficiently large gain before PGA:** Since the PGA's noise is not rejected by AAF, it goes through the folding process. To mitigate the contribution of this noise to the receiver's NF, it is crucial to allocate enough gain to the LNA+AAF during gain budgeting across the receiver chain.

RFFE Gain

Following the third point above, it is worth noting the upper and lower limits of the RFFE's gain in direct sampling receivers. Referring back to Figure 2.10, in the high-sensitivity mode, the power gain ($G_{p,RFFE,HS}$) must be large enough to amplify low-power signals to a level sufficiently higher than the ADC's noise floor. Mathematically, it means [48]:

$$G_{p,RFFE,HS} \geq \frac{F_{ADC} - 1}{F_{RX,max} - F_{RFFE}} \tag{2.28}$$

where $F_{RX,max}$ denotes the maximum acceptable noise factor of the receiver, while F_{RFFE} and F_{ADC} represent the noise factor of the RFFE and ADC, respectively.

On the other hand, in the high-tolerance mode, the voltage gain must be set to a lower level to ensure that the ADC's input does not exceed the clipping-free range. The loading factor (LF) is the parameter used to express the difference between the full-scale voltage of the ADC and its input level. This parameter is optimized for the best noise performance, and its optimal value (LF_{opt}) depends on the ADC's resolution, defining the operating range of the ADC's input. Therefore, the upper bound of the RFFE's voltage gain ($G_{v,RFFE,HT}$) can be expressed as [48]:

$$G_{v,RFFE,HT} \leq \left(FS_{ADC}[\text{dBmV}] - LF_{opt}[\text{dB}]\right) - RF_{in,max}[\text{dBmV}] \tag{2.29}$$

To determine the required range of gain adjustability in a direct RF-sampling receiver for 5G FR1 applications, we can utilize Equation 2.28 and Equation 2.29 by substituting the values from Table 2.3 and Table 2.5. The results are presented in Table 2.7. In this analysis, we consider an ADC with a SNDR of 50 dB and an LF_{opt} of 15 dB. According to Table 2.7, it is evident that a minimum gain adjustability of 24 dB must be engineered into the RFFE chain, particularly for subsampling receivers.

Figure 2.19 shows the effect of the AAF's rejection ratio on the jitter requirements in a Nyquist-rate sampling receiver for a 3CC inter-band CA scenario. In the case of 20 dB OOB rejection, the PLL must generate a σ_j below 70 fs to achieve a NF lower than 5.5 dB. However, if the rejection is improved to 26 dB, the jitter requirement becomes five times more relaxed. This effect is even more pronounced

Table 2.7: Required gain adjustability of a direct RF-sampling receiver in 5G FR1 applications.

Type of NR Receiver	NF_{RX}[1] (dB)	NF_{RFFE} (dB)	$G_{p,RFFE,HS}$ (dB)		$G_{v,RFFE,HT}$ (dB)
			f_s = 800 MHz	f_s = 14.25 GHz	
Wide-area BS	3.5	3	44.2	31.7	28
Medium-range BS	5.5	4	37.9	25.4	23
Local-area BS	7.5	4.5	33.6	21	20
UE	8	5	33	20.5	29

[1] Margins for implementation loss, mismatch, and nonlinear effects are considered in these target values.

in subsampling receivers. For instance, with a sampling frequency of 800 MHz using the same setup, an AAF with OOB rejection better than 32 dB is required.

Considering the frequency spacing between the desired aggregated bands and potential blockers, as presented in Table 2.5, it becomes clear that high-order BPFs with highly tunable quality factors and center frequencies are essential. Depending on the operational mode and CA configuration, these filters might need to be programmed in wideband mode with a relatively low rejection ratio or narrowband mode with rejection ratios as high as 40 dB.

In conclusion, it is important to highlight one of the significant advantages of direct RF-sampling receivers which enables spectrum-aware cognitive radios in telecommunication networks, as conceptualized by Mitola over two decades ago [32]. A direct RF-sampling receiver allows for the observation of the entire spectrum, facilitating the identification of free spots, crowded bands, and the location of strong blockers. This spectrum sensing capability can be adjusted with programmable sensitivity based on the activated resolution of the converter. In comparison to other methods that require the implementation of on-chip spectrum analyzers through filter banks alongside main homodyne chains [104], direct sampling architecture does not add extra power consumption and chip area. Leveraging feature extraction and compressive sensing [105] is considerably more straightforward in direct sampling architectures, leading to faster frequency sensing, thereby making it suitable for low-latency use-cases.

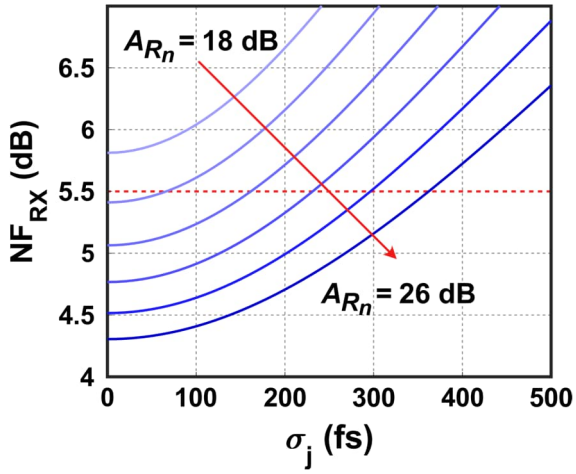

Figure 2.19: Impact of the AAF rejection ratio on jitter requirements in a Nyquist-rate sampling receiver.

2.5 Thesis Contribution

This thesis explores the significance of implementing highly reconfigurable receivers to support challenging CA scenarios and to enable spectrum-aware radios in 5G FR1 applications. It specifically focuses on direct sampling receivers and emphasizes multiple-mode, digitally assisted RFFEs for such receiver chains. The research investigates various circuit techniques for designing low-power broadband LNAs and highly adjustable RF BPFs in cutting-edge CMOS processes.

Through the dissemination of published papers, this thesis presents achievements in several aspects of the proposed RFFE, including their integration and calibration methods to mitigate uncertainties and enhance the overall performance.

Chapter 3

Broadband Low-Noise Amplifiers

In the realm of circuitry, the persistent presence of thermal noise is inevitable as long as circuits are constructed with conductors, a concept aptly elucidated by J. B. Johnson nearly a century ago: “statistical fluctuation of electric charge resulting in the thermal agitation of electricity” [106]. This notion not only sets the stage for our understanding of noise but also finds a poignant echo in the words of Arthur Schopenhauer, who eloquently captured the intrusive nature of noise: "Noise is the most impertinent of all forms of interruption. It is not only an interruption, but also a disruption of thought" [107]. In our context, this interpretation extends seamlessly to data communication and processing.

The LNA commonly serves as the initial stage within receiver front-ends, playing a pivotal role in amplifying the signal to elevate it sufficiently above the noise floor. From an alternative perspective, the LNA mitigates the noise contribution that subsequent stages may introduce. In addition to this fundamental role, the LNA also fulfills input matching conditions and, in certain scenarios, facilitates the conversion of an unbalanced input from the antenna into a balanced, differential output.

In this section, we will commence with introducing the performance metrics pertinent to wideband LNAs. Following this, we will explore a variety of circuit techniques employed to not only enhance the LNA's noise performance, operating bandwidth, and linearity, but also aim to effectively tackle the growing demand for energy-efficient, low-power, and low-voltage solutions.

3.1 LNA Performance Metrics

The evaluation of LNAs necessitates the consideration of several metrics that collectively gauge the merit of a design from various aspects including noise, bandwidth, gain, linearity, power consumption, and compactness.

Input impedance matching

Figure 3.1(a) depicts the 2-port model of an LNA. The analysis of this network's behavior can be conducted by employing scattering parameters (S-parameters). These parameters quantify the reflected waves from input and output ports ($V_{1,2}^{-}$) in relation to the incident waves ($V_{1,2}^{+}$). Mathematically, these parameters establish a linear relationship between the phasors of these waves, which can be expressed as:

$$\begin{pmatrix} V_1^- \\ V_2^- \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} V_1^+ \\ V_2^+ \end{pmatrix} \tag{3.1}$$

The input reflection coefficient (Γ_{in}) serves as an indicator of impedance matching at the input port, defined as [108]:

$$\Gamma_{in} = \frac{V_1^-}{V_1^+} = \frac{Z_{in} - Z_s}{Z_{in} + Z_s} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{3.2}$$

where Z_{in} and Z_s represent the input impedance of the LNA and the source impedance, respectively, while Γ_L denotes the output reflection coefficient (i.e., where the LNA is loaded).

In a unilateral network, where input is completely isolated from the output (S_{12}=0), Γ_{in} is equal to S_{11}. Thus, it is common to report S_{11} as a measure of impedance matching and reflection.

In the case of an ideally matched network, where Z_{in} equals Z_s, the reflection coefficient becomes zero. However, for practical implementations a threshold is considered for the maximum acceptable magnitude of S_{11} in dB. A widely accepted value within the literature and among the community is -10 dB.

Power and voltage gain

The power gain (G_p) is defined as the ratio of the average power delivered to the load to the average power received from the source, and can be derived from [108]:

$$G_p = \frac{|S_{21}|^2(1 - |\Gamma_L|^2)}{|1 - S_{22}\Gamma_L|^2(1 - |\Gamma_{in}|^2)} \tag{3.3}$$

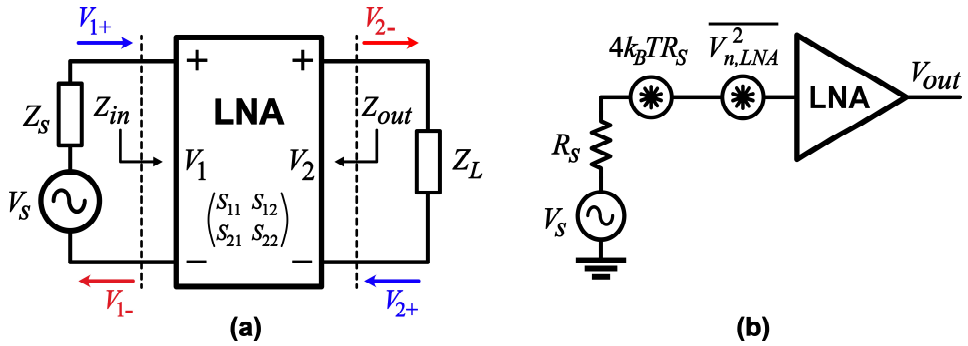

Figure 3.1: (a) Two-port model of an LNA. (b) Input-referred noise.

In the case where both input and output ports are ideally matched, meaning Γ_{in} and Γ_L are both zero, the power gain is reduced to $|S_{21}|^2$.

The voltage gain (G_v) is defined as the ratio of the output voltage amplitude to the input voltage amplitude. This gain can be related to the power gain as follows:

$$G_v = \sqrt{\frac{Re\{Y_{in}\}}{Re\{Y_{out}\}} G_p} \tag{3.4}$$

While in discrete implementation of receiver chains, the input and output impedances of circuit blocks are typically matched to the same characteristic impedance (e.g., 50 Ω system), resulting in the equality of voltage gain and power gain in the dB-scale, in integrated receiver chains, the output impedance may be optimized to a value different from the input impedance.

Noise Figure

The average power of noise at the output of an LNA is commonly referred to the input by being divided to the power gain. This concept is depicted in Figure 3.1(b), where a voltage source ($V_{n,LNA}$) represents this noise.

The noise factor (F_{LNA}) is defined as the ratio of the input SNR to the output SNR. Mathematically, it can be formulated as [68]:

$$F_{LNA} = \frac{1}{4k_B T R_s} \cdot \frac{\overline{V_{n,out}^2}}{G_p} = 1 + \frac{\overline{V_{n,LNA}^2}}{4k_B T R_s} \tag{3.5}$$

where, R_S denotes the real part of the source impedance, and $\overline{V_{n,out}^2}$ stands for the total average power of the output noise. Consequently, the noise figure is given by:

$$NF_{LNA} = 10 \log_{10} F_{LNA} \tag{3.6}$$

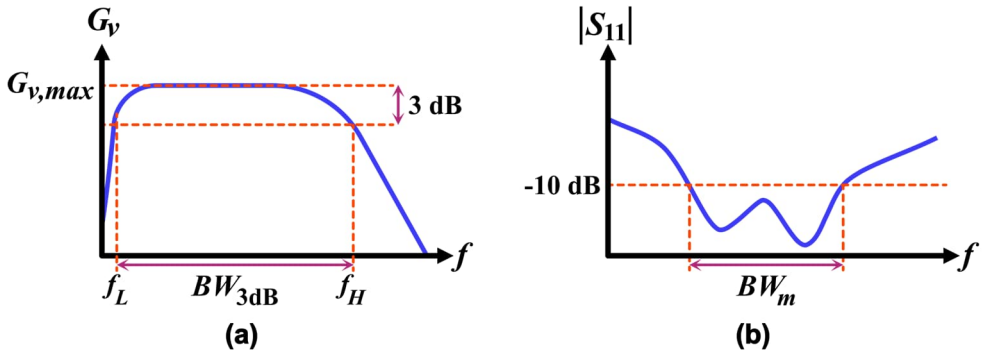

Figure 3.2: Definitions of (a) 3-dB gain bandwidth, and (b) -10-dB matching bandwidth.

Bandwidth

The previously mentioned LNA characteristics often exhibit frequency dependence. This phenomenon is visualized in Figure 3.2(a), where LNAs typically exhibit a bandpass voltage gain that remains relatively constant within a specific frequency span. An often-used criterion for delineating the gain bandwidth (BW_{3dB}) of amplifiers is a 3-dB reduction in gain.

A parallel frequency dependency applies to impedance matching. As demonstrated in Figure 3.2(b), the frequency profile of $|S_{11}|$ is commonly characterized by a number of dips. The matching condition, signified by $|S_{11}| < -10$ dB, can be met within a finite frequency range known as the matching bandwidth (BW_m).

The value of NF_{LNA} commonly reaches its minimum ($NF_{LNA,min}$) within the band of interest. As the gain decreases, NF_{LNA} tends to rise for the frequencies that fall outside the operational range. Consequently, a noise bandwidth can be established based on the maximum acceptable NF_{LNA} values.

In the design of an LNA, it is imperative to ensure that all three bandwidths, mentioned above, extend beyond the frequency range for which the LNA is intended to be employed.

Stability

Oscillations and unintended resonances, caused either by intended feedback loops or by parasitic couplings, can lead to spurious tones at the output. These internal oscillations have the potential to saturate the amplifier, constrain its in-band gain, and elevate the noise figure.

Amplifiers often need to be unconditionally stable, implying stability regardless of the connected load and source impedances. Conversely, amplifiers can also exhibit conditional stability, being subject to instability for specific combinations of load and source impedances. In the design of integrated LNAs, the pursuit of unconditional stability is often favored due to process uncertainties.

To assess amplifier stability, Rollet's stability factor (K-factor) proves useful, as formulated in [109]:

$$\mathrm{K} = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{3.7}$$

where

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{3.8}$$

A K-factor value greater than one ensures unconditional stability of the amplifier. However, it's important to note that a higher K-factor is associated with a lower gain level. Consequently, during the process of optimizing gain and noise performance, the objective is often to target a K-factor slightly above one.

It is important to highlight that the S-parameters employed in the above equations are dependent on the signal power level. Thus, it is essential to verify the LNA's stability across all input power levels required for an application.

Linearity

As discussed in Section 2.3.2, in the presence of strong interferers the LNA suffers from gain compression which subsequently increases the noise figure. Therefore, the noise figure with respect to variations in blocker power is assessed to determine the blocker noise figure. The LNA's blocker tolerance can be measured by identifying the level of blocker power at which NF rises by 1 dB.

Furthermore, the parameters IIP2, IIP3, and P_{1dB} hold great significance for LNAs, particularly in RFFEs deployed in direct RF-sampling receivers. This importance arises from the fact that in such systems, the LNA precedes the filter, allowing interfering signals to pass through the LNA without any attenuation.

Cost

Additional factors that play a pivotal role in determining the quality and implementation cost of an LNA encompass power consumption, supply voltage, die area, and the quantity of necessary on-chip inductors and off-chip components.

Expanding upon the latter consideration, on-chip inductors are susceptible to undesired couplings, pulling effects, and power loss. This often necessitates the allocation of significant vacant spaces surrounding these inductors to mitigate these drawbacks.

Likewise, off-chip components like discrete baluns and splitters introduce various challenges. These include insertion loss, imperfections in matching, and delays in interconnections between the integrated circuit and the PCB.

Wideband LNA's FoMs

In order to facilitate a comprehensive and quantitative comparison among LNAs, several FoMs have been defined in the literature. When evaluating wideband LNAs, it becomes essential to incorporate the bandwidth into these FoMs.

The following FoM includes power gain, bandwidth, noise factor, and power consumption [110]:

$$\mathrm{FoM}_1 = \frac{G_{p,av}[\mathrm{abs}] \times BW_{3\mathrm{dB}}[\mathrm{GHz}]}{(F_{LNA} - 1) \times P_{DC}[\mathrm{mW}]} \tag{3.9}$$

To account for linearity, the subsequent FoM is formulated by multiplying FOM_1 by IIP3 [110]:

$$\mathrm{FoM}_2 = \mathrm{FOM}_1 \times IIP3[\mathrm{mW}] \tag{3.10}$$

Finally, to highlight the merit of compact designs, we can normalize FoM_2 by die area [111]:

$$\mathrm{FoM}_3 = \frac{\mathrm{FoM}_2}{Area[\mathrm{mm}^2]} \tag{3.11}$$

These FoMs might be calculated in either linear or dB scale.

3.2 Bandwidth Extension

In this section, we present an overview of several circuit techniques proposed to enhance the bandwidth of LNAs. Additionally, we provide a succinct discussion of their advantages and disadvantages.

Wideband matching networks

A matching network is placed between the source and the LNA or between the LNA and its load, providing impedance conversion in a manner that the matching condition is satisfied within the desired frequency range.

While a single resonant circuit, as depicted in Figure 3.3(a), proves suitable for narrowband matching with low insertion loss, for broadband LNAs covering the entire upper mid-band, multi-resonant matching networks are required [112]. A case in point is the inductive T-network illustrated in Figure 3.3(b) [113]. In this circuit, C_p accounts for the parasitic capacitance arising from interconnects between the matching network and the antenna, along with the parasitic capacitance of the pad. Also, C_{in} stands for the total parasitic capacitance at the input node of the LNA.

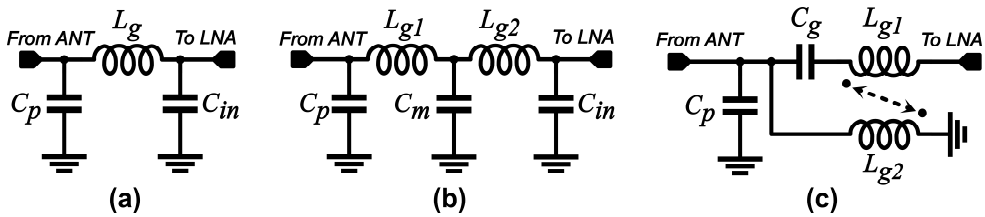

Figure 3.3: Impedance matching networks:
(a) L-network. (b) T-network. (c) Transformer-based.

At low frequencies the input impedance seen by the source equals $R_{in,LNA}$, which can be tailored to match R_S. As frequency increases, the effect of C_p and C_{in} becomes more pronounced, necessitating the utilization of inductors for compensation. It can be shown that when L_{g1} equals L_{g2}, optimal matching is achievable at:

$$\omega_0 \approx \frac{1}{\sqrt{\frac{L_g}{2} C_m}} \tag{3.12}$$

By adjusting the values of $L_{g1,2}$ and C_m, the matching condition can be met across a broad frequency spectrum beyond ω_0. Alternatively, for the creation of a dual-resonant network, a pair of mutually coupled inductors can be employed [114, 115], as shown in Figure 3.3(c).

The matching bandwidth of these networks has an inverse relationship with their quality factor (Q_m), which can be expressed as:

$$BW_m \approx \frac{\omega_0}{Q_m} \tag{3.13}$$

Consequently, an approach to achieving wideband operation involves reducing the quality factor, a technique commonly referred to as de-Qing [116]. However, this method introduces higher insertion loss, thereby degrading the maximum available gain and increasing the NF.

Inductive peaking

To compensate the effect of parasitic capacitors at higher frequencies, inductors can be used in either series or shunt configurations. This technique, known as inductive peaking, produces a smoother decrease in gain and raises the 3-dB cut-off frequency [117]. In Figure 3.4, three inductive peaking structures are presented. While the topologies shown in Figures 3.4(a, b) increase the high-frequency load impedance to maintain the gain [117, 118], the design in Figure 3.4(c) employs L_D to compensate the effect of the parasitic capacitances (C_{gs}, C_{sb}, and C_{ds}) at the cascode node [119, 120].

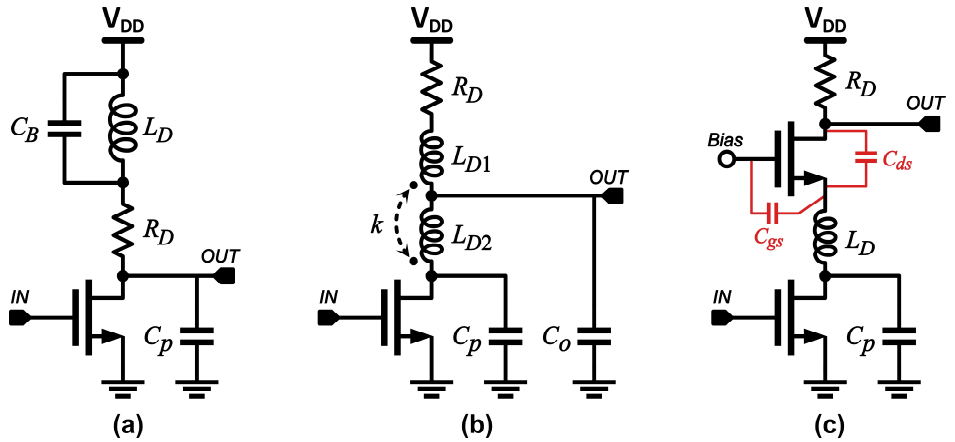

Figure 3.4: Inductive peaking structures:
(a) Bridged shunt. (b) Asymmetric T-coil. (c) Cascode compensation.

Despite its effectiveness, this approach introduces additional noise due to the limited Q-factor of on-chip inductors. Additionally, the presence of other inductors on the same chip can lead to undesired couplings and feedback loops, potentially injecting noise or causing stability issues. Moreover, the utilization of inductors invariably results in higher implementation costs and larger die area.

In advanced FD-SOI technologies like 22FDX, the depletion region underneath the source and drain is confined to the BOX layer. Therefore, the impact of C_{sb} and C_{ds} is negligible, except for mm-wave and sub-THz applications. Moreover, the value of C_{gs} in such technologies is notably smaller compared to earlier generations of bulk CMOS technologies. As a result, it becomes feasible to design adequately wideband LNAs without relying on inductive peaking techniques.

Feedback LNAs

Applying negative feedback to an amplifier enhances bandwidth by a multiplication factor of the loop gain, while the gain-bandwidth product remains constant. One of the fundamental feedback structures employed with the common-source (CS) amplifier for input impedance matching is inductive degeneration of the source [119]. Nevertheless, in this configuration, the gate resistance can result in poor noise figure, especially at higher frequencies [121].

An inductorless alternative, illustrated in Figure 3.5(a), is resistive-shunt feedback, which offers wideband input matching [122, 123]. However, achieving high gain and satisfactory NF with this topology necessitates enhancing the g_m of the CS, which requires additional power consumption or the use of larger devices, thereby increasing the parasitic capacitances and limiting the bandwidth extension.

Instead of resistive feedback, capacitive [121]-[123] and transformer-based shunt feedback [115, 126] can be employed, as seen in Figure 3.5(b) and Figure 3.5(c),

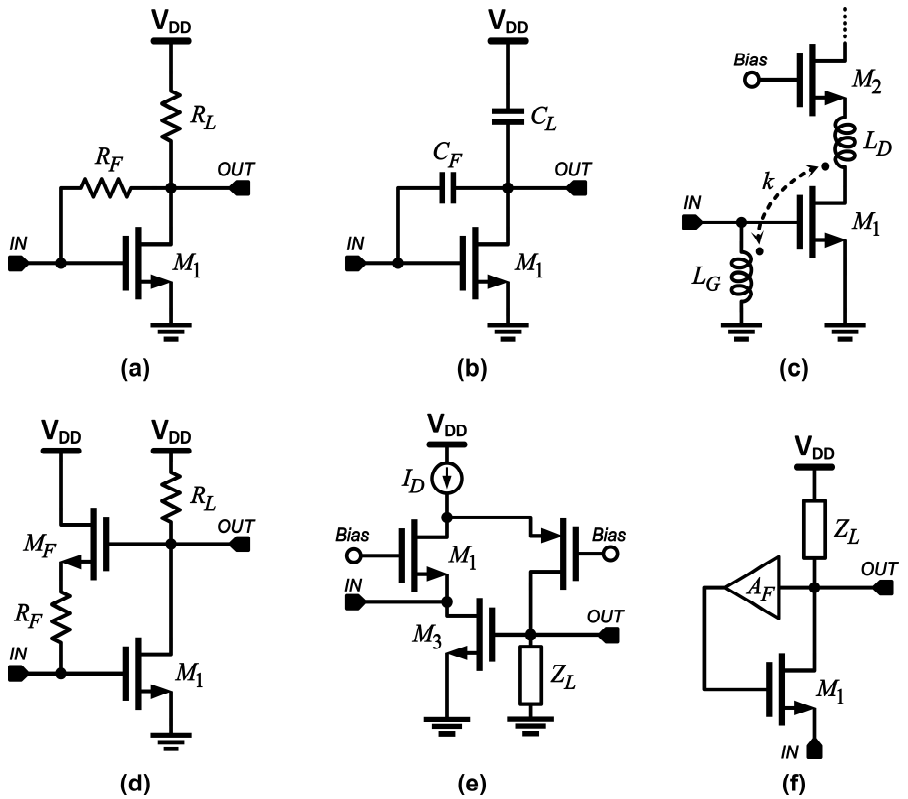

Figure 3.5: Feedback structures: (a) Resistive. (b) Capacitive. (c) Transformer-based. (d) Active-shunt CS. (e) Active-shunt CG. (f) Series CG.

respectively. Capacitive feedback offers the advantage of low excess noise due to the feedback network and the potential to use switched-capacitor circuits for reconfigurable designs [125].

An alternative approach to overcoming the gain-bandwidth trade-off in resistive shunt feedback LNAs is the use of a voltage follower between the shunt resistor (R_F) and the input node [127]-[129]. This active-shunt feedback, depicted in Figure 3.5(d), achieves a high output impedance while fulfilling the input matching criterion with R_F. However, this structure is susceptible to linearity issues.

In Figure 3.5(e), an active-shunt feedback structure is presented for the common-gate (CG) amplifier stage [130]. Since the output transconductance of the feedback device (M_3) (g_{ds3}) is in parallel with g_{m1}, variations in this parameter with signal power levels can lead to distortion, limiting the dynamic range of the LNA. Therefore, efficient methods for adjusting g_{ds} are essential to address these linearity concerns [131]. Figure 3.6(f) underscores another way of using feedback networks, in which a multi-resonant load impedance is reflected to the input in order to facilitate band-selective matching [131].

It is important to highlight that in state-of-the-art designs, multiple local and global feedback loops have been incorporated to enhance loop gain or to enable multi-fold noise/distortion cancellation [124, 126, 127, 130].

Reconfigurable multi-band LNAs

Multi-band LNAs are designed for use-cases where a predetermined set of frequency bands with fixed center frequencies are of interest. In these applications, switchable circuit elements can be integrated into the LNA's structure, allowing for optimization of the overall performance across specific operational power levels and frequencies. Moreover, such LNAs possess the capability to transition between narrowband and wideband modes, thereby adapting to a diverse range of telecommunication standards [120].

The reconfigurability can be realized through adjustments to the feedback network [129], the input matching network [120], or the load impedance [120, 132]. The adaptable circuit element may be a biasing current, a variable resistor, an active or switchable inductor, or a capacitor bank. However, it is worth noting that these types of LNAs are unsuitable for capturing a broad frequency spectrum encompassing sparse bands of interest, including various carrier aggregation scenarios discussed in Chapter 2.

3.3 Noise Cancellation

Achieving NFs lower than 3 dB while maintaining matching and stability conditions in LNAs with global feedback poses a formidable challenge. Furthermore, the pursuit of reducing noise power generated by active devices often entails an increase in power consumption and transistor dimensions, leading to constraints on bandwidth and exacerbating self-heating effects. Consequently, the concept of noise cancellation has been employed in various configurations to partially reject the noise contribution of a component that significantly affects NF.

The principle of noise cancellation is demonstrated in Figure 3.6, where two paths exist for signal and noise to reach the amplifier's output. The main path involves the amplifier stage A_1 and the auxiliary path consists of A_2. The aim here is to cancel the noise (V_{n1}) generated by A_1. The circuit is designed in a way that A_2 produces a negative copy of this noise, ideally with the same power level. By combining these positive and negative versions of the noise, the output is effectively cleansed of noise while the circuit retains amplification for the signal [133].

However, practical implementations of this technique entail two main limitations. First, the mismatch between the noise transfer functions of the main and auxiliary paths results in imperfect noise cancellation, especially at higher frequencies, leaving behind residual noise. Second, noise generated by the auxiliary path

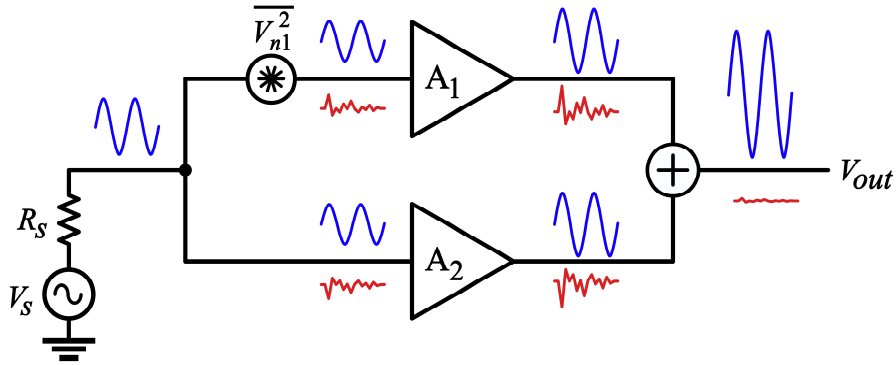

Figure 3.6: The concept of noise cancellation.

contributes to the total noise, impeding significant improvements in NF through this approach.

Since the emergence of this method, numerous circuit topologies have been proposed to improve the NF while mitigating the adverse effects of the auxiliary path on noise, power, and bandwidth.

While the resistive-shunt feedback LNA, in Figure 3.5(a), achieves noise cancellation under specific relationship among R_s, R_F, and g_m, practical trade-offs between bandwidth, matching, gain, and power consumption hinder the use of this noise-cancelling structure in wideband and high-gain applications [133].

Another fundamental noise-cancelling structure is CG-CS LNA. As depicted in Figure 3.7(a), noise from the CG device is cancelled out by the CS branch at the differential output [134]. However, to reduce the noise contribution of the CS stage, the biasing current of CS is chosen N times higher than that of the CG transistor. To maintain equal gain on both branches, the CS's load is decreased by a factor of N. Despite its potential use as an active balun, this topology exhibits poor IIP2, power supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR) due to unbalanced differential loads. Addressing this concern, a modified structure illustrated in Figure 3.7(b) employs a current-bleeding cascode device to achieve output balance while biasing the CS transistor with a sufficiently large current ($N.I_B$) [135]. Nonetheless, the noise contribution of the CS branch still necessitates high current consumption, rendering this structure unsuitable for low-power designs. Additionally, mismatches between the parasitic capacitances at the cascode nodes introduce a level of imbalance as the frequency increases.

Figure 3.7(c) presents another topology evolved from the CG-CS structure, utilizing a transformer at the input of the CG-CS [136]. In this circuit, the CS still cancels the CG's noise, while the CG partially cancels the CS's noise. This technique results in lower power consumption in the CS branch. However, limitations inherent to the transformer's bandwidth, insertion loss, and the area it occupies, may render this solution ill-suited to wideband and compact designs.

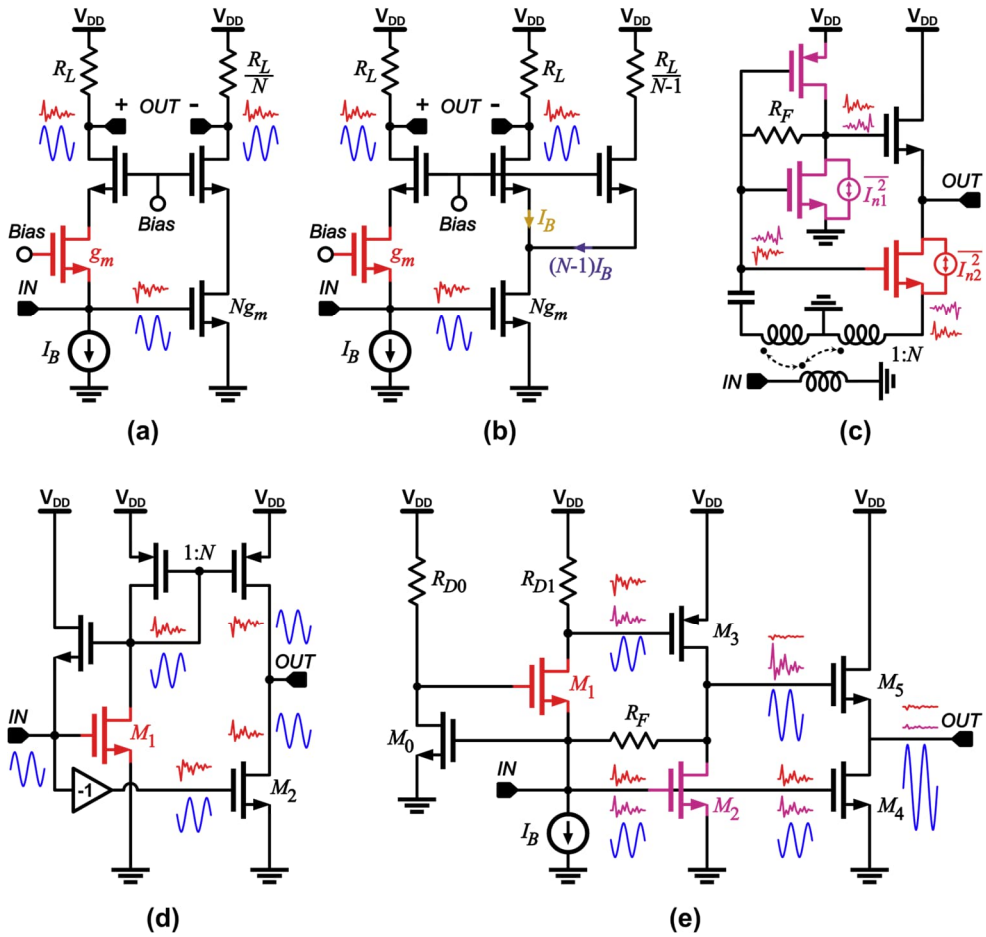

Figure 3.7: Noise-cancelling topologies: (a) Conventional CG-CS. (b) Current-bleeding CG-CS. (c) Transformer-based dual-path CG-CS. (d) CS-CS with CM combination. (e) Two-fold CG-CS.

The CS-CS LNA is another noise-cancelling alternative, in which both main and auxiliary paths consist of CS branches [127, 137, 138]. Figure 3.7(d) depicts an instance of such a circuit, where output combination is achieved through a current mirror [138]. In contrast to the CG-CS structure, the CS-CS LNA cannot function as an active balun unless an additional inverting amplifier is cascaded with one of the CS stages, potentially leading to phase/delay imbalances and additional noise.

Given the limitations of the aforementioned topologies, particularly for low-power and wideband LNAs, recent developments have introduced two-fold and concurrent noise-cancelling structures [110, 111]. In these circuits, the noise from multiple devices is cancelled simultaneously, and the residual noise from one cancellation stage undergoes subsequent cancellation processes to achieve

significant noise reduction. Figure 3.7(e) demonstrates an example of such implementations, where shunt feedback, g_m boosting, and CG-CS noise cancellation are synergistically combined [110]. The CG's noise is cancelled twice, and the CS's noise is partially cancelled at the output stage. Nonetheless, the differential implementation of this structure consumes 8 mW and requires a passive balun.

3.5 Power Efficiency Enhancement

While the desired gain, NF, and bandwidth determine the required transconductance (g_m) of LNAs, leveraging particular circuit techniques can help enhance g_m/I_d, resulting in an overall improvement in power efficiency. In the following, we shed light on two techniques that have been employed in the design of LNAs featured in this thesis: g_m boosting and current reuse.

g_m boosting

Figure 3.8(a) shows a g_m-boosted CG amplifier. The amplified version of the input voltage is applied via an inverting stage to the transistor's gate. Thus, at low frequencies, the effective g_m is given by:

$$g_{m1,boosted} = g_{m1}(A + 1) \tag{3.14}$$

Hence, assuming a consistent overdrive voltage, the biasing current can be reduced by a factor of A+1. However, as the frequency increases, the effect of parasitic capacitances becomes more pronounced. At the input, the gate-source capacitance (C_{gs1}) is magnified by the same factor as g_m. While maintaining the same overdrive voltage allows for a device that is (A+1) times smaller, it does not necessarily mean that C_{gs1} will be (A+1) times smaller. This is due to the fact that, compared to traditional bulk CMOS technologies, the contribution of overlap, fringe, and interconnect capacitances to the overall C_{gs1} of FD-SOI devices is more significant, and these parasitic capacitances are not scaled down linearly with transistor dimensions.

On the other side, the capacitance between gate and drain (C_{gd1}) adds a zero to the input-output transfer function, which can be expressed as:

$$z_1 = \frac{g_{m1}(A + 1) + g_{o1}}{A.C_{gd1}} \tag{3.15}$$

where g_{o1} is the output transconductance of M_1.

This additional zero could potentially raise stability concerns, particularly if a large boosting factor is used, while considering the limited operational bandwidth of the boosting amplifier.

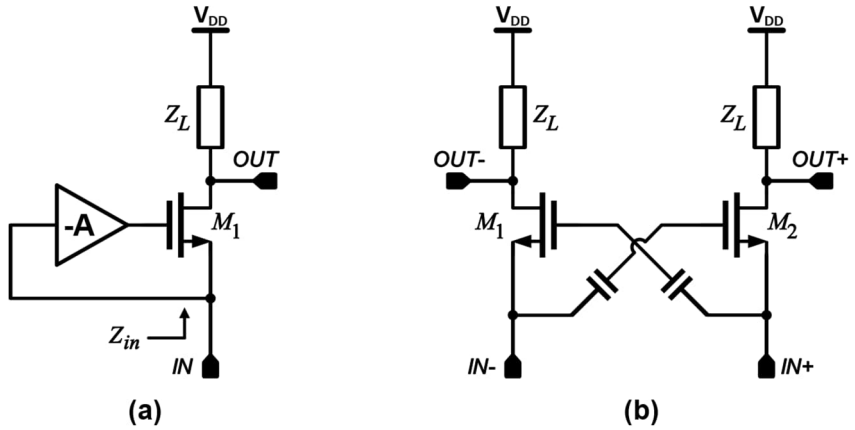

Figure 3.8: (a) g_m-boosting technique. (b) Capacitive cross-coupling topology.

Given these limitations, in RF implementations of g_m boosting, a relatively small value of A is often chosen, where single-stage amplifiers [111] or passive coupling [119, 128, 139, 140] is used. Figure 3.8(b) illustrates a simple but effective g_m boosting technique for high frequencies, employing a pair of relatively large AC-coupling capacitors. Beyond g_m boosting, this cross-coupling technique offers linearity advantages, which we will discuss further in Section 3.5.

Current reuse

Another approach for enhancing g_m/I_d is to use complementary stages. In theory, this nearly doubles g_m/I_d. However, replacing passive loads with active devices may restrict the linear range of the amplifier.

Complementary stages can be incorporated into amplifiers for various purposes. Figure 3.9 shows four fundamental topologies where current reuse is employed. Complementary CS and CG stages, illustrated in Figure 3.9(a) and Figure 3.9(b), are employed as main or auxiliary amplifier in noise/distortion cancelling LNAs. A push-pull current-reuse buffer, depicted in Figure 3.9(c), can serve as an output

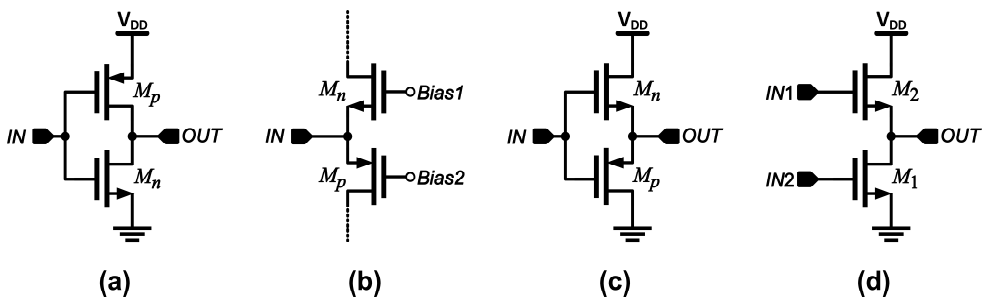

Figure 3.9: Current-reuse structures: (a) CS. (b) CG. (c) Push-pull buffer. (d) Combiner.

stage for isolation or measurement purposes. Lastly, Figure 3.9(d) demonstrates a current-reuse combiner that can be used in noise-cancelling LNAs or other blocks of the RFFE where signal subtraction or addition is required.

3.5 Linearization Techniques

Optimizing the operating points and biasing circuits, combined with meticulous gain budgeting of cascaded stages [141], is essential for realizing a highly linear RFFE. Additionally, several techniques have been proposed to construct low-power LNAs that exhibit high linearity and tolerance to blocking. Among these techniques, we emphasize derivative superposition and capacitive cross-coupling.

Derivative superposition

The drain current of a transistor is a nonlinear function of its gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}). The Taylor expansion of this function around a specific operating point (V_{GS0}, V_{DS0}) is given by:

$$I_D(V_{GS}, V_{DS0}) = I_{D0} + \sum_n \frac{1}{n!} \cdot \frac{\partial^n I_D(V_{DS0})}{\partial {V_{GS}}^n} (V_{GS} - V_{GS0})^n \tag{3.16}$$

The second and third order nonlinearities can be attributed to the following coefficients:

$$a_2 = \frac{1}{2} \cdot \frac{\partial^2 I_D}{\partial {V_{GS}}^2} = \frac{g'_m}{2}, \qquad a_3 = \frac{1}{6} \cdot \frac{\partial^3 I_D}{\partial {V_{GS}}^3} = \frac{g''_m}{6} \tag{3.17}$$

Derivative superposition is an approach through which the drain currents of K transistors are combined in a manner that ensures the algebraic summation of the derivatives of their g_m equals zero. Mathematically expressed, the output current of such an amplifier can be written as:

$$i_{out} = \left(\sum_{k=1}^{K} g_{m,k} \right) v_i + \frac{1}{2} \left(\sum_{k=1}^{K} g'_{m,k} \right) v_i^2 + \frac{1}{6} \left(\sum_{k=1}^{K} g''_{m,k} \right) v_i^3 + \cdots \tag{3.18}$$

which under the condition of zero composite derivatives, this expression can be simplified to a linear function:

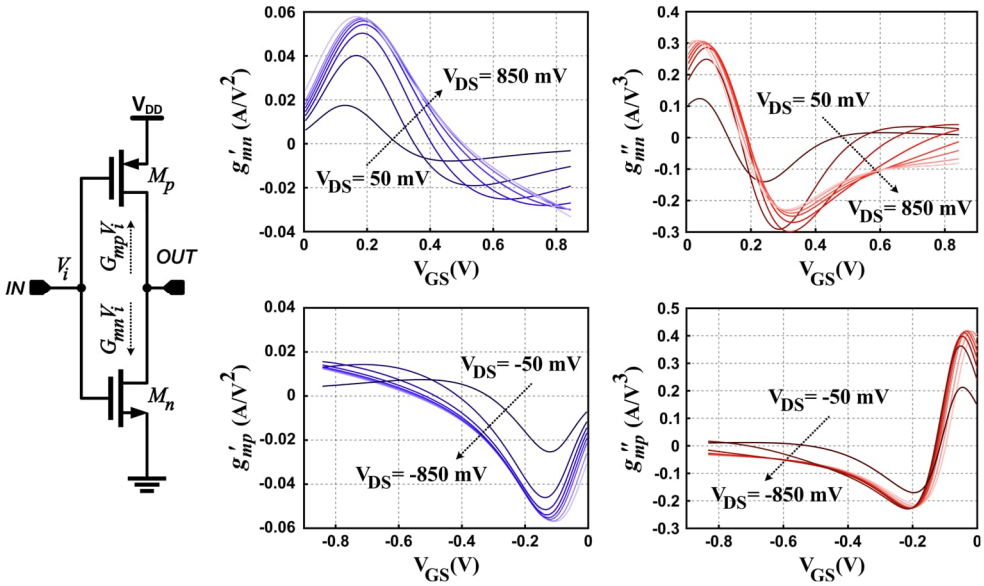

Figure 3.10: Complementary derivative superposition.

$$i_{out} = \left(\sum_{k=1}^{K} g_{m,k}\right) v_i \tag{3.19}$$

Figure 3.10 illustrates the variations of g'_m and g''_m of NFETs and PFETs in 22FDX process for a variety of operating points. In the conventional derivative superposition [142], two NFETs biased at different operating points are employed in parallel. In this configuration, one of the transistors needs to be biased in the weak/moderate inversion region to generate positive derivatives, while the other one is biased in the strong inversion region to yield negative derivatives, resulting in the cancellation of nonlinearities. However, this leads to an increase in the power consumption and exacerbates NF [142].

A complementary implementation of derivative superposition, as depicted in Figure 3.10, can effectively address these concerns [123, 129, 138, 143]. In this structure, both PFET and NFET devices can be biased in the same region, while producing derivatives with opposite signs.

Implementing this technique presents a challenge due to the narrow range of signal power that can be adequately linearized. In other words, achieving zero summation of derivatives is possible only at specific operating points. In the presence of large signals and strong blockers, the amplifier is pushed beyond this linearized region, resulting in only marginal improvement in linearity or even none at all. Various solutions have been proposed to tackle this challenge and thus extend

the linearized range. Among these, the utilization of body biasing and programmable multi-branch superposition have gained significant attention. In these techniques, the number of zero summation points is increased by activating more branches and simultaneously shifting the transconductance profile via body biasing, depending on the power level of the input signal [143].

Another limitation of this technique is that the Taylor expansion presented in Equation 3.18 holds true only at low frequencies. As discussed in Chapter 2, in general, the expansion coefficients, and therefore the nonlinearities, are frequency dependent. Consequently, instead of algebraic summation of derivatives, the vector summation of complex coefficients in the phasor domain must equal zero to cancel distortions. This necessitates the use of passive networks to maintain zero summation of phasors across a wide range of frequency [142].

Differential current balancing

The capacitive coupling demonstrated in Figure 3.8(b), not only enables g_m boosting, but also enhances IIP2 by mitigating potential imbalances arising from device mismatches and process variations [144].

Assuming the differential currents as follows:

$$i_p = g_{m2}\left(a_1 v_i + a_2 v_i^2 + a_3 v_i^3\right) \tag{3.20}$$

$$i_m = g_{m1}\left(-a_1 v_i + a_2 v_i^2 - a_3 v_i^3\right) \tag{3.21}$$

the differential output current is then given by:

$$\begin{aligned} i_{out} = i_p - i_m = a_1(g_{m2} + g_{m1})v_i + a_2(g_{m2} - g_{m1})v_i^2 \\ + a_3(g_{m2} + g_{m1})v_i^3 \end{aligned} \tag{3.22}$$

Thus, the second-order nonlinearity can be notably reduced. This reduction is particularly crucial in feedback LNAs, where minimizing the second-order nonlinearity also contributes to IIP3 enhancement [145].

3.6 Gain Programmability

As discussed in Chapter 2, contemporary receivers require the integration of reconfigurable RFFEs. Given that the LNA gain has a significant effect on the overall NF and IIP3 of the system, it becomes imperative to incorporate adjustable components in LNA design. This ensures the fulfillment of sensitivity and blocking test scenarios. At the same time, the design must be stable and robust across all possible configurations of these adaptable elements.

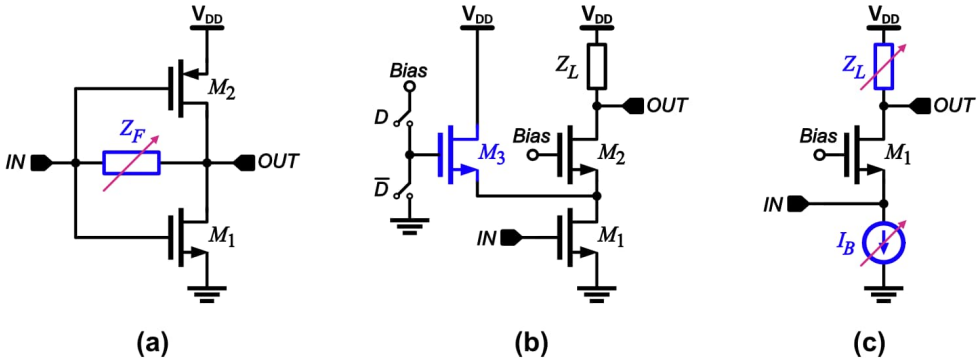

Figure 3.11: Gain programmability through: (a) Adjustable feedback network. (b) Current steering. (c) Variable load and biasing.

In Figure 3.11, three types of programmable LNAs are illustrated. In subplot (a), tunable feedback impedance is featured [146, 147], and the gain can be expressed as:

$$|G_v| = \frac{(g_{m1} + g_{m2})Z_F + 1}{(g_{o1} + g_{o2})Z_F + 1} \tag{3.23}$$

Achieving gain programmability through adjustment of the feedback factor necessitates rigorous simulations to ensure that the amplifier remains stable, and that the bandwidth is not excessively compromised.

Figure 3.11(b) highlights the utilization of the current-steering (or current-bleeding) technique [98, 146], wherein the voltage gain is given by:

$$|G_v| = g_{m1} \frac{g_{m2}}{g_{m2} + g_{m3}} Z_L \tag{3.24}$$

Although the combination of coarse digital and fine analog tuning of current division enables a wide range of gain reconfigurability, the power efficiency and bandwidth considerations must be taken into account as they may limit the applicability of this technique.

In Figure 3.12(c), a method for adjusting gain through programmable biasing current and variable load impedance is depicted [148]. It is important to note that this approach might give rise to concerns related to linearity and noise. Moreover, ensuring sufficient reverse isolation is crucial to minimize the influence of load impedance adjustments on input matching and stability.

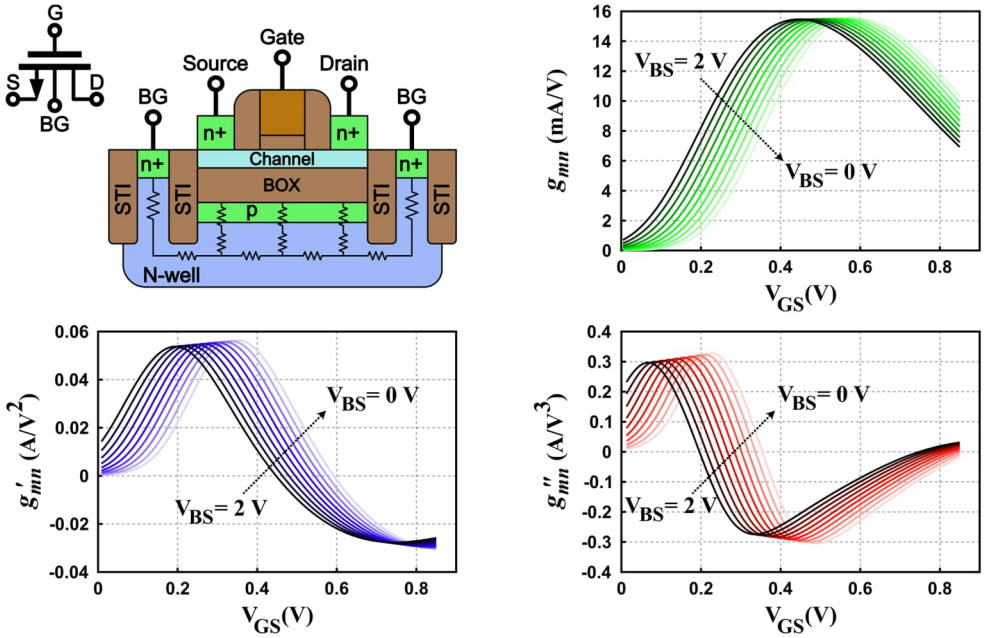

Figure 3.12: The structure of a flipped-well FD-SOI transistor and the effect of body biasing on transconductance and its derivatives.
Simulations performed on an SLVT NFET with L_g = 20 nm, and W = 8 µm.

Body biasing

The presence of a thick oxide layer beneath the channel in FD-SOI process confines the depletion regions, thus relaxing latch-up prevention requirements. By allocating exclusive wells to the most important devices, the injection of noise and leakage of signals through the substrate can be minimized. Furthermore, the I-V characteristic of transistors can be individually programmed by applying a DC voltage to the back gate (BG), which means that devices of the same type with different thresholds can be implemented next to each other.

Figure 3.12 illustrates the typical structure of a flipped-well NFET in FD-SOI process [149]. By applying a positive voltage (up to 2 V in 22FDX) to the back-gate terminal, the threshold voltage of the device decreases (for PFETs negative BG voltage is applicable). As shown in Figure 3.12, this shift causes the profiles of g_m and its derivatives to move to the right of the g_m-V_{GS} diagram. Consequently, by controlling the BG voltage, the amplifier's gain can be tailored for diverse scenarios across a broader range [150]. Moreover, when coupled with the derivative superposition, the body biasing can further extend the linear range of the LNA [143, 151]. Compared to the gain control through adjustment of the front-gate voltage, the drain current and g_m demonstrate less sensitivity to BG voltage alterations, allowing for fine gain tuning using low-resolution DACs.

It is noteworthy to underscore that the impedance of interconnects linking the BG terminal of a device with the programmable voltage source, can potentially exert a noticeable impact on the high-frequency performance of the LNA as well as its stability. Within NR FR1, the findings expounded in [149] demonstrate that making use of a large resistor (~1 MΩ) to connect the BG terminal to the control voltage source results in reduced variations in the output resistance, as compared to the case of a direct zero-Ohm connection.

3.7 Balun-LNAs

The conversion of an unbalanced signal received from an antenna into a balanced (differential) signal offers several advantages. Differential signaling doubles the SNR (i.e., plus 3 dB), notably reduces even-order nonlinearities, and improves the CMRR and the system's resistance to crosstalk and parasitic couplings. Therefore, it is advantageous to implement this conversion in the receiver chain as close to the antenna as feasible.

For this purpose, as illustrated in Figure 3.13(a), passive baluns can be used. These baluns do not consume DC power and are quite linear. However, on-chip transformers often exhibit high insertion loss and limited bandwidth while occupying considerable die area. Additionally, these two crucial performance metrics of passive baluns are subject to a trade-off [152].

Alternatively, this conversion can be embedded into LNAs to create active baluns [153, 154]. However, besides linearity concerns attributed to balun-LNAs, potential imbalances in transfer functions from the input to the inverting and non-inverting outputs must be addressed.

Figure 3.13(b) depicts the circuit model of an RFFE, where the initial stage is a balun-LNA with mismatched transconductances ($G_1 \neq G_2$) and loads ($Z_{L1} \neq Z_{L2}$). These mismatches result in imbalances in both amplitude and phase at the output nodes, namely OUT+ and OUT-, giving rise to three major concerns:

1- **Unwanted feedback loops:** In an ideal differential amplifier, the internal supply (V_{DD}) and ground (GND) nodes are supposed to be signal ground, with no signal current flowing outside the chip from these nodes. However, as demonstrated in Figure 3.13(b), the output imbalance challenges this assumption, allowing signal current to flow through the wirebond impedance. This creates undesirable feedback loops that may cause stability issues. To tackle this, multiple wirebonds should be used in parallel for both GND and V_{DD} connections to lower the equivalent impedance. Moreover, larger on-chip decoupling capacitors (C_{DEC}) are required to create low-impedance paths between GND and V_{DD} at higher frequencies. In direct sampling receivers, where the RFFE amplifies the signal without frequency translation, the feedback current from the final stages can be strong enough to induce stability

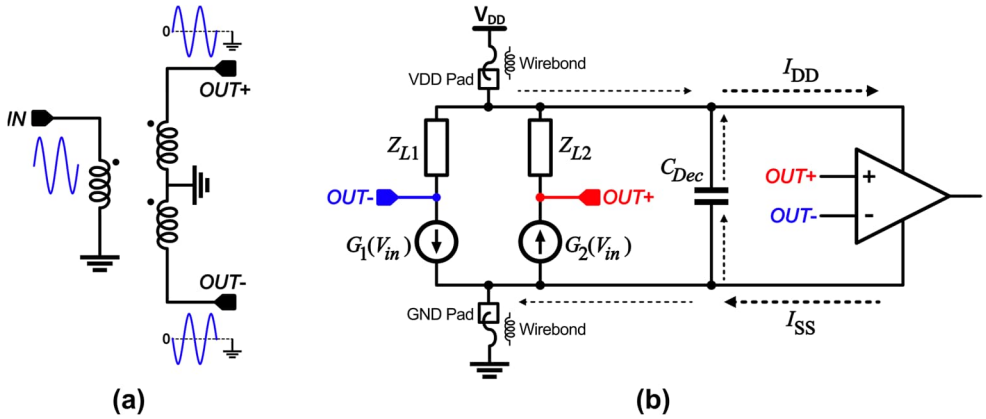

Figure 3.13: (a) Unbalanced-to-balanced conversion using a passive balun. (b) The challenge of output imbalance in active baluns.

issues. Consequently, both decoupling and wirebond treatment are more serious concerns in this type of front-ends.

2- **Limited IIP2 improvement:** In an ideal differential stage, the fundamental signal component is doubled, and the second-order distortion is completely suppressed. However, in the presence of mismatch, the fundamental output is diminished, and a second-order product appears at the output [48]. This phenomenon is illustrated in Figure 3.14(a) in the phasor domain. These effects collectively contribute to a decline in the improvement of IIP2 compared to a single-ended stage. As seen in Figure 3.14(b), while the IIP2 improvement for negligible amplitude and phase imbalances is above 40 dB, the presence of only 1 dB gain and 5 degrees phase imbalances limits the improvement to 16 dB.

3- **DC offset:** An additional consequence of combining imbalanced signals is the generation of a DC offset, which can introduce mixing issues as discussed in Chapter 2.

3.8 Thesis Contribution

The contributions of this thesis to the topics addressed in this chapter are outlined as follows:

Paper I: A Wideband Balun-LNA for Sub-6-GHz 5G NR with Multi-Mode Operation in 22-nm FD-SOI

In this contribution, the utilization of programmable biasing currents enables multi-mode operation, enhancing the blocker tolerance and noise performance of a CG-

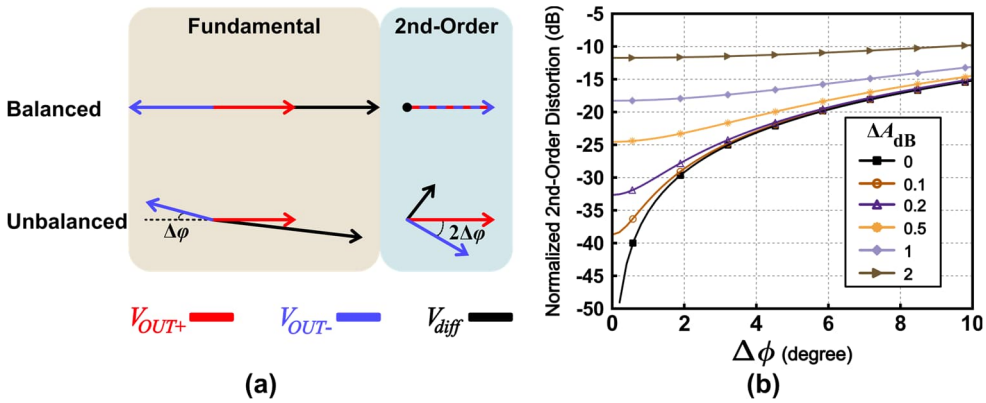

Figure 3.14: The effect of phase/amplitude imbalance on the generation of second-order nonlinearities: (a) Phasor-domain illustration. (b) Numerical analysis.

CS noise-cancelling balun-LNA. Body biasing and derivative superposition are employed to extend the linear range. The balun-LNA topology comprises current-reuse g_m-boosted CG and CS branches, and bandwidth extension is achieved through capacitive feedback. This LNA covers the entire NR FR1 and has been incorporated in the RFFE architecture detailed in Paper II, Paper III, and Paper V.

Paper IV: Broadband RF Front-End Featuring a Reconfigurable Q-Enhanced Filter for Upper Mid-Band 6G Receivers

In this paper, a cascoded CS LNA with resistive feedback is presented, featuring a dual-resonant T-network for wideband input matching. At the output, a broadband passive balun is incorporated to provide balanced signals for subsequent stages of the RFFE. This LNA covers the entire upper mid-band spectrum of 6G.

Furthermore, the circuit techniques discussed in this chapter, such as capacitive cross-coupling, current bleeding, variable feedback, and others, are applied in the core of the filter, subtractor, and PGA within the RFFEs detailed in Paper II, Paper III, and Paper V.

Chapter 4

RF Filters

Considering the crucial role of the filter in direct RF sampling receiver chain—acting as an anti-aliasing and blocker-rejection component as discussed in Chapter 2—this chapter is devoted to an overview of the performance metrics and key aspects of RF bandpass filters. Following this, an investigation into passive and active alternatives ensues, accompanied by an analysis of the advantages offered by Q-enhanced filters which constitute a central theme of this thesis. Concluding this chapter, we will provide insights into the measurement setup, verification techniques, and the importance of calibration in mitigating uncertainties. Furthermore, we touch upon the integration of ML methods to enhance the calibration process.

4.1 Specifications of RF Filters

Depicted in Figure 4.1 is the typical frequency response of a BPF, which divides the frequency spectrum into three distinct regions: 1) the passband region, 2) the transition region, and 3) the stop-band region. The filter's performance within each of these regions is evaluated through designated performance metrics. Depending on the intended applications, certain metrics might hold greater significance in the filter design. In the following, a brief overview of these specifications is provided:

Center frequency and bandwidth

The center frequency (f_c) is at the midpoint of the passband region, and the bandwidth is defined as the difference between the lower and upper 3-dB corner frequencies, represented by f_l and f_h, respectively. A related parameter, known as

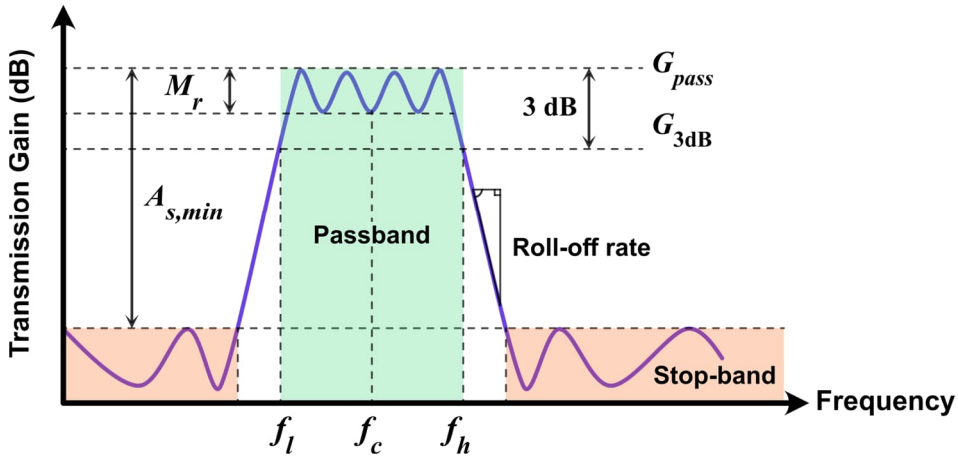

Figure 4.1: Typical frequency response of a bandpass filter.

fractional bandwidth (FBW), denotes the ratio of the bandwidth to the center frequency:

$$FBW = \frac{f_h - f_l}{f_c} \tag{4.1}$$

In addition, the quality factor (Q_{filter}) of a BPF is commonly characterized as the inverse of the FBW.

Passband ripple

The maximum fluctuation magnitude in the filter's transmission gain across the passband region is quantified by the passband ripple (M_r), which is typically expressed in dB. This parameter serves as an indicator of the passband gain flatness, a factor that can be of great importance in wideband applications.

Roll-off rate

The rate at which the transmission gain changes in the transition region is denoted by the roll-off rate, typically measured in decibels per decade (dB/dec). A larger roll-off rate corresponds to steeper edges, enhanced selectivity, and superior tolerance against close-in blockers.

Ultimate rejection

The lowest level of suppression exhibited by a filter in the stop-band region is referred to as ultimate rejection ($A_{s,min}$). In practical implementations, secondary effects such as the parasitic couplings and leakage tend to limit the ultimate

rejection. This factor is particularly important for achieving sufficient OOB blocker rejection.

Insertion loss (IL)

Due to losses in the resistive elements of filters, the transmission gain within the passband may be negative. In this case, the difference between the power levels at the filter's output and input is recognized as insertion loss. This aspect holds particular relevance in passive filters, where the insertion loss serves as a decisive benchmarking parameter as it aligns with the filter's NF.

Group delay

This parameter quantifies the time delay encountered by the envelope of signals oscillating around a center frequency as they traverse a system. For LTI systems, the group delay is mathematically expressed as follows:

$$t_g = -\frac{d\angle H(j\omega)}{d\omega} \tag{4.2}$$

where $\angle H(j\omega)$ represents the phase response of the system.

Order and type

The order of a filter is determined by the number of poles in its transfer function. A higher order corresponds to a narrower transition region and a steeper roll-off. For instance, maintaining all other parameters unchanged, a fourth-order filter achieves a roll-off rate that is twice as large as that of a second-order filter.

Filters with the same order can exhibit different characteristics depending on their type. The choice of a maximally flat magnitude (MFM) response, as in Butterworth filters, is aimed at minimizing M_r. In contrast, Chebyshev filters trade off passband flatness for a sharper roll-off. In use-cases where timing is paramount, the pursuit of linear phase (constant group delay) may be relevant, a goal that can be attained through the implementation of a Bessel filter [155].

Dynamic range

In conventional receivers employing passive off-chip band-select filters, the gain compression, and the generation of spurs in amplifiers and mixers have been the limiting factors in achieving high DR. However, with the adoption of active on-chip filters in fully integrated solutions, new concerns have arisen, specifically centered around the DR of filters. In these receivers, the DR of filters need to match or exceed that of the mixers and amplifiers [156]. Two distinct interpretations of the filter's DR can be recognized. The first one considers the input power level corresponding to the 1-dB compression point (P_{1dB}) [156], while the second incorporates the IIP3

to calculate the intermodulation-free dynamic range (IMFDR3) [157]. These definitions can be formulated as:

$$DR_{Fil} = P_{1\text{dB}}[\text{dBm}] - P_n[\text{dBm}] \tag{4.3}$$

$$IMFDR3 = \frac{2}{3}(IIP3[\text{dBm}] - P_n[\text{dBm}]) \tag{4.4}$$

In these equations, P_n stands for the integrated input-referred noise power within the passband.

Cost

The costs associated with implementing filters include several factors, such as DC power consumption, chip area and form factor, compatibility with CMOS technology for integration, and the complexity of tuning mechanism and calibration schemes.

Active filter FoMs

Among the various metrics used to evaluate the performance of RF active filters, three key FoMs are commonly employed for thorough comparison.

1- **FoM$_1$:** This FoM is established using the concept of DR as defined in Equation 4.3 [156]:

$$\text{FoM}_1 = DR_{Fil} + 10\log_{10}\left(\frac{BW}{P_{DC}}\right) \tag{4.5}$$

where BW and P_{DC} represent the filter's bandwidth and DC power consumption, respectively.

2- **FoM$_2$:** Drawing on IMFDR3 as expressed in Equation 4.4 [157]:

$$\text{FoM}_2 = IMFDR3 + 10\log_{10}\left(\frac{N \times BW}{P_{DC}}\right) \tag{4.6}$$

in which N denotes the filter's order.

3- **FoM$_3$:** This FoM is formulated to emphasize bandwidth adjustability [158]:

$$\text{FoM}_3 = \frac{OIP_3 \times f_{max} \times TR \times N}{(F_{fil} - 1) \times P_{DC}} \tag{4.7}$$

where OIP_3 accounts for the output-referred third-order intercept point, f_{max} represents the maximum achievable cut-off frequency, and TR and F_{fil} stand for the tuning range and the noise factor of the filter, respectively.

4.2 Passive RF Filters

Passive filters have found extensive use in RFFEs as band-select filters placed before the LNA. These filters, constructed without active components such as transistors and diodes, have the advantage of zero DC power consumption and provide a considerably high DR. Nevertheless, these filters have drawbacks for being employed in 5G applications demanding wideband and multiband signal reception. In the subsequent sections, we provide a brief overview of passive filters, while also pointing to the limitations they possess. These limitations underscore the imperative need for the development of active filters in fully integrated RFFEs.

4.2.1 Acoustic Filters

SAW and BAW resonators are deployed to construct RF filters characterized by high selectivity and linearity. As illustrated in Figure 4.2(a), an electroacoustic resonator exhibits a series resonance at f_s and a parallel resonance at f_p [159]. The BVD circuit model is employed as an electrical representation for piezoelectric resonators. The frequency gap between f_s and f_p determines the bandwidth of acoustic ladder filters—an example is depicted in Figure 4.2(b). This frequency separation depends on the effective electromechanical coupling coefficient (k_{eff}), a measurable parameter that pertains to each material and mode of resonance. This parameter is mathematically linked to the resonance frequencies as follows [160]:

$$k_{eff}^2 \approx \frac{\pi^2}{4}\left(\frac{f_s}{f_p}\right)\left(1-\frac{f_s}{f_p}\right) \tag{4.8}$$

By knowing the value of this parameter, the FBW of a typical ladder filter network can be calculated as [161]:

$$FBW \approx \sqrt{\left(\frac{12}{\pi^2}\right)k_{eff}^2+1}-1 \tag{4.9}$$

As discussed in Chapter 2, receivers supporting CA within NR FR1 require a band-select filter with an FBW of 40%. This FBW corresponds to k_{eff}^2=79%. However, this demand poses a physical constraint against the utilization of SAW

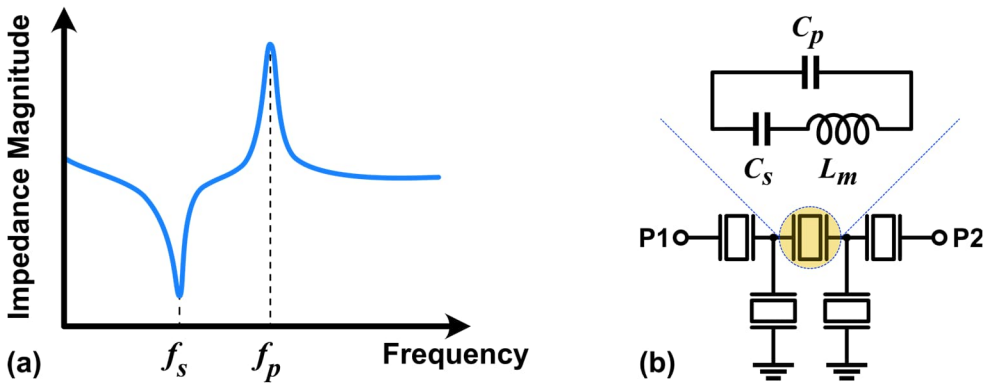

Figure 4.2: (a) Impedance of an electroacoustic resonator.
(b) A ladder acoustic filter alongside the BVD model.

and BAW filters, which are fabricated using CMOS compatible AlN films [162]. The typical values for k_{eff}^2 of these structures are around 10% [161, 163, 164], thereby resulting in an FBW of approximately 6%.

In addition to this fundamental obstacle, several other drawbacks of acoustic filters for being utilized as band-select filter or AAF in direct RF sampling RFFEs can be highlighted:

1- **Limited frequency range:** SAW filters are typically limited to 3 GHz owing to their need to narrow interdigital electrodes, resulting in lower Q and higher IL as frequency increases [165]. On the other side, BAW filters impose considerably higher implementation costs [166] and are susceptible to the emergence of spurious modes at higher frequencies [165]. These aspects have hindered commercial deployment of BAW filters beyond 6 GHz.

2- **High insertion loss and limited ultimate rejection:** Below 6 GHz, an IL ranging from 2 dB to 3 dB is expected. However, for higher frequencies such as within the upper mid-band frequency range, the value of Q is notably reduced, and IL can escalate up to 40 dB [167]. Furthermore, OOB ultimate rejection, particularly for relatively large FBWs, can fall below 20 dB [164, 168].

3- **Spurious modes:** Typically, the transmission gain of these filters exhibits undesired resonances in the stop-band region, degrading the OOB blocker rejection of the receiver [164]. Additionally, the presence of these spurious modes impairs the performance of ladder filters and other wideband structures composed of several SAW or BAW filters [160].

4- **Large chip area and CMOS compatibility**: Despite the possibility of creating monolithic chips housing both CMOS switches and acoustic resonators for multi-band receivers, the area occupied by such parallelization

can be substantial, reaching die areas as large as 12 mm^2 [169]. Furthermore, achieving fully integrated solutions might necessitate the inclusion of specialized fabrication steps and treatments, adding to the cost of the process.

5- **Fixed characteristics:** The center frequency and bandwidth of individual SAW and BAW filters are solely determined by the physical dimensions and properties of the substrate material. As a result, attaining reconfigurability must be sought through complex and bulky topologies comprised of switches, variable capacitors, and off chip inductors [160, 166, 169]. These additional elements exacerbate IL and increase design complexity, thus introducing challenges in maintaining signal integrity.

4.2.2 Distributed-Element Filters

These filters consist of waveguides, transmission lines (TL), and passive resonators. The characteristics of these filters depend on the geometry and quality factor of these passive components, the coupling between them, and the substrate loss. These filters can be constructed using microstrip lines [170]-[174], coupled lines [173, 175, 176], stubs [171]-[173], [176]-[180], substrate integrated waveguides [181, 182], and vertical TLs, employing multilayer printed circuit boards (PCBs) and low-temperature co-fired ceramic (LTCC) technology [183, 184].

Distributed-element filters can realize single-band [175, 177], [183]-[185], dual-band [170, 171], [178]-[180], or multi-band BPFs [172]-[174], [176]. Furthermore, by implementing close-to-passband transmission zeros, high roll-off rates beyond 100 dB/GHz are achievable [180, 183]. However, for 5G FR1 applications, these filters face several limitations:

1- **Physical limits to miniaturization:** The dimensions of these structures are determined by the guided wavelength (λ_g), which is closely tied to the operating wavelength ($\lambda_0 = c/f_0$, where c represents the speed of light in vacuum) [186]. This parameter is always larger than the free-space wavelength. As the value of λ_0 ranges from 73 cm to 42 mm across the 5G FR1 spectrum, the filters designed for this frequency range require substantial board area and are characterized by large form factors. Nevertheless, as the operating frequency increases, these structures can be miniaturized and integrated on CMOS chips for mm-wave and sub-THz applications [187]-[190].

2- **Large in-band IL:** Particularly in wideband high-order implementations, the in-band IL can reach levels beyond 2 dB [170, 173, 176], leading to a higher NF.

3- **Undesired resonance modes:** Typically, these filters exhibit high-frequency resonance modes, limiting OOB ultimate rejection to less than 20 dB [187].

4- **Necessity for matched inputs and outputs**: In the context of direct sampling receivers, where the filter is situated in the middle of the receiver chain,

deploying these filters demands that the signal exits the chip after the LNA and returns at the input of the PGA. This means that the output of the LNA and the input of the PGA must be impedance-matched to minimize the reflection ratio. This design constraint degrades the bandwidth and noise performance of these blocks.

5- **Interdependence of center frequencies in multi-band implementations**: The center frequencies of passbands commonly lack independent adjustability, resulting in a limitation on the number of configurations supported by the filter.
6- **Lack of programmability**: Distributed-element filters are not commonly reconfigurable through electronically switched components. Their frequency range and roll-off rate are primarily determined by their geometry. Although designs such as [191] have employed variable capacitors to tune filter response, the applicability and adjustment range of these techniques do not meet the demands of 5G FR1 radios.

4.3 Active RF Filters

Active filters employ a combination of both passive and active components to shape the frequency response. They offer several advantages compared to their passive counterparts, including amplification, digital programmability, enhanced versatility, compactness, and superior compatibility with CMOS scaling. However, the implementation of active filters also presents various limitations and challenges. The use of transistors can compromise linearity, introduce additional noise, and render the circuit more susceptible to PVT variations, all while consuming DC power. To address these issues, specific circuit design techniques are necessary.

In the overview of active RF filters, we omit active-RC and switched-capacitor filters, which are commonly employed as baseband filters in the receiver chain. These filters rely on high-gain operational amplifiers and utilize feedback to mitigate nonlinearity which limits the operational bandwidth [192]. Moreover, in modern technologies characterized by low intrinsic gain and reduced power supplies, implementing high-gain and wideband operational amplifiers for 5G FR1 applications is challenging, especially if the power efficiency is a concern [193]. In this section, we provide an overview of the advantages and disadvantages of three major types of RF filters which are G_m-C, N-path, and Q-enhanced filters. We will also highlight the typical frequency ranges in which they operate.

4.3.1 G_m-C Filters

A G_m-C filter comprises capacitors and operational transconductance amplifiers (OTAs), enabling an inductorless filter design [156]. This type of filter is

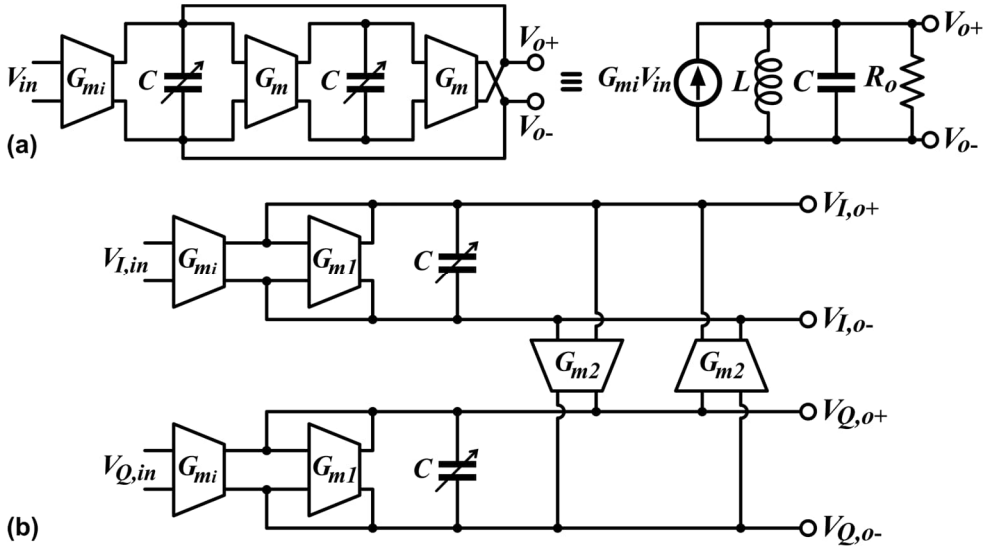

Figure 4.3: (a) Gyrator-based G_m-C BPF. (b) Tunable G_m-C complex BPF.

particularly advantageous in baseband and IF applications, where the integration of on-chip inductors becomes impractical due to their size and inherent losses. G_m-C filters offer power-efficient and compact solutions in such scenarios. Their relatively simple topology and layout make them well-suited for CMOS scaling, and these filters can be tuned digitally by switching capacitors or adjusting transconductance values.

Figure 4.3 illustrates two commonly used G_m-C structures employed in receiver chains to implement a BPF. In subplot (a), a gyrator-C active inductor creates a synthetic resonator, introducing complex poles into the frequency response [194]-[197]. This resonator can be used in series or parallel with the signal path to create bandpass or band-stop (notch) filters [196]. The center frequency and quality factor of this filter are determined by the following equations [197]:

$$\omega_c = G_m/C \tag{4.10}$$

$$Q = G_m R_o\left(1 + C_p/C\right) \tag{4.11}$$

where, R_o and C_p represent the output resistance and total output capacitance of the G_m-cell. These equations reveal trade-offs between adjustability range, power consumption, center frequency, FBW, linearity, and noise in a gyrator-C filter. For example, when aiming to improve NF at a fixed center frequency and for the same FBW, increasing G_m necessitates a proportional increase in C, resulting in larger occupied area which also corresponds to higher losses as well as a limited

adjustability range due to additional parasitic capacitance. Moreover, constructing high-Q resonators, especially at RF frequencies, poses challenges in advanced CMOS technologies characterized by low intrinsic gain.

In Figure 4.3(b), a complex G_m-C BPF is created by cross-connecting in-phase and quadrature paths through G_m-cells (i.e., G_{m2}) [198, 199]. In this structure, the center frequency and quality factor are derived as [198]:

$$\omega_c = G_{m2}/C \tag{4.12}$$

$$Q = 0.5G_{m2}/G_{m1} \tag{4.13}$$

As evident from these equations, in this structure, the filter parameters are interdependent, which limits the adjustability unless the gain is compromised. Practical considerations also constrain high-Q (low-FBW) implementations due to stability concerns [200]. In addition, this structure results in a first-order roll-off rate, which does not meet the stringent blocker requirements of 5G receivers discussed in Chapter 2.

While G_m-C filters are efficient choices for baseband and IF sections of RF chains in applications like mixer-first receivers, low-power wake-up receivers [195], SI and close-in blocker rejection [196, 201], and IoT applications [194], they face limitations that hinder their usage as RF filters in frequencies exceeding 1 GHz:

1. **Sensitivity to PVT variations:** G_m-C filters exhibit susceptibility to PVT variations. This sensitivity affects the center frequency, quality factor, and transmission gain, necessitating complex tuning scenarios and auxiliary subsystems. The tunable G_m introduces linearity variations, excess noise, and additional poles in the system [202], potentially leading to stability issues. Mitigating G_m-cell nonlinearity often requires auxiliary G_m-paths, which cancel third-order nonlinearity but come at the cost of increased noise and power consumption [197]. While various automatic tuning loops have been presented in the literature, many rely on a PLL to address undesired center frequency variations [203], incurring a significant power overhead as frequencies approach the upper limits of the 5G FR1.
2. **Low DR in narrowband configurations:** The dynamic range of a G_m-C filter depends on the setting parameters and power consumption according to the following equation [156]:

$$\text{DR} \propto FBW \times P_{DC}/\omega_c \tag{4.14}$$

Thus, at the same ω_c, maintaining the required DR in narrowband configurations necessitates an increase in power consumption compared to wideband settings. Moreover, achieving the same DR at higher center frequencies demands more power consumption.

3. **Low roll-off rate:** In recent CMOS process nodes, due to the low intrinsic gain, cascaded G_m-C filters which are intended to provide higher-order filter responses, experience degradation in the roll-off rate and produce a rounded passband gain [156].

4.3.2 N-Path Filters

Leveraging the inherent transparency of passive mixers and the translation of baseband (BB) impedance to LO frequency (f_{LO}), N-path filters have the capability to reject OOB interfering signals [204]. As depicted in Figure 4.4(a), an N-path BPF employs N non-overlapping periodic pulses with $1/N$ duty cycle to drive N switches, each connected to identical BB impedances (Z_{BB}). In the case where f_{RF} equals f_{LO}, this mixer-first receiver not only down-converts the RF signal but also rejects OOB interfering signals. In the vicinity of the harmonics of f_{LO}, this filter can be modeled as an LTI circuit, as illustrated in Figure 4.4(b). In this circuit, the impedance seen from the RF node (Z_{IN}) can be formulated as [204]:

$$Z_{IN} = R_{SW} + \sum_{k=1}^{\infty} [\gamma_k Z_{BB}(f - kf_{LO})] \parallel Z_{SH,k} \tag{4.15}$$

where R_{sw} denotes the switch resistance, γ_k equals $\mathrm{sinc}^2(k\pi/N)/N$, and $Z_{SH,k}$ represents the power loss resulting from upconversion and reradiation of signals by the k^{th} harmonic of LO [204, 205].

This approach enables precise center frequency tuning across a wide range by adjusting f_{LO}, while also allowing for independent bandwidth tuning by modifying the bandwidth of the BB impedance, which can be tailored for specific purposes such as channel selection or deep-notch interference rejection [206]. However, it is important to note that trade-offs exist between selectivity (roll-off rate), IB linearity, noise figure (NF), and power consumption [206]. As the operating frequency increases, these trade-offs become more pronounced, imposing a practical limit on N-path filter operation beyond 4 GHz.

Considering Equation 4.15, it becomes evident that the switch resistance constrains OOB rejection, as demonstrated in Figure 4.4(b). While using wider transistors can mitigate this loss, it concurrently raises the total capacitive load of the LO buffers, resulting in increased dynamic power consumption [206]. Furthermore, this amplifies parasitic capacitance, leading to de-Qing of the filter and higher insertion loss, thereby negatively impacting the NF [206].

Furthermore, N-path filters suffer from harmonic folding, a phenomenon in which blockers, aggregated interference, and noise components situated at $(1\pm kN)\times f_{LO}$ (k = 1,2,3,…) are folded back into the desired band [206]. This necessitates the use of a larger N to push the first fold-back component to higher frequencies. Moreover, a larger N reduces reradiation loss [205]. However, it comes

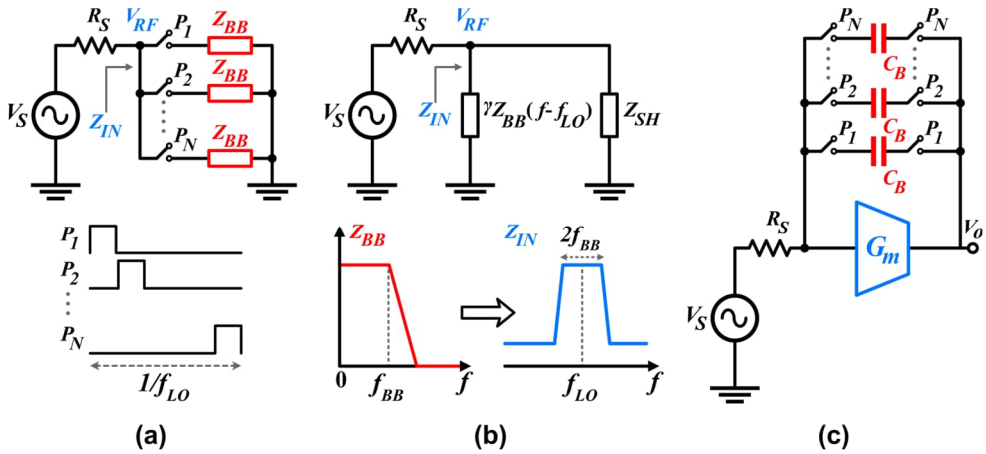

Figure 4.4: (a) An N-path filter and LO phases. (b) LTI equivalent circuit of N-path filter at f_{LO}. (c) An N-path filter in the feedback loop around a G_m-cell.

at the expense of increased dynamic power consumption along with a more complicated process to generate the required non-overlapping clocks.

To enhance the roll-off rate and attain high-order RF filters, there are three primary approaches. In the first approach, transformers and passive networks are employed to couple two or more N-path filters, achieving a roll-off rate of up to 100 [207, 208]. However, these implementations come at the cost of increased insertion loss and a larger occupied die area. Moreover, the undesirable implementation zeros raise the transmission gain at higher frequencies. As a result, the high roll-off rate of these filters is effective only within a limited range of frequencies in the OOB region. This limitation can lead to an OOB rejection as low as 20 dB [207].

The second approach to enhance selectivity is to cascade or couple two or more N-path filters using G_m-cells and active topologies [206, 209]. However, the G_m-cells impose limitations on IB linearity and create a trade-off between power consumption and linearity.

The third approach explores the use of higher-order BB impedances. To achieve this, a closed-loop structure typically employs an operational amplifier to establish a virtual ground [157], [210-214]. For capturing wideband signals, such as those with an aggregated bandwidth larger than 100 MHz in 5G FR1, these structures necessitate an amplifier with a several-GHz gain-bandwidth product (GBW). For instance, a GBW of 7.6 GHz is reported in [214]. However, this can result in high power consumption and stability concerns [157, 214]. In other words, the trade-off between IB linearity and amplifier's power consumption becomes more demanding as the desired bandwidth increases. Moreover, for direct sampling receivers and SAW-less broadband front-ends, where issues like aliasing and noise folding may arise, the impact of undesirable zeros in the transfer function of these feedback structures cannot be neglected [213].

In the pursuit of enhancing IB linearity in highly selective N-path filters, while maintaining acceptable noise performance and without incurring substantial power penalties, several techniques have been introduced. These include incorporating N-path filters in the feedback loops (as illustrated in Figure 4.4(c)) [209, 210], capacitive positive feedback [212], shunting notch [211], and BB noise cancellation [214]. However, these methods result in an increased number of switches, consequently leading to elevated dynamic power consumption. Moreover, the impact of parasitic capacitance and charge sharing becomes more pronounced, resulting in a higher insertion loss and a degraded NF. Both of these effects are exacerbated at higher frequencies.

In addition to the aforementioned trade-offs and design challenges, it is essential to address the impact of clock imperfections and parasitic capacitance on the performance of N-path filters. These specific imperfections are outlined as follows:

1. **Increased insertion loss:** At higher frequencies, clock imperfections, such as non-uniform rise/fall times, overlapping clocks, and a sinusoidal waveform instead of an ideal pulse, combined with the presence of switch parasitic capacitance, lead to a higher insertion loss. This increase in insertion loss can degrade the NF by more than 3 dB [215].
2. **Intensified trade-off between power consumption and selectivity:** As frequency increases, the detrimental impact of parasitic capacitance and implementation zeros on the roll-off rate intensifies, posing a significant challenge to the power-efficient implementation of high-order N-path filters.
3. **Exacerbated harmonic folding:** As clock duty cycle deviates from its ideal value and phase skew increases at higher frequencies, harmonic folding occurs across all harmonics of f_{LO} [216].
4. **Impact of LO phase noise:** The profile of NSD at the RF port of the filter depends on the BB impedance and peaks at f_{LO} [217]. In the presence of a strong blocker close to f_{LO}, this noise can raise the noise floor and reduces the DR. Given that achieving a sharp roll-off at high frequencies is more difficult, this noise behavior imposes more stringent requirements on the PLL. It may necessitate higher power consumption in the clock generation and distribution circuits.

An alternative implementation, known as the reflection-mode N-path filter (RMNF), utilizes a passive coupler to relax the requirements on the switch resistance [205, 218]. This approach allows for the use of smaller switches, resulting in reduced power consumption and lower parasitic capacitance. While the outcomes are promising in terms of adapting the concept of N-path filtering for upper midband and 5G FR2 applications, when it comes to frequencies below 6 GHz, on-chip integration of the coupler becomes impractically large and introduces insertion loss, thus compromising the form factor and noise performance.

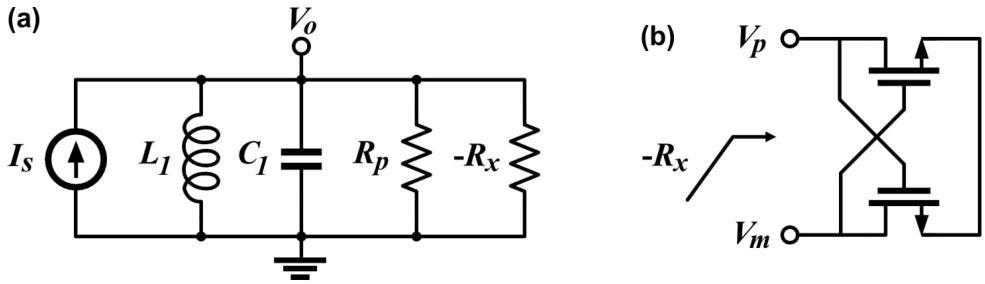

Figure 4.5: (a) Circuit model of a Q-enhanced filter. (b) Cross-coupled structure as an active negative resistance.

4.3.3 Q-Enhanced Filters

While G_m-C and N-path implementations rely on frequency translation and emulative active inductors, Q-enhanced filters utilize a passive inductor for constructing an RF resonator. However, to achieve the desired quality factor and, consequently, the required bandwidth, the losses associated with the passive inductor are partially compensated by employing active structures [219, 220]. In this way, highly selective filters with sharp roll-off can be realized without complexities involved in other types of active filters. Furthermore, as frequency increases beyond the reach of the state-of-the-art N-path filters, on-chip inductors exhibit both a higher quality factor and a more compact form factor, making Q-enhanced filters advantageous when compared to other categories.

The circuit diagram of a Q-enhanced resonator connected to a signal current (I_s) is depicted in Figure 4.5(a). The negative resistor ($-R_x$) is realized by active circuits, such as cross-coupled pair shown in Figure 4.5(b) which produces a $-2/g_m$ small-signal equivalent differential resistor.

The quality factor of this enhanced LC-tank at the resonance frequency (ω_o) is given by:

$$Q_{tank} = \frac{1}{(G_p - G_x)L_1\omega_o} \tag{4.16}$$

where $G_p = 1/R_p$ and $G_x = 1/R_x$.

Thus, this circuit can be employed as a second-order filter [219-223]. The center frequency can be dynamically adjusted by using variable capacitors, such as varactors, MOS capacitors, or a bank of digitally switched capacitors. The FBW can be tuned in a wide range through changing the cross-coupled pair's biasing current.

The magnitude and phase of the impedance of this enhanced LC-tank can be written as:

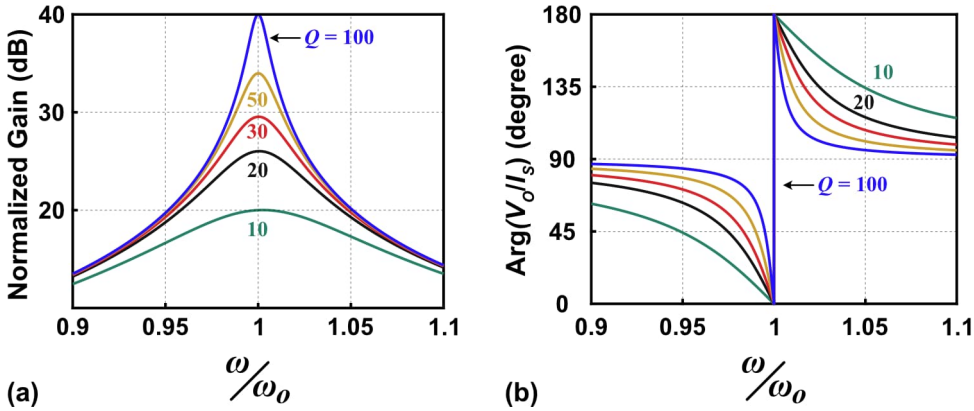

Figure 4.6: Impedance of a Q-enhanced resonator close to the resonance frequency: (a) Magnitude. (b) Phase.

$$|Z_{tank}| = \frac{\left(\frac{\omega}{\omega_o}\right)}{\sqrt{\left(1-\left(\frac{\omega}{\omega_o}\right)^2\right)^2 + \left(\frac{1}{Q_{tank}}\right)^2}} L_1\omega_o \tag{4.17}$$

$$\angle Z_{tank} = \frac{\pi}{2} - \tan^{-1}\left(\frac{\frac{1}{Q_{tank}}}{1-\left(\frac{\omega}{\omega_o}\right)^2}\right) \tag{4.18}$$

Figure 4.6 shows the calculated results based on Equations 4.17 and 4.18 in the proximity of the resonance frequency for a set of Q_{tank} values (the magnitude is normalized to $L_1\omega_o$). From these plots we can conclude that the magnitude is a linear function of Q_{tank}. Thus, if an adjustable Q-enhanced tank is inserted within an RFFE, it produces different values of the current-to-voltage transmission gain depending on the intended FBW. Therefore, a PGA is required to equalize the receiver gain across all configurations.

Furthermore, it is essential to consider the sensitivity of the enhanced resonator to the value of G_x, especially since this circuit is susceptible to oscillation when $G_p \leq G_x$. As the narrowband filtering requires a larger G_x, the risk of oscillation becomes more pronounced when the FBW decreases.

As discussed in the previous sections, for 5G FR1 applications, second-order filter response is not sufficient to adequately suppress close-in blockers. Therefore, we will introduce two types of architectures, based on Q-enhanced LC tanks, to realize higher order filters.

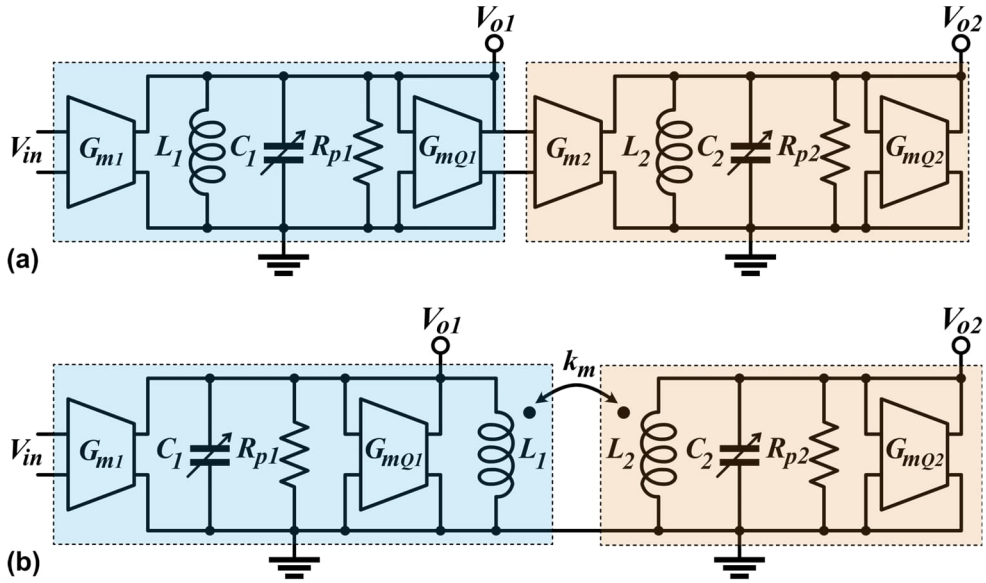

Figure 4.7: A Fourth-order Q-enhanced filter through: (a) Cascading. (b) Magnetic coupling.

High-order filtering through cascading and coupling

A $2N^{th}$-order filter can be implemented by cascading N Q-enhanced LC tanks. As depicted in Figure 4.7(a), the voltage across the first tank (V_{o1}) stimulates the inputs of the G_m-cell in the second stage. Thus, the filter's input (V_{in}) is filtered twice by second-order LC tanks, resulting in a fourth-order BPF response [224-227]. If all the N stages are centered at the same frequency, a narrowband BPF with $40N$ dB/dec roll-off rate is achieved. On the other hand, for wideband filtering the resonance frequencies need to be distributed within the passband, where the separation between them ($\Delta\omega$) and the quality factor of individual resonators determines M_r. For instance, Figure 4.8 depicts the magnitude and phase of the transmission gain for a cascaded fourth-order filter across different values of Q. As shown, a specific combination of $\Delta\omega$ and Q must be chosen to attain a desired bandwidth, while M_r does not exceed a certain tolerable ripple.

Another approach towards constructing high-order filters is to magnetically couple two or more Q-enhanced LC tanks [228, 229, 230], as demonstrated in Figure 4.7(b).

However, these implementations suffer from the following drawbacks:

1- **Limited dynamic range:** In cascaded filters, the linearity of the stages placed at the end of the chain must be notably higher than that of the initial stages. Particularly, in the case of high-Q filtering, the last stage might be fed by highly amplified in-band blockers, which leads to desensitization and

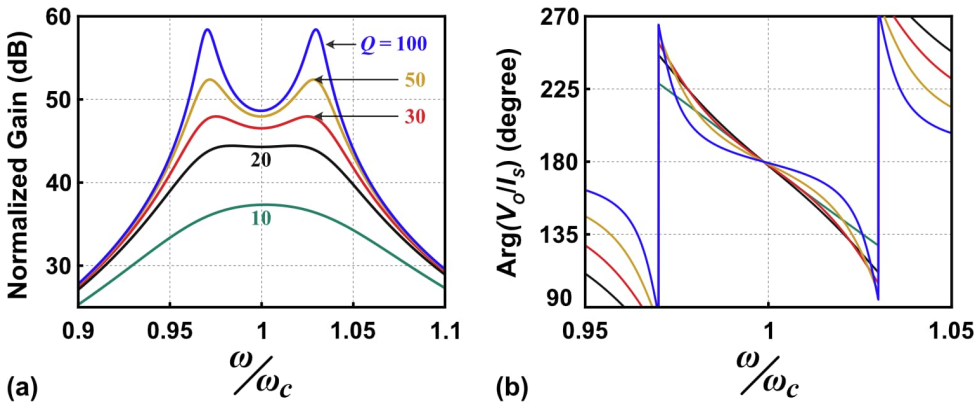

Figure 4.8: Impedance of a fourth-order Q-enhanced filter close to the center frequency: (a) Magnitude. (b) Phase.

saturation. Similarly, the loss of passive components and magnetic coupling degrades the DR in the transformer-based approach.

2- **Loading effect:** Since the impedance of subsequent stages loads each LC tank, the Q tuning can be a complex process in practical implementation.
3- **High sensitivity:** The sensitivity of the overall response to individual components is intensified through cascading. Particularly, in the transformer-based approach, the performance of the filter highly relies on the coupling coefficients. This requires thorough modeling and extensive simulation to ensure a satisfactory level of agreement between simulation and experimental results.
4- **Challenging frequency tuning at low frequencies:** Realizing a cascaded or magnetically coupled filter that fulfills the fine adjustment of both center frequency and quality factor is challenging in NR FR1 radios, where a broad range of frequency spectrum is to be covered.

High-order filtering through parallelization

In this alternative approach, the DR of a second-order resonator is maintained while creating a fourth-order BPF response. This is achieved by feeding the signal current into two resonators concurrently and then subtracting the voltages across them from each other as illustrated in Figure 4.9. It can be mathematically proven that such a subtraction results in the following transmission gain [231]:

$$Q_{tank} = \frac{\omega_{o1}\omega_{o2}\left(\frac{\omega_{o2}}{Q_1} - \frac{\omega_{o1}}{Q_2}\right)s}{\left(s^2 + \left(\frac{\omega_{o1}}{Q_1}\right)s + \omega_{o1}^2\right)\left(s^2 + \left(\frac{\omega_{o2}}{Q_2}\right)s + \omega_{o2}^2\right)} \tag{4.19}$$

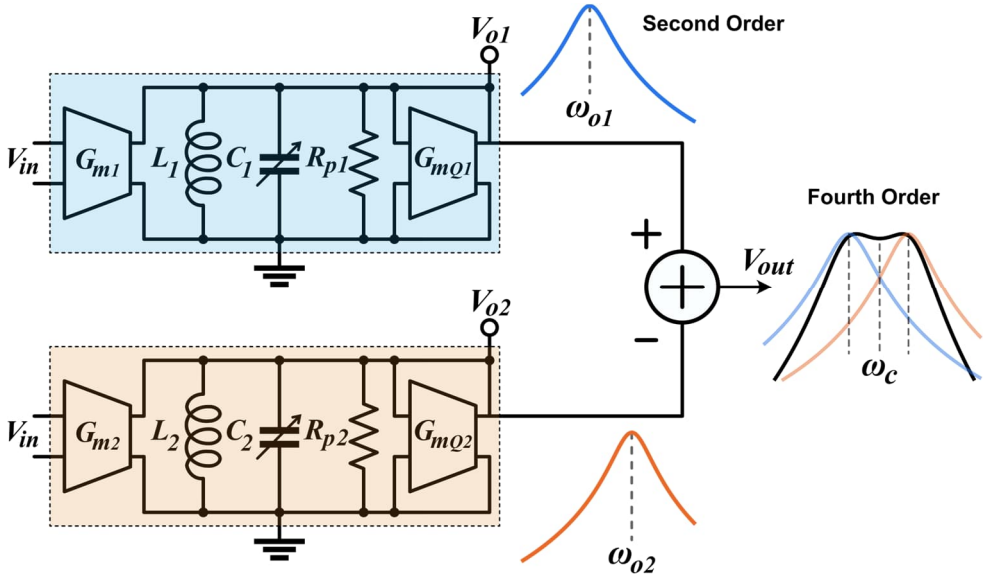

Figure 4.9: Concept and architecture of a fourth-order Q-enhanced filter achieved by subtracting.

where ω_{o1} and ω_{o2} represent the center frequencies, and Q_1 and Q_2 denote the quality factors.

Consequently, when parasitic coupling and pulling effects are negligible, the center frequency of the resonators and quality factors can be adjusted with minimal loading effects. This allows for FBW adjustments ranging from a few percent to above 50%. As presented in Paper II, this transfer function can be tailored to various configurations depending on the maximum acceptable M_r and desired roll-off rate. The FBW has a direct relationship with $\Delta\omega$, while it is inversely proportional to the quality factors [231].

Nevertheless, to utilize this solution in direct RF sampling receivers for 5G applications, these practical concerns must be addressed:

1- **Trade-off between die area and isolation:** Imperfect isolation between the resonators degrades the DR and complicates the adjustment process. The physical distance between the inductors determines the isolation of the resonators. Thus, to minimize pulling and leakage effects, the compactness of the design might be compromised. However, special layout techniques such as 8-shaped inductors can be employed to relax this trade-off.

2- **Low-noise implementation:** Despite cascading, in this approach, the input-referred noise of each resonator reaches the input of the filter without attenuation. Hence, a low-noise, moderately linear circuit implementation is required.

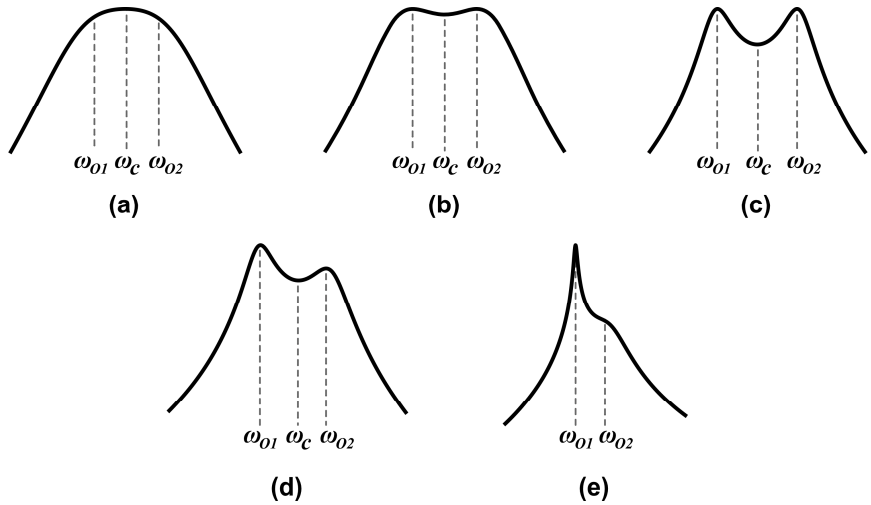

Figure 4.10: Various responses of a Q-enhanced filter in the presence of PVT variations: (a) Under-enhanced. (b) Desirably enhanced. (c) Over-enhanced. (d) Asymmetrical. (e) Lopsided.

3- **Uncertainty and sensitivity issues:** While this architecture is less susceptible to loading effects when compared to cascading and coupling techniques, the Q-enhanced resonators can still experience issues like oscillation or deviation from the desired BPF response. Methods to mitigate these effects will be discussed later in this chapter.

4.4 Uncertainties and Calibration

Stochastic PVT variations can potentially induce oscillations or lead to under/over-enhanced states in Q-enhanced filters. To uphold the stability and desired functionality of the filter, the implementation of calibration and trimming schemes becomes imperative.

4.4.1 Effects of PVT Variations on Q-Enhanced Filter

Process variations include deviations in the values of capacitors, extending up to ±10%. This discrepancy contributes to an approximate ±5% uncertainty in adjusting resonance frequencies. In addition, g_m and g_{ds} of G_m-cells and cross-coupled pairs vary from sample to sample. Concurrently, mismatches in differential structures introduce uncertainties in G_p and G_x values. Assuming that both transconductances

are Gaussian random variables with an equivalent standard deviation (σ_G), the quality factor of an enhanced tank exhibits almost the same degree of dispersion.

Supply voltage variations can affect the biasing currents and voltages of G_m-cells, potentially leading to undesired oscillation, distortion, and more pronounced nonlinearities. Similar to VCOs, particularly in the case of employing varactors for frequency tuning, this deviation from nominal V_{DD} can induce a "pushing effect" [232].

Temperature variations not only change the conductivity of devices, and thereby the transconductances, but also trigger deviations in the impedance of passive interconnects by affecting resistivity. These variations can also manifest themselves in frequency response and undermine noise performance.

Apart from the critical concern of oscillation, PVT variations can result in anomalies in the transmission gain. Figure 4.10 illustrates five potential cases of frequency response of a fourth-order Q-enhanced filter, including:

1- **Under-enhanced:** Q_1 and Q_2 fall below required values for the existing $\Delta\omega$, or the resonance frequencies are closer to each other than intended.
2- **Desirably enhanced:** The resonators are both appropriately adjusted.
3- **Over-enhanced:** Both Q_1 and Q_2 exceed the desired values, or $\Delta\omega$ is larger than expected.
4- **Asymmetrical:** Q_1 is larger than the proper value, or Q_2 needs to be increased, or ω_{o1} is smaller than expected, or ω_{o2} requires an upward shift.
5- **Lopsided:** Q_1 is substantially larger than Q_2, posing a potential risk of oscillation.

4.4.2 Calibration Schemes

Before delving into the specific calibration schemes designed for RF filters and RFFEs, it is important to outline the various categories of calibration methods.

From a system-level perspective, calibration methods can be categorized into foreground and background calibrations. Foreground calibration is performed when the device under test (DUT) is not actively operational, while background calibration is conducted concurrently with the normal system operation. Although background calibration offers the advantage of uninterrupted data reception, it requires minimal loading effects and power consumption. Conversely, foreground calibration can rigorously measure the system's key performance indicators, resulting in more accurate and reliable adjustments. Therefore, a commonly adopted hybrid calibration strategy involves more frequent minor background calibration complemented by less frequent but thorough foreground calibration.

From a practical standpoint, calibration systems can be implemented either on-chip or off-chip. Off-chip implementations necessitate accessible test points within the chip's subsystems, potentially leading to an increase in the number of pads and packaging costs. However, the measurement instruments used in off-chip schemes

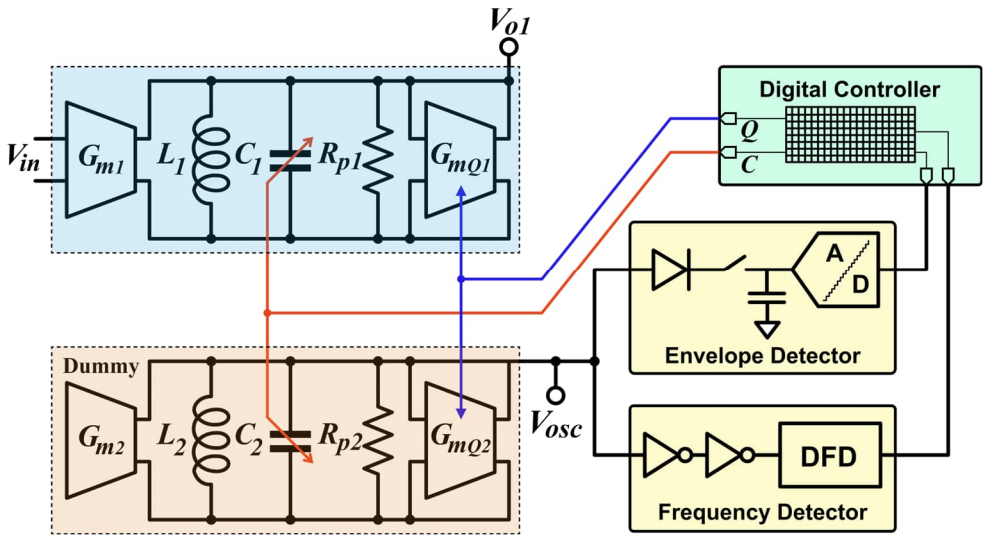

Figure 4.11: Architecture of primary-replica calibration method.

are generally more accurate, and there is often more available processing power and memory dedicated to this purpose. Conversely, on-chip calibration provides access to a multitude of measurable parameters and a wide range of control settings, although this may lead to a compromise in terms of measurement accuracy.

A calibration scheme is a solution to an optimization problem, involving the minimization of an error function through the adjustment of a defined set of control parameters guided by a policy. Given the well-defined characteristics of Q-enhanced filters, it is possible to establish a function between the control parameters ($Q_{1,2}$, $\omega_{o1,2}$, and $G_{m1,2}$) and the target parameters. Subsequently, the error function is calculated from the difference between the measured and target values. The calibration policy is formulated to minimize the error function through an iterative procedure. An optimal calibration policy is distinguished by its efficiency concerning implementation costs and the algorithm's convergence time.

In the subsequent sections, our focus will turn to the exploration of on-chip calibration schemes specifically suited for direct-sampling RFFEs featuring Q-enhanced filters.

Primary-replica calibration

In this approach, as demonstrated in Figure 4.11, one of the filters is deliberately configured to oscillate, and the resonance frequency is subsequently measured by a digital frequency detector (DFD) [233, 234]. Concurrently, an envelope detector monitors the onset of oscillation, and by measuring the amplitude of oscillations, it contributes to the calculation of the quality factor. Then, the capacitor value is increased to bring down the resonance frequency to the intended value for the

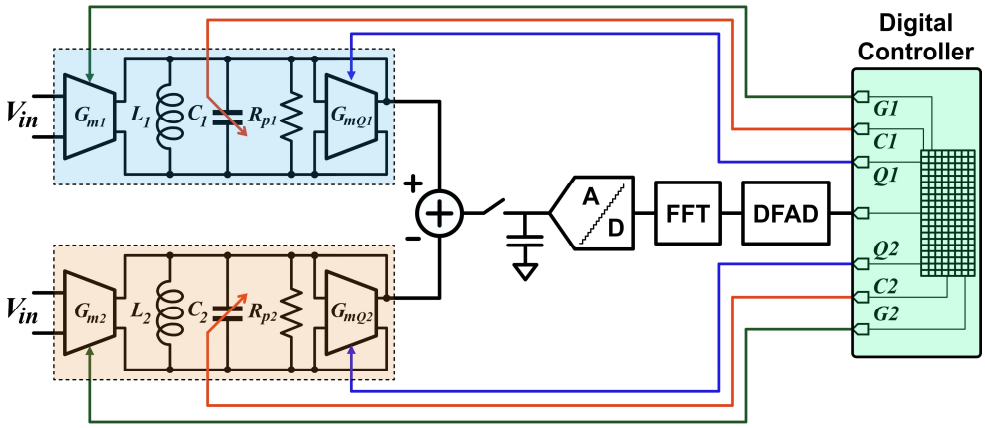

Figure 4.12: Architecture of on-chip digital calibration in a direct RF sampling receiver.

desired filter configuration. In parallel, the Q value is fine-tuned based on the measured oscillation parameters. The control parameters of both replica and primary units are set to the same values, under the assumption that they are matched and have the same structure. While this scheme proves effective for calibrating Q-enhanced filters in case of stable operation and minor PVT variations, its applicability diminishes when being employed for non-identically implemented resonators. For example, the filter structure presented in Paper II utilizes different types of transistors in the construction of its two resonators.

Reinforcement-learning-assisted controller

One of the most notable advantages of direct RF sampling receivers is their capacity to observe the entire spectrum. Essentially, such receivers come equipped with an on-chip spectrum analyzer that serves well for calibration purposes.

Figure 4.12 provides a conceptual depiction of on-chip digital calibration for an RF sampling receiver. During calibration, the receiver input is connected to either a single-tone frequency-sweeping source or a wideband noise source. In this architecture, the filter output is digitized, and its spectral components are derived through FFT. Subsequently, a digital frequency and amplitude detector (DFAD) identifies peak amplitudes within the output spectrum and their corresponding frequencies. These measured data then enable recognition of the filter's status, empowering a digital controller to determine the necessary adjustments for the resonator parameters.

To establish a fully digital control and calibration system, current-DACs are commonly employed for the adjustment of G_m-cells. Switched-capacitor banks are digitally programmed to tune the resonance frequencies.

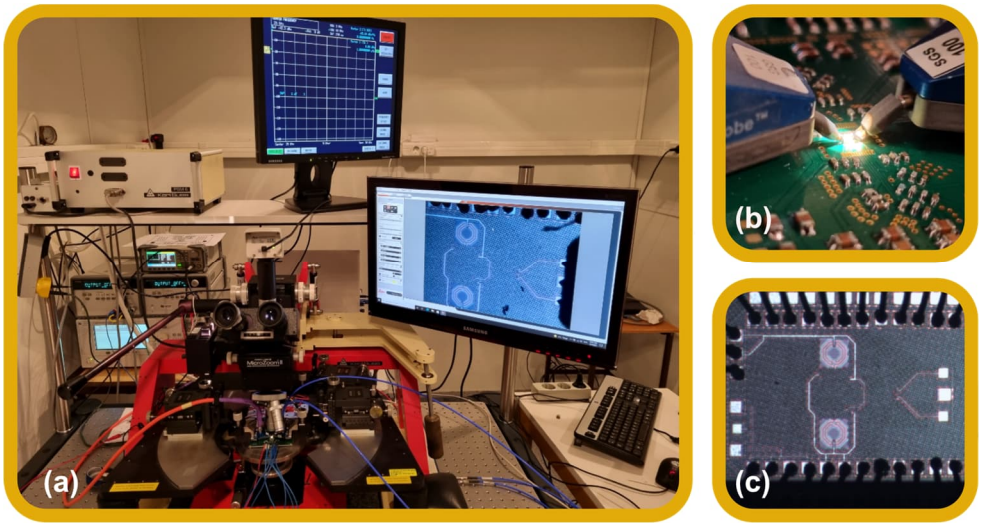

Figure 4.13: (a) Measurement setup. (b) Probing.
(c) A microphotograph of the wire-bonded chip.

Yet, given the diverse range of uncertainties that could lead to similar imperfections and anomalies in the frequency response, implementing a conventional digital controller necessitates exhaustive system characterization, including secondary effects. This requires extensive measurements, robust circuit models, and thorough mathematical formulation, which often proves to be unfeasible. For instance, as discussed earlier, an asymmetrical response represents a complex deviation that could arise from a combination of PVT variations. Attempting to encompass all potential mechanisms within a conventional controller to efficiently minimize deviations is intricate and almost impractical.

Hence, while system characterization and mathematical modeling is achievable to a certain extent, and the effect of tuning each parameter on the shape of the frequency response can be predicted, the optimal sequence of decisions and the minimum calibration time can be achieved through reinforcement learning. In other words, while a conventional controller is constructed based on the existing knowledge of the system, the tuning gradients of each parameter between successive measurements and the optimal order of adjusting Q, G_m, and center frequencies are acquired through learning by an RL-agent.

4.5 Measurement and Verification

In the characterization of the RFFE and its key component—a reconfigurable Q-enhanced filter—as depicted in Figure 4.13, a GSG Infinity probe was used for

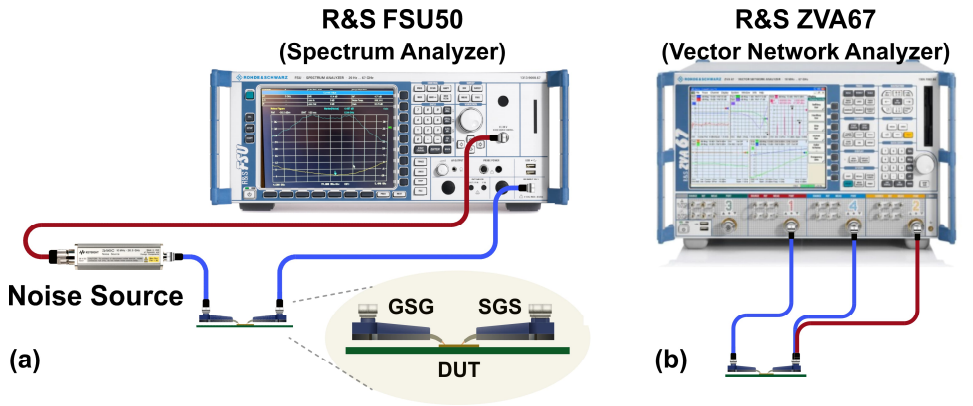

Figure 4.14: Experimental setup for measuring (a) NF and (b) S-parameters.

feeding in an unbalanced input, and a balanced output was measured through an SGS probe. All the bias references, supply, ground, and digital signals are connected using wire-bonding (Figure 4.13(c)). Noise, gain, and linearity measurements were conducted using two primary setups, the details of which will be elucidated in the following sections.

4.5.1 Noise and gain measurements

The noise figure of the RFFE was measured adopting the Y-factor method, in which a wideband noise source (Keysight 346C) with an excess noise ratio (*ENR*) of 15 dB was employed. The setup for this measurement is depicted in Figure 4.14(a).

Figure 4.14(b) illustrates the utilization of a vector network analyzer (Rohde & Schwarz ZVA67) to measure S-parameters. These parameters were used to evaluate transmission gain as well as input and output matching. To circumvent potential unintended spurious signals that could arise due to mismatches in the electrical length of connections at the output, the instrument was configured in "true differential mode." Figure 4.15 shows the S-parameter calibration process using a standard substrate and the short-load-open-through (SLOT) method.

4.5.2 Linearity measurements

As illustrated in Figure 4.16(a), P_{1dB} and IIP3 measurements were conducted using two signal generators (Keysight E8257D) and a spectrum analyzer (Rohde & Schwarz FSU50). The evaluation of IB-IIP3 was achieved through a two-tone test with a frequency spacing of 10 MHz, as depicted in Figure 4.16(b). For measuring OOB-IIP3, two tones were spaced from the center frequency by Δf and $2\Delta f$, where $\Delta f > BW$, as shown in Figure 4.16(c).

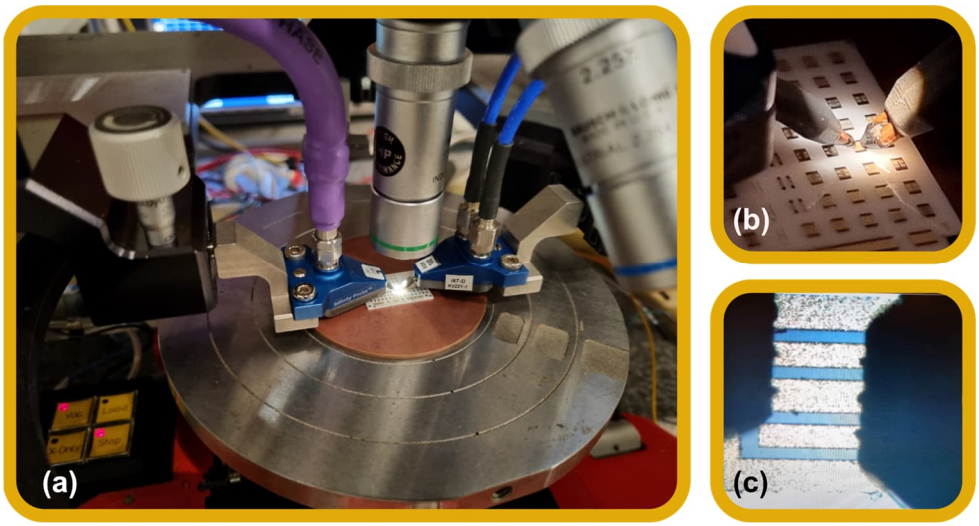

Figure 4.15: S-parameter calibration setup: (a) Probe station. (b) Calibration substrate. (c) A closer view.

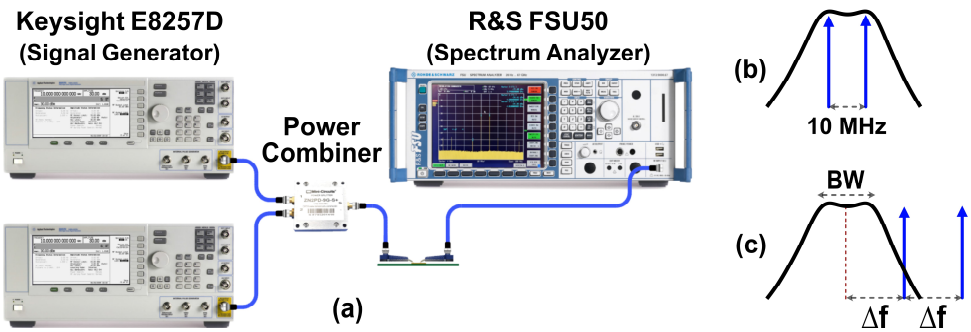

Figure 4.16: (a) Experimental setup for linearity measurements. Frequency settings in two-tone test for measuring (b) IB-IIP3 and (c) OOB-IIP3.

4.6 Thesis Contribution

In the following the research contributions of this thesis are highlighted to the subjects covered in this chapter.

Paper II: A 1.7-6.4 GHz fourth-order RF filter with 1-40% fractional bandwidth in 22-nm FDSOI

This contribution presents a low-power, low-voltage, compact implementation of a synthetic fourth-order Q-enhanced filter. Fabricated using cutting-edge 22-nm FD-SOI CMOS technology, this design provides a remarkable 1% to 40% FBW adjustability and significant gain programmability. Given its wide coverage of the spectrum, the filter finds applicability in receiver RFFEs for 5G FR1 applications.

Paper III: A Reconfigurable RF Filter with 1-40% Fractional Bandwidth for 5G FR1 Receivers

This paper introduces a reconfigurable front-end tailored for 5G FR1 direct sampling SDRs. Comprehensive characterization of the front-end reveals a FoM that surpasses state-of-the-art published designs catering to the same frequency range. Leveraging various circuit techniques elucidated in Chapter 3, the front-end attains power consumption under 45 mW while excelling in both sensitivity and linearity test scenarios. The paper also reports on the stochastic variations of the quality factors concerning PVT uncertainties. The paper also demonstrates how considering design margins and making use of body biasing effectively compensate for these variations.

Paper IV: Broadband RF Front-End Featuring a Reconfigurable Q-Enhanced Filter for Upper Mid-Band 6G Receivers

In this contribution, we extend the filtering-by-subtracting concept to materialize a multiple-mode filter. It can be configured as a dual-band fourth-order filter, a dual-band filter with an OOB notch, or a wideband filter with an IB notch. Furthermore, this filter is specifically tailored to meet the requirements of the forthcoming 6G upper mid-band transceivers. The integration of 8-shaped inductors serves to minimize undesirable pulling effects and parasitic couplings, simultaneously achieving a compact and power-efficient implementation.

Paper V: Wideband programmable RF front-end for 5G direct sampling receivers

This paper, in continuation of Paper III, presents an in-depth circuit analysis on the effectiveness of capacitive cross-coupling, current bleeding, and body biasing techniques in linearizing the RFFE. Particularly it demonstrates a linearization technique for Q-tuning cross-coupled pairs. In addition to presenting the structure

of the gain-equalizing PGA and the output buffer, it proposes a calibration algorithm and an RL-assisted scheme to minimize the calibration time.

Chapter 5

Conclusions and Outlook

In this thesis, a top-down analysis of the challenges inherent in receiver design for 5G and beyond telecommunication technologies is provided. We have demonstrated how the deployment of advanced frequency allocation techniques like CA and DSS, coupled with the utilization of high-order digital modulation schemes to enhance spectral efficiency, intensifies the conventional trade-offs in designing energy-efficient, low-noise, and highly tolerant receivers.

Throughout this research, we have outlined the advantages and disadvantages of various receiver architectures, with a particular focus on the potential of the direct RF-sampling approach for realizing spectrum-aware SDRs and CRs. However, the promising capabilities of direct sampling receivers can only be fully harnessed if we can develop highly adjustable RF front-ends that cover a wide frequency range. These front-ends are required to offer significant reconfigurability for the reception of various frequency bands, bandwidths, and power levels.

We have emphasized the advancement in mixed-signal and switched-capacitor circuits, made possible by the progress in deeply scaled-down CMOS technologies. However, we have also highlighted the challenges these cutting-edge process nodes pose for RF designers, including lower voltage headroom, intrinsic gain limitations, increased resistance of interconnects and gates, self-heating effects, and substrate loss. This underscores the need for exploring more digitalized and versatile solutions, which have been at the heart of this research project.

We have discussed the significance of high-DR RF filters with sharp roll-off characteristics in the performance of direct RF-sampling receivers. In that regard, we have provided an overview of passive and active alternatives, with a specific focus on the design of Q-enhanced filters tailored for 5G and beyond use-cases. These filters combine current-reuse, noise-cancelling, g_m-boosting, and capacitive cross-coupling techniques to achieve high tolerance and low-noise performance.

Furthermore, we have leveraged body biasing, a feature of FD-SOI technology, to achieve superior control over the behavior of individual transistors. This has enabled gain adjustment and the mitigation of PVT variations in all blocks of the receiver chain.

Drawing from the content of the included papers, the achievements of this doctoral dissertation are summarized as follows:

- Investigation of gain, noise, and linearity requirements of 5G FR1 front-ends, with a particular emphasis on the direct RF-sampling receiver architecture.
- Design and implementation of a balun-LNTA capable of covering the entire 5G FR1 spectrum. This circuit can be programmed for low-noise or high-tolerant operation modes to succeed in both sensitivity and blocking verification scenarios.
- Design and implementation of a reconfigurable Q-enhanced filter with widely adjustable center frequency, FBW, and gain.
- Integration of the previously mentioned blocks, along with a PGA, to create a complete RF front-end chain with 15 dB to 49 dB gain, 1% to 40% FBW, and 55 dB ultimate OOB rejection. This flexibility accommodates various test scenarios and CA strategies.
- Adoption of a calibration method to address uncertainties in our design, achieving optimized implementation cost and latency.
- Extension of the developed filter concept for future wireless technologies operating in upper mid-band frequency range and requiring multiple mode filters to capture wideband signals while simultaneously rejecting OOB interferences.

Considering the broader landscape of RF circuit and system design, as well as the evolving trends in wireless technology, the following developments building upon the outcomes of this research project are proposed:

- Integrating a high-speed ADC to complete the front-end, enabling system-level verification and facilitating further optimizations.
- Designing and integrating a self-calibration unit in a complete transceiver architecture, which consists of DACs and transmitter-side amplifiers for generating stimuli during the calibration process.
- Investigating the feasibility of employing auxiliary low-resolution ADCs for on-chip linearity assessment and spectrum observation based on the principles of compressive sensing and feature extraction.
- Evaluating and optimizing the RFFE performance when integrated into MIMO CRs that utilize digital/hybrid beamforming techniques.
- Conducting system-level power optimization that includes all the components of a receiver, i.e., RFFE, PLL, ADC, and DSP.

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