# Design and Control of Long-Pulse High-Power Klystron Modulators

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# Design and Control of Long-Pulse High-Power Klystron Modulators

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Design and Control of Long-Pulse High-Power Klystron Modulators

# Design and Control of Long-Pulse High-Power Klystron Modulators

Max Collins


LUND
UNIVERSITY

DOCTORAL DISSERTATION

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*Faculty opponent*
Dr. Craig Burkhart, Stanford (SLAC National Accelerator Laboratory)

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**Abstract**

The European Spallation Source (ESS) is an under-construction material science research facility in Lund, Sweden, and will upon completion host the most powerful superconducting linear accelerator (linac) in the world. The ESS linac is powered by klystron modulators required to deliver long high-power pulses (pulse amplitude 115 kV/100 A, pulse length 3.5 ms, pulse repetition rate 14 Hz) of very high quality (combined flat top ripple and droop < 0.15% of the pulse amplitude, pulse-to-pulse variability < 0.15% of the pulse amplitude, 0-99% pulse rise time < 150 µs) while maintaining excellent AC grid power quality (low flicker operation < 0.2%, line current THD < 3%, unitary power factor). Conventionally, solid-state modulators are based on pulse transformers due to their high performance, robustness, simplicity and straightforward design. However, pulse transformer size is fundamentally linked to application pulse length, pulse power and pulse rise time, i.e., considering this modulator topology for the unprecedented and extremely demanding pulse power requirements posed by the ESS linac results in very large and unpractical modulator systems. As an alternative, this dissertation presents the novel Stacked Multi-Level (SML) modulator topology based on a modular power converter chain including an active constant-power capacitor charger (eliminating flicker, line current harmonics and reactive power) and a switched pulse generation stage utilizing a pulse modulation-demodulation technique in effectively eliminating the direct size - pulse length dependency.

This dissertation develops models and design optimization frameworks for both the conventional pulse transformer-based modulator topology, serving as benchmark, as well as the novel SML modulator topology. The developed models are validated through both simulations and experiments, and the use of the optimization frameworks are exemplified through the design and implementation of modulator systems for, e.g., the Facility for Antiproton and Ion Research (FAIR) in Germany and the ESS in Sweden. The developed optimization frameworks are also used to directly compare the two modulator topologies in view of high-power applications (115 kV/100 A) through parametric studies, sweeping the pulse length from 1-10 ms and the pulse repetition rate from 1-50 Hz.

The dissertation ends with a complete description and experimental validation of both a reduced-scale technology demonstrator as well as the full-scale klystron modulators developed for and implemented at the ESS.



**Key words**

Accelerator power supplies, pulse power systems, pulse shaping methods, klystron modulators, high-power electronics, power quality, power conditioning

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# Popular summary

Civilization is currently faced with a number of serious issues and threats, and the European Commission has identified prioritized areas termed grand societal challenges deemed to particularly impact society. These focus areas may be summarized to include energy, transportation, environment and climate, health and life, and foods. From a technological perspective, these problems are in part due to current limitations in and understanding of available materials and their use. Research on and development of new advanced materials could therefore directly and significantly impact all of the above areas. Developments of this kind derive from a deep understanding of the nature and properties of materials, in turn most readily obtained from their internal structure and dynamics. In such studies, neutrons - being charge neutral and therefore having the ability to deeply penetrate and probe material samples - serve as an invaluable tool for scientific inquiry.

The European Spallation Source (ESS) in Lund, Sweden, is an under-construction material science research facility and will upon completion be the brightest neutron source in the world. Its unprecedented neutron flux will greatly facilitate material science experimentation, spurring advances in a number of technical fields with hopes of contributing both to and beyond the above cited challenges of society. As indicated by the name, the ESS is a spallation source, in which a linear particle accelerator accelerates protons to approach the speed of light, ultimately colliding with a heavy metal target in expelling neutrons from the nuclei of the target atoms (spallation). Accordingly, the ESS will host the most powerful linear accelerator in the world. This accelerator is powered by so-called **modulators** drawing power from the electrical grid; converting and shaping it to match the requirements of the accelerator systems. The remarkable accelerator requirements translate into extremely demanding modulator requirements, and it was early realized that conventional modulator technology would not be viable in powering the ESS.

In essence, this work attempts to answer the following questions:

- How to best exploit modern power electronics in developing a new modulator technology suitable for the unprecedented and extremely demanding requirements posed by the ESS linear accelerator application?
- How should the proposed modulator system and the comprising components be designed in attaining an optimized modulator solution?
- How should the modulator power converters be controlled in optimizing power quality, both with respect to the electrical grid and to the accelerator?
- How would the proposed technology compare to conventional solutions?
- How could the proposed technology be used in future upgrades of the ESS accelerator, or even in future more demanding accelerator applications?

# 1. Introduction

In this doctoral dissertation, topics related to power converters intended for pulse power generation in particle accelerator applications are treated. In particular, much of the work has been carried out as part of a Research & Development (R&D) effort in collaboration with the European Spallation Source (ESS) in Lund, Sweden, an under-construction material science research facility based on a linear particle accelerating structure, [1.1].

This introductory chapter aims to provide context and outline the overarching motivation of this work by discussing the background and scientific case for the ESS project. A brief technical description of the ESS project is given with an examination of the consequences for its linear accelerator and power source. This chapter also provides an overview of the dissertation by listing essential contributions to the field of pulsed power technology as well as an account of related scientific writings published by the author and colleagues.

## 1.1 Background

Civilization is currently faced with a number of serious issues and threats. As part of the Horizon 2020 programme the European Commission identified prioritized areas termed *grand societal challenges* deemed to particularly impact society [1.2]. These focus areas may be summarized to include energy, transportation, environment and climate, health and life, and foods. From a technological perspective, these problems are in part due to current limitations in and understanding of available materials and their use [1.3]. Furthermore, it is clear that research on and development of new advanced materials could directly and significantly impact all of the above areas.

Developments of this kind derive from a deep understanding of the nature and properties of materials, in turn most readily obtained from their internal structure and dynamics [1.4]. In such studies, neutrons serve as an invaluable tool for scientific inquiry [1.5]-[1.9]. Neutrons are charge neutral and therefore have the ability to deeply penetrate and probe material samples. In addition, the wavelength of neutrons is generally comparable to the interatomic spacings of condensed matter [1.10]-[1.11]. Neutron waves are therefore scattered when interacting with

materials, and subjecting a material sample to a beam of neutrons yields diffraction patterns containing information about the inner structure of the material [1.10]-[1.11]. Several advanced techniques have been developed based on the ideas of neutron scattering and are used in research studies covering length scales from the order of picometers up to the order of meters, and covering time scales from the order of femtoseconds up to hours [1.12].

The nature of these experiments requires a large flux of neutrons, and neutron scattering facilities obtain the requisite flux by one of two methods-

- Fission: research reactors are nuclear fission reactors intended to serve mainly as a source of neutrons [1.13]-[1.15]. Here, a thermal neutron approaches a uranium nucleus causing a fission event. Several neutrons resulting from the fission go on to cause further fission events in additional uranium nuclei. Consequently, the number of neutrons (and fission events) rapidly grow in a chain reaction. The resulting neutrons may then be collected and used for scattering experiments.

  Some notable reactor-based neutron sources include Institut Laue-Langevin (ILL), [1.16], the High Flux Isotope Reactor (HFIR), [1.17], and the High Flux Advanced Neutron Application Reactor (HANARO), [1.18].

- Spallation: spallation sources utilize a linear particle accelerating structure to collide protons (or electrons, though less effectively) with a heavy metal target, [1.19]-[1.20]. The collision expels neutrons from the nuclei of the target atoms, which may then be collected and used in scattering experiments.

  Some notable spallation sources include the Spallation Neutron Source (SNS), [1.21], the Japan Proton Accelerator Research Complex (J-PARC), [1.22], the ISIS neutron and muon source, [1.23], and the Los Alamos Neutron Science Center (LANSCE), [1.24].

With multiple emerging research areas and increasing problem complexity, neutron science progress is limited by achievable source intensity, [1.25]. Accordingly, the need for a next generation spallation neutron source was identified some twenty years ago, [1.25]. The promising outlook over time developed into an ambitious European commitment titled the European Spallation Source (ESS). In 2009, Sweden was selected as host country for the ESS and, with ground-breaking in 2014, ESS is currently under construction in Lund, Sweden.

Upon completion, ESS will be the brightest and most powerful neutron source in the world, [1.26]. Its unprecedented neutron flux will greatly facilitate material science experimentation, spurring advances in a number of technical fields with hopes of contributing both to and beyond the above cited challenges of society.

## 1.2 The European Spallation Source

The quantity and quality of neutron science-based studies directly depend on the amount of available neutron flux, [1.25]. At ESS, the requisite neutron flux will be obtained via a nuclear reaction called spallation, [1.26]. Here, protons derived from an ion source are accelerated in a linear particle accelerator to approach the speed of light, [1.27]. The accelerated protons are subsequently smashed into a rotating tungsten target, and the ensuing nuclear reaction – spallation – releases free neutrons which are guided to a suite of state-of-the-art neutron science instruments for experimentation, [1.28].

Figure 1.1 shows a comparison of single pulse source brightness as a function of time for ESS, ILL, SNS, J-PARC and ISIS targets 1 and 2. Representing an on-target average beam power of 5 MW, ESS will provide up to 100 times brighter neutron beams than that of current facilities, [1.26]. Upon completion, ESS will be one of the most technologically advanced Big Science facilities on the planet, and its ambitious nature directly impacts the requirements put on each of its systems. In particular, to supply the required high power proton beam, ESS will host the most powerful proton linear accelerator in the world, [1.29]. This linear accelerator is to provide 2.86 ms long proton pulses at 2 GeV repeated at 14 Hz, [1.27]. Corresponding to a 4% duty cycle, accelerator operation requires a collection of pulsed RF power sources capable of delivering 125 MW of peak power. The following sections detail the operation and requirements of the linear accelerator and its power source.

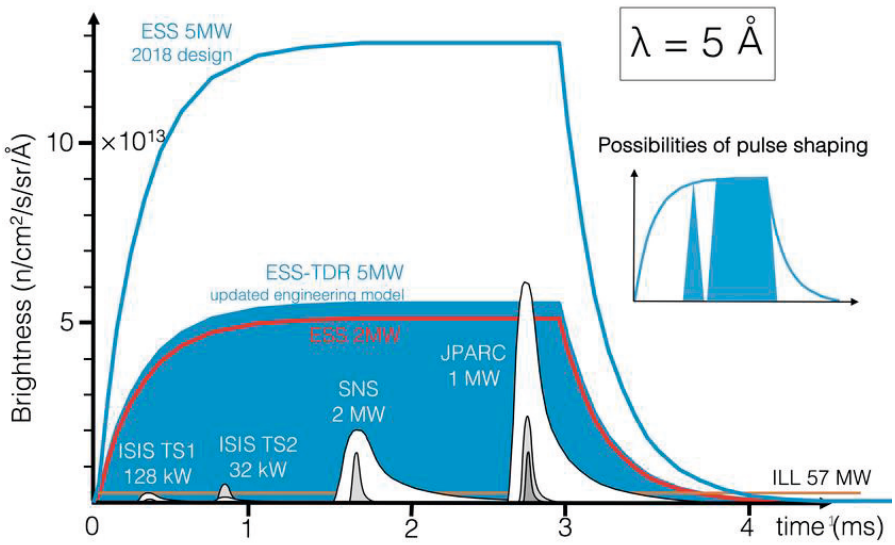



Figure 1.1: Comparison of single pulse source brightness as a function of time for notable neutron sources.

Figure 1.2: Overview of the European Spallation Source. Relative dimensions not to scale.

### 1.2.1 Linear accelerator

The linear accelerator supplies the beam of protons needed for spallation. The ESS will host the most powerful linear accelerator in the world, schematically depicted in Figure 1.3, [1.27].

Accelerator operation is summarized in the following [1.27]-

1. The ion source generates a proton beam.
2. The proton beam is guided via the Low Energy Beam Transport (LEBT) section to the Radio Frequency Quadrupole (RFQ).
3. In the RFQ, the proton beam is bunched and accelerated to 3.6 MeV.
4. The protons are then guided via the Medium Energy Beam Transport (MEBT) section to the drift tube linac (DTL).
5. In the DTL, the proton beam is accelerated to 90 MeV.
6. The DTL is followed by a section of 26 superconducting double-spoke cavities (SPK) accelerating the proton beam to 216 MeV. These cavities have a geometric beta value of 0.50, and are cooled by liquid helium to -271 °C.
7. The proton beam now enters the main part of the linear accelerator comprised by 36 Medium Beta Linac (MBL) cavities and 84 High Beta Linac (HBL) elliptical cavities. The MBL and HBL cavities have a geometric beta value of 0.67 and 0.86, respectively.
8. Following acceleration, the proton beam has reached 96% of the speed of light. The proton beam is guided to the target via the High Energy Beam Transport (HEBT) section.
9. The accelerated beam of protons collides with the tungsten target, causing spallation. Generated neutrons are directed to a suite of instruments for research experimentation.

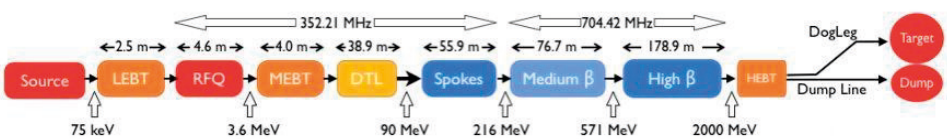



Figure 1.3: Overview of the European Spallation Source linear accelerator.

### 1.2.2 Radiofrequency power amplifiers

For their operation, each of the accelerating cavities (part of the RFQ, DTL, spoke, MBL and HBL sections in the preceding description) requires a radiofrequency power source. In the case of ESS, high power pulsed klystrons are used.

*Klystrons*

Klystrons are vacuum tube radiofrequency (RF) amplifiers, [1.30]-[1.31]. The klystron operating principle is shown in Figure 1.4. Here, the klystron cathode is heated by a filament, producing electrons. By connecting a DC high voltage source between the klystron cathode and anode, the generated electrons are attracted towards the anode. This part of the klystron acts as an electron gun producing a beam of high-speed electrons.

The beam of electrons first passes through what is known as a buncher cavity. This cavity is excited at its resonance frequency with a low power AC signal, generating a standing electromagnetic wave within the cavity. Electrons entering the cavity during one half cycle of the resonance experience an electric field in the same direction as their motion and are consequently accelerated. Electrons entering the cavity during the other half cycle experience an electric field in the opposite direction and are thus decelerated. Following the buncher cavity, the electrons enter the klystron drift space. Here, accelerated electrons catch up with earlier decelerated electrons and vice versa, effectively forming bunches of electrons.

The electron bunches then enter an appropriately positioned second cavity known as a catcher cavity. The bunches excite standing waves in the catcher cavity which may be extracted and directed towards an RF load (in this case an accelerating cavity loaded by a passing proton beam) via a waveguide. If the resonance frequency of the catcher cavity equals that of the buncher cavity, the klystron output is an amplification of the input signal. In this process, the kinetic energy of the electrons is transformed into electric potential energy, decelerating the bunch.

After passing the catcher cavity, the decelerated electron beam is absorbed by a collector electrode at the end of the klystron.

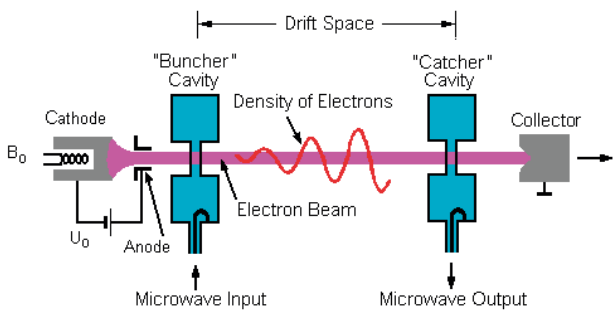



Figure 1.4: Overview of simple two cavity klystron.

In modern klystron amplifiers, multiple buncher cavities are used to further increase the power gain. Here, gains on the order of hundreds of thousands are typical.

For the ESS linear accelerator, 1.5 MW pulsed klystrons have been adopted. The klystrons are distributed along the linear accelerator as follows-

- RFQ: 1 klystron operated at 352.21 MHz.
- DTL: 5 klystrons operated at 352.21 MHz.
- Medium Beta: 36 klystrons operated at 704.42 MHz.
- High Beta: 84 klystrons operated at 704.42 MHz.

### 1.2.3 Power modulators

As explained in the preceding section, klystrons require a high voltage source applied between anode and cathode to provide base electron kinetic energy. Using pulsed klystrons, ESS thereby requires a large number of pulsed high voltage high power sources. These sources are generally referred to as pulsed power modulators, and represent the fundamental electrical power source of the accelerator.

In the case of ESS, the large number of klystrons required by the accelerator made it highly desirable to have each modulator system power multiple klystrons in parallel to reduce the total modulator quantity and thereby cost and accelerator gallery footprint. Ultimately, it was decided that each power modulator should be able to operate four klystrons in parallel according to the below scheme, Figure 1.5-

- One modulator powers the RFQ klystron and one DTL klystron in parallel.
- Two modulators each power two DTL klystrons in parallel.
- Nine modulators each power four Medium Beta klystrons in parallel.
- Twenty-one modulators each power four High Beta klystrons in parallel.

Accounting for the properties of the klystron and component efficiencies, each modulator system is thereby required to supply pulses with amplitude 11.5 MW (115 kV, 100 A) over the full accelerator proton pulse length of ~2.9 ms (the actual modulator pulse length is ~3.5 ms accounting for pulse rise time, pulse stabilization, and cavity fill time) repeated at 14 Hz. Given the high average power associated with the accelerator complex, the 0-99% pulse rise time is limited to 120 μs to ensure high system efficiency. Furthermore, in order to facilitate effective cavity field control, the combined flat top ripple and droop is restricted to 0.15% of the flat top amplitude. In view of contemporary modulator technology, these pulse power requirements are combined in an unprecedented and extremely demanding way.

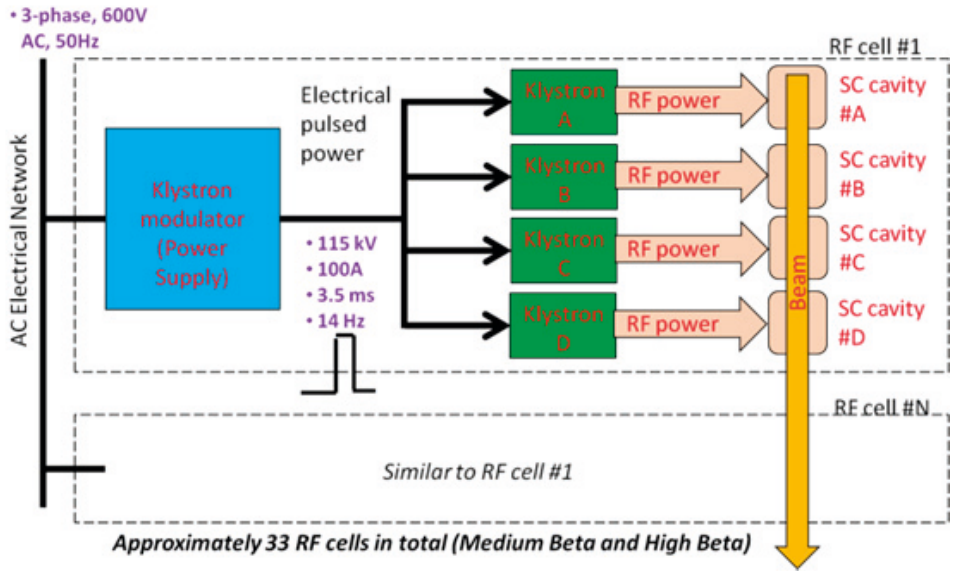



Figure 1.5: Configuration of pulsed power modulators and klystrons for ESS linear accelerator.

## 1.3 Scope and scientific contributions

This dissertation work is part of a joint R&D collaboration between the European Spallation Source and Lund University aimed to develop and implement a modulator topology suitable for the exceptional requirements of the ESS linac and future long pulse high power applications. The scope and scientific contributions of this dissertation include the following items-

- A comprehensive review of available long pulse modulator technology. The working principle, advantages and disadvantages of notable modulator topologies are discussed. The qualities of existing modulator systems are examined and compared in view of ESS application requirements. This review is presented in chapter 2.
- The R&D efforts resulted in a modulator topology now termed the Stacked Multi-Level (SML) modulator topology. A technology demonstrator was designed and implemented, and upon its validation the SML topology was adopted for the ESS linear accelerator modulators. The underlying ideas and fundamental development work is presented in chapter 3. Then, aspects of design, manufacturing and testing for the reduced scale technology demonstrator as well as for the full-scale modulators now in use at ESS are treated in chapters 8 and 9, respectively.

- Modeling and design of SML-type modulators is treated in chapter 5. Design equations for each modulator component are derived. The developed models are incorporated in a framework for SML modulator optimization. The developed models and framework are validated by simulation of and experimentation on a complete full scale ESS SML modulator and its components, chapters 8 and 9.
- Modeling and design of pulse transformer-based modulators is treated in chapter 4. Modulators based on pulse transformers are a serious candidate for many pulse power applications. Design equations for the required modulator components in view of long-pulse high-power applications are developed and incorporated in a framework for optimization. The developed procedure is established by design, simulation and experimental validation of two pulse transformer systems. Importantly, representing a common and proven modulator topology, this framework is also used to check and verify the appropriateness of the developed SML modulator topology.
- Comparison of pulse transformer-based modulators and SML-type modulators. The developed design frameworks are used in considering both modulator types for use in the European Spallation Source linear accelerator project as well as a host of other long pulse high power applications. This comparison is the topic of chapter 6.
- Development of control methods is treated in chapter 7:
    - The capacitor charger of the SML modulator topology represents a significant improvement with respect to conventional modular technology. Advanced control methods have been developed to facilitate flicker free operation with sinusoidal line current absorption and power factor compensation.
    - The SML pulse generator is modular and based on high frequency modulation techniques affording possibilities for more advanced output pulse control. Several control methods are developed and compared with respect to attainable pulse rise time, pulse overshoot and droop compensation.
    - Use of high frequency switching obliges strict transformer flux control in order to avoid transformer saturation. A technique suitable for modular systems including an open loop zero average flux tracking algorithm with built in elimination of pulse-to-pulse remanent flux accumulation has been developed.

## 1.4 List of publications

Part of the work presented in this doctoral dissertation is based on the following list of scientific publications. The publications are divided into journal publications, conference publications, technical reports and other publications. For each category, publications are listed in reverse chronological order-

*Journal publications*

- M. Collins and C.A. Martins, “An Integrated Optimal Design Procedure for Pulse Transformer-based Klystron Modulators for Long-Pulse High-Power Applications”. IEEE Trans. Plasma Sci., vol. 51, no. 11, pp. 3358-3367.
- M. Collins and C.A. Martins, "Design and Control of an Electronic Bouncer Circuit for Volume-Optimal Long-Pulse High-Power Pulse Transformers". IEEE Trans. on Plasma Sci., vol. 50, no. 10, pp. 3692-3700.
- M. Collins and C.A. Martins, “Evaluation of feasibility of high-power long-pulse transformers using single layer and pancake winding techniques”. IEEE Trans. on Plasma Sci., vol. 49, no. 7, pp. 2217-2226.
- M. Collins and C.A. Martins, “Optimal design of electronic bouncers for long-pulse high-power modulators”, IEEE Trans. Plasma Sci., vol. 49, no. 12, pp. 819-829.
- M. Collins and C.A. Martins, “Optimal design of a high voltage DC/DC converter for the 11.5 MW/115 kV ESS long-pulse modulator”, IEEE Trans. Plasma Sci., vol. 48, no. 10, pp. 3332-3341.
- M. Collins and C.A. Martins, “Evaluation of a novel capacitor charging structure for flicker mitigation in high-power long-pulse modulators”, IEEE Trans. Plasma Sci., vol. 47, no. 1, pp. 985-993.
- M. Collins and C.A. Martins, “A modular and compact long-pulse modulator based on the SML topology for the ESS linac”, IEEE Trans. Dielectr. Electr. Insul., vol. 24, no. 4, pp. 2259-2267.

*Conference publications*

- M. Collins and C.A. Martins, "Evaluation of Klystron Modulator Performance in Interleaved Pulsing Schemes for the ESS Neutrino Super Beam Project", 2022 IEEE International Power Modulator and High Voltage Conference (IPMHVC22), Knoxville, TN, USA, 19-23 June, 2022.
- C.A. Martins and M. Collins, "The Stacked Multi-Level Klystron Modulators for the ESS Linac". 2022 IEEE International Power Modulator and High Voltage Conference (IPMHVC22), Knoxville, TN, USA, 19-23 June, 2022.

- B. Gålnander, M. Collins, M. Eshraqi, C.A. Martins, R. Miyamoto, A. Farricker, “Status of ESS linac upgrade studies for ESSnuSB”, in Proc. Int. Particle Accelerator Conference (IPAC19), Melbourne, Australia, 2019.
- M. Collins and C.A. Martins, “Optimal design of a high voltage high frequency transformer and power drive system for long pulse modulators”, in Proc. IEEE Int. Pulsed Power and Plasma Sci. Conf. (PPPS19), Orlando, FL, USA, 22-28 Jun. 2019.
- M. Collins and C.A. Martins, “Evaluation of trends in optimal design of pulse transformers for long pulse high power applications”, in Proc. IEEE Int. Power Modulator High Voltage Conf. (IPMHVC), Jackson Lake Lodge, WY, USA, Jun. 2018, pp. 31-36.
- M. Collins and C.A. Martins, “A constant power capacitor charging structure for flicker mitigation in high power long pulse klystron modulators”, in Proc. IEEE Int. Pulsed Power Conf. (PPC17), Brighton, UK, 18-22 Jun. 2017.
- M. Collins and C.A. Martins, “Zero average flux tracking algorithm for high frequency transformers used in long pulse applications”, in Proc. IEEE Int. Pulsed Power Conf. (PPC17), Brighton, UK, 18-22 Jun. 2017.
- C.A. Martins, M. Collins, G. Göransson, M. Kalafatic, ” Pulsed high power klystron modulators for ESS linac based on the stacked multi-level topology”, in Proc. 28th Linear Accelerator Conf. (LINAC16), East Lansing, MI, USA, 25-30 Sept. 2016.
- M. Collins, C.A. Martins, A. Reinap, G. Göransson, M. Kalafatic, “Stacked multi-level long pulse modulator topology for ESS”, in Proc. IEEE Int. Power Modulator and High Voltage Conf. (IPMHVC16), San Francisco, CA, USA, 5-9 July 2016.
- C.A. Martins, M. Collins, A. Reinap, “Development of a long pulse high power klystron modulator for the ESS linac based on the stack multi-level topology”, in Proc. 7th Int. Particle Accelerator Conf. (IPAC16), Busan, Korea, 8-13 May 2016.

*Technical reports*

- B. Gålnander, M. Collins, M. Eshraqi, C.A. Martins, H. Danared, “H-source design integration into ESS and RF upgrade studies”, 2019.

*Other publications*

- A. Alekou, E. Baussan, A.K. Bhattacharyya, N. Blaskovic Kraljevic, M. Blennow, M. Bogomilov, B. Bolling, E. Bouquerel, O. Buchan, A. Burgman, C.J. Carlile, J. Cederkall, P. Christiansen, M. Collins, E.

Cristaldo Morales, P. Cupiał, L. D'Alessi, H. Danared, D. Dancila, J. P. A. M. de André, J.P. Delahaye, M. Dracos, I. Efthymiopoulos, T. Ekelöf, M. Eshraqi, G. Fanourakis, A. Farricker, E. Fernandez-Martinez, B. Folsom, T. Fukuda, N. Gazis, B. Galnander, Th. Geralis, M. Ghosh, G. Gokbulut, L. Halić, M. Jenssen, A. Kayis Topaksu, B. Kildetoft, B. Kliček, M. Kozioł, K. Krhač, Ł. Łacny, M. Lindroos, C. Maiano, C. Marrelli, C. Martins, M. Mezzetto, N. Milas, M. Oglakci, T. Ohlsson, M. Olvegard, T. Ota, J. Park, D. Patrzalek, G. Petkov, P. Poussot, R. Johansson, S. Rosauro-Alcaraz, D. Saiang, B. Szybiński, J. Snamina, G. Stavropoulos, M. Stipčević, R. Tarkeshian, F. Terranova, J. Thomas, T. Tolba, E. Trachanas, R. Tsenov, G. Vankova-Kirilova, N. Vassilopoulos, E. Wildner, J. Wurtz, O. Zormpa, Y. Zou, "The European Spallation Source neutrino Super Beam Conceptual Design Report", The European Physical Journal ST, vol. 231, no. 21, 2022.

- E. Baussan, N. Blaskovic Kraljevic, M. Blennow, M. Bogomilov, E. Bouquerel, A. Burgman, C. J. Carlile, J. Cederkall, P. Christiansen, M. Collins, E. Cristaldo Morales, L. D'Alessi, H. Danared, J. P. A. M. de André, J. P. Delahaye, M. Dracos, I. Efthymiopoulos, T. Ekelöf, M. Eshraqi, G. Fanourakis, E. Fernandez-Martinez, B. Folsom, M. Ghosh, G. Gokbulut, L. Halić, A. Kayis Topaksu, B. Kliček, K. Krhač, M. Lindroos, M. Mezzetto, M. Oglakci, T. Ohlsson, M. Olvegård, T. Ota, J. Park, G. Petkov, P. Poussot, S. Rosauro-Alcaraz, G. Stavropoulos, M. Stipčević, F. Terranova, J. Thomas, T. Tolba, R. Tsenov, G. Vankova-Kirilova, N. Vassilopoulos, E. Wildner, J. Wurtz, O. Zormpa, Y. Zou, "Update physics performance of the ESSνSB Experiment", The European Physical Journal C, vol. 81, pp. 1-12, 2021.

- A. Alekou and E. Baussan and N. Blaskovic Kraljevic and M. Blennow and M. Bogomilov and E. Bouquerel and A. Burgman and C. J. Carlile and J. Cederkall and P. Christiansen and M. Collins and E. Cristaldo Morales and P. Cupial and L. D Alessi and H. Danared and J. P. A. M. de Andre and J. P. Delahaye and M. Dracos and I. Efthymiopoulos and T. Ekelof and M. Eshraqi and G. Fanourakis and E. Fernandez-Martinez and B. Folsom and N. Gazis and Th. Geralis and M. Ghosh and G. Gokbulut and L. Halic and A. Kayis Topaksu and B. Kildetoft and B. Klicek and M. Koziol and K. Krhac and L. Lacny and M. Lindroos and M. Mezzetto and M. Oglakci and T. Ohlsson and M. Olvegard and T. Ota and J. Park and D. Patrzalek and G. Petkov and P. Poussot and R. Johansson and S. Rosauro-Alcaraz and B. Szybinski and J. Snamina and G. Stavropoulos and M. Stipcevic and F. Terranova and J. Thomas and T. Tolba and E. Trachanas and R. Tsenov and G. Vankova-Kirilova and N. Vassilopoulos and E. Wildner and J. Wurtz and O. Zormpa and Y. Zou, "The European Spallation Source neutrino Super Beam", in Proc. of Snowmass 2021.

## 1.5 References

[1.1] About the European Spallation Source. Accessed: June 5, 2023. [Online]. Available: https://europeanspallationsource.se/about

[1.2] Horizon 2020, societal challenges. Accessed: June 5, 2023. [Online]. Available: https://www.h2020.md/en/content/societal-challenges

[1.3] Why does the EU support research and innovation for chemicals and advanced materials? Accessed: June 5, 2023. [Online]. Available: https://research-and-innovation.ec.europa.eu/research-area/industrial-research-and-innovation/key-enabling-technologies/chemicals-and-advanced-materials_en

[1.4] International Atomic Energy Agency: Materials research. Accessed: June 5, 2023. [Online]. Available: https://www.iaea.org/topics/materials-research

[1.5] N. Kardjilov et al., "Neutron imaging in materials science", Materials Today, vol. 14, no. 6, pp. 248-256, 2011.

[1.6] European Spallation Source: Science using neutrons. Accessed: June 5, 2023. [Online]. Available: https://europeanspallationsource.se/science-using-neutrons

[1.7] M. Bull, "Neutron scattering: Materials research for modern life". Accessed: June 5, 2023. [Online]. Available: https://www.isis.stfc.ac.uk/Pages/impact-of-neutron-scattering-brochure13478.pdf

[1.8] Oak Ridge National Laboratory: Materials and Engineering. Accessed: June 5, 2023. [Online]. Available: https://neutrons.ornl.gov/science/materials-engineering

[1.9] U.S. Department of Energy: Neutron Scattering. Accessed: June 5, 2023. [Online]. Available: https://science.osti.gov/bes/mse/Research-Areas/Neutron-Scattering

[1.10] A.T. Boothroyd, Principles of Neutron Scattering from Condensed Matter, 1st ed. Oxford University Press, 2020.

[1.11] B.T.M. Willis and C. J. Carlile, Experimental Neutron Scattering, 1st ed. Oxford University Press, 2017.

[1.12] European Spallation Source: What Do Neutron Tell Us? Accessed: June 5, 2023. [Online]. Available: https://europeanspallationsource.se/science-using-neutrons#what-do-neutrons-tell-us

[1.13] International Atomic Energy Agency: Exploring Research Reactors and Their Use. Accessed: June 5, 2023. [Online]. Available: https://www.iaea.org/newscenter/news/exploring-research-reactors-and-their-use

[1.14] World Nuclear Association: Research Reactors. Accessed: June 5, 2023. [Online]. Available: https://world-nuclear.org/information-library/non-power-nuclear-applications/radioisotopes-research/research-reactors.aspx

[1.15] U.S. Nuclear Regulatory Commission: Backgrounder on Research and Test Reactors. Accessed: June 5, 2023. [Online]. Available: https://www.nrc.gov/reading-rm/doc-collections/fact-sheets/research-reactors-bg.html

[1.16] ILL: Neutrons for Society. Accessed: June 5, 2023. [Online]. Available: https://www.ill.eu/

[1.17] HFIR: High Flux Isotope Reactor. Accessed: June 5, 2023. [Online]. Available: https://neutrons.ornl.gov/hfir

[1.18] HANARO: High Flux Advanced Neutron Application Reactor. Accessed: June 5, 2023. [Online]. Available: http://hanaro.kaeri.re.kr/main.html

[1.19] Britannica, The Editors of Encyclopaedia, "Spallation". Accessed: June 5, 2023. [Online]. Available: https://www.britannica.com/science/spallation

[1.20] G. J. Russell, "Spallation Physics - An Overview", in Proc. Int. Collaboration on Advanced Neutron Sources, KEK, Tsukuba, Oct. 1990.

[1.21] SNS: Spallation Neutron Source. Accessed: June 5, 2023. [Online]. Available: https://neutrons.ornl.gov/sns

[1.22] J-PARC: Japan Proton Accelerator Research Complex. Accessed: June 5, 2023. [Online]. Available: https://j-parc.jp/c/en/

[1.23] ISIS Neutron and Muon Source. Accessed: June 5, 2023. [Online]. Available: https://www.isis.stfc.ac.uk/Pages/About.aspx

[1.24] Los Alamos Neutron Science Center. Accessed: June 5, 2023. [Online]. Available: https://lansce.lanl.gov/

[1.25] J. Finney, "The scientific case for the ESS project". Accessed: June 5, 2023. [Online]. Available: https://www-llb.cea.fr/rapport/essScientificCase-II-1997.pdf

[1.26] The ESS mandate. Accessed: June 5, 2023. [Online]. Available: https://europeanspallationsource.se/ess-mandate

[1.27] The ESS linear accelerator: how it works. Accessed: June 5, 2023. [Online]. Available: https://europeanspallationsource.se/accelerator/how-it-works

[1.28] The ESS target: how it works. Accessed: June 5, 2023. [Online]. Available: https://europeanspallationsource.se/target/how-it-works

[1.29] How do you power the world's most powerful linac? Accessed: June 5, 2023. [Online]. Available: https://europeanspallationsource.se/article/how-do-you-power-worlds-most-powerful-linac

[1.30] Britannica, The Editors of Encyclopaedia, "Klystron". Accessed: June 5, 2023. [Online]. Available: https://www.britannica.com/technology/klystron

[1.31] G. Caryotakis, "The Klystron: A Microwave Source of Surprising Range and Endurance", in Proc. Plasma Physics Conference, Pittsburgh, PA, Nov. 1997.

# 2. Power modulators: state of the art

The aim of this chapter is to present and review the state of the art of the field of power modulators for long pulse high power applications. Generally, a klystron load is assumed throughout this text. In order for this treatment to be meaningful, this chapter begins with a discussion on the general function of power modulators to provide a common frame of reference in subsequent discussions regarding performance in pulsed applications. This introductory section is followed by detailed descriptions of the working principle of prevalent modulator topologies. Their advantages and disadvantages are discussed and relevant existing systems are presented. The chapter is concluded with a comprehensive comparison of available modulator topologies with respect to their merits in prospective long pulse high power applications.

## 2.1 Function and performance of power modulators

Pulsed power modulators are electronic converters drawing power from the electrical grid, shaping it such that it can be usefully absorbed by a pulsed load. Such modulators may be divided into two basic classes based on their principle of operation – line-type semi-controllable modulators and fully controllable modulators. Regardless of modulator type, there are two general main stages to any such conversion - a charging stage and a pulse forming stage [2.1], Figure 2.1. The following sections describe the function and performance characteristics of these two main conversion stages.

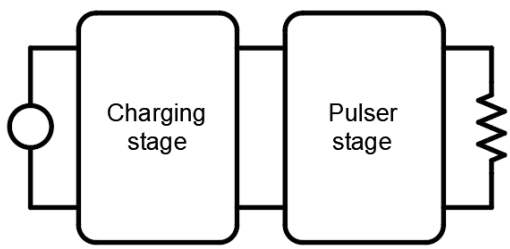



Figure 2.1: Overview of generic pulsed power modulator. The charging stage draws electrical power from the grid and deposits it in an energy storage. The pulse generation stage then delivers the stored energy to the load in the form of a well-defined pulse.

### 2.1.1 Charging stage

The charging stage draws electrical power from the grid and deposits it in an energy storage. In the case of a line-type modulator, it charges an arrangement of one or more transmission lines (or equivalent) in preparation for pulsing. Similarly, in fully controllable modulators the charging stage charges a bank of energy storage capacitors.

In many cases, and in particular in those applications in which system average power is low, the charging stage is comparatively trivial and design efforts are primarily directed towards the pulse generation circuit. However, in long-pulse applications requiring high pulse repetition rate, the resulting system average power may be substantial. Additionally, the impact of the pulsed nature of the modulator load on the electrical grid must be considered. Here, in addition to aspects of, e.g., system cost, volume, and efficiency, design of a pulsed power modulator charging stage crucially must consider several issues related to grid power quality. In particular, contemporary standards, e.g., family IEC 61000, cover limitations on multiple power quality items directly influenced by the charging stage units, among others, e.g., flicker, harmonic distortion and power factor [2.2][2.3]. These power quality items are discussed in the following sections.

*Flicker*

Large power fluctuations impact the voltage at the common point of connection via the voltage drop across the source impedance. Significant variation of the voltage waveform is related to a number of adverse effects, of which one of the most important is termed flicker [2.4]. Power line flicker may be described as visible variations in the intensity of light sources connected to the supply with effects ranging from fatigue and disturbances to photo induced epileptic attacks [2.4][2.5]. Additional issues related to voltage fluctuations in power systems include disturbing sensitive electrical equipment, e.g. computers, and accidental maloperation of relays, contactors, UPS systems, and so on [2.4][2.5]. Flicker is typically caused by loads and systems with a high rate of change of power with respect to the short circuit capacity at the point of common connection, [2.4][2.5][2.6]. Such loads include large welders, electric arc furnaces, and motor systems [2.7][2.8]. Depending on the network to which they are connected, even cranes and elevators are systems that may cause significant voltage fluctuations [2.7][2.8].

For the above noted reasons, standards such as [2.9] and [2.10] describe imposed limitations on voltage changes, voltage fluctuations and flicker in public supply systems. Figure 2.2 is reprinted from [2.9] and shows the allowed relative voltage amplitude variation as a function of the number of load changes per minute due to electronic equipment connected to low voltage public grids. As is seen, for fluctuation frequencies on the order of 10 to 30 Hz, i.e., representing 600 to 1800 changes per minute, the limit curve approaches its minimum at just below 0.3%.

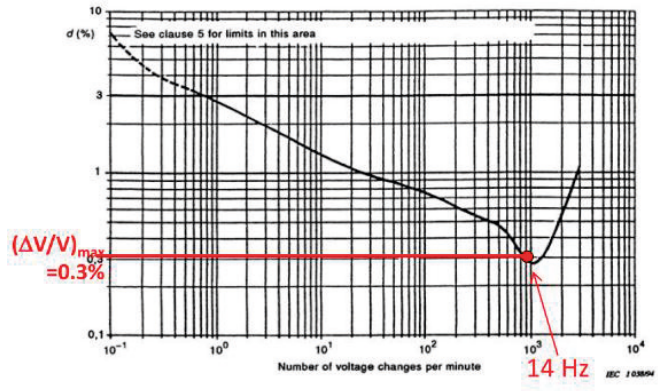



Figure 2.2: Imposed flicker limits according to [2.9]; allowed amount of distortion as function of number of voltage changes per minute. Reprinted from [2.9].

Here, it shall be pointed out that the referenced standard is not directly applicable to accelerator systems. This is mainly because 1) modulator systems are typically not connected to the low voltage public grid, and 2) the type of load that they represent do not entirely correspond to the focus of these standards. However, it is still clear that since accelerator systems utilize high power pulsed converters operating synchronously, i.e., representing extremely large pulsed loads, it is of utmost importance that such loads are adequately decoupled from the electrical grid. Consequently, the above standards provide an appropriate frame of reference and have as a matter of fact been adopted by, e.g., the European Spallation Source [2.11] and the European XFEL facility [2.12]. Here, the ESS Linac pulse repetition rate of 14 Hz corresponds to 840 fluctuations per minute, i.e., representative of the most tightly constrained flicker level prescribed by the standard.

*Harmonic distortion*

Standards impose clear limitations on voltage and current distortion. Typically, limits are imposed both on individual harmonics as well as the total harmonic distortion. Following IEEE 519-2014, [2.13], Table 2.1 presents limits on maximum current distortion.

**Table 2.1: Current distortion limits for systems rated 120 V through 69 kV. Reprinted from [2.13].**

| Maximum harmonic current distortion in percent of $I_L$ | | | | | | |
|---|---|---|---|---|---|---|
| Individual harmonic order (odd harmonics)[a, b] | | | | | | |
| $I_{SC}/I_L$ | $3 \le h < 11$ | $11 \le h < 17$ | $17 \le h < 23$ | $23 \le h < 35$ | $35 \le h \le 50$ | TDD |
| $< 20$[c] | 4.0 | 2.0 | 1.5 | 0.6 | 0.3 | 5.0 |
| $20 < 50$ | 7.0 | 3.5 | 2.5 | 1.0 | 0.5 | 8.0 |
| $50 < 100$ | 10.0 | 4.5 | 4.0 | 1.5 | 0.7 | 12.0 |
| $100 < 1000$ | 12.0 | 5.5 | 5.0 | 2.0 | 1.0 | 15.0 |
| $> 1000$ | 15.0 | 7.0 | 6.0 | 2.5 | 1.4 | 20.0 |

Harmonic propagation is typically limited by use of harmonic filters. Harmonic filters can be either passive, active (active power filters), or a combination of both (hybrid filters) [2.14][2.15][2.16]. If the load contains active rectifier circuits, appropriate converter control may be used in combination with harmonic filters to limit harmonic generation [2.17].

For high power modulators, design of the charging stage clearly must incorporate considerations of harmonic mitigation in order to limit generated harmonics, with direct implications for total system cost, efficiency and volume. For the ESS klystron modulators, the uppermost row applies and total current harmonic distortion at the point of common connection must be limited to below 5%.

*Power factor*

Most solutions to this issue are based on some arrangement of shunt capacitors or reactors for local reactive power generation. Here, static VAR compensators (SVC) utilizing banks of thyristor-switched capacitors or reactors represent a common solution. Alternatively, shunt active power filters as discussed in relation to harmonic mitigation may also be used for reactive power compensation. Finally, loads with active rectifier circuits can typically independently control the input current to be in phase with the supply voltage, eliminating reactive power [2.17].

The design of the charging stage to be used in a high-power modulator must incorporate considerations of reactive power compensation.

### 2.1.2 Pulse forming stage

In the pulse forming stage, the energy stored by the charging stage is released to the modulator load during a relatively short period of time. Figure 2.3 shows a sample (though somewhat exaggerated) modulator output pulse waveform for an application requiring 1 ms long pulses of 100 kV repeated at 50 Hz. As indicated, in contrast to an ideal pulse, a realistic pulse waveform has non-zero rise and fall times, may overshoot, may undershoot, droops overtime, and may have regular and/or irregular flat top variations.

Definitions of the terms indicated in Figure 2.3 vary widely in available research literature. In this thesis, the following definitions are adopted. Subsequent sections discuss the importance of these pulse quality items and justify their definition-

- Useful pulse width is the period of time during which the generated pulse power productively supplies the load. Considering an accelerator klystron load, this time equals $t_c + T_p$, where $t_c$ is the cavity fill time and $T_p$ is the accelerator beam time.
- Pulse flat top amplitude is defined as the maximum value of the pulse during the useful pulse width.
- Pulse rise time, $t_r$, is defined as the period of time required for the pulse waveform to rise from 0% to 99% of the pulse flat top amplitude.
- Pulse overshoot refers to the pulse waveform exceeding the target pulse flat top amplitude following the pulse rise. A given pulse may or may not exhibit overshoot. It is defined as the ratio between the highest value of the pulse waveform and the pulse flat top amplitude. It is usually specified as a percentage value.
- Pulse undershoot may be seen following the pulse event, and is - like pulse overshoot - defined as the peak value of the undershoot versus the flat top amplitude. It is usually specified as a percentage value.
- Pulse stabilization time, $t_s$, refers to the period of time following the pulse rise required for possible overshoot to diminish and for the pulse waveform to settle. This time period is usually not defined mathematically but determined with respect to the pulse shape on a case-to-case basis.
- Flat top droop is a measure of the reduction of the pulse waveform from its flat top amplitude over the usable pulse width. It is defined as the ratio between the reduction and the flat top amplitude, and is usually specified as a percentage value.
- Oscillatory variations through the usable pulse width are termed ripple. Ripple is defined as the peak-to-peak value of the waveform variation. It is usually specified as a ratio with respect to the pulse flat top amplitude.

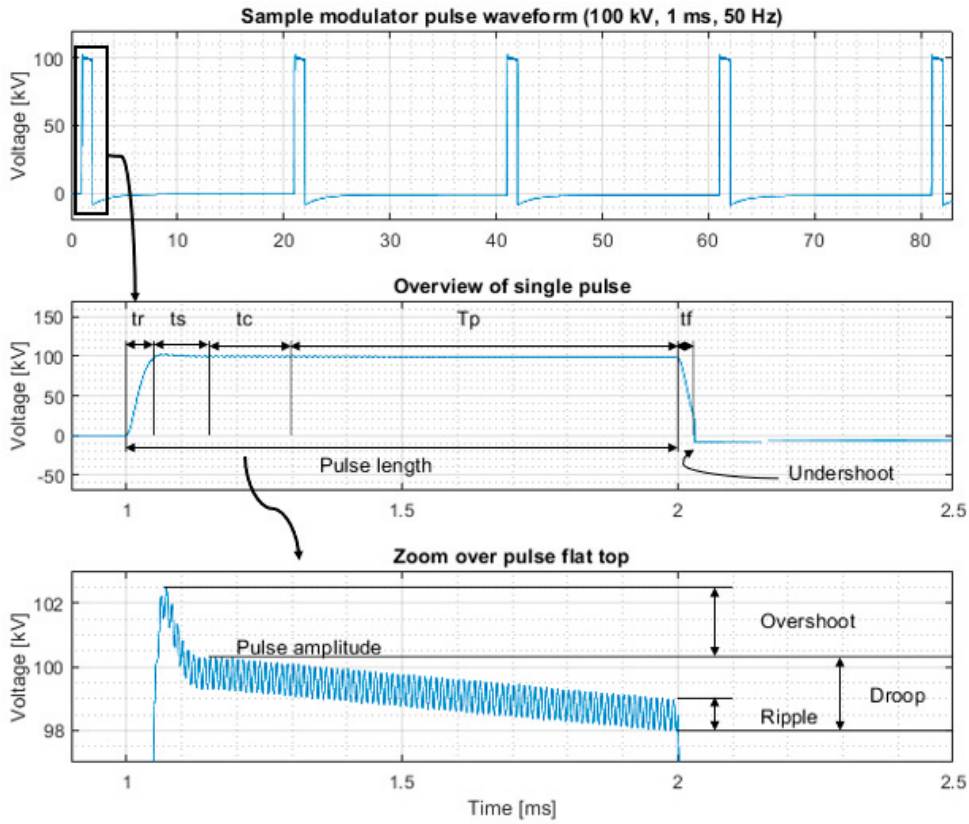



Figure 2.3: Sample modulator pulse waveform. Top) Overview of pulsed modulator operation. Middle) Zoom over one pulse event with definition of important time periods. Bottom) Zoom over pulse flat top with definition of important pulse flat top quantities.

*Useful pulse width*

Typically, the output pulse is only considered useful once it is stable and within a certain range of the pulse flat top amplitude. The permissible flat top ripple and droop levels vary depending on application. For klystron modulators, it is during this period of time that the klystron may be operated. If the voltage is unstable or changing rapidly, LLRF (low-level RF) regulation of the RF pulse is complicated. Hence, for klystron modulators, typical limit values are on the order of 1%, [2.18].

The required useful pulse width is highly application dependent, and ranges between sub-nanosecond to milliseconds. The following sections will demonstrate that, apart from modulator peak power, the useful pulse width is one of the strongest determinants in selecting an appropriate topology for the modulator pulse forming stage.

*Pulse efficiency*

In available literature, modulator efficiency is almost without exception implicitly synonymous with electrical efficiency. However, in order to be able to make comparisons between modulator topologies, and in particular when discussing high power modulators, it is extremely important to consider also what may be termed 'pulse efficiency' [2.19]-

As noted in the previous section, the generated pulse waveform is only considered useful once stable and while within a certain range of the pulse flat top amplitude. From this perspective, the power expended during the pulse rise time, pulse stabilization time, and - in the case of klystron modulators - cavity fill time, are effectively considered losses. This is an important consideration as both the pulse shape and the pulse rise time are directly connected to the chosen modulator topology and its implementation. Consequently, two modulator systems could have identical electrical efficiency but still represent very different overall system efficiency. Again, in discussing high power modulators used in, e.g., spallation sources with electrical bills on the order of tens of millions of Euros per year, these considerations are naturally of great importance [2.19][2.20][2.21].

From the above, pulse efficiency may be defined as the ratio of the average pulse flat top power versus the full average pulse power, (2.1). The overall system efficiency is then given by the product of the pulse efficiency and the modulator electrical efficiency, (2.2), [2.19].

$$\eta_p = \frac{PT_p}{P\left(T_p + kt_r + t_s + t_c\right)} \tag{2.1}$$

$$\eta = \eta_p \eta_m \tag{2.2}$$

Here, $P$ is the modulator peak power. In the case of klystron modulators, it is given by $P = V_k I_k$, where $V_k$ is the applied cathode voltage (i.e., modulator output voltage), and $I_k$ is the corresponding cathode current (i.e., modulator output current). The constant $k$ represents the fact that not the full peak power is being generated during the pulse rise. This is discussed further in the following section.

*Pulse rise time*

In available literature on pulsed power modulators, several definitions of pulse rise time exist. The most common definition of rise time is the length of time corresponding to the leading edge of the pulse rising from 10% to 90% of the pulse flat top amplitude. Other similar definitions include the 0-99% rise time and the 0-100% rise time. As implied in the preceding section, the pulse shape and pulse rise time can have significant effects on system efficiency. Thus, in order to be able to

reliably compare system concepts, a coherent definition of rise time is needed. Consider for example the situation depicted in Figure 2.4. Shown in blue is a step response of a first order system. As will be seen in a later chapter, long pulse klystron modulators utilizing pulse transformers are very well represented by first order LR circuits [2.22]. The step response of a second order system, a good representation of among others the so-called Stacked Multi-Level (SML) topology, is shown in orange.

Figure 2.4.a indicates the rise time of both systems according to the 10-90% definition. According to this definition, the rise time of the two waveforms differ by approximately 10 µs. On the other hand, using the 0-99% definition as depicted by Figure 2.4.b, the rise time differs by as much as 30 µs.

This difference is further aggravated if the second order system is controllable, which is the case with, e.g., the SML modulator topology. In this case, it is possible to request a greater step in the beginning and then lower it as the pulse waveform approaches its target flat top amplitude. Figure 2.5 depicts this situation. Here, the yellow trace represents exactly the same system as the orange trace, but with the above-described simple control mechanism implemented. Now, the difference in pulse rise time between the second order system and the first order system is more than 50%.

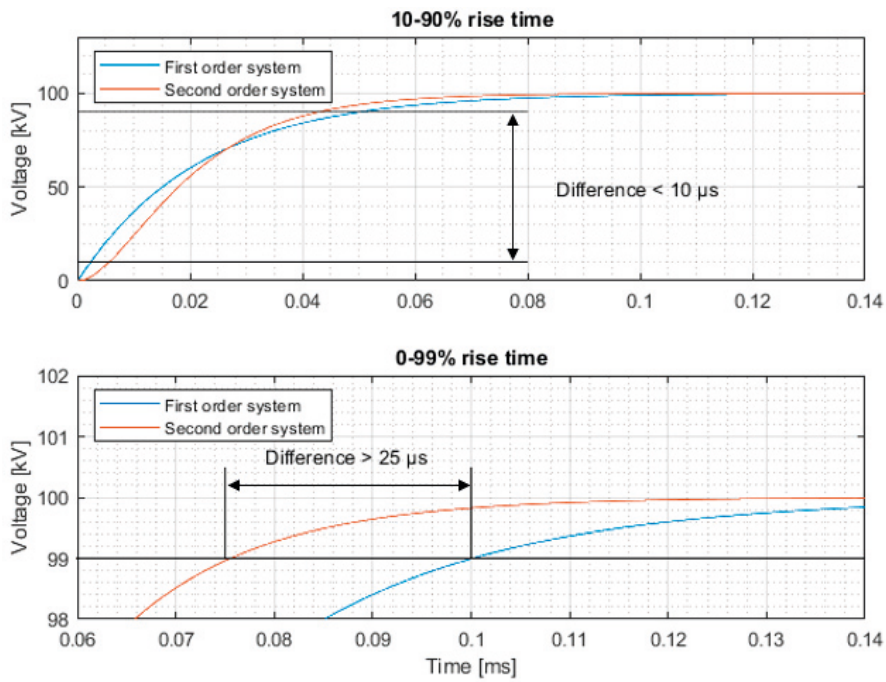



Figure 2.4: Difference between first and second order systems with respect to the definition of pulse rise time

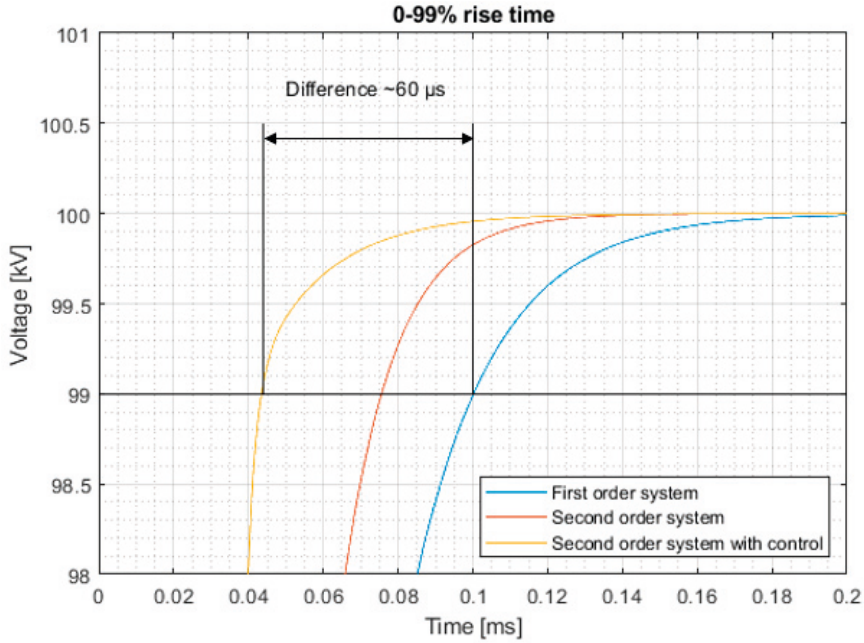



Figure 2.5: Impact of controllability on pulse rise time

Furthermore, it should be noted that the shown pulse waveforms have different shapes. This is important, as it connects directly to the expended power during the pulse rise. This is captured by the constant $k$ in (2.1). As it happens, this further favors the faster second order system in terms of pulse efficiency [2.19].

In this work, the 0-99% pulse rise time definition has been adopted namely because 1) the pulse waveform is only considered useful close to its intended flat top amplitude, i.e., typically within 1%, and because 2) its capacity to better resolve the discrepancies pertaining to pulse efficiency with respect to differences in pulse rise time and pulse shape. These differences should be kept in mind in the following literature review and discussions on available modulator systems.

*Pulse overshoot and stabilization time*

As indicated in Figure 2.3, the pulse waveform output by a modulator system may contain an overshoot. Generally, this stems from higher order effects. In pulse transformer-based modulators, for example, the stray capacitance of the high voltage windings may contribute sufficiently such that the pulse transformer and the load form an equivalent second order RLC circuit. Similarly, the SML topology is well represented by a second order system and therefore, depending on the applied control methodology, may exhibit an overshoot in response to a pulse request. It shall be pointed out that these effects are not detrimental in and of themselves. Actually, the added dynamic typically speeds up the step response and thus shorten

the pulse rise time. However, there is usually an upper limit on pulse overshoot dictated by the application or the high voltage insulation. In klystron modulators, for example, the upper limit is usually given by the peak voltage rating of the klystron. Thus, the maximum overshoot is in practice limited to a few percent above that of the target flat top amplitude. In addition, since the pulse is not useful during the overshoot, an added stabilization time is required to ensure that the pulse overshoot has diminished. Clearly, this added time must be weighed against the benefits of the shortened pulse rise time.

*Flat top ripple*

Depending on modulator topology and in-use auxiliary systems, oscillations may be present in the pulse flat top. In accelerator systems, oscillations in the pulse flat top directly impact the quality of the generated beam [2.23][2.24]. It is therefore of great importance that any such oscillations are both reproducible and limited to such an extent that they may readily be compensated for by the low-level RF system. A typical flat top ripple specification could be on the order of 1%. In the case of the European Spallation Source klystron modulators, the peak-to-peak flat top ripple must be limited to be below 0.15% of the flat top amplitude.

*Pulse undershoot*

Depending on modulator implementation, the pulse waveform may have a negative voltage swing following termination of the pulse event. Particularly, this type of undershoot is common when utilizing pulse transformers [2.25]. Here, following the end of the pulse, the transformer core must be demagnetized, i.e., a negative voltage is enforced which is transformed and thus experienced by the klystron load. Klystrons, given their diode-like characteristics are especially susceptible to this and may be damaged unless the amplitude of the swing is limited [2.25].

*Pulse to pulse repeatability*

As the modulator output pulse power quality directly affects the quality of the generated accelerator beam, pulse waveform repeatability is extremely important [2.26]. Furthermore, generated flat top ripple compensation by external control loops is greatly facilitated by pulse repeatability.

## 2.2 Line type semi-controllable modulators

In line type modulators, the load is connected to an arrangement of one or more pre-charged transmission lines or lumped LC networks [2.27]-

Modulators using transmission lines are called pulse forming lines (PFL). Here, a high voltage power supply charges the transmission line(s) prior to pulsing. By

switching the end of (one of) the transmission line(s), a traveling wave is generated which propagates the length of the transmission line(s). By carefully matching the impedance of the transmission line(s) to the impedance of the load, a well-defined pulse waveform is generated across the load. Such modulators feature excellent pulse quality and are generally inexpensive and comparatively simple to design and manufacture [2.27][2.28]. Since this type of modulator is based on the traversal of electromagnetic waves along the length of transmission lines, the attainable pulse length is given and directly limited by the length of the system [2.27][2.28]. For these reasons it is typically the technology of choice for applications requiring high peak power and very short pulse lengths [2.27]. This includes, among others, X-ray generation, plasma generation, breakdown testing, lasers, ion implantation and certain biomedical applications [2.29].

However, due to their nature, such modulators quickly become impractical trying to extend the pulse length beyond that of a few microseconds. Pulse forming networks (PFN) are an attempt to utilize lumped LC networks approximating the function of transmission lines to facilitate generation of longer pulses [2.30]. Using this technique, it is possible to adapt the ideas of PFL modulators to applications requiring high voltage and long pulse length. Still, in considering multi-millisecond applications with average powers of hundreds of kilowatts, the required ladder components become very bulky. In addition to the added volume, large geometries exhibit parasitic effects to a greater degree. This affects the characteristics of the lumped network and impairs the transmission line equivalence, directly contributing to degradation of the pulse waveform in terms of added pulse overshoot and flat top ripple [2.1].

Given that the topic of this doctoral dissertation pertains to long pulse applications orders of magnitude beyond that of the intended application range of line type modulators, this family of modulators will mostly be disregarded throughout the remainder of this work. For the sake of completeness, however, general descriptions of the most common line type modulators and their features are provided below.

### 2.2.1 Transmission line pulser

The simplest line type modulator is shown in Figure 2.6. Here, a high voltage source is connected to the load via a length of transmission line in series with a high voltage switch $S_P$. The impedance of the load is matched to the impedance of the transmission line, $Z_L = Z_0$.

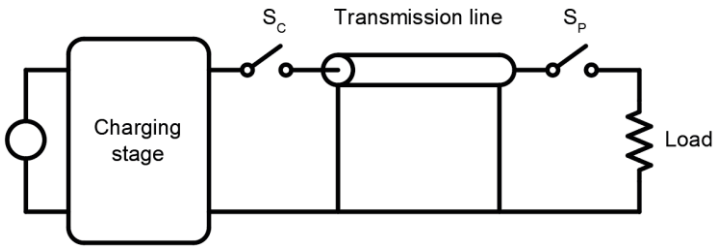



Figure 2.6: Simple transmission line modulator

Modulator operation may be described as follows-

- First, the switch $S_P$ is left open and the transmission line is charged to a voltage $V$ by the charging stage through the switch $S_C$. The charger is then disconnected. If the application average power is low, this function is usually implemented by replacing $S_C$ by a resistor with high ohmic value with respect to the characteristic impedance of the transmission line.
- Pulse generation is initiated by closing the switch $S_P$.When $S_P$ is closed, a voltage $V/2$ appears across the load. This represents a negative voltage step with respect to the transmission line, generating a traveling wave propagating from the load side towards the source side with propagation velocity $v$. Upon arrival at the source side, the traveling wave experiences an open circuit (i.e., either an open switch $S_C$ or a high value series resistor) and is reflected back towards the load. Throughout this series of events, the load voltage is fixed at $V/2$. Thus, if the length of the transmission line is denoted $l$, the obtained effective pulse length is given by $T_P = 2l/v$.
- Following the pulse event, the transmission line is completely discharged and the procedure may be repeated.

This type of generator is inexpensive and simple to design, manufacture and operate [2.31]. However, the generated pulse voltage amplitude is only half the source voltage $V$. The charging stage must therefore be able to operate at voltage levels twice that of the intended load voltage. This is clearly a serious drawback in considering high voltage applications. Furthermore, in this circuit the high voltage switch has to be placed on the load side for proper operation. This means that 1) the switch has to be rated for twice the load voltage, and that 2) the switch cannot be grounded, requiring complex drive circuitry.

### 2.2.2 Blumlein modulator

The above-described difficulties were addressed by Alan Blumlein in 1937 through his invention of the circuit now called the ‘Blumlein generator’ or the ‘Blumlein transmission line’ [2.32]. In this circuit, the load is connected in between two

transmission lines of equal length, Figure 2.7. One transmission line is connected to the high voltage switch, now placed on the source side, whereas the other is open circuited at the other end. The impedance of the load is matched to twice the impedance of the transmission lines, $Z_L = 2Z_0$.

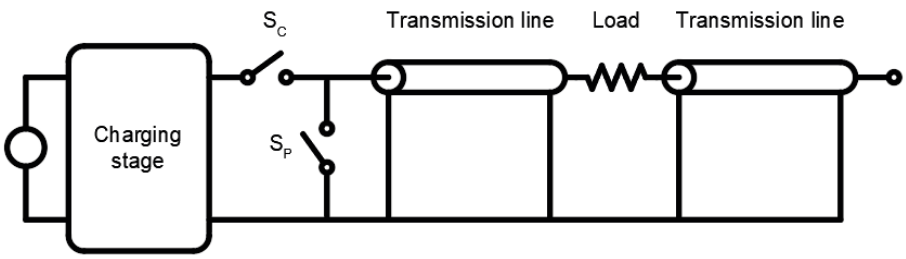



Figure 2.7: Blumlein generator

Modulator operation may be described as follows-

- First, the switch $S_P$. is left open and the transmission lines are charged to a voltage $V$ by the charging stage through the switch $S_C$. Note that the outer transmission line is charged via the load. The charger is then disconnected. As for the transmission line pulser, if the application average power is low $S_C$ is replaced by series resistor.
- Pulse generation is initiated by closing the switch $S_P$. When $S_P$ is closed, the left side of the left transmission line experiences a negative voltage step $V$, generating a traveling wave propagating from towards the load with propagation velocity $v$. Until the wave arrives at the load, the load voltage is zero.
- Upon arrival at the load, the above-described impedance matching results in the traveling wave being half-transmitted and half-reflected. The reflected wave propagates back towards the source side with amplitude $-V/2$. The transmitted wave propagates towards the open end of the right transmission line with amplitude $+V/2$. The voltage difference $V$ is seen across the load. Since the two transmission lines have equal length, both waves reach the end of their respective transmission line at the same time, where they experience an open circuit and are reflected back towards the load. Again, if the length of the transmission lines is denoted $l$, the obtained effective pulse length is given by $T_P = 2l/v$.
- Following the pulse event, the transmission lines are completely discharged and the procedure may be repeated.

Similar to the transmission line pulser, the Blumlein generator is also relatively cheap and generally simple to design, manufacture and operate [2.33]. In addition to this, the above description highlights that 1) the obtained pulse voltage amplitude is the entire charging voltage V, simplifying the charging circuit and the modulator switches; and that 2) the high voltage switch is placed on the source side, allowing it to be grounded.

The above descriptions demonstrate that the relationship $T_P = 2l/v$, where the propagation velocity $v$ is on the order of the speed of light, fundamentally limits the attainable pulse length for PFL type modulators. As an example, the geometry and material properties of most coaxial cables more precisely correspond to a propagation velocity around 2/3 of the speed of light. Thus, the attainable pulse length is approximated by $T_p = 1/(c/3) = \sim l/10^8$, or $l = T_p 10^8$. In effect, if a pulse length of 1 µs is desirable, this corresponds to a 100 m coaxial transmission line rated for high voltage and high power. Here, it should be noted that the required application pulse length of the ESS klystron modulators is on the order of 3500 µs, directly impacting the required length. It is for these reasons that PFL type modulators are completely impractical in long pulse applications.

### 2.2.3 Pulse forming network

As noted, artificial transmission lines may be formed by interconnection of inductors and capacitors in lumped networks, Figure 2.8. Pulse generators based on this idea are called pulse forming networks (PFN). A number of circuits have been devised for this purpose, each with its own advantages and disadvantages. These circuits are usually denoted the Rayleigh line, Figure 2.8, as well as the Guillemin circuit types A through F, Figure 2.10.

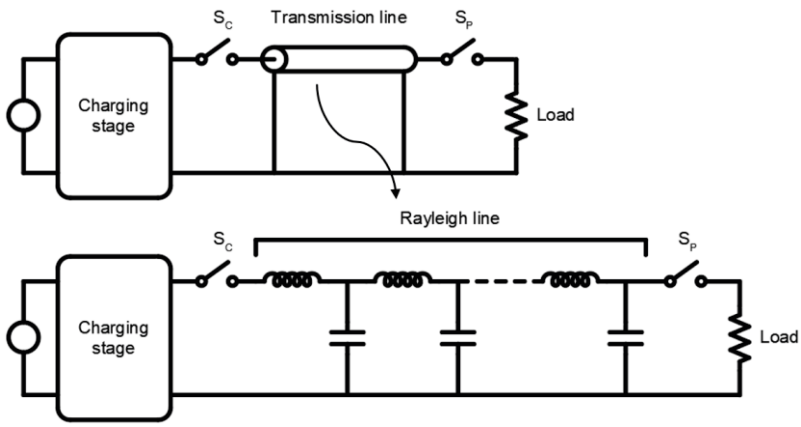



Figure 2.8: Transmission line replaced by Rayleigh line, an artificial transmission line based on a network of inductors and capacitors.

The Rayleigh line is the simplest pulse forming network, consisting of an LC ladder network with identical sections, Figure 2.8. In this case, the LC sections are designed according to equations (2.3)-(2.4), [2.34]. Here, $Z_0$ is the equivalent characteristic impedance and $N$ is the number of ladder network sections. Matching the load impedance to the characteristic impedance of the Rayleigh line, an approximation of the transmission line pulser is obtained and a rectangular pulse may be generated provided that the number of ladder network sections is large, [2.34].

$$L_0 = \frac{Z_0 T_p}{2N} \tag{2.3}$$

$$C_0 = \frac{T_p}{2NZ_0} \tag{2.4}$$

Figure 2.9 shows simulation results derived from the Rayleigh line circuit shown in Figure 2.8. Here, the Rayleigh line has been designed according to (2.3)-(2.4) for a characteristic impedance of 100 ohm and a desired pulse length of 10 µs. The number of Rayleigh line sections is shown as a parameter. As an example, the network with 5 sections corresponds to circuit values $L_0 = 100\ \mu F$ and $C_0 = 10\ nF$.

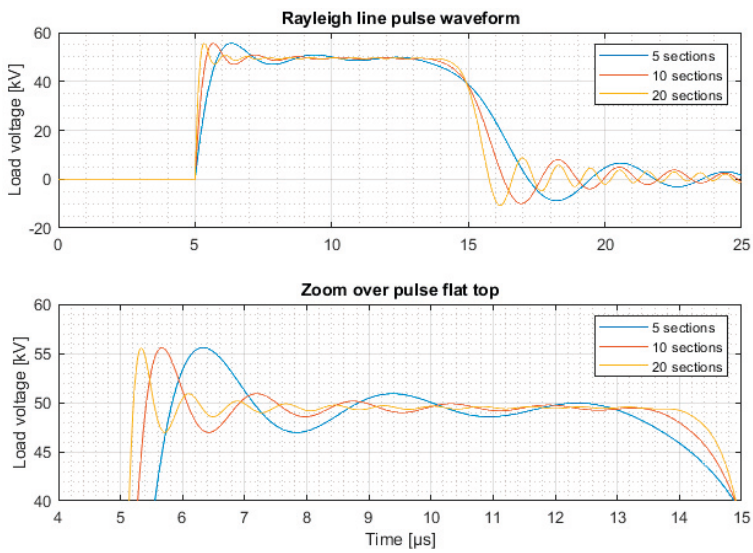



Figure 2.9: Simulation of circuit shown in Figure 2.8 with the number of ladder sections as parameter. The characteristic impedance is 100 ohm and the desired pulse length is 10 µs. The charging stage charges the Rayleigh line to 100 kV.

The above noted ladder network parameters and associated simulation results demonstrate that PFN circuits clearly are a viable solution extending the functionality of PFL based modulators to longer application pulse lengths. As a matter of fact, pulses of arbitrary pulse length may in principle be generated with PFN based circuits. However, it is also seen that the pulse quality is nowhere near that of equivalent PFL modulators unless the number of sections is very high.

Figure 2.9.b shows a zoom of the pulse flat tops. As can be seen, even with 20 sections the ladder network is seen to feature a ~10% pulse overshoot, 20% negative pulse undershoot and a flat top ripple of ~1%. On the other hand, Figure 2.9 also shows that this type of circuit has excellent pulse rise time on the order of 1%. Although desirable for reasons of pulse efficiency, this standard of pulse rise time is generally not needed for most power modulators, and a slower pulse rise time would be acceptable-

In his work, Guillemin discovered that the resulting pulse overshoot and flat top ripple associated with Rayleigh line networks were directly related to the implicit attempt to approximate the rectangular pulse generated using transmission lines [2.35]. He further showed that if, e.g., a trapezoidal pulse would be acceptable, significantly better pulse quality could be obtained with fewer ladder sections [2.35. This work resulted in six distinct circuit types commonly termed types A to F, [2.36], Figure 2.10. Out of these, types A, B, C, and F require differently valued capacitance values for each network section. For high voltage pulse generators with a large number of PFN sections, these options are rarely cost effective or practical. Circuit type D is a mathematical construct allowing the section capacitance values to be equal. However, this is made possible by placing negative inductance values in series with each capacitor, and is therefore impossible to realize physically. Finally, type E represents a practical equivalent of the type D circuit by use of mutually coupled inductors. In practice, the required coupled inductor circuit is usually implemented by winding the inductor coils on a single tube and adjusting their spacing in accordance with the mutual inductance requirement [2.37]. The mathematical details as well as suitable design procedures of Guillemin circuits are thoroughly discussed in [2.38].

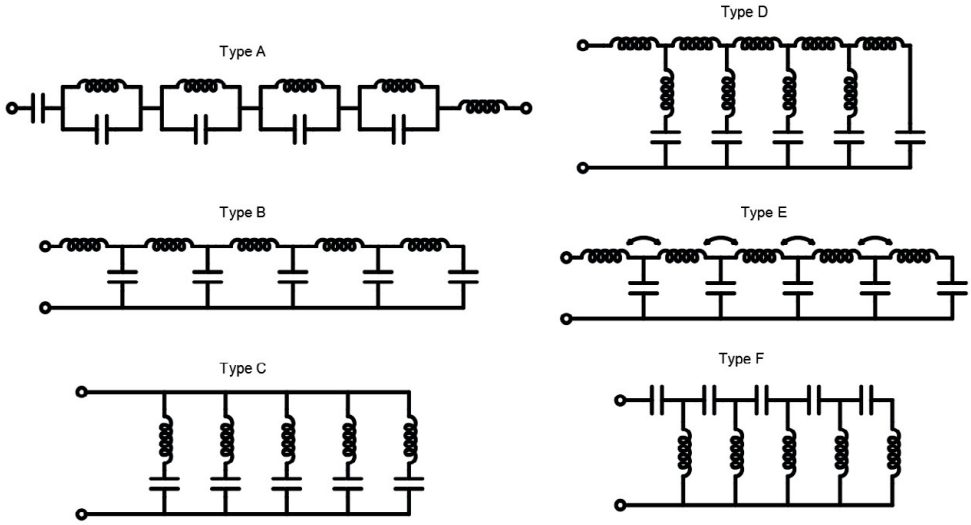



Figure 2.10: Overview of Guillemin circuits type A-F with 5 sections.

*Examples of modulators based on pulse forming networks*

As part of the literature review, a number of existing modulators and interesting projects based on PFN circuits were identified.

- [2.39] describes a PFN type modulator for 520 MW pulsed klystrons with 14 μs pulse length (usable pulse width ~10 μs) repeated at 50 Hz. The average power is 350 kW, and the generated pulse voltage is on the order of 600 kV. The pulse flatness is kept within +/- 0.5%. This modulator is based on parallel connection of 4 identical 20 section air insulated Rayleigh lines. Here, each Rayleigh line inductor is tunable to allow pulse shaping.
- [2.40] outlines the development of a PFN type modulator for 46 MW pulsed klystrons intended for the earlier planned Superconducting Super Collider (SSC). Here, the pulse length is 75 μs (usable pulse width ~60 μs), and pulses are repeated at 10 Hz. The average power is on the order of 35 kW, and the pulse output voltage is 230 kV. This modulator is based on a 20-section air insulated Rayleigh line. As in [ness1], the inductors are tunable to provide a pulse flatness within that of +/- 0.25%.
- [2.40] also describes another 8 MW PFN type modulator for SSC with a pulse length of 105 μs (usable pulse width ~90 μs) repeated at 10 Hz. Similar to the above project, this modulator is based on a single 20 section Rayleigh line with tunable inductors.

These modulator systems demonstrate that the PFN technique is versatile and may be utilized to develop modulator systems providing high quality pulses of extremely

high peak power (> 500 MW), high average power (hundreds of kilowatts), and longer pulse lengths (on the order of 100 μs); though likely not all at the same time.

However, while interesting, these systems also establish that the use of PFN technology in implementing modulator specifications comparable to that of ESS requirements is unfeasible. For example, the 8 MW modulator outlined in [2.40] produces a pulse amplitude of 125 kV and 64 A, not very unlike that of ESS modulator requirements. On the other hand, the pulse length is limited to ~100 μs and the average power is only 8.4 kW. Extending the pulse length by a factor of ~35 and the average power by a factor of ~80 for the admittedly already quite spacious system would require additional and much larger Rayleigh lines. The larger components would magnify parasitic effects, distorting the pulse waveform. This further complicates the situation as the pulse flat top quality requirements are here significantly more stringent than the above +/- 0.25%, thus requiring additional Rayleigh sections and highly tunable inductors. Here, individual component tuning is undesirable due to the large modulator count and thus number of components.

Finally, it is noted that no Guillemin type circuits were found in modulators for long pulse nor high average power applications. In addition to the aforementioned issues, this is likely due to difficulties in assembling an appropriate mutual inductance circuit given the high average power. In this case, the usual method of winding the inductor coils on a single form seems highly undesirable. Furthermore, stray capacitance between inductor windings would be exceedingly difficult to counteract, in part because the stray effects would be widely different for each Guillemin section.

## 2.3 Fully controllable modulators

In fully controllable modulators, the energy storage - invariably a large capacitor bank - is applied to the load by some arrangement of switches. In contrast to line type modulators, such pulse generators only discharge a portion of the stored energy in pulsing and thereby require a fully controllable switch that can open while conducting the full load current [2.1]. Historically, such switches were typically implemented by a ‘hard’ high-vacuum tube fitted with a control grid, hence the term ‘hard tube modulator’ [2.1]. Today, fast solid-state switches are replacing vacuum tubes, enhancing modulator performance, efficiency, controllability, reliability and cost while enabling entirely new modulator topologies to emerge.

Whereas in line type modulators the pulse length is determined and fixed by the length of transmission lines (or their equivalent), in hard tube modulators the attainable pulse length essentially corresponds to the period of time during which the discharging energy storage is able to maintain sufficient voltage across the load. Assuming constant load power, this period of time is well approximated by equation

(2.5), [2.41], where $T_p$ is the pulse length, $C$ is the capacitance of the energy storage, $p$ expresses the allowable flat top droop in percent of the pulse flat top amplitude, $V$ is the initial capacitor bank voltage, and $P_k$ is the klystron load power.

$$T_p \leq \frac{CpV^2}{P_k} \tag{2.5}$$

In some cases, these considerations result in a simple modulator design in which the storage capacitor is sized according to (2.5) and the switch is chosen or manufactured to simply withstand the load voltage and pulse power requirements. However, (2.5) reveals that, especially for long pulse high power applications with stringent flat top requirements, an extremely large storage capacitor could be necessary. As an example, consider the ESS klystron modulator application with $P_k = 11.5\,MW$, $T_p = 3.5\,ms$ and with a flat top stability requirement of $p \leq 0.15\%$. For a capacitor bank voltage of 1 kV, adopted for the ESS modulators to allow use of standardized off-the-shelf semiconductor devices, the required capacitor bank capacitance would be on the order of 50 F. This is obviously unfeasible, and almost invariably some sort of droop compensation mechanism is implemented in trade-off with the modulator capacitor bank. Selection and implementation of an appropriate droop compensator is one of the most important considerations in developing hard tube modulators, for which reason several such compensation techniques will be evaluated as part of this thesis.

As will be seen, the choice of a suitable hard tube modulator topology in combination with a suitable droop compensation mechanism makes possible high power pulse generation for a wide range of pulse lengths. Note also that their use of fully controllable switches provides great flexibility in terms of the pulse length - virtually any pulse length between zero and that given by (2.5) may be arbitrarily generated as desired by opening the switch at the appropriate time. Short pulse generation is generally limited by the intrinsic inductance of the switch(es) and the circuit layout. For this reason, line type modulators are oftentimes (though not always) a more appropriate choice for generation of very short pulses.

In the sections that follow, the working principle and state of the art of four hard tube modulator topologies (families) will be reviewed- 1) the hard switch topology; 2) the pulse transformer-based topology; 3) the Marx generator topology; and 4) topologies based on resonant converters.

### 2.3.1 Hard switch topology

The hard switch topology is sometimes also referred to as the single switch topology and the direct switch topology. It is the simplest solid-state modulator topology, consisting only of a single switch providing a hard connection between the storage capacitor and the load, Figure 2.11. Here, the switch is operated in a manner analogous to turning on and off a lamp. By closing the switch, the storage capacitor voltage is directly applied to the load. The load is disconnected by opening the switch. Pulsed power may thus be generated by repeatedly opening and closing the switch in this manner.

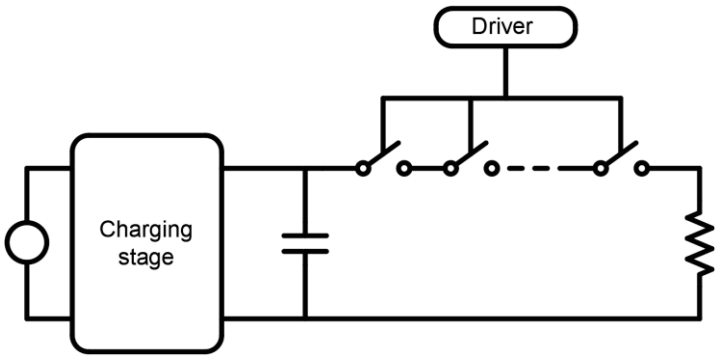



Figure 2.11: Hard switch topology. A single switch, typically formed by series connecting a large number of fully controllable semiconductor switches, directly connects the load to the energy storage. Pulsed power is generated by repeatedly opening and closing the switch.

The main advantages of this modulator topology are its operational and topological simplicity and directness. In addition, the stored energy is kept to a minimum (with respect to other hard tube pulsers), and as the pulse waveform rise time is mainly determined by the equivalent series parameters of the hard switch comparatively fast and efficient pulses may be expected, [2.42]. The disadvantages of this modulator topology, and especially in application to long pulse high power problems, however also lie in the implied simplicity of a single switch providing direct connection between energy storage and load-

First, as the storage capacitor directly imposes the load voltage, this implies the need of a high voltage high power capacitor charger. Furthermore, it is clear that the solid-state switch must be rated for the entire load voltage (typically in the range of tens to hundreds of kilovolts) and also be able to handle the full peak and average load power requirements. Using semiconductor technology, this invariably requires series connection of a large number of switches forming a stack, Figure 2.11. Design and operation of such a switch is not trivial, requiring very accurate and precise timing while presupposing very careful circuit layout [2.43].

In addition to the above, switch redundancy is usually necessary as if a single switch in the stack fails and is bypassed, stress is increased across the remaining switches. Furthermore, switch control electronics cannot be grounded, thus complicating drive circuitry and design. Finally, the entire solid-state stack typically needs to be submerged in oil, severely affecting maintenance and repair times.

*Examples of modulators based on the hard switch topology*

For hard switch modulators, the obtainable pulse power and pulse length is in principle only limited by the storage capacitance and the power handling capability of the hard switch. However, as pointed out in [2.43], achieving a mechanical design ensuring long term switch reliability while minimizing stray capacitive effects (distorting the pulse waveform) and losses is highly challenging. For these reasons, use of the hard switch modulator topology in high power and, especially, long pulse applications is limited. In the literature review, three existing notable exceptions were found-

- [2.44] describes a 125 MW (500 kV, 265 A) power modulator with 3.2 μs long pulses repeated at 180 Hz intended for the earlier proposed Next Generation Linear Collider (NLC). It was found that good pulse shape was obtained with an efficiency exceeding 90%. However, details regarding pulse rise time, fall time or pulse flat top performance were never reported. Interestingly, out of three modulator topologies considered (the other two being a pulse transformer-based modulator and a Marx based modulator) for this application, the implementation based on the hard switch topology was determined to be the most complex despite its topological simplicity.

- [2.45] outlines a 4.95 MW (110 kV, 45 A) power modulator with a pulse length of up to 2.0 ms repeated at 50 Hz for the ISIS front end test stand. This is an interesting case as the peak pulse power, voltage level, and required pulse length are somewhat similar to that required by the ESS application (115 kV, 100 A, 3.5 ms). However, in considering a similar hard switch modulator for ESS requirements the following issues may be raised-

  - The resulting droop is here on the order of 5%. Correcting this to 0.15% would require a significant bouncer circuit. As will be seen later in this thesis, bouncer circuit design for long pulse high power applications is not trivial. A somewhat comparable bouncer circuit is discussed in relation to the following modulator system example [2.46].

- The solid-state switch is complex, requiring series connection of 10 IGBTs. The peak power of the ESS modulators is more than twice as high, likely requiring a switch upgrade.
- While this is a long pulse modulator, the ESS modulators require a 75% longer pulse length. At a pulse repetition rate of 14 Hz, this furthermore corresponds to an increase in modulator average power of more than 30%.
- The capacitor bank energy storage as well as the complete pulse generation stage must be fitted in large oil tanks.

- [2.46] discusses a 22 MW (135 kV, 165 A) power modulator with a 1.5 ms pulse length for the International Linear Collider (ILC). This impressive modulator system is also rated according to somewhat similar specifications to that of the ESS application. Again, several concerns may be raised in considering a similar hard switch modulator for ESS requirements-

  - The required average input power of the ESS modulators is more than three times higher than that shown in [2.45]. High power capacitor charger systems are typically procured off-the-shelf, and the corresponding ESS charging system may therefore be expected to be around three times larger.
  - The ESS pulse energy is around 20% greater than that seen in [2.45]. In addition, as the pulse voltage of the ESS application is somewhat less, the main capacitor bank volume may be expected to be between 20-50% larger.
  - Given the noted pulse energy, the resulting droop must be compensated with a bouncer circuit. The ESS has significantly more stringent pulse flat top stability requirements (0.15% peak-to-peak versus +/- 0.5%) and furthermore operates at a higher pulse repetition rate (14 Hz versus 5 Hz). Consequently, the resulting bouncer circuit will be even more spacious and expensive than shown in [2.45].
  - Finally, the reliability of the hard switch assembly has not been reported.

It is worth pointing out that the authors of [2.44]-[2.46] in their later work related to the ESS application decided on a pulse transformer-based approach (to be discussed in the following section) in favour of the hard switch topology. For the above reasons, the hard switch topology will not be further considered in this thesis.

### 2.3.2 Pulse transformer-based topology

This topology may be considered to be a direct extension of the hard switch topology. Comparing Figure 2.11 and Figure 2.12, it is seen that a step-up transformer has been inserted between the switch and the load in recognition of the complexities in designing and manufacturing the required hard switch topology components for certain applications. For this reason, this topology is sometimes called the hybrid modulator topology (i.e., a hybrid including a hard switch and a pulse transformer). By inclusion of a pulse transformer, one or a few suitable off-the-shelf low voltage switches may be series connected in straightforward fashion to form the switch assembly. Thus, as - in principle - everything else remains the same, this topology retains the topological simplicity of the hard switch modulator topology while immensely simplifying switch design. This is the greatest benefit of the pulse transformer-based topology.

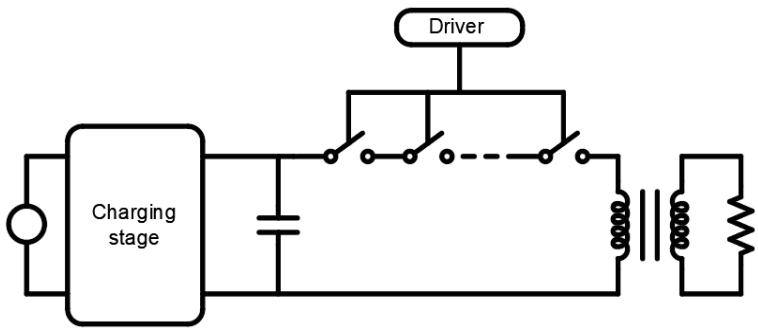



Figure 2.12: Pulse transformer-based topology.

However, in high power applications, there are a number of disadvantages and issues that must be considered. All of these areas will be extensively treated in a later chapter-

*Pulse transformer design*

Depending on application, the design of the pulse transformer component may be non-trivial. Design aspects such as system volume, efficiency, impact on pulse quality, reliability, manufacturability and so on have to be appropriately balanced. Here, little conclusive data exists on key components and material performance, especially under low frequency pulsed excitation. In [2.22], it was shown that pulse transformers for certain long pulse high power applications may be required to be, e.g., above 2 meters tall and weigh on the order of 10000 kg to satisfy modulator pulse power requirements. Such limitations significantly impact manufacturability and maintainability of modulator systems.

*Parasitic elements*

Addition of the pulse transformer furthermore adds loop inductance and parasitic capacitive elements between the transformer windings and from transformer windings to the system (oil tank) enclosure, deteriorating pulse quality, [2.47]-[2.50]. In addition, it has been shown in, e.g., that pulse transformers via their inherent stray capacitance may form non-negligible common mode current paths, impacting line side quantities. These issues also have to be considered in system design. Finally, it should also be noted that the leakage and magnetizing inductances of the transformer represent additional stored energy that has to be released in case of an arc event.

*Auxiliary systems*

During the pulse event, the energy storage is applied to the primary winding(s) of the pulse transformer and the transformer core is thereby positively magnetized. Here, it must be ensured that the transformer core magnetization is restored (demagnetization) prior to the following pulse event or the flux will build up with each pulse and over time saturate the magnetic core. For long pulse high power applications, such systems are in general quite difficult to implement given the relationship between the maximum demagnetization period, linked to the pulse repetition rate of the modulator, and the maximum allowable reverse voltage imposed by the klystron load.

Practical demagnetization systems often work by dissipating the stored magnetic energy in a resistive element [2.25]. Such systems have the advantage of being relatively easy to design and implement while requiring only passive components thus eliminating issues of control. However, the stored magnetic energy can be significant and may therefore represent a prohibitive reduction in efficiency.

Then, given the aforementioned size associated with pulse transformers intended for long-pulse applications, it is often desirable to also include an auxiliary core flux bias system. Negatively biasing the transformer flux in principle allows doubling the transformer core flux swing for a given core area, granting the possibility to significantly reduce the transformer volume [2.51]-[2.52]. Commonly, a tertiary winding is added to the pulse transformer and connected to a low voltage dc power supply. The power supply generates a current which with proper winding design negatively biases the transformer core in preparation for pulsing.

Transformer demagnetization and flux biasing may also be obtained using active components. A ‘lossless reset circuit’ was introduced in [2.53]. Here, a capacitor is used to capture the stored magnetic energy following the pulse event. This energy is then fed back in the opposite direction to negatively bias the transformer, recycling the energy. However, it shall be pointed out that such a system requires an additional pre-charge system and increases system complexity [2.53].

*Examples of modulators based on the pulse transformer-based topology*

Many high-power modulators are based on the hybrid topology. Several noteworthy cases were found as part of the literature review-

- [2.54] describes a 125 MW (500 kV, 265 A) power modulator with up to 5 μs long pulses to be repeated at 180 Hz intended for the earlier proposed Next Generation Linear Collider (NLC). Given the high peak pulse voltage amplitude, an 80 kV switch was utilized. Here, given the added inductance of the pulse transformer, serious design efforts were required to optimize pulse efficiency.
- [2.55] outlines the design and operation of two long pulse modulators for the High Energy Accelerator Research Organization (KEK). One modulator generates 12 MW (130 kV, 92 A) pulses whereas the other produces 16.8 MW (120 kV, 140 A). Both modulators have a maximum usable flat top width of 1.5 ms repeatable at 5 Hz, and use LC bouncer circuits to ensure proper flat top quality (though the required or obtained flat top droop and stability were never reported).
- [2.56] discusses a modulator prototype for the European XFEL. This modulator is rated for a pulse voltage amplitude of 120 kV and a pulse current amplitude of up to 140 A. The pulse duration is 1.7 ms repeatable at 30 Hz, leading to a considerable average power of 380 kW. The obtained flat top stability is less than +/- 0.3%.
- [2.57] describes a modulator development for SNS- and ESS-like requirements. The proposed modulator is capable of delivering 100 kV, 50 A, 3.5 ms pulses repeated at 14 Hz. The pulse droop is less than 1%, and the flat top ripple is less than 0.1%. While interesting, it shall be noted that the pulse transformer on which this modulator is based weighs more than 7500 kg. Scaling this system to the full ESS power requirements seems difficult.

These existing systems demonstrate the versatility and broad applicability of pulse transformer-based modulators. Application pulse lengths range from sub-microsecond level to several milliseconds, whereas peak power levels are observed from a few MW up to hundreds of MW. Pulse voltage amplitudes have been obtained up to the MV level.

Based on the existence of the above modulator systems in conjunction with the abundance of available research literature, pulse transformer-based modulators should be considered a serious candidate for long pulse high power applications. Part of the material within this thesis outlines the design, development and experimental evaluation of pulse transformer-based modulators, and directly adds to a number of the above noted research topics.

### 2.3.3 Marx generator

The principal idea of the Marx generator is to charge an array of capacitors in parallel at low voltage and then discharge them in series to generate a high voltage pulse. This type of circuit was first implemented by Erwin Otto Marx in 1924 using resistors and spark gaps, [2.58], Figure 2.13. In this circuit, the spark gaps are designed to have a breakdown voltage greater than that of the output of the charging stage and thereby either of the capacitors. Thus, the spark gaps initially act as open circuits and the capacitors are charged in parallel via the resistors. The pulse is generated by actively triggering a voltage breakdown in the leftmost spark gap. By doing so, this spark gap practically acts as a short circuit and the two first capacitors in the stack are series connected. This addition of voltage causes the second spark gap in the stack to break down and short circuit, and a chain reaction (called Marx stack erection) is caused in which the spark gaps sequentially short circuit and the voltages of the entire stack add up. In the end of the chain reaction, the spark gap connecting the Marx stack to the load breaks down, applying the full stack voltage $nV_{dc}$ to the load. Here, $n$ is the number of Marx stages and $V_{dc}$ is the charging voltage.

During the pulse event, the storage capacitors discharge and the generated load voltage droops. Note here that as spark gaps are not fully controllable switches, the classical circuit shown in Figure 2.13 necessarily fully depletes the energy storage capacitors each pulse event and is therefore technically not a hard tube pulser. Therefore, this circuit requires a pulse forming line or pulse forming network at the generator output in order to produce an acceptable pulse waveform.

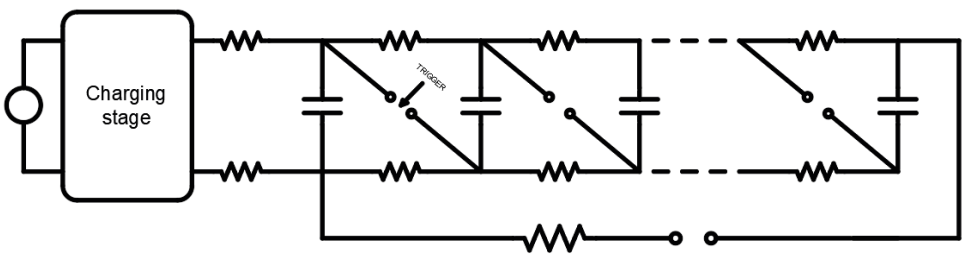



Figure 2.13: Classical high voltage generator circuit as described by Marx in 1924.

A solid-state Marx generator may be formed by replacing the spark gaps with fully controllable switches that may open while conducting the full load current, e.g., IGBTs or MOSFETs. This way, similar to the above-described hard switch and pulse transformer-based topologies, pulses with arbitrary pulse length may be generated, again limited only by the capacity of the energy storage and the power handling capability of the switches. In such modulators, unless the application duty cycle and average power level are very low, the charging resistors are generally

replaced using one of several techniques, most commonly one of the following [2.59]-

- Diode + inductor series combination: the diode facilitates more efficient charging via the inductor, acting as an open circuit during the high voltage discharge. This method is an improvement to the classical chain of resistors but is still limited to lower duty cycles and shorter pulses.
- Common mode choke: the choke inductor allows efficient and much faster charging by exhibiting low impedance in differential mode while appearing as an open circuit (high common mode impedance) during the high voltage discharge. Due to the faster charging, significantly higher duty cycle and pulse repetition rate is made possible [2.60]. However, the practical pulse length and modulator average power remains somewhat limited.
- A second stack of controllable switches: each Marx circuit stage is complemented by an additional switch. By appropriate switch selection, this technique accommodates the full range of average power and duty cycle. On the other hand, this technique is more costly and requires active switches, increasing circuit complexity.

For long pulse high power applications, some variation of the charging scheme based on additional controllable switches is usually adopted by necessity. This type of circuit is exemplified in Figure 2.14, derived from [2.61]. Here, by turning on the lower row of switches, a low impedance charging path is formed. Once charging is complete, these switches are again turned off. Then, by turning on the upper row of switches, the capacitors are connected in series in a manner similar to that described in relation to Figure 2.13, generating the output pulse.

Note that the Marx stage switches may be controlled independently from one another - those Marx stages not turned on are simply bypassed by its parallel diode, [2.61]. Thus, in addition to facilitating efficient pulse generation with variable pulse length, the added controllability of the solid-state Marx generator furthermore permits selection of the pulse amplitude. This functionality may also be used for droop compensation, where a number of auxiliary Marx stages may be switched in successively during the pulse event as the output voltage droops [2.62].

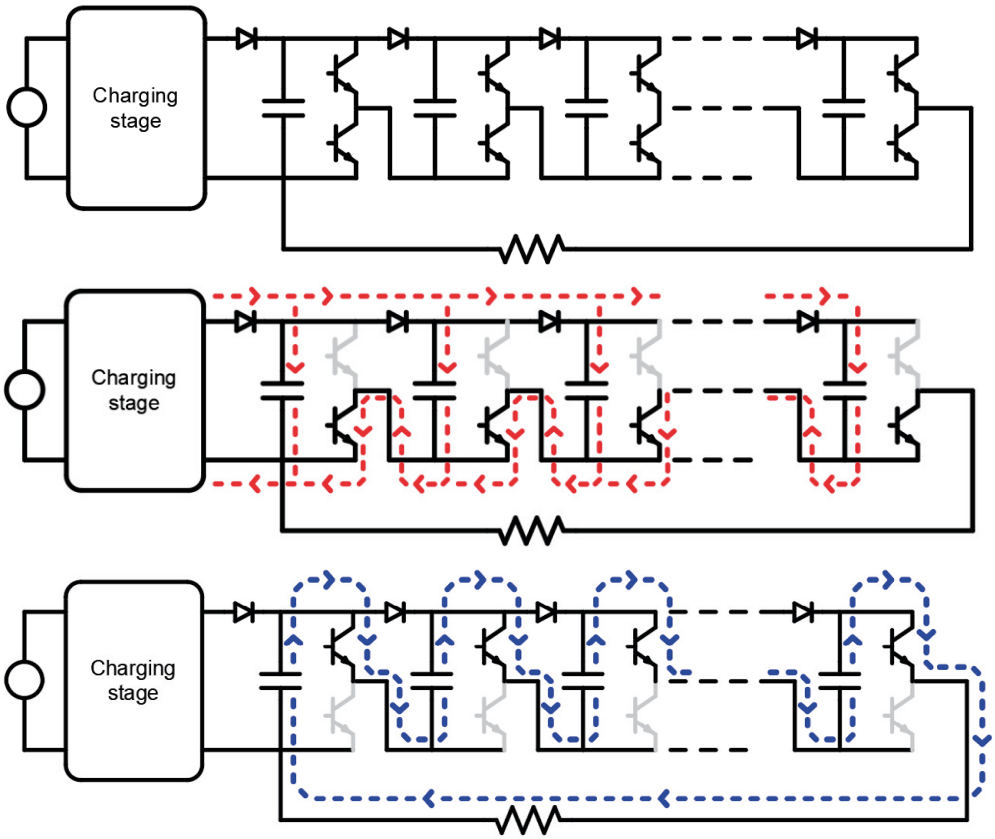



Figure 2.14: Solid state Marx generator topology utilizing second switch stack for charging; a) overview of topology; b) charging procedure; c) Marx stage erection.

Advantages of the solid-state Marx modulator topology include-

- Excellent controllability and flexibility with settable pulse length and pulse amplitude.
- Transformerless construction, eliminating the need for auxiliary demagnetization and bias systems while minimizing stored energy.
- Inherent droop compensation through supplementary Marx stages.
- Relatively short pulse rise time mainly defined by the series inductance of the Marx stage switches, corresponding to high pulse efficiency.
- Simplified switch design (with respect to the hard switch topology).

For these reasons, solid state Marx modulators are used for a large range of applications from hundreds of nanoseconds up to milliseconds.

Some disadvantages of this topology include the following-

- Difficult trade-off in Marx stage voltage level selection for high voltage pulse generation.

  High voltage pulse generation requires either a large number of low voltage stages or a smaller number of high voltage stages-

  - Using a large number of low voltage stages may be impractical due to 1) parasitic capacitance between stages, affecting pulse quality; 2) added losses, especially during charging; 3) cost inefficiency; and 4) high circuit complexity and poor reliability (too many components). [2.59] notes that high-power solid-state Marx generators based on low voltage semiconductors (i.e., maximum voltage rating below a few kV) are impractical for voltages exceeding that of 40-60 kV.
  - Using a small number of high voltage stages solves some of these issues, though suitable switches will be difficult to find commercially off-the-shelf, challenging modulator availability and curtailing access to spare units. Furthermore, using only a few Marx stages complicates droop compensation as the resolution of the pulse output voltage is poor.

  A Marx modulator utilizing a small number of high voltage stages to generate the bulk of the pulse as well a number of low voltage compensator stages was suggested in [2.63]. This is an interesting possibility, though the number of required stages is still high considering long pulse high power applications. Furthermore, this type of system corresponds to added complexity and its feasibility in accurately compensating flat top droop without exceeding stringent flat top ripple requirements remains to be evaluated.

- Difficult trade-off in isolation system selection for high voltage pulse generation

  In high voltage generation, an appropriate isolation system must be used to avoid high voltage breakdown. Due to their simplicity, the high voltage components of hard switch modulators and pulse transformer-based modulators may readily be placed inside an oil tank enclosure. While this is also a possibility for Marx based modulators, placement of especially a large number of active components in the oil tank severely affects the maintainability of the system. For this reason, most Marx generators are air isolated, though this seems unfeasible considering long pulse high power applications due to both cooling requirements and the necessary high voltage isolation level.

- Floating switches and control electronics

As with the hard switch topology, the Marx stack switches and their respective control electronics cannot be grounded, complicating the associated drive circuitry. Furthermore, control electronics jitter may affect pulse flat top performance on a pulse-to-pulse basis.

- Unproven reliability

  The long-term reliability of long-pulse high-power modulators based on the Marx generator topology is yet to be proven.

*Examples of long pulse modulators based on the Marx generator topology*

Several noteworthy long pulse modulators based on the Marx generator topology were found as part of the literature review-

- [2.64] and [2.65] describe a long pulse Marx modulator for the ILC. This modulator is rated for 140 kV, 160 A pulses at 1.5 ms and repeated at 5 Hz. The modulator is based on twenty core Marx stages, responsible for generating the bulk of the pulse, as well as sixteen auxiliary Marx stages for droop compensation. Here, each core Marx stage is based on two sets of six series connected 7 kV IGBT modules. As explained in relation to Figure 2.14, one set is used for charging, whereas the other is used for pulse generation. The auxiliary Marx stages are based on low voltage IGBT modules and ensure a pulse flatness within 1%. The full Marx stack is housed in an oil tank. The full modulator system is quite spacious, and an extension to satisfy ESS requirements seems inappropriate.
- [2.66] outlines an "ILC class" modulator for KEK, quite similar to that described in [2.64] and [2.65]. Here, the developed modulator supplies 120 kV, 120 A, and 1.7 ms long pulses. Similarly, it is based on 20 high voltage core Marx stages for high voltage generation and 16 low voltage supplementary Marx stages for droop compensation. The obtained flat top performance was not reported.
- [2.67] describes a Marx modulator for a 100 kV, 20 A, 1 ms pulsed application. Due to the low average power, on the order of a few kW, this modulator is air isolated. Remarkably, the size of the high voltage structure is therefore on the order of 7 cubic meters. The system is based on 34 core modules and 24 corrector modules. The attainable flat top droop and ripple are on the order of 1%.
- [2.68] describes a new Marx modulator concept intended for multi-millisecond applications. This circuit instead utilizes a parallel boost converter for droop compensation. Though interesting, it was never taken beyond a relatively limited prototyping stage, generating pulses of 3.2 kV, 3.2 A, 3.6 ms at a pulse repetition rate of 0.25 Hz. It is stated that scaling to higher power levels is straightforward, though this remains to be evaluated.

### 2.3.4 Resonant converter topology

The above treated modulator topologies are fairly straightforward in that they essentially provide a direct connection between energy storage and load. Though conceptually simple, extending these modulator topologies for use in long pulse high power applications with stringent flat top requirements is, as has been discussed, not entirely uncomplicated.

However, in considering multi-millisecond applications, pulse efficiency may be conserved with pulse rise times on the order of hundreds of microseconds. Thus, for such applications modern semiconductor technology promotes the possibility of high-power pulse generation by use of modulation techniques. In relation to long pulse modulator applications, this idea was first introduced in [2.69]. Here, a power electronic resonant converter generates a high frequency modulation of the output pulse. For this reason, this topology is sometimes referred to as the "converter modulator". The modulated waveform is stepped up by a high frequency transformer and subsequently demodulated into the intended pulse shape by rectification and filtering, Figure 2.15.

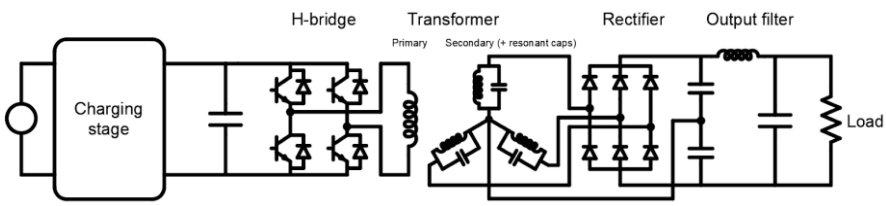



Figure 2.15: Simplified schematic of resonant converter modulator as proposed in [2.69].

Though clearly topologically more complex than the previously discussed modulator topologies, requiring several additional conversion stages, such a modulator has numerous advantages-

- Simplified switch design. As a transformer is used for voltage amplification, in many cases low voltage off-the-shelf semiconductor devices may be used in implementing the pulser.
- Compact construction. By utilization of high frequency switching, the transformer(s) providing voltage amplification can be made significantly more compact than that of an equivalent pulse transformer.
- High efficiency. By use of resonant converter topologies permitting soft switching, high electrical efficiency may be retained. Typically, the efficiency is at least as high as that of the earlier discussed topologies [2.70].
- Inherent droop control. As the resonant converter is pulse width modulated, the capacitor bank droop may be compensated for by successively

increasing the converter output voltage reference throughout the pulse event.

- Modularity is facilitated as the energy storage is not directly linked to the load, augmenting modulator reliability (provided the number of modules and components remains modest).
- Reduced EMI.

Some general disadvantages and difficulties of modulators based on soft switching resonant converters are listed below-

- More complex topology requiring additional conversion stages and components.
- Converter switching adds pulse flat top ripple. A filter balanced with the chosen converter switching frequency is required to ensure that the flat top ripple is limited to load specifications.
- Significantly more complicated control than the previous topologies, especially considering aspects of droop compensation, ripple mitigation and tuning over the full modulator power operating range.
- Component selection in high power applications is not entirely straightforward-

Using resonant converters, high switching frequency is generally preferable to minimize both the transformer and the resonant capacitor. However, present day 1.7 kV high power IGBT technology limits switching frequency to between 15 and 20 kHz. For IGBTs with higher voltage ratings, the maximum switching frequency is further reduced. One such application (further discussed below) required resonant capacitors cycling several MVAR approaching 100 kVAC. Importantly, operation of capacitors at such high power and frequency is associated with both thermal cycling and dielectric fatigue, severely affecting reliability.

On the other hand, while MOSFETs are able to operate at significantly higher switching frequencies, they are limited in both power and voltage handling capability. Here, on the other extreme, one such long pulse high power modulator (further discussed below) required over 500 MOSFETs including drivers to meet the specified pulse power requirements. Such an implementation is extremely complex, upsetting reliability and system maintainability.

Finally, it is pointed out that both MOSFETs (generally) as well as high-voltage IGBTs are quite limited with respect to current handling capacity. Thus, it must be ensured that operation of the resonant converter reliably results in soft switching throughout the entire operating range of the modulator, including during flat-top droop compensation, as loss of soft switching would result in drastic increase of converter losses and therefore transistor destruction. Importantly, considering the

often quite wide operating range of modulators, this is very difficult to achieve and therefore a significant drawback of this type of topology.

*Examples of modulators based on the resonant converter topology*

A number of interesting long pulse modulators based on the converter modulator topology was found as part of the literature review-

- [2.71] describes a resonant converter-based modulator for the Spallation Neutron Source (SNS). This modulator features 11 MW, 140 kV, 1.2 ms long pulses repeated at 50 Hz. This was the first long pulse high power modulator based on resonant converters, and represented a major advance in modulator pulse length and average power.

  This system utilizes 3.3 kV IGBTs operated at the relatively high switching frequency of 20 kHz, which markedly impacted their reliability and lifetime. This later led to serious redesign efforts [ref]. From the perspective of resonant converters, however, this switching frequency is quite low and large resonant capacitors cycling 3.5 MVAR at 85 kVAC were required for proper operation, further impacting reliability. Finally, the reported pulse flat top performance does not seem optimal and it appears unlikely that correcting this to match the flat top requirements of the ESS modulators represents a straightforward task.

- [2.72] outlines a similar long pulse modulator for the Korea Atomic Energy Research Institute (KAERI). This modulator is rated for 105 kV, 50 A, 1.5 ms pulses repeated at 60 Hz. The development represents an improved version of that presented in [2.71] benefitting from the accumulated experience with the topology at SNS and SLAC. Here, the IGBTs were fitted with snubbers allowing also zero voltage switching (ZVS), further improving modulator efficiency and IGBT lifetime. The pulse flat top performance appears improved with respect to [2.71], though still suboptimal.

- [2.73]-[2.76] describes design efforts of a resonant converter modulator later procured by ESS from Ampegon. The modulator was developed by Ampegon in collaboration with ETHZ, and operates at reduced ESS modulator specifications at 115 kV, 25 A, 3.5 ms and 14 Hz.

  This modulator system is very complex, requiring an extreme number of components and interconnections (more than 500 MOSFETS, several thousand diodes, and tens of thousands of capacitors). Furthermore, the reported pulse flat top performance appears suboptimal despite utilization of complex control loops. The system footprint is large, and in conjunction

with the above noted issues, scaling to full ESS klystron modulator requirements and beyond appears challenging.

## 2.4 Comparison of modulator topologies

This chapter has reviewed the characteristics of pulsed power modulators. Performance criteria with respect to long pulse applications have been discussed and a survey of available modulator technology and existing systems has been conducted. This section aims to compile this information and to provide a condensed comparison of available high power modulator technology. It is again emphasized that definitions of applicable performance criteria vary in available literature, and that therefore this comparison is not perfectly accurate though highly indicative.

### 2.4.1 Qualitative comparison of available modulator topologies

First, a somewhat qualitative comparison of the characteristics of the above discussed modulator topologies considering a tentative extension to the requirements imposed by the ESS linear accelerator application (and, in the future, other long pulse high power application areas) is given. The results are summarized in table 2.4.1-

*Modularity*

The hard switch and pulse transformer-based topologies are by design based on singular components (i.e., single hard switch, and single hard switch plus single pulse transformer, respectively), generating topologically simple pulsers with straightforward circuit control and operation. However, as has been shown, in long pulse high power applications the required componentry becomes both complicated and extremely large. Use of monolithic components in such applications severely impacts maintainability and repair times. Furthermore, all such components must be custom designed and are therefore proprietary and single source.

Implemented properly, a modular topology can alleviate these system issues. However, such designs are usually more complex and, if taken to the extreme, modularity may itself become a considerable issue. For example, solid state Marx modulators require a large number of rather complicated stages to provide high voltage pulses with good flat top performance. Here, the Marx stage switches require independent drive circuitry and the full stack must be placed in oil.

*Scalability*

Scalability is important in considering available technology for the ESS linear accelerator as well as for future developments. Examples of the monolithic

topologies already require extremely large components. Scaling these systems for even higher power levels and longer pulse widths seems disadvantageous and may for future projects even be impossible. Similarly, adding even more Marx stages to, e.g., [2.64] or additional resonant converter modules to, e.g., [2.73] in order to meet ESS pulse power requirements is objectionable given their present complexity.

*Complexity*

In assessing complexity several criteria must be considered. For example, monolithic modulators are topologically simple but require complicated component design. On the other hand, modular topologies may be based on simple and widely available off-the-shelf components but require significantly more complicated control and system level consideration. The below overview includes issues of topological complexity, complexity in system design, and complexity of control.

*Pulse quality*

Modulator pulse power quality is evaluated according to the criteria outlined in section 2.1.2. In particular, pulse rise time, flat top ripple and flat top droop are considered. Here, most of the above-described modulator systems have been developed for a flat top stability requirement on the order of +/-0.5%. While some of these modulators display flat top performance well within these limits, the viability of further reducing the flat top ripple and flat top droop levels while extending the pulse length by several milliseconds must be taken into consideration (scalability).

*Efficiency*

Given the required high average power of the ESS klystron modulators and, in extension, the ESS linear accelerator, efficiency is of key importance. Most of the discussed modulators have experimentally displayed electrical efficiencies on the order of 90% and above.

However, in addition to electrical efficiency, pulse efficiency must also be considered. Pulse transformer-based modulators for long pulse high power applications are well represented by first order systems, thereby showing relatively poor pulse efficiency. Hard switch and Marx based modulators, on the other hand, are in principle limited only by the series inductance of the switch, allowing significantly shorter pulse rise periods. Modulators based on resonant converters typically fall somewhere in between those two extreme cases. Such modulators generally require an output filter to limit the flat top ripple, corresponding to a direct trade-off with pulse rise time.

*Summary*

Table 2.4.1 summarizes the above discussion points. Here, future accelerator projects and other long pulse power applications should be kept in mind in addition to that of the ESS linac project-

**Table 2.2: Qualitative comparison of available modulator technology, considering extension to ESS klystron modulator requirements and future long pulse high power application areas.**

| | | **Single switch** | **Pulse transformer** | **Solid state Marx** | **Resonant converter** |
|---|---|---|---|---|---|
| Modularity | | Monolithic | Monolithic | Excessive | (Design) |
| Scalability (power, pulse length) | | Very poor | Very poor | Very poor | Poor |
| Complexity | Topology | Simple | Simple | Moderate | High |
| | System design | Very challenging | Challenging | Challenging | Very challenging |
| | Control | Simple | Simple | Challenging | (Very) challenging |
| Reliability | | Very good | Excellent | Poor | Very poor |
| Maintainability | | Poor | Poor | Poor | Poor |
| Pulse quality (rise time, ripple, droop) | | Very good | Very good | Good | Good |
| Efficiency | Electrical | Very good | Very good | Very good | Very good |
| | Pulse shape | Excellent | Poor | Excellent | Good |
| Size (component volume, footprint) | | Very poor | Very poor | Poor | Poor |

This summary demonstrates that while available modulator technology produces high-quality high-power pulses (generally very good pulse quality and modulator efficiency), there are appreciable challenges in conveniently further expanding modulator power levels and attainable pulse length. Most notably, use of either a small number of very large components or a large number of very small components, corresponds to issues related to complexity as well as challenges in appropriate system design and modulator maintainability. Already substantial in present day technology, these issues are magnified in scaling, especially as pulse flat top performance must be both improved and maintained over an extended pulse length period. Additionally, system footprint is generally demonstrably large for these modulators. Increased average power levels are here likely to result in prohibitive designs.

### 2.4.2 Quantitative summary of state-of-the-art modulator technology

The preceding section provided an overall assessment of modularity, complexity, reliability and other performance criteria based on corresponding modulator topology. This section summarizes the review of available high power modulator technology by relating attainable pulse length, peak pulse power, and modulator average power in a series of plots. These plots were generated using information published in, among other, the above reviewed literature.

Figure 2.16 shows existing modulator systems by graphing their maximum pulse length versus their maximum average power and peak pulse power. Applications with required pulse lengths from a few microseconds up to several milliseconds are included. Typically, the required pulse repetition rate of klystron modulators is on the order of tens of Hz. Therefore, the application pulse length is an important determinant of modulator average power. Hence, as can be seen, modulators with peak pulse powers on the order of hundreds of MW may still represent relatively modest modulator average power. Considering modulator systems in the millisecond range, it is seen that all of them represent the same scope of peak pulse power.

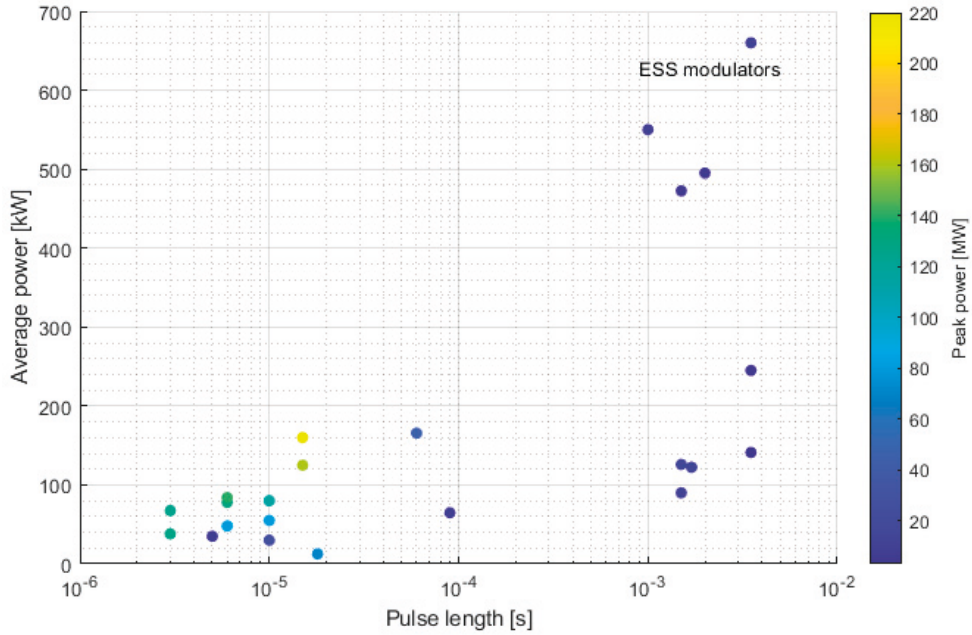



Figure 2.16: Overview of existing modulator systems. Attainable pulse length is plotted versus modulator average power and modulator peak pulse power.

Figure 2.17 expands on the region representing applications in the millisecond range. Members of each modulator family (with the exception of PFN based modulators) from the above list of literature are featured. Note here that in comparison to existing state of the art modulator technology, ESS klystron modulator requirements represent a significant increase in either or both required pulse length and modulator average power. In two cases, a higher peak power on the order of 20-40% is seen. In these cases, however, ESS requirements correspond to a pulse length increase of ~230% and an average power increase of ~440%.

This plot illustrates some of the objections raised in the previous section regarding basing the ESS modulators on more conventional modulator technology-

The modulator system closest in pulse length to ESS application requirements hinges on a pulse transformer-based approach. As discussed in section 2.3.2, this pulse transformer weighs on the order of 7500 kg. Scaling such a system to be capable of delivering twice the peak power and three times the average power with significantly improved flat top performance is both inconvenient and highly challenging. Similarly, the modulator with most similar average power is based on a resonant converter. Here, extending the pulse length by 350% does not seem feasible given the documented reliability issues and suboptimal flat top performance. As outlined in Table 2.2, similar objections may be raised for each of the modulator systems depicted in Figure 2.17.

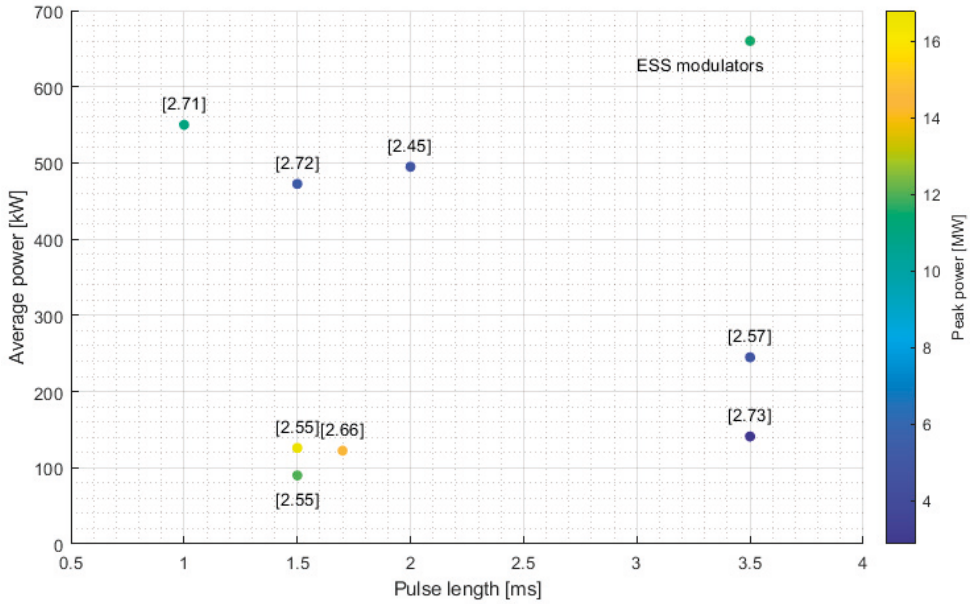



Figure 2.17: Overview of existing modulator systems for millisecond applications. Attainable pulse length is plotted versus modulator average power and modulator peak pulse power.

## 2.5 References

[2.1] N. G.Glasoe and J. V. Lebacqz, “Pulse Generators”, MIT Radiation Laboratory Series, vol. 5, McGraw-Hill Book Company, New York, 1948.

[2.2] International Electrotechnical Commission. EMC Product Family Standards: Emission. Accessed: Jun. 16, 2018. [Online]. Available: http://www.iec.ch/emc/emc_prod/prod_emission.htm

[2.3] Harmonic Control in Electric Power Systems. IEEE Standard 519-2022, 2022.

[2.4] M. K. Walker, “Electric Utility Flicker Limitations,” IEEE Trans. Ind. Appl., vol. IA-15, no. 6, pp. 644-655, Nov. 1979.

[2.5] S. Prerea and S. Elphic, Applied Power Quality: Analysis, Modelling, Design and Implementation of Power Quality Monitoring Systems, 1st ed. Oxford: Elsevier, 2023.

[2.6] M. Bishop et al., “Voltage flicker measurement and analysis system,” IEEE Computer Applications in Power, vol. 7, no. 2, pp. 34-38, Apr. 1994.

[2.7] M. H. Rashid, Power Electronics Handbook, 3rd ed. Oxford: Elsevier, 2011.

[2.8] Voltage fluctuations, flicker and power quality. Accessed: June 25, 2023. [Online]. Available: https://www.fluke.com/en/learn/blog/power-quality/voltage-fluctuations-flicker

[2.9] IEC 61000-3-11:2017 (Limitation of voltage changes, voltage fluctuations and flicker in public low-voltage supply systems). Accessed: June 25, 2023. [Online]. Available: https://webstore.iec.ch/publication/27902

[2.10] IEC 61000-3-3:2013 (Limitation of voltage changes, voltage fluctuations and flicker in public low-voltage supply systems). Accessed: June 25, 2023. [Online]. Available: https://webstore.iec.ch/publication/68776

[2.11] M. Collins and C. A. Martins, “Evaluation of a novel capacitor charging structure for flicker mitigation in high-power long-pulse modulators,” IEEE Trans. Plasma Sci., vol. 47, no. 1, pp. 985–993, Jan. 2019.

[2.12] H. J. Eckoldt, "Long Pulse Modulators". Accessed: June 25, 2023. [Online]. Available: https://cds.cern.ch/record/2038627/files/217-244-Eckoldt.pdf

[2.13] Harmonic Control in Electric Power Systems. IEEE Standard 519-2022, 2022.

[2.14] R. Sanjeevikumar et al., “Power Quality in Modern Power Systems”, 1st ed. Oxford: Elsevier, 2020.

[2.15] Application and Specification of Harmonic Filters. IEEE Guide 1531-2020, 2021.

[2.16] L. Motta and N. Faúndes, “Active / passive harmonic filters: Applications, challenges & trends” in Proc. of the 17th Int. Conf. on Harmonics and Quality of Power (ICHQP), Belo Horizonte, Brazil, Oct. 2016, pp. 657-662.

[2.17] C-C. Hou et al., “Modelling and Control of Three-Phase Active front-end Converters” in 33rd IEEE Annual Conference on Industrial Electronics, Taipei, Taiwan, 2007, pp. 1449-1454

[2.18] S. Pütz et al., “Klystron Modulators for the FAIR pLINAC” in Proc. 2018 IEEE Int. Power Modulator and High Voltage Conf. (IPMHVC), Jackson, WY, USA, Jun. 2018, pp. 337-338.

[2.19] M. Collins et al., “Evaluation of klystron modulator performance in interleaved pulsing schemes for the ESS neutrino super beam project,” in Proc. IEEE Int. Power Modulator and High Voltage Conf., Knoxville, TN, USA Jun. 2022, pp. 60-63.

[2.20] B. Gålnander et. al., “H- source design, integration into ESS and RF upgrade studies”. Technical report. May 2019, pp. 1-37

[2.21] A. Alekou, E. Baussan, A.K. Bhattacharyya, N. Blaskovic Kraljevic, M. Blennow, M. Bogomilov, B. Bolling, E. Bouquerel, O. Buchan, A. Burgman, C.J. Carlile, J. Cederkall, P. Christiansen, M. Collins, E. Cristaldo Morales, P. Cupiał, L. D'Alessi, H. Danared, D. Dancila, J. P. A. M. de André, J.P. Delahaye, M. Dracos, I. Efthymiopoulos, T. Ekelöf, M. Eshraqi, G. Fanourakis, A. Farricker, E. Fernandez-Martinez, B. Folsom, T. Fukuda, N. Gazis, B. Galnander, Th. Geralis, M. Ghosh, G. Gokbulut, L. Halić, M. Jenssen, A. Kayis Topaksu, B. Kildetoft, B. Kliček, M. Kozioł, K. Krhač, Ł. Łacny, M. Lindroos, C. Maiano, C. Marrelli, C. Martins, M. Mezzetto, N. Milas, M. Oglakci, T. Ohlsson, M. Olvegard, T. Ota, J. Park, D. Patrzalek, G. Petkov, P. Poussot, R. Johansson, S. Rosauro-Alcaraz, D. Saiang, B. Szybiński, J. Snamina, G. Stavropoulos, M. Stipčević, R. Tarkeshian, F. Terranova, J. Thomas, T. Tolba, E. Trachanas, R. Tsenov, G. Vankova-Kirilova, N. Vassilopoulos, E. Wildner, J. Wurtz, O. Zormpa, Y. Zou, "The European Spallation Source neutrino Super Beam Conceptual Design Report", The European Physical Journal ST, vol. 231, no. 21, 2022.

[2.22] M. Collins and C. A. Martins, “Evaluation of feasibility of high-power long-pulse transformer using single-layer and pancake winding techniques,” IEEE Trans. Plasma Sci., vol. 49, no. 7, pp. 2217–2226, Jun. 2021.

[2.23] J. Holma and M. J. Barnes, “Measurements on a 12.5/17.5 kV Inductive Adder with Extremely High Stability for the Damping Ring Kickers of the Compact Linear Collider at CERN” in Proc. 21st European Conf. on Power Electronics and Applications (EPE'19), Genova, Italy, Sept. 2019, pp. 1–10

[2.24] J. Holma and M. J. Barnes, “Prototype Inductive Adders With Extremely Flat-Top Output Pulses for the Compact Linear Collider at CERN,” IEEE Trans. Plasma Sci., vol. 46, no. 10, pp. 3348-3358, Jun. 2018.

[2.25] C. A. Martins, F. Bordry, and G. Simonet, “A solid state 100 kV long pulse generator for klystrons power supply,” in Proc. 13th Eur. Conf. Power Electron. Appl., Barcelona, Spain, Sep. 2009, pp. 1–10

[2.26] C. A. Martins, “The Stacked Multi-Level Klystron Modulators for the ESS Linac”, presented at the IEEE Int. Power Modulator and High Voltage Conf., Knoxville, TN, USA, Jun. 2022.

[2.27] G. Metzger, “Transmission Lines with Pulse Excitation”, 1st ed. Cambridge: Academic Press, 2012.

[2.28] G. A. Mesyats, "Pulsed Power, 1st ed. NY: Springer, 2007.

[2.29] I. A. D. Lewis and F. H. Wells, "Millimicrosecond Pulse Techniques", 1st ed. Oxford: Pergamon Press, 1959.

[2.30] J. Lehr, "Foundations of Pulsed Power Technology", 1st ed. Hoboken, NJ: Wiley, 2018.

[2.31] A. Haddad and D. F. Warne, "Advances in High Voltage Engineering", 1st ed. Londong, England: Institution of Engineering and Technology, 2004.

[2.32] A. Blumlein, "Improvements in or relating to apparatus for generating electrical impulses", UK Patent 589127, June 12, 1947.

[2.33] I. C. Somerville et al., “An efficient stacked-Blumlein HV pulse generator”, Measurement Science and Technology, vol. 1, no. 9, pp. 865-868, Apr. 1990.

[2.34] R. Ness, "Rayleigh Line PFN Formulas". Accessed: June 25, 2023. [Online]. Available: https://www.nessengr.com/techdata/pfn/pfn.html#Rayleigh

[2.35] E. A. Guillemin, "Comunication networks: the classical theory of long

lines, filters and related networks". New York, N.Y.: John Wiley & Sons,

Inc., vol. 2, 1953.

[2.36] C. Burkhart, “Pulsed Power Engineering Basic Topologies”, presented at the 2011 USPAS, Hampton, VA, USA, Jan. 2011.

[2.37] R. Ness, "Type E Guillemin Circuit Formulas". Accessed: June 25, 2023. [Online]. Available: https://www.nessengr.com/techdata/pfn/pfn.html#TypeE

[2.38] N. G. Glasoe and J. V. Lebacqz, "Guillemin's Theory and the Voltage-fed network" in Pulse Generators, MIT Radiation Laboratory Series, vol. 5, McGraw-Hill Book Company, New York, 1948, pp. 189-207.

[2.39] R. Ness, "520 MW Klystron Line Type Modulator". Accessed: June 25, 2023. [Online]. Available: https://www.nessengr.com/capabilities/pulse-generators/line-type-modulators/#BM520_MW

[2.40] R. Ness, "8 MW Klystron Line Type Modulator". Accessed: June 25, 2023. [Online]. Available: https://www.nessengr.com/capabilities/pulse-generators/line-type-modulators/#BM8_MW

[2.41] M. Collins and C. A. Martins, “Optimal design of electronic bouncers for long-pulse high-power modulators,” IEEE Trans. Plasma Sci., vol. 49, no. 2, pp. 819–829, Feb. 2021.

[2.42] C. Burkhart, “Pulsed Power Engineering Basic Topologies”, presented at the 2011 USPAS, Hampton, VA, USA, Jan. 2011.

[2.43] M. P. J. Gaudreau et al., "Modulator development for the Next Generation Linear Collider" in Proc. of the 24th Int. Power Modulator Symposium, Norfolk, VA, USA, Jun. 2000, pp. 153-156.

[2.44] J. A. Casey et al., “Solid-state pulsed power systems for the Next Linear Collider” in Proc. of the 25th Int. Power Modulator Symposium, Hollywood, CA, USA, 30 Jun.-3 Jul. 2002, pp. 102-105.

[2.45] M. Kempkes et al., “A Klystron Power Systems for the ISIS Front End Test Stand” in Proc. of the 2010 Int. Particle Accelerator Conf., Kyoto, Japan, May 2010, pp. 3326-3328.

[2.46] I. Roth et al., “A high-voltage hard-switch modulator for the international linear collider” in Proc. of the 2007 IEEE Particle Accelerator Conference (PAC'07), Albuquerque, NM, USA, Jun. 2007, pp. 2301-2303.

[2.47] Y. Wang, M. Li, K. Li, and G. Zhang, “Optimal design and experimental study of pulse transformers with fast rise time and large pulse duration,” IEEE Trans. Plasma Sci., vol. 42, no. 2, pp. 300–306, Feb. 2014.

[2.48] D. Habibinia and M. R. Feyzi, “Optimal winding design of a pulse transformer considering parasitic capacitance effect to reach best rise time and overshoot,” IEEE Trans. Dielectr. Electr. Insul., vol. 21, no. 3, pp. 1350–1359, Jun. 2014.

[2.49] J. Biela, D. Bortis, and J. W. Kolar, “Modeling of pulse transformers with parallel- and non-parallel-plate windings for power modulators,” IEEE Trans. Dielectr. Electr. Insul., vol. 14, no. 4, pp. 1016–1024, Aug. 2007.

[2.50] J. Biela and J. W. Kolar, “Using transformer parasitic for resonant converters-a review of the calculation of the stray capacitance of transformers,” IEEE Trans. Ind. Appl., vol. 44, no. 1, pp. 223–233, Jan./Feb. 2008

[2.51] D. Bortis et al., “Optimal Design of a DC Reset Circuit for Pulse Transformers” in Proc. IEEE Applied Power Elec. Conf. and Exposition, Anaheim, CA, USA, 25 Feb.-1 Mar. 2007, pp. 1171-1177.

[2.52] D. Aguglia et al., “Design solutions for compact high current pulse transformers for particle accelerators' magnets powering” in Proc. of 17th European Conf. on Power Electronics and Applications (EPE'15), Geneva, Switzerland, Sept. 2015, pp. 1-8.

[2.53] D. Bortis et al., “Design and control of an active reset circuit for pulse transformers,” IEEE Trans. Dielectr. Electr. Insul., vol. 16, no. 4, pp. 940-947, Aug. 2009.

[2.54] M. P. J. Gaudreau et al., “Modulator development for the Next Generation Linear Collider” in Proc. of the 24th International Power Modulator Symposium, Norfolk, VA, USA, Jun. 2000, pp. 153-156.

[2.55] M. Akemoto et al., “Long-pulse modulator for the superconducting RF test facility at KEK” in Proc. of the 16th IEEE Int. Pulsed Power Conference (PPC'07), Albuquerque, NM, USA, Jun. 2007, pp. 1044-1048.

[2.56] H. Leich et al., “Development and test of XFEL modulator prototypes” in Proc. of the 2009 IET European Pulsed Power Conf., Geneva, Switzerland, Sept. 2009, pp. 1-3.

[2.57] I. Roth et al., “Regulator / hard switch modulator” in Proc. of the 2013 Particle Accelerator Conf., Pasadena, CA, USA, Dec. 2013, pp. 722-724.

[2.58] E. Marx, “Versuche über die Prüfung von Isolatoren mit Spanningsstößen”, Elektrotechnische Zeitschrift, vol. 45, pp. 652-654, 1924.

[2.59] J. A. Casey et al., “Marx Bank Technology for Accelerators and Colliders” in Proc. of the 2008 IEEE Int. Power Modulator and High-Voltage Conf., Las Vegas, NV, USA, May 2008, pp. 124-127.

[2.60] J. O'Loughlin et al., “High repetition rate charging a Marx type generator” in Proc. of the 28th IEEE Int. Conf. on Plasma Sci. and the 13th IEEE Int. Pulsed Power Conf., Las Vegas, NV, USA, Jun. 2001, pp. 242-245.

[2.61] Z. Zhong et al., "Review on Solid-State-Based Marx Generators", IEEE Trans. Plasma Sci., vol. 49, no. 11, pp. 3625-3643, Nov. 2021.

[2.62] F. Arntz et al., "New concepts for pulsed power modulators: Implementing a high voltage Solid-State Marx Modulator" in Proc. of the 2012 IEEE Int. Power Modulator and High-Voltage Conf. (IPMHVC), San Diego, CA, USA, Jun. 2012, pp. 28-30.

[2.63] M. Kempkes et al., “Marx Bank Technology for the International linear collider” in Proc. of the 2007 IEEE Particle Accelerator Conf. (PAC), Albuquerque, NM, USA, Jun. 2007, pp. 2590-2592.

[2.64] J. A. Casey et al., “Marx Bank Technology for Accelerators and Colliders” in Proc. of the 2008 IEEE Int. Power Modulators and High-Voltage Conf., Las Vegas, NV, USA, May 2008, pp. 124-127.

[2.65] F. Arntz et al., “New concepts for pulsed power modulators: Implementing a high voltage Solid-State Marx Modulator” in Proc. of the 2012 Int. Conf on Vacuum Electronics, Monterey, CA, USA, Apr. 2012, pp. 427-428.

[2.66] M. P. J. Gaudreau et al., “ILC-class Marx modulator at KEK” in Proc. of the 2014 Int. Conf on Vacuum Electronics, Monterey, CA, USA, Apr. 2014, pp. 449-450.

[2.67] M. Acharya and P. Shrivastava, “A 100 kV, 20 A, 1 ms long pulse solid-state Marx modulator for klystron”, Nuclear Instruments and Methods in Physics - Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, vol. 905, no. 11, pp. 96-103, Oct. 2018.

[2.68] C. Yeckel, "Multistage Marx with Parallel Active Droop Compensation for Long Pulses”, presented at the 2015 IEEE Pulsed Power Conference, Austin, TX, USA, Jun. 2015.

[2.69] W. A. Reass et al., “The polyphase resonant converter modulator system for the Spallation Neutron Source linear accelerator” in Proc. of the 25th Int. Power Modulator Symposium, Hollywood, CA, USA, Jun. 2002, pp. 684-688.

[2.70] W. A. Reass et al., “Polyphase resonant converter-modulators for the KAERI proton engineering frontier project accelerator klystron RF amplifier system”, in Proc. of the 2008 IEEE Int. Power Modulators and High-Voltage Conf., Las Vegas, NV, USA, May 2008, pp. 231-234.

[2.71] W. A. Reass et al., “High-frequency multimegawatt polyphase resonant power conditioning”, IEEE Trans. Plasma Sci., vol. 33, no. 4, pp. 1210-1219, Aug. 2005.

[2.72] W. A. Reass et al., “Design and control of an active reset circuit for pulse transformers,” IEEE Trans. Dielectr. Electr. Insul., vol. 18, no. 4, pp. 1104-1110, Aug. 2011.

[2.73] M. Jaritz and J. Biela, “115KV solid state long pulse modulator for the European spallation source (ESS)" in Proc. of the 21st Int. Conf. on Pulsed Power (PPC'17), Brighton, UK, Jun. 2017, pp. 1-4.

[2.74] M. Jaritz and J. Biela, “System Design and Measurements of a 115-kV/3.5-ms Solid-State Long-Pulse Modulator for the European Spallation Source”, IEEE Trans. Plasma Sci., vol. 46, no. 10, pp. 3232-3239, Mar. 2018.

[2.75] M. Jaritz et al., “Control of a modular series parallel resonant converter system for a solid state 2.88MW/115-kV long pulse modulator" in Proc. of the 17th European Conf. on Power Electronics and Applications (EPE'15), Geneva, Switzerland, Sept. 2015, pp. 1-11.

[2.76] M. Jaritz and J. Biela, “Optimal Design of a Modular Series Parallel Resonant Converter for a Solid State 2.88 MW/115-kV Long Pulse Modulator”, IEEE Trans. Plasma Sci., vol. 42, no. 10, pp. 3014-3022, Jul. 2014.

# 3. Stacked Multi-Level modulator

Chapter 1 introduced the European Spallation Source linac application and the associated power modulator requirements. In light of these requirements, chapter 2 conducted an in-depth review of available modulator technology. In particular, it was demonstrated that extending or scaling existing modulator systems to ESS application requirements would represent a significant challenge. This chapter discusses the most important limitations in achieving scaling, and consequently develops the novel Stacked Multi-Level (SML) modulator topology in directly addressing the identified shortcomings.

## 3.1 Synopsis and justification

It may be inferred from the literature review conducted in chapter 2 and qualitatively presented in Table 2.2 that issues related to modulator scalability is pertinently related to unavoidable complications resulting from aspects of modularity. The performance of monolithic systems depends exclusively on individual components. For example, considering the single switch topology, developing a single hard switch capable of long pulse high power operation combining excellent pulse quality, mechanical stability and system maintainability is extremely challenging, [ref]. Further increases to pulse length and pulse power directly advances and aggravates these issues. Another important complication of high-power systems of low modularity is the dependency on medium to high voltage capacitor chargers in limiting system primary side current. Such charger systems, further described in chapter 7, are notably spacious, feature poor AC line power quality and deteriorate electrical efficiency.

On the other hand, resolving the above issues through series connection of multiple independent output circuits – though possible – typically results in an overly modular system. For example, considering use of modern solid state Marx generator technology would require several tens of circuits with independent floating control electronics, all submerged in a dedicated oil tank assembly. Here, whereas design of individual switch circuitry has been simplified, design and control of the complete system is equally complicated. Again, further extending the pulse length and pulse power requires additional Marx stages in extending droop compensation

while maintaining the flat top ripple constraint, crippling system maintainability and furthering complexity.

The same issues are also present in considering resonant converter systems. Whereas MOSFETs permit operation at high switching frequency, preferred in maximizing the benefits of soft switching and minimizing the associated transformer volume, the high application average power requires use of many hundreds or even up to several thousands of MOSFET switches and associated circuitry. Instead utilizing IGBTs permits a significant reduction in the number of components. However, as the switching frequency is comparatively limited, the benefits of resonant converter technology is moderate. At the same time, the amount of reactive power cycled at high voltage is substantial, translating into reliability issues. These limits are dictated by available semiconductor technology and, presently, there appears to be no appropriate compromise in this type of application.

With difficulties in adapting existing modulator technology to the challenges presented by the ESS linac application, it was necessary to develop and implement a new modulator topology directly addressing the identified shortcomings of existing technology. Section 3.2 outlines the fundamental basis of this development work and section 3.3 provides references to chapters and published material addressing specific topics related to the developed modulator topology.

## 3.2 Development of the Stacked Multi-Level topology

The literature review presented in chapter 2 and analysed in the above determined that one of the principal challenges in choosing a suitable modulator topology in view of long pulse high power applications is the selection of an appropriate and, concurrently, achievable level of modularity. On one hand, monolithic or non-modular systems generally result in large and impractical systems, with their topological simplicity being in conflict with the consolidation of pulse quality, system size, efficiency and maintainability. On the other hand, excessive modularity entails overly complex and difficult to maintain systems, and should similarly be avoided. Consequently, in view of the present long pulse high power application, a suitable modulator topology should allow limiting modularity to, e.g., between 4 to 10 modules. This boundary on modularity suggests several consequences in light of present-day semiconductor technology. First, given the required pulse output voltage and the level of modularity, it is immediately clear that the system is to be transformer-based. As will be discussed at length in chapter 5, one of the key issues with pulse transformer-based systems is that such transformers have to be sized for the full voltage-time integral associated with the long pulse, Figure 3.1.a. In combination with stringent pulse rise time demands, this requirement results in extremely large transformer units, [3.1]. Furthermore, as indicated, the transformer

unit must be fully demagnetized in-between pulse events, corresponding to a sizable reverse voltage across the klystron load, strictly limiting the maximum attainable pulse length for a given application pulse repetition rate, [3.2]. Again, further extending the pulse length aggravates these issues. Therefore, instead, it would be favourable to consider transformers intended for high-frequency switched operation in minimizing system size and enhancing maintainability. The operation of such a transformer is illustrated in Figure 3.1.b. Note that this type of operation presents no such inherent limitations to extending pulse length or pulse repetition rate provided pulse and average power handling requirements are managed properly. Of course, this type of operation, following transformer amplification, would require rectification and filtering in producing a smooth output pulse waveform. It must also be ensured that the proposed pulse waveform modulation-demodulation can be handled such that, e.g., both the flat top ripple constraint and pulse rise time constraints are met. These considerations are treated in detail in chapter 5.

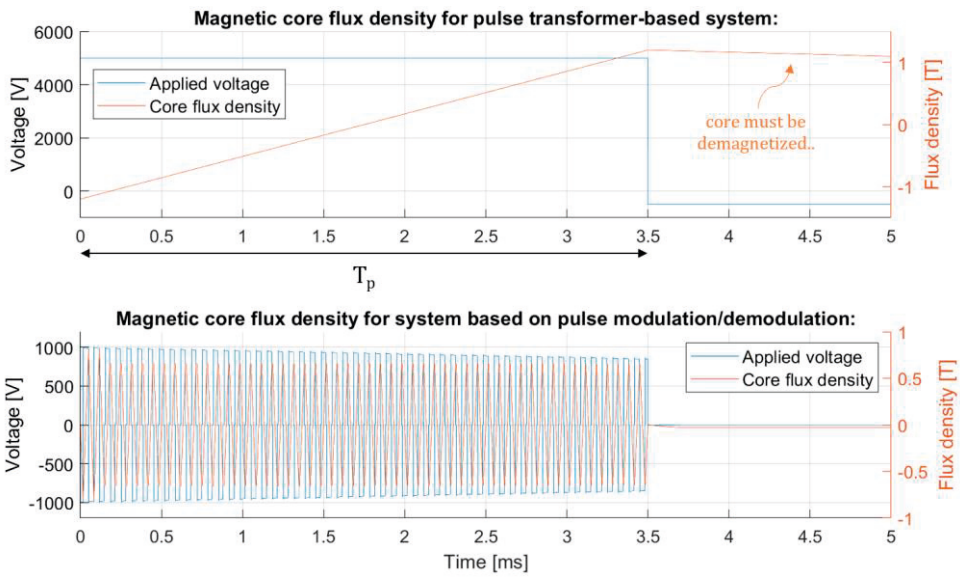



Figure 3.1: Magnetic core flux density for excitation in a) pulse transformer-based system; and in b) proposed scheme based on pulse modulation-demodulation strategy. The proposed strategy both 1) corresponds to significantly reduced voltage-time integral, resulting in substantially smaller modulator components; and 2) eliminates topologically imposed limitations on achievable pulse length and pulse repetition rate.

Further note that the above level of modularity and proposed mode of operation aptly match the features and attributes of available high power IGBT technology. Here, the level of modularity and the transformation ratio should be chosen in an arrangement which 1) permits use of low voltage capacitor chargers in improving system size and efficiency, 2) permits placement of all active components in low voltage cabinets for ease of access in ensuring maintainability, and 3) allows use of

standardized IGBT modules in view of current and power cycling handling capability. Finally, resonant converter operation should be avoided given the limits on switching frequency in considering high-power IGBT technology and resonant capacitors, [3.3].

### 3.2.1 Pulse generation stage

Based on the above discussion, the basic pulse generation circuit depicted in Figure 3.2 is proposed, [3.4]-[3.5]. The fundamental working principle of this pulse generation circuit is described in the following referring to Figure 3.3. Here, it is assumed that the capacitor charger – to be discussed in further detail in the following – has charged the capacitor bank to some primary-side voltage $V_p$. To generate a pulse, the H-bridge converter synthesizes an ac voltage waveform as shown in Figure 3.3.b. This voltage waveform is applied to and amplified by the transformer, Figure 3.3.c. Importantly, the amplitude-duration of the positive and negative half cycles of this waveform should be equal over time to avoid saturation of the transformer unit as described in [3.6]. The amplified waveform is subsequently rectified, Figure 3.3.d, and filtered in producing the output pulse, Figure 3.3.e. Note how, as the main capacitor bank voltage (and, consequently, the H-bridge output voltage) droops throughout the duration of the pulse event, the H-bridge duty cycle is continuously adjusted in maintaining the average value of the module output voltage.

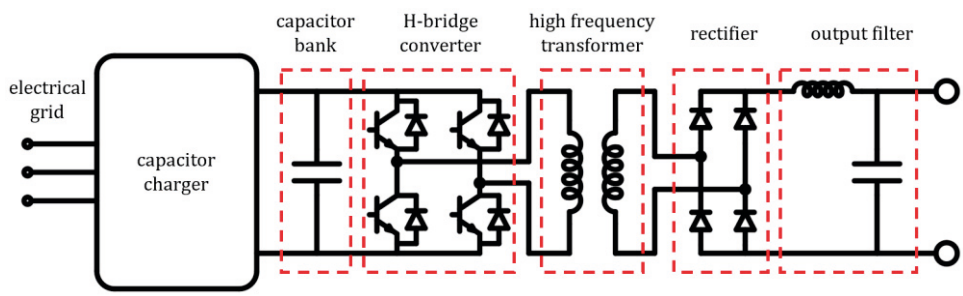



Figure 3.2: Basic pulse generation circuit based on pulse modulation-demodulation technique

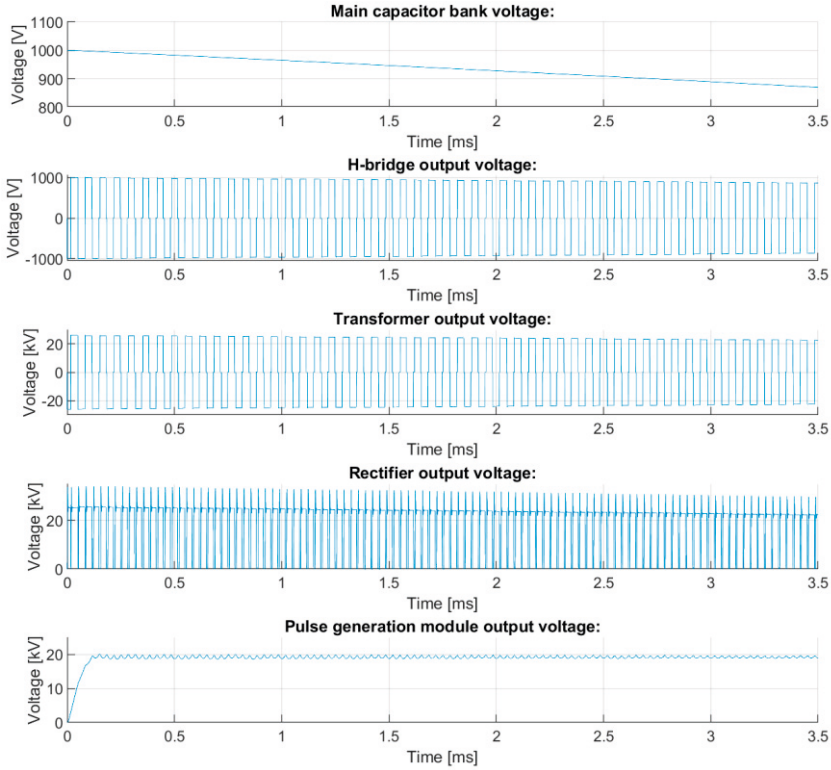



Figure 3.3: Working principle of single module of the proposed pulse generation circuit

The presented results were obtained from a single pulse generation module operated at 15 kHz and with a transformation ratio 1:26. Clearly – considering the evidently unpassable module output voltage – handling ESS application requirements with a single (or even a few) pulse generation module would be unfeasible since, e.g., 1) reducing the pulse output ripple to conform with the specified limits would require either a significant increase in H-bridge switching frequency, beyond the limits of present-day IGBT technology, [3.3], or significant reinforcement of the output filter, prohibitively degrading pulse rise time; 2) developing the described subsystems for the full power required by the ESS linac application would result in exceptional complication; and 3) the required transformation ratio (given the reliance on low voltage semiconductors) would result in extreme primary-side currents.

Instead, several such pulse generation modules may be connected in series at their respective output terminals as indicated in Figure 3.4. Here, simultaneously, the output pulse ripple and pulse rise time may be decreased. First, phase shifting the control signals of the $N_p$ pulse generation modules over 180 degrees results in analogous phase shift in the $N_p$ module output voltages. Through series connection, then, the generated ripple may be cancelled or at least significantly reduced.

Furthermore, the $N_p$ modules must clearly be designed taking into account both component and interconnection voltage drops as well as capacitor bank droop such that the required pulse flat top amplitude may be attained throughout the entire pulse event. However, during the pulse rise time, capacitor bank droop is imperceptible, Figure 3.3. Additionally, component voltage drop is generally related to the current amplitude, which is also reduced during the pulse rise time. Hence, the effective applied voltage during the pulse rise time may significantly exceed that required to produce the prescribed application voltage, substantially reducing pulse rise time.

These ideas are illustrated in Figure 3.5 and Figure 3.6. In Figure 3.5, the outputs of two pulse generation modules such as that shown in Figure 3.2 have been series connected. As shown in Figure 3.5.a, the modules independently produce output voltage waveforms comparable to that of Figure 3.3.e. However, as described, the phase shifted module control signals result in interleaving of the pulse generation module output voltages and, thereby, a significant reduction in system output voltage ripple. This principle is expanded on in Figure 3.6, where the outputs of six pulse generation modules such as that shown in Figure 3.2 have been series connected. In this case, the module input voltage of ~1 kV is amplified by the 1:26 transformer transformation ratio – taking into account capacitor bank droop and subsystem voltage drops – in generating an average module output voltage of around 19.2 kV, Figure 3.3.e and Figure 3.6.a. Hence, series connecting six such modules generate the required application voltage of 115 kV, Figure 3.6.b. Especially note, in keeping with the above, the 1) significantly improved pulse rise time, on the order of 120 μs; and the 2) considerable ripple cancellation in producing the extremely flat pulse voltage waveform.

From the above, it should be clear that modularity plays a highly important role in design, one that must be appropriately balanced with the selection of system operating frequency, output pulse quality, implications on subsystem/component design and maintainability, as well as on system size and efficiency. Design of the SML pulse generation system is discussed in detail in chapter 6.3. Also, as aforementioned, the power split between modules permits use of low voltage capacitor chargers. The features and fundamental operation of these chargers are described in the following section.

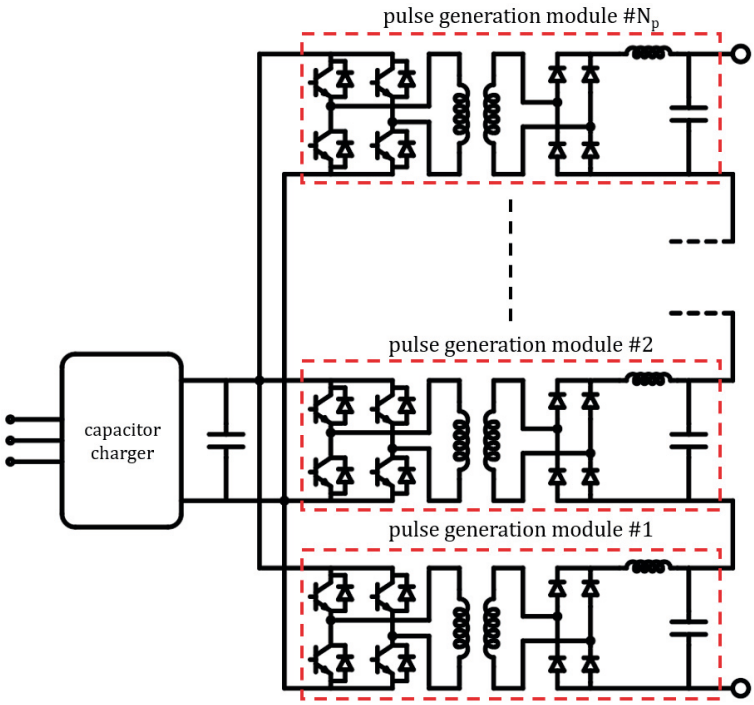



Figure 3.4: Modularity through series connection of multiple pulse generation circuits at the output

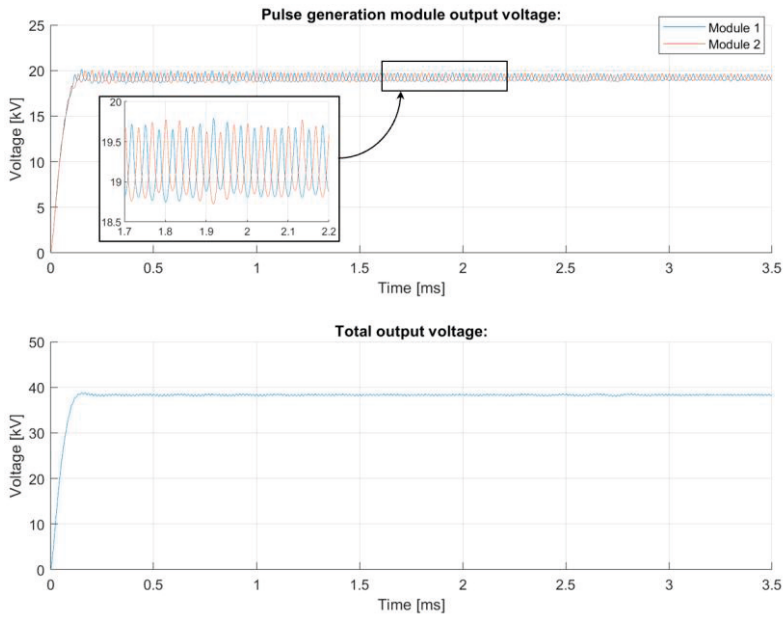



Figure 3.5: Pulse generation by two series connected output modules. Note the improved pulse quality with respect to Figure 3.3.e as a result of ripple cancellation due to module interleaving.

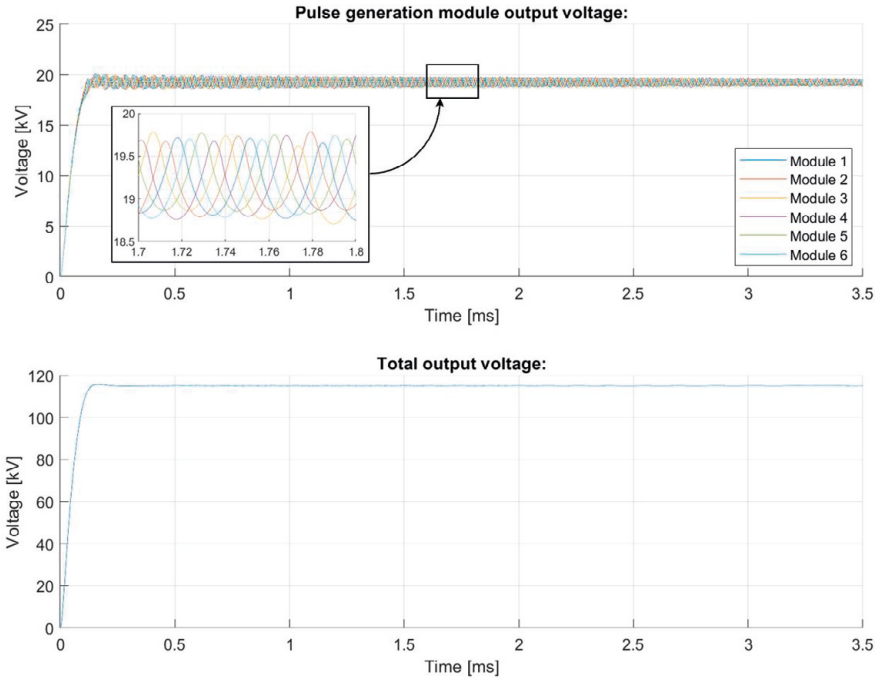



Figure 3.6: Pulse generation by six series connected output modules. Significantly improved pulse quality and pulse rise time.

### 3.2.2 Capacitor charger stage

As noted, the capacitor chargers of conventional high-power modulators are typically based on parallel connection of off-the-shelf medium-voltage capacitor chargers. Such charger systems are spacious, feature poor AC line power quality and deteriorate electrical efficiency. In keeping with section 3.2.1, this section proposes an efficient high-performance low-voltage capacitor charger.

Figure 3.7 shows the capacitor charger system connected to the $N$ pulse generation modules discussed in the above. This charger circuit is comprised of a passive LCL-type line filter, an active rectifier circuit, a dc/dc converter, and an inductive link. The charger functions as follows. The active rectifier circuit is implemented by a three-phase voltage source converter connecting the modulator system to the electrical grid via the line filter, [3.7]. Measurement of the line voltage along with the resulting line current allows for active control of the line current shape, amplitude and phase through appropriate selection of the converter output voltage. Here, knowledge of the required modulator average power and the desired dc-link voltage straightforwardly provides the necessary grid current reference. In practice, active rectifier control is implemented in a rotating reference frame in generating converter output voltage reference waveforms used in sinusoidal pulse width

modulation. A complete description of the control procedure is given in chapter 7. This procedure is indicated in Figure 3.8, where the resulting line currents are actively controlled to be sinusoidal and in-phase with the corresponding line voltage waveform whilst generating a stable dc-link voltage. The line-side filter attenuates the high frequency content of the line current waveforms generated in PWM-based switching in ensuring line current THD in accordance with applicable standards.

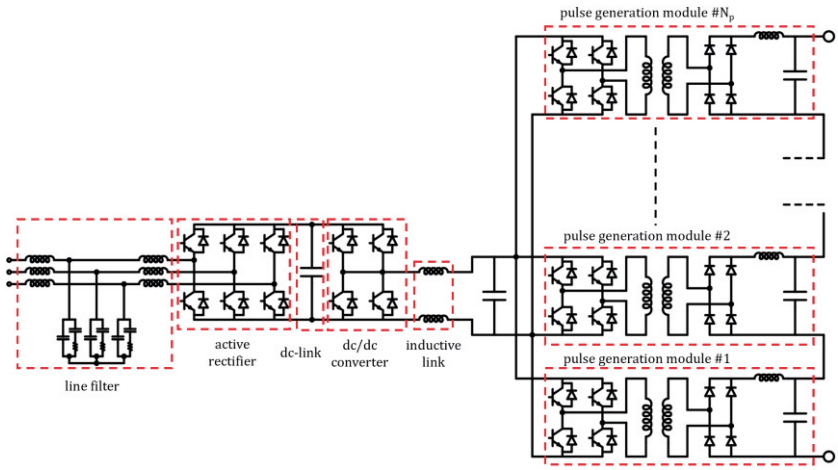



Figure 3.7: Low voltage charger configuration charging the main modulator capacitor bank energy storage powering the modulator pulse generation stage

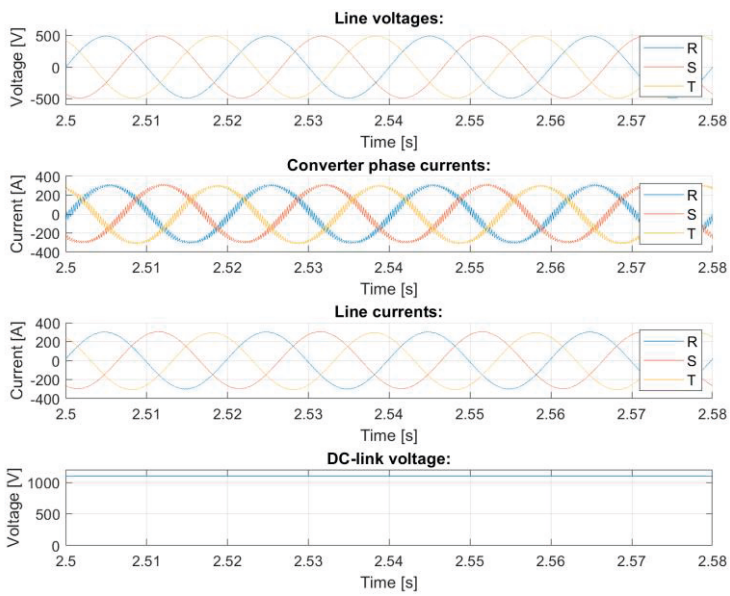



Figure 3.8: Typical active rectifier waveforms

Following the active rectifier circuit, the dc/dc converter connects the dc-link to the main capacitor bank through the inductive link, again permitting current control. Operation of the dc/dc converter is described in relation to Figure 3.9. As shown, in pulsing, energy is taken from the capacitor bank storage and supplied to the load. This energy needs to be replenished before the next pulse, and – ideally – this is done at constant rate such that constant power is drawn from the electrical grid in minimizing line flicker, [3.8]-[3.9]. Equivalently, the charging current should exhibit inverse behaviour with respect to the capacitor bank voltage waveform in a way that the required energy is replenished just in time for the next pulse. Practically, this is accomplished by setting the current reference to equal the power reference divided by the instantaneous capacitor bank voltage. Here, the required power reference is estimated from 1) the difference between the required capacitor bank voltage and the capacitor bank voltage sampled immediately following the pulse event, and 2) the period of time before the next pulse event. Additionally, a parallel integral-action controller is used in ensuring steady state performance. A complete description of this control procedure and an assessment of its robustness to changes to, e.g., requested pulse repetition rate, pulse length and pulse power is provided in chapter 7.

In summary, the proposed low voltage capacitor charger system permits constant power (flicker-free) capacitor bank charging while effectively shaping the line currents to be sinusoidal and in-phase with the corresponding line voltage waveforms in minimizing line current harmonics and reactive power, [3.8]-[3.9].

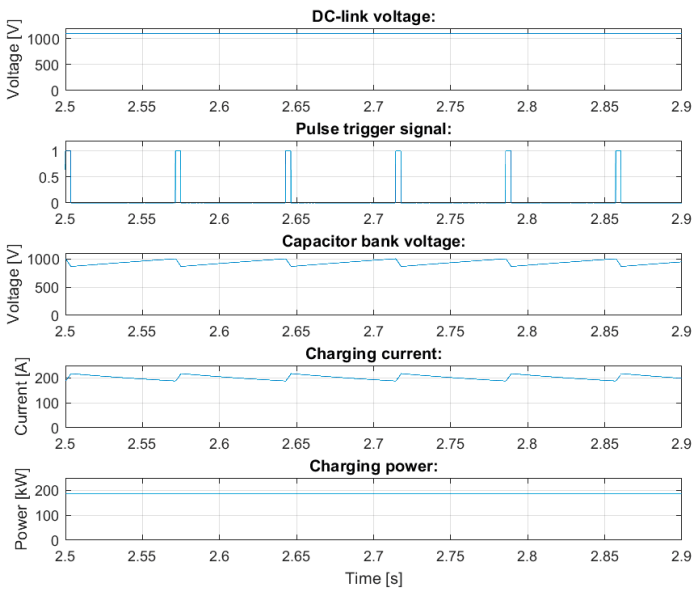



Figure 3.9: Typical dc/dc converter waveforms

Note that the above proposed charger system, Figure 3.7, may also be modularized in permitting straightforward scaling to higher average power levels. Figure 3.10 illustrates a possible arrangement of $N_c$ capacitor chargers each supplying an individual capacitor bank. Each capacitor bank supplies then a portion of the $N_p$ pulse generation modules. In practice, if desirable, the $N_c$ capacitor banks may also be connected in parallel. Here, each capacitor charger module is equipped with an individual line-side inductor. Note that this also permits phase shifting of the high frequency carrier wave used in sinusoidally pulse width modulating the active rectifier circuits. Using a common line-side filter, this results in interleaving of the generated high frequency line side current ripple, achieving significant current ripple cancellation in ensuring line current THD is within prescribed limits. This idea is exemplified in Figure 3.11 for a three-charger system.

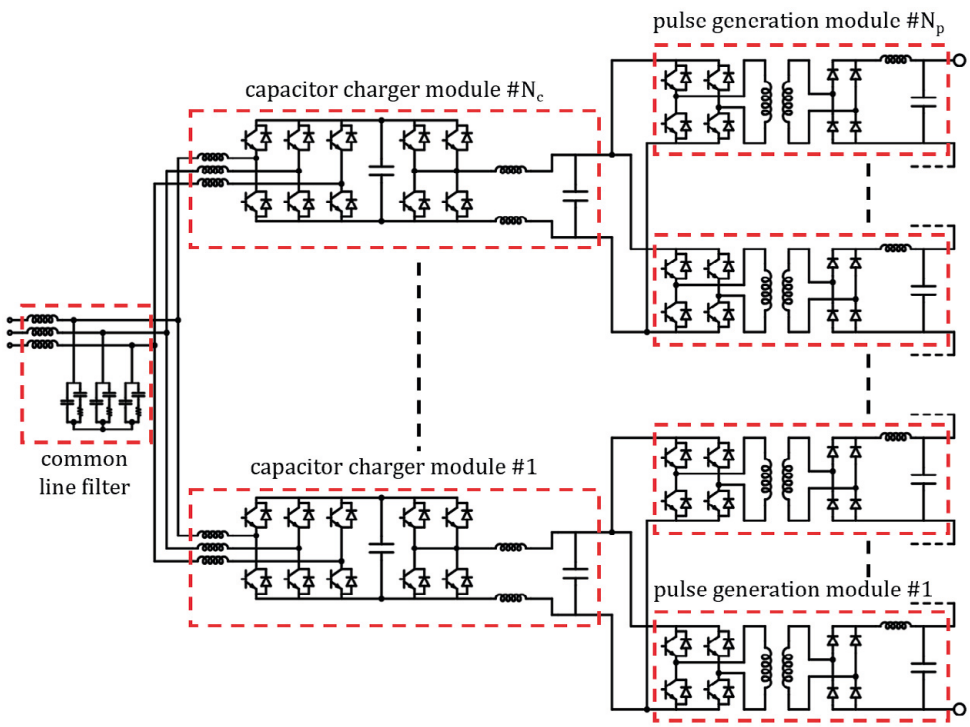



Figure 3.10: The proposed modular Stacked Multi-Level klystron modulator topology

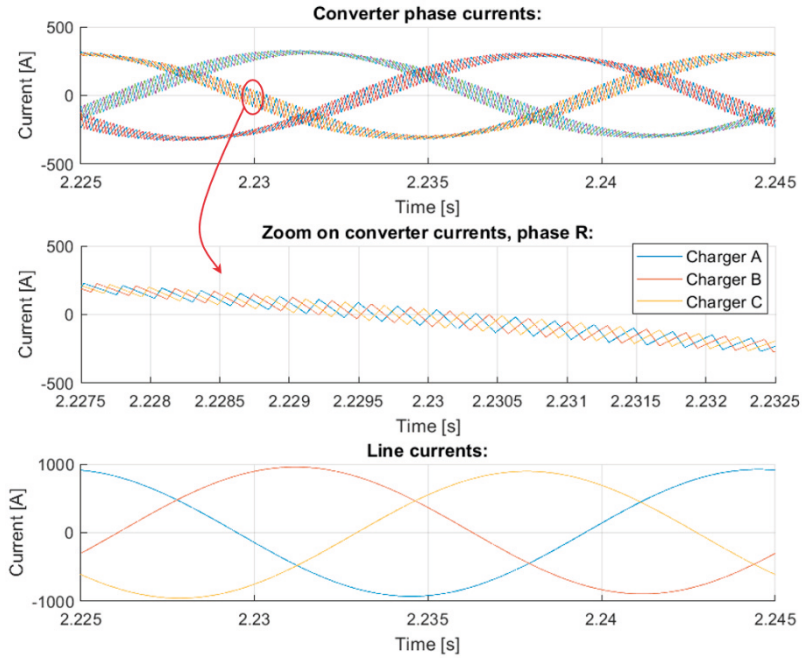



Figure 3.11: Line current ripple cancellation for sample three-charger system

## 3.3 Summary

Continuing where chapter 2 left off, this chapter begun by analysing the most pertinent limitations and difficulties in extending conventional modulator technology in suiting long pulse high power applications. Here, it was seen that – in view of present-day semiconductor technology – available modulator technology results in either 'under-modular' or 'over-modular' systems. Monolithic (or under-modular) systems generally result in large and impractical systems, with their topological simplicity being in conflict with the consolidation of pulse quality, system size, efficiency and maintainability. On the other hand, over-modular systems are impractically complex and difficult to maintain. In response, again in view of available semiconductor technology, the fundamental features and characteristics of a novel modular hard-switched converter-based modulator topology were developed.

The proposed modulator topology…

- greatly benefits from limited modularity; the use of 4…10 pulse generation modules seems appropriate.

- may suitably be based on standardized, commercial off-the-shelf low voltage semiconductor components.
- avoids placement of active components in oil tank assembly in enhancing system maintainability.
- is based on a pulse modulation/demodulation scheme, resulting in compact and efficient pulse generation modules capable of operation over a wide range of operating points.
- utilizes active front end-based capacitor chargers for flicker-free operation with minimization of generated line current harmonics and reactive power.
- features a great degree of freedom and potential for optimization in design.
- presents no inherent topological limitations to extending pulse length, pulse repetition rate or pulse power.
- permits a great degree of freedom in output pulse waveform control.

The proposed topology is treated in detail throughout the remainder of this thesis. The reader is referred to the following chapters and published literature for further information on specific topics:

- Chapter 5, [3.1] and [3.4]-[3.5] concern aspects of modeling and design optimization of SML-type modulator systems and associated components:
    - Section 5.2 focuses on the capacitor charger systems.
    - Section 5.3 focuses on the pulse generation modules.
    - Section 5.4 develops an integrated design optimization framework for SML-type modulators.
    - Section 5.5 presents a complete design optimization case study considering the ESS klystron modulator application requirements.
- Chapter 6 employs the models developed in chapter 5 in comparing the proposed modulator topology to that of the conventional pulse transformer-based modulator topology (developed in detail in chapter 4).
- Chapter 7, [3.6] and [3.8]-[3.10] treat aspects of control of SML-type modulators:
    - Section 7.1 discusses the development and assessment of the proposed constant power capacitor charging method for flicker-free modulator operation.

- Section 7.2 presents prospects in managing control of the pulse generation modules in optimizing the quality of the output pulse waveform.
- Section 7.3 studies the adaptability of the proposed SML topology in accommodating pulsing schemes with varied pulse amplitude, pulse length and pulse repetition rate.

- Chapters 8 and 9 as well as [3.1] and [3.4]-[3.5] present material related to the design, implementation and assessment of both a technology demonstrator as well as the full-scale series klystron modulators developed for the ESS linac application as based on the proposed SML topology.

## 3.4 References

[3.1] M. Collins and C. A. Martins, “Evaluation of feasibility of high-power long-pulse transformer using single-layer and pancake winding techniques,” IEEE Trans. Plasma Sci., vol. 49, no. 7, pp. 2217–2226, Jun. 2021.

[3.2] C. A. Martins, F. Bordry, and G. Simonet, “A solid state 100 kV long pulse generator for klystrons power supply,” in Proc. 13th Eur. Conf. Power Electron. Appl., Barcelona, Spain, Sep. 2009, pp. 1–10.

[3.3] A. Wintrich et al., “Application manual power semiconductors,” SEMIKRON Int. GmbH, Nuremberg, Germany, Tech. Rep., 2015, pp. 126–129. [Online]. Available: https://www.semikron.com/servicesupport/application-manual.html

[3.4] M. Collins et al, "Stacked multi-level long pulse modulator topology for ESS," in Proc. IEEE Int. Power Modulator High Voltage Conf. (IPMHVC), San Francisco, CA, USA, Jul. 2016, pp. 552–557.

[3.5] M. Collins et al., “Optimal design of a high-voltage DC/DC converter for the 11.5-MW/115-kV ESS long-pulse modulator,” IEEE Trans. Plasma Sci., vol. 48, no. 10, pp. 3332–3341, Oct. 2020.

[3.6] M. Collins and C. A. Martins, “Zero average flux tracking algorithm for high frequency transformers in long pulse applications,” in Proc. IEEE 21st Int. Conf. Pulsed Power, Brighton, U.K., Jun. 2017, pp. 1–4.

[3.7] C-C. Hou et al., “Modelling and Control of Three-Phase Active front-end Converters” in 33rd IEEE Annual Conference on Industrial Electronics, Taipei, Taiwan, 2007, pp. 1449-1454

[3.8] M. Collins and C. A. Martins, “A constant power capacitor charging structure for flicker mitigation in high power long pulse klystron modulators,” in Proc. IEEE Int. Pulsed Power Conf., Brighton, U.K., Jun. 2017, pp. 1–8.

[3.9] M. Collins and C. A. Martins, “Evaluation of a novel capacitor charging structure for flicker mitigation in high-power long-pulse modulators,” IEEE Trans. Plasma Sci., vol. 47, no. 1, pp. 985–993, Jan. 2019.

[3.10] M. Collins et al., “Evaluation of klystron modulator performance in interleaved pulsing schemes for the ESS neutrino super beam project,” in Proc. IEEE Int. Power Modulator and High Voltage Conf., Knoxville, TN, USA Jun. 2022, pp. 60-63.

# 4. Optimization of pulse transformer-based modulators

## 4.1 Introduction

The classical pulse transformer-based modulator topology was described in chapter 2. As indicated, it is one of the most common, well-established and versatile topologies for high pulse power generation. Consequently, it was selected as suitable benchmark in evaluating the developed SML modulator topology. The goal of this chapter, then, is to develop a comprehensive framework for design optimization and study of pulse transformer-based modulator systems, in particular considering (though not limited to) long-pulse high-power applications. To achieve this, each modulator component is first modelled and studied independently. Here, the European Spallation Source klystron modulator application requirements are used as a representative case to study implications in long pulse high power design. The chapter is disposed as follows-

- Section 4.2 first describes pulse transformer modeling and design. A generalized pulse transformer model is proposed and used in developing a design optimization procedure for pulse transformers. The developed optimization procedure is used in studying trends in pulse transformer design for long pulse high power applications, ultimately leading to the analytical derivation of a feasibility equation expressing the maximum attainable pulse length as a function of the application pulse parameters and system constraints.
- Section 4.3 discusses bouncer systems used for capacitor bank droop compensation. Complete design models are developed for both the classical passive LC bouncer as well as the active electronic bouncer circuit.
- Section 4.4 concerns the modulator high voltage switch assembly. Pulse transformer-based modulators for high power applications typically operate on a primary voltage of several kV, often requiring series connection of several switches. Here, a complete design procedure is developed taking into account the issues of static and dynamic voltage compensation.

- Section 4.5 treats auxiliary circuits for pulse transformer magnetic core bias and demagnetization. Complete design models are developed for both the classical passive bias and demagnetization circuit as well as the recently proposed active auxiliary circuit.
- Section 4.6 unifies the design models described in sections 4.2-4.5 in proposing an integrated framework for design and optimization of pulse transformer-based modulators.
- Finally, sections 4.7 through 4.9 describe real case studies in which the developed models and design procedures have been employed.

The developed optimization framework is employed in chapter 6 in comparing the pulse transformer-based modulator topology to that of the developed SML modulator topology.

# 4.2 Pulse transformer design

## 4.2.1 General remarks

A generic physical structure of a high voltage pulse transformer is shown in Figure 4.1. This section is focused on developing models describing the performance of transformers of this type. Discussions related to issues such as capacitor bank droop compensation, pulse transformer demagnetization and other aspects are reserved for subsequent sections. With this in mind, the pulse transformer shown in Figure 4.1 is considered from the perspective of an equivalent two-port network. Here, the IEEE standard for pulse transformers describes the following equivalent circuit, Figure 4.2 [4.1].

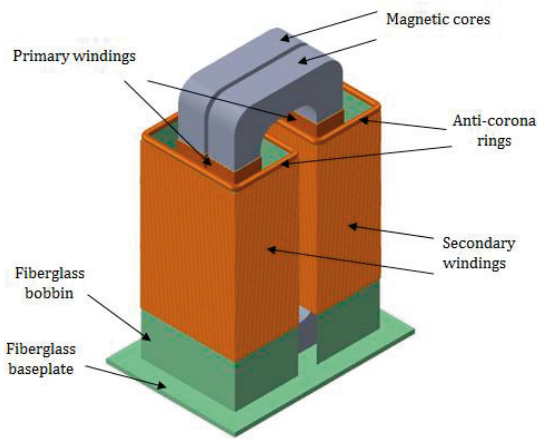



Figure 4.1: Generic high voltage pulse transformer geometry

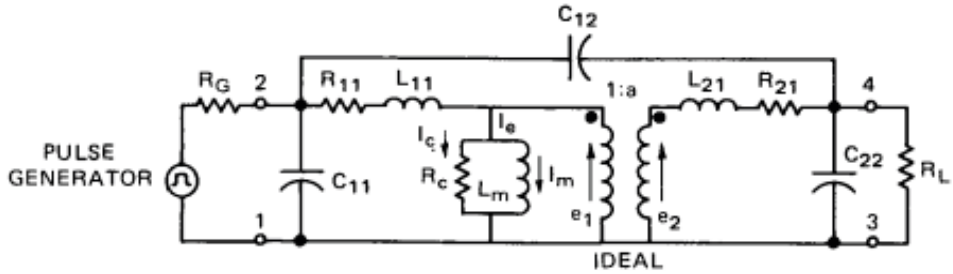



Figure 4.2: Complete generalized equivalent circuit of pulse transformer [4.1]

In this circuit, the input terminals - 1 and 2 - are connected to a pulsed voltage source with internal resistance $R_g$ representing the resistive drop of, e.g., the high voltage switch assembly and the ESR of the capacitor bank. The pulsed source generates an ideal rectangular waveform of pulse length $T_p$ and amplitude $V_p$. The output terminals of the pulse transformer - 3 and 4 - are connected to the load $R_L$. The elements in this equivalent circuit are defined as follows-

- $R_{11}$ and $R_{21}$ are the winding resistances of the primary and secondary windings, respectively.
- $L_{11}$ and $L_{21}$ are lumped inductive elements representing the effects of the leakage flux in the pulse transformer.
- $R_m$ is a resistive element representing the core losses of the pulse transformer.
- $L_m$ is the magnetizing inductance of the pulse transformer.
- $C_{11}$ represents the stray capacitance between the primary side of the pulse transformer and ground, i.e., the primary winding(s) and the transformer core.
- $C_{12}$ represents the stray capacitance between the two sides of the transformer, i.e., generally the capacitance between the primary and secondary windings.
- $C_{22}$ represents the stray capacitance between the secondary side of the pulse transformer and ground, i.e., typically the secondary winding and the oil tank body.

From the perspective of high-voltage high-power engineering, the following statements can be made-

- The output voltage is typically much greater than the input voltage, i.e., at least ~20 times higher. The stored energy in stray capacitance $C_{11}$ is therefore relatively speaking very small and may be neglected.
- Due to the great potential difference between the primary and the secondary, the capacitance $C_{12}$ is well approximated by a capacitance of equal value instead placed between secondary and ground, i.e., in parallel with capacitance $C_{22}$.
- The load current is much greater than the magnetization current, i.e., the leakage inductances may be grouped to a single series inductor $L_s$. As will be seen, it is convenient to place this inductor on the secondary side of the equivalent circuit.

Consequently, despite the fact that pulse transformers may be implemented in a variety of ways, analysis and design may generally be split into two distinct parts, one related to transformer core magnetization and one related to transformer loading, Figure 4.3.

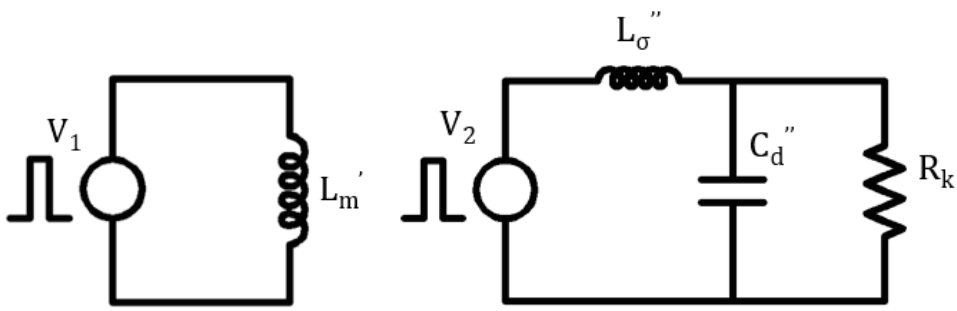



Figure 4.3: Simplified circuits for use in pulse transformer design- a) magnetization of pulse transformer; b) pulse output circuit.

*Magnetization - satisfying the voltage-time integral*

As the high-voltage switch assembly is closed, the source voltage is applied to the primary winding of the pulse transformer. Assuming proper droop compensation, the applied voltage is well approximated by an ideal DC source and the resulting magnetization flux may conveniently be considered from the perspective of the secondary of the transformer as given by (4.1) and shown in Figure 4.3. Here, $V_2$ is the output voltage of the transformer, $k_{fe}$is the magnetic fill factor, $A_{fe}$ is the magnetic cross-sectional area of the core, $B_{max}$ is the maximum peak magnetic flux

density, and $T_p$ is the length of the applied pulse. Some, though not all, applications permit series connection of the secondary windings. This possibility is described by the factor $k_w$, representing either the series ($k_w = 2$) or parallel ($k_w = 1$) connection of the secondary windings. In addition, as shown in Figure 4.4, negatively pre-magnetizing (biasing) the core allows a larger flux swing. Here, this is represented by the factor $k_b$, ranging between 1 and 2.

$$V_2 = k_w N_2 \frac{d\emptyset}{dt} = k_w k_{fe} A_{fe} N_2 \frac{\Delta B}{T_p} = k_w k_b k_{fe} A_{fe} N_2 \frac{B_{max}}{T_p}$$
$$\rightarrow N_2 A_{fe} k_w k_b \geq \frac{V_2 T_p}{k_{fe} B_{max}} \tag{4.1}$$

It is pointed out that $V_2$ and $T_p$ are generally given by the application. Furthermore, parameters $B_{max}$ and $k_{fe}$ depend on the selected core material. For high voltage high power applications, tape wound C cores are invariably used due to 1) the required transformer size, and 2) being suitable for long core leg designs allowing low leakage inductance. For such cores, $B_{max}$ may practically be taken to be ~1.2 T and $k_{fe}$to be ~0.9 [4.2]. Hence, the product of the transformer number of turns and magnetic cross-sectional area must be appropriately chosen to be larger than a number determined by the application.

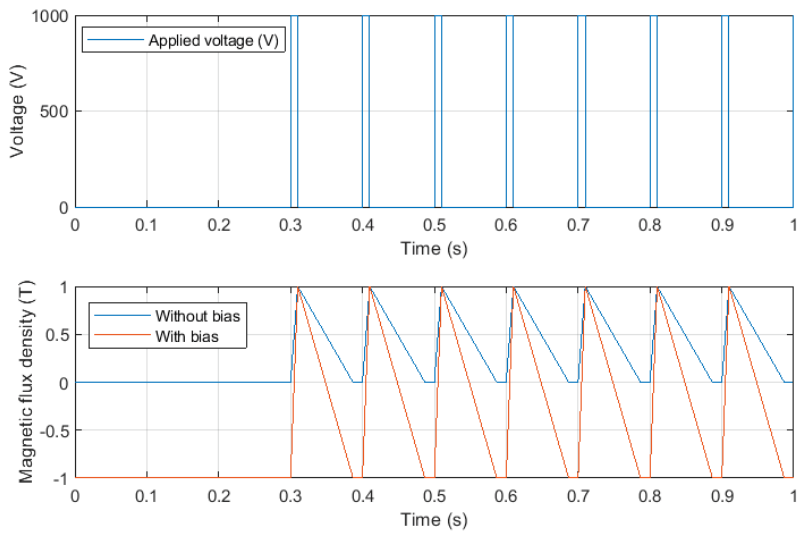



Figure 4.4: Pulsed source with amplitude 1 kV, pulse length 10 ms and repetition rate 10 Hz excites a magnetic core to 1 T. Biasing the core allows doubling the magnetic flux swing.

*Loading - compliance with pulse performance requirements*

The selected turns-area product together with requirements on high voltage isolation essentially define a complete pulse transformer geometry. As indicated in Figure 4.2 and Figure 4.3, the magnetic coupling between the windings is non-ideal, i.e., part of the generated magnetic flux does not fully link both winding geometries. The stored energy in this part of the flux may be related to an equivalent leakage inductance $L_s$. Similarly, the energy stored in the generated electric field between 1) the winding geometries, 2) the winding geometries and the magnetic core, and 3) the winding geometries and the oil tank body (as well as other components) may be related to an equivalent stray capacitance $C_d$. The resulting RLC circuit, Figure 4.3.b, represents a second order system with damping factor given by (4.2). Clearly, all aspects of the resulting output pulse and the corresponding pulse performance are strongly and directly influenced by the parasitic elements, Figure 4.5.

$$\zeta = \frac{1}{2R}\sqrt{\frac{L_\sigma}{C_d}} \tag{4.2}$$

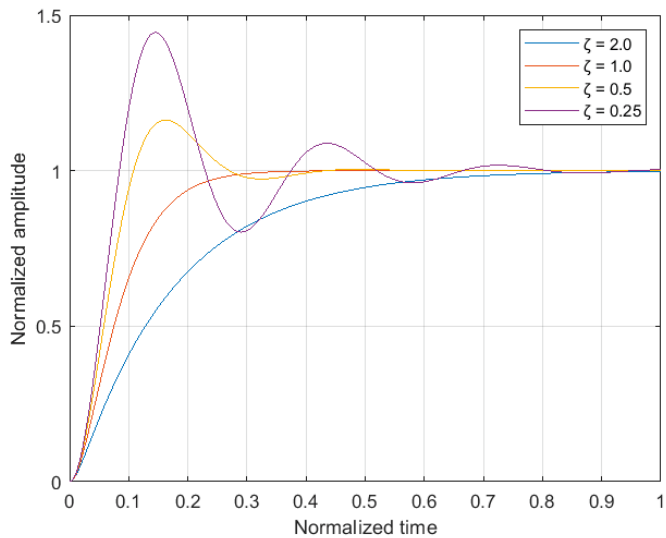



Figure 4.5: Normalized output pulse as function of damping

*Summary*

This preliminary discussion on the features of high voltage high power pulse transformers has shown that, from a functional perspective, the transformer number of turns and magnetic cross sectional area must be carefully selected to 1) satisfy

the voltage-time integral condition, and to 2) ensure that the parasitic elements associated with the resulting transformer geometry together with the application load impedance represent a circuit with a transient response appropriately matching the specified pulse requirements, e.g. pulse rise time and maximum pulse overshoot. While it is clear that many combinations of these design parameters can satisfy these functional requirements, these solutions may be very different in terms of transformer extents volume, transformer weight, efficiency, and so on. Furthermore, aspects of reliability and maintainability must be considered.

### 4.2.2 Pulse transformer modeling

The complete expression describing magnetization of the pulse transformer core was established in the previous section, (4.1). To ensure that the generated output pulse matches the specified pulse performance requirements, accurate models linking the transformer geometry to estimates of the parasitic elements are needed.

An overview of the basic pulse transformer geometry is shown in Figure 4.6 and Figure 4.7. As mentioned in the previous section, the transformer core is generally made up of tapewound double C cores. The primary windings are low voltage windings wound around a bobbin placed closely around the magnetic core. The secondary windings are high voltage windings and must, given the large potential difference, be physically separated from the primary windings, the transformer core, the oil tank body as well as from other components. Geometrically, the secondary windings may be conic or parallel. Additionally, parallel windings may be wound either in a single layer, in multiple layers or in a sequence of interconnected stacks termed pancakes. Further note that if the secondary windings are series connected the two secondary windings may be sized independently within the limits of high voltage isolation to manipulate the resulting equivalent parasitic elements.

In the following, generalized analytical models for calculating the parasitic elements associated with transformers using the parallel and the conic secondary winding geometries will be developed. Then, the particularities of the different winding techniques are worked out such that the performance of a given design, i.e., chosen transformer geometry wound with a given winding technique, may readily be estimated. It is noted that other variations are possible, e.g., transformers with multiple input- and/or output circuits may be considered. These are not treated in detail but follow as a straightforward extension of the developed models.

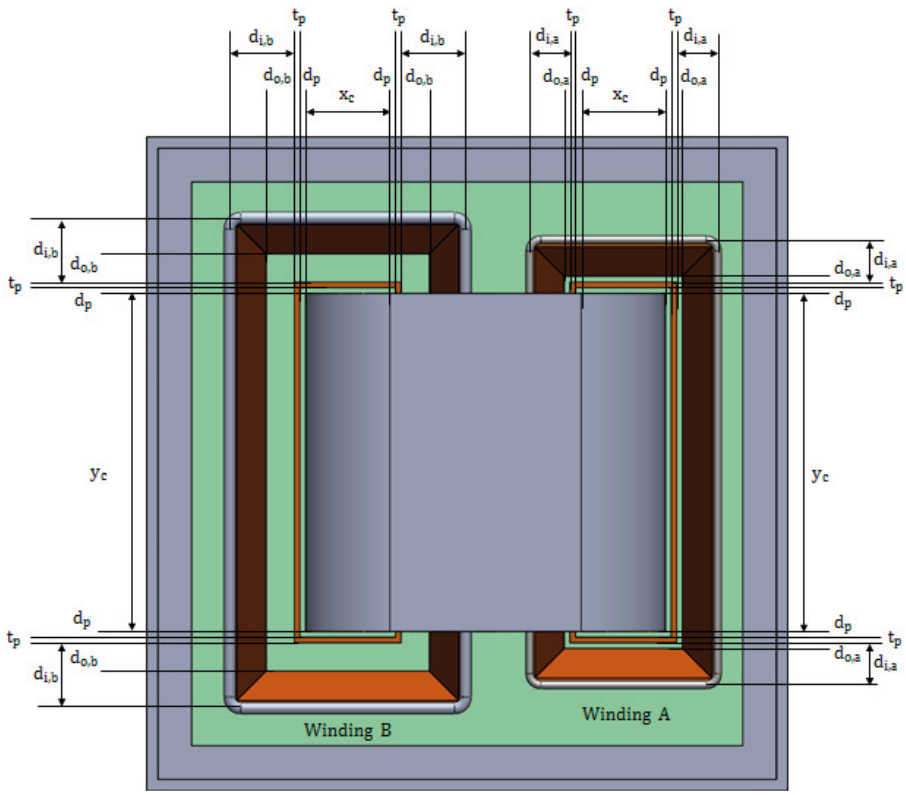



Figure 4.6: Definition of pulse transformer geometry, top-down view

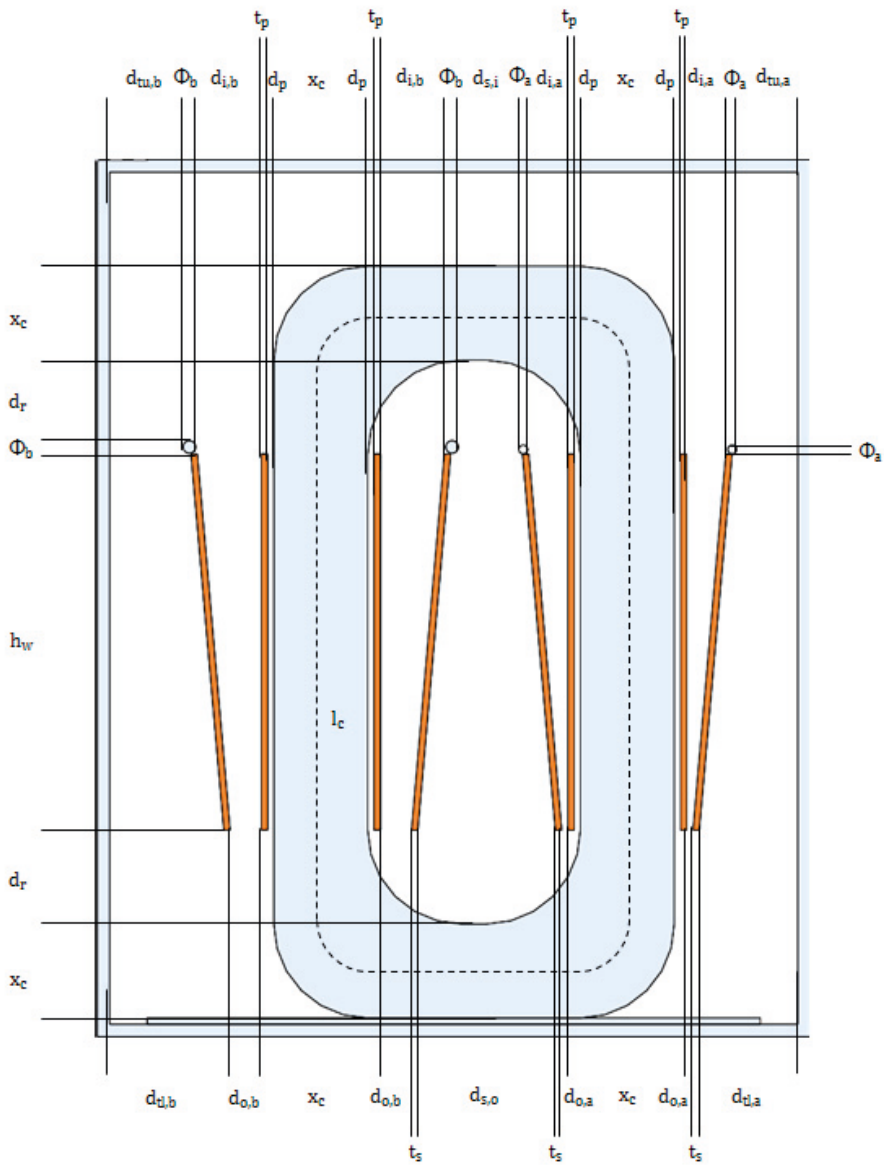



Figure 4.7: Definition of pulse transformer geometry, front view

### 4.2.3 Estimation of stray capacitance

The lumped capacitive elements shown in Figure 4.2 are related to the energy stored in the generated electric field within and surrounding the pulse transformer geometry. As such, methods presented in literature typically model the electric field as a function of geometry and applied voltages, integration of which yields the stored energy used in calculation of the corresponding capacitances, (4.3). As mentioned, in high voltage applications $V_s \gg V_p$ and a single lumped capacitor generally well approximates the entirety of stray capacitive effects, (4.4).

$$W_e = \frac{1}{2}\varepsilon_0\varepsilon_r \int\int\int \vec{E}\, dxdydz = \frac{1}{2}C_d V_2^2 \tag{4.3}$$

$$C \sim \frac{2\sum_n W_{e,n}}{V_2^2} \tag{4.4}$$

Here, finite element method-based field calculations are often favoured because of their broad applicability and good accuracy [4.3]-[4.4]. However, direct inclusion of such procedures in optimization routines significantly increases runtime, especially when considering parameter sweeping. In literature, only a few articles study the problem of analytical estimation of parasitic elements in high voltage pulse transformer structures. [4.5] develops analytical models for calculation of stray capacitance and leakage inductance, but considers only the stored energy between the primary and secondary windings, i.e., the electric field between, e.g., secondary windings and oil tank walls is neglected. Furthermore, some of the presented results appear unphysical, e.g., increasing stray capacitance with increasing winding separation. [4.6] presents a rather complete treatment of parasitic capacitance calculation. However, all calculations implicitly assume parallel connected secondary windings. In practice, series connected secondary windings are common, producing a different field picture in some of the studied regions. In addition, no details on the calculation of leakage inductance are presented.

These sections aim to present a complete generalization of pulse transformer equivalent circuit parameter modeling in the context of high voltage high power applications. In this regard, Figure 4.8 and Figure 4.9 again depict the generic pulse transformer geometry, here subdivided into eight regions that may be categorized using six distinct region types. In the following, some of the stray capacitance calculations presented in [4.6] are reviewed and generalized for the geometry of Figure 4.8 and Figure 4.9, including the possibility of series connected secondary windings. The relationship between parallel and conic windings is also discussed.

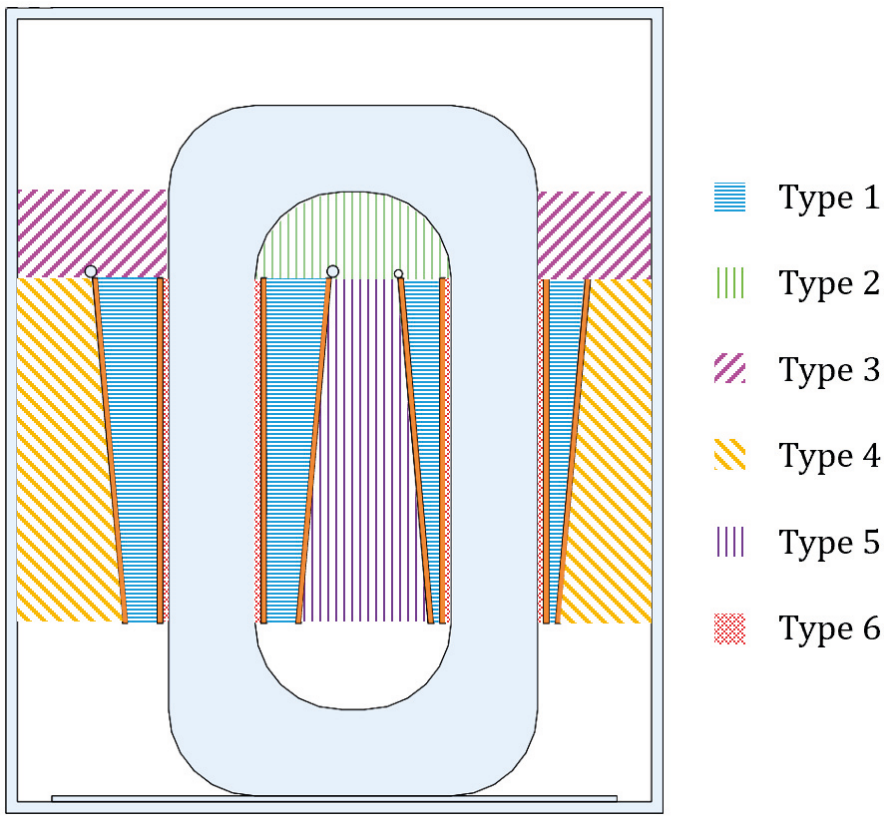



Figure 4.8: Front view of pulse transformer indicating regions used for calculation of lumped stray capacitance element

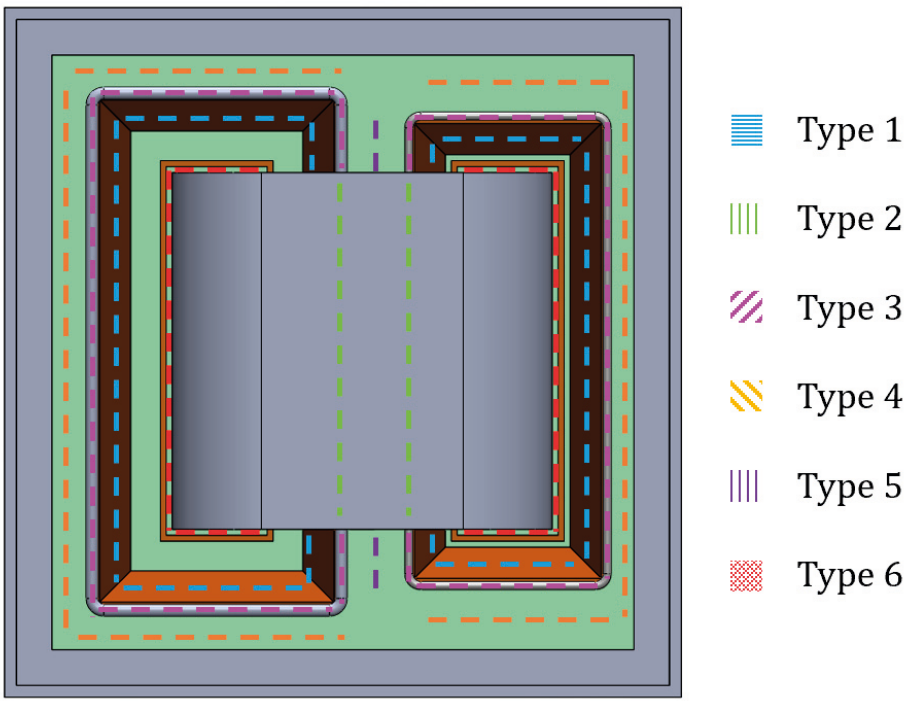



Figure 4.9: Top view of pulse transformer indicating paths used for calculation of lumped stray capacitance element

*Calculation of energy between the secondary and primary windings (region type 1)*

This region type represents the volume between primary and secondary windings. To calculate the energy stored in this volume, the simplified geometry depicted in Figure 4.10 is used. Since $d_i$ is typically much greater than the thickness of the isolator and $\varepsilon_{oil} \cong \varepsilon_{iso}$, the impact of the isolator may be neglected.

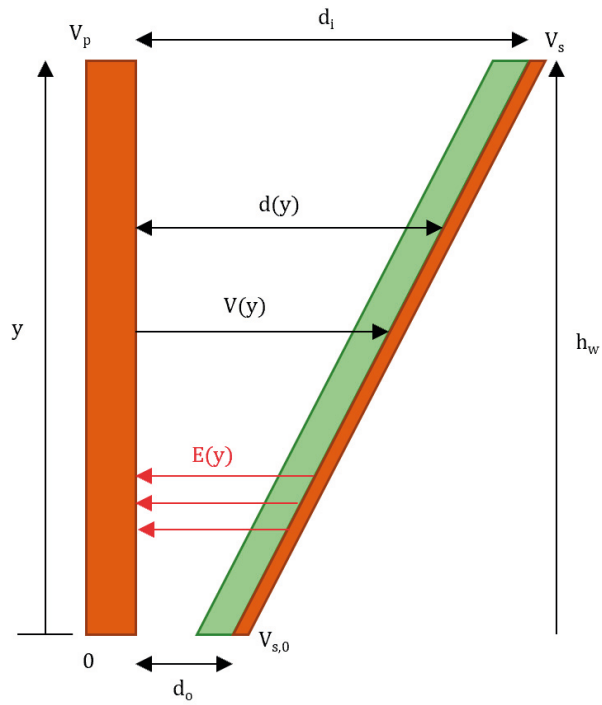



Figure 4.10: Geometry used in estimating stored energy in winding region type 1

The windings are modelled as plates with linear voltage distribution. The low side of the primary winding is generally grounded and increases linearly towards $V_p$ at the top. The low side of the secondary winding begins at $V_{s,0}$ and increases towards $\hat{V}_s$ at the top. Consequently, the potential difference between the two windings as a function of spatial dimension $y$ may be written as (4.5). Similarly, the distance between the two windings as a function of $y$ is written as (4.6). Again, as the secondary voltage generally is much higher than the primary voltage, the primary voltage is most usually omitted from these calculations for simplicity.

$$V_s(y) = V_{s,0} + \left(\hat{V}_s - V_{s,0}\right)\frac{y}{h_w} \tag{4.5}$$

$$d(y) = d_0 + (d_i - d_0)\frac{y}{h_w} \tag{4.6}$$

Assuming that the resulting electric field lines run straight from the secondary winding to the primary winding, i.e., orthogonally to the primary winding, the electric field may be estimated from (4.7). Then, the stored energy is given by (4.8).

$$\left|\vec{E}(y)\right| = \frac{V_s(y)}{d(y)} = \frac{V_{s,0} + \left(\hat{V}_s - V_{s,0}\right)\frac{y}{h_w}}{d_0 + (d_i - d_0)\frac{y}{h_w}} = \frac{V_{s,0}h_w + \left(\hat{V}_s - V_{s,0}\right)y}{d_0 h_w + (d_i - d_0)y} \tag{4.7}$$

$$W_e = \frac{1}{2}\varepsilon_0\varepsilon_r \int_0^{d_0+(d_i-d_0)\frac{y}{h_w}} \int_0^{h_w} \int_0^{l_{R1}} \left(\frac{V_{s,0}h_w + \left(\hat{V}_s - V_{s,0}\right)y}{d_0 h_w + (d_i - d_0)y}\right)^2 dxdydz \tag{4.8}$$

The first part of this integral is given by (4.9). Then, integration over $z$ corresponds to multiplication of $l_{R1}$, (4.10), i.e., the stored energy is calculated by the integral shown in (4.11).

$$\int_0^{d_0+(d_i-d_0)\frac{y}{h_w}} \left(\frac{V_{s,0}h_w + \left(\hat{V}_s - V_{s,0}\right)y}{d_0 h_w + (d_i - d_0)y}\right)^2 dx = \frac{\left(V_{s,0}h_w + \left(\hat{V}_s - V_{s,0}\right)y\right)^2}{d_0 h_w + (d_i - d_0)y}\frac{1}{h_w} \tag{4.9}$$

$$\int_0^{l_{R1}} \frac{\left(V_{s,0}h_w + \left(\hat{V}_s - V_{s,0}\right)y\right)^2}{d_0 h_w + (d_i - d_0)y}\frac{1}{h_w}dz = \frac{l_{R1}}{h_w}\frac{\left(V_{s,0}h_w + \left(\hat{V}_s - V_{s,0}\right)y\right)^2}{d_0 h_w + (d_i - d_0)y} \tag{4.10}$$

$$W_e = \frac{1}{2}\varepsilon_0\varepsilon_r \frac{l_{R1}}{h_w}\int_0^{h_w} \frac{\left(V_{s,0}h_w + \left(\hat{V}_s - V_{s,0}\right)y\right)^2}{d_0 h_w + (d_i - d_0)y} \tag{4.11}$$

This integral is of the type described by (4.12). Substituting the values of (4.13) into (4.12) and simplifying yields the final expression shown in (4.14).

$$\begin{aligned}&\int_0^n \frac{(a+by)^2}{c+ey}dy \\ &= \frac{\left[\begin{matrix} b^2e^2n^2 + 4abe^2n - 2b^2cen + 2a^2e^2\ln(en+c) + 4abceln(c) \\ -2a^2e^2\ln(c) + 2b^2c^2\ln(en+c) - 4abceln(en+c) - 2b^2c^2\ln(c)\end{matrix}\right]}{2e^3}\end{aligned} \tag{4.12}$$

$$\begin{Bmatrix} a = V_{s,0} h_w \\ b = (\hat{V}_s - V_{s,0}) \\ c = d_0 h_w \\ e = (d_i - d_0) \\ n = h_w \end{Bmatrix} \tag{4.13}$$

$$W_e = \frac{1}{4}\varepsilon_0 \varepsilon_r \frac{l_{R1} h_w}{(d_i - d_0)^3} \Bigg[ (d_i - d_o)(\hat{V}_s - V_{s,0}) \big[ d_i (\hat{V}_s + 3V_{s,0}) - d_o (V_{s,0} + 3\hat{V}_s) \big] - 2ln\left(\frac{d_i}{d_o}\right) \left[ \hat{V}_s d_i - V_{s,0} d_o \right] \Bigg] \tag{4.14}$$

*Calculation of energy close to corona ring, inside winding window (region type 2)*

In [4.6], this region was modelled as a coaxial structure as shown in Figure 4.11. In this case, the electrical energy is given by (4.15).

$$W_e = \frac{\pi}{4}\varepsilon_0 \varepsilon_r l_{R2} \frac{{\hat{V}_s}^2}{ln\left(1 + \frac{2d_i}{k_2 \emptyset}\right)} \tag{4.15}$$

However, this simplification is clearly only possible for parallel connected secondary windings. For series connected secondary windings, the corona rings are at different potentials and are furthermore placed at a non-negligible distance from one another. In this case, the complete field distribution may instead be estimated using the superposition principle. Here, the field between each corona ring and the magnetic core is seen as one fourth of a coaxial structure, whereas the field between the corona rings may be expressed as the field generated between two parallel rods, Figure 4.11.b. In this case, the stored electrical energy is given by (4.16).

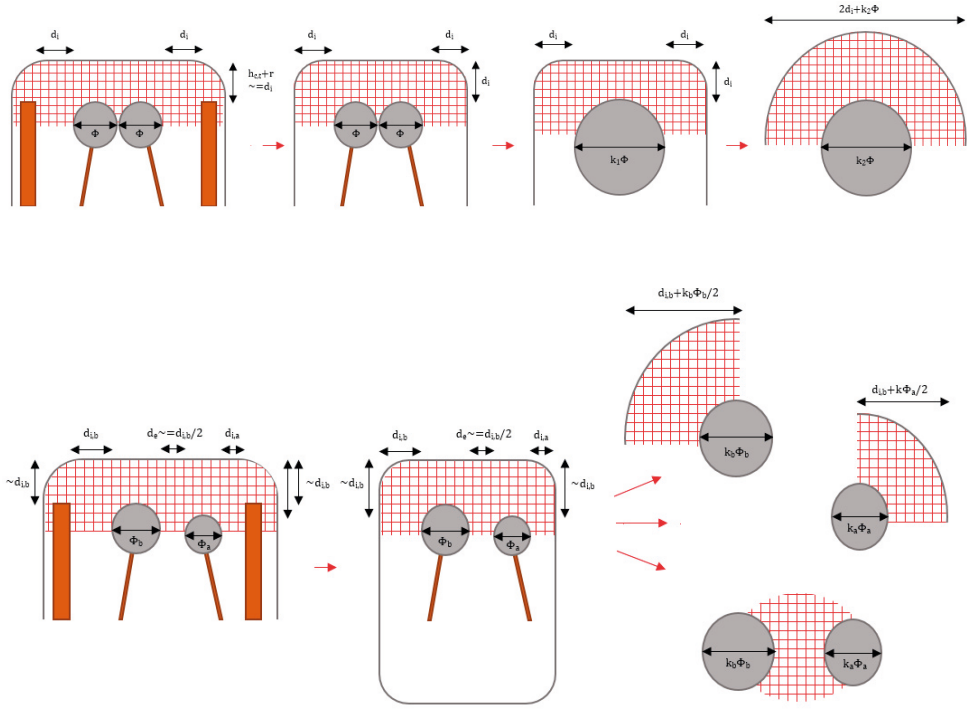



Figure 4.11: Geometry used in estimating stored energy in winding region type 2- a) parallel connected secondary windings; b) series connected secondary windings

$$W_e = \frac{\pi}{2}\varepsilon_0\varepsilon_r l_{R2}\left[\frac{1}{4}\frac{\hat{V}_{s,a}{}^2}{ln\left(1+\frac{2d_{i,a}}{k_a\emptyset_a}\right)}+\frac{1}{4}\frac{\hat{V}_{s,b}{}^2}{ln\left(1+\frac{2d_{i,b}}{k_b\emptyset_b}\right)}+\frac{\left(\hat{V}_{s,b}-\hat{V}_{s,a}\right)^2}{\ln(2)+ln\left(1+\frac{d_{i,b}}{k_b\emptyset_b+k_a\emptyset_a}\right)}\right] \tag{4.16}$$

*Calculation of energy close to corona ring, outside winding window (region type 3)*

In [4.6], this region was modelled as a coaxial structure, Figure 4.12, with the electrical energy given by (4.17).

$$W_e = \frac{\pi}{2}\varepsilon_0\varepsilon_r l_{R3}\frac{\hat{V}_s{}^2}{\ln\left(1+\frac{2d_i}{k_3\emptyset}\right)} \tag{4.17}$$

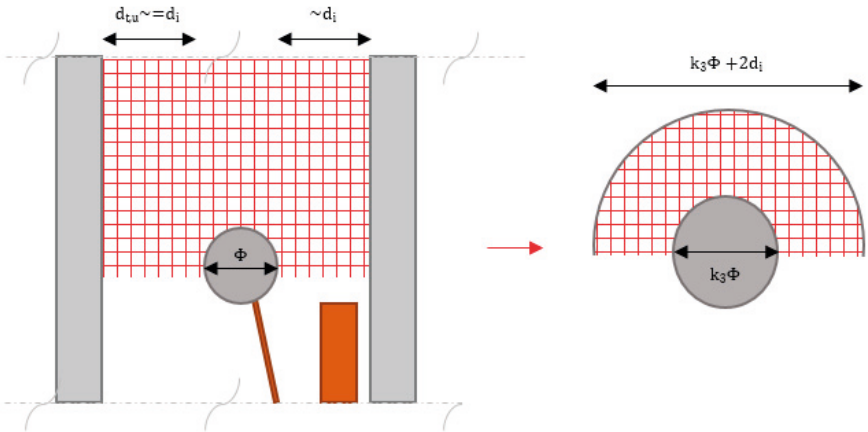



Figure 4.12: Geometry used in estimating stored energy in winding region type 3

*Calculation of energy between secondary winding and oil tank body (region type 4)*

This region is clearly very similar to that of region R1. Following the definitions outlined in Figure 4.13 and (4.18)-(4.19), the integral described by (4.20) is obtained. This is an integral of the same type as that presented in (4.11) for R1. Consequently, the electrical energy may be calculated from (4.21).

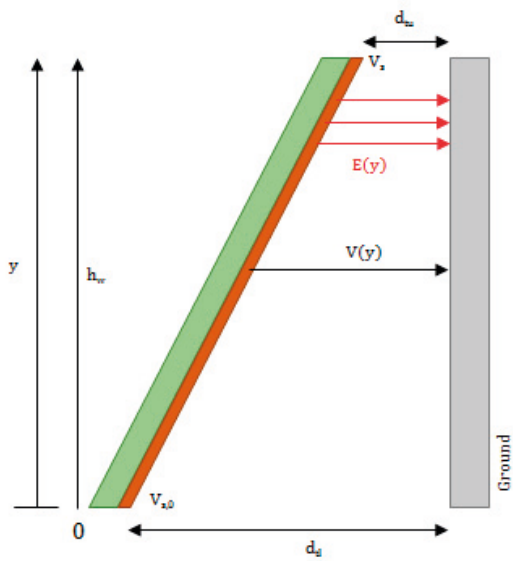



Figure 4.13: Geometry used in estimating stored energy in winding region type 4

$$V_s(y) = V_{s,0} + \left(\hat{V}_s - V_{s,0}\right)\frac{y}{h_w} \tag{4.18}$$

$$d(y) = d_{t,l} - \left(d_{t,l} - d_{t,u}\right)\frac{y}{h_w} = d_{t,l} + \left(d_{t,u} - d_{t,l}\right)\frac{y}{h_w} \tag{4.19}$$

(4.20)

$$W_e = \frac{1}{4}\varepsilon_0\varepsilon_r \frac{l_{R4}h_w}{\left(d_{t,u} - d_{t,l}\right)^3}\Bigg[\left(d_{t,u} - d_{t,l}\right)\left(\hat{V}_s - V_{s,0}\right)\left[d_{t,u}\left(\hat{V}_s + 3V_{s,0}\right) - d_{t,l}\left(V_{s,0} + 3\hat{V}_s\right)\right] - 2ln\left(\frac{d_{t,u}}{d_{t,l}}\right)\left[\hat{V}_s d_{t,u} - V_{s,0}d_{t,l}\right]\Bigg] \tag{4.21}$$

*Calculation of energy between secondary windings (region type 5)*

In [4.6], the geometry shown in Figure 4.14.a was considered. For parallel connected secondary windings, the generated field will clearly point downwards. Under the assumption that the generated field lines run in parallel to the primary windings, the electric field may be approximated from (4.22). Note that the accuracy of this approximation worsens progressively as $d_i$ approaches $d_o$. On the other hand, as mentioned in [4.6], the stored electrical energy is relatively low due to 1) the limited volume and 2) the low stored energy density and may therefore often be neglected.

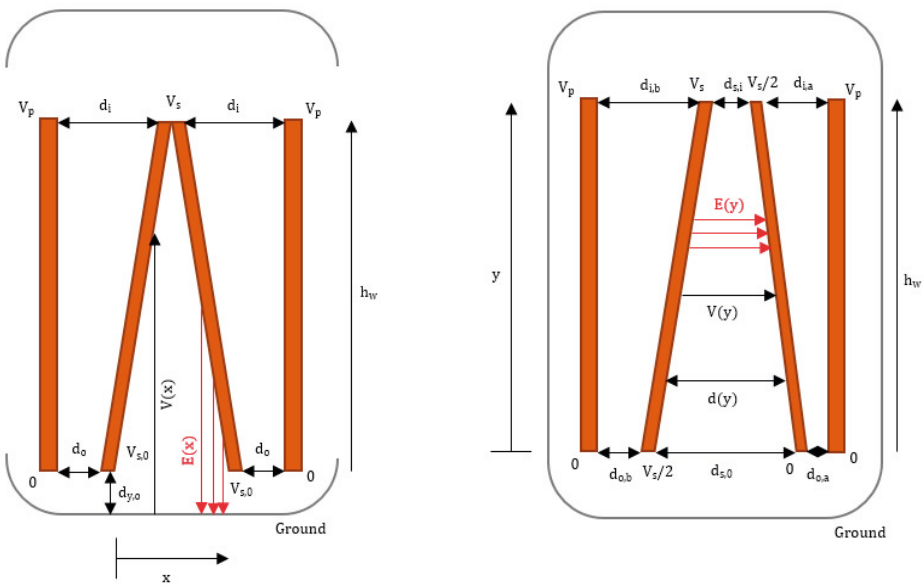



Figure 4.14: Geometry used in estimating stored energy in winding region type 5-a) parallel connected secondary windings; b) series connected secondary windings.

The stored electrical energy is then given by (4.23). The first part of this integral is given by (4.24). Then, integration over $z$ corresponds to multiplication of $l_{R5}$, (4.25), i.e., the stored energy is calculated by the integral shown in (4.26).

$$\left|\vec{E}(x)\right| = \frac{V(x)}{d(x)} = \frac{\frac{x}{d_i - d_o}\hat{V}_s}{d_{y,0} + x\frac{h_w}{d_i - d_o}} = \frac{x\hat{V}_s}{d_{y,0}(d_i - d_o) + xh_w} \tag{4.22}$$

$$W_e = \frac{1}{2}\varepsilon_0\varepsilon_r \int_0^{d_i - d_0} \int_0^{d_{y,0} + x\frac{h_w}{d_i - d_o}} \int_0^{l_{R5}} \left(\frac{x\hat{V}_s}{d_{y,0}(d_i - d_o) + xh_w}\right)^2 dxdydz \tag{4.23}$$

$$\int_0^{d_{y,0} + x\frac{h_w}{d_i - d_o}} \left(\frac{x\hat{V}_s}{d_y(d_i - d_o) + xh_w}\right)^2 dy = \frac{\left(x\hat{V}_s\right)^2}{d_{y,0}(d_i - d_o) + xh_w}\frac{1}{(d_i - d_o)} \tag{4.24}$$

$$\int_0^{l_{R5}} \frac{\left(x\hat{V}_s\right)^2}{d_{y,0}(d_i - d_o) + xh_w}\frac{1}{(d_i - d_o)}dz = \frac{l_w}{(d_i - d_o)}\frac{\left(x\hat{V}_s\right)^2}{d_{y,0}(d_i - d_o) + xh_w} \tag{4.25}$$

$$W_e = \frac{1}{2}\varepsilon_0\varepsilon_r \frac{l_{R5}}{(d_i - d_o)}\hat{V}_s{}^2 \int_0^{d_i - d_0} \frac{x^2}{d_{y,0}(d_i - d_o) + xh_w}dx \tag{4.26}$$

This integral is of the type described by (4.27). Substituting the values of (4.28) into (4.27) and simplifying yields the final expression shown in (4.29).

$$\int_0^n \frac{x^2}{a + bx}dx = \frac{2a^2(ln(a + bn) - \ln(a)) + b^2n^2 - 2abn}{2b^3} \tag{4.27}$$

$$\left\{\begin{matrix} a = d_{y,0}(d_i - d_o) \\ b = h_w \\ n = d_i - d_0 \end{matrix}\right\} \tag{4.28}$$

$$W_e = \frac{1}{2}\varepsilon_0\varepsilon_r \frac{l_{R5}(d_i - d_o)}{h_w{}^3}\hat{V}_s{}^2 \cdot \left[d_{y,0}{}^2\left[ln\left(d_{y,0} + h_w\right) - \ln\left(d_{y,0}\right)\right] + \frac{1}{2}h_w{}^2 - d_{y,0}h_w\right] \tag{4.29}$$

Conversely, for series connected secondary windings, the generated electric field runs between the two secondary windings, orthogonal to the primary winding, Figure 4.14.b and (4.30)-(4.32).

$$\Delta V(y) = V_{s,2}(y) - V_{s,1}(y) = \left(\hat{V}_s/2 + \hat{V}_s/2\frac{y}{h_w}\right) - \left(0 + \hat{V}_s/2\frac{y}{h_w}\right) = \hat{V}_s/2 \tag{4.30}$$

$$d(y) = d_0 + \frac{d_i - d_0}{h_w}y \tag{4.31}$$

$$\left|\vec{E}(y)\right| = \frac{\Delta V(y)}{d(y)} = \frac{\hat{V}_s/2}{d_0 + \frac{d_i - d_0}{h_w}y} = \frac{1}{2}\frac{\left(\hat{V}_s/2\right)h_w}{d_0 h_w + (d_i - d_0)y} \tag{4.32}$$

The stored electrical energy is then given by (4.33). The first part of this integral is given by (4.34). Then, integration over $z$ corresponds to multiplication of $l_{R5}$, (4.35), i.e., the stored energy is calculated by the integral shown in (4.36).

$$W_e = \frac{1}{2}\varepsilon_0\varepsilon_r \int_0^{d_0 + (d_i - d_0)\frac{y}{h_w}} \int_0^{h_w} \int_0^{l_{R5}} \left(\frac{\left(\hat{V}_s/2\right)h_w}{d_0 h_w + (d_i - d_0)y}\right)^2 dxdydz \tag{4.33}$$

$$\int_0^{d_0 + (d_i - d_0)\frac{y}{h_w}} \left(\frac{\left(\hat{V}_s/2\right)h_w}{d_0 h_w + (d_i - d_0)y}\right)^2 dx \tag{4.34}$$

$$\int_0^{l_{R5}} \frac{\left(\left(\hat{V}_s/2\right)h_w\right)^2}{d_0 h_w + (d_i - d_0)y}\frac{1}{h_w}dz = \frac{\left(\hat{V}_s/2\right)^2}{d_0 h_w + (d_i - d_0)y}h_w l_{R5} \tag{4.35}$$

$$W_e = \frac{1}{2}\varepsilon_0\varepsilon_r h_w l_{R5}\left(\hat{V}_s/2\right)^2 \int_0^{h_w} \frac{1}{d_0 h_w + (d_i - d_0)y} \tag{4.36}$$

This integral is of the type described by (4.37). Substituting the values of (4.38) into (4.37) and simplifying yields the final expression shown in (4.39).

$$\int_0^n \frac{1}{a + by}dy = \frac{ln(a + bn) - \ln(a)}{b} \tag{4.37}$$

$$\left\{\begin{matrix} a = d_0 h_w \\ b = (d_i - d_0) \\ n = h_w \end{matrix}\right\} \tag{4.38}$$

$$W_e = \frac{1}{2}\varepsilon_0\varepsilon_r h_w l_{R5}\left(\hat{V}_s/2\right)^2 \frac{\ln(d_i) - ln(d_o)}{d_i - d_o} \tag{4.39}$$

*Calculation of energy between primary windings and magnetic core (region type 6)*

This region is essentially composed of two parallel plates separated by distance $d_p$ and with potential difference according to (4.40). Clearly, this region is therefore a special case of region 1. Letting $d_o$ approach $d_i = d_p$ in equation (4.14) yields the

expression of (4.41). Note that this equation is in the familiar form of a parallel plate capacitor approximation.

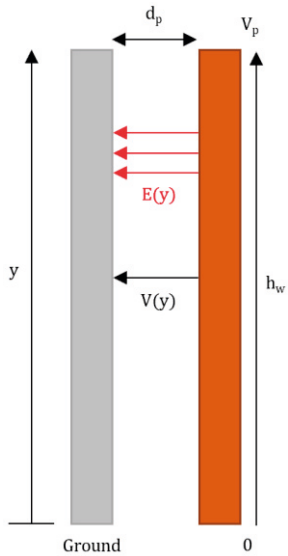



Figure 4.15: Geometry used in estimating stored energy in winding region type 6

$$V(y) = \frac{x}{h_w}\hat{V}_p \tag{4.40}$$

$$W_e = \frac{1}{6}\varepsilon_0\varepsilon_r \frac{l_{R6}h_w}{d_p}\hat{V}_p{}^2 \tag{4.41}$$

*Calculation of energy between winding turns*

Methods for estimating the stored energy between winding turns have been proposed in [4.7]-[4.9]. However, as aforementioned, in high voltage high power pulse transformers this energy is most usually negligible with respect to that stored in regions R1 to R5, above, and will not be further discussed here.

*Calculation of lumped stray capacitance*

In keeping with the above and the definitions of Figure 4.2 and Figure 4.3, the lumped stray capacitance $C_d$ may be calculated according to (4.42).

$$C_d = \frac{2\sum_n W_n}{V_2^2} \tag{4.42}$$

### 4.2.4 Estimation of leakage inductance

Similar to stray capacitance, the pulse transformer leakage inductance is related to the energy stored in the leakage magnetic field. The leakage magnetic field is seen in between the primary and secondary windings, i.e., region type 1, and may be assumed to run in lines parallel with the primary winding. Here, the magnetomotive force is given by (4.43). From this, the stored magnetic energy is given according to (4.44).

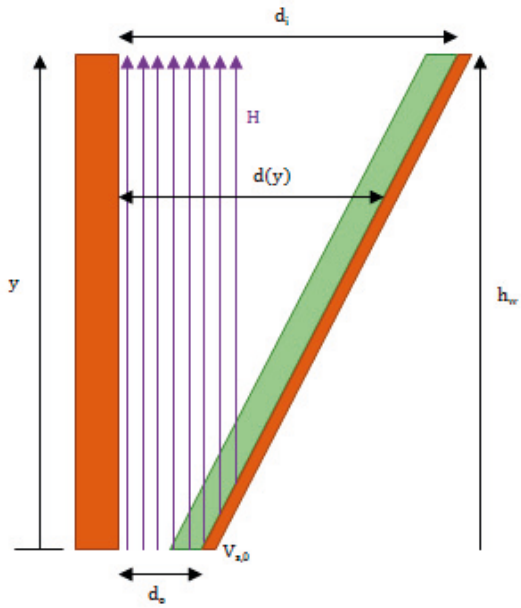



Figure 4.16: Geometry used in calculation of leakage inductance

$$H = \frac{N_2 I_2}{h_w} \tag{4.43}$$

$$W_m = \frac{1}{2}\mu_0\mu_r \int_0^{d_0+(d_i-d_o)\frac{y}{h_w}} \int_0^{h_w} \int_0^{l_{R1}} \left(\frac{N_2 I_2}{h_w}\right)^2 dxdydz \tag{4.44}$$

The first part of this integral is given by (4.45). Then, integration over z corresponds to multiplication of $l_{R1}$, (4.46), i.e., the stored energy is calculated by the integral shown in (4.47). Note that as $d_o$ again approaches $d_i$ this generalized equation comes to equal that expected by a parallel winding structure.

$$\int_0^{d_0+(d_i-d_o)\frac{y}{h_w}} \left(\frac{N_2 I_2}{h_w}\right)^2 dx = \left(\frac{N_2 I_2}{h_w}\right)^2 d_0 + \left(\frac{N_2 I_2}{h_w}\right)^2 \frac{(d_i - d_o)}{h_w} y \tag{4.45}$$

$$\int_0^{l_{R1}} \left(\frac{N_2 I_2}{h_w}\right)^2 d_0 + \left(\frac{N_2 I_2}{h_w}\right)^2 \frac{(d_i - d_o)}{h_w} y \, dz$$
$$= l_{R1}\left[\left(\frac{N_2 I_2}{h_w}\right)^2 d_0 + \left(\frac{N_2 I_2}{h_w}\right)^2 \frac{(d_i - d_o)}{h_w} y\right] \quad (4.46)$$

$$W_m = \frac{1}{2}\mu_0\mu_r l_{R1}\int_0^{h_w}\left[\left(\frac{N_2 I_2}{h_w}\right)^2 d_0 + \left(\frac{N_2 I_2}{h_w}\right)^2 \frac{(d_i - d_o)}{h_w} y\right] dy$$
$$= \frac{1}{2}\mu_0\mu_r (N_2 I_2)^2 \frac{l_{R1}}{h_w}\left(d_o + \frac{d_i - d_o}{2}\right) \quad (4.47)$$

*Calculation of lumped leakage inductance*

In keeping with the above, the leakage inductance of a given winding may be calculated according to (4.48). In forming the simplified equivalent pulse transformer circuit, the leakage inductance of each winding is thus calculated and then collectively combined into a single lumped inductive element according to secondary winding connection principle.

$$W_m = \frac{1}{2} L_{s,w} I_2^2 \rightarrow L_{s,w} = \mu_0\mu_r \frac{l_{R1}}{h_w}\left(d_o + \frac{d_i - d_o}{2}\right) N_2^2 \quad (4.48)$$

### 4.2.5 Estimation of magnetization inductance

Application of the main capacitor bank voltage to the pulse transformer primary windings magnetizes the transformer core. Here, an accurate estimation of the transformer magnetization inductance is important in calculating the corresponding magnetization current. In particular, this will be shown to be important in designing the transformer bias circuit and the transformer demagnetization circuit when such are required. In this work, the magnetization inductance is estimated directly from the magnetic core reluctance in accordance with (4.49).

$$L'_m \cong \frac{N^2}{R} = \frac{\mu_0\mu_r x_c y_c k_f}{2h_w + 2d_i + 4\frac{\pi}{2}(x_c/2 + d_i)} N_1^2 \quad (4.49)$$

### 4.2.6 Relationship between parallel and conic windings

As indicated in the preceding sections, the parallel winding is a special case of the conic winding structure with $d_o$ approaching $d_i$. This is exemplified in Figure 4.17, plotting the normalized stored electric and magnetic energies for a volume of region

type 1 over the ratio$d_o/d_i$. At the other extreme, setting $d_o = 0$, it is possible to reduce the stored magnetic energy (and consequently the leakage inductance) by a factor 2 while increasing the stored electric energy (and consequently the stray capacitance). This is clearly of great interest in applications requiring very short rise time. Furthermore, by varying the ratio $d_o/d_i$, one can optimize the pulse response by directly influencing the damping factor without affecting the pulse transformer extents volume.

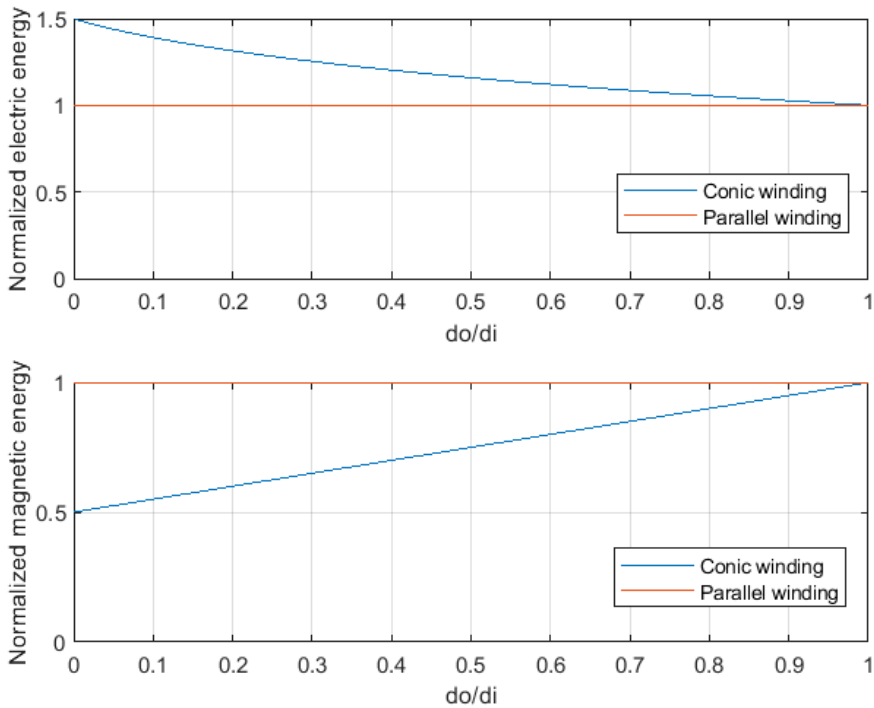



Figure 4.17: Normalized stored electric and magnetic energy for a volume of region type 1 over the ratio $d_o/d_i$.

### 4.2.7 Equivalent circuit analysis and pulse performance

As was noted in an earlier section, from the perspective of output pulse performance the full equivalent circuit shown in Figure 4.2 may be reduced to that of Figure 4.3 or Figure 4.18. The procedures developed in sections 4.2.3-4.2.5 allow accurate analytical calculation of each of the lumped circuit elements of Figure 4.18, i.e., equivalent circuit analysis may now be used to evaluate the output pulse performance corresponding to a given transformer geometry.

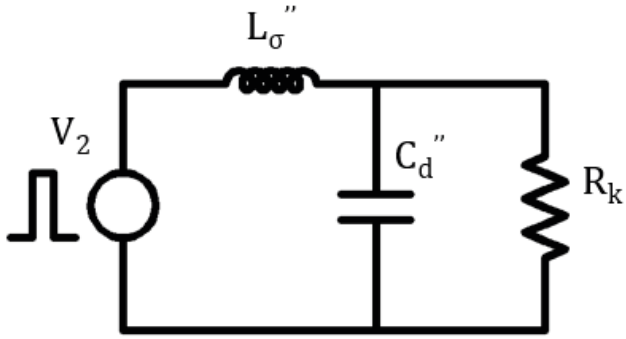



Figure 4.18: Equivalent circuit representation of pulse transformer output circuit

Note that the equivalent circuit in Figure 4.18 is a second order RLC circuit, i.e., analysis using the standard form of the second order system is convenient. Closing the HV switch assembly corresponds to step excitation of the system, (4.50). Here, $\zeta$ is the damping and $\omega_0$ is the natural frequency of the system, defined according to (4.51) and (4.52), respectively.

$$V(s) = \frac{V_2}{s}\frac{\omega_0^2}{(s^2 + 2\zeta\omega_0 s + \omega_0^2)} \tag{4.50}$$

$$\zeta = \frac{1}{2R}\sqrt{\frac{L_\sigma}{C_d}} \tag{4.51}$$

$$\omega_0 = 1/\sqrt{L_\sigma C_d} \tag{4.52}$$

Importantly, the complete pulse waveform in the time domain may be calculated analytically by inverse Laplace transformation of (4.50), i.e., pulse rise time, pulse overshoot, and any other interesting performance criteria may be directly obtained, (4.53)-(4.54). Note that whereas the overshoot can be calculated analytically, there is no general expression for the pulse rise time as defined here. Hence, the rise time will be calculated numerically from the waveform.

$$t_r = \min\left(t : L^{-1}\{V_2(s)\} \geq 0.99V_2\right) \tag{4.53}$$

$$M_p = \max\big(v_2(t)\big) - V_2 \tag{4.54}$$

The inverse Laplace transformation of (4.50) takes one of three distinct forms depending on $\zeta$-

*Underdamped circuit ($0 < \zeta < 1$)*

Analysis of underdamped circuits is simplified by introducing the damped natural frequency $\omega_d$, (4.55). With this, the inverse Laplace transformation of (4.50) is given by (4.56).

$$\omega_d = \omega_0\sqrt{1-\zeta^2} \tag{4.55}$$

$$v_2(t) = L^{-1}[V_2(s)] = V_2\left(1 - e^{-\zeta\omega_0 t}\left[cos(\omega_d t) + \frac{\zeta}{\sqrt{1-\zeta^2}}sin(\omega_d t)\right]\right) \tag{4.56}$$

The step response of an underdamped circuit is characterized by an overshoot given analytically according to (4.57). As will be discussed in a later section, it is crucial that this overshoot is limited to, e.g., 1...3 % of the nominal flat top voltage $V_2$.

$$M_p = \max\big(v_2(t)\big) - V_2 = V_2 e^{-\pi\frac{\zeta}{\sqrt{1-\zeta^2}}} \tag{4.57}$$

*Critically damped circuit ($\zeta = 1$)*

For critically damped circuits, the output pulse is given by (4.58). Clearly, such a system has no overshoot. It is pointed out that in this context the critically damped circuit is somewhat of an ideal curiosity as, both numerically and in practice, a system with unity damping does not exist.

$$v_2(t) = L^{-1}[V_2(s)] = V_2(1 - e^{-\omega_0 t}[1 + \omega_0 t]) \tag{4.58}$$

*Overdamped circuit ($\zeta > 1$)*

For overdamped circuits, the output pulse is given by (4.59). Again, such a system has no overshoot. The overdamped circuit is of special interest in long pulse high power applications as, typically, the leakage inductance is much greater than the stray capacitance and the load resistance is relatively small, i.e., the damping is often significantly greater than unity. In this case, one of the two decaying exponentials seen in (4.59) decreases much faster than the other and may be neglected, i.e., the system is well approximated by a first order system with time constant $L_s/R_k$. Hence, the 0-99% pulse rise time may often be approximated by $t_r = 4.6\,L_s/R_k$.

$$v_2(t) = L^{-1}[V_2(s)]$$
$$= V_2\left(1 + \frac{\omega_0}{2\sqrt{\zeta^2-1}}\left[\frac{e^{-\left(\zeta+\sqrt{\zeta^2-1}\right)\omega_0 t}}{\left(\zeta+\sqrt{\zeta^2-1}\right)\omega_0} - \frac{e^{-\left(\zeta-\sqrt{\zeta^2-1}\right)\omega_0 t}}{\left(\zeta-\sqrt{\zeta^2-1}\right)\omega_0}\right]\right) \quad (4.59)$$

### 4.2.8 Optimization routine

The preceding sections have treated pulse transformer modeling such that the pulse response can be calculated for a given pulse transformer geometry used in a specific application. The procedure is summarized in Figure 4.19.

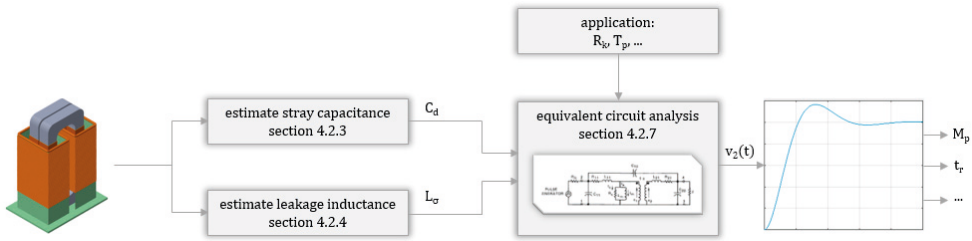



Figure 4.19: Procedure used to evaluate pulse transformer performance

*Design parameters*

To generate a procedure for design and optimization, an appropriate set of design parameters from which the rest of the complete pulse transformer geometry can be derived must be selected. In this approach, the following design parameters are considered fundamental-

- Magnetic core leg width, $x_c$
- Number of turns per secondary winding, $N_2$
- Secondary winding height, $h_w$

In addition, the following design choices must be made-

- Use of core bias system, $k_b = 1 \ldots 2$
- Application dependent: parallel connection ($k_w = 1$) or series connection ($k_w = 2$) of secondary windings

- Winding type: single layer windings, multiple layer windings, or pancake windings
- For single layer windings: use of parallel windings or conic windings

In the following, a generalized procedure will be developed. The developed procedure may then, for a given application, be followed for interesting combinations of the above design choices-

First, as was noted in relation to equation (4.1), the product of the number of turns per secondary winding and magnetic cross-sectional area must be chosen to be larger than a number determined by the application. Thus, having selected the magnetic core leg width and the number of turns per secondary winding, the required magnetic core depth is directly given by (4.60).

$$y_c = \frac{V_2 T_p}{k_w k_b k_f x_c B_{max} N_2} \tag{4.60}$$

As mentioned earlier, system damping is naturally substantial in long pulse high power applications. For this reason, there is seldom need or purpose to sensitively shape transformer stray capacitances, i.e., the distances $d_i$, $d_o$, $d_{t,u}$, $d_{t,l}$, $d_r$, $d_{s,i}$ and $d_{s,o}$ defined in Figure 4.6 and Figure 4.7 may be considered to be fully determined by high voltage isolation requirements. For the same reason, only parallel and 'fully' conic windings will be considered in the following. Consequently, the above distances are given by (4.61) for parallel windings and (4.62) for conic windings, respectively.

Finally, the transformer windings must be sized. Importantly, the windings must be able to support the RMS current of the load pulse corresponding to a given power dissipation, (4.63)-(4.64). Here, $I_w$ is the winding current amplitude, $T_p$ is the pulse length, and $f_r$ is the pulse repetition rate.

$$
k_w = 1: \quad
\begin{array}{lll}
 & k_g = 1: & k_g = 2: \\
d_{o,a} = & d_{iso} & d_{iso} \\
d_{i,a} = & 0 & d_{iso} \\
d_{o,b} = & d_{iso} & d_{iso} \\
d_{i,b} = & 0 & d_{iso} \\
d_{tu,a} = & d_{iso} & d_{iso} \\
d_{tu,b} = & d_{iso} & d_{iso} \\
d_{tl,a} = & 2d_{iso} & 2d_{iso} \\
d_{tl,b} = & 2d_{iso} & 2d_{iso} \\
d_{s,o} = & 0 & d_{iso} \\
d_{s,i} = & 2d_{iso} & d_{iso}
\end{array}
\tag{4.61}
$$

$$
k_w = 2: \quad
\begin{array}{lll}
 & k_g = 1: & k_g = 2: \\
d_{o,a} = & d_{iso}/2 & d_{iso}/2 \\
d_{i,a} = & 0 & d_{iso}/2 \\
d_{o,b} = & d_{iso} & d_{iso} \\
d_{i,b} = & d_{iso}/2 & d_{iso} \\
d_{tu,a} = & d_{iso}/2 & d_{iso}/2 \\
d_{tu,b} = & d_{iso} & d_{iso} \\
d_{tl,a} = & d_{iso} & d_{iso}/2 \\
d_{tl,b} = & 2d_{iso} & d_{iso} \\
d_{s,o} = & d_{iso}/2 & d_{iso} \\
d_{s,i} = & 2d_{iso}/2 & d_{iso}
\end{array}
\tag{4.62}
$$

$$I_w = \frac{k_w \hat{I}_2 \sqrt{T_p f_r}}{2} \tag{4.63}$$

$$P_{cu} = \rho_{cu} J^2 = \rho_{cu} (I_w / A_{cu})^2 \tag{4.64}$$

*Design of single layer windings*

Windings of this type consist of a single layer of standard enamelled round copper wire. As shown in Figure 4.20, the copper wire has diameter $\emptyset_w$ and is wound along the winding bobbin with an inter-turn spacing $d_y$.

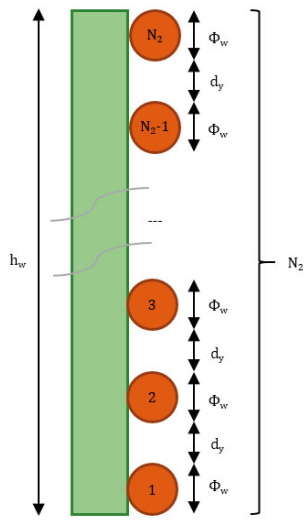



Figure 4.20: Overview of the single layer winding technique

Allowing a maximum RMS current density $J$, the wire diameter $\emptyset_w$ is sized according to (4.65). From Figure 4.20, this yields a winding height $h_w$ according to (4.66). Alternatively, the distance between winding turns is given by (4.67). Here, $k_i$ represents the dielectric strength of the insulating material. Typically, with hundreds of turns per secondary winding, this distance is often more than adequately covered by the wire isolation itself.

$$A_{cu} = \pi \left(\frac{\Phi_w}{2}\right)^2 \rightarrow \Phi_w = \sqrt{\frac{2 k_w \hat{I}_2 \sqrt{T_p f_r}}{J_{max} \pi}} \tag{4.65}$$

$$h_w = N_2 \Phi_w + (N_2 - 1) d_y \tag{4.66}$$

$$d_y \geq \frac{(V_s - V_{s,0})}{N_2} k_i \tag{4.67}$$

The per winding resistance is given by (4.68) with, using the definitions outlined in Figure 4.6 and Figure 4.7, the single layer winding mean path length given by (4.69).

$$R_w = \rho \frac{l}{A} = \rho \frac{N_2 [MPL]}{A_{cu}} \tag{4.68}$$

$$[MPL]_w = 2\left(x_c + y_c + 4d_p + 4\Phi_p + 4\left(\frac{d_o + d_i}{2}\right) + 4\frac{\Phi_w}{2}\right) \tag{4.69}$$

*Design of multiple layer windings*

Windings of this type consist of $l$ winding layers, each with $N_l$ turns, of enamelled rectangular copper wire. Here, $N_2 = lN_l$ such that the above definitions still hold. The copper wire has height $w_h$ and thickness $w_t$ and is again wound with a vertical inter-turn spacing $d_y$. For a rectangular wire, the cross-sectional area is given by (4.70). As will be seen, the winding height is often used as a design parameter, i.e., it is practical to calculate $w_h$ from a minimum $d_y$ thus yielding $w_t$ in accordance with (4.71). Here, taking into account that the winding is wound in multiple layers, the winding height is given by (4.72).

$$A_{cu} = w_t w_h \rightarrow w_t \geq \frac{2k_w \hat{I}_2 \sqrt{T_p f_r}}{J_{max} w_h} \tag{4.70}$$

$$d_y \geq \left(\frac{(V_s - V_{s,0})}{l} / N_l\right) k_i \tag{4.71}$$

$$h_w = N_l \Phi_w + (N_l - 1) d_y \tag{4.72}$$

Importantly, for a given winding potential difference $V_s - V_{s,0}$, the potential difference per winding is $(V_s - V_{s,0})/l$, i.e., the maximum horizontal inter-turn voltage is $2(V_s - V_{s,0})/l$. Consequently, a horizontal isolation distance $d_x$ is necessary between layers, (4.73). Here, $k_i$ represents the dielectric strength of the insulating material. This distance is typically implemented using insulating sheets.

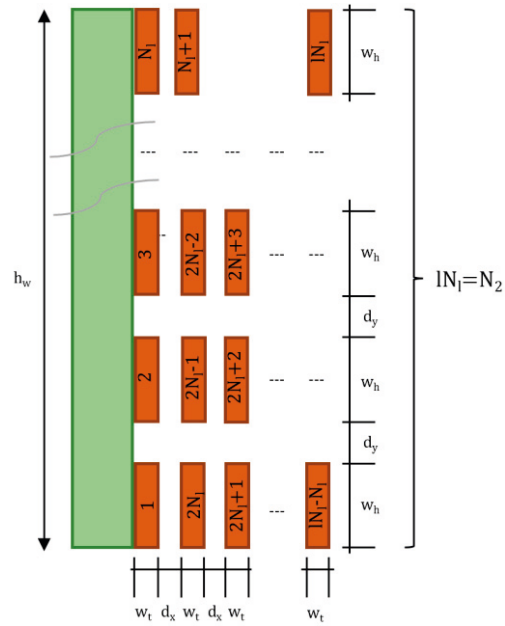



Figure 4.21: Overview of the multiple layer winding technique

$$d_x = 2\frac{\hat{V}_s - V_{s,0}}{l}k_i \tag{4.73}$$

Finally, the per-winding resistance is again given by (4.68) with the mean path length calculated according to (4.74).

$$[MPL] = 2\left(x_c + y_c + 4d_p + 4\Phi_p + 4\left(\frac{d_o + d_i}{2}\right) + 4\left(lw_t + \frac{(l-1)}{2}d_x\right)\right) \tag{4.74}$$

*Design of pancake stack windings*

In this winding technique, a copper strip glued to an isolating strip is wound, one on top of the other, $g_l$ layers around a frame forming a stack (pancake). To form a winding, $g_s$ stacks are then placed on top of each other and interconnected in series, Figure 4.22. Again, $N_2 = g_s g_l$ such that the above definitions hold. The thickness of the isolating strip is termed $d_x$ and is defined by the dielectric strength of the insulating material, (4.75).

$$d_x = \frac{\hat{V}_s - V_{s,0}}{N_2} k_i \tag{4.75}$$

The vertical isolation distance $d_y$ must also be large enough to withstand the voltage between stacks. Practically, however, this distance is usually set significantly larger to allow straightforward and convenient series connection of the pancake stacks. Hence, the pancake height $g_h$ is related to the winding height, the number of pancake stacks and the vertical isolation distance according to (4.76).

$$h_w = g_s g_h + (g_s - 1) d_y \tag{4.76}$$

Finally, the thickness of the copper strip $g_t$ must be selected in accordance with the maximum RMS current density, (4.77), yielding the pancake mean path length, (4.78).

$$A_{cu} = g_h g_t \rightarrow g_t = \frac{k_w \hat{I}_2 \sqrt{T_p f_r}}{2 J_{max} g_h} \tag{4.77}$$

$$[MPL] = 2\left(x_c + y_c + 4d_p + 4\Phi_p + 4\left(\frac{d_o + d_i}{2}\right) + 4\left(g_l g_t + \frac{(g_l - 1)}{2} d_x\right)\right) \tag{4.78}$$

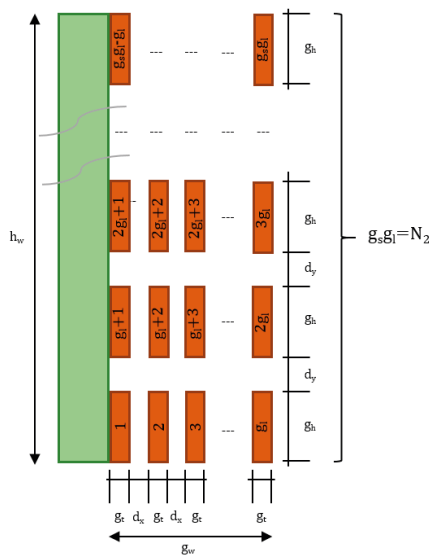



Figure 4.22: Overview of the pancake winding technique

*Design procedure*

Selection of the fundamental design parameters $(x_c, N_2, h_w)$ and design choices allow generation and evaluation of a complete pulse transformer geometry. This process is summarized in Figure 4.23.

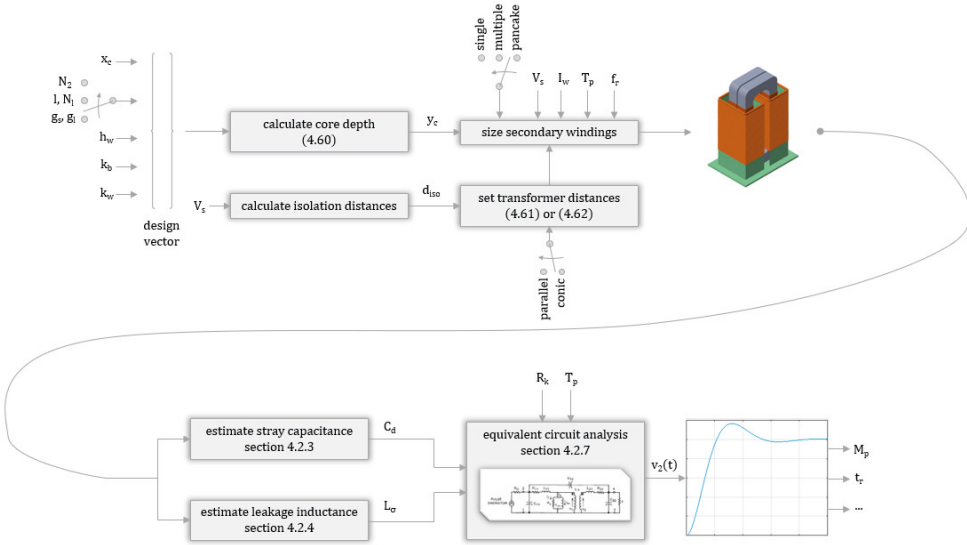



Figure 4.23: Overview of developed design procedure. Selection of fundamental design parameters allow generation and evaluation of complete pulse transformer geometry.

Finally, according to the workflow defined in chapter 4, design constraints and objectives must be defined to ensure that the evaluated design is viable and in accordance with application requirements.

*Design constraints*

As mentioned, the basic function of the pulse transformer unit is ensured by inspection of the generated output pulse waveform $v_2(t)$. Typically, performance constraints are put on the pulse overshoot and the pulse rise time. Here, the maximum pulse overshoot is usually specified as a percentage of the flat top amplitude, (4.79), whereas the maximum pulse rise time is often specified as a percentage of the flat top width, (4.80).

$$M_p = max(v_2(t)) - V_2 \leq k_p V_2 \tag{4.79}$$

$$t_r \leq k_r T_p \tag{4.80}$$

In addition, there are always clear limitations on system size in any application which in view of the pulse transformer may be expressed as a maximum pulse transformer height $\hat{h}_c$ and a maximum magnetic core depth $\hat{y}_c$, (4.81)-(4.82). Further constraints may be included to impose restrictions on, e.g., copper wire/strip diameter/thickness, geometry proportional relationships, and similar but are not included here for the purpose of generality.

$$h_w + 2x_c + 2d_{iso} \leq \hat{h}_c \tag{4.81}$$

$$y_c \leq \hat{y}_c \tag{4.82}$$

If these constraints cannot be met, the design is considered unviable and is to be rejected, i.e., new design parameter values must be chosen to solve the optimization problem.

*Objective function*

Generally, transformer design may be interpreted as a trade-off between transformer volume and loss. This is summarized by (4.83), where the transformer losses have been split into copper losses and core losses for clarity.

$$f(x) = \frac{V}{V_n}k + \frac{P_{cu} + P_{fe}}{P_n}(1-k) \tag{4.83}$$

However, transformer losses are of limited interest in this context as 1) high transformer efficiency is typical, especially when compared to other modulator components (e.g., the capacitor charger), as 2) the impact of transformer losses on usable pulse power is often small in relation to, e.g., the effects of the pulse shape, (2.1), and as 3) the transformer power dissipation is small with respect to the component volume and corresponding surface area, i.e., thermal effects are negligible. Consequently, in this work, the general objective function specified in (4.83) will be reduced to that shown in (4.84), i.e., aiming to minimize pulse transformer volume. Note that, here, the transformer volume is modelled by the magnetic core volume.

$$f(x) = V = x_c y_c l_c = x_c y_c \left(2h_w + 2d_i + 4\frac{\pi}{2}(x_c/2 + d_i)\right) \tag{4.84}$$

*Optimization procedure*

The optimization problem is summarized in (4.85). Note that the problem has been formulated in view of a given core bias system, a given winding technique (single layer, multiple layers, or pancake stacks), a given secondary winding connection

(parallel or series connected), and a given winding shape (parallel or conic). The solver can then be called for interesting combinations of these options.

$$\begin{gathered} minimize\ f(x) = x_c y_c \left( 2h_w + 2d_i + 4\frac{\pi}{2}(x_c/2 + d_i) \right) \\ x = \{x_c, N_2, h_w\} \\ \\ subject\ to: \\ x_l \le x \le x_u \\ G(x) = 0 \\ H(x) \le 0 \\ \\ where: \\ x_l = \{x_{c,min}, N_{2,min}, h_{w,min}\} \\ x_u = \{x_{c,max}, N_{2,max}, h_{w,max}\} \\ H(x) = \{h_w + 2x_c + 2d_i - \hat{h}_c, y_c - \hat{y}_c, t_r - k_r T_p, M_p - k_p V_2\} \end{gathered} \tag{4.85}$$

The problem is solved using the MATLAB fmincon solver, [4.10]. The solver sets the fundamental design parameters $(x_c, N_2, h_w)$, evaluating the objective function $f(x)$ and the constraints $H(x)$ using the procedures described in sections 4.2.3-4.2.7 and summarized in Figure 4.23.

### 4.2.9 Trends in long pulse high power applications

In this section, the developed models and proposed optimization routine are used to study trends in design of HV pulse transformers. In particular, the resulting pulse transformer volume is studied as a function of pulse length for a number of application parameters. In the following studies, the pulse transformer output voltage and output current are set to 115 kV and 100 A; respectively, and the pulse repetition rate to 14 Hz. These settings reflect the European Spallation Source modulator requirements summarized in Table 4.1. Pulse length is varied from 500 μs to 15 ms, with the ESS application being represented at 3.5 ms. Pulse rise time (0-99%) is allowed to be at most 3.43% of the pulse length, i.e., corresponding to 120 μs for a pulse length of 3.5 ms, Table 4.1. Table 4.2 collects material constants and problem constraints used in the studies. For practical reasons related to manufacturability and maintainability, total pulse transformer height is limited to 1.5 m and magnetic core depth to 1.0 m. The significance of these constraints is studied in a subsequent section. In addition, full transformer core bias (i.e., $k_b = 2$) and series connected secondary windings (i.e., $k_w = 2$) is assumed.

**Table 4.1: Required output pulse performance for European Spallation Source klystron modulator systems**

| Symbol | Quantity | Value |
|---|---|---|
| $V_2$ | Rated output voltage | $115\ kV$ |
| $I_2$ | Rated output current | $100\ A$ |
| $T_p$ | Pulse length | $3.5\ ms$ |
| $t_r$ | Rise time (0-99%) | $120\ \mu s$ |
| $T_{max}$ | Pulse repetition rate | $14\ Hz$ |

**Table 4.2: Summary of material constants, settings and problem constraints used in study of trends in long pulse high power applications**

| Symbol | Quantity | Value |
|---|---|---|
| | Material constants | |
| $J_{max}$ | Maximum RMS current density | $4\ A/mm^2$ |
| $B_{max}$ | Peak magnetic flux density | $1.2\ T$ |
| $k_f$ | Magnetic core fill factor | 90% |
| $\varepsilon_r$ | Relative permittivity of oil | 2.2 |
| | Problem constraints | |
| $\hat{h}_c$ | Maximum pulse transformer height | $1.5\ m$ |
| $\hat{y}_c$ | Maximum magnetic core depth | $1.0\ m$ |
| | Application settings | |
| $V_2$ | Rated output voltage | $115\ kV$ |
| $I_2$ | Rated output current | $100\ A$ |
| $f_r$ | Pulse repetition rate | $14\ Hz$ |
| $\langle T_p \rangle$ | Range of pulse length sweep | $500\ \mu s - 15\ ms$ |
| $T_{max}$ | Pulse rise time | $3.43\%\ of\ T_p$ |

*Trend analysis: single layer winding technique*

As aforementioned, the goal of the optimizer is to minimize pulse transformer volume while satisfying the voltage time integral and pulse rise time conditions. It was shown in [4.11] that, under these circumstances, the best strategy is to add as many secondary winding turns as possible, corresponding to increasing pulse transformer height. Magnetic core cross sectional area should be made as small as possible with necessary increases made predominantly to core depth yc. Only when absolutely necessary should the core leg width xc be increased.

Figure 4.24 shows the outcome of the procedure for a pulse transformer based on the single layer winding technique. Here, the tight rise time constraint strictly limits the maximum transformer leakage inductance. In addition, the number of winding turns per unit of winding height is further limited by the high load current, (4.65)-(4.66). Therefore, in order to be able to add as many winding turns as possible, the optimizer here introduces a relatively large space in between winding turns, (4.48) and (4.66), to optimally utilize the allowed pulse rise time and allowed pulse transformer height. As pulse length is increased, the allowable pulse rise time (and thus leakage inductance) increases proportionally and additional winding turns may be added by simultaneously decreasing the distance between turns. However, at some point - here at application pulse length 3.0 ms - the core depth eventually reaches its prescribed limit and the required magnetic core area may only be obtained by increasing the core leg width. Note that this forces a decrease in the transformer winding height, equation (4.81), thereby drastically limiting the potential increase of transformer winding turns. Shortly thereafter, at application pulse length 3.2 ms, the distance between winding turns can no longer be decreased and some transformer winding turns must actually be removed in order to satisfy the imposed constraints. These two effects compound - adding core leg width forces a decrease in transformer number of turns, implying that an even greater core leg width is required to satisfy the voltage time integral condition - and a sharp increase in core volume is seen. It is also seen that the optimizer at this stage no longer is able to properly utilize the allowance in pulse rise time. This situation quickly escalates to the point of optimizer solution infeasibility, here seen for those application pulse lengths above that of 3.5 ms. In other words, with the pulse requirements and system constraints outlined in Table 4.2, the maximum attainable pulse length for a pulse transformer based on the single layer winding technique is around 3.5 ms. At this point, a pulse transformer with a 1.5 m high magnetic core with a volume of 0.85 m3 and weighing close to 7000 kg is required. To produce higher pulse power or pulse lengths longer than this, size constraints must be relaxed, severely impacting manufacturing costs and maintainability.

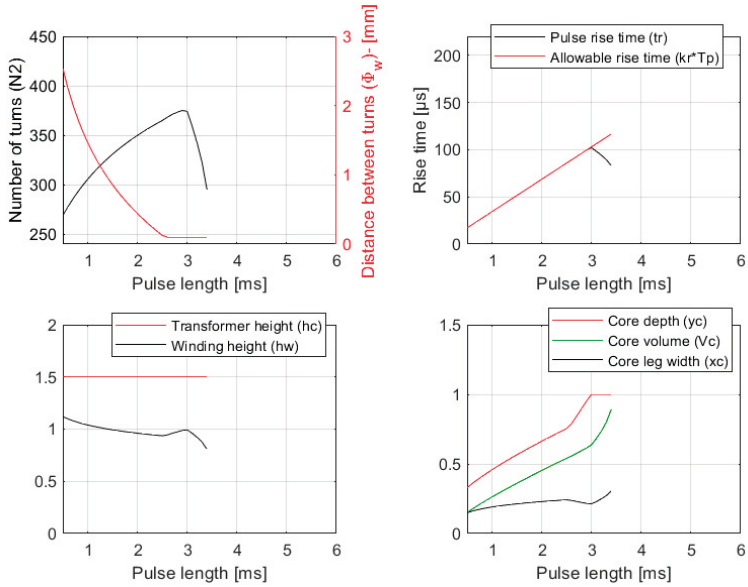



Figure 4.24: Trends for pulse transformer based on single layer winding technique

*Trend analysis: pancake stack winding technique*

In [4.11], the pancake winding technique was evaluated as an alternative to the simpler single layer winding technique. In that case, a pulse rise time of 10% of the pulse length was permissible and as a result pulse transformers based on the single layer winding technique quickly reached the imposed height constraint in minimizing the magnetic core volume. In contrast, the pancake winding technique allowed for significantly more compact pulse transformer designs due to its inherent ability to add winding turns widthwise (i.e., on top of each other) even after reaching the prescribed height limitation.

Figure 4.25 shows the outcome of the procedure for a pulse transformer based on the pancake winding technique according to the specifications presented in Table 4.2. Here, the pulse transformer windings have been assumed to be assembled of twenty pancake stacks each. The impact of the number of stacks on pulse transformer volume is evaluated subsequently. It is remarked that the results seen for application pulse lengths up to that of 2.5 ms match exactly those of the single layer winding technique, Figure 4.24. As can be seen, the winding height is similarly optimized by appropriately selecting the winding stack height. Note here that as the stack height decreases the stack width must correspondingly increase to supply the necessary conductor area, though with minimal effect on pulse transformer volume, (4.84). The similarities between Figure 4.24 and Figure 4.25 are seen because the present application requires a significantly shorter relative pulse rise time and higher power than that studied earlier in [4.11]. Here, the resulting transformer number of

turns is small in relation to the necessary pulse transformer size and the corresponding winding window and may therefore easily be accommodated by a winding consisting only of a single layer of turns. Therefore, it is understood that the pancake winding technique is of limited use in such applications. However, it should be noted that the properties of the pancake winding technique – to a great extent effectively decoupling the number of winding turns from the winding height – allows the attainment of somewhat longer pulse lengths for the same pulse power parameters and size constraints than the single layer winding technique. Here, optimizer solution infeasibility is reached only at 5.5 ms. It is stressed, however, that at this application pulse length the magnetic core size and weight are extremely large, above 1.2 m3, corresponding to that of ~9500 kg.

Figure 4.26 shows optimized pulse transformer volume as a function of application pulse length with the number of pancake stacks per winding as parameter. Here, near-identical results are seen for number of pancake stacks between 15 and 35. It is desirable to avoid using too few pancake stacks, as it would result in tall and unnecessarily heavy stacks with a large number of turns per stack. On the other hand, using too many pancake stacks results in a wasteful (the distance overhead between stacks required for stack interconnection reduces the winding height available for winding turns) and unpractical design (due to the large number of interconnections to be made in assembly). For this reason, windings assembled from around twenty pancake stacks appear to be a reasonable arrangement considering the results presented in Figure 4.25, i.e., around 20 winding turns per pancake stack for the intended application.

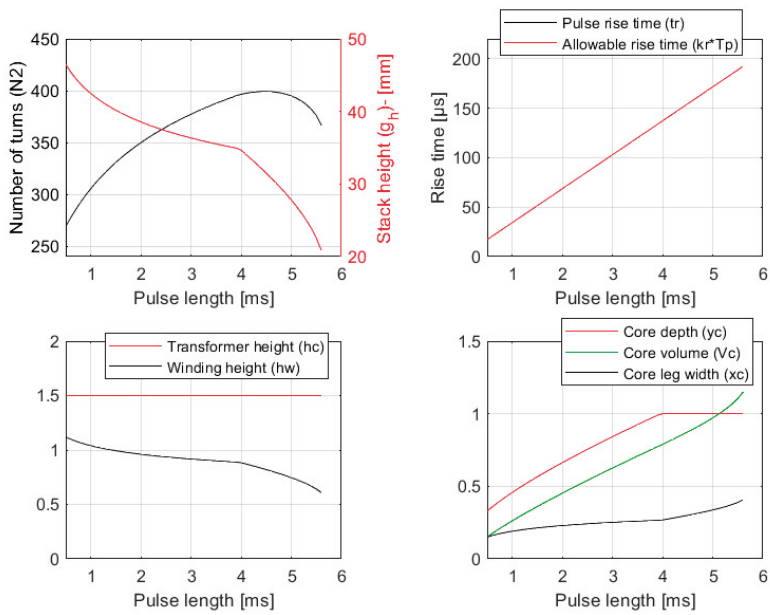



Figure 4.25: Trends for pulse transformer based on pancake stack winding technique

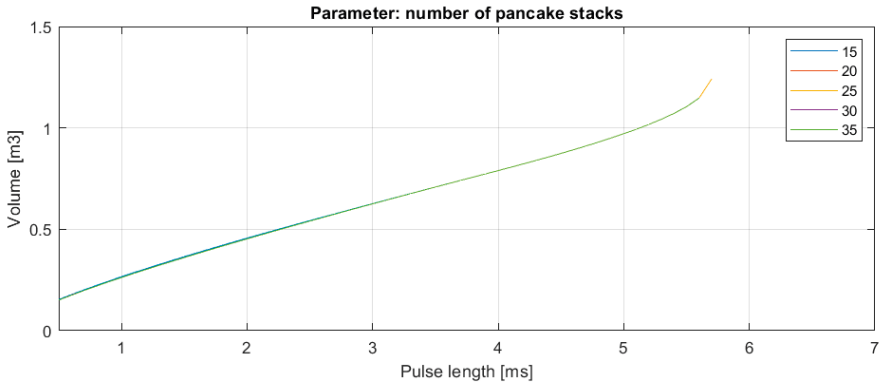



Figure 4.26: Optimized magnetic core volume for pulse transformer based on pancake stack winding technique as a function of application pulse length with the number of pancake stacks as parameter

*Trend analysis: multiple layer winding technique*

Figure 4.27 shows the outcome of the procedure for a pulse transformer based on the multiple layer winding technique according to the specifications presented in Table 4.2. Here, the pulse transformer windings have been assumed to be assembled of five winding layers each. The impact of the number of winding layers on pulse transformer volume is evaluated subsequently. Interestingly, in this case the results match exactly those of the pancake stack winding technique. As discussed, the main issue with the single layer winding technique is that the constrained transformer height is intrinsically and directly linked to the number of winding turns. Here, this issue is managed by dividing the turns between the winding layers and adjusting the conductor height appropriately. Importantly, Figure 4.25 and Figure 4.27 indicate that there is a general lower limit to pulse transformer volume irrespective of chosen winding technique.

Figure 4.28 shows optimized pulse transformer volume as a function of application pulse length with the number of winding layers per winding as parameter. Here, near-identical results are seen for three to six winding layers. With only two winding layers, trends similar to that shown in Figure 4.24 are seen, though occurring at a greater pulse length. At this point - though the obtained results for the pancake stack winding technique and the multiple layer winding technique are identical - important differences with regards to winding construction must be discussed. As described in section 4.2.7, the way the pancake stacks are assembled the voltage between stacks is limited according to (4.75). For a setup with series connected secondary windings and twenty or so stacks per winding, this corresponds to a voltage of only a few kV, appropriately managed by the distance required for stack interconnection. On the other hand, for a similar transformer based on the multiple layer winding technique, the voltage between stacks is given by (4.73). For a transformer with two layers, this voltage is on the order of 30 kV. Using up to five layers, the voltage is still more than 10 kV, requiring several layers of insulating

paper between each winding layer. In addition, one must consider the creepage distance in design, further aggravating the situation. Then, considering the size of the transformer, Figure 4.27, construction of such windings appears much more complicated than that of corresponding pancake-based windings. For these reasons, windings based on this technique are seldom utilized in high voltage applications.

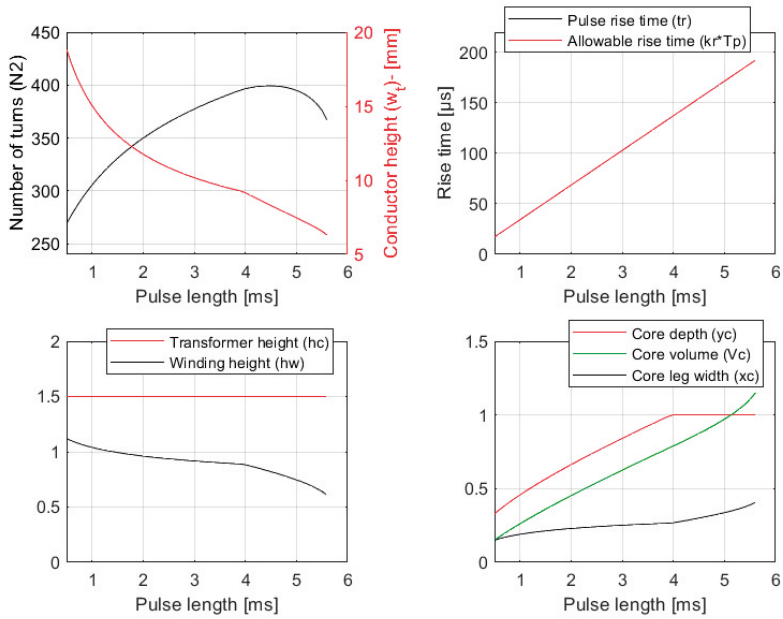



Figure 4.27: Trends for pulse transformer based on multiple layer winding technique

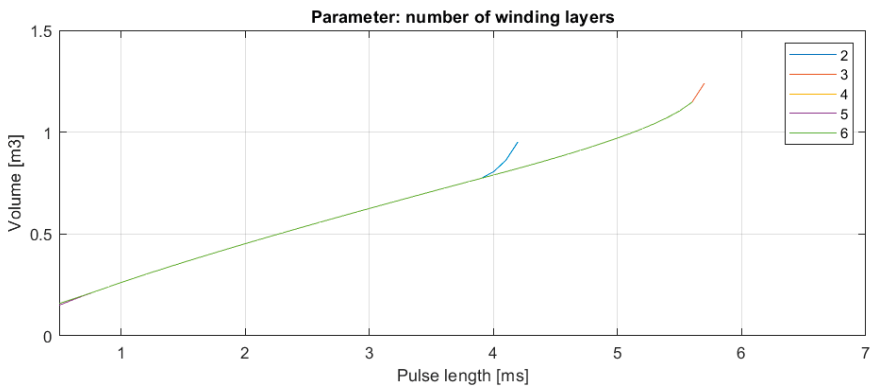



Figure 4.28: Optimized magnetic core volume for pulse transformer based on multiple layer winding technique as a function of application pulse length with the number of winding layers as parameter

The obtained results establish the fact that pulse transformers intended for present day long pulse high power applications will be inherently large, markedly impacting system manufacturability and maintainability. Future projects are likely to require even higher peak pulse power and/or longer pulse length, calling into question the applicability of pulse transformer-based modulator solutions to these applications.

*Trend analysis: comparison of winding techniques*

In the following, the effect of several important application parameters on pulse transformer volume for the different winding techniques will be studied. In particular, the effects of the pulse transformer height constraint, the application load current, and the pulse rise time requirement will be considered. Again, the basic settings outlined in Table 4.2 are applied.

Figure 4.29 depicts the optimized pulse transformer magnetic core volume as function of pulse length as the pulse transformer height constraint is varied. As can be seen, the height constraint strongly affects the attainable pulse length as well as – though to a lesser degree – the resulting pulse transformer volume. This may be understood by considering, e.g., the single layer winding technique. There, the height constraint directly limits the number of transformer turns thereby strongly impacting the attainable pulse length. In essence, the same type of trend is seen but is shifted in relation to the height constraint. As was shown in the preceding sections, for a maximum transformer height of 1.5 m, all three winding techniques require a magnetic core volume of around 0.75 m3 for the ESS application pulse length of 3.5 ms. Importantly, permitting a taller transformer, e.g., up to 2 m, allows design for applications with longer pulse lengths, but does not decrease the required core volume. Note also that while this permits a longer pulse length, the resulting magnetic core volume for such pulse lengths would (in addition to the transformer height) be prohibitive in practice.

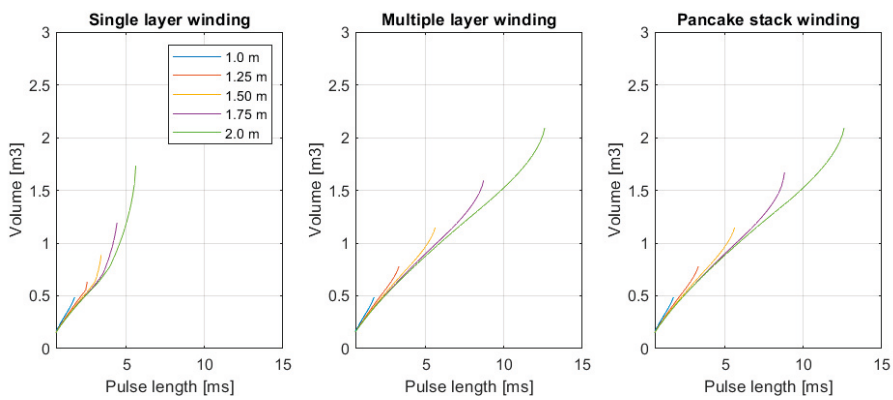



Figure 4.29: Optimized magnetic core volume for pulse transformer as function of application pulse length with application height constraint as parameter

Figure 4.30 illustrates optimized pulse transformer magnetic core volume as function of pulse length as the application load current is varied. Expectedly, the load current has a significant effect on both the attainable pulse length as well as the resulting pulse transformer volume. For example, in the multi-millisecond range the difference between a load current of 75 A and 100 A corresponds to a difference in attainable pulse length on the order of ~1 ms for both the multiple layer winding and pancake stack winding techniques. At the same time, the difference in resulting magnetic core volume can be as great 0.1-0.2 m3, representing a magnetic core weight difference on the order of 1000 kg. Most directly, this is attributable to the variation in winding RMS current and thereby required conductor cross-sectional area, i.e., for a lower load current one can fit more winding turns in a given unit of winding height. Additionally, a lower load current corresponds to a higher optimal leakage inductance permitting a greater number of winding turns for a given pulse rise time requirement.

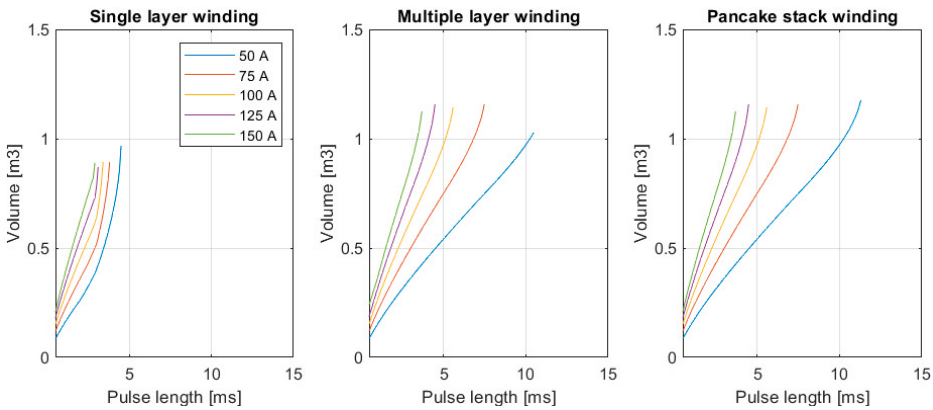



Figure 4.30: Optimized magnetic core volume for pulse transformer as function of application pulse length with application load current as parameter

Finally, though it has been discussed as part of the other studies, the direct effect of required pulse rise time on the pulse transformer volume is studied in Figure 4.31 Here, the limits of the single layer winding technique are clearly illustrated. As was shown in part in Figure 4.24, allowing a longer pulse rise time and thereby permitting additional winding turns in order to reduce pulse transformer volume, the available winding window is quickly utilized and the difference between the cases is small. Again, the benefits of the more flexible multiple layer winding and pancake stack winding techniques is demonstrated.

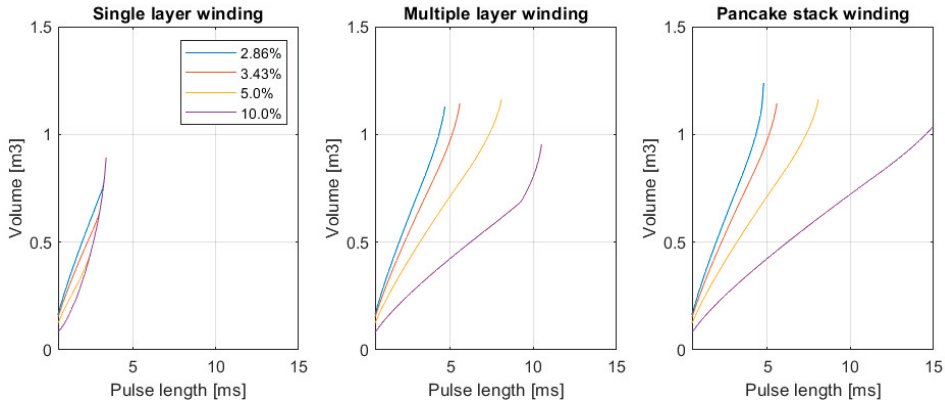



Figure 4.31: Optimized magnetic core volume for pulse transformer as function of application pulse length with pulse rise time constraint as parameter

### 4.2.10 Mathematical analysis of feasibility of pulse transformers for long pulse high power applications

The results presented in the preceding sections have in common that there appears to be a point of infeasibility beyond which the optimizer is unable to satisfy the voltage time-integral condition. This section presents a mathematical study reaching the same conclusion through direct analysis of the voltage-time integral condition, (4.1). The resulting expression is developed for all winding techniques, and is solved for a general existence condition expressing maximum attainable pulse length in terms of application pulse parameters and system constraints.

*Single layer winding technique*

The voltage time integral condition relates the product of output pulse voltage and pulse length directly to the design parameters and material constants of the optimization problem. For a pulse transformer based on single layer windings, $N_2$ may be expressed in terms of winding height and wire diameter, (4.66), which with $N_2 \gg 1$ yields equation (4.86).

$$V_2 T_p = k_w k_b k_{fe} x_c y_c N_2 B_{max} = 4 x_c y_c k_{fe} B_{max} \frac{h_w}{\Phi_w + d_y} \tag{4.86}$$

As the limit of feasibility is approached, pulse transformer height and magnetic core depth are at their respective limits, Figure 4.24. Hence, winding height is under these circumstances given by rearranging (4.81) as expressed by (4.87). Combining

(4.81), (4.86) and (4.87), solving for the core leg width satisfying the voltage time integral yields equation (4.88). This equation relates the now only unknown design parameter to the pulse parameters of the problem and the imposed system constraints.

$$h_w = \hat{h}_c - 2x_c - 2d_i \tag{4.87}$$

$$x_c = \frac{\hat{h}_c/2 - d_i}{2} \pm \sqrt{\frac{\left(\hat{h}_c/2 - d_i\right)^2}{4} - \frac{V_2 T_p \left(\Phi_w + d_y\right)}{8 y_c k_{fe} B_{max}}} \tag{4.88}$$

Equation (4.88) indicates that under these circumstances only two values for the core leg width will satisfy the voltage time integral condition. Clearly, the smallest such value constitutes the optimal solution in terms of transformer volume. It is also remarked that this equation contains a condition for existence since the contents of the square root must be positive in order for a real solution to exist.

Setting the expression within the square root of (4.88) to be larger than zero yields an inequality that may be solved for, e.g., the pulse length parameter. Assuming $d_y \ll \emptyset_w$, (4.89) is found. As can be seen, this inequality immediately yields the maximum attainable pulse length as function of the application pulse parameters, the imposed constraints, and the assumed curves overlapping material constants. Note also that this inequality could equally well be reformulated providing, for instance, an upper limit of, e.g., modulator load current given a desired pulse length.

$$T_p < \left[ 2 y_c k_{fe} B_{max} \frac{\left(\hat{h}_c/2 - d_i\right)^2}{V_2 \sqrt{\frac{4 I_2 \sqrt{f_r}}{J_{max} \pi}}} \right]^{4/5} \tag{4.89}$$

Figure 4.32 explores this relationship in further detail, plotting maximum attainable pulse length versus the imposed constraints on pulse transformer height and magnetic core depth. Figure 4.32.a shows the results given directly by (4.89), whereas Figure 4.32.b shows equivalent results obtained by sweeping the developed optimization routine over the space of the imposed constraints. Here, the pulse length is iteratively increased for each constraint combination until the optimizer is unable to generate feasible results. The results presented in Figure 4.32.a and Figure 4.32.b have been confirmed to match with a discrepancy no greater than 2%. This estimation error is in part attributable to the step size of the pulse length in the iterative optimization procedure and the simplification made in deriving (4.89),

above. As can be seen, both the derived equation and the developed optimization procedure yield a maximum pulse length of 3.5 ms for the imposed constraints given in Table 4.2. Again, to go beyond this pulse length or to increase, e.g., pulse power, a substantial increase in transformer height upwards of 2 m is necessary.

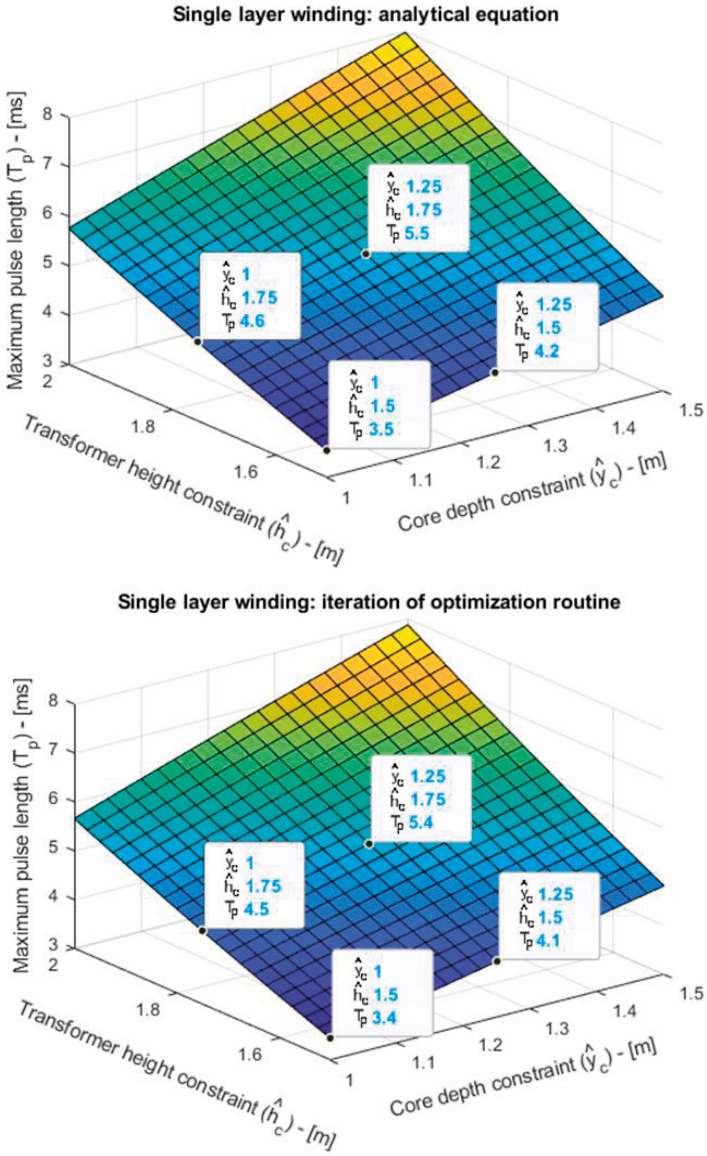



Figure 4.32: Maximum attainable pulse length for pulse transformer based on single layer winding technique as function of pulse transformer height and magnetic core depth constraints:- a) as derived from equation (4.89); b) as derived by the optimization procedure outlined in section 4.2.7.

*Pancake stack winding technique*

A similar equation may be derived for a pulse transformer based on the pancake winding technique, although its derivation is not as straightforward as that outlined for the single layer winding technique. The complication arises from the fact that, for the pancake winding technique, the winding height is not directly connected to the transformer number of turns (added degree of freedom for multi-layer windings). However, under these circumstances the attained pulse rise time always coincides with the maximum allowable pulse rise time, Figure 4.25. Hence, the resulting transformer leakage inductance may be calculated from (4.90). Then, since leakage inductance may also be calculated from transformer geometry, (4.48), the combination of these two equations yields a substitute expression for the transformer number of turns, (4.91).

$$t_r \cong 4.6\frac{L_s I_2}{V_2} = k_r T_p \rightarrow L_s = \frac{k_r T_p V_2}{4.6 I_2} \tag{4.90}$$

$$N_2 = \sqrt{\frac{k_r T_p V_2 \left(\hat{h}_c - 2x_c - 2d_i\right)}{4.6\mu_0 I_2 \left(3x_c d_i + 3\hat{y}_c d_i + 5d_i^2\right)}} \tag{4.91}$$

Substituting (4.91) back into the first part of equation (4.86), common to both winding techniques, the resulting equation may be solved for the required core leg width. In this case a third order equation is obtained. Although this equation may be solved algebraically, the primary interest is an existence condition similar to that of (4.89).

Figure 4.33 plots the obtained third order equation versus core leg width for a range of pulse lengths assuming the application parameters of Table 4.2. As can be seen, the smallest of the three roots is always negative, i.e., unphysical, and may therefore be neglected. Out of the two remaining roots, the smallest root again constitutes the optimal solution in terms of transformer volume.

It was shown in Figure 4.25 that the maximum attainable pulse length for the specifications of Table 4.2 was approximately 4.5 ms. This is again seen in Figure 4.33 since when this point of infeasibility is passed the function value of the local maximum becomes less than zero, corresponding to complex and therefore unphysical roots. This is exemplified by, e.g., the 5.0 ms trace, Figure 4.33. The local maximum is easily found by derivation and may be substituted back into the original third order equation. Setting the resulting equation to be larger than zero again yields an existence condition similar to that of (4.89). Expressing this inequality in terms of pulse length yields the inequality (4.92).

$$T_p < \frac{16}{27}\left(\frac{B_{max}^2 \hat{y}_c^2 k_f^2 k_r}{4.6\mu_0 V_2 I_2 d_i}\right)\frac{\left(\hat{h}_c/2 - d_i\right)^2}{\left(\hat{h}_c + 3\hat{y}_c + 3d_i\right)} \tag{4.92}$$

Figure 4.34 shows similar results to that presented in Figure 4.32 although shifted upwards, corresponding to somewhat longer attainable pulse lengths for the same conditions in accordance with that demonstrated in the preceding section. Again, note the close match between results obtained by the developed equation and those obtained by iteration of the developed optimization procedure.

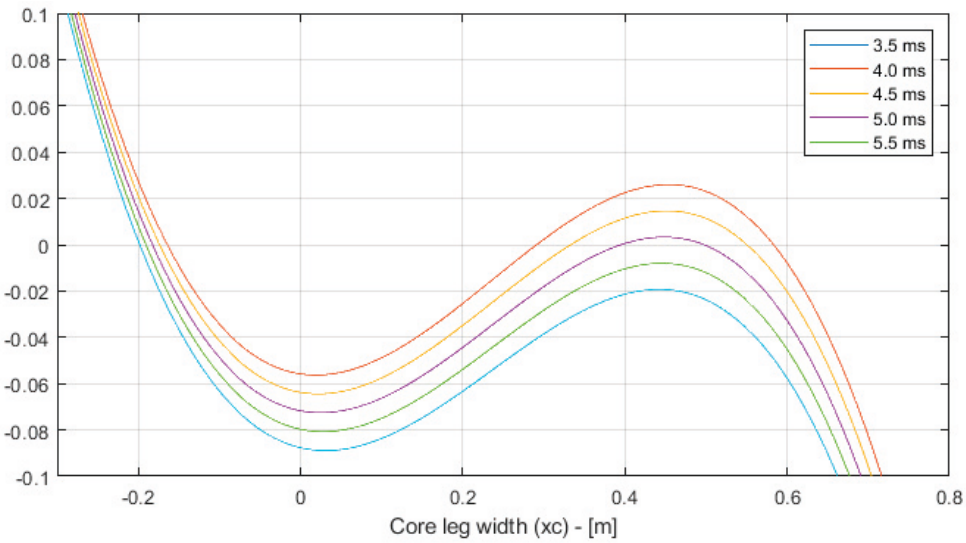



Figure 4.33: Nature of third order equation expressing required core leg width to satisfy voltage time integral condition for a range of pulse lengths

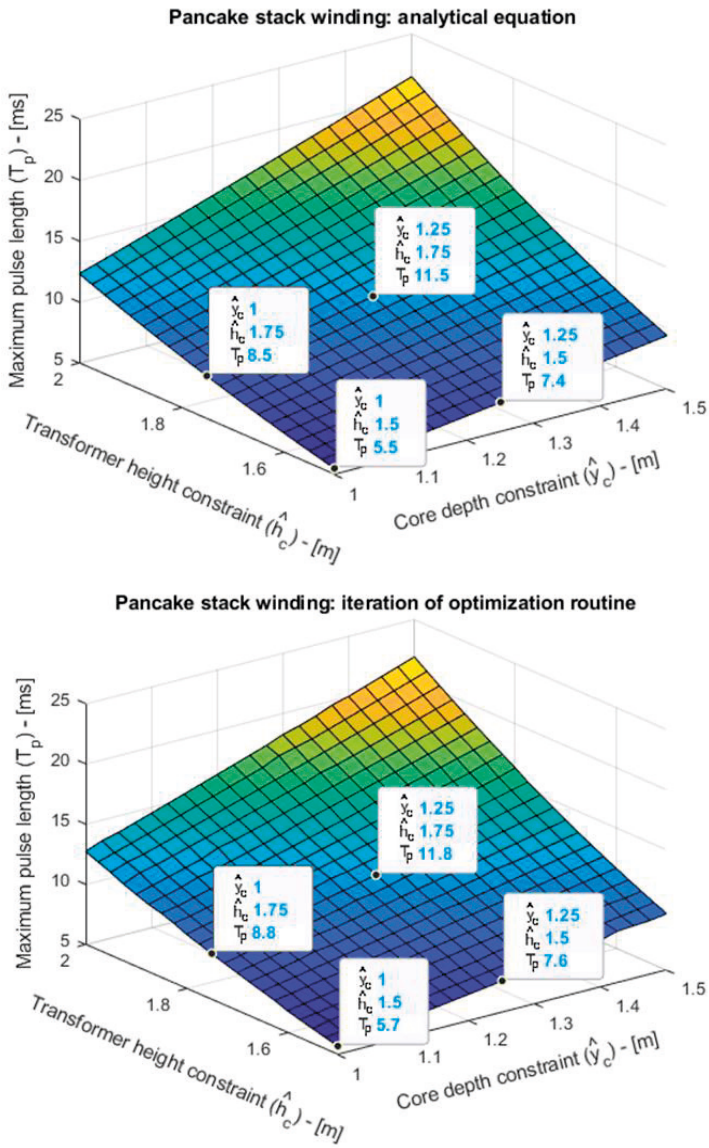



Figure 4.34: Maximum attainable pulse length for pulse transformer based on pancake winding technique as function of pulse transformer height and core depth constraints:- a) as derived from equation (20); b) as derived by the optimization procedure outlined in section 4.2.7.

*Multiple layer winding technique*

Given the mathematical similarities between the pancake stack winding and multiple layer winding techniques demonstrated in Figure 4.25 and Figure 4.27, (4.92) is directly compared to results derived by iteration of the optimization procedure for a pulse transformer based on multiple layer windings, Figure 4.35.

Again, excellent agreement is seen between the derived analytical equation and the results derived by iteration of the optimization routine.

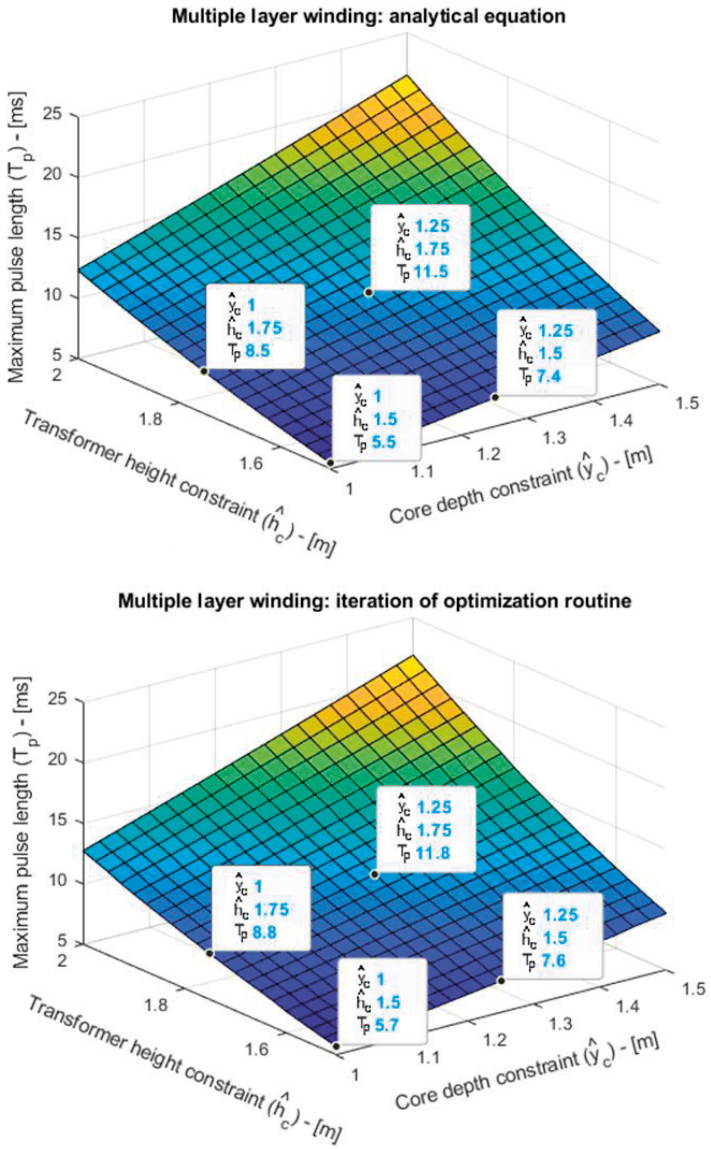



Figure 4.35: Maximum attainable pulse length for pulse transformer based on multiple layer winding technique as function of pulse transformer height and core depth constraints:- a) as derived from equation (4.92); b) as derived by the optimization procedure outlined in section 4.2.7.

## 4.3 Design of bouncer systems

As the main capacitor bank energy storage is discharged during the pulse event the capacitor bank voltage drops correspondingly. Without compensation the capacitor discharge manifests as output pulse droop, (4.93), prohibitive in most modern pulse power applications. Attempting to satisfy droop requirements by oversizing the capacitor bank results in impractical solutions, (4.94). For example, considering oversizing the capacitor bank for ESS application requirements results in a capacitor bank volume exceeding that of 10 $m^3$.

$$\Delta V_{cbk} = \frac{I_2' T_p}{C_{bk}} \tag{4.93}$$

$$C_{bk} = \frac{I_2' T_p}{\Delta V_{cbk}} = \left(\frac{k_w N_2}{N_1}\right)^2 \frac{I_2 T_p}{p V_2} \tag{4.94}$$

A type of auxiliary circuit known as a 'bouncer' has been developed to mitigate the issue of capacitor bank voltage droop. The choice of bouncer solution depends mainly on 1) chosen modulator topology and 2) application pulse length, [4.12]. For pulse transformer-based modulators, three main bouncer topologies have been developed: the passive LR bouncer, the passive LC bouncer, and the active electronic bouncer.

The next section reviews published works discussing these bouncer topologies, listing their working principle as well as their advantages and drawbacks, particularly with respect to long pulse high power applications. Based on this review, the classical passive LC bouncer as well as the electronic bouncer are selected for further study. Subsequent sections develop detailed design and optimization procedures for the chosen bouncer circuits, ending with a case study considering the requirements on bouncer systems intended for use in the ESS application.

### 4.3.1 Overview of bouncer circuits

Though bouncer circuits are commonly used in modulator applications, little information exists with regards to their design.

*Passive LR bouncer*

The LR bouncer consists of a parallel LR network inserted in series with the pulse transformer primary winding, Figure 4.36. This simple compensation circuit acts by smoothening the pulse waveform around the required flat top voltage and requires no active components [4.13]. It is effective up to the low microsecond range,

although the added losses may be substantial. In particular, the technique is impractical in long-pulse applications mainly due to excessive loss in the bouncer resistance as well as the required bulky components. For these reasons, the LR bouncer is not further discussed in this work.

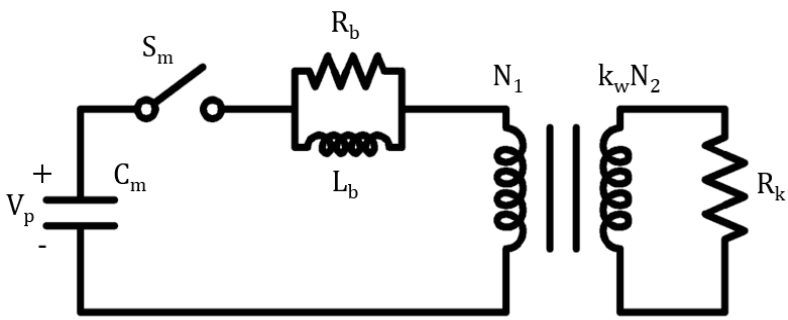



Figure 4.36: LR bouncer circuit

*Passive LC bouncer*

The basic LC bouncer circuit is shown in Figure 4.37.a. The circuit consists of a capacitor $C_b$ pre-charged to voltage $V_{cb,0}$, a switch and an inductor $L_b$. The switch is typically made up of a thyristor $T_b$ with an anti-parallel diode $D_b$. Generally, the circuit is placed in series with the transformer primary winding. Operation of the circuit begins prior to the pulse event by sending a short trigger pulse to the thyristor. The bouncer capacitor is now in series with the bouncer inductor, causing an LC oscillation with period $T_0 = 2\pi\sqrt{L_b C_b}$. The main switch $S_m$ is then triggered close to the zero crossing of the generated LC oscillation, starting the pulse event. Consequently, the klystron load experiences the voltage expressed in (4.95). As indicated, according to the first order Taylor expansion $\sin(t) \approx t$, the bouncer voltage is approximately linear around the zero crossing, i.e., effective droop cancellation may be obtained by appropriately selecting the bouncer resonance frequency and the bouncer pre-charge voltage $V_{cb,0}$ in relation to the application pulse length. The pulse event ends by opening the main switch, upon which the LC oscillation continues. Once the oscillation reverses, the anti-parallel diode conducts and recharges the bouncer capacitor. Since only a short trigger pulse was sent to the thyristor, the oscillation ends at the end of the resonance period, and the circuit has been reset in preparation for the next pulse event.

As described in [4.14]-[4.15], this bouncer circuit is widely used, particularly due to its robustness, simplicity and ease of use. Design procedures detailing selection of bouncer circuit parameters$L_b$ and $C_b$ as function of application requirements have been detailed in both [4.14] and, in particular, [4.15]. However, these publications

do not detail physical sizing of the bouncer components. Development of such sizing models is undertaken in later sections of this chapter where their implication in long pulse high power applications is demonstrated. As will be seen, the very low required resonant frequency of the LC combination and the associated large size of the passive components make use of this circuit extremely inconvenient when considering use in applications in the multi-megawatt (MW) range with pulse lengths of several milliseconds, stringent flat top requirements (< 1%) and high pulse repetition rates on the order of tens of Hz.

$$\begin{aligned} v_s(t) = \left(\frac{N_2}{N_1}\right)(v_{Cm}(t) - v_{Cb}(t)) &\approx \left(\frac{N_2}{N_1}\right)\left(\left[V_p - i_p(t)\frac{t}{C_m}\right] - k_b t\right) \\ &\approx \left(\frac{N_2}{N_1}\right)V_p \end{aligned} \tag{4.95}$$

*Variation: Passive LC bouncer with two-winding inductor*

It has been proposed that the inductive element in the classical LC bouncer circuit may be implemented as a so-called “two-winding inductor”, [4.16]-[4.17]. While operation of this circuit is identical to the classical LC bouncer, the two-winding inductor allows adaptation of the circuit voltage and current to better suit the ratings of commercially available semiconductor devices. However, in long pulse high power applications, the required passive LC bouncer circuit voltage and current are both extremely high rendering circuit adaptation meaningless. Furthermore, implementing the proposed winding structure in a way that yields the required inductance typically seen in long pulse applications is deemed impractical. For these reasons, this variation of the classical LC bouncer circuit will not be further discussed in this work.

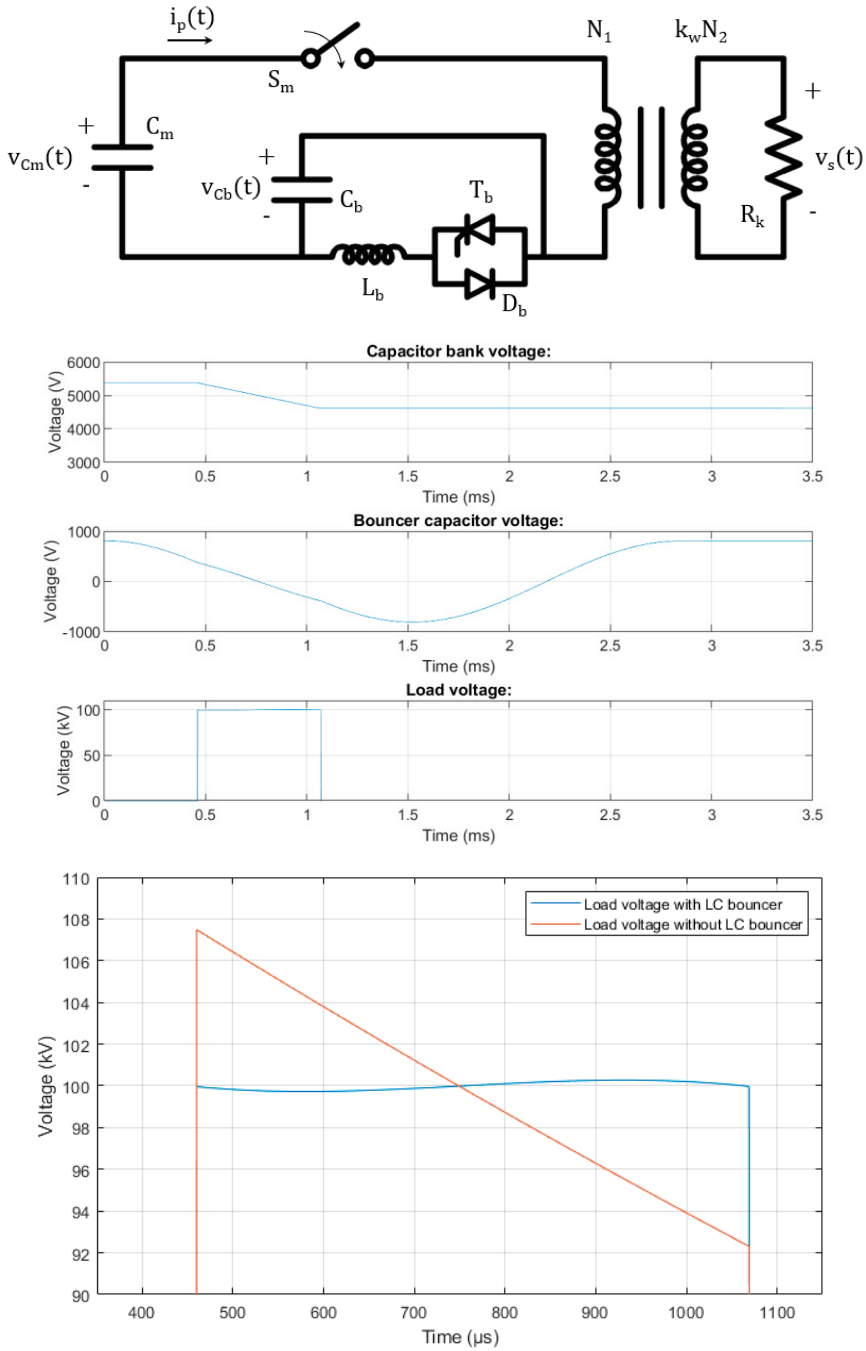



Figure 4.37: LC bouncer circuit: a) Simplified schematic of modulator using LC bouncer circuit in series with pulse transformer primary winding; b) Bouncer operation for application with $T_p$ = 600 μs, note that the capacitor bank droop is matched by the voltage trajectory of the bouncer circuit; c) Zoom on the load voltage flat top shown in (b) - combined flat top ripple and droop has been limited to ~0.5% of the flat top amplitude.

*Active electronic bouncer*

Conceptually, the electronic bouncer circuit consists of a storage capacitor $C_{in}$, a dc/dc converter, a series inductor $L_b$, and an output bouncer capacitor $C_b$, Figure 4.38. Here, the output bouncer capacitor is placed in series with the main capacitor bank and the general idea is to charge it such that the bouncer capacitor voltage matches the main capacitor bank voltage droop, (4.96), throughout the pulse event to produce a smooth pulse. To counteract the main capacitor bank droop, an output bouncer capacitor current according to (4.97) is required. The details of this process are described in the following.

$$\Delta V_{cbk} = \frac{I_2' T_p}{C_{bk}} \tag{4.96}$$

$$\bar{\imath}_{Cb} = \frac{\Delta V_{cbk} C_b}{T_p} \tag{4.97}$$

Operation of the bouncer circuit begins prior to the pulse event by closing the switch $S_b$ to short circuit the bouncer capacitor. The bouncer inductor current is then controlled to equal the to-be-generated pulse load current referred to the primary added to that of the compensation current, (4.97).

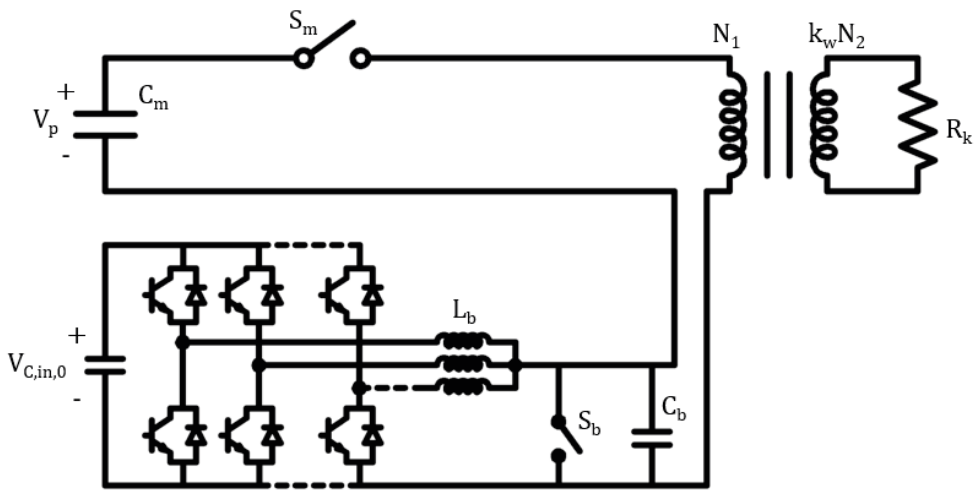



Figure 4.38: Electronic bouncer circuit

Once the bouncer inductor has been pre-charged, the pulse event may be started by closing the main switch $S_m$. At the same time, $S_b$ is opened such that the output bouncer capacitor is charged according to (4.97). Consequently, capacitor bank voltage droop is corrected and the voltage fed to the load is constant. This operational phase lasts until the end of the pulse event. The pulse event ends by opening the main switch $S_m$. Here, the bouncer dc/dc converter is turned off as well, and the energy stored in the inductor $L_b$ is allowed to charge the output bouncer capacitor. Finally, the dc/dc converter is operated in boost mode to pump the bouncer output capacitor energy back into the bouncer storage capacitor $C_{in}$. The electronic bouncer is then ready to be used in the next pulse event.

The electronic bouncer circuit has been discussed in [4.12] and [4.18]-[4.20]. Notably, [4.18] and [4.19] present important considerations in bouncer circuit control regarding pulse-to-pulse repeatability and stability, respectively. While electronic bouncers are clearly unsuitable for most pulse applications in the low microsecond range and below due to the extremely high required converter switching frequency, they may be implemented using off-the-shelf semiconductors operated at moderate switching frequencies to provide highly efficient and accurate flat top droop compensation in long pulse applications.

*Variation: hybrid bouncer circuit*

Finally, it has been proposed in [4.21] and [4.22] that the benefits of the classical LC bouncer and the electronic bouncer circuits may be combined using a hybrid circuit. Though interesting, this possibility has not been pursued in this work.

### 4.3.2 Modeling and design of passive LC bouncer circuit

Circuit analysis of the passive LC bouncer was described in [4.15]. There, a simplified dimensioning procedure for the bouncer inductor $L_b$ and the bouncer capacitor $C_b$ based on stored energy minimization was proposed. This section, first, reviews the fundamental circuit relationships developed in [4.15]. These relationships are further complemented by state space modeling to support accurate calculation of pulse flat top droop. Then, design models for the bouncer inductor, bouncer capacitor and bouncer switch are developed and integrated in an optimization procedure. In a later section, the developed design procedure is used to characterize and compare the droop compensation technique to the more advanced electronic bouncer circuit in the context of long pulse high power applications.

*Fundamental circuit relationships*

The bouncer circuit is placed in series with the primary winding and therefore experiences the full load current referred to the primary, $i_p(t)$. Assuming proper droop compensation is accomplished, the load current may be modeled as an ideal rectangular pulse, and the equivalent circuit presented in Figure 4.39 may be used in analyzing the behavior of the circuit. Basic operation of this circuit was summarized in the previous section.

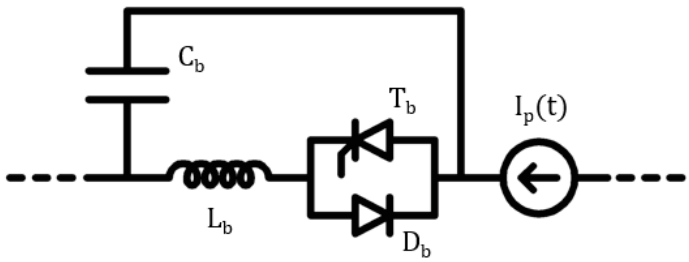



Figure 4.39: Equivalent circuit used in phase plane analysis of LC bouncer circuit

In [4.15], the relationship between the application pulse length and the bouncer resonance frequency was described by the angle $\alpha$, (4.98). With this definition, phase plane analysis was used to study the waveforms of Figure 4.37.b in developing the relationships (4.99)-(4.102). In [4.15], in addition to the application pulse length $T_p$, $I_p$ and $\Delta V_{cbk}$ were also considered constants determined by the application. Thus, by sweeping design parameters $I_r$ and $\alpha$, a set of bouncer designs could be generated. Furthermore, it was argued that the energy stored in the bouncer, proportional to the bouncer volume, generally approaches its minimum for $I_r$ = 0.5, i.e., a volume optimized bouncer may be derived from (4.102) by selecting $\alpha$ according to imposed droop requirements.

$$\alpha = \pi \frac{T_p}{T_0} = \frac{T_p}{2\sqrt{L_b C_b}} \tag{4.98}$$

$$\Delta V_c = \left(\frac{N_2}{N_1}\right)\frac{I_s T_p}{C_{bk}} = \frac{I_p T_p}{C_{bk}} \tag{4.99}$$

$$I_r = \frac{I_p}{I_{Lb,0}} \tag{4.100}$$

$$x_b = \frac{-I_r cot(\alpha) + \sqrt{1 - I_r^2 + cot^2(\alpha)}}{1 + cot^2(\alpha)} \tag{4.101}$$

$$\begin{cases} L_b = \dfrac{\Delta V_c T_p I_r}{4 x_b \alpha I_p} \\ C_b = \dfrac{I_p x_b p}{\alpha \Delta V_c I_r} \end{cases} \tag{4.102}$$

This approach is sufficient for many pulsed applications. However, several challenges arise in considering long pulse high power applications with stringent flat top requirements-

- The angle $\alpha$ is indirectly related to the obtainable flat top droop. To fully ensure droop compensation on the order of 0.15% and below, accurate simulation models are required.
- To obtain droop compensation on the order of 0.15% for a pulse length of several milliseconds, an extremely long resonant time period is necessary. This results in very large bouncer components.
- The load current referred to the primary is usually on the order of several kA. The bouncer components experience a current $I_r$ times greater than this, which with the aforementioned resonant time period corresponds to considerable peak and RMS current values.
- Given these challenges, it is also of clear interest to consider $\Delta V_{cbk}$and $I_p$ (i.e., by way of choosing $V_p$) as design variables, consequently affecting not only the bouncer but each individual modulator component. This calls for an integrated optimization procedure.

These issues are in part addressed in the following subsections-

*State space modeling of LC bouncer circuit*

A state space model is used to accurately calculate the droop corresponding to use of a given bouncer circuit. Figure 4.40 suggests two distinct circuit states useful in calculating the flat top droop. Here, the first circuit corresponds to the circumstances prior to the pulse event and is described by (4.103)-(4.104). As the pulse event is triggered, the second circuit is used with the voltages and currents calculated using the first circuit serving as initial conditions, (4.105)-(4.106). Conceivably, it would be appropriate to time the pulse event such that it would be centred around the zero crossing of the bouncer voltage waveform, i.e., $t_b = T_0/4 - T_p/2$. However, switching in the load circuit alters the trajectory of the resonant waveform, i.e., the model should be evaluated for a series of values $t_x$ such that $t_b = T_0/4 - T_p/2 - t_x$ to ensure optimal compensation for a given bouncer circuit. The combined flat

top droop and ripple may then be evaluated directly from the simulated waveform according to (4.107).

$$A = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & -1/C_b \\ 0 & 1/L_b & 0 \end{bmatrix}; B = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} \tag{4.103}$$

$$v_2(t) = 0 \tag{4.104}$$

$$A = \begin{bmatrix} -1/(R_k C_{bk}) & 1/(R_k C_{bk}) & 0 \\ 1/(R_k C_{bk}) & -1/(R_k C_{bk}) & -1/C_b \\ 0 & 1/L_b & 0 \end{bmatrix}; B = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} \tag{4.105}$$

$$v_s(t) = \left(\frac{N_2}{N_1}\right)(v_{cbk}(t) - v_{cb}(t)) \tag{4.106}$$

$$\Delta v_s = \max\left(v_s(t)\right) - \min\left(v_s(t)\right) \tag{4.107}$$

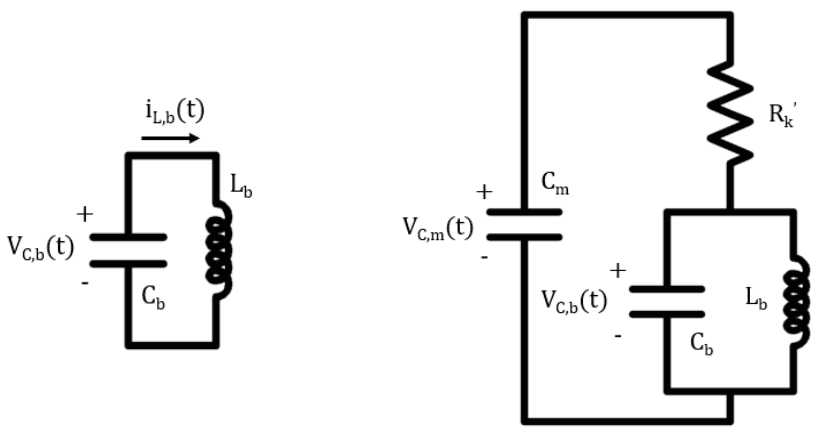



Figure 4.40: Circuit states used in state space modeling of LC bouncer circuit- a) circuit used prior to and following the pulse event; b) circuit used during pulse event.

*LC bouncer capacitor design*

Once the bouncer capacitance $C_b$ has been determined from (4.102), appropriate capacitors must be selected for implementation. Here, the general capacitor selection procedure outlined in Appendix A is followed. In particular, it must be ensured that the selected capacitor unit can withstand the resulting per-capacitor peak and RMS currents associated with bouncer operation and as shown in Figure 4.41. Generally, the RMS value of the bouncer current, $I_b$, may be calculated from (4.108) with the definitions shown in (4.109). This results in the general expression (4.110). As noted, however, for long pulse high power applications $T_0 \gg T_p$ and the

expression shown in (4.111) may be used. Furthermore, in such applications the RMS current may be on the order of several kA. Hence, in this work a catalogue of heavy-duty AC capacitors from the Electronicon capacitor family E62HC has been adopted [4.23].

$$I_b = \sqrt{f_r \int_0^{1/f_r} (i_b(t))^2 dt} = \sqrt{f_r T_0} \sqrt{\frac{1}{T_0} \int_0^{T_0} (i_b(t))^2 dt} \tag{4.108}$$

$$i_b(t) = \begin{Bmatrix} t < \frac{T_0}{4} - \frac{T_p}{2}: & \hat{I}_b \sin(\omega_0 t) \\ \frac{T_0}{4} - \frac{T_p}{2} \le t \le \frac{T_0}{4} + \frac{T_p}{2}: & (\hat{I}_b - I_p) \sin(\omega_0 t) \\ t > \frac{T_0}{4} + \frac{T_p}{2}: & \hat{I}_b \sin(\omega_0 t) \end{Bmatrix} \tag{4.109}$$

$$I_b = \sqrt{f_r T_0} \sqrt{\frac{1}{T_0}\left(\frac{\hat{I}_b}{2} T_0 + I_p^2 T_p - \frac{2\hat{I}_b I_p}{\omega_0}\left[cos\left(\omega_0\left[\frac{T_0}{4} + \frac{T_p}{2}\right]\right) - cos\left(\omega_0\left[\frac{T_0}{4} - \frac{T_p}{2}\right]\right)\right]\right)} \tag{4.110}$$

$$\rightarrow \{T_0 \gg T_p\} \rightarrow I_b = \sqrt{f_r T_0} \frac{\hat{I}_b^2}{\sqrt{2}} \tag{4.111}$$

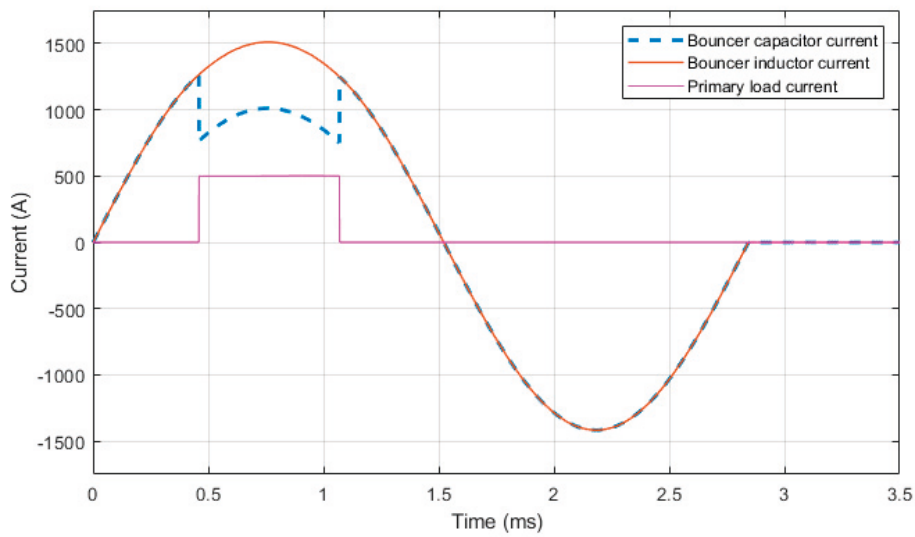



Figure 4.41: Overview of passive LC bouncer circuit currents

*LC bouncer inductor design*

As has been indicated, in order to effectively compensate for the capacitor bank droop without exceeding the imposed flat top ripple constraint, the resonant frequency of the passive bouncer circuit must be very low. Combined with the very large peak and RMS current values of the bouncer circuit, (4.109)-(4.111), this results in the requirement of a very large bouncer inductor. For these reasons use of an air core solenoid inductor is proposed, Figure 4.42. Here, $N$ winding turns of diameter $\Phi_w$ are wound in $l$ layers around a circular bobbin with diameter $2r_b$.

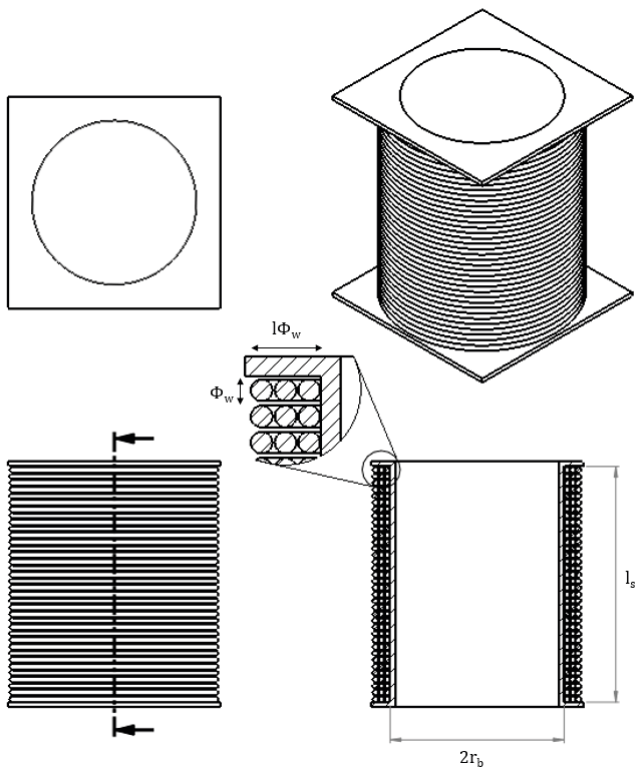



Figure 4.42: Overview of solenoid inductor geometry suitable for high current applications

The winding wire diameter $\Phi_w$ is determined by (4.112). For $l$ layers, this corresponds to a solenoid length of (4.113). The inductance of the structure is then approximated by (4.114), i.e., selection of the inductor number of turns $N$ yields the required solenoid radius $r_b$. Often, as indicated in (4.113)-(4.114), $l_i$ and $r_b$ are constrained by system size limitations and other practical reasons.

$$\emptyset_w = \sqrt{\frac{4I_b}{\pi J}} \tag{4.112}$$

$$l_i = \emptyset_w N_l \leq \hat{l}_i \tag{4.113}$$

$$L = \mu_0 \pi r_b^2 \frac{N^2}{l_i} \rightarrow r_b = \sqrt{\frac{L_b l_i}{\mu_0 \pi N^2}} \leq \hat{r}_b \tag{4.114}$$

The mean path length of solenoid winding turns is estimated by (4.115), yielding the inductor volumetric power loss density as (4.116). While bouncer efficiency is an important issue in itself, it must also be ensured that the inductor can withstand the corresponding temperature rise. Assuming 1) a uniform power loss distribution throughout the solenoid coil and 2) that the majority of the power dissipation is removed by natural convection from the surface of the outermost solenoid layer, the temperature rise may be estimated by (4.117). Here, the temperature rise is limited to some value $\hat{T}$.

$$[MPL]_i = 2\pi(r_b + \emptyset_w l/2) \tag{4.115}$$

$$p_{cu} = \rho_{cu} J^2 T_0 f_r \tag{4.116}$$

$$T_h = T_a + \frac{p_{cu} V_{cu}}{2\lambda_{eq}} + \frac{p_{cu}(\emptyset_w l)^2}{2hA_s} \leq \hat{T} \tag{4.117}$$

The procedure is summarized in Figure 4.43. Note that, due to the simple geometry, there are only two design parameters - $N$ and $l$ - both of which are relatively well constrained integers. Consequently, the optimal inductor design can often quickly be found by evaluating the procedure for the entire parameter space and applying an appropriate objective function, (4.118). Here, $V_i$ is the inductor extent volume defined by (4.119), $P_{i,cu}$, is the total inductor power loss defined by (4.120), $V_{i,n}$ and $P_{i,n}$ are normalization factors, and $K$ is a weighting factor. Alternatively, all viable solutions can be stored and included as part of a larger set of solutions, e.g., complete bouncers or complete modulator systems.

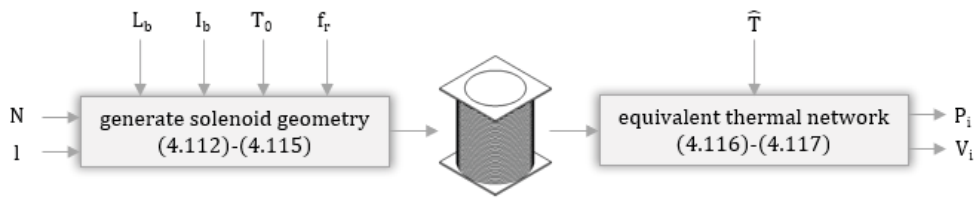



Figure 4.43: Solenoid bouncer inductor design procedure

$$f(x) = \frac{p_{cu} V_{cu}}{P_{i,n}} K + \frac{V_i}{V_{i,n}} (1 - K) \tag{4.118}$$

$$V_i = \pi (r_b + \emptyset_w l)^2 l_i \tag{4.119}$$

$$P_i = \rho_{cu} V_{cu} J^2 T_0 f_r = \rho_{cu} N \pi (\emptyset_w / 2)^2 [MPL]_i J^2 T_0 f_r \tag{4.120}$$

*LC bouncer switch design*

As noted, the LC bouncer switch is generally a thyristor with an antiparallel diode. A short pulse on the thyristor gate triggers the LC oscillation. From the perspective of the bouncer current, Figure 4.41, the thyristor conducts the positive half-cycle whereas the diode conducts the negative half-cycle. Clearly, both the thyristor and the diode must be rated for both the full bouncer voltage $V_{cb,0}$ as well as the full bouncer current $\hat{I}_b = I_p / I_r$. Furthermore, the power losses generated in switch conduction must be limited to 1) ensure high efficiency operation, and to 2) ensure that the associated junction temperature profile neither exceeds the limitations of the switch nor deteriorates device lifetime. Here, a catalogue of suitable thyristors and diodes from ABB was assembled storing for each component reference the repetitive peak reverse voltage, the maximum average forward current, the maximum RMS forward current, the device threshold voltage, the slope resistance, the thermal resistance (separate entries are included to account for cooling applied to the anode side, the cathode side or both sides) and the transient thermal impedance parameters. The developed design procedure is described in the following and is summarized in Figure 4.44.

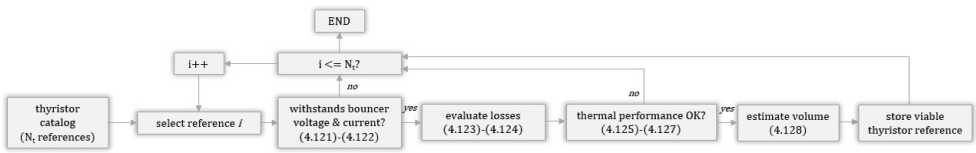



Figure 4.44: Design procedure for bouncer switch

To design an appropriate switch assembly, the following steps are carried out for each thyristor reference in the assembled catalogue of commercially available thyristors. First, it is ensured that the thyristor reference under consideration can withstand the full bouncer voltage as well as the full bouncer current with margin, (4.121)-(4.122).

$$k_v V_{cb,0} \leq V_{dwm} \tag{4.121}$$

$$k_i \hat{I}_b/\pi \leq I_{avm} \tag{4.122}$$

Since the thyristor conducts during the positive half cycle, the average conduction loss *during the pulse* may be calculated according to (4.123) whereas the total average conduction loss may be calculated according to (4.124).

$$\hat{P}_{cond} = V_{T,0}\hat{I}_b/\pi + r_T(\pi/2)^2\left(\hat{I}_b/\pi\right)^2 \tag{4.123}$$

$$\bar{P}_{cond} = \left[V_{T,0}\hat{I}_b/\pi + r_T(\pi/2)^2\left(\hat{I}_b/\pi\right)^2\right] f_r T_0 \tag{4.124}$$

The thermal resistance is a datasheet parameter termed $R_{th}$, whereas the thermal impedance is calculated according to (4.125), where $R_i$ and $\tau_i$ are the Foster network datasheet parameters.

$$Z_{th,j-c}(t) = \sum_{i=1}^{n} R_i\left(1 - e^{-t/\tau_i}\right) \tag{4.125}$$

Consequently, the average junction temperature may be calculated from (4.126), whereas the junction temperature swing is given by (4.127).

$$\bar{T}_j = T_a + R_{th}\bar{P}_{cond} \tag{4.126}$$

$$\Delta T_j = Z_{th,j-c}(T_0)\left[V_{T,0}\hat{I}_b/\pi + r_T(\pi/2)^2\left(\hat{I}_b/\pi\right)^2\right] \tag{4.127}$$

Finally, the thyristor switch volume is given by (4.128).

$$V_t = \emptyset_t^2 h_t \tag{4.128}$$

From the perspective of bouncer circuit operation, the diode is characterized by essentially the same parameters as the thyristor and is furthermore subjected to essentially the same current waveform, though during the negative half cycle. Therefore, the same steps are adopted and carried out for each diode reference in the assembled catalogue of commercially available diodes. Components that do not fulfil the requirements specified by constraints corresponding to equations (4.121)-

(4.122) are rejected. Each of the remaining thyristor/diode permutations may then be evaluated by an objective function, (4.129).

$$f(x) = \frac{V_t + V_d}{V_n} k + \frac{\bar{P}_{cond,t} + \bar{P}_{cond,d}}{P_n} (1 - k) \tag{4.129}$$

*LC bouncer design procedure*

A complete LC bouncer design procedure is described in the following and is summarized in Figure 4.45. In accordance with the analysis detailed in [4.15], $\alpha$ and $I_r$ are the main design variables. Here, selection of $\alpha$ is bounded by the fact that the resonant time period $T_0$ cannot exceed the time period defined by the pulse repetition rate, (4.130). Then, once $\alpha$ and $I_r$ have been selected, $L_b$ and $C_b$ may be calculated from (4.99)-(4.102) as described in [4.15]. State space analysis is then carried out to 1) minimize the obtainable combined flat top ripple and droop, and to 2) ensure that the combined flat top ripple and droop does not exceed application requirements. If this cannot be guaranteed, the design procedure is terminated and this combination of $\alpha$and $I_r$ must be considered non-viable. On the other hand, if the combined flat top ripple and droop is within the limits prescribed by the application, the LC bouncer components are to be designed. As mentioned in the sections detailing component design, each component may be designed individually resulting in a single LC bouncer design. Alternatively, a large set of viable designs may be generated for each component, i.e., viable permutations generated from a combination $<\alpha; I_r>$ may be evaluated by a general objective function (4.131), allowing a choice from a set of viable LC bouncer designs.

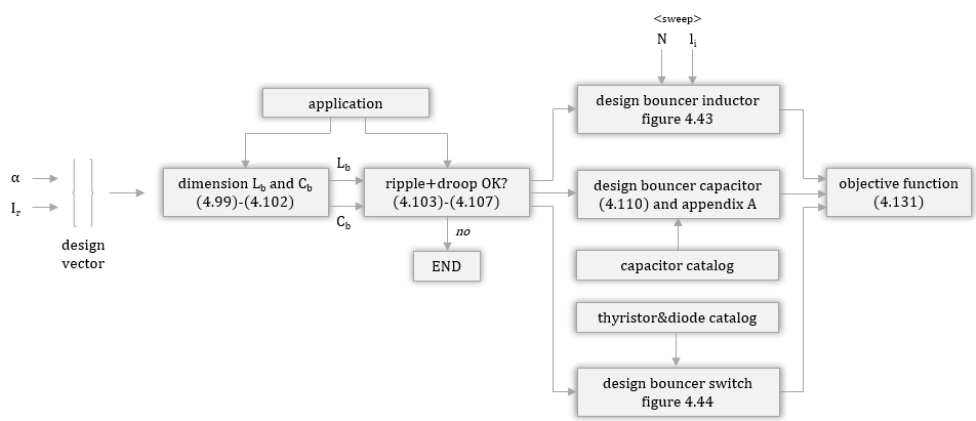



Figure 4.45: Complete LC bouncer design procedure

$$T_0 = \pi \frac{T_p}{\alpha} \leq 1/f_r \tag{4.130}$$

$$f(x) = \frac{V_c + V_i + V_t + V_t}{V_n} k + \frac{P_i + \bar{P}_{cond,t} + \bar{P}_{cond,d}}{P_n} (1 - k) \tag{4.131}$$

### 4.3.3 Modeling and design of electronic bouncer

Circuit analysis of the electronic bouncer circuit has been described in, e.g., [4.18]-[4.20]. Furthermore, the author has published a paper on optimal design of electronic bouncers, [4.12]. This section reviews and expands on the content published in [4.12].

*Design of electronic bouncer energy storage*

Firstly, the bouncer energy storage capacitor $C_{in}$ must hold enough energy to be able to bring the bouncer output capacitor to a voltage at least equalling the main capacitor bank voltage droop. For a linearly increasing bouncer output voltage and with $i_{Cb} \ll I_2'$, the required stored energy is well estimated by (4.132). Here, the smallest possible capacitor configuration is obtained if the energy storage is fully utilized, i.e., if the energy storage capacitor voltage equals the bouncer output voltage at the end of the pulse, (4.133). An appropriate capacitor configuration is chosen using the capacitor selection procedure outlined in Appendix A, ensuring that the peak voltage as well as the peak and rms currents are withstood.

$$E_{C,in} \geq E_{out} = \frac{\hat{V}_{Cb} I_2' T_p}{2} \tag{4.132}$$

$$C_{in} = \frac{2E_{out}}{V_{C,in}^2 - \hat{V}_{Cb}^2} \tag{4.133}$$

*Notes on output pulse flat top ripple*

It is well known that PWM operation of power converters is associated with output voltage ripple. In this case, the generated output voltage ripple is amplified by the pulse transformer and seen in the pulse flat top. The remaining bouncer components - namely the dc/dc converter, the bouncer inductor and the bouncer output capacitor - all greatly impact the generated output voltage ripple. Given the stringent requirements on flat top ripple and droop, design of these components must include restrictions on their effects on ripple generation. For electronic bouncer circuits, two main sources of flat top voltage ripple exist-

First, as is well known, output voltage ripple often emanates from the inductor current ripple generated in PWM-based switching. Assuming that the output capacitor absorbs the full ripple current, the generated output voltage ripple for a given current ripple may generally be calculated from (4.134), [4.12]. For a single-phase dc/dc converter, the current ripple is given by (4.135) and the resulting output voltage ripple is calculated from (4.136).

$$\Delta V_{o,p-p} = \frac{1}{8}\frac{\Delta i_L}{C_b f_{sw}} \tag{4.134}$$

$$\Delta i_L = \frac{V_{in}(\delta - \delta^2)}{L_b f_{sw}} \tag{4.135}$$

$$\Delta V_{o,p-p} = \frac{1}{8}\frac{V_{in}(\delta - \delta^2)}{L_b C_b f_{sw}^2} \tag{4.136}$$

However, use of a multiphase converter allows phase interleaving for ripple reduction. This class of converter is also advantageous as it permits current sharing between transistor modules (it should be kept in mind that the electronic bouncer itself is a high-power pulsed converter). Here, Figure 4.46 shows the converter phase currents for a 2-phase dc/dc converter interleaved by 180 degrees. Though the per-phase ripple is the same as that given by (4.135), the converter output sees the sum of the phase currents, i.e., significant ripple cancellation is possible, Figure 4.46. Adding additional converter phases further reduces the output current ripple at the price of added component count and circuit complexity. Here, Figure 4.47 shows the output voltage ripple reduction ratio as a function of converter duty cycle with the number of phases as parameter.

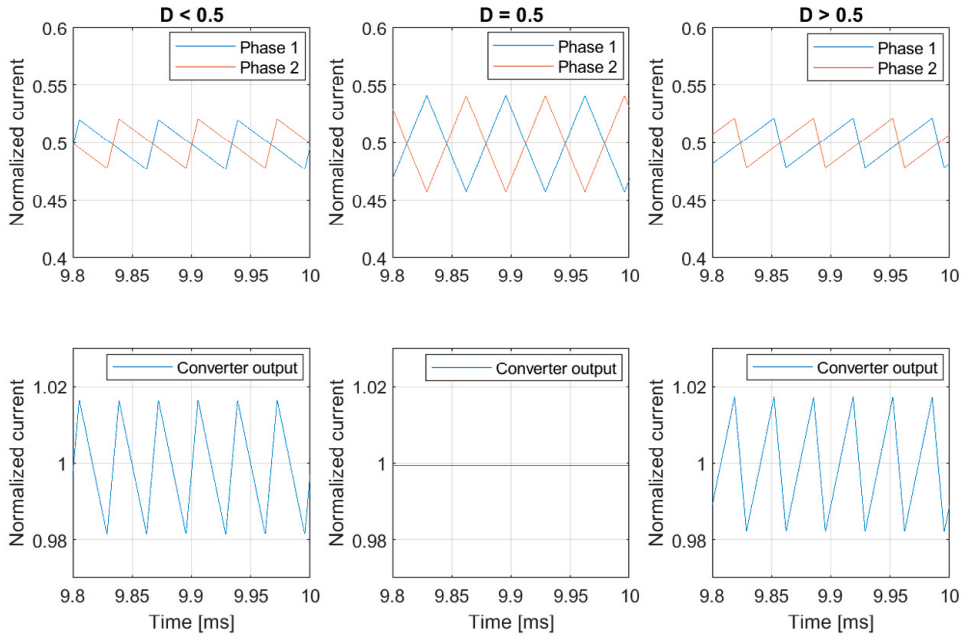



Figure 4.46: Converter currents for interleaved 2-phase dc/dc converter. Whereas the per-phase current ripple has its maximum for D = 0.5, equation (4.135), the corresponding total converter output current ripple is zero, Figure 4.47.

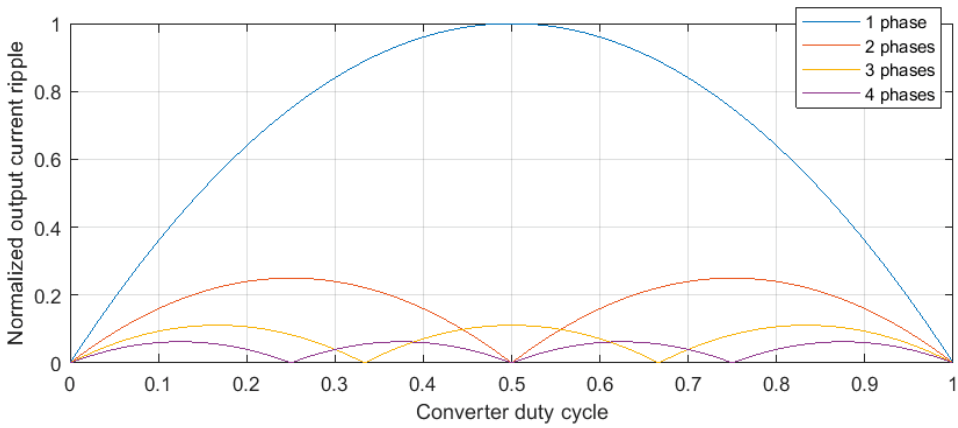



Figure 4.47: Normalized converter output voltage ripple reduction ratio for interleaved dc/dc converter as a function of duty cycle with the number of converter phases as parameter

As the voltage on the bouncer output varies throughout the pulse event, the worst-case ripple should be considered and limited to be conservatively within application ripple requirements. Following the procedure for calculating bouncer output current ripple for multiphase dc/dc converters outlined in [4.24]-[4.25], the largest possible capacitor current ripple may be calculated from (4.137). Substituting (4.137) into

(4.134), the corresponding flat top ripple may be calculated according to (4.138). In these equations, $V_{Cin,0}$ is the initial (charged) bouncer input voltage and $N_2/N_1$ represents the transformer turns ratio.

$$\Delta\hat{\imath}_{Cb} = \frac{V_{Cin,0}}{4L_b f_{sw} N_m} \tag{4.137}$$

$$\Delta V_{pp,fsw} = \frac{V_{Cin,0}}{32L_b C_b (N_m f_{sw})^2}\left(\frac{k_w N_2}{N_1}\right) \tag{4.138}$$

Then, in addition to the aforementioned issue, a second source of output voltage ripple in multiphase converters used in electronic bouncers emerges due to the continuous variation in converter duty cycle. As noted in the preceding section, the bouncer energy storage is chosen so as to minimize the volume of the storage capacitor configuration. Thus, the converter duty cycle will vary linearly from ~0 to ~1 throughout the pulse duration. Consequently, the ripple reduction ratio due to phase interleaving will also vary in time. From Figure 4.47, it should be understood that this corresponds to a sinusoidal envelope around the current ripple. Intuitively, this ripple has frequency $N_m/T_p$ and the worst-case peak-to-peak ripple at this frequency is given by (4.139).

$$\Delta V_{pp,i} = \frac{\Delta\hat{\imath}_{Cb} T_p}{\pi N_m C_b} \tag{4.139}$$

In designing a suitable electronic bouncer circuit, the bouncer inductance and the bouncer output capacitance must be chosen considering an $N_m$-phase converter operated at switching frequency $f_{sw}$ to limit the generated voltage ripple according to application requirements.

*Design of electronic bouncer dc/dc power converter*

In designing the dc/dc converter, it should be kept in mind that the bouncer circuit experiences at least the full primary load current, typically on the order of several kA. Furthermore, as bouncer operation is essentially limited to the pulse event itself, operation entails power cycling at pulse frequency $f_r$ and the semiconductor modules must be carefully selected taking this into account. For these reasons, it is often advantageous to utilize a multiphase dc/dc converter to 1) split the current between phases and to 2) obtain output voltage ripple reduction due to phase interleaving. Such a converter is depicted in Figure 4.48. Here, the current is split among $N_m$ converter phases each made up of $N_s$ parallel modules.

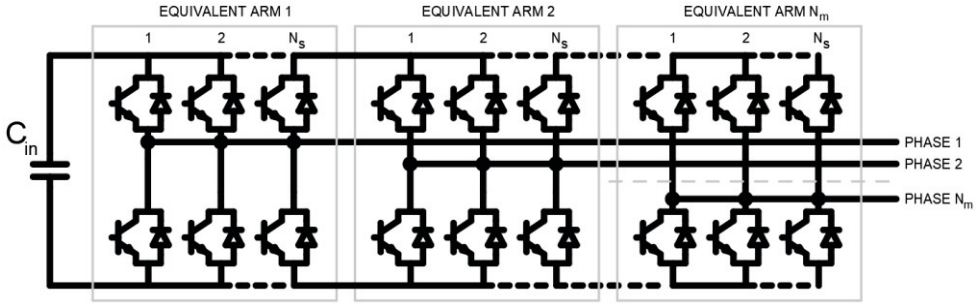



Figure 4.48: Multiphase dc/dc converter with Nm phases and Ns parallel modules per phase

For this converter, the module conduction and switching losses *during the pulse* are given by (4.140)-(4.143). Here, $\bar{\delta}$ is the average converter duty cycle given by (4.144) provided the energy storage has been designed as indicated in a preceding section. Finally, the average converter losses are given by (4.145).

$$P_{IGBT,c} = \left[V_{ce,0} + r_{ce}\frac{I_2' + \bar{\imath}_{Cb}}{N_m N_s}\right]\frac{I_2' + \bar{\imath}_{Cb}}{N_m N_s}\bar{\delta} \tag{4.140}$$

$$P_{IGBT,sw} = f_{sw}E_{sw}\left[\frac{\frac{I_2' + \bar{\imath}_{Cb}}{N_m N_s}}{I_{c,ref}}\right]^{K_{i-i}}\left[\frac{\bar{D}V_{Cin,0}}{V_{ce,ref}}\right]^{K_{v-i}} \tag{4.141}$$

$$P_{diode,c} = \left[V_{f,0} + r_f\frac{I_2' + \bar{\imath}_{Cb}}{N_m N_s}\right]\frac{I_2' + \bar{\imath}_{Cb}}{N_m N_s}\left(1 - \bar{\delta}\right) \tag{4.142}$$

$$P_{diode,sw} = f_{sw}E_{rr}\left[\frac{\frac{I_2' + \bar{\imath}_{Cb}}{N_m N_s}}{I_{f,ref}}\right]^{K_{i-d}}\left[\frac{\bar{D}V_{Cin,0}}{V_{f,ref}}\right]^{K_{v-d}} \tag{4.143}$$

$$\bar{\delta} = \frac{\hat{V}_{Cb}/2}{V_{Cin,0}} \tag{4.144}$$

$$\bar{P}_{dc/dc} = \left[P_{IGBT,c} + P_{IGBT,sw} + P_{diode,c} + P_{diode,sw}\right]N_s N_m f_r T_p \tag{4.145}$$

With the power losses estimated by (4.140)-(4.145), estimation of the thermal performance of the power converter is possible. Here, the semiconductor selection procedure outlined in Appendix B is adopted, allowing characterization and comparison of complete converters based on commercially available semiconductor modules. In order to find a suitable design, the number of phases, the converter switching frequency and the semiconductor module must be carefully selected together with appropriate design of the bouncer inductor and bouncer output

capacitor to ensure application requirements are met while optimizing converter performance and limiting converter complexity.

*Design of electronic bouncer inductor*

The bouncer inductor connects the output of the dc/dc converter to the bouncer output capacitor. In case a multiphase dc/dc converter is used it is necessary to utilize either 1) one bouncer inductor per phase leg, or 2) a single multiphase inductor coupling the phase legs, [4.26]-[4.27]. In the application of interest, the primary current is very high, typically on the order of several kA. Furthermore, high switching frequency is usually needed to meet the stringent flat top ripple requirements. With these considerations in mind, a toroidal air core-type inductor is appropriate. The basic geometry is summarized in Figure 4.49.

In this formulation, the toroidal inner radius $A$, the toroidal outer radius $B$, the toroidal height $H$ and the inductor number of turns $N$ are considered design parameters. From these parameters, the inductance $L_b$ of the structure is estimated by (4.146), [4.28].

$$L_b = \mu_0 N^2 \frac{H}{2\pi} log\left(\frac{B}{A}\right) \tag{4.146}$$

The full bouncer current was earlier given in (4.109). For a multiphase pulsed converter, the RMS current per inductor unit may be calculated from (4.147). From this, the required winding conductor cross sectional area is estimated by (4.148), and the equivalent cross-sectional area of the winding is given by (4.149).

$$I_{L,b} = \frac{\left[I_2' + \frac{\Delta V_{cbk} C_b}{T_p}\right]}{N_m} \sqrt{T_p f_r} \tag{4.147}$$

$$A_{cu} = \frac{I_{L,b}}{J} \tag{4.148}$$

$$A_w = \frac{N A_{cu}}{k_{f,cu}} \tag{4.149}$$

From this, the winding width $W$ is calculated according to (4.150). Intuitively, $A_w \leq \pi A^2$, Figure 4.49.

$$W = A - \sqrt{A^2 - A_w/\pi} \tag{4.150}$$

In addition to the above characterization, it is important to ensure that the candidate inductor design is thermally viable, i.e., the winding hotspot temperature should not exceed its thermal classification. Here, per-volume losses are given by (4.151). Then, estimating the effective copper volume according to (4.152), the hotspot temperature is estimated from a linear equivalent thermal network assuming 1) uniformly distributed loss dissipation and 2) convective heat transfer at the inductor surface, (4.153)-(4.154). In these equations, $\rho_{cu}$ is the conductivity of copper, $F_R$ is the AC resistance factor, $h$ is the equivalent heat transfer coefficient, $\lambda_{eq}$ is the equivalent thermal resistivity of the winding, $T_h$ is the resulting hot-spot temperature, and $T_{max}$ is the maximum permissible hot-spot temperature.

$$P_{i,v} = \rho_{cu} F_R J^2 \tag{4.151}$$

$$V_{cu} = NA_{cu}[MPL] \cong NA_{cu}[2(B - A + W) + 2(H + W)] \tag{4.152}$$

$$A_s \cong 2\pi((B + W)^2 - (A - W)^2 + H(B + A)) \tag{4.153}$$

$$T_h = T_a + \frac{P_{i,v} V_{cu}}{hA_s} + \frac{P_{i,v} W^2}{2\lambda_{eq}} \leq T_{max} \tag{4.154}$$

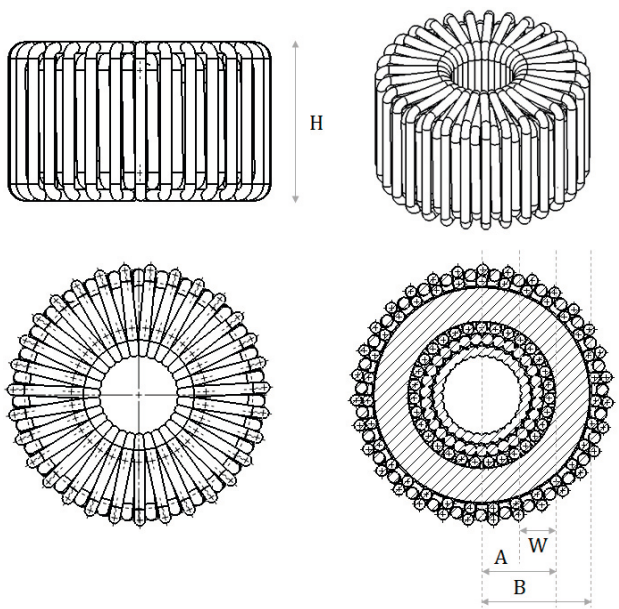



Figure 4.49: Overview of toroidal inductor adopted for use in electronic bouncer circuit

Provided the design is thermally viable, (4.154), the design is evaluated in terms of dissipated power, (4.155), and its extents volume, (4.156). As noted, multiphase converters require one inductor per phase leg, i.e., total loss and volume are obtained by multiplication with $N_m$.

$$P_i = P_{i,v} V_{cu} \tag{4.155}$$

$$V_i \approx \pi (B + W)^2 (H + 2W) \tag{4.156}$$

*Design of electronic bouncer output capacitor*

The bouncer output capacitor is placed in series with the main capacitor bank and is charged in counteracting flat top droop. The output capacitor must be chosen to conservatively limit the theoretical worst-case ripple at the frequencies $f_{sw}$ and $N_m/T_p$, (4.138)-(4.139).

In addition to selecting the capacitance value $C_b$, it must also be ensured that the chosen capacitor configuration can withstand the resulting peak voltage as well as the necessary peak and RMS currents. The bouncer output capacitor charging current was provided in (4.97) whereas the worst-case current ripple was given in (4.137). From this, worst case peak and RMS currents are given in (4.157)-(4.158). As aforementioned, the energy in the bouncer inductors is allowed to shift to the bouncer output capacitor following the end of the pulse event corresponding to a voltage increase, (4.159). It must be ensured that the chosen capacitor model can withstand this peak voltage.

$$\hat{\imath}_{Cb} = \bar{\imath}_{Cb} + \Delta\hat{\imath}_{Cb}/2 \tag{4.157}$$

$$I_{Cb} = \sqrt{{\bar{\imath}_{Cb}}^2 + \left(\frac{\Delta\hat{\imath}_{Cb}}{2\sqrt{3}}\right)^2} \tag{4.158}$$

$$\hat{V}_{Cb} = \sqrt{\Delta V_{cbk}^2 + \frac{L_b {I_2'}^2}{N_m C_b}} \tag{4.159}$$

Here, (4.157)-(4.159) are used in selecting an appropriate bouncer capacitor configuration according to the developed capacitor selection procedure outlined in Appendix A using a catalogue of high current capacitors from Electronicon families E53 and E55, [4.29].

*Electronic bouncer optimization procedure*

A complete electronic bouncer design procedure is described in the following and is summarized in Figure 4.50. Here, the number of converter phases, the converter switching frequency, the bouncer input voltage as well as the bouncer inductor geometry ($A$, $B$, $H$, $N$) are considered the main design parameters. Additional interleaved converter phases allow reduction in switching frequency and hence improved efficiency. Here, $N_m$ is limited by complexity constraints whereas $f_{sw}$ is bounded by the limitations of the chosen semiconductor technology [4.30]. For a given converter configuration, $L_b$, $C_b$ and $C_{in}$ are dimensioned according to the procedures outlined in the preceding sections.

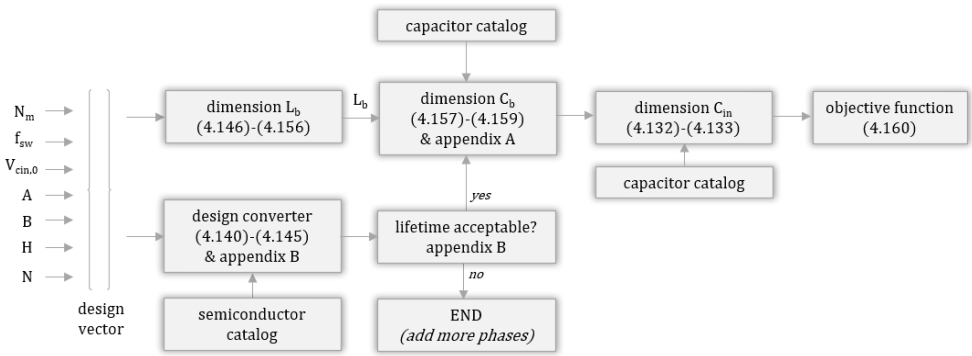



Figure 4.50: Design procedure for electronic bouncer circuit

Finally, the design is evaluated according to the objective function specified in (4.160). It is pointed out that as though the bouncer circuit experiences the full load current, the bouncer only outputs a fraction of the load voltage (i.e., the droop). Thus, the average converted power is typically 5-10% of the load power (for droop between 10-20%), i.e., electronic bouncer losses are often negligible from the perspective of modulator efficiency. This matter is further treated in the following section.

$$f(x) = \frac{V_{dc/dc} + V_i + V_{Cb} + V_{Cin}}{V_n} k + \frac{\bar{P}_{dc/dc} + P_i}{P_n} (1 - k) \tag{4.160}$$

### 4.3.4 Case study: bouncer system for ESS modulator requirements

In this section, the passive LC bouncer and the electronic bouncer are studied and compared in view of the ESS application requirements. The most important requirements in view of bouncer operation are summarized in Table 4.3.

Table 4.3: Summary of ESS modulator requirements for bouncer design

| Symbol | Quantity | Value |
|---|---|---|
| $V_2$ | Rated output voltage | 115 kV |
| $I_2$ | Rated output current | 100 A |
| $T_p$ | Pulse length | 3.5 ms |
| $f_r$ | Pulse repetition rate | 14 Hz |
| - | Maximum peak-to-peak flat top ripple | 0.15% |
| - | Maximum flat top droop | 0.15% |

*Design of modulator capacitor bank energy storage*

As noted in the introduction to this chapter, the purpose of a bouncer circuit is to counteract droop without resorting to oversizing the capacitor bank energy storage. Thus, the resulting capacitor bank itself should be included in the comparison of circuits and designs. Here, the capacitor bank must be rated for the full primary side voltage, $V_p$, and be able to carry the full load current referred to the primary, $I_2'$. The required capacitance value of the capacitor bank for a given droop $\Delta V_{cbk}$ is estimated by (4.161), and an appropriate capacitor configuration is selected using the procedure outlined in Appendix B. Here, high voltage power electronics capacitors from the Electronicon capacitor family E51 are considered. In the following comparisons the capacitor bank voltage droop is swept from 1% to 30% of the primary voltage, resulting in a variety of bouncer designs to be evaluated in terms of system volume, system losses and generated flat top ripple.

$$C_{bk} = \frac{I_2' T_p}{\Delta V_{cbk}} = \frac{I_2' T_p}{p V_p} \tag{4.161}$$

*Setup of passive LC bouncer design procedure*

The design procedure shown in Figure 4.45 is used in generating viable LC bouncer designs for the requirements specified in Table 4.3. For a given capacitor bank voltage droop, $I_r$ is allowed to vary between 0 to 1 and $\alpha$ is allowed to vary between 0 and $\pi/2$. Furthermore, several primary voltage levels between 3 kV and 6 kV are considered. Though the primary voltage also has an effect on the other parts of the modulator, these effects are not considered in the following analysis but are treated in a later section. In addition to the basic bouncer requirements shown in Figure 4.45, the maximum peak bouncer current is limited to 10 kA whereas the bouncer voltage referred to the secondary is restricted to be below 15% of the output voltage

amplitude. A catalogue of heavy-duty AC capacitors from the Electronicon capacitor family E62HC are used in selecting an appropriate configuration for the bouncer capacitor [4.23]. Suitable devices for the bouncer switch are selected from a catalogue of thyristors and diodes assembled from ABB, [4.31] and [4.32], respectively. In designing the inductor, between 1 to 1000 winding turns are allowed to be wound in between 1 to 3 layers, Figure 4.42. Finally, though the absolute peak-to-peak ripple requirement of the ESS application is 0.15% of the output voltage amplitude, the allowable ripple constraint is varied between 0.15% to 1% to investigate the effect on circuit viability due to this requirement.

*Setup of electronic bouncer design procedure*

The design procedure shown in Figure 4.50 is used in generating viable electronic bouncer designs for the requirements specified in Table 4.3. For the electronic bouncer circuit, a primary voltage of 3 kV is considered, with the capacitor bank voltage droop swept according to the above. A dc/dc converter with multiple interleaved phase legs is considered. Here, the design procedure in appendix B is adopted using a catalogue of IGBT switches assembled from Mitsubishi and SEMIKRON datasheets, [4.33]-[4.34]. The converter switching frequency is allowed to vary from 1 kHz up to some maximum determined by the guidelines specified in [4.30]. For the per-phase bouncer inductor, the number of turns is allowed to vary between 1 to 1000 whereas the toroid outer radius and the toroid height are allowed to be as large as 0.5 m and 0.3 m, respectively. The bouncer input capacitor and the bouncer output capacitors are designed using the procedure outlined in appendix A using catalogues of high current capacitors from Electronicon families E53 and E55.

Figure 4.51 depicts design results derived from the above conditions considering an electronic bouncer based on a dc/dc converter with three interleaved phase legs. Here, the optimization weighting factor $k$ has been swept from 0 to 1 to study trade-offs between efficiency and system volume (given by adding the capacitor bank volume to the estimated electronic bouncer volume) in design, (4.160). In Figure 4.51, the ratio between bouncer losses and the rated modulator output power is a parameter considered to express the contribution of the bouncer losses to the total modulator efficiency. As noted, and as seen in Figure 4.51, the electronic bouncer circuit only needs to convert a fraction of the modulator power, i.e., its effect on modulator efficiency is minimal. Hence, the trade-off depicted in Figure 4.51 is largely negligible and, for the purposes of generating an accurate comparison, the objective function specified in (4.160) will henceforth be reformulated to that of (4.162) to focus on finding practical solutions minimizing system volume. In the following, dc/dc converters with between one to five interleaved phase legs are considered.

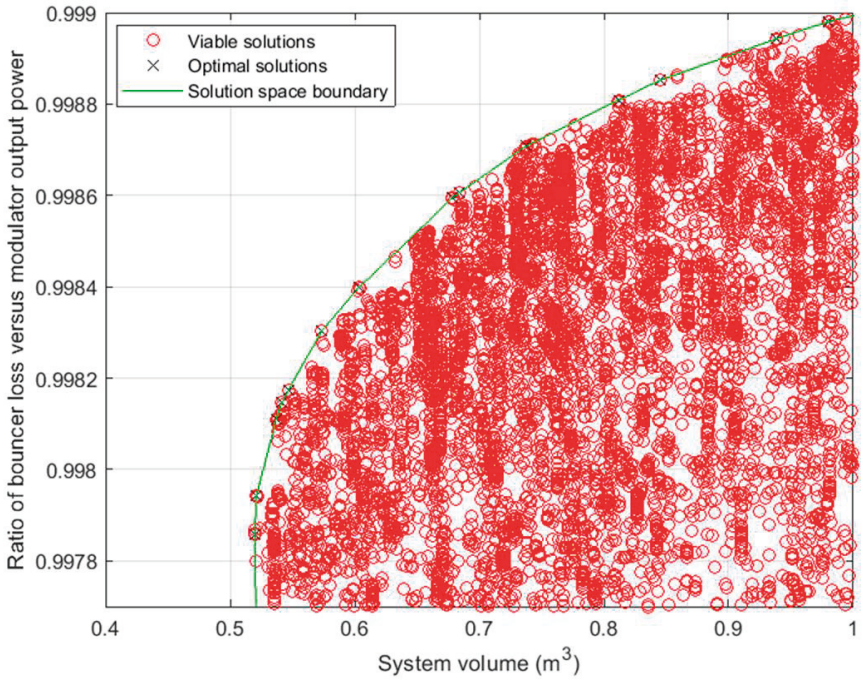



Figure 4.51: Optimization results

$$f(x) = \left[V_{dc/dc} + V_i + V_{Cb} + V_{Cin}\right] \tag{4.162}$$

*Results: comparison*

Evaluating the design procedures for the conditions outlined in the preceding sections, the results shown in Figure 4.52 are generated. Here, the system volume (capacitor bank volume added to the respective bouncer volume) and the corresponding bouncer losses are graphed versus the generated flat top ripple. Designs based on the passive LC bouncer circuit are represented with circles whereas designs based on the electronic bouncer circuit are represented by the line.

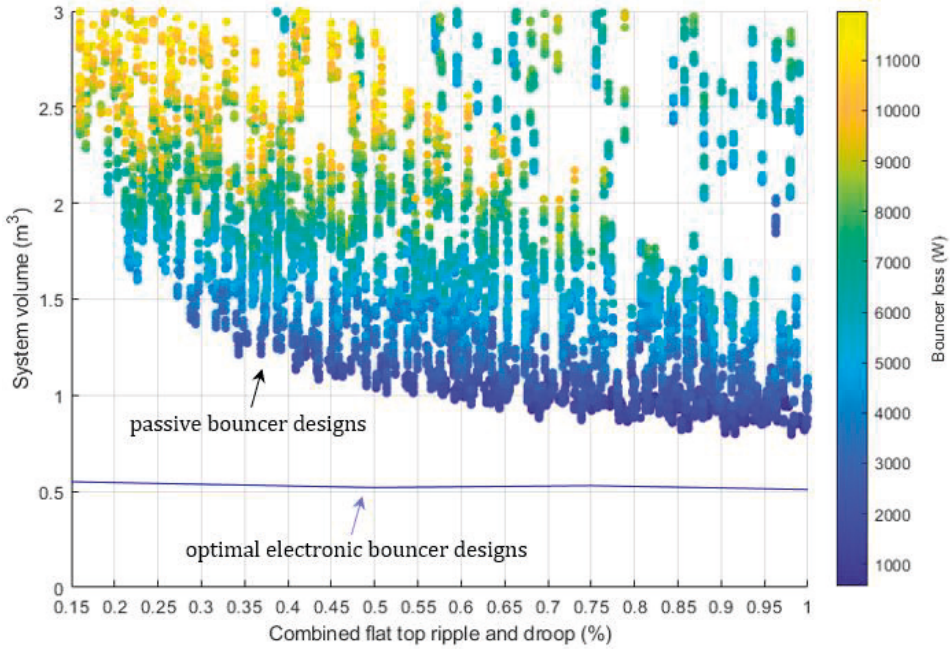



Figure 4.52: Comparison of optimization results; system volume and losses as function of combined flat top ripple and droop for passive bouncer circuit and electronic bouncer circuit.

As noted in Table 4.3, the ESS klystron modulators are required to satisfy a flat top ripple constraint of 0.15%. As shown in Figure 4.52, a bouncer based on the electronic bouncer topology may fulfil this requirement with a system volume of ~0.52 m3 and a circuit efficiency of 99.8% with losses on the order of 1.2 kW. On the other hand, satisfying this flat top ripple requirement with a passive LC bouncer circuit demands a total system volume on the order of 2.5-3.0 m3, i.e., 5-6 times larger than the proposed electronic bouncer design. In these extreme cases, the volume of the passive bouncer circuit has surpassed the volume of the capacitor bank by more than a factor of 2. Moreover, viable passive bouncer designs represent losses between 8 and 12 kW, or 1.4 to 2.1% of rated modulator output power, Table 4.3. This great disparity highlights the benefits of the electronic bouncer circuit in view of long pulse high power applications. Here, the inferior performance of the passive LC bouncer circuit is attributed to the combination of 1) the extremely long resonant period required to adequately compensate droop without exceeding the stringent flat top ripple constraint; and 2) the relatively high operating voltage and current levels.

Relaxing the flat top ripple and droop constraint allows a significantly more compact and more efficient passive bouncer system. Though the same improvements are not seen for the electronic bouncer circuit, it should be noted that even if a combined flat top ripple and droop value of up to 1% would be permissible, the proposed

electronic bouncer design (i.e., capable of delivering a flat top ripple limited to that of 0.15%) would still be smaller by a factor of ~1.7.

*Selection of bouncer design*

The preceding analysis has shown that the electronic bouncer is the much-preferred solution in considering long-pulse high-power bouncer-based modulators with strict requirements on pulse quality. In the following, detailed analysis and design of electronic bouncers will be carried out in view of the ESS application requirements.

To further study the options minimizing system volume, optimization was performed for a series of predetermined values of modulator main capacitor bank voltage droop. Here, the voltage droop was swept from 100 V to 1100 V (i.e., from around 3% to 35% of the primary voltage). A breakdown of resulting system volume as function of main capacitor bank voltage droop and with number of parallel converter phases as parameter is shown in Figure 4.53. Here, it is immediately seen that the main capacitor bank volume is inversely proportional to the pre-set main capacitor bank voltage droop. This is expected as the modulator main capacitor bank capacitance value is inversely proportional to the voltage droop, (4.161). This is of importance in design as increasing voltage droop impacts the electronic bouncer - excessive voltage droop is undesirable and bounded by the diminishing returns on main capacitor bank volume.

Figure 4.53.b depicts the resulting bouncer volume as a function of capacitor bank voltage droop. As can be seen, bouncer volume is comparatively small and increasing weakly with voltage droop. This is in part attributable to the corresponding increase in bouncer input voltage, necessitating larger passive component values to maintain flat top performance. Interestingly, for the case of $N_m = 2$, bouncer volume is seen to quickly increase after a certain threshold voltage droop. Although losses do not significantly impact modulator efficiency, thermal cycling is still present and must be managed as explained in Appendix B. As voltage droop and, consequently, bouncer input voltage increase, so does semiconductor loss, (4.141) and (4.143). At a certain point converter switching frequency must be reduced to limit losses and bouncer component values are increased to maintain flat top performance, (4.138). Note here the dependence on the number of parallel converter phases $N_m$. It is also important to point out that as the bouncer input voltage exceeds ~700 V, 1.2 kV IGBT technology is ruled out, i.e., switching frequency is further limited and semiconductor performance is reduced.

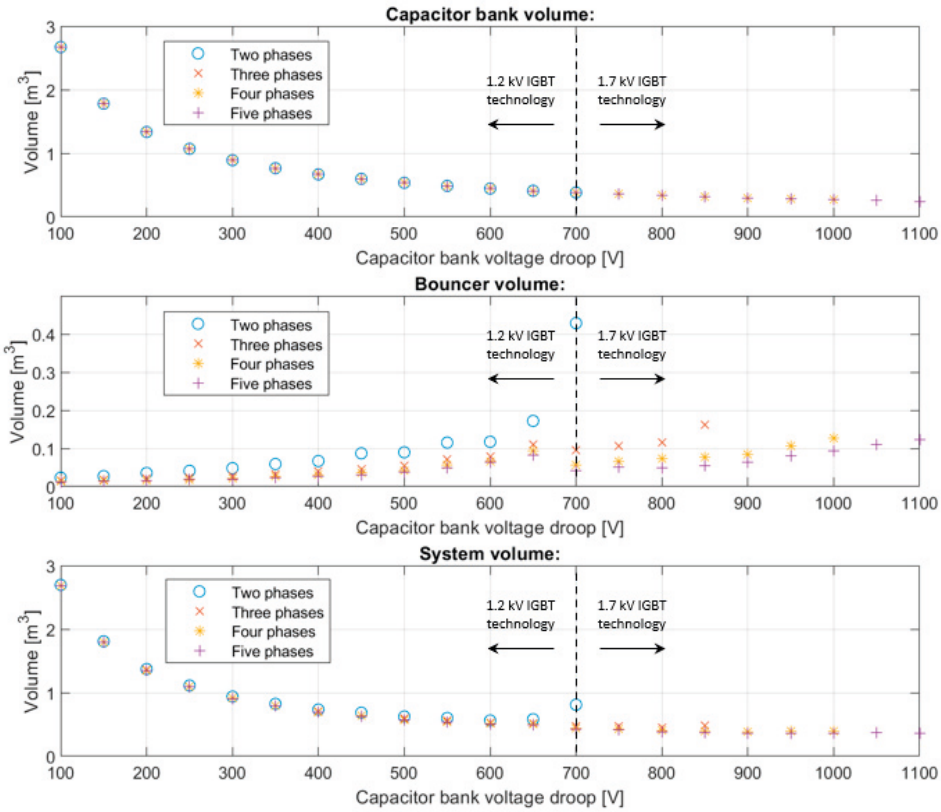



Figure 4.53: Resulting component volumes as function of imposed main capacitor bank voltage droop: a) main capacitor bank volume, b) bouncer volume, and c) the sum of the main capacitor bank and bouncer volumes.

Based on the above observations, it seems reasonable to choose a design which minimizes system volume without resorting to a larger number of parallel converter phases and without transitioning to 1.7 kV IGBT technology. Consequently, an electronic bouncer design intended for a capacitor bank voltage droop of ~650 V (compatible with 1.2 kV IGBT technology) and utilizing a three-phase interleaved buck converter was selected for further analysis. The chosen solution is summarized in Table 4.4. This design features the half bridge IGBT module CM1400DUC-24S from Mitsubishi. The losses are split almost evenly between the DC/DC converter IGBT modules and the converter phase inductors. A breakdown of system volume is shown in the pie chart of Figure 4.54. As can be seen, the main capacitor bank is by far the largest component in the system corresponding to the chosen design, representing 80% of total system volume. Still, the system volume of 0.52 m3 should be compared to the system without compensation circuit as exemplified by (4.94), i.e., by use of the electronic bouncer the required system volume may be decreased approximately by a factor 20.

Table 4.4: Overview of chosen electronic bouncer design

| Symbol | Quantity | Value |
|---|---|---|
| $V_2$ | Rated output voltage | 115 kV |
| $I_2$ | Rated output current | 100 A |
| $T_p$ | Pulse length | 3.5 ms |
| - | Maximum peak-to-peak flat top ripple | < 0.15% |
| - | Maximum flat top droop | < 0.15% |
| $C_{bk}$ | Capacitor bank | 20.6 mF |
| $V_{cbk}$ | Capacitor bank voltage | 3 kV |
| $\Delta V_{cbk}$ | Capacitor bank voltage droop | 650 V |
| $V_{cin,0}$ | Bouncer input voltage | 750 V |
| $C_{in}$ | Bouncer input capacitor | 62 mF |
| $L_b$ | Bouncer phase inductor | 6.1 µH |
| $C_b$ | Bouncer output capacitor | 630 µF |
| $N_m$ | Number of dc/dc converter phases | 3 |
| $N_s$ | Number of parallel IGBT modules per phase | 1 |
| $f_{sw}$ | Converter switching frequency | ~22 kHz |
| - | System volume | 0.52 $m^3$ |
| - | Contr. of electronic bouncer to system efficiency | >99.8% |

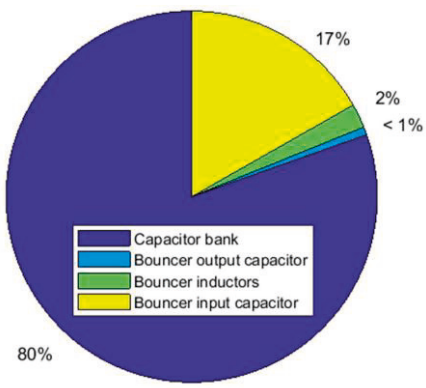



Figure 4.54: Breakdown of chosen electronic bouncer design component volumes

*Simulation results: finite element analysis*

Finite element analysis is carried out in COMSOL Multiphysics(R) as one step in validating the chosen electronic bouncer design. Here, magnetostatic analysis as well as heat transfer analysis of the bouncer inductor is performed. A detailed description of the bouncer inductor part of the electronic bouncer design of Table 4.4 is given in Table 4.5.

**Table 4.5: Overview of bouncer inductor corresponding to design in Table 4.4**

| Symbol | Quantity | Value | |
|---|---|---|---|
| | | Design 1 | Design 2 |
| $A$ | Toroidal inner radius | 5.60 cm | 5.60 cm |
| $B$ | Toroidal outer radius | 8.93 cm | 8.93 cm |
| $H$ | Toroid height | 8.40 cm | 8.40 cm |
| $W$ | Winding width | 1.27 cm | 1.27 cm |
| $N$ | Inductor number of turns | 28 | 24 |
| $\tilde{L}_b$ | Estimated inductance | 6.1 µH | - |
| $L_b$ | Simulated inductance | 8.5 µH | 6.2 µH |
| $\tilde{T}_{max}$ | Estimated hot-spot temperature | 100 °C | 100 °C |
| $T_{max}$ | Simulated hot-spot temperature | 103 °C | - |

First, the magnetostatic analysis is performed mainly to evaluate the inductance value. The simulated peak magnetic flux density of the bouncer inductor is shown in Figure 4.55. As indicated in Table 4.5, the inductance was estimated to be 6.1 µH whereas the corresponding simulated inductance value is close to 8.5 µH. This rather large difference is attributable to the fact that the simplified inductance equation, (4.146), is derived considering the flux in the inductor coil interior only. In practice, the energy stored in the surrounding field as shown in Figure 4.55 needs to be taken into account as well. It should be pointed out that this higher inductance value actually improves bouncer output voltage filtering. Still, an alternative to this design is to slightly reduce the number of turns, e.g., from 28 to 24, yielding a simulated inductance of 6.2 µH. This value is significantly closer to the initially estimated inductance value and would yield a slightly more conservative thermal design.

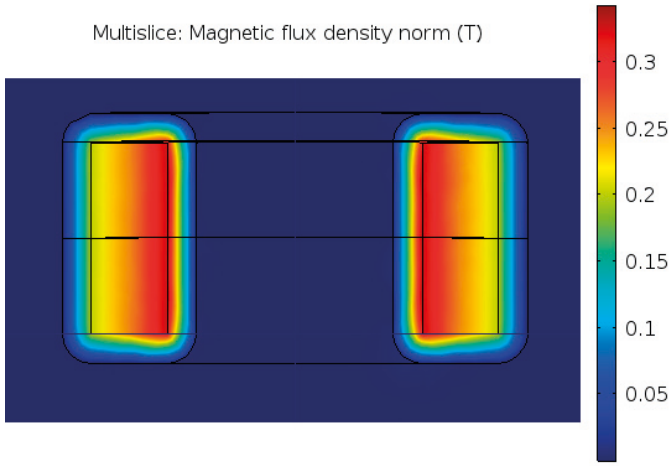



Figure 4.55: Magnetostatic analysis of bouncer inductor design

Thermal analysis of the revised inductor design is carried out to ensure that the estimated hotspot temperature of the bouncer inductor is limited to the prescribed value $T_{max}$. Again, the ambient temperature is assumed to be 40 °C. The winding surface area is assumed to be convective, with assumed heat transfer coefficient $h$. The inductor losses are assumed to be uniformly distributed throughout the inductor winding. The simulation results are shown in Figure 4.56. As can be seen, the hotspot temperature of the inductor matches the targeted $T_{max} \cong 100$ ℃.

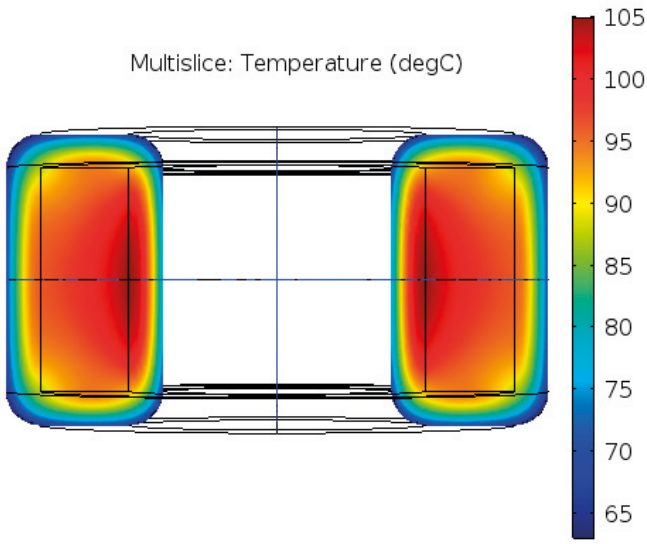



Figure 4.56: Heat transfer analysis of bouncer inductor design

*Simulation results: circuit simulation*

A complete circuit model representation was developed and implemented in MATLAB® Simulink® to validate the chosen design. Figure 4.57, Figure 4.58 and Figure 4.59 show the generated circuit simulation results. As can be seen, in addition to the compensating charging current, the bouncer circuit is pre-charged to that of the load current. The capacitor bank voltage may be seen to droop the expected 650 V throughout the duration of the pulse, Table 4.4. Bouncer output capacitor charging begins as the modulator output voltage reaches its peak, and the bouncer output capacitor voltage is seen to inversely match the capacitor bank voltage droop resulting in a smooth modulator output flat top. At the end of the pulse, the energy stored in the bouncer inductors may be seen to transition into the bouncer output capacitor. The energy is then fed back to the bouncer input capacitor via converter boost mode operation. Figure 4.58 shows a zoom of the sum of the bouncer inductor currents. As noted, this current ripple generates an associated bouncer output capacitor voltage ripple seen in the modulator output voltage. The two main sources of associated voltage ripple, (4.138)-(4.139), are clearly seen in the zoomed-in-view of the output voltage flat top, Figure 4.59. Utilizing the information in Table 4.4 for equation (4.139) yields an estimated peak-to-peak flat top ripple of 172.5 V, corresponding to that of 0.15 % of 115 kV. This estimation is clearly verified in Figure 4.59. Furthermore, Figure 4.59.a shows that electronic bouncer operation does not affect modulator output pulse rise time, here seen to be on the order of 150 μs.

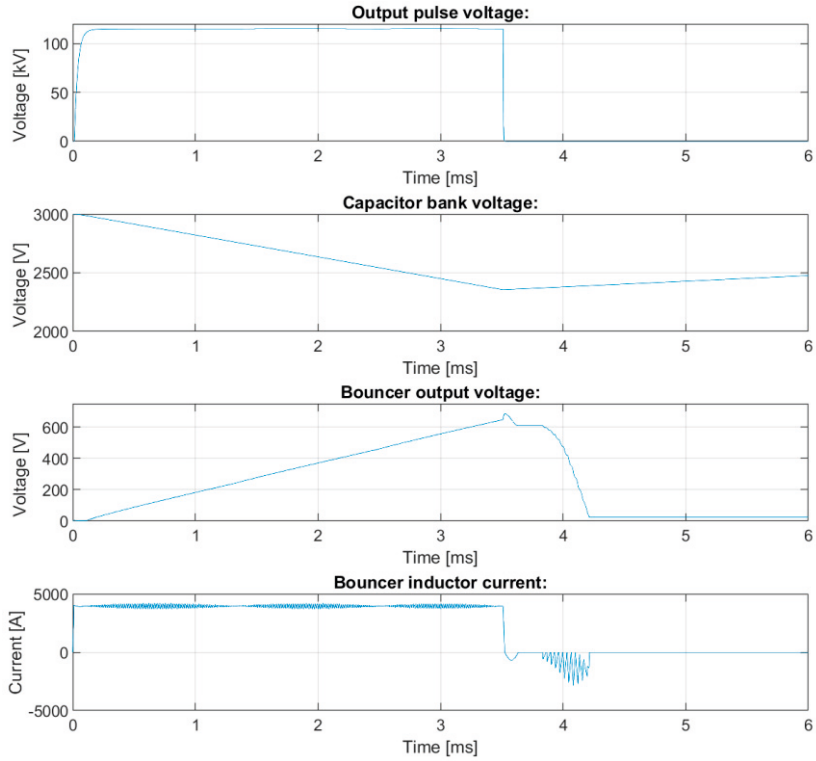



Figure 4.57: Overview of circuit simulation results for chosen bouncer inductor design

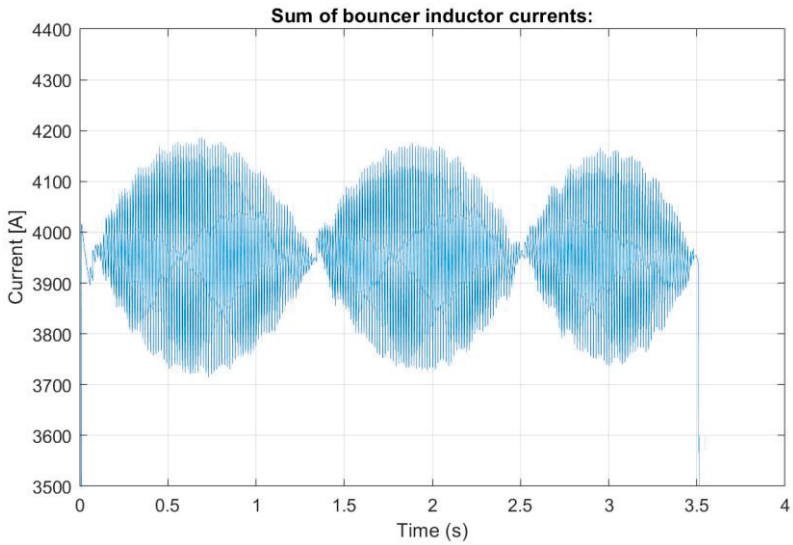



Figure 4.58: Zoom on sum of bouncer inductor currents

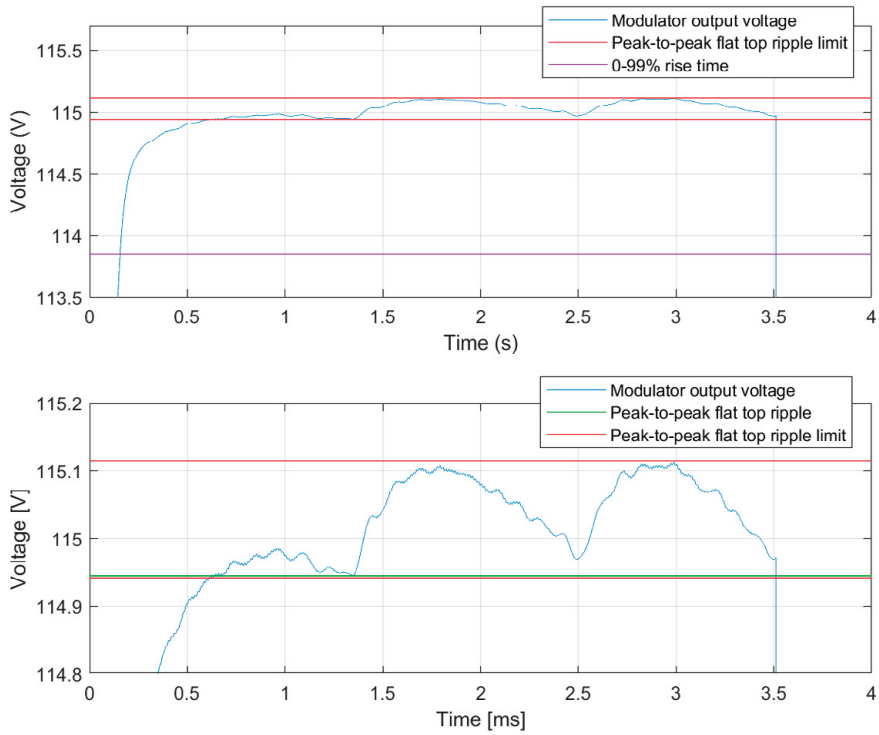



Figure 4.59: Zoom on pulse flat top, a) pulse rise time (0-99%) maintained at ~150 μs; b) combined droop and peak-to-peak flat top ripple is within prescribed limit of 0.15%.

*Discussion*

In this section, a two-quadrant interleaved multiphase dc/dc converter was utilized. The placement of the electronic bouncer circuit, Figure 4.38, is beneficial as it allows for efficient and precise droop compensation whilst converting only a fraction of the pulse power, facilitating use of commercially available semiconductor technology. Use of a two-quadrant converter allows for the retrieval of some of the energy stored in the output bouncer capacitor at the end of the pulse event. In the design proposed in the case study, the retrieved energy was comparatively small in relation to the bouncer input capacitor energy. It may then be argued that a one quadrant converter could be used instead, discharging the bouncer output capacitor via a parallel resistor. This approach was adopted in [4.35]. Another possibility would be to use an H-bridge four quadrant converter. Here, circuit operation is similar but would allow negative pre-charging of the output bouncer capacitor, permitting use of a smaller output bouncer capacitor and, potentially, use of low voltage switches at higher switching frequency. On the other hand, the output bouncer capacitor is in any case rather small in comparison to the bouncer energy storage and the main capacitor bank. Furthermore, it is likely that 1) the use of low voltage switches is impractical given the high pulse current

amplitudes; and that 2) their advantages are offset by added component count and circuit complexity. It should also be noted that the modulator capacitor bank must be overcharged in order to compensate for the negative bouncer voltage; if the droop is large, it must be ensured that the capacitor can withstand the added voltage. Using this technique to further reduce the main capacitor bank seems ineffective given the present diminishing returns on capacitor bank volume.

## 4.4 Design of solid-state switch assembly

The solid-state switch assembly is switched on to connect the capacitor bank to the transformer unit in generating a pulse. The pulse event is then terminated at some appropriate time by opening the switch assembly. Consequently, the assembly must 1) be composed of fully controllable switches capable of breaking the full load current referred to the primary side, 2) be able to withstand the full capacitor bank voltage in off-state, and 3) reliably be able to withstand the power cycling associated with high power pulsed operation. Considering on/off operation at tens of Hz with voltage levels on the order of several kV and associated primary side currents on the order of several kA, use of high-power press-pack IGCT devices is appropriate [4.36]. An overview of a typical IGCT power unit is shown in Figure 4.60. To ensure reliable operation, several IGCT units must be connected in series. Typical integration of such IGCT power units in forming a HV switch assembly is shown in Figure 4.61. Additionally, compensators for static and dynamic asymmetry must be designed and implemented.

In this section, a complete design procedure for such solid-state switch assemblies is developed. Then, a case study considering the design of a solid-state switch assembly for ESS application requirements is presented.

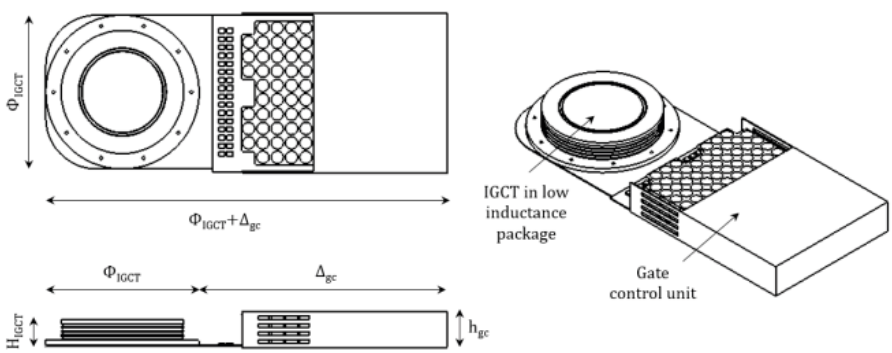



Figure 4.60: Overview of typical IGCT power unit.

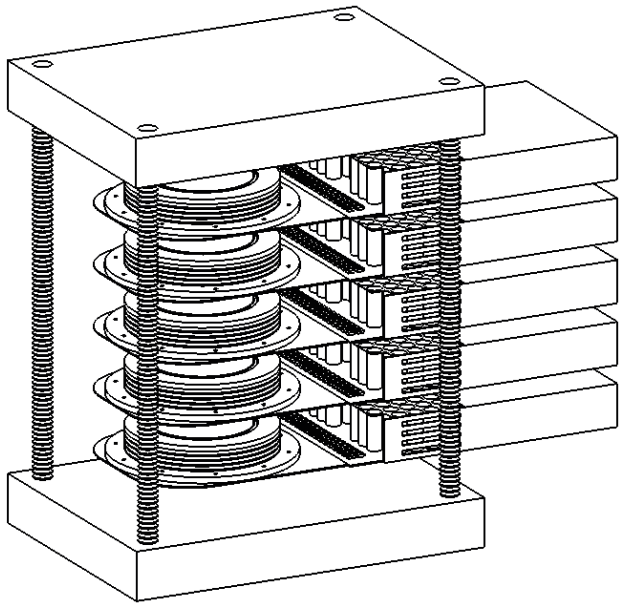


Figure 4.61: Typical integration of IGCT power units into HV switch assembly.

### 4.4.1 Series connection of switches

Pulse transformer-based modulators intended for long pulse high power applications typically operate on a capacitor bank voltage of between 3 to 10 kV. To ensure reliable repetitive switch operation it is often necessary to connect multiple IGCT units in series. Unfortunately, direct series connection of power semiconductors is not feasible due to both internal and external differences between the power components resulting in voltage asymmetry among the series connected units.

*Compensator for static asymmetry*

IGCT units are often described in datasheets in terms of their repetitive peak off-stage voltage $V_{drm}$ and their corresponding off-state current $I_{drm}$. Thus, a simplified model of a solid-state switch assembly with $N_s$ series connected switches may be drawn as shown in Figure 4.62. Here, the IGCT leakage resistance is given by (4.163). Importantly, according to, e.g., [4.30], the practical off-state leakage current can vary between units by up to 85% of the specified datasheet value. Hence, in off-state, one or several IGCTs may experience a disproportionally high share of the voltage, i.e., to ensure reliable switch operation one must either use significantly oversized IGCTs or include a static compensator for voltage symmetrisation.

$$R_l \cong \frac{V_{drm}}{I_{drm}} \tag{4.163}$$

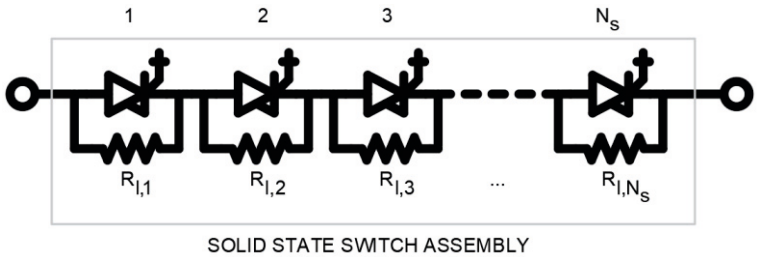



Figure 4.62: Simplified model of series connected IGCT units forming a solid-state switch assembly. Variations in the IGCT leakage resistances result in static off-state voltage asymmetry.

For series connection of components intended for 1.2 kV operation or above, it is common practice to include a parallel resistor $R_c$ for voltage symmetrisation [4.30], Figure 4.63. Here, the worst-case scenario is seen when $N_s - 1$ switches experience the normal off-state current $I_{drm}$, corresponding to resistance $R_l$, whereas the remaining switch experiences an off-state current deviating by the referenced 85%, corresponding to resistance $R_w$, (4.164). In this case, the worst case IGCT voltage is given by (4.165), and it must be ensured that this voltage does not exceed the specified maximum repetitive off-state voltage $V_{drm}$ with some safety margin.

$$R_w = R_l/(1 - \Delta I_{drm}) \tag{4.164}$$

$$V_w = V_p \frac{\frac{R_w R_c}{R_w + R_c}}{\frac{R_w R_c}{R_w + R_c} + (N_s - 1)\frac{R_l R_c}{R_l + R_c}} \leq k_v V_{drm} \tag{4.165}$$

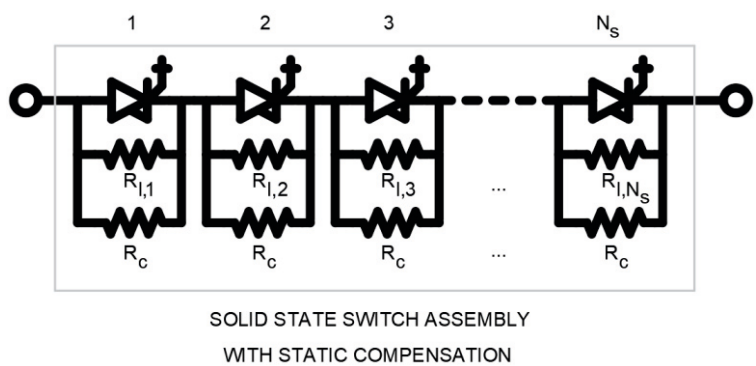



Figure 4.63: Model of series connected IGCT units forming a solid-state switch assembly. Compensation resistors $R_c$ are placed in parallel with each IGCT unit to ensure static voltage symmetry among the semiconductor switches.

*Compensator for dynamic asymmetry*

In addition to static voltage asymmetry discussed above, voltage asymmetry during switching events may be seen due to differences in, e.g., the internal module inductances, the external circuit inductances, or the gate drive circuits [4.30]. Such differences influence device switching times and thereby the voltage distribution during the switch event. In this application, switch turn-on may be considered soft given the transformer leakage inductance. Issues related to switch assembly turn-off can be mitigated by inclusion of the compensation circuit shown in Figure 4.64. Though active solutions exist [4.30], these are typically not adopted in high power IGCT applications and will not be considered here.

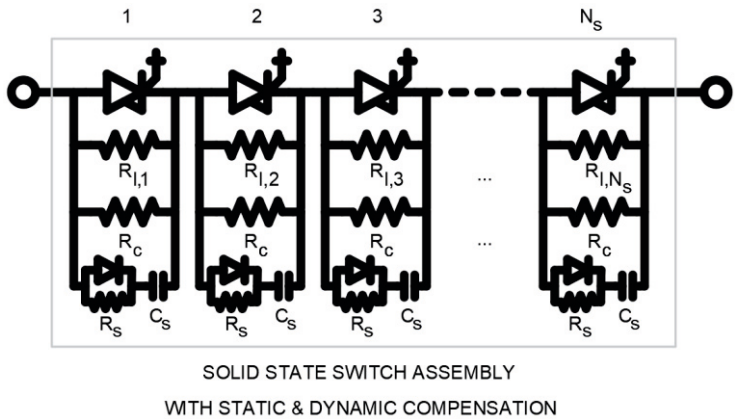



Figure 4.64: Model of series connected IGCT units forming a solid-state switch assembly. Compensation resistors $R_c$ are placed in parallel with each IGCT unit to ensure static voltage symmetry among the semiconductor switches. RCD circuits are used to ensure dynamic voltage symmetry among the semiconductor switches during assembly turn-off.

To dimension the dynamic compensation circuit, the switch assembly may be considered to be in series with an ideal voltage source, the leakage inductance of the pulse transformer and the klystron load resistance. This corresponds to an ideal RLC circuit, and the total equivalent capacitance may be chosen according to (4.166). With $N_s$ switches in series, the per-unit capacitance is given by (4.167). Finally, the compensation resistance is set according to (4.168), [4.37], such that the compensation capacitor is fully discharged during the pulse event and may be used during the next turn-off event.

$$C_{eq} \sim \frac{L_s}{R_k'^{\,2}} \tag{4.166}$$

$$C_s = C_{eq}/N_s \tag{4.167}$$

$$R_s = \frac{T_p}{2.3 C_s} \tag{4.168}$$

### 4.4.2 Switch design procedure

In the following, a complete solid state switch assembly design procedure is developed. The procedure is summarized in Figure 4.65. The procedure is based on a catalogue of commercially available IGCT units from ABB formed by, for each component reference, the repetitive peak off-state voltage, the repetitive peak off-state current, the threshold voltage, the slope resistance, the controllable turn-off current, the turn-off time, the turn-off pulse energy, the static thermal resistance from junction to heatsink, and the transient thermal impedance parameters. For each catalogue reference, the following calculations are carried out. First, for $N_s$ switches, the compensation resistance is swept to find a value which 1) yields appropriate voltage symmetry such that the $N_s$ switches can withstand the voltage in the worst-case scenario presented in equation (4.165), and 2) minimizes the compensation resistance loss, (4.169). While, according to [4.30], the off-state current and thereby the equivalent off-state resistance can vary with respect to the datasheet value by as much as 85%, the statistical distribution is not well known. Thereby, (4.169) appropriately calculates the power dissipation in terms of selecting a suitable resistor, though somewhat pessimistically in terms of estimating system efficiency.

Once the static compensators have been dimensioned, the dynamic compensators are dimensioned according to (4.166)-(4.168).

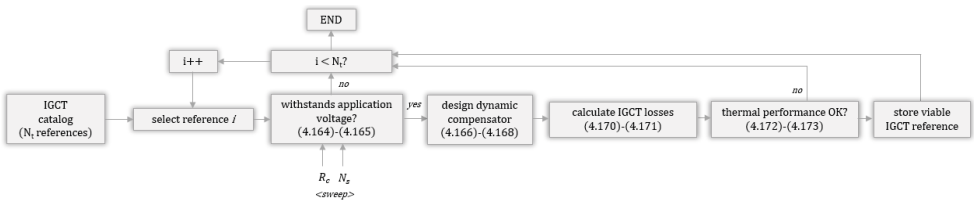



Figure 4.65: Solid state switch assembly design procedure

$$P_w = \frac{V_w^2}{R_c} \tag{4.169}$$

Finally, the IGCT losses are estimated. Here, the conduction losses generated during the pulse is given by (4.170) whereas the switch turn-off losses are given by (4.171). Then, the average IGCT junction temperature is estimated by (4.172) and the IGCT junction temperature swing is given by (4.173). As usual, it is important to ensure that the obtained thermal performance does not deteriorate switch lifetime in accordance with the principles presented in Appendix B.

$$\hat{P}_{cond} = \left(V_{t,0} + r_t I_2'\right) I_2' \tag{4.170}$$

$$\hat{P}_{sw} = \frac{E_{off}}{t_d} \tag{4.171}$$

$$T_j = T_a + R_{th}\left(\hat{P}_{cond} T_p f_r + \hat{P}_{sw} f_r\right) \tag{4.172}$$

$$\Delta T_j = Z_{th}(T_p)\hat{P}_{cond} + Z_{th}(t_d)\hat{P}_{sw} \tag{4.173}$$

Finally, total switch assembly losses are calculated according to (4.174) and total switch assembly volume is calculated according to (4.175). Evaluating the complete catalogue of IGCTs allows a choice of viable switch assemblies in terms of system efficiency and system volume.

$$\bar{P}_{ssa} = N_s\left(\hat{P}_{cond} T_p f_r + \hat{P}_{sw} f_r + P_w\right) \tag{4.174}$$

$$V_{ssa} = N_s \emptyset_{IGCT}^2 (h_{IGCT} + \Delta h) \tag{4.175}$$

### 4.4.3 Case: switch assembly for ESS modulator requirements

In this section, the developed design procedure for the solid-state switch assembly component is applied to ESS modulator requirements. The relevant design requirements are specified in Table 4.6. The modulator primary side voltage will be swept from 3000 V to 6000 V. Though the primary voltage also has an effect on the other parts of the modulator, these effects are not considered in the following analysis. In the following, a catalogue of IGCT switches from ABB is considered [4.36].

**Table 4.6: Summary of ESS modulator requirements for switch design**

| Symbol | Quantity | Value |
|---|---|---|
| $V_2$ | Rated output voltage | 115 kV |
| $I_2$ | Rated output current | 100 A |
| $T_p$ | Pulse length | 3.5 ms |
| $f_r$ | Pulse repetition rate | 14 Hz |
| $t_r$ | Maximum 0-99% pulse rise time | 120 µs |

In keeping with the analysis presented in earlier sections, the modulator output circuit is assumed to be overdamped. Thus, the transformer leakage inductance may be estimated directly from (4.176).

$$L_s \approx \frac{t_r V_2}{4.6 I_2} \tag{4.176}$$

Evaluating the design procedure for the above conditions yields the selection of switch assemblies presented in Figure 4.66, plotting switch assembly losses versus switch assembly volume. Several choices are available for each voltage level. Expectedly, however, both losses and volume appear to generally increase with voltage. This is further illustrated in Figure 4.67, plotting a curve fit (R-square value of fits above 95%) of switch assembly power losses as well as switch assembly volume versus primary voltage. Here, the switch assembly with lowest losses has been chosen to represent each primary voltage level. Increasing the primary side voltage reduces the primary side current. On the other hand, a larger number of switches must be used to support the voltage in keeping with (4.165), with the net effect being increasing power loss and volume, (4.174)-(4.175). Still, it is again emphasized that reducing the primary side voltage influences both the design and the performance of all other modulator components, i.e., an integrated design procedure is necessary to ensure optimal system performance.

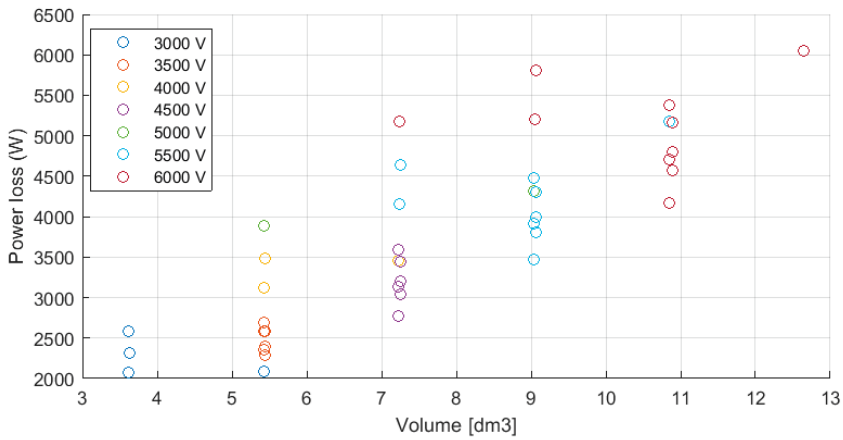



Figure 4.66: Switch assembly power losses versus switch assembly volume for ESS application requirements.

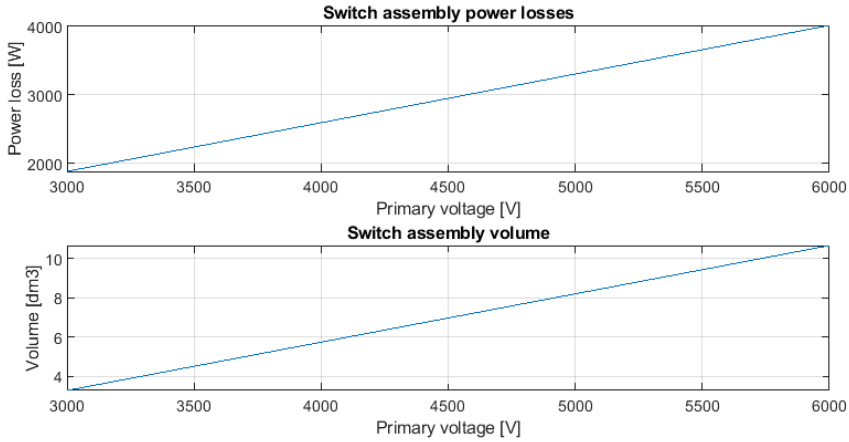



Figure 4.67: Optimized switch assembly power loss and switch assembly volume versus primary side voltage.

For the purposes of this case study, a primary side voltage of 5 kV is selected. The chosen switch assembly is based on 5 series connected IGCT units and has a power loss of around 3300 W, representing ~0.5% of the rated modulator power, Figure 4.67.

## 4.5 Design of transformer bias and demagnetization auxiliary circuits

As pointed out in relation to (4.1), the transformer must be sized for a flux swing $\Delta B$ associated with pulsed excitation of the core. Here, use of a core biasing circuit allows a greater flux swing and consequently a smaller transformer turns-area product. This is illustrated in Figure 4.68, showing the full B-H characteristics of some typical transformer material. As can be seen, in steady state operation without a biasing circuit the transformer core flux density at the beginning of each pulse event is $B_{rem}$. With the core flux density being limited to $B_{max}$, the maximum flux swing is $\Delta B = B_{max} - B_{rem}$. However, for transformer core materials used in pulse transformers (particularly considering long pulse high power applications), $B_{rem}$ is typically quite low and may often be assumed to be zero, i.e., $\Delta B \cong B_{max}$. On the other hand, using a biasing circuit the transformer core flux density may be brought to $-B_{max}$ prior to each pulse event, i.e., the core flux swing may be as high as $\Delta B = 2B_{max}$, representing a reduction of the required turns-area product by 2.

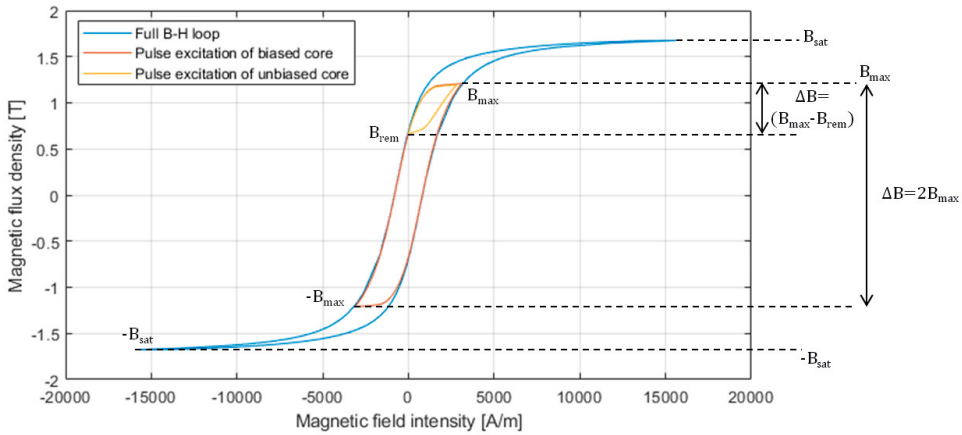



Figure 4.68: Magnetization curve for magnetic material. Features are exaggerated for clarity.

Following each pulse event, regardless if a biasing circuit is used or not, the transformer core flux must be reset to its initial value prior to the following pulse event or the transformer will saturate over the course of a few pulses. This is done with a demagnetization circuit. The functions of these circuits (bias and demagnetization) are closely interrelated and, as will be shown in the following sections, their designs are often highly interdependent.

Finally, it is noted that in addition to the stored magnetic energy resulting from pulsed excitation, the transformer assembly also stores electric energy by way of the stray capacitive elements discussed as part of section 4.2.3. However, the stored electric energy is many orders of magnitude smaller than that of the stored magnetic energy in the transformer core. For this reason, the stored electrical energy has been disregarded in the following section.

### 4.5.1 Overview of techniques

In this section, an overview of common techniques for transformer core bias and demagnetization is presented.

*Passive demagnetization circuit: freewheeling diode*

The magnetic energy stored in the transformer is directly related to the corresponding circuit currents. Thereby, following the pulse event, a freewheeling circuit of some sort is required to allow the currents to continue flowing. The simplest type of freewheeling circuit is shown in Figure 4.69 and is described in, e.g., [4.38]-[4.39]. Here, the forward voltage drop of the freewheeling diode will dissipate the stored transformer over time, demagnetizing the transformer. Reducing the current from $\hat{I}_m$ to 0 over the off-period, the required average voltage for a given

transformer can be calculated according to (4.177). Implementing this circuit, the necessary voltage is often obtained by either 1) series connecting multiple freewheeling diodes, or 2) installing a resistor in series with the freewheeling diode. Using the above-described pulse transformer as an example, (4.177) shows that several hundred volts would be required over the demagnetization period. Clearly, using series connected diodes to provide the required voltage is inappropriate for such long pulse applications. Instead, the possibility to use a resistor in series with the freewheeling diode is investigated in the following.

$$\bar{v}_r = L'_m \frac{\Delta i}{\frac{1}{f_r} - T_p} \tag{4.177}$$

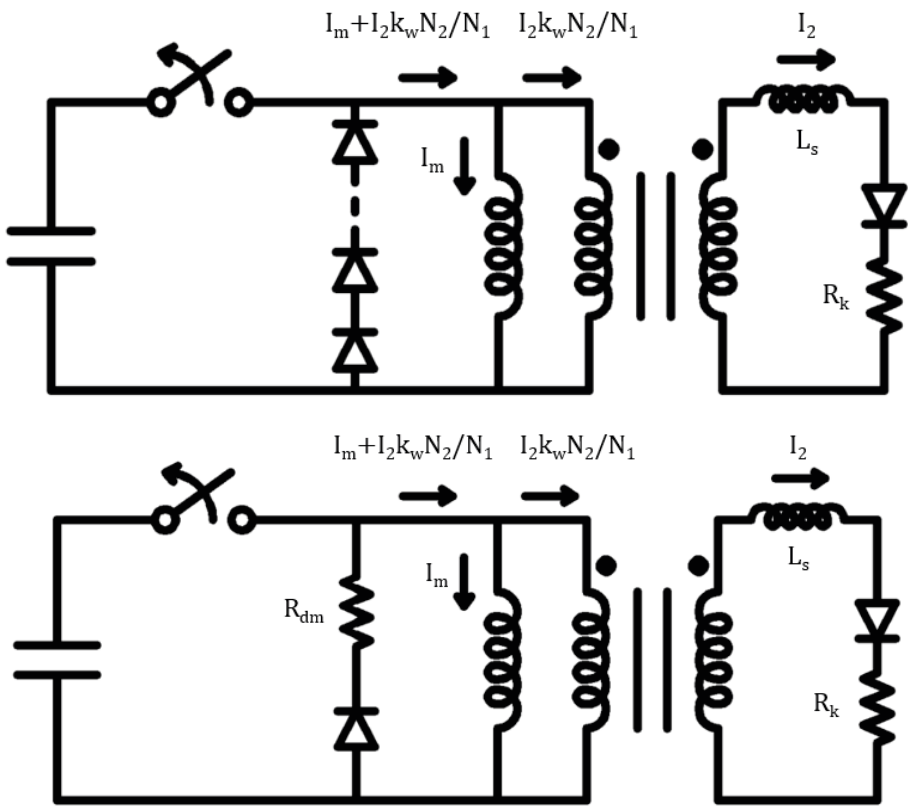



Figure 4.69: Simple passive circuit used for transformer demagnetization. As the switch is opened, the inductive currents freewheel and the stored energy is dissipated over time. The required voltage for demagnetization is obtained by either a) series connecting multiple diodes [4.38]-[4.39], or b) installing a resistor in series with the freewheeling diode.

The demagnetization period is shown in Figure 4.70. Two distinct phases may be seen. The first phase is derived from the fact that the secondary current referred to the primary is significantly greater than the magnetization current of the transformer. This phase is well described by the circuit shown in Figure 4.71.a. Here, the energy stored in the output circuit, i.e., the leakage inductance, is discharged by the demagnetization resistance $R_r$ as well as the freewheeling diode and the equivalent klystron resistance $R_k$, (4.178). To provide the necessary voltage, $R_r$ typically needs to be significantly greater than both $r_F$ and $R'_k$, (4.178). On the other hand, the energy stored in the leakage inductance is often much smaller than that stored in the magnetization inductance corresponding to a relatively fast discharge, (4.179) and Figure 4.70. Most importantly, as the full load current referred to the primary flows through the demagnetization resistor, a significant voltage spike may be generated and reflected to the secondary. Here, it is important to note that excessive reverse voltages are prohibitive in using klystron loads. Typically, a maximum reverse voltage corresponding to up to, e.g., 20% of the nominal load voltage is permitted. However, in design, a maximum reverse voltage of only 10% of the nominal load voltage is usually permitted, setting a strict upper bound for the value of $R_r$, (4.180). The first phase ends as the secondary current approaches zero.

$$L_s \frac{di_{L,s}}{dt} = V_{f,0} + \left(r_f + R_r + R'_k\right) i_{L,s} \cong R_r i_{L,s} \tag{4.178}$$

$$t_1 \cong 4.6 \frac{L_s}{R_r} \ll 1/f_r - T_p \tag{4.179}$$

$$R_r \leq \frac{V'_{k,max}}{I'_2} \cong 0.1 \frac{V_2 \left(\frac{V_1}{V_2}\right)}{I'_2} \tag{4.180}$$

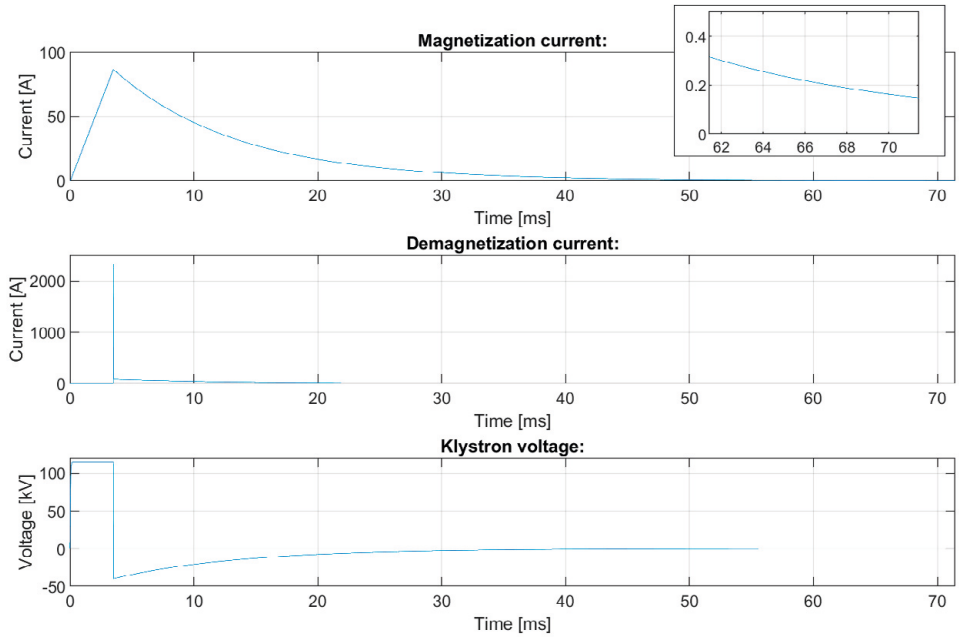



Figure 4.70: Demagnetization interval

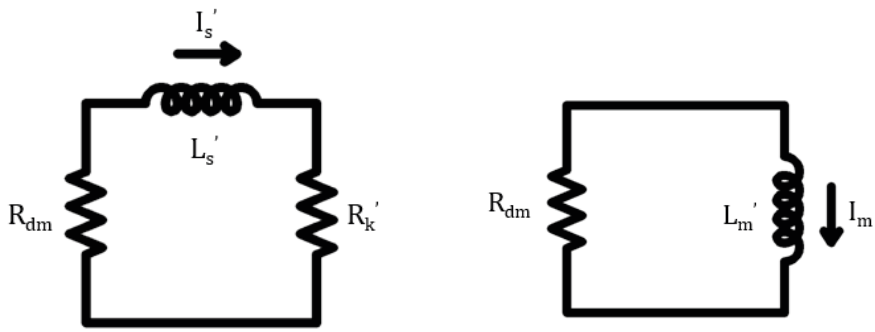



Figure 4.71: Equivalent circuits used in analyzing demagnetization with freewheeling circuit with series resistor, a) Phase 1- stored energy in transformer leakage inductance is dissipated in klystron and demagnetization resistor; b) Phase 2- stored energy in transformer magnetization inductance (transformer core) is dissipated in demagnetization resistor.

In the second phase, the transformer magnetization inductance is demagnetized by the demagnetization resistor, Figure 4.71. Importantly, the magnetization inductance must be discharged prior to the following pulse event as described by (4.181), providing a lower bound for the demagnetization resistance, (4.182).

$$t_2 - t_1 = 1/f_r - T_p - t_1 \cong 1/f_r \rightarrow 4.6\frac{L'_m}{R_r} \leq 1/f_r \tag{4.181}$$

$$R_r \geq 4.6 f_r L'_m \tag{4.182}$$

Equations (4.180) and (4.182) thereby describe the design space for selecting the demagnetization resistance $R_r$. Importantly, using the sample pulse transformer described in section 4.2 as illustration, it becomes apparent that no feasible solution exists. For this reason, this demagnetization technique cannot be reliably used in this type of application. Based on the above analysis, the simple freewheeling circuit using series connected diodes and/or series resistor will not be treated further in this thesis.

*Passive demagnetization: freewheeling diode with parallel RC circuit*

The simple freewheeling circuit described in the above can be improved by adding a capacitor in parallel with the resistor, Figure 4.72. This way, the stored magnetic energy can be smoothly transferred to the capacitor and then discharged over time in the resistive element. This demagnetization circuit was studied analytically in [4.15]. However, the presented analysis is somewhat limited in the sense that it assumes that the capacitor is always fully discharged by the end of the demagnetization interval. This is not necessarily true and, as shall be seen, is actually quite common in considering long pulse high power applications. Furthermore, no design procedure was suggested. This section presents a brief review of the analysis given in [4.15]. A complete design procedure incorporating features of the pulse transformer as well as an optional bias circuit, to be discussed in the following, is presented in section 4.5.2.

The demagnetization process for the freewheeling circuit using a parallel RC circuit is shown in Figure 4.73. Here, three distinct phases described by the equivalent circuits of Figure 4.74 can be seen.

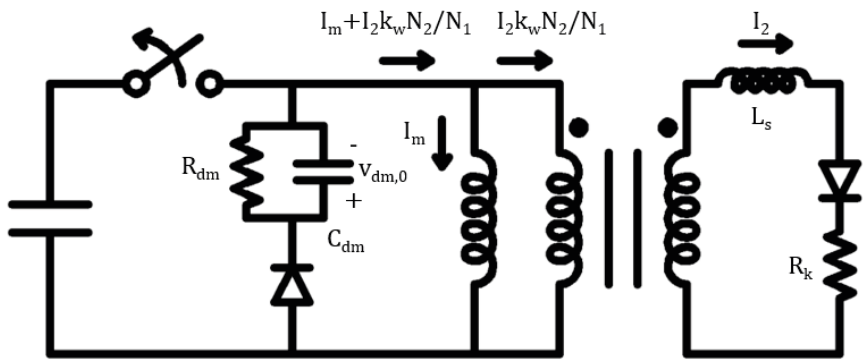



Figure 4.72: Improved passive circuit for transformer demagnetization.

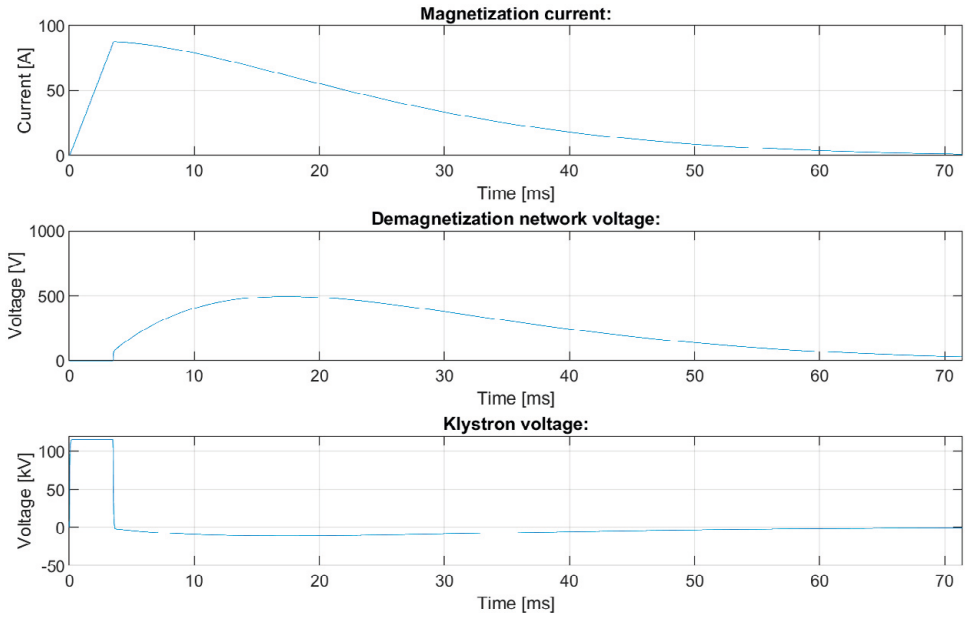



Figure 4.73: Demagnetization interval using freewheeling circuit with parallel RC circuit.

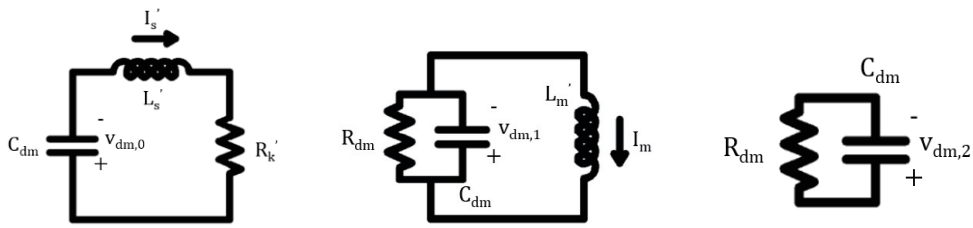



Figure 4.74: Equivalent circuits used in analyzing demagnetization with freewheeling circuit with parallel RC circuit, a) Phase 1- stored energy in transformer leakage inductance is transferred to capacitive element, some of it being dissipated in the klystron; b) Phase 2- the magnetization current freewheels charging the capacitor, and as the capacitor voltage increases the stored energy is discharged into the demagnetization resistor; c) Phase 3- once the transformer core has been demagnetized, the energy transferred to the capacitor is dissipated in the demagnetization resistor. The capacitor does not need to be fully discharged prior to the next pulse event.

The first phase is very similar to that described for the basic freewheeling circuit, above. The secondary current referred to the primary is significantly greater than that of the magnetization current and therefore dominates the first demagnetization period. During this period, the energy stored in the transformer leakage inductance is transferred to the capacitor, some of it being dissipated in the klystron. Since the stored energy is relatively small and the associated time period is extremely short, the effects of the magnetization inductance as well as the demagnetization resistor may be neglected, justifying the simplified circuit of Figure 4.74.a. Once the energy stored in the transformer leakage inductance has been transferred to the capacitor, the second phase begins. During this period, the magnetization current freewheels

charging the capacitor. As the capacitor voltage increases, the stored energy is discharged in the demagnetization resistor. Importantly, as the voltage across the load circuit is negative, the load is open circuited, justifying the simplified circuit of Figure 4.74.b. Finally, once the transformer core has been demagnetized, the remaining energy in the capacitor is dissipated in the demagnetization resistor as shown in Figure 4.74.c. Note that the capacitor does not need to be fully discharged prior to the next pulse event as long as a stable condition may be reached in which 1) the peak capacitor voltage referred to the secondary does not exceed the limitations of the klystron, and 2) the transformer core is fully demagnetized each period.

As noted, and here emphasized, the passive demagnetization methods dissipate the stored transformer core energy each pulse period often amounting to significant losses, (4.183). Again, using the sample transformer presented in section 4.2, minimum demagnetization losses are on the order of ~6 kW, or around 1% of the rated power of the ESS modulators. Later, an active demagnetization circuit with energy recovery is treated.

$$\bar{P}_r \geq E_m f_r = \frac{L'_m \Delta i^2}{2} f_r \tag{4.183}$$

*Passive bias: direct current supplied through tertiary winding*

The most common way of biasing the transformer core is by supplying a direct current $I_3$, to a tertiary transformer winding typically referred to as the bias winding, Figure 4.75. The current is often supplied with a constant low voltage power supply. During the pulse event, the capacitor bank voltage $V_p$ is applied to the transformer primary and seen on the secondary, $V_s$, and tertiary windings, $V_3$, according to their respective turns ratio with respect to the primary. Typically, the pulse voltage experienced by the tertiary winding is often on the order of several kV. Consequently, an inductor $L_3$ is installed in series with the tertiary winding to protect the low voltage power supply and to limit the tertiary current increase. This passive biasing technique is well known and has been studied in, e.g., [4.40]-[4.41]. Still, no complete design procedure for these components and auxiliary circuits has been presented.

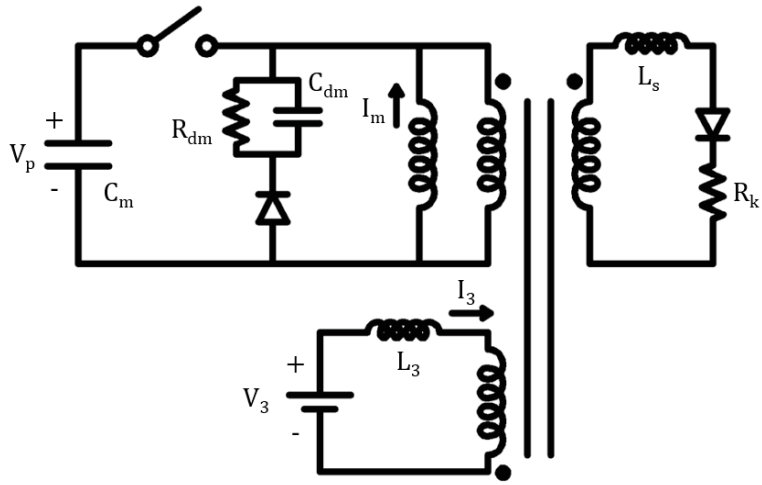



Figure 4.75: Passive bias circuit applied to pulse transformer. A constant low voltage power supply provides a current through a tertiary transformer winding to bias the transformer core. An inductor is placed in series with the tertiary winding to protect the low voltage power supply during the pulse event (pulse voltage is reflected to the tertiary winding) and to limit the tertiary current increase.

*Active circuit: bias with recovery of magnetization energy*

In the passive demagnetization schemes discussed in the preceding sections the stored magnetic energy in the pulse transformer and passive bias inductor is dissipated in a resistive element. Using active switches, the stored energy may be transferred to a capacitor which may then immediately be re-applied to the transformer in reverse in biasing the transformer core. A practical circuit implementing this idea was proposed in [4.42] and is shown in Figure 4.76. This circuit is treated in detail in section 4.5.3 and is compared to passive options in the case study presented in section 4.5.4.

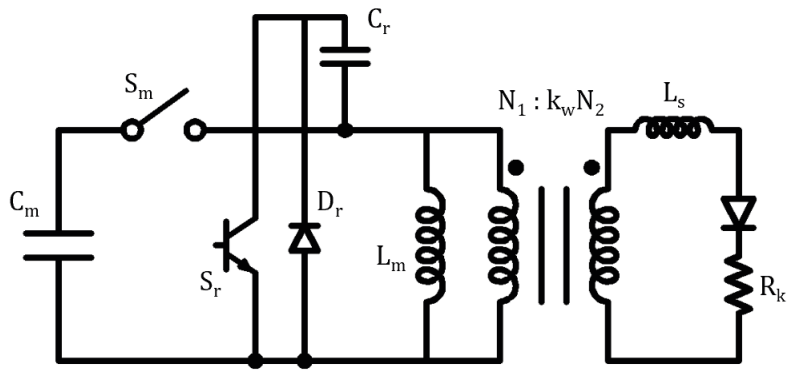



Figure 4.76: Active auxiliary circuit implementing pulse transformer biasing and demagnetization

### 4.5.2 Modeling and design of passive auxiliary circuits

In pulsing, the primary side voltage $V_p$ is applied to the transformer primary winding(s) and the core is magnetized corresponding to a magnetization current according to (4.184). Hence, to maximize the utilization of the transformer core, the core should be pre-magnetized to $-B_{max}$ by pre-magnetization current $I_3 = \left(\frac{N_1}{N_3}\right)\Delta i/2$, i.e., corresponding to symmetrical bipolar magnetization $\Delta B = 2B_{max}$.

$$V_p = L'_m \frac{di}{dt} \rightarrow \Delta i = \frac{V_p T_p}{L'_m} \tag{4.184}$$

As noted, the primary voltage is also reflected to the tertiary winding during the pulse event, (4.185). To protect the low voltage power supply, an inductor is placed in series with the tertiary winding. Here, the series inductor must be sized to withstand the voltage-time integral of the pulse while sufficiently limiting the tertiary winding current increase. For a fractional tertiary winding current increase $p$, the series inductance may be calculated according to (4.186).

$$V_3 = V_p \frac{N_3}{N_p} \tag{4.185}$$

$$L_3 = \frac{V_t T_p}{p I_3} \tag{4.186}$$

In the following, models intended for use in design of the passive bias circuit are developed. As noted, in case the passive bias circuit is used, the series bias inductor must also be demagnetized every pulse period. Consequently, modeling and design of the bias circuit will be treated before details on the demagnetization circuit are given.

*Modeling of tertiary winding*

The tertiary winding has $N_3$ turns and may be wound around the low voltage end of the secondary winding bobbin (in case the secondary windings are series connected, the lower voltage winding is preferred for practical reasons), around the primary winding bobbin, or in some cases even on top of the transformer core. Most often, given the relatively low voltage and low power, a foil-type winding is used. Here, a copper strip glued in-between two strips of insulating material are wound several layers around the frame of choice in forming a winding. For a maximum current

density $J_{w,3}$ and a copper strip height $w_h$, the required copper strip thickness is given by (4.187).

$$w_t = \frac{I_3}{J_{w,3} w_h} \tag{4.187}$$

Using insulating material with thickness $t_i$, the thickness of the complete winding is given by (4.188). From this, the mean path length of the tertiary winding is given by (4.189). Finally, the tertiary winding resistance and the corresponding voltage drop and power dissipation are given by (4.190)-(4.192), respectively.

$$t_{w,3} = w_t N_3 + 2t_{i,3}(N_3 - 1) \tag{4.188}$$

$$[MPL]_{w,3} = 2\left[x_c + y_c + \frac{8}{2} d_3 + \frac{8}{2}\left(N_3 w_t + 2t_{i,3}(N_3 - 1)\right)\right] \tag{4.189}$$

$$R_{w,3} = \rho_{cu} \frac{N_3 [MPL]_{w,3}}{w_t w_h} \tag{4.190}$$

$$V_{w,3} = R_{w,3} i_3 \tag{4.191}$$

$$\bar{P}_{w,3} = V_{w,3} I_3 \tag{4.192}$$

*Modeling of series bias inductor*

The inductance value of the series bias inductor was given in (4.186), above. Using the volume-optimized transformer for ESS modulator requirements presented in section 4.2, the magnetization inductance referred to the primary side, (4.49), is on the order of 0.25 H. Hence, assuming a tertiary winding voltage of 5 kV and a 50% increase in the tertiary winding current, the required bias inductance according to (4.184)-(4.186) is on the order of 1 H. To obtain a relatively compact solution, a tapewound double C core with multiple layer windings should be used. Given the relatively large current increase required to keep the necessary series inductance to a minimum, a distributed air gap is used. Here, $N_g$ air gaps of length $g$ are used per core leg. The basic geometry is shown in Figure 4.77.

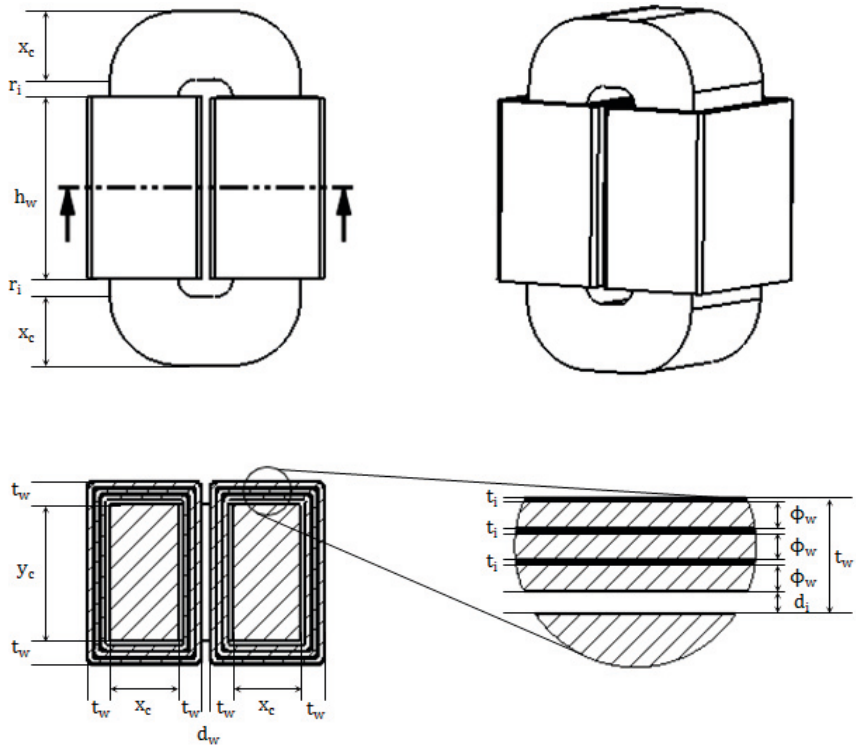



Figure 4.77: Overview of series bias inductor geometry

The inductance of this geometry is estimated by (4.193). Using $x_c$, $N_2$ and $g$ as main design parameters ($l$ and $N_g$ can be varied as integers within a limited range according to what is considered practical given the application at hand), the required magnetic core depth is calculated from (4.194). At this point, it should be ensured that the resulting peak magnetic flux density (i.e., at the end of each pulse event) does not exceed that allowed by the material, (4.195). If the constraint is not satisfied, the design procedure starts over with new design parameter value selection.

$$L_3 = \frac{V_t T_p}{p i_3} = \mu_0 \frac{x_c y_c (2N_2)^2}{2 k_g g} \tag{4.193}$$

$$y_c = \frac{k_g g L_3}{2\mu_0 x_c N_2^2} \tag{4.194}$$

$$\hat{B} = \frac{\mu_0 N_2 I_3 (1+p)}{k_g g} \leq B_{max} \tag{4.195}$$

Given the relatively low current, round enamelled copper wire is appropriate. Here, the required turn diameter is given by (4.196). From this, the winding height is given by (4.197) and the mean path length of the winding is given by (4.198).

$$\emptyset_w = \sqrt{\frac{4I_3}{J_{L,3}\pi}} \tag{4.196}$$

$$h_w \approx \frac{k_{f,cu}\emptyset_w N_2}{l} \tag{4.197}$$

$$\lfloor MPL \rfloor_{L,3} = 2\left[x_c + y_c + \frac{8}{2}d_{L,3} + \frac{8}{2}\left(N_2\emptyset_w + t_{i,3}(N_2 - 1)\right)\right] \tag{4.198}$$

$$R_{L,3} = \rho_{cu}\frac{2N_2\lfloor MPL \rfloor_{L,3}}{\pi(\emptyset_w/2)^2} \tag{4.199}$$

$$V_{L,3} = R_{L,3}i_3 \tag{4.200}$$

$$\bar{P}_{L,3} = V_{L,3}I_3 \tag{4.201}$$

In designing the passive bias circuit, an appropriate low voltage power supply must be chosen, capable of delivering the required voltage, (4.202), and matching the dissipated power, (4.203). Finally, it is pointed out that if a passive bias circuit is to be used in a long pulse high power application, the tertiary circuit should be designed at the same time as the demagnetization circuit. This is because the current increase described by (4.186) is also brought down by the demagnetization circuit. Thus, in order to ensure the function of the demagnetization circuit and also to get a correct trade-off between volume and losses, these should be considered simultaneously.

$$\sum V = V_{w,3} + V_{L,3} \leq \hat{V}_{lvps} \tag{4.202}$$

$$\sum P = \bar{P}_{w,3} + \bar{P}_{L,3} \leq \bar{P}_{lvps} \tag{4.203}$$

*Modeling of passive demagnetization circuit*

Following the pulse event, the transformer core has been magnetized to magnetic flux density $B_{max}$ associated with the magnetization current $I_m = \Delta i/2$. Furthermore, if the tertiary circuit described in the above section is employed, the current through the series bias inductor has increased from $I_{3,0} = \Delta i/2$ to $I_3 = (1 + p)\Delta i/2$. These currents represent energy stored in the transformer core and

the series inductor core, respectively. The energy added in a given pulse event must be removed prior to the following pulse event, or the magnetic components will saturate over the course of a series of pulses.

As discussed in the introductory section, the passive demagnetization circuit based on freewheeling diode with RC network is sometimes appropriate for long pulse high power applications. Here, the demagnetization resistance and capacitance must be selected such that 1) the magnetic components can be demagnetized or 'reset' within a time period $1/f_r - T_p$, and 2) the peak reverse klystron voltage is limited to load requirements. Furthermore, circuit losses should be minimized. As mentioned, in considering long pulse high power applications, it is not necessary that the demagnetization capacitance is discharged each pulse period. In such cases, it is necessary to solve the equations corresponding to the equivalent circuits of Figure 4.74 for multiple periods, each time using the initial conditions from the previous cycle. For such calculations, a state-space approach is favoured as described in the following.

In the first demagnetization period, immediately following the pulse event, the freewheeling diode starts conducting and the energy stored in the transformer leakage inductance is transferred to the demagnetization capacitance, some of it being dissipated in the load impedance, Figure 4.74.a. The behaviour of the circuit during this period is described by (4.204). Here, the initial condition of the inductor current is the peak load current referred to the primary, i.e., $I_2 k_w \frac{N_2}{N_1}$. Importantly, the initial condition of the demagnetization capacitor voltage is to be set according to the value obtained from the previous cycle, i.e., $v_{r(k)}(0) = v_{r(k-1)}(1/f_r)$. Obviously, if $k = 1$ then $v_{r(k)} = 0$.

$$\begin{pmatrix} \dot{v_r} \\ \dot{\imath_s'} \end{pmatrix} = \begin{pmatrix} 0 & 1/C_r \\ -1/L_s' & -R_k'/L_s' \end{pmatrix} \begin{pmatrix} v_r \\ i_s' \end{pmatrix} \tag{4.204}$$

During the second demagnetization period, the energy stored in the transformer core, i.e., the magnetization inductance, is transferred to the demagnetization network through the freewheeling diode, Figure 4.74.b. The behaviour of the circuit during this period is described by (4.205). The initial condition of the demagnetization capacitor voltage is set according to the previous period, $v_{r(k)}(t_1)$. The initial condition of the magnetization inductance current and the series bias inductor current are set in relation to the values obtained from the previous cycle, representing magnetization of the cores. Correspondingly, $i_{m(k)}(t_1) = i_{m(k-1)}\left(1/f_r - T_p\right)$ and $i_{3(k)}(t_1) = i_{3(k-1)}\left(1/f_r - T_p\right)$. Crucially, in a stable solution, the added magnetization should always be balanced by an equal

demagnetization each period. For $k = 1$, $i_{m(k)}(t_1) = \Delta i/2$ and $i_{3(k)}(t_1) = (1 + p)\,\Delta i/2$. If a bias circuit is not used, the corresponding row is simply omitted.

$$\begin{pmatrix} \dot{v}_r \\ \imath_m \\ \imath_3' \end{pmatrix} = \begin{pmatrix} -1/(R_r C_r) & 1/C_r & 1/C_r \\ -1/L_m' & 0 & 0 \\ -1/L_3' & 0 & 0 \end{pmatrix} \begin{pmatrix} v_r \\ i_m \\ i_3' \end{pmatrix} \tag{4.205}$$

Finally, during the third demagnetization period the freewheeling diode stops conducting, disconnecting the demagnetization network from the rest of the modulator circuit. Here, the demagnetization capacitor is discharged through the demagnetization resistor. The behaviour of the circuit during this period is described by (4.206). Again, the initial condition of the demagnetization capacitor voltage is set according to the previous period, $v_{r(k)}(t_2)$. Note that the third period is evaluated for a period of time approximately equalling $1/f_r$ as the capacitor is discharged also during the following pulse event itself.

$$\dot{v}_r = (-1/R_r C_r) v_r \tag{4.206}$$

As noted, in case the demagnetization capacitor is not fully discharged during period 3, the above set of equations must be solved for multiple pulse periods. The calculations are carried out until either the demagnetization capacitor voltage stabilizes on a period-to-period basis, i.e., $v_{r(k)}(1/f_r) \approx v_{r(k-1)}(1/f_r)$, or the transformer and/or series bias inductor cores saturate.

Given the fact that multiple sets of coupled differential equations need to be solved over several cycles in order to accurately determine 1) the stability of the solution and 2) the performance of the solution, no simple analytical design rule may be found. However, given that almost the entirety of stored inductive energy is transferred to the demagnetization network during the second period, a suitable starting point for design may be obtained by considering the parallel resonant circuit of Figure 4.74.b. Here, one could choose an undamped resonance frequency $\omega_0 = \frac{1}{(1/f_r - T_p)/2}$, yielding $C_r$ according to (4.207). Then, $R_r$ could be selected to yield a suitable damping factor resulting, e.g., in a critically damped system, (4.208). It is emphasized that the circuit of Figure 4.74.b is only valid for part of the demagnetization interval, and that these simplified values therefore merely should serve as a starting point for design.

$$C_{r,0} = \frac{1}{(2\pi)^2 \frac{L'_m L'_3}{L'_m + L'_3} \left( \left( f_r - 1/T_p \right)/2 \right)^2} \tag{4.207}$$

$$R_{r,0} = \sqrt{\frac{\left[ \frac{L'_m L'_3}{L'_m + L'_3} \right]}{4C_{r,0}}} \tag{4.208}$$

*Design procedure for passive auxiliary circuits*

In the following, the above considerations are summarized in formulating a complete design procedure for passive auxiliary circuit(s) (i.e., with or without transformer bias). It is emphasized that the circuits are auxiliary and can only be designed once the pulse transformer itself has been specified. At the same time, the implications of the auxiliary circuits in long pulse high power applications are non-negligible (e.g., in terms of added volume and power dissipation) and an integrated design approach should be used to ensure globally optimal performance. Such a design procedure is developed in section 4.6.

The design procedure for the passive auxiliary circuits is summarized in Figure 4.78. First, if a bias circuit has been assumed in pulse transformer design, this circuit must now be dimensioned. The passive bias circuit is essentially composed of a low voltage power supply, a tertiary winding and a series inductor. The number of tertiary winding turns $N_3$ determines the relationship between the tertiary winding voltage and the required tertiary current to appropriately bias the transformer core. In this formulation, $N_3$ is included as a swept parameter. Given $N_3$, characterization of the tertiary winding is simple given commercially available conductor sizes, (4.187)-(4.192). In parallel, the series bias inductor is optimized using the above developed design procedure. Here, the total voltage drop and power dissipation of the tertiary winding and the series bias inductor must be within the limitations of the power supply. If the power supply is already specified, these requirements become limiting constraints.

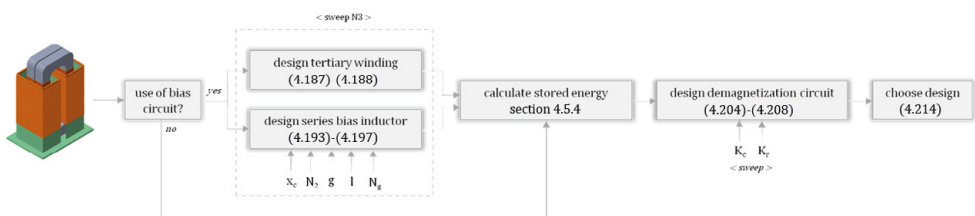



Figure 4.78: Design procedure for passive auxiliary circuit (tertiary bias winding and passive demagnetization)

Then, the demagnetization circuit is to be dimensioned (immediately, if no bias circuit was assumed in pulse transformer design). Here, the starting values $C_{r,0}$ and $R_{r,0}$ are calculated using (4.207)-(4.208). Then, with $C_r = K_c C_{r,0}$ and $R_r = K_r R_{r,0}$, $K_c$ and $K_r$ are swept and the corresponding demagnetization circuit performance is evaluated using (4.204)-(4.206). Generally, it is to be ensured that the magnetic flux density of the pulse transformer and the series bias inductor are reset each pulse period without exceeding the maximum reverse voltage requirements of the klystron load.

### 4.5.3 Modeling and design of active auxiliary circuit

Design of the active auxiliary circuit essentially comprises selection of 1) the auxiliary capacitor, 2) its fundamental operating voltage and 3) the active switch. However, as the operating current is relatively speaking very low (directly related to the magnetization current of the pulse transformer) and without much impact on system efficiency, circuit design is straightforward and without need for significant optimization. Instead, it will be seen that the downside of this circuit, and especially in long pulse high power applications, is the added system complexity. This section reviews the operating principle of the circuit and presents the corresponding circuit waveforms and design equations.

*Modeling and design*

Active auxiliary circuit operation is explained in the following referring to the circuit waveforms of Figure 4.79. The transformer core is assumed to be pre-biased, corresponding to a magnetization current of $-I_m$. The first pulse event begins at $t = 0$ by closing the main switch assembly $S_m$ and the transformer core is magnetized from $-I_m$ to $+I_m$ over the pulse period $T_p$. The pulse event ends by opening the main switch assembly $S_m$ at which time the magnetization current keeps flowing via the freewheeling diode $D_r$ into the auxiliary circuit capacitor $C_r$. Here, the magnetization inductance matches the auxiliary capacitor voltage (plus the forward voltage drop of the diode). As long as the capacitor voltage is relatively stable, i.e., within, e.g., 10-20% of its initial value, the demagnetization interval can be calculated according to (4.209).

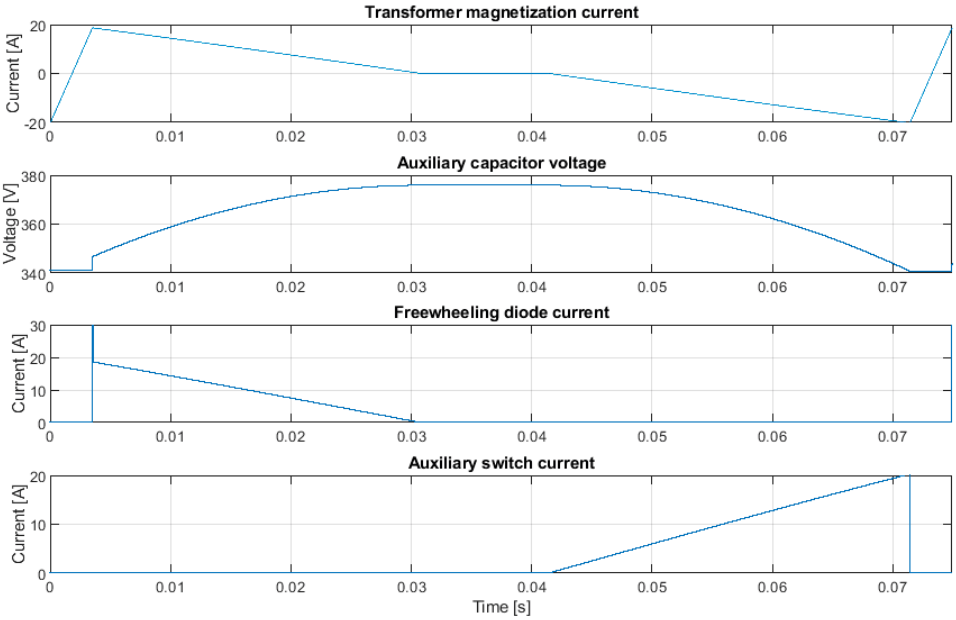



Figure 4.79: Fundamental active auxiliary circuit waveforms

$$v_L = L\frac{di_L}{dt} \rightarrow T_{dm} = L'_m \frac{I_m}{\bar{v}_{cr}} \tag{4.209}$$

$$v_{cr,min} = L'_m \frac{I_m}{\left(1/f_r - T_p\right)/2} \tag{4.210}$$

$$i_C = C\frac{dv_C}{dt} \rightarrow C_r \approx \frac{I_m\left(1/f_r - T_p\right)}{4k\bar{v}_{cr}} \tag{4.211}$$

Following the demagnetization interval, the auxiliary circuit switch $S_r$ is closed, applying the capacitor voltage $v_{c,r}$ to the pulse transformer primary winding in reverse. Since, according to the above, the capacitor voltage is approximately constant, the transformer is biased in roughly the same time period $T_{dm}$. Hence, it can be understood that the minimum auxiliary capacitor voltage $v_{cr,min}$, i.e., without interlocking period, is given by (4.210). The capacitance value itself must be set to ensure that the condition of voltage stability is met, (4.211). Here, $k$ is a constant indicating that $v_{cr}$ is to be kept within 10-20% of its stationary value.

Then, an appropriate auxiliary switch must be selected. Note here that the magnetization current is very low with respect to the capabilities of contemporary semiconductor technology. Still, the switch must be able to withstand the full

primary side voltage, i.e., in the case of long pulse high power modulators typically on the order of 5-10 kV. Provided that the voltage requirement can be met the losses are negligible from the perspectives of efficiency and thermal design given the low current and low switching frequency (i.e., the pulse repetition rate). Yet, in practice the associated losses – though relatively small – must be supplied somehow or the capacitor will discharge over time. Here, [4.42] notes the possibility to avoid use of an external power supply by enforcing a self-stabilizing flux condition. If the capacitor starts to discharge, it will not fully bias the core thus resulting in an asymmetric flux with an end of pulse magnetization current greater than $I_m$. This corresponds to additional energy which is used to bring the capacitor back to its initial voltage. For certain conditions, this state can be shown to be self-stabilizing [4.42]. Unfortunately, this type of operation requires an oversized magnetic core (unless a series of partial pulses are used to charge the capacitor over time before full pulsed operation begins, which is practically undesirable) which is not feasible in the present case. Instead, the lost energy must be supplied through an external power supply. Here, [4.42] proposes the solution of using a dc/dc boost converter connecting the auxiliary circuit to the main capacitor bank. Again, this requires a switch capable of switching the full primary side voltage at appreciable frequency. Yet another possibility involves using a separate grid-connected power supply. Evidently, the active auxiliary circuit is advantageous from a perspective of system losses and volume but is significantly more complex than that of the corresponding passive auxiliary circuits which are self-sustaining requiring no control.

### 4.5.4 Case study: bias and demagnetization system for pulse transformer for ESS modulator requirements

In this section, the developed design procedures for auxiliary circuits are applied to the case of the ESS modulator requirements. Here, the relevant design requirements are specified in Table 4.7. The modulator primary side voltage is assumed to be 6000 V. Though the primary voltage has an effect on the other parts of the modulator, these effects are not considered in the following analysis. In this case study, the optimized pulse transformer design derived for ESS application requirements in section 4.2 is used as illustration. Important characteristics of this pulse transformer design are also provided in Table 4.7. Complete optimization routine for pulse transformer-based modulators.

Table 4.7: Summary of ESS modulator requirements and assumed pulse transformer configuration for auxiliary circuit design

| Symbol | Quantity | Value |
|---|---|---|
| | Klystron modulator requirements | |
| $V_2$ | Rated output voltage | 115 kV |
| $I_2$ | Rated output current | 100 A |
| $T_p$ | Pulse length | 3.5 ms |
| $f_r$ | Pulse repetition rate | 4 Hz |
| | Pulse transformer characteristics | |
| $V_1$ | Primary-side voltage | 6 kV |
| $L_m^{'}$ | Primary-side magnetization inductance | 78.5 mH |

*Passive auxiliary circuit*

First, the design procedure for the passive auxiliary circuits – tertiary bias circuit and passive demagnetization circuit – is set up. As discussed in the preceding section, the tertiary bias circuit must be designed prior to the demagnetization circuit. Considering the significant losses represented by pulse transformer and bias inductor demagnetization it would be ideal to include the complete problem in a single concurrent optimization loop. As a matter of fact, optimizing the bias circuit without consideration of the corresponding demagnetization losses could be very misleading. At the same time, it is desirable to avoid looping the state space model, (4.204)-(4.206), required to fully characterize the demagnetization circuit to keep optimization time to a minimum. For these reasons, the bias circuit will be designed independently though accurately by estimating the losses given in demagnetization of the pulse transformer and the bias inductor by (4.212).

$$\langle P_{dm} \rangle = f_r \left[ \frac{1}{2} L'_m I_m^2 + \frac{1}{2} L_3 (I_3 p)^2 \right] \tag{4.212}$$

In designing the bias circuit, the following variables are considered free design parameters. For the bias inductor, the core leg width (xc), the number of winding turns ($N$), the air gap length ($g$) and the maximum RMS winding current density ($J$) are freely set by the optimizer; for the tertiary winding, the number of winding turns ($N_3$) is freely set by the optimizer. In addition, the number of winding layers per bias inductor winding ($N_l$) and the number of air gaps per inductor core leg ($K_g$) are swept. In designing the demagnetization circuit, the design procedure outlined in

section 4.5.2 is applied straightforwardly, providing refinement to the estimated demagnetization losses, (4.212).

In view of the above, the decoupled optimization problems may be formulated as (4.213)-(4.214). Here, $K$ is swept from 0 to 1 in generating trade-offs between bias inductor volume and the losses represented by the auxiliary circuits taking the corresponding demagnetization losses into account. The procedure is repeated for different integer values of $K_g$ and $N_l$. In the following, the core depth is limited to 1.0 m, the inductor height is limited to 1.0 m, the current density is limited to 5 A/mm$^2$, the peak magnetic flux density is limited to 1.0 T, and the length per air gap ($g$) is limited to 10 mm. Lower bounds are imposed mainly to prevent impractical and unphysical solutions.

$$\begin{gathered} minimize\ f(x) = K\frac{(x_c y_c l_c)}{V_0} + (1-K)\frac{\left(\bar{P}_{L,3} + \bar{P}_{w,3} + \bar{P}_m\right)}{P_0} \\ x = \{x_c, N_b, g, J, N_3\} \\ \\ subject\ to: \\ x_l \le x \le x_u \\ H(x) \le 0 \\ \\ where: \\ x_l = \left\{x_{c,min}, N_{b,min}, g_{min}, J_{min}, N_{3,min}\right\} \\ x_u = \left\{x_{c,max}, N_{b,max}, g_{max}, J_{max}, N_{3,max}\right\} \\ H(x) = \left\{h_w + 2x_c + 2r_i - \hat{h}_c, y_c - \hat{y}_c, \hat{B} - B_{max}\right\} \end{gathered} \tag{4.213}$$

$$\begin{gathered} minimize\ f(x) = P_{dm} \\ x = \{C_{dm}, R_{dm}\} \\ \\ subject\ to: \\ H(x) = \{\max(v_r) - 0.1V_2\} \le 0 \end{gathered} \tag{4.214}$$

Running (4.213) using MATLAB fmincon assuming one winding layer per inductor winding ($N_l = 1$) and three air gaps per inductor leg ($K_g = 3$) result in the solution space presented in Figure 4.80. Here, a clear trade-off between the bias inductor volume and auxiliary circuit losses is seen. Note that, for these settings, the total losses always exceed that of 14 kW, i.e., more than 2% of rated modulator power. Study of the trade-off region reveals that use of a comparatively smaller bias inductor, e.g., with a magnetic core volume of 0.25 $m^3$ corresponding to ~1900 kg, implies losses approaching 22 kW, beyond 3% of the rated modulator power.

Evaluating the same procedure sweeping the number of winding layers as well as the number of air gaps per core leg generates the results shown in Figure 4.81. Here, only the pareto optimal solutions are shown for clarity. As can be seen, adding winding layers allows a more compact solution for the same loss dissipation. For a given geometry, keeping the number of winding turns constant represents constant losses though the winding (and thus its height) may be subdivided in several sections. Of course, this comes at the price of a somewhat more complicated construction.

As described by (4.213), the length per air gap has been limited to 10 mm to ensure reasonable control of fringe field effects. Still, the effective air gap may be increased by use of several air gaps (i.e., a distributed air gap) over the length of the core leg. The benefit of this may be understood by analysing (4.193) and (4.195) simultaneously. Consider first an inductor utilizing a single air gap per core leg. Adding a second air gap per core leg in principle allows doubling the number of winding turns without saturating the magnetic core, (4.195). At the same time, these changes – adding a second air gap per core leg and doubling the number of winding turns – correspond to a doubling of the inductance, thereby allowing significantly smaller core geometry for a given target inductance provided the added number of turns can be accommodated by the inductor geometry without violating the inductor height constraint. This effect is clearly seen in Figure 4.81.

Importantly, however, even if five air gap spacers per core leg and four winding layers per bias inductor winding would be used, the total loss still exceed 12 kW and requires a bias inductor magnetic core volume of ~0.25 $m^3$. Here, the feasibility and practicalities of such a design must be taken into account. In the following, a more practical (though still extremely discouraging) solution based on three air gap spacers per core leg and four winding layers per bias inductor winding is assumed in considering design of the demagnetization circuit. Such a design is seen to correspond to minimum auxiliary circuit losses of approximately ~38 kW and a bias inductor core volume of 0.175 $m^3$.

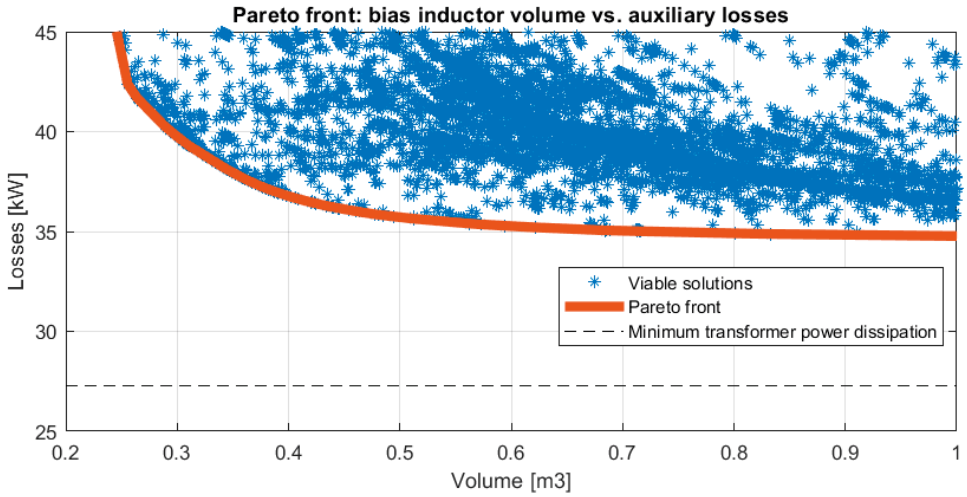



Figure 4.80: Solution space for passive auxiliary circuit intended for the pulse transformer-based modulator application summarized in Table 4.7. The Pareto front illustrates trade-offs between viable solutions by considering the relationship between bias inductor volume versus auxiliary circuit losses.

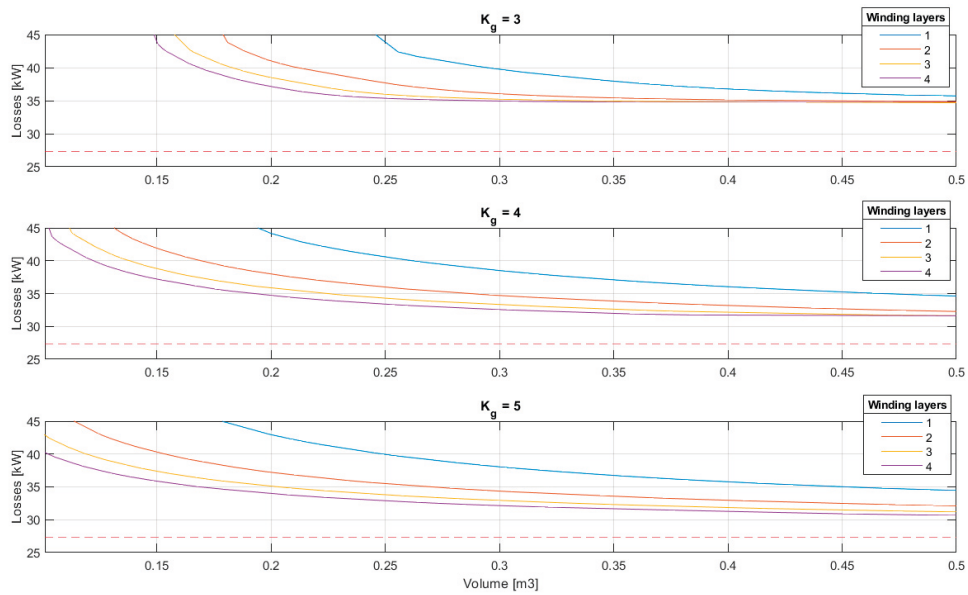



Figure 4.81: Pareto optimal solutions for passive auxiliary circuit intended for the pulse transformer-based modulator application summarized in Table 4.7. Each subplot corresponds to a number of air gaps per inductor core leg with the number of winding layers per bias inductor winding shown as parameter.

To design the demagnetization circuit, (4.214) is evaluated by sweeping $C_r$ and $R_r$ according to $C_{r,0}$ and $R_{r,0}$ via the state space equations derived in (4.204)-(4.206). Here, the above design is utilized. The results are shown in Figure 4.82. As can be

seen, the losses shown in Figure 4.81 estimated from the stored magnetic energy correspond very well to that actually simulated by looping (4.204)-(4.206).

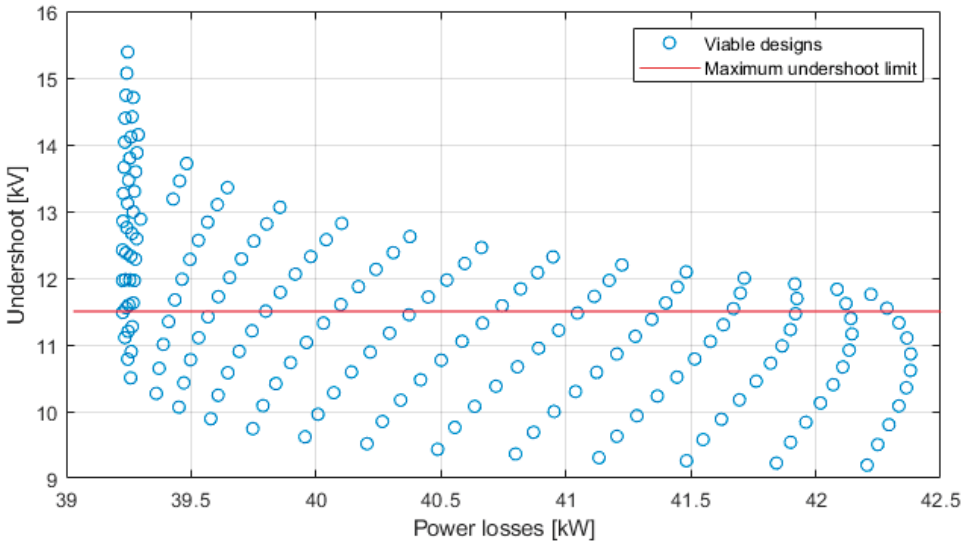



Figure 4.82: Trade-off between resulting klystron undershoot voltage and demagnetization power losses

In conclusion, implementing the passive auxiliary circuit in view of long pulse high power applications expectedly requires a quite large inductor (bulkier than the pulse transformers considered in many other applications) and represents losses on the order of several percent of the rated modulator power. For these reasons, though conceivable, the passive auxiliary circuit should here be considered disadvantageous and impractical.

*Active auxiliary circuit*

As mentioned in section 4.5.3, the majority of the active auxiliary circuit is dimensioned by way of equations (4.210)-(4.211). Assuming a demagnetization period $T_{dm} = \left(1/f_r - T_p\right)/2 - t_i = 32\,ms$, where $t_i$ is the intermediary interlocking period, (4.210)-(4.211) suggest an auxiliary capacitor of 32.6 mF with a nominal operating voltage of approximately 275 V. Such a capacitor configuration may be realized by parallel connection of, e.g., 15 units of the capacitor ALS30A222NP500, [4.43]. This capacitor is rated 500 V and each capacitor can represents 2200 µF, yielding a total capacitance of 33 mF.

The auxiliary switch must be rated for the full primary voltage, here assumed to be 6000 V. Here, it is possible to implement the switch and the freewheeling diode using a single IGBT module. Note that the freewheeling diode experiences the surge current seen in demagnetizing the leakage inductance referred to the primary, i.e.,

with a primary voltage of 6 kV representing a current peak on the order of 2 kA. As the module must be rated to withstand this current, the switch may be implemented by, e.g., IGBT module FZ750R65KE3 from Infineon, [4.44]. This module is rated 6.5 kV operation and a repetitive peak collector current of 1.5 kA. Since the time required to demagnetize the leakage inductance is far shorter than the rated surge current time, it is very likely to withstand the 2 kA surge in this case.

Figure 4.83 shows simulation results for the above-described auxiliary circuit. First, the auxiliary capacitor is charged by an external power supply over 100 ms to its nominal voltage of 300 V. Then, the auxiliary switch is closed to apply the auxiliary capacitor voltage to the primary winding of the transformer. The transformer core is now biased to $-I_m$ over the period $T_{dm}$. During this interval, the auxiliary switch carries the magnetization current and the auxiliary capacitor voltage drops somewhat accordingly. Following transformer biasing, the auxiliary switch is opened and the main switch assembly is closed. During the pulse, the transformer core is magnetized from $-I_m$ to $+I_m$. Then, following the pulse event, both the main switch assembly and the auxiliary switch are open and the circuit current freewheels via the diode into the auxiliary capacitor. Note the surge current associated with demagnetizing the leakage inductance. Note also that, given the low conduction losses and low transformer resistive losses, the magnetization energy is essentially fully recovered to charge the auxiliary capacitor back to its nominal value. Therefore, in practice, only a small typical 400 V low power supply would be needed to sustain circuit operation.

Finally, Figure 4.84 importantly shows the pulse output voltage. In particular, a zoom on the pulse undershoot shows that the maximum undershoot value is limited to 7 kV, i.e., well within the limits of the klystron. Note also that the klystron voltage is zero during the interlocking period.

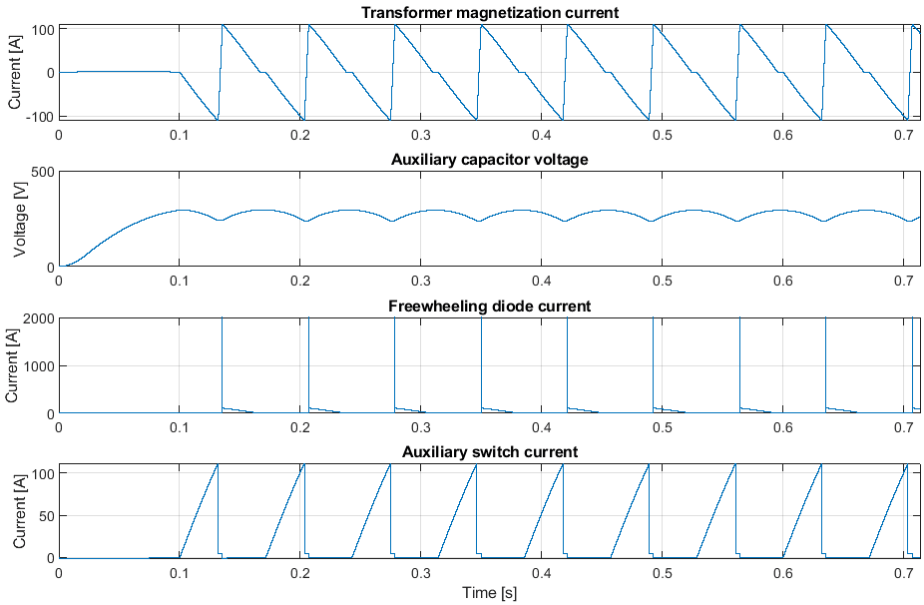



Figure 4.83: Simulated circuit waveforms for chosen auxiliary circuit intended for pulse transformer biasing and demagnetization in klystron modulator application summarized in Table 4.7.

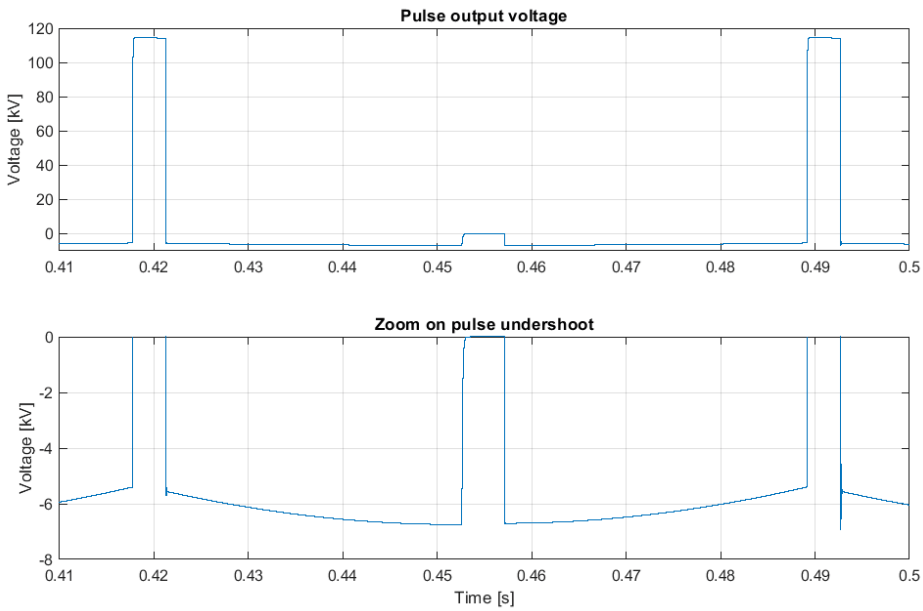



Figure 4.84: Simulated pulse output voltage waveform using chosen auxiliary circuit. The pulse undershoot is limited to 7 kV, well below 10% of the rated klystron voltage, Table 4.7.

The chosen design is compact and efficient. The capacitor has a diameter of 7.7 cm and a height of 14.6 cm, i.e., the total capacitor configuration footprint is less than 0.1 $m^2$ and the corresponding volume is less than 0.015 $m^3$. The weight is below 15 kg. The capacitor has a specified ESR of 0.06 ohm per capacitor can [4.43]. Assuming a triangular current profile essentially corresponding to the transformer magnetization current, Figure 4.83, total capacitor losses may be estimated as $\bar{P}_c = \frac{ESR_C}{N_c}\left(\frac{I_m}{\sqrt{3}}\right)^2$ and seen to be on the order of 15 W. Similarly, considering the semiconductors, switch and diode conduction times are similar and approach $2/fr$. Consequently, modules losses are on the order of a few tens of W, minimal with respect to modulator power and requiring little to no cooling. In this case, comparing the results to that of the corresponding passive auxiliary circuit, the added complexity of the active auxiliary circuit is undoubtedly justified.

# 4.6 Optimization of complete pulse transformer-based modulator

The preceding sections have presented mathematical modeling and sizing of the main power components comprising the pulse transformer-based modulator with the exception of the capacitor charger. In this thesis, the capacitor charger is assumed – as is typically the case – to be based on the integration of commercially available rack-mount chargers. This is discussed in section 4.6.1. Then, section 4.6.2 provides additional treatment of the design of the main capacitor bank energy as well as the electromechanical integration of the required modulator components. Finally, based on the work and the results presented in this chapter, section 4.6.3 proposes an integrated optimization procedure for pulse transformer-based modulators, [4.45].

## 4.6.1 Capacitor charger

The capacitor charger replenishes the main capacitor bank energy storage in-between pulse events. As generally $T_p \ll 1/f_r$, the charger assembly is sized to deliver the system average power. Considering high-power klystron modulator applications, capacitor chargers are typically assembled in standardized electrical cabinets, interconnecting multiple commercially available rack-mount charger units. In principle, this idea may be extended to cover any power rating by parallel connecting additional charger units. A survey on commercially available high-power capacitor chargers in the 1-20 kV range, [4.46]-[4.48], establishes the preference to handle integration using 800x800x2000 cabinets, resulting in a typical average power density of approximately 150 kW per cabinet. The corresponding

electrical efficiency ranges from 85-95%, though the conditions underlying these measurements are vague. In practice, the impact on modulator system efficiency is somewhat greater due to the generated line-side harmonics and reactive power as well as the fact that the charger system cannot be operated at full load. In this work, a typical electrical efficiency of 90% is assumed. In keeping with the above, the trend relating capacitor charger footprint to rated average power shown in Figure 4.85 is developed.

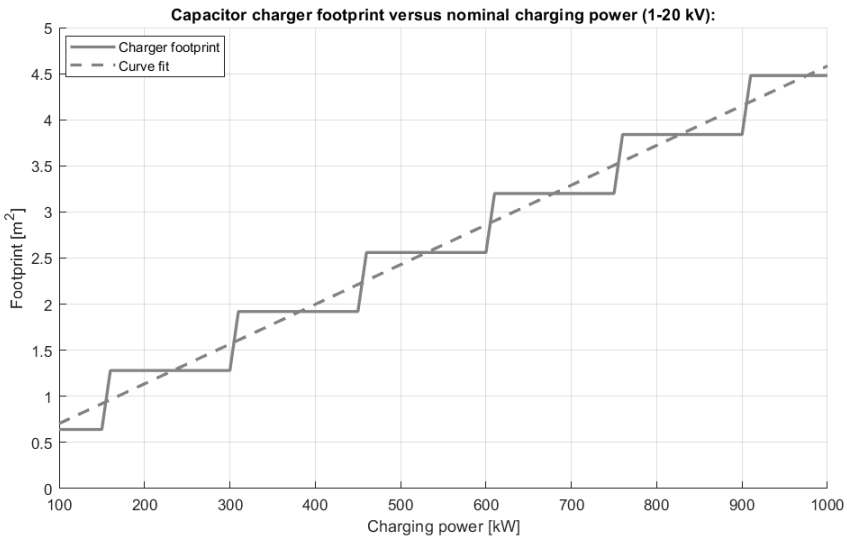



Figure 4.85: Estimated capacitor charger footprint as function of rated average power considering commercially available rack-mount charger units

## 4.6.2 Electromechanical integration

First, in ensuring a globally optimal design, placement of the main power components in electrical cabinets must be considered. Here, standard cabinets with depth $D_c$ = 800 mm and height $H_c$ = 2000 mm are considered. The width, $W_c$, may vary (600 mm, 800 mm, or 1200 mm) according to requirements. The relevant procedure for sizing and integrating the capacitor charger units was described in the preceding section. The rest of the components are treated in the following.

*Main capacitor bank energy storage*

Despite use of a droop compensation circuit (bouncer) in minimizing the capacitor bank energy storage, it is still a sizable component considering long-pulse high-power applications, requiring a dedicated (set of) cabinet(s). Use of high-energy density polypropylene capacitors integrated in rectangular casing is assumed.

Importantly, in achieving the required capacitance, the capacitor reference should be chosen such that the external dimensions of the electrical cabinet(s) housing the required capacitor cases are minimized. Here, it should be recognized that a given capacitor unit may be arranged in six geometrically unique orientations. From a catalogue of commercially available capacitors assembled from, e.g., [4.46]-[4.48], an appropriate capacitor reference may be selected as follows. The process is summarized in Figure 4.86. First, for each capacitor reference, the number of required capacitor units is calculated from $C_m/C_i$, where $C_i$ is the per-unit capacitance of the i:th capacitor reference. Considering each of the possible capacitor orientations, the number of capacitor units that may be fit per unit cabinet height and depth is calculated according to (4.215) and (4.216), respectively.

$$N_{c,h} = H_c/[H_i(o_c)] \tag{4.215}$$

$$N_{c,d} = D_c/[D_i(o_c)] \tag{4.216}$$

where $H_i(o_x)$ and $D_i(o_c)$ are the height and depth of the i:th capacitor reference as function of the considered capacitor orientation $o_c$. From this, the required number of capacitor columns is given by (4.217).

$$N_{c,c} = ceil\big(C_m/\big(N_{c,h}N_{c,d}C_i\big)\big) \tag{4.217}$$

Then, starting with a single cabinet with $W_c$ = 600 mm, it is checked if the required capacitor bank width, i.e., $N_{c,c}W_i(o_c)$, would fit. If not, the cabinet width is successively increased in accordance with the above. If it turns out that a 1200 mm cabinet is insufficient to house the capacitors, a second cabinet may be added. The process is repeated until a suitable arrangement has been found. The minimal external dimensions of the capacitor bank cabinet for the i:th capacitor reference in the orientation $o_c$ directly follow. Repeating the procedure for all capacitor references in the developed catalogue, an optimal arrangement is straightforwardly found.

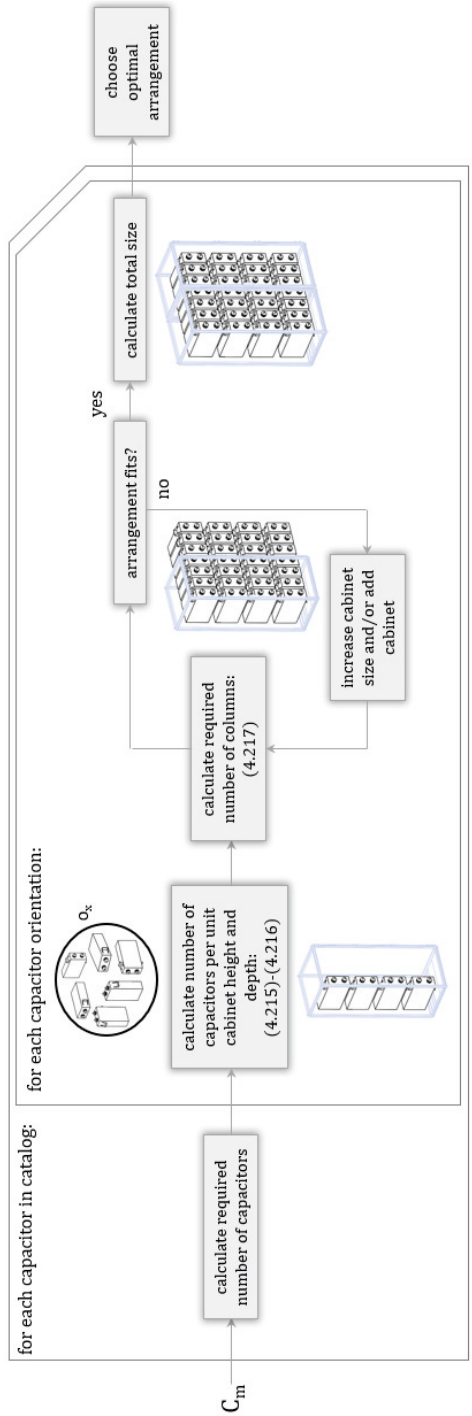



Figure 4.86: Flowchart summarizing procedure in optimizing set of cabinets housing the main capacitor bank storage.

*Electronic bouncer circuit*

In considering electromechanical integration of the electronic bouncer circuit, it should first be noted that an independent (low-voltage) capacitor charger is required. Importantly, in view of high-power multi-millisecond applications with repetition rates beyond that of ~10 Hz, this charger must be rated for several tens of kW – even upwards of ~100 kW – possibly requiring a significant portion of a typical electrical cabinet in accordance with that presented in section 4.6.1. Then, the multi-phase DC/DC converter requires $N_p N_m$ high-power half-bridge modules assembled in a power stack arrangement including water cooled heatsink, gate drivers, and other features. Importantly, the required IGBTs (and consequently, the power stack itself) are chosen largely with respect to peak power requirements in managing converter lifetime, [4.30]. Hence, power stack size is not significantly impacted by the system average power. The remaining power components are, though non-negligible, comparatively small and, similarly, less affected by system average power. Consequently, unless the rated modulator power is excessive, it is assessed that the complete electronic bouncer circuit may appropriately be housed in a single 1200x800 electrical cabinet. For very high rated modulator power, larger or several cabinets may be necessary.

*HV switch assembly*

Then, a single 800x800 cabinet is used to integrate the solid-state switch assembly and the auxiliary circuit. Additionally, this cabinet may also fittingly house the klystron auxiliary power supplies (filament, electromagnet and electron gun power supplies) as well as the main modulator control system. Again, all of these components are little affected by the modulator average power rating.

*Pulse transformer*

Finally, the pulse transformer is to be integrated in a high-voltage oil tank assembly including high-voltage sensor, output current sensor(s), and other auxiliaries. In this work, the size of the integrated oil tank assembly is estimated directly from the size of the pulse transformer. As was shown throughout section 4.2, the height of pulse transformers used in long-pulse high-power applications easily approach and exceed that of 1.5-2.0 m. To sustain reasonable system maintainability, the corresponding oil tank assembly height is limited by placing the HV sensor next to the pulse transformer unit such that the oil tank footprint may be estimated by $(W_T + 2d_i)(D_T + 3d_i + \emptyset_s)$, where $\emptyset_s$ is the external diameter of the HV sensor.

It is pointed out that it is not generally self-evident how the developed electrical cabinets and oil tank assembly should be placed in optimizing the resulting modulator design. For this reason, in this work, the resulting modulator footprint is estimated by algebraically summing the footprints of the comprising systems. It is also emphasized that the above models and procedure neglect power cabling, routing, signal measurements, contactors, capacitor discharge systems, and other

required auxiliary components. Of course, these components must also be carefully considered in developing a complete klystron modulator design.

### 4.6.3 Integrated optimization procedure

Now, the developed models are integrated in a framework for design optimization. The process is summarized in Figure 4.87. It is preferable to begin modulator design with the optimization of the pulse transformer component. This is because it is typically the most complex component with several design constraints tied to modulator pulse performance. Furthermore, assuming proper bouncer operation, it may be assumed that the pulse transformer experiences a constant primary-side voltage $V_1$, i.e., design is independent from that of the other modulator components. If a feasible transformer design cannot be found within the constraint imposed by the applications, it may be necessary to consider use of a different modulator topology. On the other hand, for a feasible transformer, the solid-state switch assembly and the active auxiliary circuit may straightforwardly be designed using the procedures outlined in sections 4.4 and 4.5.3, respectively.

Then, in considering design of the main capacitor bank, the associated capacitor charger and the droop compensation circuit, it is of interest to sweep the droop (through $k_d$) in studying the possible trade-offs between system volume and system efficiency. For a given droop, $C_m$ is given by (4.94) and implemented using the procedure summarized in Figure 4.86. Then, the main capacitor charger is sized for the power given by (4.218).

$$\bar{P}_{C,m} = \frac{f_r C_m}{2} V_1^2 \left[2k_d - k_d^2\right] \tag{4.218}$$

Then, the electronic bouncer charger is sized for the power given by (4.219).

$$\bar{P}_{C,b} = \frac{f_r}{2}\left[k_d \hat{V}_{Cm} I_2' T_p - C_{b,o}\left(k_d \hat{V}_{Cm}\right)^2\right] \tag{4.219}$$

Here, $\bar{P}_{C,b}$ typically evaluates to be $\sim(k_d/2)\bar{P}_{C,m}$. Finally, the component losses and volumes resulting from the above modeling are summed, allowing selection of a suitable modulator design from a Pareto front.

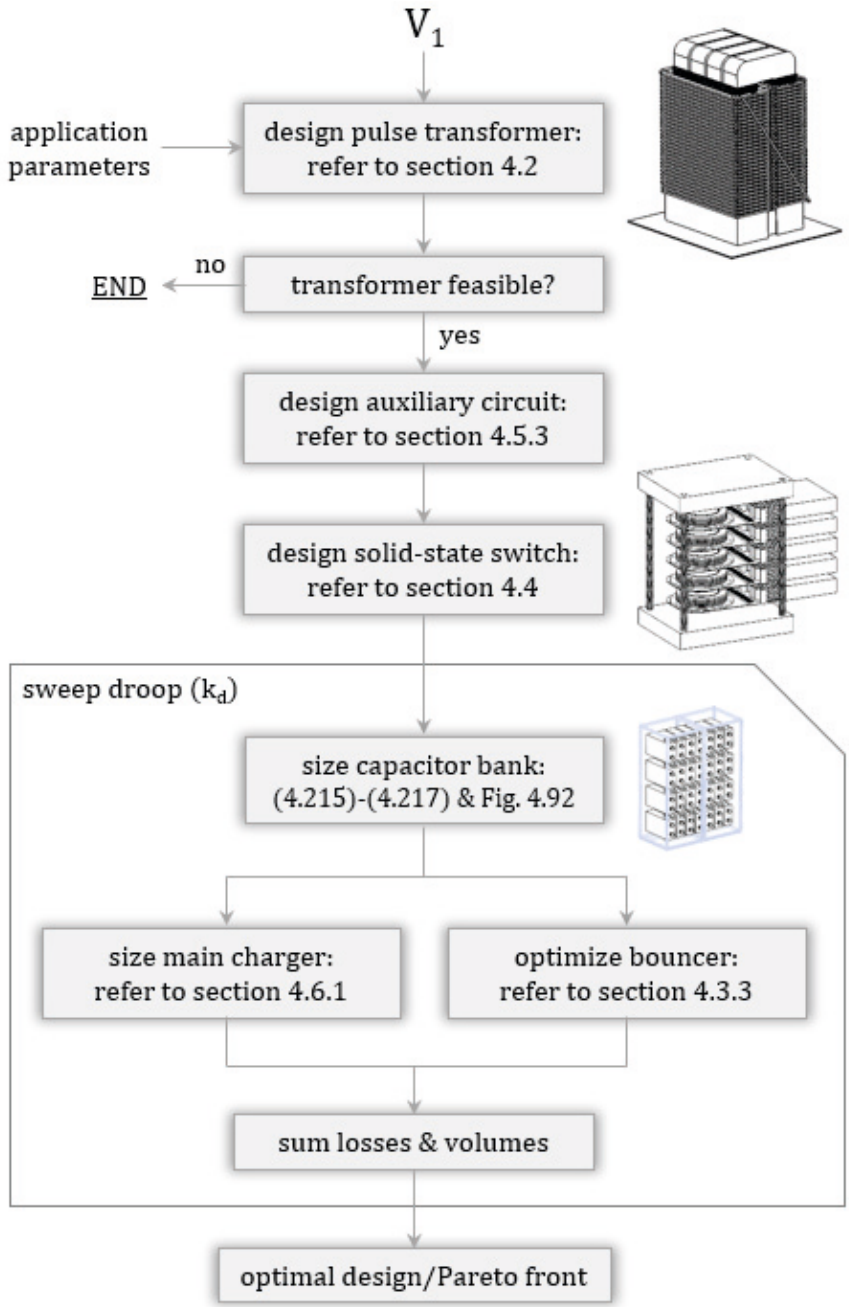



Figure 4.87: Optimizaton procedure for complete pulse transformer-based modulator

# 4.7 Case study: commercial HV pulse transformer

## 4.7.1 Background

In 2015, a commercial modulator system was lent to ESS from CERN to facilitate the then on-going early conditioning and testing of klystrons. At CERN, this modulator had been intended for use in the SPL (Superconducting Proton Linac) project, with specifications outlined in Table 4.8. As has been described, the ESS klystron modulators drive up to four klystrons in parallel, and comparing the ESS modulator requirements, Table 4.1, to those of Table 4.8, it is clear that one SPL-type modulator is sufficient to drive one such klystron.

**Table 4.8: Summary of SPL modulator requirements**

| Symbol | Quantity | Value |
|---|---|---|
| | Klystron modulator requirements | |
| $V_2$ | Rated output voltage | 115 kV |
| $I_2$ | Rated output current | 25 A |
| $T_p$ | Pulse length | 2.8 ms |
| $f_r$ | Pulse repetition rate | 4 Hz |
| $t_r$ | Pulse rise time | 300 μs |
| $\Delta V_{pp}$ | Flat top droop requirement | $\leq 1\%$ |

In 2016, during testing, a fatal modulator error occurred. Upon investigation, it was found that the glue attaching the pulse transformer windings to the fiberglass bobbin was not compatible with the oil. The pulse transformer windings were based on the pancake winding technique and at least one pancake had become fully detached from the bobbin. Then, falling on top of the below pancake, resulting in a short circuit across the transformer output.

During refurbishment of the pulse transformer, i.e., re-winding the transformer secondary windings, inclusion of winding spacers between pancakes, and utilization of compatible glue, a complete characterization the entire modulator system including the pulse transformer was made to better understand the system.

The purpose of this section is twofold-

1. Describe the use of the developed models to characterize the commercial modulator (individual components as well as the integrated system), where possible comparing calculated and simulated values and waveforms to experimental results obtained from measurements on the modulator.
2. Use the proposed optimization procedure to develop a complete modulator design for the specification of Table 4.8, comparing the result to that of the commercial modulator.

As shall be seen, the proposed optimization procedure generates a design very similar to that of the commercial modulator, validating the developed models and design procedures.

### 4.7.2 Evaluation of commercial modulator system

An overview of the commercial modulator system is shown in Figure 4.88, and the corresponding reduced schematic of the modulator is shown in Figure 4.89.

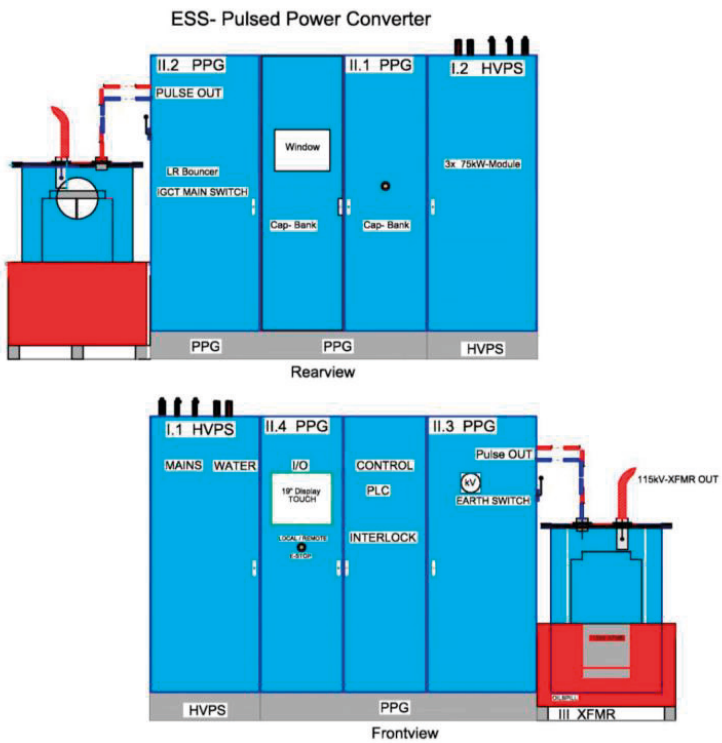



Figure 4.88: Overview of commercial modulator system

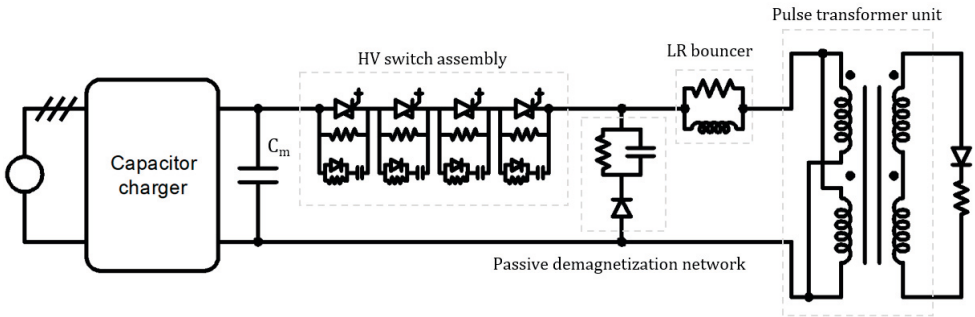



Figure 4.89: Reduced simplified schematic of commercial modulator system

*Capacitor charger and main capacitor bank*

The modulator utilizes a 225-kW capacitor charger (SV225-00, 3x75 kW charger modules from Poynting) charging the modulator main capacitor bank to 5.5 kV. Here, the main capacitor bank is itself comprised of 8 capacitor units of 880 µF each (E56.N88-8841A0 from Electronicon) for a total capacitance of 7.04 mF. Here, two important comments are made-

- Considering the modulator average output power, Table 4.8, it appears that two (as opposed to three) 75 kW charger modules would be more than sufficient, even when accounting for system efficiency.
- The main capacitor bank is very large, representing a main capacitor bank droop of less than 4%. This is because a passive LR bouncer is used for droop compensation. Still, as will be seen, this arrangement does not appropriately compensate the flat top droop.

*HV switch assembly*

The HV switch assembly is based on 4 series connected IGCTs, model 5SHY 35L4512, from ABB. As explained in section 4.4, each IGCT is equipped with static and dynamic compensation circuits. For static compensation, a $0.25\ M\Omega$ resistor is placed in parallel with each IGCT. Substituting 5SHY 35L4512 datasheet values into (4.165) with $N_s = 4$ and $R_C = 0.25\ M\Omega$ yields a worst-case static switch voltage of just below 2.6 kV, less than the rated 2.8 kV permanent DC voltage for 100 FIT failure rate, [4.49]. For dynamic compensation, a parallel RCD snubber is used. Here, $R_s = 10\ \Omega$ and $C_s = 2.5\ \mu F$.

*Pulse transformer*

A photograph of the pulse transformer unit (after the aforementioned refurbishment) is shown in Figure 4.90. As can be seen, the secondary windings are series connected and are based on the pancake winding technique. For this reason, the windings are parallel to the primary windings and to the core. The distance between

the smaller secondary winding and the associated primary winding is 2 cm, and the distance between the larger secondary winding and the associated primary winding is 4 cm; appropriately corresponding to a peak potential difference on the order of 3 kV/mm. Here, the smaller secondary winding has 22 pancake stacks whereas the larger secondary winding has 21 pancake stacks. Each stack is comprised of 45 winding layers for a total of 1935 secondary winding turns. The layer strip width is 15 mm and the layer strip thickness is 0.2 mm, representing a relatively conservative RMS current density of ~1.65 A/mm2. A distance of roughly 7 mm has been introduced between stacks for ease of interconnection. As discussed in section 4.2, the secondary winding experiencing a lower voltage has been made smaller in minimizing leakage inductance.

The pulse transformer core is biased through a tertiary winding placed on the lower end of the smaller secondary winding. As can be seen, the tertiary winding is essentially a single pancake stack, here also with 56 layers. For simplicity, the same copper strip used in constructing the secondary winding stacks has been used in constructing the tertiary. The primary windings, though not explicitly shown in Figure 4.90, are implemented using rectangular enamelled copper wire. Here, each primary winding has 90 turns with a cross-section 5x2 $mm^2$. As indicated in Figure 4.89, the primary windings are parallel connected.

The pulse transformer core is comprised by five Si-Fe magnetic cores, each with an external cross-section of 10 x 10 cm.

Finally, using the definitions developed in section 4.2, the external width of the pulse transformer unit is ~0.49 m, the external height is ~0.86 m, and the external depth is ~0.68 m.

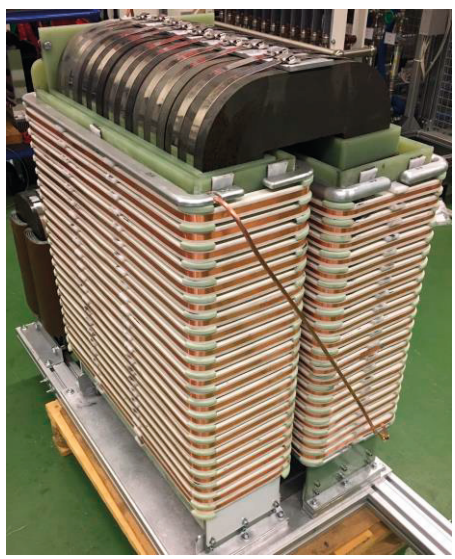


Figure 4.90: Pulse transformer unit used in commercial modulator (after refurbishment of secondary windings)

At this point, the summarized information may be used to calculate the peak magnetic flux density yielding 1.55 T. Similarly, assuming $\mu_r \sim 3000$, (4.49) is used to estimate the magnetization inductance seen from the primary to 0.91 H. These values are verified in the following by simulating the geometry of Figure 4.90 under magnetostatic conditions. Two simulations are made as shown in Figure 4.91: a) the core is biased by exciting the tertiary winding while the primary and secondary windings are left open, and b) the core is excited from both the tertiary and the primary windings whereas the secondary winding is left open. These simulations neglect the load current and correspond to the expected peak magnetization conditions represented by the instants in time a) just prior to pulsing (i.e., fully reset and biased magnetic core) and b) just following a given pulse event. As predicted, both cases simulated and shown in Figure 4.91 display a straight section peak magnetic flux density of 1.55 T, representing symmetrical magnetization. Note that the peak magnetic flux density of, e.g., the corners of the magnetic core is quite high, exceeding 2.5 T. This, however, is due to the assumption of a linear core material. In practice, when part of the material approaches the material saturation point, the local permeability is reduced thereby equalizing the field over the width of the core leg. Then, though somewhat redundant, the magnetization inductance may be verified by integrating the energy stored in either field shown in Figure 4.91, noting that the stored energy should correspond to $\sim 1/2\, LI^2$. From this, the value 0.93 H was derived, i.e., within ~1.5% of that calculated using (4.49).

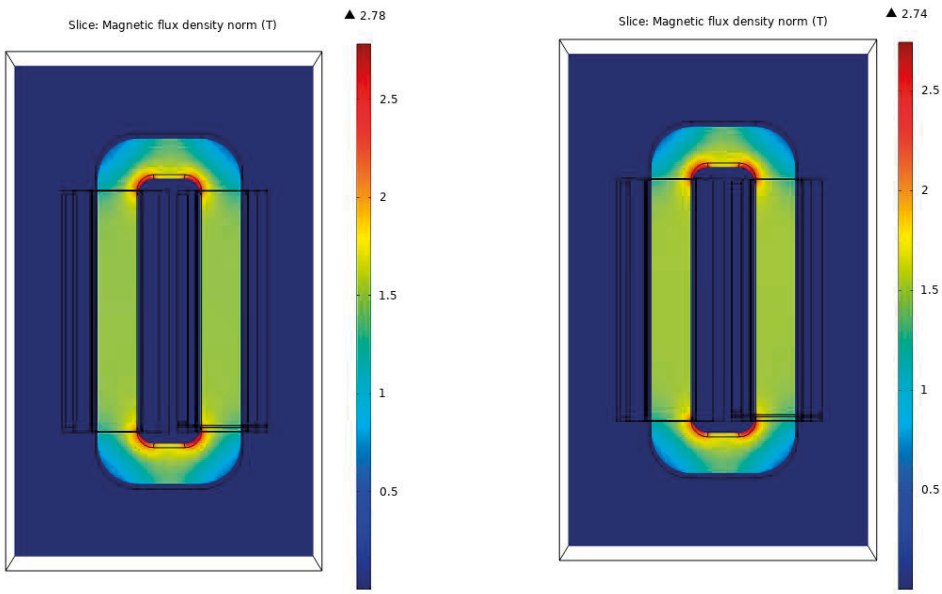



Figure 4.91: Magnetostatic simulation of pulse transformer geometry, a) pulse transformer excited from tertiary winding with open circuited primary and secondary windings; b) pulse transformer excited from both tertiary and primary windings with open circuited secondary winding.

Then, exciting the pulse transformer according to peak load conditions, i.e., with $I_2 = 25\ A$ and $I_1 = \big((N_{2,a} + N_{2,b})/N_1\big)I_2 \sim 269\ A$, and neglecting magnetization allows calculation of the pulse transformer leakage inductance. Magnetostatic simulation results under these conditions are shown in Figure 4.92. Here, integration of the magnetic energy density over the transformer volume yields $L_s'' = 0.238$, verified to be within 8% of that calculated using the procedure developed in section 4.2.4.

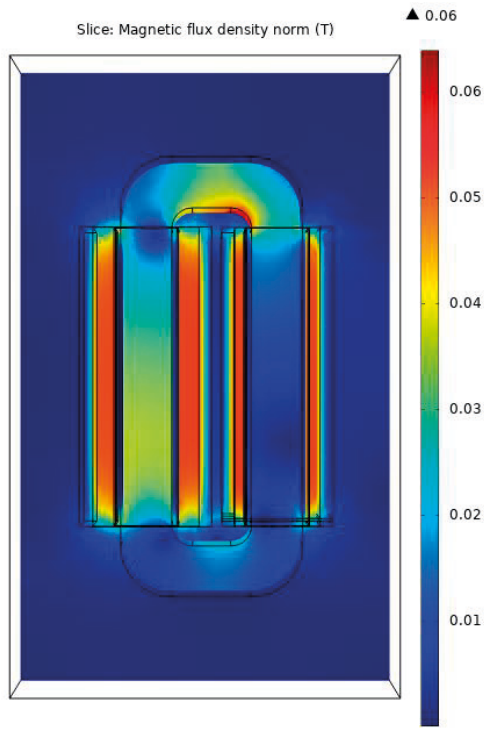



Figure 4.92: Magnetostatic simulation of pulse transformer geometry. Pulse transformer excited from primary and secondary windings according to peak load conditions.

Finally, it is also of interest to simulate the pulse transformer under electrostatic conditions to 1) verify the peak electrostatic field strength and to 2) derive the equivalent lumped stray capacitance value. Here, as shown in Figure 4.93, anti-corona rings of have been installed on top of the smaller secondary winding leg as well as on the bottom of the larger secondary winding leg, whereas an oval anti-corona ring of 25x10 mm in diameter has been installed on top of the larger secondary winding leg for electric field enhancement.

In this simulation, the voltage across the secondary windings is imposed according to (4.5) such that a linearly increasing electric potential is obtained. Similarly, the

voltage across the primary windings is set according to (4.40). The magnetic core and the oil tank walls are grounded.

A two-dimensional slice passing through the center of pulse transformer geometry in the front plane and depicting the simulated electrostatic potential is shown in Figure 4.93, validating the above statements. The corresponding electrostatic field strength is shown in Figure 4.95 (front plane) and Figure 4.96 (top plane). These figures demonstrate that electrostatic field strength is limited to well below that of 10 kV/mm. As a matter of fact, the peak electrostatic field strength appears to be on the order of 7…8 kV/mm, expectedly along the anti-corona ring of the larger secondary winding leg. The electrostatic field strength in the bulk volume of the pulse transformer geometry is conservatively limited to between 2…3 kV/mm.

Integration of the simulated electrostatic field strength over the pulse transformer geometry volume yields an estimate of the lumped stray capacitance and is simulated to be 0.615 nF. This value is compared to the analytical estimate, (4.42), calculated to be 0.584 nF. These values are within 5% of one another.

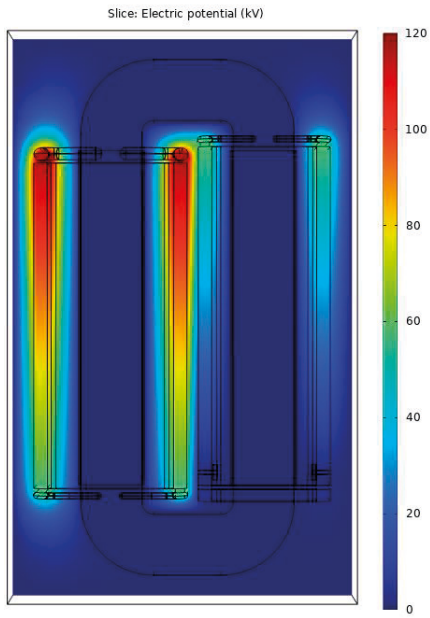



Figure 4.93: Electrostatic simulation of pulse transformer geometry. Electrostatic potential.

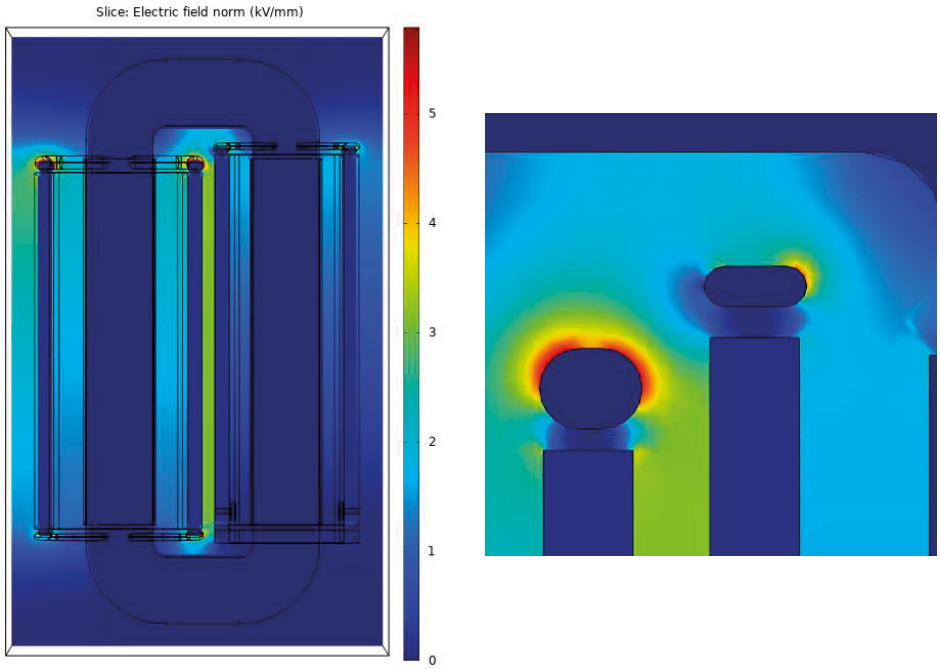



Figure 4.94: Electrostatic simulation of pulse transformer geometry. Electrostatic field strength.

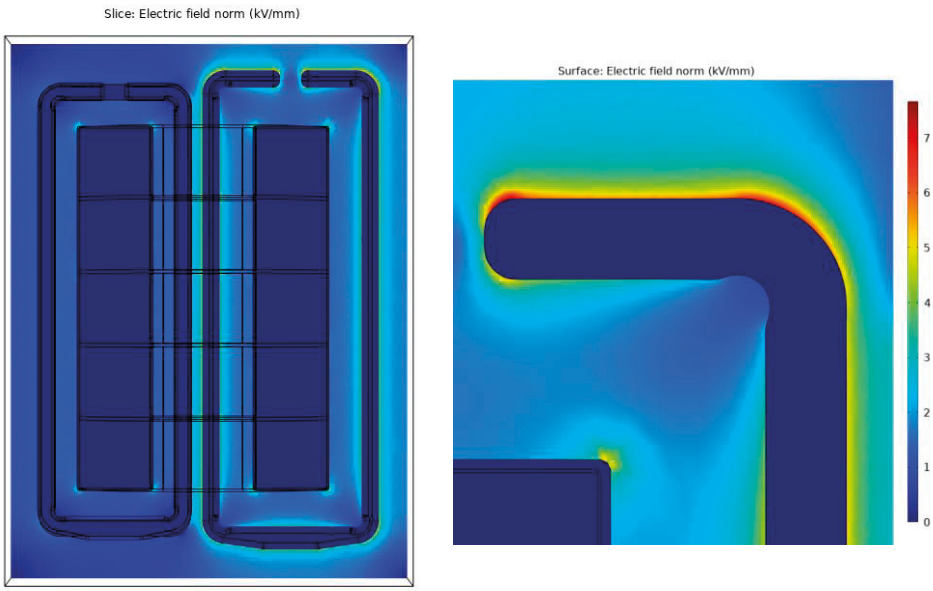



Figure 4.95: Electrostatic simulation of pulse transformer geometry. Electrostatic field strength. Top-down view.

*Passive bias*

Unfortunately, details regarding the passive bias circuit and the associated series inductor were not made available by the manufacturer. Consequently, these components are neglected in this analysis.

*Passive demagnetization circuit*

The commercial modulator employs the passive demagnetization circuit described in section 4.5.2. Here, the capacitor is comprised of two 68 μF capacitors. The resistor is comprised of 16 parallel 2 $k\Omega$ resistors forming an equivalent 125 Ω resistor placed in parallel with an adjustable 24 Ω resistor for tuning. The performance of the passive demagnetization network will be evaluated through circuit simulation in a subsequent section.

*Passive LR bouncer*

As noted, the commercial modulator uses a passive LR bouncer to compensate the output voltage droop. As shown in the simplified schematic of Figure 4.89, the LR bouncer is a parallel LR network placed in series with the primary winding. In this case, the inductor is comprised of four 600 μH inductors placed in parallel whereas the resistor is comprised of seven parallel branches, each branch with four 6 Ω resistors in series. Equivalently, then, $L_b = 150\ \mu H$ and $R_b = 3.42\ \Omega$.

No models have been developed for the LR bouncer in this thesis. For this reason, the performance and characteristics of the LR bouncer will only be assessed through system circuit simulation as described in the following section.

*System simulation*

The components comprising the modulator system have been characterized in the preceding sections. In this section, the developed component models are integrated and simulated in a complete circuit representation.

First, Figure 4.96 shows the klystron load voltage for two complete periods as well as a zoom on a single output pulse and an estimation of the 0-99% pulse rise time. Figure 4.97 shows a zoom over the pulse flat top and the corresponding main capacitor bank voltage. Importantly, in Figure 4.97, a comparison between the system with and without LR bouncer circuit is made. As may be seen, the capacitor bank voltage droop is – with or without bouncer circuit - on the order of 200 V corresponding to only ~3.6% of the nominal capacitor bank voltage. Of course, during the flat top, the main capacitor bank voltage droop is less, approximately 160 V, corresponding to a ~3% flat top voltage droop without bouncer. Use of the LR bouncer increases the pulse rise time but, disappointingly, does not markedly decrease the flat top droop. Here, a flat top droop of around 2.5% is seen.

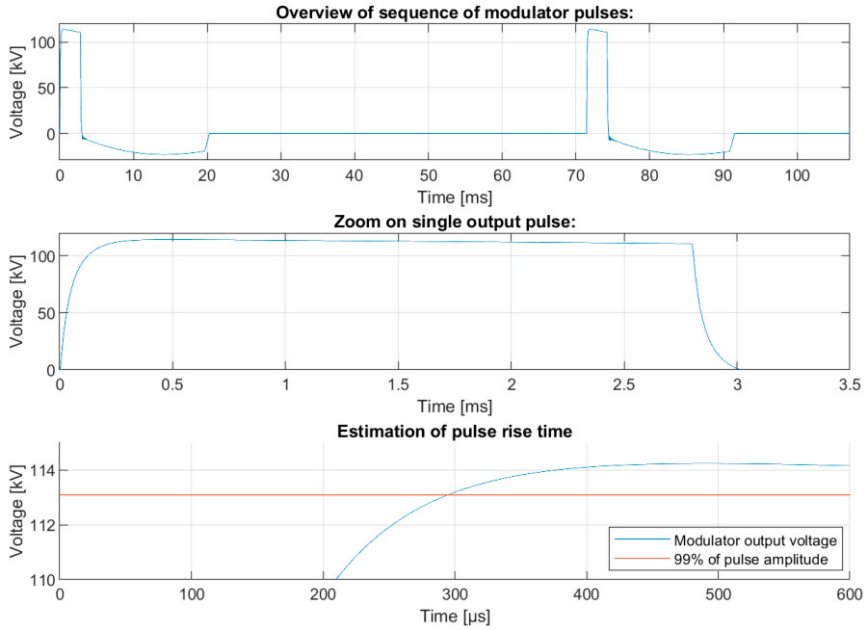



Figure 4.96: Simulated klystron load voltage, a) overview of load voltage waveform for period including two pulse events; b) zoom on single pulse event; c) zoom across pulse rise.

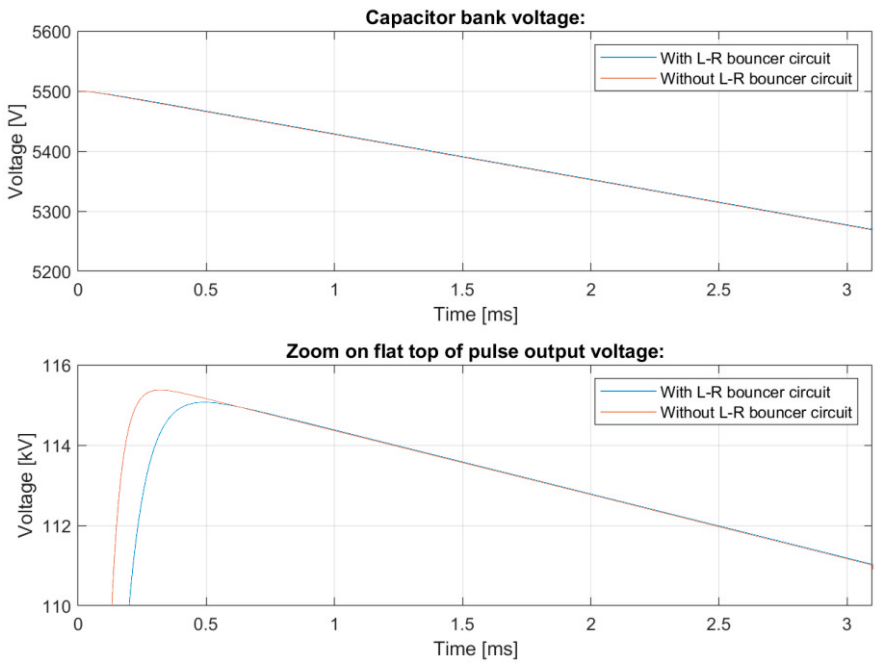



Figure 4.97: Main capacitor bank voltage and zoom on flat top of load voltage waveform with and without LR bouncer circuit.

Then, Figure 4.98 shows the voltage across the LR bouncer during a single pulse event. Of course, this voltage is experienced directly by the bouncer resistor corresponding to bouncer power dissipation. Figure 4.98.b shows the cumulative average power integral over a complete pulse event. As seen, power is dissipated only at the beginning and immediately following the end of the pulse event, in total representing losses on the order of 200 W, or roughly 0.15% of the rated modulator average input power. Note that these 200 W are split among the 28 resistors comprising the bouncer resistor component such that less than 8 W (average power) is dissipated per resistor.

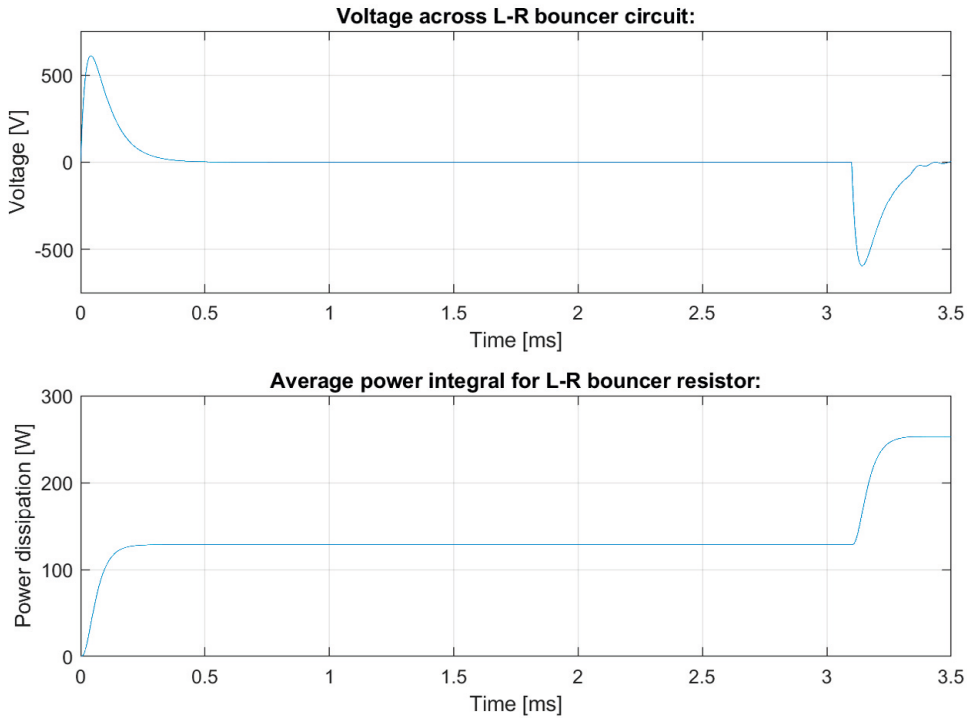



Figure 4.98: Voltage across LR bouncer circuit during pulse event and corresponding average power integral of the LR bouncer resistor

Finally, Figure 4.99 shows the transformer magnetization and demagnetization over a complete pulse period. As may be seen, the transformer is magnetized from -8.5 A to +8.5 A during the pulse event. Hence, the pulse transformer is appropriately biased and fully symmetrical transformer magnetization is achieved.

Following the pulse event, the transformer is demagnetized over a time period of approximately 17 ms, well before (on the order of ~50 ms) the next pulse event. During the demagnetization period, the voltage across the demagnetization network

exceeds ~1 kV, and evaluating the average power integral of the demagnetization network resistor, an average power dissipation of ~2.5 kW is seen. As mentioned, further note that this negative voltage (undershoot) is magnified by the pulse transformer and seen across the klystron load, Figure 4.96, representing a peak voltage of ~20 kV. This is extremely close to the typical maximum rating of klystrons (on the order of ~20%). This issue is discussed further in the following section on demagnetization network design.

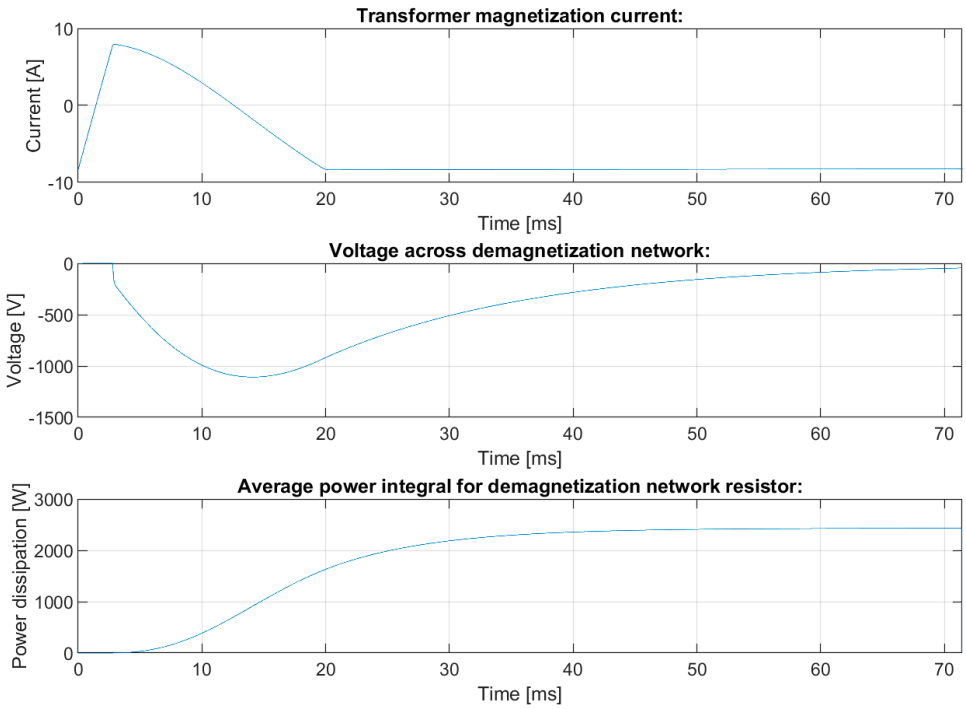



Figure 4.99: Transformer magnetization over a complete pulse event period, a) Transformer magnetization current; b) Voltage waveform across transformer demagnetization network; c) Associated average power integral for demagnetization network resistor

### 4.7.3 System design

In this section, the developed design procedures will be used to generate a complete modulator design for the requirements listed in Table 4.8. In order to represent a fair and direct comparison between systems, the primary voltage has been pre-set to that of 5.5 kV and – to an as great extent as possible – only the same type of components is considered. The main exception here is the bouncer circuit. As was seen in the preceding section, use of an LR bouncer does not quite result in adequate droop

compensation despite use of a very large capacitor bank. Instead, the LC bouncer circuit is considered. For clarity, design of each component is treated individually-

*Pulse transformer*

Given the requirements listed in Table 4.8, the pulse transformer is assumed to be fully biased and with series connected secondary windings. Again, to provide a fair comparison to the commercial pulse transformer, the same or at least similar system constraints, material properties and assumptions are adopted as summarized in Table 4.9.

**Table 4.9: Summary of constraints and material properties for design of pulse transformer according to requirements presented in Table 5.7.X**

| Symbol | Quantity | Value |
|---|---|---|
| | Material constants | |
| $J_{max}$ | Maximum RMS current density | 4 A/mm$^2$ |
| $B_{max}$ | Peak magnetic flux density | 1.55 T |
| $k_f$ | Magnetic fill factor | 90% |
| $\varepsilon_r$ | Relative permittivity of oil | 2.2 |
| | Problem constraints | |
| $\hat{h}_c$ | Maximum pulse transformer height | 0.86 m |
| $\hat{y}_c$ | Maximum magnetic core depth | 0.55 m |

In the following, the optimization procedure given in (4.85) is set up according to Table 4.8 and Table 4.9 for the three winding techniques presented in section 4.2.7. To establish the difference between the resulting pulse transformer designs, the design pulse length is swept from 500 µs to 3.5 ms, with the application pulse length represented at 2.8 ms. The results of this procedure are summarized in Figure 4.100 and are discussed in the following.

The imposed constraint on pulse transformer height implies a direct limitation on the transformer number of turns for a transformer based on the single layer winding technique. Consequently, the magnetic core volume increases steeply and, right after passing the application pulse length, the solver no longer converges to a solution. Setting up the winding with multiple layers allows a greater number of turns for a given winding height, prolonging the effects.

Conversely, in this case the pancake winding technique offers a more compact design because of its ability to add winding turns on top of each other widthwise after reaching the imposed height limitation, thereby constituting an added degree

of freedom for the optimizer. As mentioned, the multiple layer winding technique is not practical at this voltage level but is an interesting theoretical development. Comparing instead the single layer winding technique to the pancake winding technique, a significant difference is seen. Here, at the application pulse length, using the single layer winding technique results in an optimized magnetic core volume more than three times greater than that of the corresponding pancake winding-based transformer.

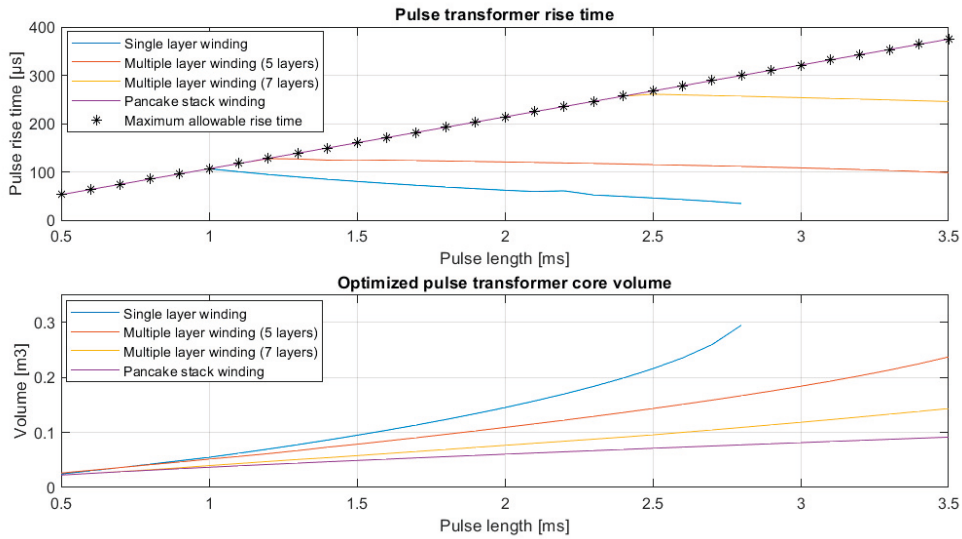



Figure 4.100: Optimization results for pulse transformer unit with the requirements listed in Table 4.8

Based on the above analysis, it is clear that in this case the pancake winding technique is superior. Interestingly, comparing the commercial pulse transformer to the optimized pulse transformer (Figure 4.100, pancake winding technique at the application pulse length of 2.8 ms) in a side-by-side view, Figure 4.101 and Table 4.8, reveals a striking similarity. Interestingly, the optimizer proposes a somewhat smaller magnetic core depth and a somewhat greater number of winding turns per secondary winding. This discrepancy is seen mainly because the commercial pulse transformer has been designed for a somewhat shorter pulse rise time such that when the LR bouncer is added the extended final pulse rise time is 300 µs. This was demonstrated in Figure 4.97, above. However, in this case an LC bouncer operating directly on the pulse flat top is utilized. Hence, the pulse transformer may be designed for a pulse rise time of 300 µs such that additional winding turns and an associated reduction in magnetic core area is permitted.

Table 4.10: Comparison of pulse transformer designs

| Symbol | Quantity | Value | |
|---|---|---|---|
| | | Commercial | Optimized |
| $x_c$ | Magnetic core leg width | 10 cm | 10 cm |
| $y_c$ | Total magnetic core depth | 50 cm | 43.5 cm |
| $N_2$ | Secondary turns per winding | 945 and 990 | 1408 |
| $g_s$ | Stacks per winding | 21 or 22 | 22 |
| $g_l$ | Layers per stack | 45 | 64 |
| $h_w$ | Secondary winding height | 57 cm | 58 cm |

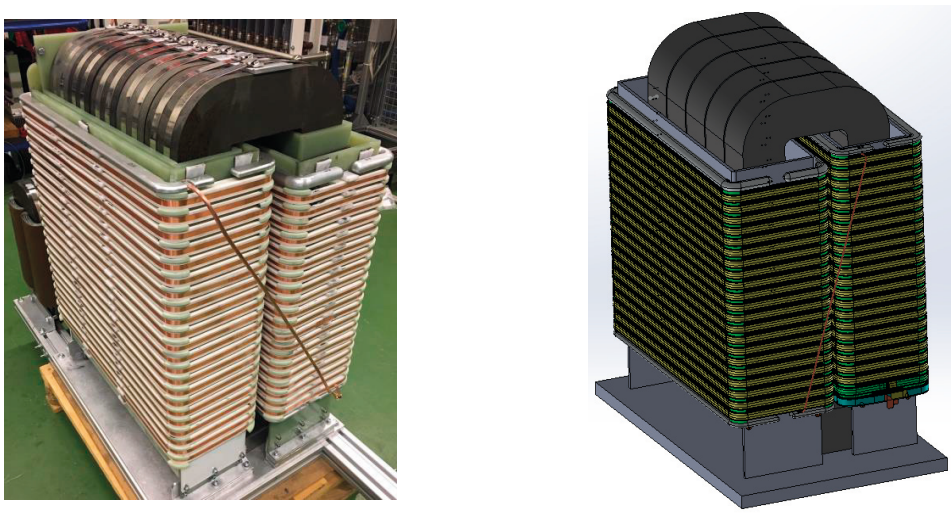


Figure 4.101: Comparison between commercial pulse transformer (after rewinding of secondary windings) and pulse transformer optimized using the proposed design procedure

*Auxiliary circuit*

Again, for comparative purposes, it is of interest to consider use of passive auxiliary circuits. For pulse transformer bias, this implies implementation of a tertiary winding with series inductor as discussed in section 4.5.1. Here, the transformer design summarized in Table 4.10, above, serves as input to the design procedure presented in section 4.5.2. Here, the number of air gaps per inductor core leg was set to 1 and the number of winding layers was swept from 1 to 5. Additionally, given that the pulse transformer core handles at least 1.55 T, the maximum magnetic flux density is swept from the standard value of 1.2 T to 1.55 T. The results obtained from the optimization procedure are shown in the form of a Pareto front in Figure

4.102. As can be seen, allowing the peak magnetic flux density to extend to 1.5 T and implementing the bias inductor using 3-5 winding layers allows a compact and efficient design. Here, the bias inductor can easily be made to be on the order of ~10 times smaller than the pulse transformer and with system demagnetization losses on the order of ~1.7 kW, corresponding to roughly ~1.2-1.3% of the rated system power. This should be considered fully acceptable and use of more complicated solutions (e.g., the active auxiliary circuit) is not advised.

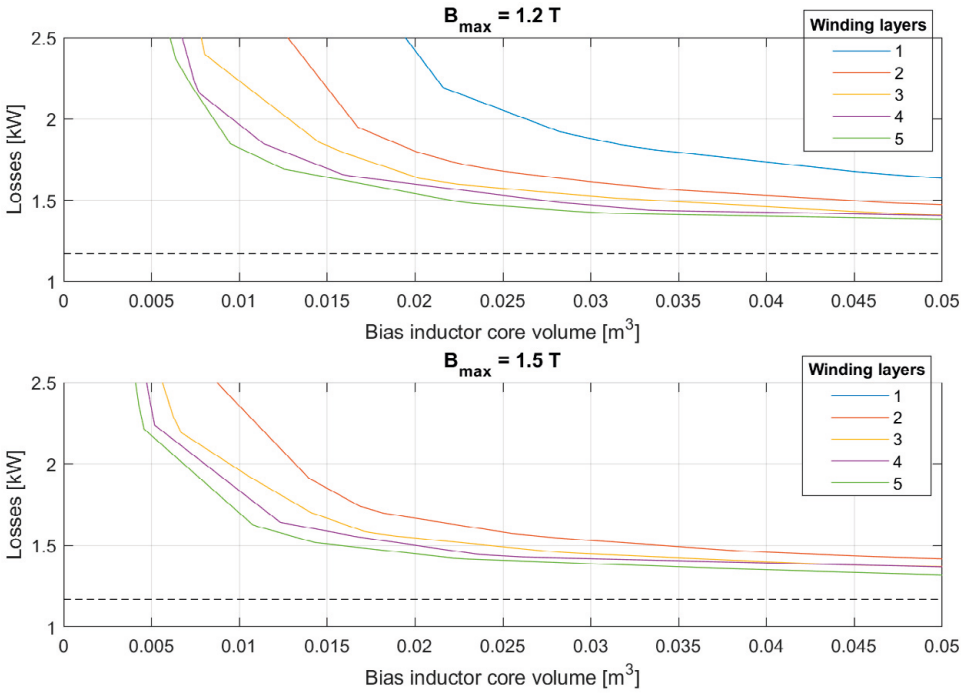



Figure 4.102: Pareto front for passive bias circuit with the requirements listed in Table 4.8

*Transformer demagnetization network*

Passive demagnetization of the pulse transformer magnetic core is accomplished by use of the freewheeling circuit with parallel RC network, section 4.5.2. This type of system was also implemented for the commercial modulator system. There, however, demagnetization was carried out in less than 25% of the time available for demagnetization resulting in a klystron voltage undershoot around 20% of the peak amplitude of the nominal pulse voltage waveform. This is very close to the aforementioned limit of the klystron and should be avoided. In this work, a design margin limit of ~10% is imposed. Setting up the passive demagnetization network design procedure outlined in section 4.5.2 with the above presented transformer and

bias inductor designs and choosing the design with minimal losses yields $C_{dm} = \sim 350\ \mu F$ and $R_{dm} = \sim 14\ \Omega$. Here, the greater $C_{dm}$ (compared to the commercial system) prolongs the demagnetization process thereby reducing the amplitude of the klystron undershoot. The performance of the derived demagnetization network will be assessed through simulation in a subsequent section.

*HV switch assembly*

The HV switch assembly must be designed for a nominal DC voltage of 5.5 kV and the pulsed application load current referred to the primary of ~520 A. Setting the design procedure proposed in section 4.4.2 to minimize total switch losses results in the suggestion to use four series connected 5SHY 50L5500 IGCT switches. The associated static compensation resistor is proposed to be $345\ k\Omega$ per switch, both 1) limiting the worst-case switch voltage to below ~3200 V, i.e., below the maximum permanent DC voltage for 100 FIT failure rate (in this case 3.3 kV), and 2) limiting the power dissipation per resistive element to be below that of 30 W. Finally, the dynamic compensators are evaluated to be $R_s = \sim 200\ \Omega$ and $C_s = \sim 1.55\ \mu F$. Clearly, the HV switch assembly obtained from the proposed design procedure is very similar to that of the commercial klystron modulator system.

*Main capacitor bank and bouncer circuit*

As discussed in section 4.3, the bouncer circuit is to be designed in conjunction with the main capacitor bank to ensure the required flat top droop and ripple requirements are satisfied while minimizing system volume and losses. In this particular case, it is of interest to see if the existing LR bouncer could be converted into an LC bouncer, and if so to evaluate what the associated impact would be on, e.g., system volume and losses. As discussed, the existing LR bouncer in part consists of four 600 µH inductors placed in parallel. Three such inductors may instead be placed in series to form an equivalent 1.8 mH inductor. It is here assumed and it will later be verified that the resulting inductor can withstand the required bouncer current. Imposing this setting and running a reduced version of the design procedure outlined in section 4.3.2 yields the results presented in Figure 4.103 plotting combinations of $C_m$ and $C_b$ which appropriately limit the flat top droop to less than 1%. As may be seen, despite significantly improving flat top droop with respect to the original LR bouncer, it is further possible to reduce the main capacitor bank from 8 x 800 µF to, e.g., 2 x 880 µF (i.e., 1.76 mF) by adding a small ~1.2 mF low voltage bouncer capacitor. Of course, designing the LC bouncer circuit without imposing the bouncer inductance value would result in even greater space and cost savings. The performance of the derived bouncer circuit will be further assessed through simulation in the following.

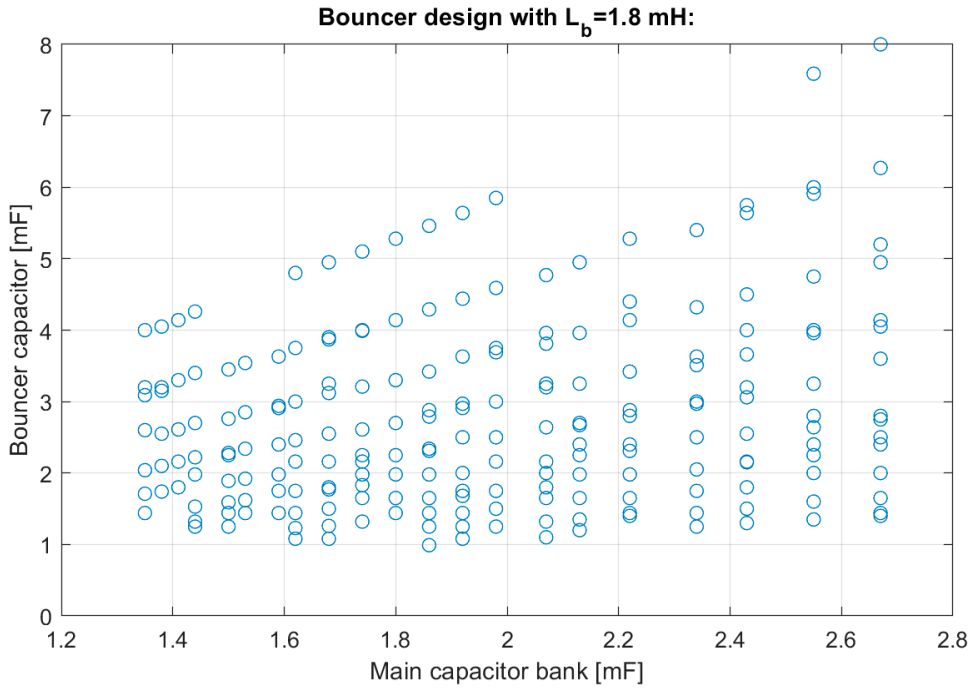



Figure 4.103: Combinations of main capacitor bank and bouncer capacitor values which with a bouncer inductor of 1.8 mH limit the flat top droop to less than 1%.

*Capacitor charger*

The capacitor charger is sized based on the considerations outlined in section 4.6. Here, two 75 kW modules (including control unit) from Poynting are integrated in a single 800x800 cabinet for a total charging capacity of 150 kW. As noted in the preceding section, this is more than sufficient for the requirements presented in Table 4.8. The total charger efficiency is estimated to be between 90-95% depending on operating condition [4.48].

*System simulation*

The components comprising the designed modulator system have been characterized in the preceding sections. In this section, the developed component models are integrated and simulated in a complete circuit representation.

First, Figure 4.104 shows the klystron load voltage for five complete periods as well as a zoom on a single output pulse and an estimation of the 0-99% pulse rise time. Here, the pulse rise time is seen to be ~275 µs, slightly better than the design value. This is mainly because the main capacitor bank voltage has been adjusted somewhat

from 5.5 kV to 5.8 kV to match LC bouncer operation. The increased capacitor bank voltage is easily handled by the HV switch assembly given the conservative design.

Figure 4.105 provides an overview of the LC bouncer operation. As can be seen in Figure 4.105.a, the main capacitor bank droop of ~17.5% is well matched by the LC bouncer output voltage such that the flat top droop is significantly reduced, Figure 4.105.c. Here, a comparison to the original LR bouncer is shown.

Finally, Figure 4.106 shows the transformer magnetization and demagnetization over several pulse periods. As may be seen, the transformer is magnetized from -5 A to +5 A during each pulse event. Hence, the pulse transformer is appropriately biased and symmetrical transformer magnetization is achieved. Following the pulse event, the transformer is demagnetized over a time period of approximately 30 ms. Hence, in comparison with the commercial modulator demagnetization network where the transformer was demagnetized in only 17 ms, the undershoot voltage is here better limited to ~600 V. As noted, this voltage is reflected to the klystron via the pulse transformer, representing ~10% of the nominal pulse amplitude.

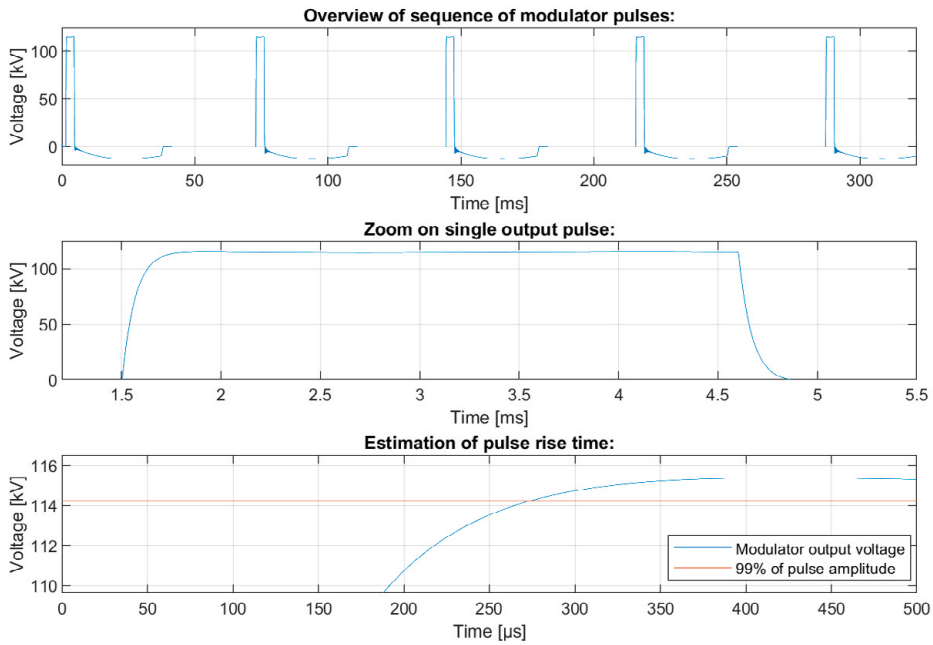



Figure 4.104: Overview of simulation results

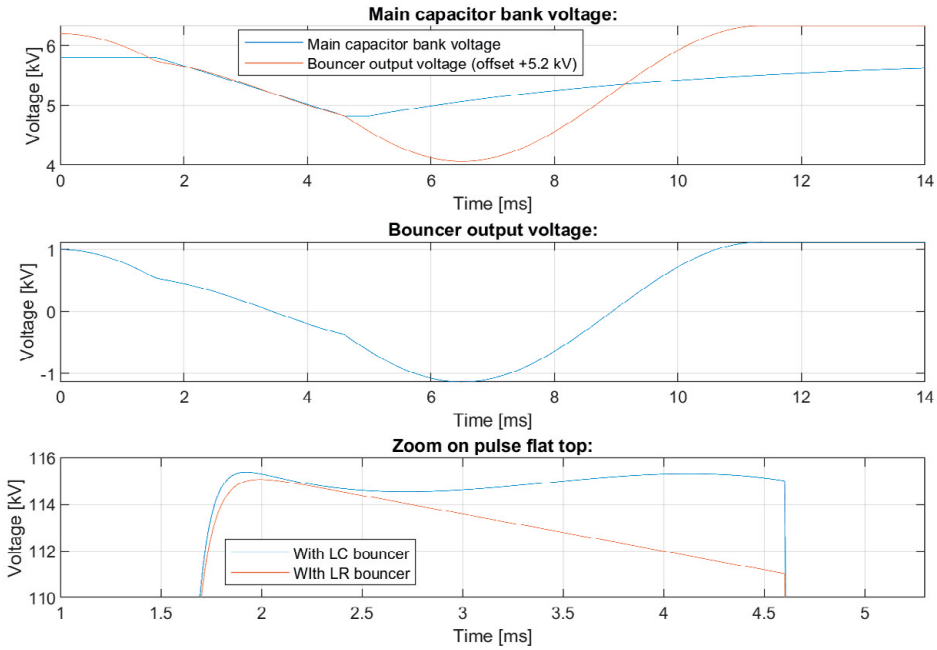



Figure 4.105: Simulation results, bouncer operation

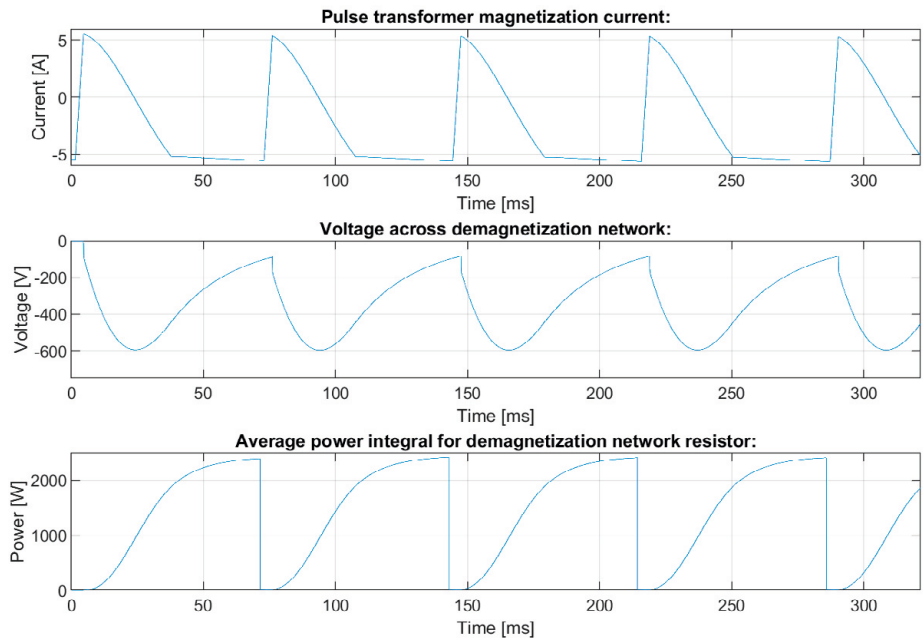



Figure 4.106: Simulation results, pulse transformer magnetization and demagnetization

### 4.7.4 Conclusions

In this section, the developed models have been used to 1) characterize the components of a commercial klystron modulator, and to 2) design an improved modulator system for the same application parameters. In studying the commercial modulator system, the characterization was seen to correspond well to available measurement data. Furthermore, simulation in a finite element analysis tool revealed a good match between analytical calculation, simulation and experimental values. Interestingly, in designing an equivalent modulator system, a majority of the designed modulator components were very similar to those of the commercial modulator system. The differences were noted and discussed. In particular, given the poor performance of the commercial LR bouncer system, the choice was made to adopt instead an LC bouncer system. Here, importantly, pulse flat top performance was significantly improved whereas the main capacitor bank volume was reduced by a factor 4. This study highlights the unsuitability of the LR bouncer in long pulse high power applications.

## 4.8 Case study: long pulse transformer for FAIR pLinac

### 4.8.1 Background

The GSI (Gesellschaft für Schwerionenforschung) Helmholtz Center for Heavy Ion Research is a research laboratory located in Darmstadt, Germany. The research center was founded in 1969 to conduct both fundamental and applied heavy ion physics research. At the time of writing, GSI is being expanded through the construction of the accelerator Facility for Antiproton and Ion Research (FAIR). With focus on research in the areas of particle physics, anti-matter physics and high-density plasma physics, several important experiments are planned. In particular, PANDA is considered a key experiment, utilizing proton-antiproton annihilation to study strong interaction physics. Here, in order to generate the antiproton beam intensity required by the experiment, a dedicated proton LINAC (pLINAC) is being constructed. The pLINAC is to be powered by klystrons, and the associated modulators are to be rated for a nominal pulse power amplitude of 115 kV / 54 A, an effective pulse length of 360 μs, and a pulse repetition rate of up to 5 Hz.

In 2019, the author initiated research collaboration between Lund University and GSI, linked to the klystron modulator development at FAIR. Core project deliverables included 1) global optimization study of high voltage pulse transformer and required auxiliary systems accounting for the pre-existing modulator primary stage, 2) complete electromagnetic high voltage pulse transformer design, 3) production of a full-scale prototype device (contracted to industrial partner), and 4) experimental verification of the developed prototype device. This section describes

the application of the models proposed in this chapter to the case of the FAIR klystron modulators. The developed full scale prototype device is presented along with experimental results in validating the suggested design procedure.

### 4.8.2 Project scope

An overview of the typical pulse transformer-based modulator was shown in Figure 2.12. The basic requirements of the FAIR klystron modulators were noted in the preceding section. Importantly, the majority of the components of the required klystron modulator – including the capacitor charger, the capacitor bank and the high voltage switch assembly – had already been selected and procured or developed. Furthermore, it was desirable to avoid the use of a controllable bouncer circuit. Hence, project work was focused mainly on the development of the high voltage pulse transformer and directly related auxiliary circuits. Minor changes to the above noted components were possible if such would prove advantageous to pulse transformer design or modulator operation:

- The modulator primary side voltage had been pre-defined to 3.6 kV but could be shifted somewhat within the limits prescribed by the other components. Practically, an increase to the primary side voltage is limited by the maximum switch voltage whereas a decrease is limited by the maximum switch current.
- The nominal capacitance of the main capacitor bank is 5.4 mF. However, the main capacitor bank is modular and could be increased in discrete steps to either $1.25C_m$ or $1.50C_m$.

### 4.8.3 Study of application

Given the size of the main capacitor bank, regardless of if additional capacitance is added according to the above or not, it is clear that some form of compensating circuit must be added to obtain the required usable pulse length. With the desire to avoid use of controllable bouncer systems, it was decided to add a series inductor to extend the pulse length. At the same time, however, though the required rated usable pulse length is 360 µs, the more probable application pulse length is on the order of only 200 µs. For this reason, it was desirable to find a solution which could operate adequately both with ($T_p \geq 360\ \mu s$; in case the full pulse length would be needed) and without ($200\ \mu s \geq T_p \geq 360\ \mu s$; for improved efficiency in the more probable case) the series inductor. In considering this possibility, it is clear that the developed pulse transformer should have a reasonable pulse profile in both operating conditions. Hence, the pulse transformer must be designed such that the pulse rise

time without series inductor is appropriate. Imposing a too short rise time unnecessarily limits the number of transformer turns and thereby leads to a larger transformer. Furthermore, it would be considerably more difficult to reach the required pulse length in accordance with the above discussion. On the other hand, too long rise time corresponds to an unreasonable pulse shape (rise time not in proportion to pulse flat top). Given this trade-off, a target rise time of 50 µs was set.

To choose the values of the primary side voltage, the capacitance of the main capacitor bank and the series inductor, the complete system was studied by setting up a state-space model, (4.220). Here, $L_s'$ is the pulse transformer leakage inductance referred to the primary, $R_k'$ is the equivalent klystron resistance referred to the primary, $C_d'$ is the equivalent pulse transformer stray capacitance referred to the primary, $L_{ser}$ is the added series inductance, $v_{Cm}$ is the capacitor bank voltage, $i_{Ls}{}'$ is the current through the leakage inductance referred to the primary (i.e., equivalent to the current through the series inductance), and $v_{Cd}{}'$ is the voltage across the transformer stray capacitance (i.e., equivalent to the transformer output voltage) referred to the primary. For each combination of $C_m$ and $L_{ser}$, the capacitor bank voltage was set to some low voltage $V_{Cm,0}$ and progressively increased until the required pulse output amplitude was reached. Then, the usable flat top width was derived directly from the calculated waveform according to the above definition. Figure 4.107 shows the results, plotting the resulting usable flat top length as a function of the added series inductance with the capacitance $C_m$ and the transformer turns ratio as parameters.

$$\begin{pmatrix} \dot{v_{Cm}} \\ \dot{\imath_{Ls}}{}' \\ \dot{v_{Cd}}{}' \end{pmatrix} = \begin{pmatrix} 0 & -1/C_m & 0 \\ 1/(L_s' + L_{ser}) & 0 & -1/(L_s' + L_{ser}) \\ 0 & 1/C_d' & -1/(R_k' C_d') \end{pmatrix} \begin{pmatrix} v_{Cm} \\ i_{Ls}{}' \\ v_{Cd}{}' \end{pmatrix} \qquad (4.220)$$

Here, the following observations were made:

- Without series inductor, use of the pre-defined capacitor bank (i.e., $C_m = 5.44\ mF$) yields the minimum usable pulse length of 200 µs only for pulse transformer turns ratios of 29 and below. However, this corresponds to an ideal capacitor bank voltage of ~4 kV beyond, less than 10% away from the switch assembly maximum rating. Furthermore, the required series inductance required to obtain a usable flat top of 360 µs is very large, on the order of 200 µH.
- Space for additional capacitor bank units had been foreseen and the required capacitors had already been procured. Adding capacitor units such that $C_m = 1.50 C_{m,0}$, above, allows minimization of the series inductance. In this case, according to Figure 4.107, $L_{ser} = 80 \ldots 100\ \mu H$.

- Choosing a pulse transformer turns ratio of 30.5 provides a margin of 15% to the switch maximum voltage limit while minimizing the switch current to 1650 A.
- System operation under these conditions requires a primary side voltage of 3.75 kV.

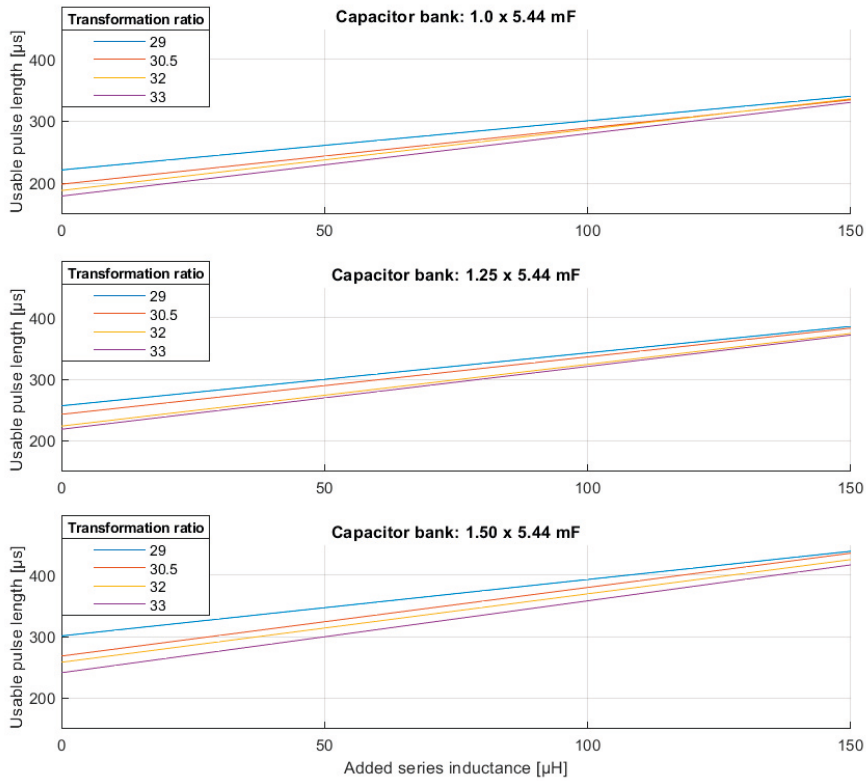



Figure 4.107: Study of usable pulse flat top length as function of added series inductance and with pulse transformer turns ratio and the capacitance of the main capacitor bank as parameters. The presented curves have been fitted (R-square > 90%).

In summary, the outcome of the application pre-study was 1) to install additional capacitor bank modules to increase $C_m$ by a factor 1.5; 2) to change the primary side voltage from 3.6 kV to 3.75 kV; 3) to choose a pulse transformer with series connected secondary windings and utilize a passive bias circuit, and should be designed for the transformer turns ratio 30.5 with a pulse rise time constraint of 70 µs; and 4) if needed, to add a series inductor of around 90 µH to extend the pulse length to the rated 360 µs. The design of the series inductor was not part of the agreement.

### 4.8.4 System design

In this project, the two components to be designed – the pulse transformer and the bias inductor - were considered individual design problems and are set up and treated in the two following sections.

*Pulse transformer optimization*

The pulse transformer has series connected secondary windings and is to be designed considering use of a bias circuit. In accordance with the discussion presented in section 4.2, the secondary windings are to be parallel to the primary winding and the magnetic core and are to be based on the single layer winding technique. The pulse transformer design problem is summarized in Table 4.11.

**Table 4.11: Summary of constraints and material properties for design of pulse transformer according to requirements presented in Table 4.8**

| Symbol | Quantity | Value |
|---|---|---|
| | Material constants | |
| $J_{max}$ | Maximum RMS current density | 2 A/mm$^2$ |
| $B_{max}$ | Peak magnetic flux density | 1.2 T |
| $k_f$ | Magnetic fill factor | 90% |
| $\varepsilon_r$ | Relative permittivity of oil | 2.2 |
| | Problem constraints | |
| $\hat{h}_c$ | Maximum pulse transformer height | 0.8 m |
| $\hat{y}_c$ | Maximum magnetic core depth | 0.4 m |

As may be understood from the above discussion, pulse transformer efficiency was not prioritized other than in ensuring the requisite pulse length. Hence, the problem was set-up in accordance with that of (4.85) and resulted in the design summarized in Table 4.12 and shown in overview in Figure 4.108-

Table 4.12: Overview of generated pulse transformer design

| Symbol | Quantity | Value |
|---|---|---|
| $x_c$ | Magnetic core leg width | 7.5 cm |
| $y_c$ | Total magnetic core depth | 37.5 cm |
| - | Number of magnetic cores | 5 |
| - | Secondary winding type | Single layer |
| $N_2$ | Secondary turns per winding | 428 |
| $h_w$ | Secondary winding height | 47 cm |
| - | Primary winding type | Single layer (parallel) |
| $N_p$ | Primary turns per winding | 28 |
| - | Primary winding height | 47 cm |

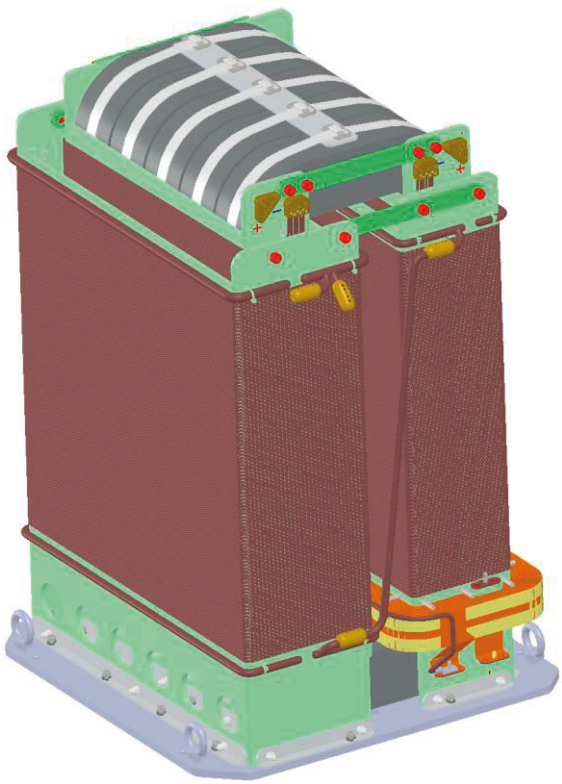


Figure 4.108: Overview of the generated pulse transformer design

*Bias inductor optimization*

The bias inductor is of the type discussed in section 4.5. The design assumptions used for the pulse transformer unit and summarized in Table 4.11 were also used for the bias inductor. Furthermore, for economic reasons, it was also desirable to use the same magnetic strip as that used to construct the pulse transformer magnetic cores. Here, it was important to limit the bias inductor voltage drop below 20 V to be compliant with the existing bias power supply unit. Hence, the problem was set-up in accordance with that developed in section 4.5.2. and resulted in the design summarized in Table 4.13 and shown in overview in Figure 4.109-

**Table 4.13: Overview of generated bias inductor design**

| Symbol | Quantity | Value |
|---|---|---|
| $x_c$ | Magnetic core leg width | 7.5 cm |
| $y_c$ | Total magnetic core depth | 14 cm |
| - | Number of magnetic cores | 2 |
| - | Winding type | Multiple layer |
| $N_2$ | Turns per winding | 63 |
| $N_l$ | Winding layers | 8 |
| $h_w$ | Winding height | 47 cm |
| $g$ | Air gap length | 5 mm |
| $k_g$ | Number of air gaps per leg | 2 |

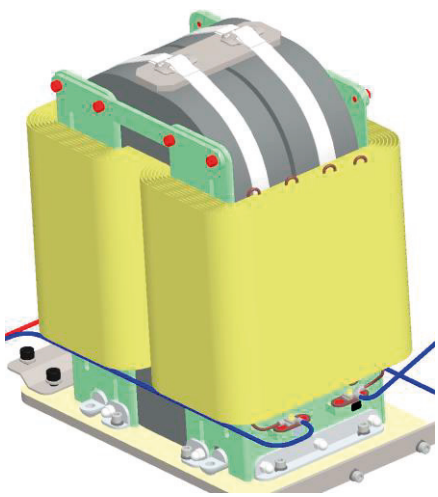


Figure 4.109: Overview of the generated tertiary winding bias inductor design

### 4.8.5 Simulation results

Before production, the designed components were validated in simulation both individually using primarily finite element analysis and collectively through comprehensive 3D finite element and circuit simulations.

*Finite element analysis: pulse transformer*

Both magnetostatic and electrostatic 3D finite element analysis was carried out on the developed pulse transformer geometry. Three magnetostatic simulation cases are considered. First, the pulse transformer is excited from the tertiary winding with a current $I_3 = 10\ A$ according to the above. A two-dimensional slice (front view, through the middle of the pulse transformer) of the simulated field under these conditions is shown in Figure 4.110. As can be seen, the magnetic flux density is simulated to be on the order of 1.2 T in the core straight sections. This result importantly confirms that the intended tertiary winding current appropriately biases the magnetic core. Note also that the magnetic flux density is quite high in the corners of the magnetic core, exceeding 2.5 T. This, however, is due to the assumption of a linear core material. In practice, when part of the material approaches the material saturation point, the local permeability is reduced thereby equalizing the field over the width of the core leg.

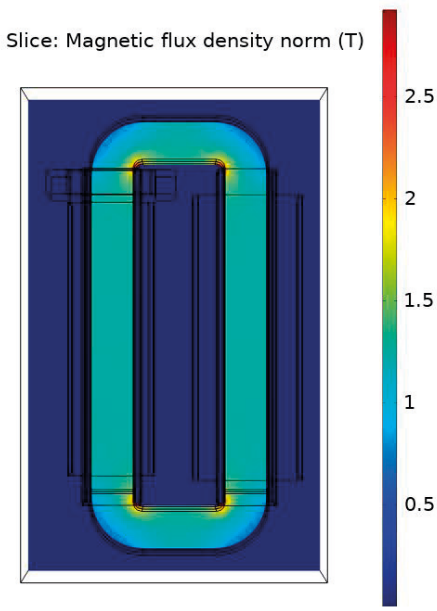



Figure 4.110: Simulated magnetic field distribution of the developed pulse transformer geometry. In this figure, the pulse transformer is excited from the tertiary winding.

Secondly, the pulse transformer is additionally excited from the primary winding. With the magnetization inductance estimated according to (4.49), the corresponding estimate of the magnetization current at the end of the pulse event is given by (4.221). Thus, the transformer is excited both from the tertiary according to the above as well as from the primary with the current according to (4.221). Importantly, here the current given by (4.221) is split between the two primary windings as they are connected in parallel. The results of this field simulation are shown in Figure 4.111.

$$V_{L,m} = V_p = L_m \frac{\Delta i_m}{T_p} \rightarrow \Delta i_m = \frac{V_p T_p}{L_m} \tag{4.221}$$

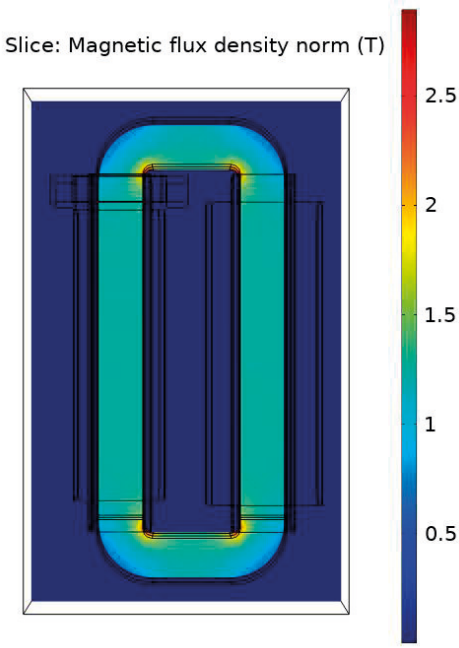



Figure 4.111: Simulated magnetic field distribution of the developed pulse transformer geometry. In this figure, the pulse transformer is excited from both the primary and the tertiary windings.

Note the essentially identical result as compared to Figure 4.110. Of course, this is due to the fact that the tertiary winding current was set according to $I_3 = \Delta i_m/2$. Hence, provided that the relative permeability of the core material is accurately represented, these simulation results validate the analytical calculation of the magnetization inductance and furthermore demonstrate that the magnetic core has been appropriately sized in limiting the peak magnetic flux density to 1.25 T.

Finally, the pulse transformer is excited according to peak load conditions, i.e., with $I_2 = 54\ A$ and $I_1 = nI_2 = 1650\ A$. It is again noted that $I_1$ is to be divided between the two primary windings. Clearly, this setting neglects the additional current due to pulse transformer magnetization, i.e., $2N_2I_2 = 2N_1(I_1/2)$, and thereby provides an estimate of the leakage field. The result of this field simulation is shown in Figure 4.112. Expectedly, according to the simplifications in proposing the models described in section 4.2.4, the field is essentially confined to the space between the primary and the secondary windings. From this, the equivalent leakage inductance referred to the secondary is estimated by (4.48) to be 31.5 mH. Comparing this result to that calculated using the analytical methods developed in section 4.2.4 reveals a match within 5%. Here, $p_m$ is the magnetic energy density.

$$W_m \sim \frac{1}{2} L_s I_2^2 \rightarrow L_s = \frac{2W_m}{I_2^2} = \frac{2}{I_2^2} \int p_m \, dV \tag{4.222}$$

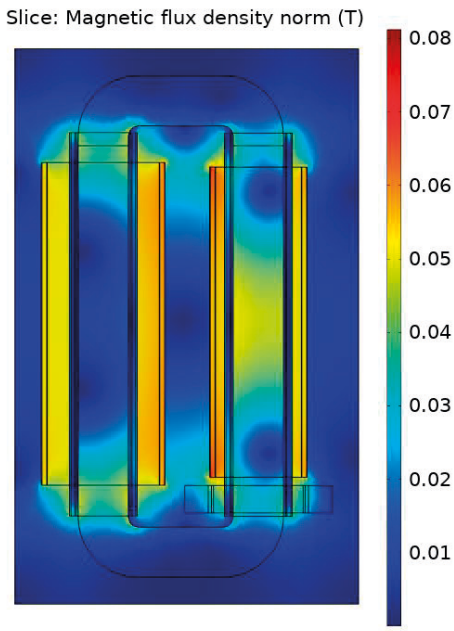



Figure 4.112: Simulated magnetic field distribution of the developed pulse transformer geometry. In this figure, the pulse transformer is simultaneously excited from all windings. Neglecting transformer magnetization, the core flux is largely cancelled permitting study of the transformer leakage field.

Then, an electrostatic finite element simulation was carried out to study the electric field strength. The electric potential is applied in accordance with that described in section 4.2.3 and as shown in Figure 4.113. Here, the voltage on the windings

increases from 0 to $V_s/2$ and from $V_s/2$ to $V_s$. The corresponding electrostatic field strength is shown in Figure 4.114 and Figure 4.115-

Figure 4.114 shows the electrostatic field strength in the front-plane placed through the middle of the pulse transformer geometry. Here, the peak electrostatic field strength is – as expected - seen close to the anti-corona ring and is limited to below 9 kV/mm. Note also that the electrostatic field strength is limited to around 3 kV/mm in the transformer bulk volume.

Figure 4.115 similarly shows the electrostatic field strength in the top-plane placed through a) the center of the top anti-corona ring, and b) the center of the pulse transformer geometry. Again, the peak electrostatic field strength on the anti-corona ring is limited to below 9 kV/mm. In the center of the pulse transformer geometry, the peak electrostatic field strength is seen in the corners of the magnetic core. Here, however, the field is only ~5 kV/mm.

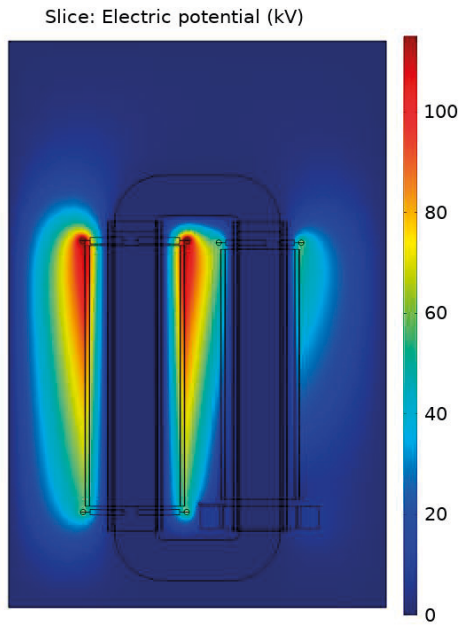



Figure 4.113: Simulated electrostatic potential of developed pulse transformer geometry.

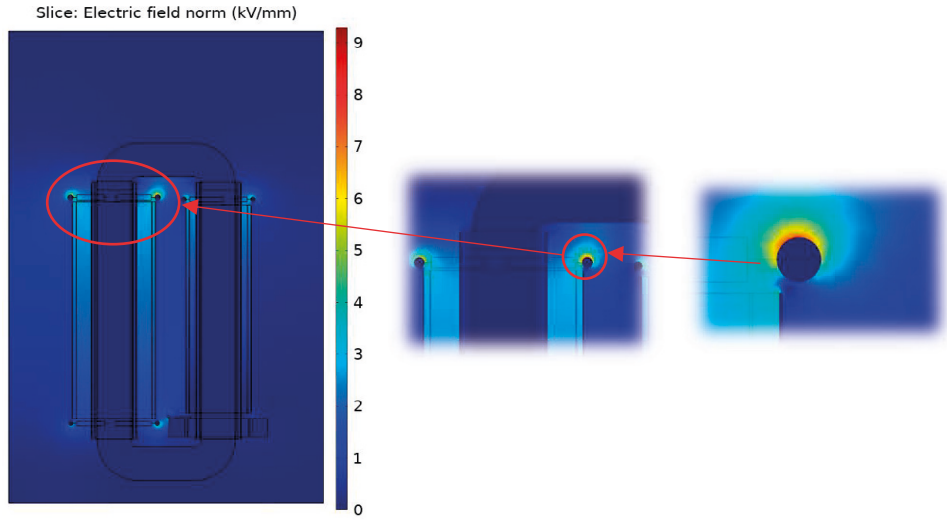



Figure 4.114: Simulated electrostatic field strength distribution of developed pulse transformer geometry- a) front plane, overview; b) front plane, zoom on top of high voltage winding; c) front plane, zoom on cross section of anti-corona ring, indicating the peak electrostatic field strength of the geometry.

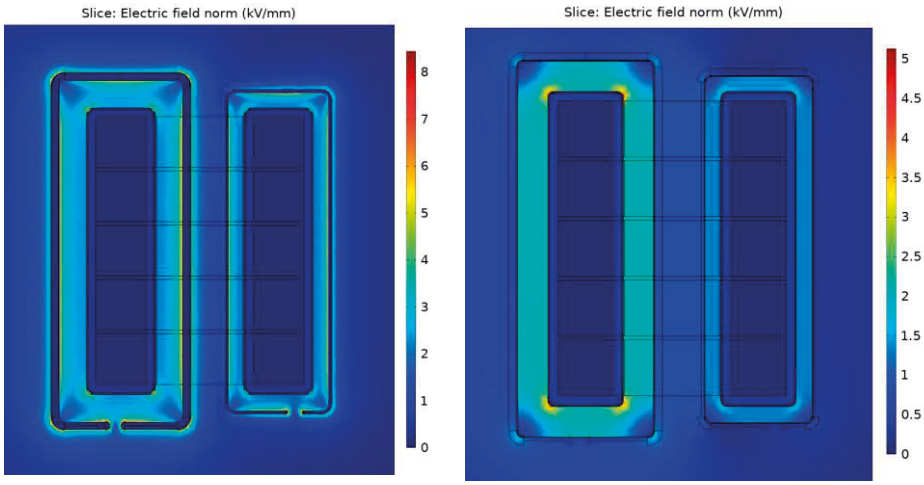



Figure 4.115: Simulated electrostatic field strength distribution of developed pulse transformer geometry- a) top plane, aligned with the center of the anti-corona rings; b) top plane, through the middle of the pulse transformer geometry.

Finally, the stray capacitance may be estimated through integration of the electric energy density, (4.223). From this, the equivalent stray capacitance referred to the secondary is estimated to ~550 pF. Comparing this result to that calculated using the analytical methods developed in section 4.2.3 reveals a match within 5%.

$$W_e \sim \frac{1}{2} C_d V_s^2 \rightarrow C_d = \frac{2W_e}{V_s^2} = \frac{2}{V_s^2} \int p_e \, dV \tag{4.223}$$

*Finite element analysis: bias inductor*

Magnetostatic 3D finite element analysis was carried out on the developed bias inductor geometry. Here, the current $I_3(1+p)$ is imposed on both inductor windings to ensure that the magnetic peak flux density at the highest current does not exceed that of 1.25 T. Furthermore, the analytically estimated inductance value should be compared to that obtained through simulation. Simulation results under these conditions are shown in Figure 4.116. As can be seen, the current in the straight section is limited to 1.25 T. Note that the peak magnetic flux density of, e.g., the corners of the magnetic core is quite high, exceeding that of 2.5 T. Again, as was explained in section 4.7, this is due to the assumption of a linear core material. In practice, when part of the material approaches the material saturation point, the local permeability is reduced thereby equalizing the field over the width of the core leg. The inductance value is simulated using the same technique as described for the pulse transformer. From this, the inductance of the tertiary bias inductor is estimated to be ~0.86 H. Comparing this result to that calculated using the analytical methods developed in section 4.5.2 reveals a match within 5%.

$$L_3 = \frac{2W_m}{\left(I_3(1+p)\right)^2} = \frac{2}{\left(I_3(1+p)\right)^2} \int p_m \, dV \tag{4.224}$$

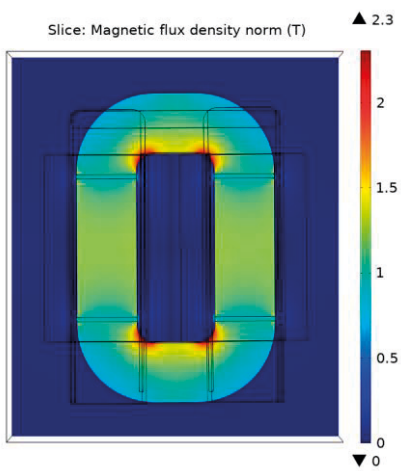



Figure 4.116: Magnetostatic simulation of developed bias inductor geometry

*Complete circuit simulation*

Finally, it is of interest to simulate a circuit representation of the complete system to ensure the function of the modulator. Here, a circuit including mainly the main capacitor bank, the switch assembly, the series inductor, the pulse transformer, the tertiary circuit and the demagnetization circuit was implemented. In addition, more simplified models for the capacitor charger and the bias power supply were included for the sake of completeness. In this circuit model, the circuit parameter values derived from above finite element models are used. Figure 4.117 and Figure 4.118 show the simulated pulse output voltage both with and without the series inductor. As can be seen, without the series inductor the desired 50 µs 0-99% pulse rise time is closely approximated. Furthermore, it can be seen that the usable flat top width is on the order of 250-260 µs in accordance with the prediction presented in Figure 4.107. Then, adding a 90 µ$H$ series inductor significantly prolongs both the pulse rise time and the usable flat top width. Here, the 0-99% rise time is on the order of 200 µs whereas the usable flat top width just exceeds 360 µs. These simulation results demonstrate the feasibility of the proposed solution.

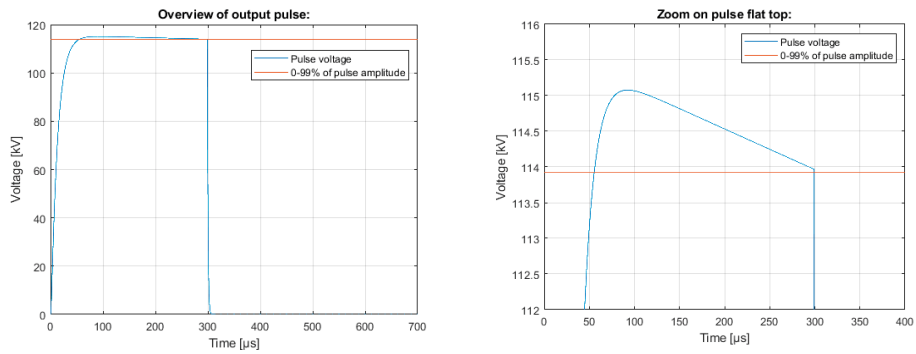



Figure 4.117: Simulated pulse output voltage of developed modulator without series inductor. The pulse rise time is verified to be ~52 µs and the usable pulse length is verified to be ~250 µs, satisfying design requirements.

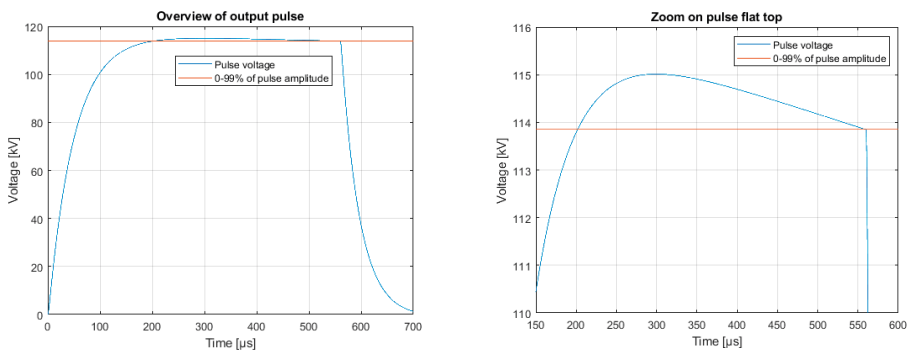



Figure 4.118: Simulated pulse output voltage of developed modulator with series inductor. The series inductor prolongs the pulse event. The resulting pulse rise time is now ~200 µs and the usable pulse length is verified to be 360 µs, satisfying design requirements.

Finally, Figure 4.119 shows the simulated tertiary winding current and the corresponding pulse transformer magnetization current for the system using the series inductor. Here, pulsing begins after 2.5 s. Prior to pulsing, the 20 V bias power supply brings the tertiary winding current to the intended bias point of ~10 A. Correspondingly, the pulse transformer magnetization current seen from the primary side expectedly approaches -20 A. Then, as pulsing begins, the magnetization current is brought from approximately -20 A to +20 A whereas the tertiary winding current is brought from approximately +10 A to +15 A, corresponding well to the imposed $p$. The existing demagnetization network is seen to appropriately demagnetize both the pulse transformer as well as the bias inductor before the following pulse event. Steady state operation is seen after a few pulses. Again, the presented simulation results are in agreement the design models.

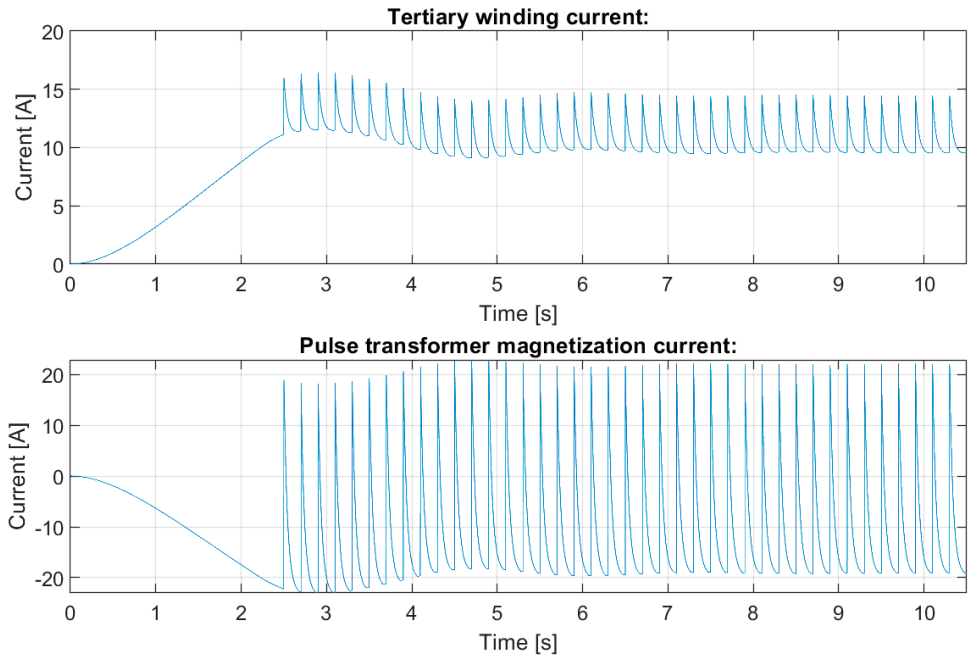



Figure 4.119: Simulated tertiary winding current and associated estimated magnetization current seen from pulse transformer primary. The tertiary winding is powered by a 20 V constant voltage source slowly bringing the tertiary winding current and, correspondingly, the transformer magnetization current to the identified bias point. At $t = 2.5\,s$, pulsing begins and a symmetrical steady state magnetization current swing (and thus magnetic flux swing) is seen.

## 4.8.6 Experimental results

The developed assembly is currently being tested at FAIR, but – unfortunately – final results are not available at the time of writing. Instead, this chapter presents experimental results obtained as part of the Factory Acceptance Test (FAT) prior to

delivery to FAIR. The FAT protocol comprised the following check and tests of the developed components and assemblies:

- Visual inspection
- Voltage withstand testing (hipot test + dynamic voltage withstand test)
- LCR meter measurements (derivation of equivalent circuit parameters)
- Power choke testing (accurate inductance measurements)

The following text is focused primarily on describing the experiments used in 1) verifying the calculated and simulated equivalent circuit parameters through measurement, 2) evaluating preliminary pulse performance, and 3) ensuring voltage withstand capability.

*Pulse transformer: overview*

The developed pulse transformer component is shown in Figure 4.120. The transformer differs slightly from that summarized in Table 4.12 in two ways. First, instead of having two secondary windings with 428 turns each, the larger leg has 435 turns whereas the smaller leg has 421 turns. Still, note that the total number of secondary winding turns is retained. Furthermore, since the deviation from the original number of turns per secondary winding is comparatively small, the impact on (particularly) the leakage inductance parameter should be negligible. Second, the primary winding turns are implemented using five parallel wires ‘wound as one’. This is simply a practical matter, permitting use of a copper wire with smaller diameter in simplifying the manufacture of the transformer.

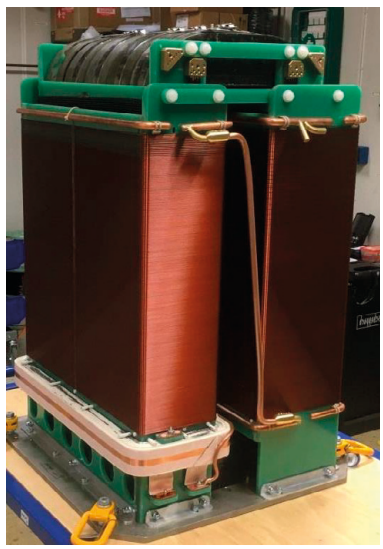


Figure 4.120: Developed high-voltage pulse transformer component with tertiary winding

*Pulse transformer: measurement of winding resistance (LCR meter)*

The main purpose of the LCR-meter measurements is to verify the estimations of the winding resistances. Note that, since the LCR-meter operates at comparatively low voltage, it is preferable to assess the inductance parameters using a dedicated power inductor measurement instrument (see following subsection). All LCR-meter measurements were carried out using the E4980AL instrument from Keysight. Here, the total equivalent resistance of the primary, secondary and tertiary windings was measured by setting the LCR-meter for series LR circuit measurement and using the configurations schematically represented in Figure 4.121.

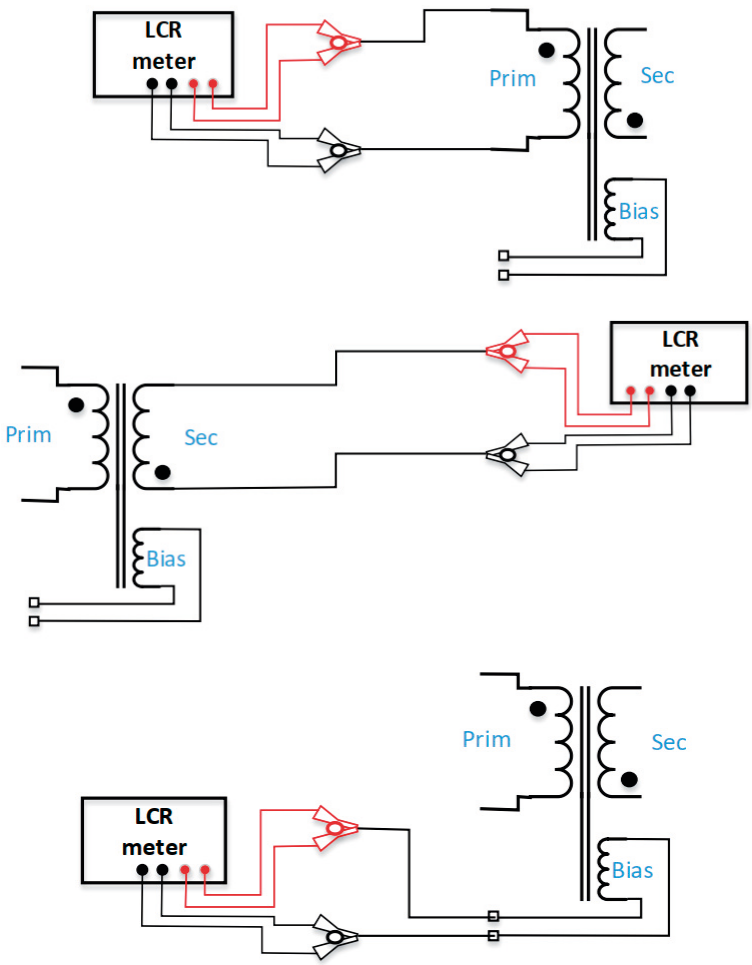



Figure 4.121: LCR-meter configurations for winding resistance measurement: a) primary windings, b) secondary windings, c) tertiary winding

Under these conditions, the total primary winding resistance was measured to be 5.7 mΩ, the total secondary winding resistance was measured to be 26.3 Ω, and the total tertiary winding resistance was measured to be 0.17 Ω. This is compared to the analytical estimates obtained by applying the methods described in section 4.2.8 to the developed design. Here, the corresponding expected values are 5.9 mΩ, 20.3 Ω and 0.16 Ω. The error between the analytical and measured values for the primary and tertiary winding are on the order of 5% and are attributed to the accuracy of the estimation model as well as possible differences in the assumed resistivity (e.g., due to temperature differences) of the material. On the other hand, the measured total secondary winding resistance is close to 30% greater than that of the predicted value. Still, the measured secondary winding resistance value is only ~1% of the equivalent klystron resistance, and is largely negligible.

*Pulse transformer: measurement of inductance (choke tester)*

The inductance parameters of the pulse transformer as well as the tertiary winding series inductor were measured using the power choke tester DPG10-1000B from ed-k GmbH, [4.50]. To measure the pulse transformer leakage inductance, the power choke tester was connected to the pulse transformer as shown in Figure 4.122.

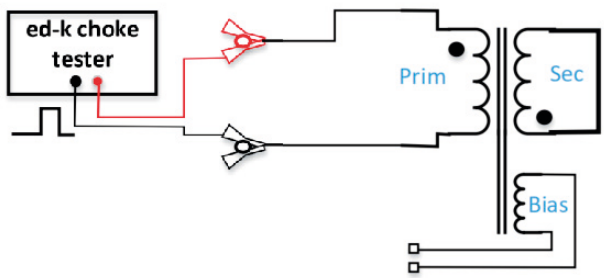



Figure 4.122: Power choke tester configuration for measurement of pulse transformer leakage inductance

Unfortunately, likely due to measurement noise (see Figure 4.123 and Figure 4.124, below), the associated power choke tester software was unable to output the inductance parameters (and the measured waveforms). Instead, while operating the configuration of Figure 4.122 as intended, an external oscilloscope was connected to measure the resulting primary voltage and primary current, i.e., the same information used by the power choke tester to estimate the inductance parameters. The resulting waveforms are shown in Figure 4.123.

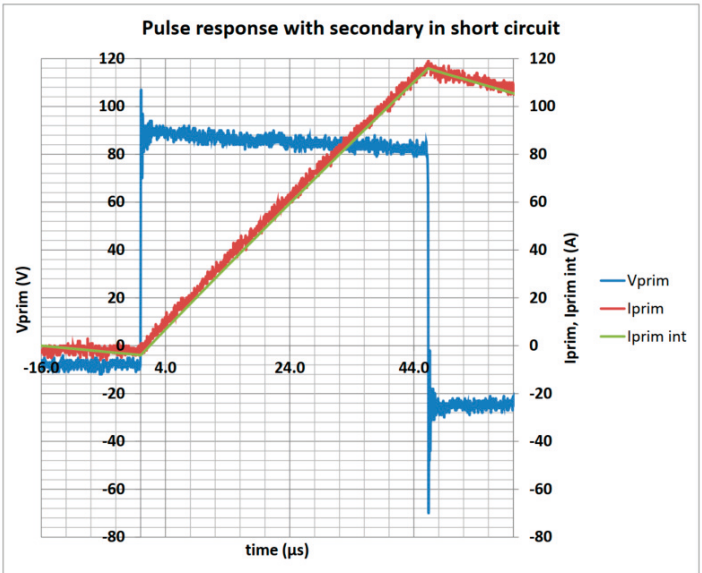



Figure 4.123: Measurement of leakage inductance of pulse transformer component

From these waveforms, the leakage inductance referred to the primary may be estimated from:

$$v_L = L\frac{di}{dt} \rightarrow L'_s \approx \frac{\bar{V}_{prim}\Delta t}{\Delta I_{prim}} \approx \frac{85 \cdot 47 \cdot 10^{-6}}{118} = 33.9\ \mu H \tag{4.225}$$

Then, the leakage inductance referred to the secondary is directly given through the transformation ratio of the pulse transformer component:

$$L_s = L'_s\left(\frac{N_{2,a} + N_{2,b}}{N_1}\right)^2 = 31.6\ mH \tag{4.226}$$

Note that this value is within 1% of the value (31.5 mH) obtained through 3D finite element analysis, (4.222).

The magnetization inductance was then obtained in a similar manner, again using the power choke tester and external oscilloscope for waveform acquisition, Figure 4.124. Here, the tertiary winding was supplied with 10 A to negatively bias the pulse transformer core prior to the measurement. As may be seen, the jump in the primary

current close to $t = 0.004\ s$ indicates that the transformer has been saturated. As mentioned, bias circuit design was carried out assuming a low relative permeability, e.g., ~3000. In this case, the actual relative permeability is significantly higher such that the pulse transformer requires significantly less bias current to reach the intended bias point. This is verified by estimating the magnetizing inductance from the linear portion of the associated primary current waveform:

$$I_{prim,interp}(t) = \frac{1}{L_{M1}} \int V_{prim}(t)dt \tag{4.227}$$

Setting $L_{M1} = 140\ mH$ in (4.227) yields the green fit shown in Figure 4.124. Importantly, this inductance is ~3 times greater than that estimated in the design phase. This difference is fully attributed to the underestimation of the relative permeability of the magnetic core material. As described, this underestimation was done deliberately, yielding a somewhat oversized (though still small compared to the pulse transformer) tertiary winding series inductor design. It is again emphasized that instead overestimating the relative permeability may instead result in inductor saturation. In light of the obtained results, it is recommended to operate the bias power supply at lower current than initially specified. The correct bias current is currently being determined as part of testing at FAIR.

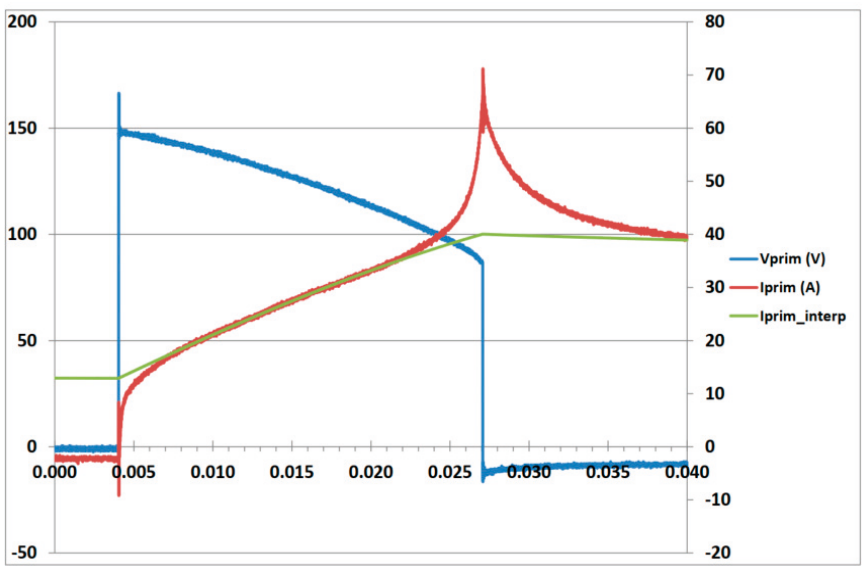



Figure 4.124: Measurement of magnetization inductance of pulse transformer component

*Tertiary winding series inductor: overview*

The developed tertiary winding series inductor component is shown in Figure 4.125. The developed component corresponds directly to that summarized by Table 4.13.

Figure 4.125: Developed tertiary winding series inductor component

*Tertiary winding series inductor: measurement of winding resistance (LCR meter)*

To measure the winding resistance of the tertiary winding series inductor, the LCR-meter E4980AL from Keysight was set up as indicated in Figure 4.126. Again, the LCR-meter was set for series LR circuit measurement. Note that, in this case, as the rated operating condition of the series inductor is significantly lower (intended to be powered by a 20 V/10 A power supply), the LCR-meter is able to provide a reasonably accurate measurement of both the resistance as well as the inductance parameter.

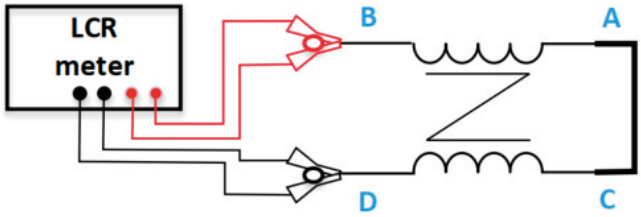



Figure 4.126: LCR-meter configuration for series resistance measurement of tertiary winding series inductor

Here, setting the LCR-meter to 1 V and 50 Hz, the winding resistance was measured to be 1.88 Ω and the differential mode inductance was measured to be 0.733 mH. The measured resistance is compared to that given by applying (4.196)-(4.199) to the developed design, yielding 1.79 Ω, i.e., on the order of 5% within the measured value. As with the pulse transformer winding resistance measurements, this difference is attributed to the accuracy of the estimation model as well as possible differences in the assumed resistivity (e.g., due to temperature differences) of the material.

*Tertiary winding series inductor: measurement of DM inductance (choke tester)*

To ensure accuracy, the power choke tester DPG10-1000B from ed-k GmbH was utilized to verify the inductance estimation, Figure 4.127. In this case, the instrument was able to generate the complete current-inductance mapping presented in Figure 4.128.

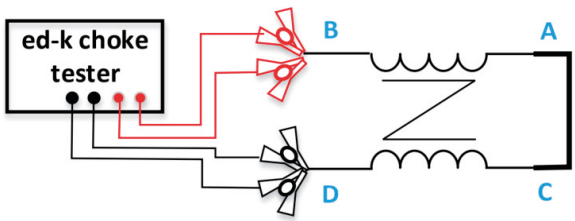



Figure 4.127: Choke tester configuration for DM inductance measurement of tertiary winding series inductor

Here, it is noted that the inductor has been designed for a nominal tertiary winding current of ~10 A with the current increasing up to ~15 A during the pulse event. As is seen, the inductance is largely linear up to ~20 A, providing the desired margin to saturation. The inductance is measured to be ~770 mH at 10 A, dropping to ~755 mH at 15 A. These values are compared to the 860 mH obtained through finite element analysis and (4.224), representing a ~10% deviation. This level of deviation is to be expected, and may be due to one (or quite likely, a combination) of several reasons, e.g., physical tolerances, difference in air gap length, magnetic core fill

factor and/or material permeability, or fringe field effects. Still, note that the obtained values are still somewhat greater than that originally predicted by (4.193). Additionally, the design margin to saturation is emphasized.

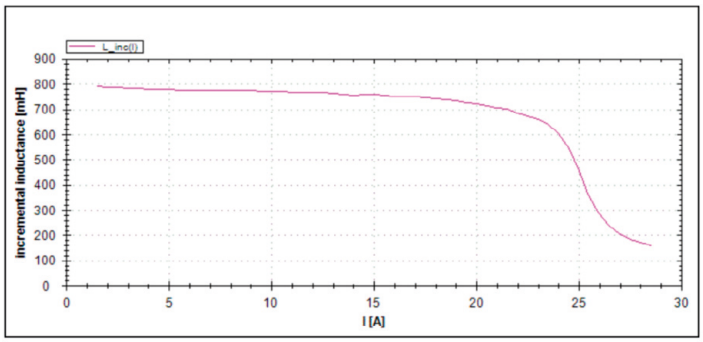



Figure 4.128: Differential mode inductance measurement of tertiary winding series inductor

*Summary: equivalent circuit parameters*

Table 4.14 summarizes the obtained equivalent circuit parameters, both as estimated by the methods developed throughout this chapter and through the above-described measurements.

**Table 4.14: Estimated and measured equivalent circuit parameters**

| Parameter | Symbol | Value | |
|---|---|---|---|
| Description | | Estimated | Measured |
| Number of primary winding turns | $N_1$ | 28 | |
| Number of secondary winding turns | $N_{2,a} + N_{2,b}$ | 856 | |
| Number of tertiary winding turns | $N_3$ | 56 | |
| Transformer primary winding resistance (referred to the primary) | $R_{w,1}/2$ | 5.9 mΩ | 6.3 mΩ |
| Transformer secondary winding resistance (referred to the secondary) | $R_{w,2,a} + R_{w,2,b}$ | 20.3 Ω | 26.3 Ω |
| Transformer tertiary winding resistance (referred to the tertiary) | $R_{w,3}$ | 0.16 Ω | 0.17 Ω |
| Transformer stray capacitance (seen from the secondary) | $C_d$ | 340 pF | - |
| Transformer leakage inductance (seen from the secondary) | $L_s$ | 31.6 mH | 31.5 mH |
| Transformer magnetization inductance (seen from the primary) | $L'_m$ | 45..150 mH | 140 mH |
| Tertiary winding series inductor resistance | $R_{L,3}$ | 1.79 | 1.88 Ω |
| Tertiary winding series inductor inductance | $L_3$ | 850 mH | 770 mH |

*High-voltage assembly: dynamic voltage withstand test*

Finally, it was desired to test the dynamic voltage withstand capability of the pulse transformer unit. To do this, the system was set up according to Figure 4.129. Operating the pulse generator with a pulse duration of 100 µs and a pulse repetition rate of 1 Hz, the primary voltage was progressively adjusted in reaching a secondary peak voltage amplitude of 160 kV (well above the nominal operating voltage of 115 kV). The system was then operated in this condition for 1 minute. Typical waveforms obtained in this operating mode are shown in Figure 4.130. Though these tests are not entirely indicative of long-term reliability, the voltage withstand capability of the pulse transformer component is clearly demonstrated.

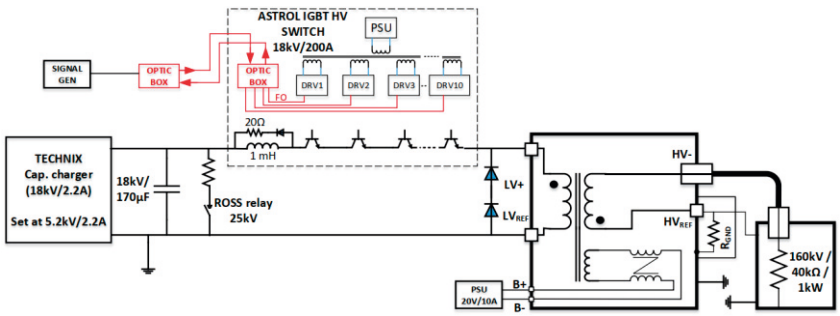



Figure 4.129: Configuration for dynamic insulation withstand testing in pulsed mode at 160 kV, 100 µs, 1 Hz, 1 min

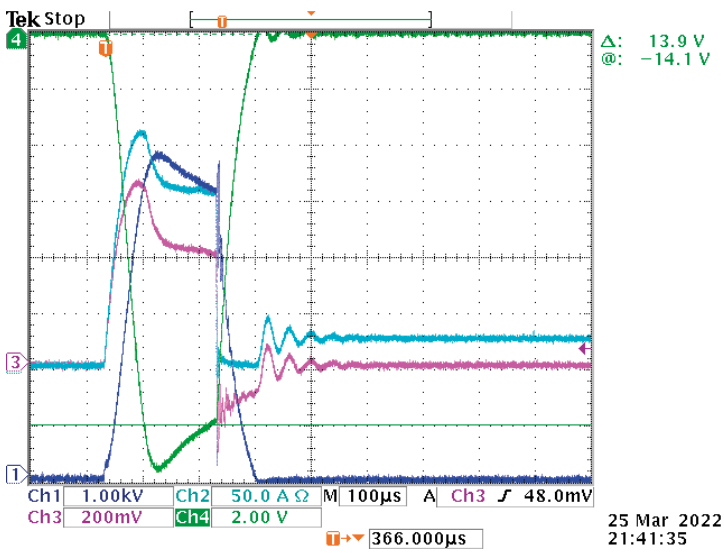



Figure 4.130: Typical waveforms obtained in dynamic insulation withstand testing. Dark blue: primary voltage (obtained using Tektronix differential probe, P5200A), light blue: primary current (obtained using Tektronix current probe, TCP404XL), purple: secondary current (obtained using current transformer, 0.1 V/A), green: secondary voltage (obtained with HV divider, 10 V represents 115 kV).

# 4.9 Case study: short pulse split-core transformer

## 4.9.1 Background

The preceding two case studies illustrate applications where the pulse length exceeds several hundred microseconds. For the sake of completeness, it is also of interest to verify the applicability of the developed equations to short pulse problems. Short pulse transformers are used regularly in, e.g., radio therapy applications, with typical modulator requirements as given in Table 4.15. Here, it is often beneficial to consider split-core pulse transformers to permit use of standardized off-the-shelf primary-side semiconductor components.

**Table 4.15: Typical short pulse application requirements**

| Symbol | Quantity | Value |
|---|---|---|
| | Klystron modulator requirements | |
| $V_2$ | Rated output voltage | 50 kV |
| $I_2$ | Rated output current | 100 A |
| $T_p$ | Total pulse length | 10 µs |
| $f_r$ | Pulse repetition rate | 50 Hz |
| $t_r$ | Pulse rise time | 2 µs |
| $M_p$ | Maximum overshoot | 1% |

This case study begins by outlining the essentials of split-core transformers in section 4.9.2. Then, in section 4.9.3, the developed design equations are adjusted to be compatible with the split-core layout. Here, the fundamental design choices are outlined and discussed in generating an optimal pulse transformer design for the requirements given in Table 4.15. Section 4.9.4 details finite element analysis and circuit simulation of the developed pulse transformer. Furthermore, a sensitivity analysis studying the effect of differences between the primary-side systems is presented. Finally, section 4.9.5 presents an experimental characterization of the developed pulse transformer system.

## 4.9.2 Split-core transformer theory

Split-core transformers have earlier been discussed in, e.g., [4.51]-[4.52]. The fundamental idea is to physically split the magnetic core longitudinally into several

pieces, placing independent primary windings on each split core leg. The secondary windings are wound in the usual manner, i.e., here encircling all split cores. As usual, the induced voltage in one of the secondary windings is given by $V_2 = N_2 \frac{d\Phi}{dt}$. Note here that $\Phi$ refers to the total core flux. Thus, for a transformer with $S$ split cores, the induced voltage may be expressed according to (4.228). Here, $\Phi_1$ represents the magnetic flux through split core 1, $\Phi_2$ represents the magnetic flux through split core 2, and so on. Of course, $\frac{d\Phi_1}{dt} = \frac{V_{p,1}}{N_{p,1}}$, $\frac{d\Phi_2}{dt} = \frac{V_{p,2}}{N_{p,2}}$, …, such that if 1) the number of winding turns for all primary winding are equal, i.e. $N_{p,1} = N_{p,2} = \cdots = N_p$, and if 2) the voltage applied to each primary winding is constant, i.e. $V_{p,1} = V_{p,2} = \cdots = V_p$, equation (4.228) may be rewritten according to (4.229). Of course, $V_2 I_2 = 2SV_p I_p$, i.e., $I_p$ may be written as (4.230). The essential benefit of split-core technology is this additional degree of freedom; by appropriately selecting $S$ and correspondingly matching the relationship $N_2/N_p$, both $V_p$ and $I_p$ – defining the primary-side source – may be set to match the capacity of standardized off-the-shelf semiconductor components.

$$V_2 = N_2 \frac{d\Phi}{dt} = N_2 \frac{d}{dt}(\Phi_1 + \Phi_2 + \cdots + \Phi_s) \tag{4.228}$$

$$V_2 = N_2 \left( \frac{V_{p,1}}{N_{p,1}} + \frac{V_{p,2}}{N_{p,2}} + \cdots \right) = 2SN_2 \left( \frac{V_p}{N_p} \right) \rightarrow \left( \frac{V_2}{V_p} \right) = 2S \left( \frac{N_2}{N_p} \right) \tag{4.229}$$

$$I_p = \frac{V_2 I_2}{2SV_p} = \left( \frac{N_2}{N_p} \right) I_2 \tag{4.230}$$

### 4.9.3 Pulse transformer design

As noted, the main reason in adopting the split-core pulse transformer approach is to facilitate primary circuit design and implementation. In this case, it was decided to split the magnetic core into six sub-cores (i.e., $S = 6$) in supporting twelve independent primary circuits. For the application requirements outlined in Table 4.15, this choice allows, e.g., the combination $V_1 = 1.2\ kV$ and $I_1 = 350\ A$. Clearly, these requirements are easily satisfied using off-the-shelf semiconductor components (e.g., IGBTs), facilitating modularization and thus ease of production. The application dictates that the secondary windings should be parallel connected. To further promote simplicity, single-layer parallel windings are adopted. Additionally, no core bias is to be implemented.

*Further design considerations*

In the pulse transformer design procedure developed in section 4.2.7, a maximum magnetic core depth constraint was imposed. As was seen, this is of importance to limit pulse transformer size in considering long pulse high power applications. Here, on the other hand, it is understood that the pulse transformer will be rather small and, conversely, a lower-bound constraint on particularly the per-core magnetic depth $y_c/S$ should be imposed to ensure the mechanical stability of the assembly. Additionally, a distance $d_s$ should be included in-between primary windings to facilitate assembly of the pulse transformer unit. In this case study, it was decided that $y_c/S \geq 15\ mm$ and $d_s = 9\ mm$. Finally, it is noted that, in this work, the total leakage inductance of the pulse transformer unit was calculated using the procedure developed in section 4.2.4 in estimating output pulse performance. This approach is sufficient for these purposes but may – as the leakage inductance is not evenly distributed among the different circuits – have other effects that may need to be taken into account in system design. This topic is further discussed in section 4.9.4.

*Pulse transformer optimization*

The pulse transformer design procedure outlined in section 4.2.7 was set up taking the above considerations into account. Here, given that the system average power is only on the order of a few kW, (4.84) is again considered an appropriate objective function in design. The resulting split-core pulse transformer design is summarized in Table 4.16 and shown in overview in Figure 4.131-

**Table 4.16: Overview of generated split-core pulse transformer design**

| Symbol | Quantity | Value |
|---|---|---|
| $x_c$ | Magnetic core leg width | 30.4 mm |
| $y_c/S$ | Magnetic core depth per split core | 18 mm |
| $S$ | Number of split cores | 6 |
| - | Number of independent primary windings | 12 |
| - | Secondary winding type | Single layer (parallel) |
| $N_2$ | Secondary turns per winding | 160 |
| $h_w$ | Secondary winding height | 27 cm |
| - | Primary winding type | Single layer (independent) |
| $N_p$ | Primary turns per winding | 23 |
| - | Primary winding height | 27 cm |

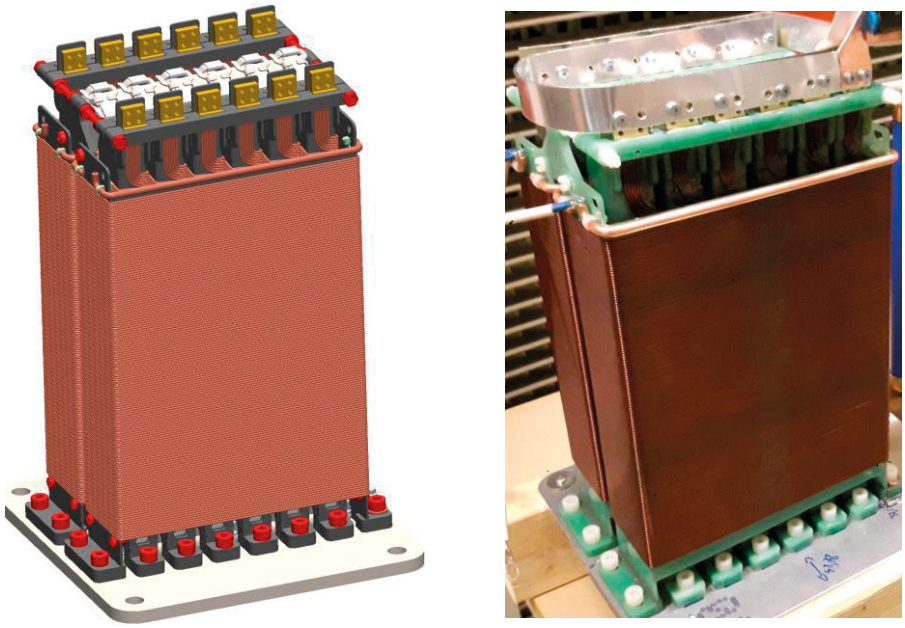


Figure 4.131: Overview of the developed split-core pulse transformer geometry- a) CAD drawing; b) built transformer.

### 4.9.4 Simulation results

Before production, the designed split-core pulse transformer was validated through 3D finite element analysis and circuit simulation-

*Finite element analysis*

Both magnetostatic and electrostatic 3D finite element analysis were carried out on the developed pulse transformer geometry. Two magnetostatic simulation cases are considered in the following. As in the preceding case studies, to obtain the magnetization inductance and to study the peak magnetic flux density in the magnetic core, the pulse transformer is first excited from the primary according to (4.231) leaving the secondaries open. Importantly, here $L_m$ represents the estimated total equivalent magnetization inductance as seen from the primary, i.e., $I_p = \Delta i_m/(2S)$. The simulated magnetostatic field distribution under these conditions is shown in Figure 4.132.a. Again, the magnetic flux density in the core leg straight sections is limited to ~1.2 T, and calculating the magnetization inductance according to (4.232) yields $L_m$~252 $\mu H$, within 2% of the analytically calculated value.

$$V_{L,m} = V_p = L_m \frac{\Delta i_m}{T_p} \rightarrow I_p = \frac{\Delta i_m}{2S} = \frac{V_p T_p}{2S L_m} \tag{4.231}$$

$$W_m \sim \frac{1}{2} L_m \left(2SI_p\right)^2 \rightarrow L_m = \frac{2W_m}{\Delta i_m{}^2} = \frac{2W_m}{\left(2SI_p\right)^2} = \frac{2}{\left(2SI_p\right)^2} \int p_m \, dV \tag{4.232}$$

Then, the pulse transformer is excited according to peak load conditions, i.e., with $I_2 = 100\ A$ and $I_1 = nI_2/(2S) = \sim 350\ A$. Again, this setting neglects the above studied transformer magnetization current in providing an estimate of the leakage field. Here, the obtained magnetostatic field distribution is shown in Figure 4.132.b. In accordance with the simplifications used in proposing the models described in section 4.2.4, the field is essentially confined to the space between the primary and the secondary windings. From this, the equivalent leakage inductance referred to the secondary is estimated according to (4.233). Here, the obtained leakage inductance value is on the order of 20% lower than the analytically calculated value. This discrepancy is somewhat greater than that seen in the preceding case studies, and may be attributed to the neglected area in-between primary windings.

$$W_m \sim \frac{1}{2} L_s I_2^2 \rightarrow L_s = \frac{2W_m}{I_2^2} = \frac{2}{I_2^2} \int p_m \, dV \tag{4.233}$$

Finally, an electrostatic finite element simulation was carried out to study the electric field strength. The electric potential is applied in accordance with the description given in section 4.2.3 for parallel windings. Here, the voltage on both windings increases from 0 to $V_s$. The corresponding electrostatic field strength is shown in Figure 4.133 and Figure 4.134. Figure 4.133 shows the electrostatic field strength in the front-plane placed through the middle of the pulse transformer geometry. Here, the peak electrostatic field strength is – as expected - seen close to the anti-corona ring and is limited to below that of 10 kV/mm. Note also that – with the exception of the volume in direct proximity to the anti-corona rings – the electrostatic field strength is limited to around 3-4 kV/mm in the transformer bulk volume. Figure 4.134 similarly shows the electrostatic field strength in the top-plane placed through the center of the pulse transformer geometry. Here, the peak electrostatic field strength is seen in the corners of the magnetic core and is limited to ~5 kV/mm. Finally, the stray capacitance is estimated through integration of the electric energy density, (4.234). From this, the equivalent stray capacitance referred to the secondary is estimated to be ~294 pF. Comparing this result to that calculated using the analytical methods developed in section 4.2.3 reveals a match within 7%.

$$W_e \sim \frac{1}{2} C_d V_s^2 \rightarrow C_d = \frac{2W_e}{V_s^2} = \frac{2}{V_s^2} \int p_e \, dV \tag{4.234}$$

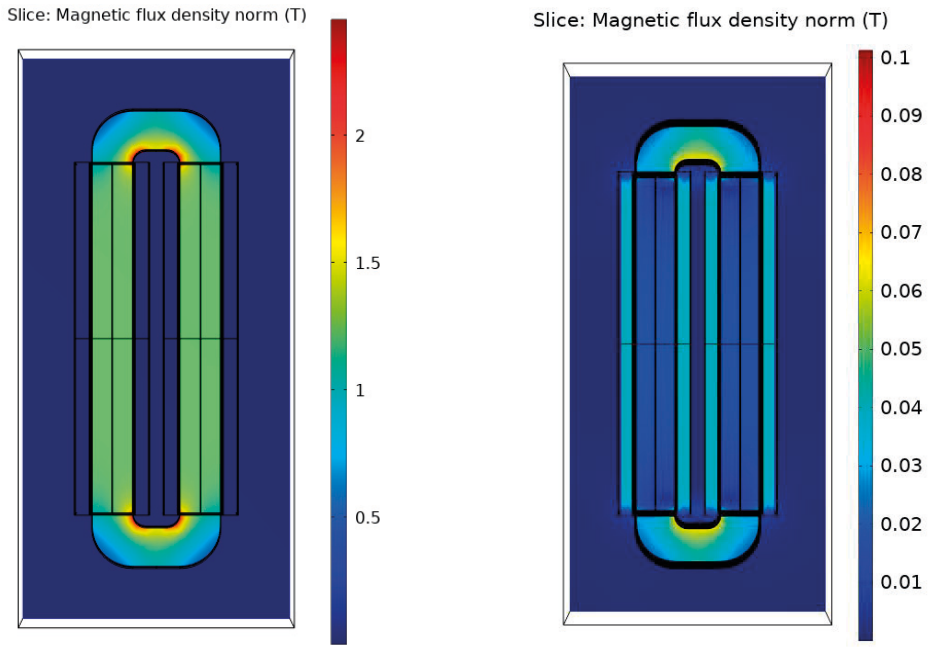



Figure 4.132: Magnetostatic simulation results for developed split-core transformer: a) open circuit; b) short circuit

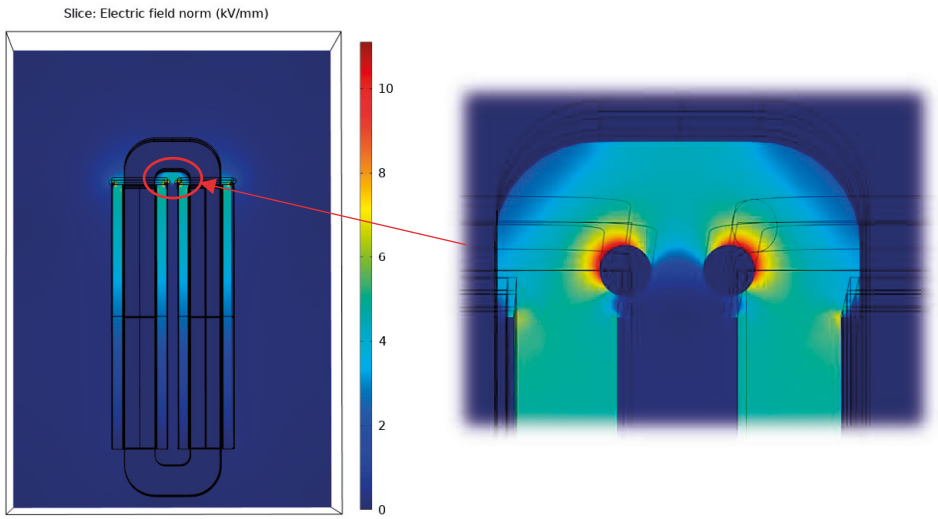



Figure 4.133: Electrostatic simulation results for developed split-core transformer. Front-plane: a) overview; b) zoom on anti-corona rings.

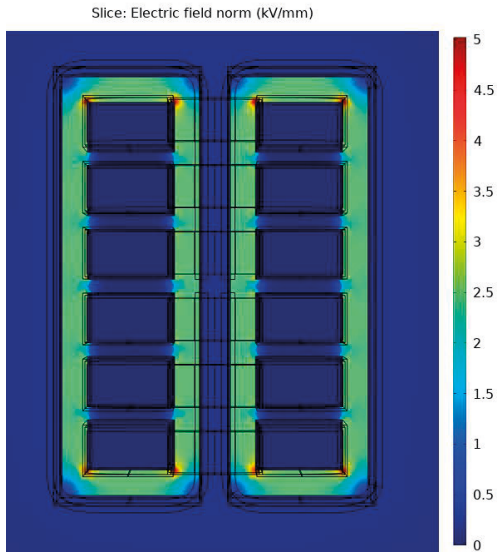



Figure 4.134: Electrostatic simulation results for developed split-core pulse transformer. Top-plane.

*Circuit simulation*

Finally, it is of interest to simulate a circuit representation of the complete system to ensure the function of the modulator. In this circuit representation, the lumped equivalent circuit parameters derived in the described finite element analysis are used. The split-core pulse transformer was modelled as a multi-winding transformer with 12 independent primary circuits and a single output circuit. Here, each primary circuit includes a separate voltage source, a separate switch that may be operated with an independently settable time delay $t_d$, a separate lumped busbar inductance $L_b$, and a separate lumped leakage inductance $L_s$. In this first section, the primary circuits are assumed to be identical such that $t_{d,1} = t_{d,2} = \cdots = t_{d,n} = 0$, $L_{b,1} = L_{b,2} = \cdots = L_{b,n} = L_{b,0}$ and $L_{s,1} = L_{s,2} = \cdots = L_{s,n} = 2SL_s$. Simulation under these conditions yields the results presented in Figure 4.135. Expectedly, as the primary circuits are identical, the twelve primary current waveforms are also identical and thus overlapping. Importantly, under these conditions, the desired pulse requirements may be seen to be adequately met – the 0-99% pulse rise time matches the required 2 µs without pulse overshoot.

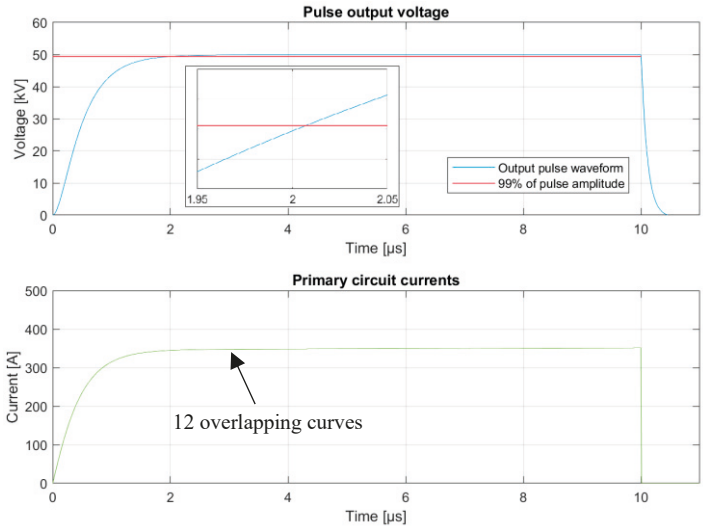



Figure 4.135: Circuit simulation results

In this section, it has been assumed that the twelve primary circuits are completely identical. Of course, this is a practical impossibility. In particular, it is of importance to study the effect of differences in 1) primary switch time delays, 2) primary circuit busbar inductance, and 3) split-core leakage inductance on, e.g., the output pulse waveform as well as the primary circuit currents. Sensitivity to these differences is studied in the following sections.

*Sensitivity analysis: leakage inductance*

Clearly, as discussed in section 4.2.4, the path of integration varies between the different primary winding sets. Still, the total equivalent leakage inductance value, here expressed in relation to the secondary as (4.235), should remain unaltered such that the stored magnetic energy, e.g., as calculated from the above finite element analysis, is conserved.

$$L'_s = \frac{1}{\frac{1}{k_1 L'_{s,w,0}} + \frac{1}{k_2 L'_{s,w,0}} + \cdots + \frac{1}{k_{2S} L'_{s,w,0}}} \tag{4.235}$$

Again, it may be seen that in particular the path of integration is significantly longer for the four windings located on the outermost corners of the magnetic assembly. Hence, writing $L'_{s,w,e} = L'_{s,w,0} k_e$ and $L'_{s,w,m} = L'_{s,w,0} k_m$, where $L'_{s,w,e}$ is the leakage inductance associated with the windings located on the outermost corners and $L'_{s,w,m}$ represents the leakage inductance associated with the windings located in the middle

of the assembly, (4.235) may be expressed as (4.236). Thus, to conserve the stored magnetic energy, $k_m$ may be written as a function of $k_e$ and $S$, (4.237).

$$L'_s = \frac{1}{\frac{4}{k_e L'_{s,w,0}} + \frac{2(S-2)}{k_m L'_{s,w,0}}} \tag{4.236}$$

$$k_m = \frac{S-2}{S-2/k_e} \tag{4.237}$$

Considering the geometry of Figure 4.131, it was determined that $k_e \approx 1.2 \rightarrow k_m = \sim 0.92$. Figure 4.136 shows simulated waveforms under these conditions in comparison to the idealized waveforms previously shown in Figure 4.135. Importantly, the effect on the pulse output voltage waveform is virtually non-existent. This is expected as the equivalent leakage inductance has been conserved through (4.235)-(4.237). On the other hand, a sizable difference is seen between the primary circuit currents. Here, the primary circuits supplying the primary windings located in the middle of the assembly experience an increase of up to 10% in current with respect to the idealized case. Clearly, consideration of this aspect is of great importance in choosing an appropriate primary side switch.

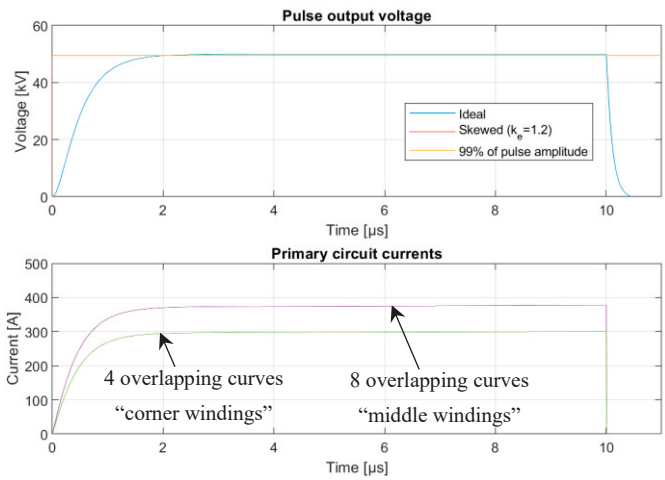



Figure 4.136: Simulation results, skewed leakage inductance

Then, a randomized factor $(1 + k_{r,n})$ was generated for and multiplied with each base leakage inductance value as given by (4.235)-(4.237). In the following, $-0.2 \leq k_{r,n} \leq 0.2$. Simulation results under these somewhat exaggerated conditions are shown in Figure 4.137. Still, the effect on the pulse output voltage waveform is seen

to be negligible. This is because the random effects distributed over $2S = 12$ primary circuits even out on average. The effect on individual primary circuit currents, however, is more significant. Here, some switches are seen to carry currents more than 20% greater than that earlier suggested in idealized simulation.

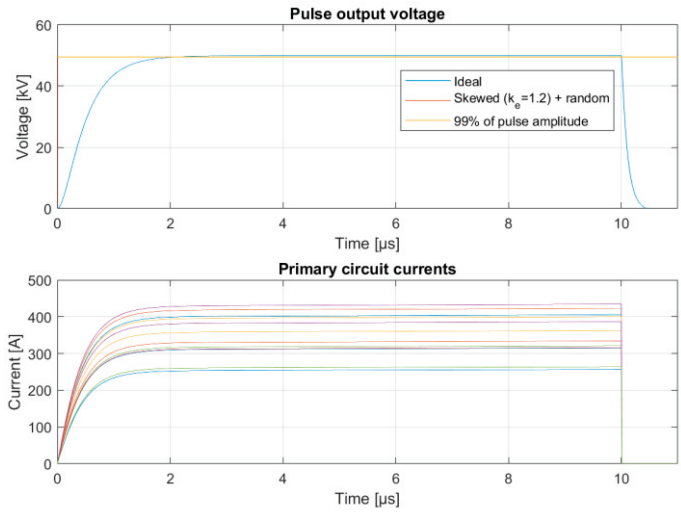



Figure 4.137: Simulation results, randomly skewed leakage inductance

*Sensitivity analysis: busbar inductance*

The busbars interconnecting the different primary circuits to the different pulse transformer primary windings invariably vary in length. In particular, in the developed experimental setup to be further described in the following section, two distinct groups of primary side circuits were – for entirely practical reasons - placed at different distances from the split-core pulse transformer unit. Of course, this fact may straightforwardly be modelled in the developed circuit representation by inclusion of a busbar length factor $k_{b,n}$ such that $L_{b,n} = L_{b,0}k_{b,n}$. In this case, considering first the above-described test setup, the two groups of primary-side circuits were set up such that $k_{b,1-6} = 1$ and $k_{7-12} = 1.5$, i.e., representing the fact that one group of circuits connect to the pulse transformer with 50% longer busbars.

Simulated waveforms under these conditions are shown in Figure 4.138. This time, a slight increase in 0-99% pulse rise time is seen. Of course, this is expected as the total primary-side inductance has been increased somewhat. Still, the busbars represent a relatively small part of the total inductance such that the increase is essentially negligible as compared to the accuracy of the developed equations.

Of course, in practice, there are further differences also between busbars within the same group. Here, this is represented by adding a random $\pm 0.2 L_{b,0}$ to each primary-side circuit. Simulated waveforms under these conditions are shown in Figure 4.139. Expectedly, with a relatively large number of primary-side circuits, the impact on pulse rise time is limited as the net leakage inductance is retained. At the same time, a greater distribution in primary circuit current is seen.

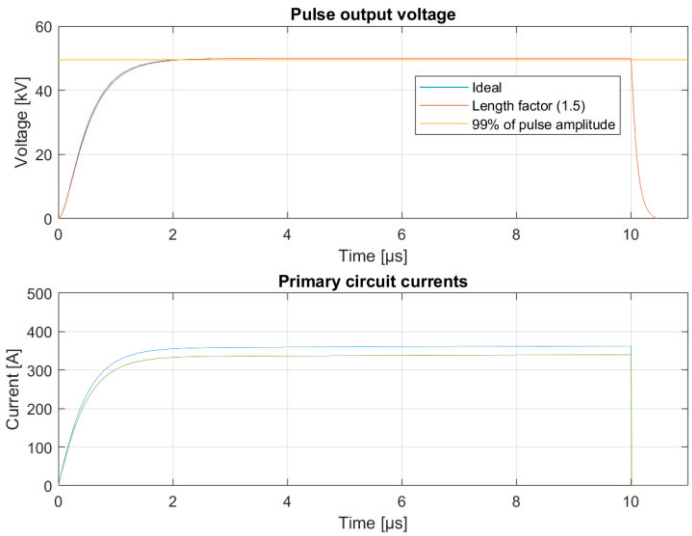



Figure 4.138: Simulation results, impact of busbar length

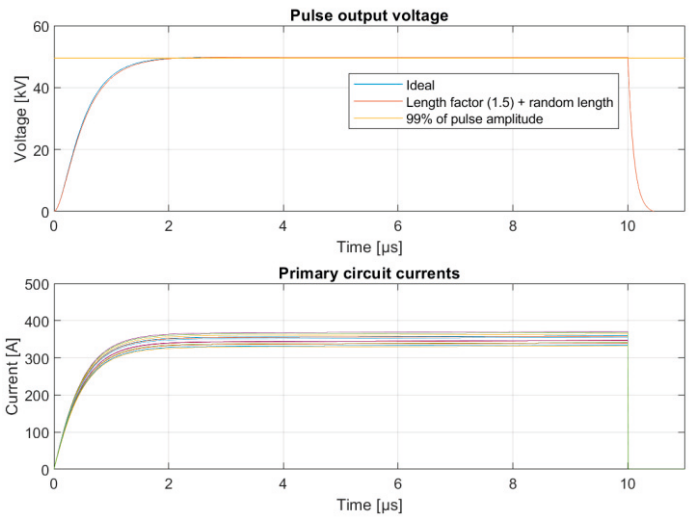



Figure 4.139: Simulation results, impact of busbar length (random)

*Sensitivity analysis: primary circuit time delay*

Finally, there might be unavoidable time delays between the different primary circuits. As will be seen in the following section, this was the case in the developed experimental setup. There, one of the two aforementioned groups of primary-side circuits was delayed with respect to the other. Most importantly, this time delay is translated into pulse rise time elongation as the effective equivalent primary voltage is reduced during part of the pulse rise.

The results obtained by simulating with a time delay of 0.1 µs (i.e., 5% of the nominal pulse rise time) for half of the primary-side circuits are shown in Figure 4.140. As can be seen, the resulting pulse rise time has increased to ~2.06 µs, representing an increase of 3% with respect to the idealized case. Additionally, the group without time delay are seen to carry currents around 10% greater than that of the idealized case under nominal load conditions. Again, this represents an important consideration in choosing the primary-side switch.

Finally, the preceding case is extended by an additional randomized time delay (between 0-0.1 µs) to the delayed group. Expectedly, this results in a further extension of the pulse rise time – in this case to ~2.12 µs – as well as a further increase to the primary-side current of the non-delayed circuits.

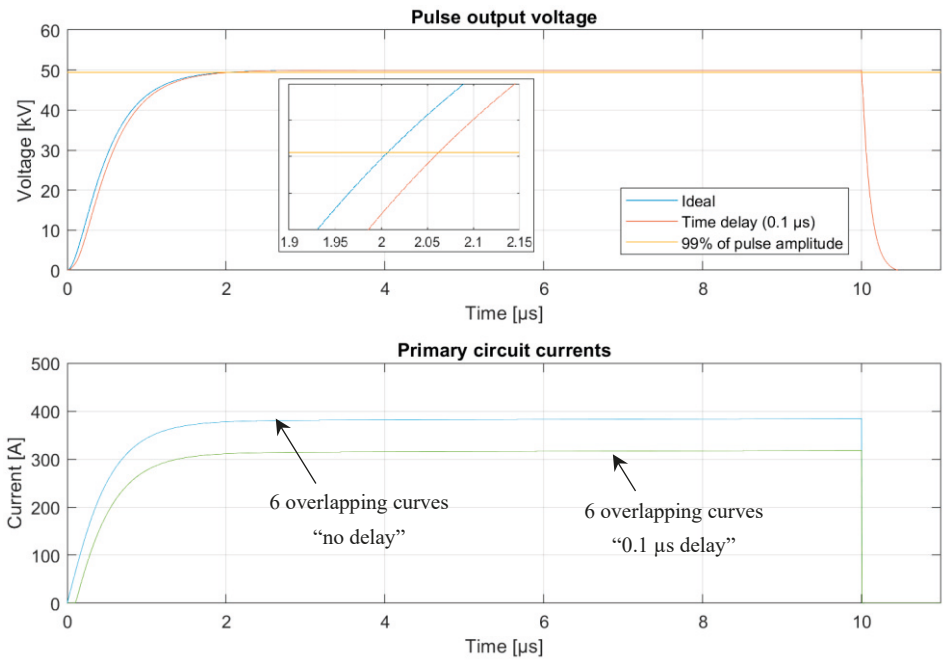



Figure 4.140: Simulation results, impact of gate driver time delay

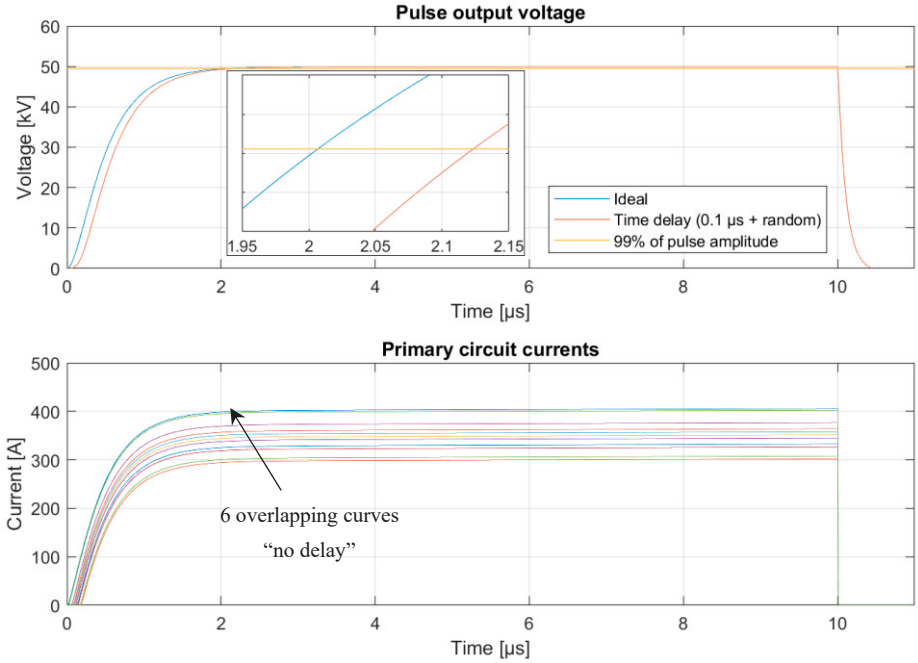



Figure 4.141: Simulation results, impact of gate driver time delay (with added randomized delay)

## 4.9.5 Experimental results

The preceding section presented an in-depth simulation study of the developed split-core pulse transformer design. Based on these results, the developed transformer was built and tested. This section presents experimental verification of the built transformer with particular focus on the following items-

- Pulsed operation at nominal operating conditions
- Measurement of transformer magnetization inductance
- Measurement of transformer leakage inductance

*Nominal power testing*

For testing at nominal power, the output of the pulse transformer unit was connected to a resistive load designed to exhibit resistance according to $R_k = V_2/I_2 = 500\ \Omega$, Figure 4.142. Here, four power resistors from Metallux (50 kV, 600 W, 500 Ω) were used. The system was powered by the CCR1KV-10KJ capacitor charger (1 kV, 10 kW) from Technix. As described, using pre-existing equipment to implement the primary circuit switches led to two distinct groups of primary-side circuits placed at different distances from the split-core pulse transformer units. Here, a set of three

SEMIX IGBT power modules from SEMIKRON was used in implementing the primary circuit switches.

Figure 4.142: Resistive load used in testing the developed split-core pulse transformer

Experimental results are shown in Figure 4.143. As shown in Figure 4.143.a, the pulse is triggered at approximately $t = -2\ \mu s$, lasting the intended 10 µs before being turned off at $t = +8\ \mu s$. Then, as shown in Figure 4.143.b and Figure 4.143.c, following a 2 µs interlocking delay, i.e., at $t = 0$, the first group of six primary switches is turned on. Then, after a ~0.5 µs signal delay, the second group (i.e., the remaining six primary switches) is turned on. The resulting output pulse voltage waveform is shown in Figure 4.143.d. Here, the designed 0-99% pulse rise time of ~2 µs is verified. Importantly, the predicted primary current asymmetry appears to not have appreciable impact on the pulse waveform. Furthermore, there is no indication of pulse transformer magnetic core saturation.

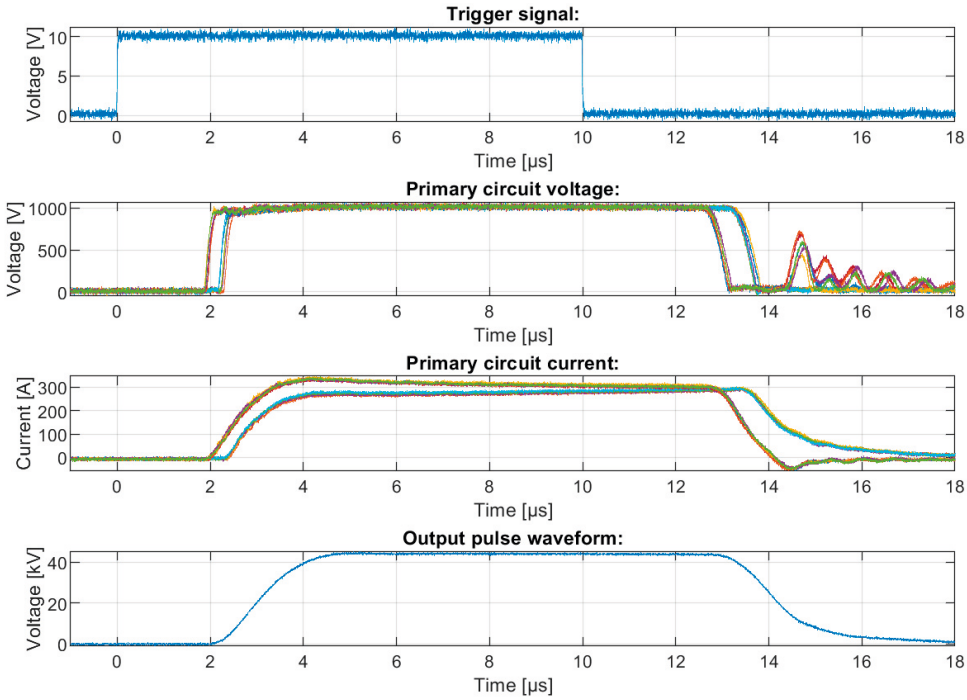



Figure 4.143: Nominal power testing

*Measurement of transformer leakage inductance*

The power choke tester DPG10-1000B from ed-k, [4.50], was used in measuring the pulse transformer leakage inductance. Here, the secondary windings were short circuited whereas the twelve primary windings were connected in parallel, Figure 4.144. Measurement in this configuration yields the total leakage inductance seen from the primary. Transforming this value to the secondary side of the transformer allows comparison to the analytically estimated value, Figure 4.145. Expectedly, the measured leakage inductance is rather constant over the range of applied currents. Furthermore, the measured value is seen to be within 20% of the estimated value.

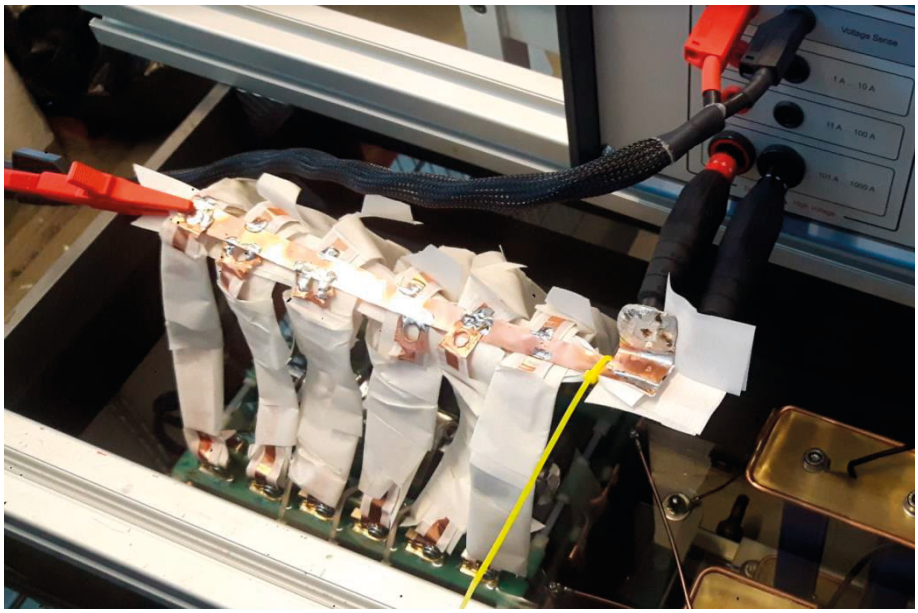


Figure 4.144: Setup for measuring the total leakage inductance of the developed split-core transformer

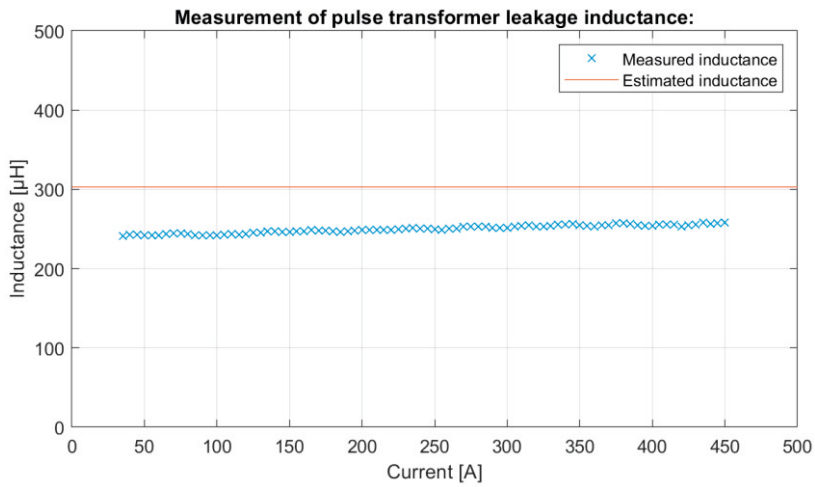



Figure 4.145: Leakage inductance measured with ed-k power choke tester compared to estimated inductance value

*Measurement of transformer magnetization inductance*

The power choke tester DPG10-1000B from ed-k, [4.50], was used in measuring the pulse transformer leakage inductance. This time, the secondary windings were open circuited and may be neglected in analysis. The primary windings were again connected in parallel. The obtained results are shown in Figure 4.146-

The measured applied magnetization current corresponding to the intended peak magnetic flux density of 1.2 T is indicated with a black line, Figure 4.146.a. Importantly, the transformer core material is far from saturating at the intended operating point. Figure 4.146.b and Figure 4.146.c depict the measured magnetization inductance and the corresponding relative permeability, respectively. Expectedly, these quantities are highly non-linear. Calculating the average measured magnetization inductance over the applicable range of currents yields 218 µH, within 20% of the estimated magnetization inductance of 263 µH. As indicated in Figure 4.146.c, this is very likely – at least in part - due to a discrepancy between the assumed and the actual relative permeability values.

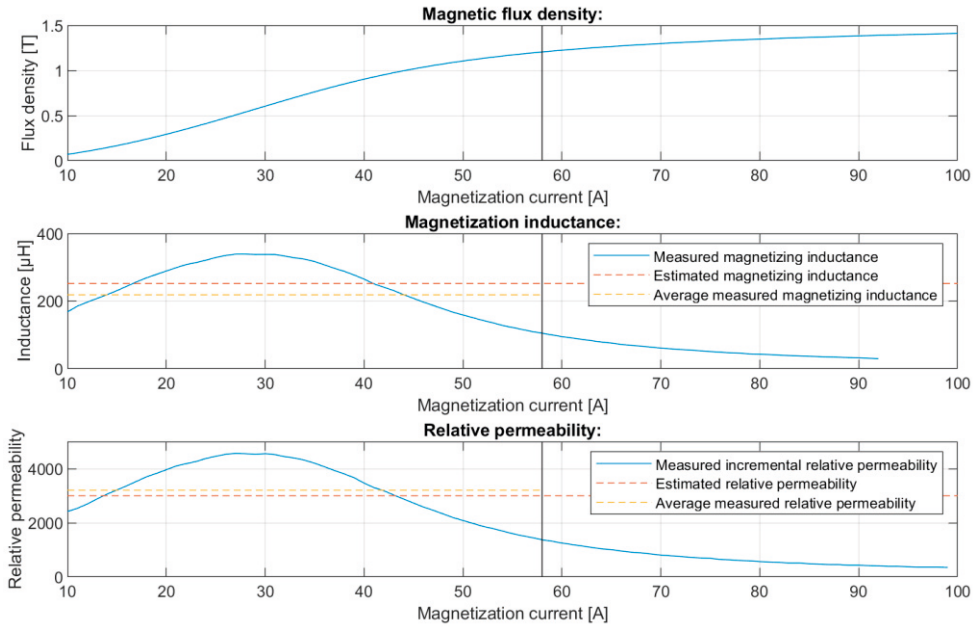



Figure 4.146: Split-core transformer magnetization measurements with ed-k power choke tester

## 4.10 References

[4.1] Pulse Transformers, IEEE standard 390-197, 1987 (reaffirmed 2007).

[4.2] M. Alaküla et al., Power Electronics: Devices, Converters and Applications. Lund: Lunds Universitet Media-Tryck, 2013.

[4.3] S. Candolfi, P. Viarouge, D. Aguglia, and J. Cros, "Finite-element-based optimal design approach for high-voltage pulse transformers," IEEE Trans. Plasma Sci., vol. 43, no. 6, pp. 2075–2080, Jun. 2015.

[4.4] Y. Wang, M. Li, K. Li, and G. Zhang, "Optimal design and experimental study of pulse transformers with fast rise time and large pulse duration," IEEE Trans. Plasma Sci., vol. 42, no. 2, pp. 300–306, Feb. 2014.

[4.5] D. Habibinia and M. R. Feyzi, "Optimal winding design of a pulse transformer considering parasitic capacitance effect to reach best rise time and overshoot," IEEE Trans. Dielectr. Electr. Insul., vol. 21, no. 3, pp. 1350–1359, Jun. 2014.

[4.6] J. Biela, D. Bortis, and J. W. Kolar, "Modeling of pulse transformers with parallel- and non-parallel-plate windings for power modulators," IEEE Trans. Dielectr. Electr. Insul., vol. 14, no. 4, pp. 1016–1024, Aug. 2007.

[4.7] J. Biela and J. W. Kolar, "Using transformer parasitic for resonant converters-a review of the calculation of the stray capacitance of transformers," IEEE Trans. Ind. Appl., vol. 44, no. 1, pp. 223–233, Jan./Feb. 2008

[4.8] A. Ayachit and M. K. Kazimierczuk, "Self-capacitance of single-layer inductors with separation between conductor turns," IEEE Trans. Electromagn. Compat., vol. 59, no. 5, pp. 1642–1645, Oct. 2017.

[4.9] G. Grandi, M. K. Kazimierczuk, A. Massarini, and U. Reggiani, "Stray capacitance of single-layer solenoid air-core inductors," IEEE Trans. Ind. Appl., vol. 35, no. 5, pp. 1162–1168, Sep./Oct. 1999.

[4.10] MATLAB fmincon optimizer. Accessed: June 24, 2023. [Online]. Available: https://se.mathworks.com/help/optim/ug/fmincon.html

[4.11] M. Collins and C. A. Martins, "Evaluation of Trends in Optimal Design of Pulse Transformers for Long Pulse High Power Applications" in Proc. 2018 IEEE Int. Power Modulator and High Voltage Conf. (IPMHVC), Jackson, WY, USA, Jun. 2018, pp. 31-36.

[4.12] M. Collins and C. A. Martins, "Optimal design of electronic bouncers for long-pulse high-power modulators," IEEE Trans. Plasma Sci., vol. 49, no. 2, pp. 819–829, Feb. 2021.

[4.13] C. Pappas, G. d'Auria, P. del Giusto, A. Franceschinis, A. Turchet, and L. Veljak, "Power modulators for Fermi's linac klystrons," in Proc. IEEE Part. Accel. Conf. (PAC), Albuquerque, NM, USA, Jun. 2007, pp. 2448–2450.

[4.14] D. Gerber and J. Biela, "Bouncer circuit for a 120 MW/370 kV solid state modulator" in Proc. 2011 IEEE Pulsed Power Conf. (PPC), Chicago, IL, USA, Jun. 2011, pp. 1-6.

[4.15] C. A. Martins, F. Bordry, and G. Simonet, "A solid state 100 kV long pulse generator for klystrons power supply," in Proc. 13th Eur. Conf. Power Electron. Appl., Barcelona, Spain, Sep. 2009, pp. 1–10.

[4.16] D. Bortis et al., "Optimal design of a two-winding inductor bouncer circuit" in Proc. 2009 IEEE Pulsed Power Conf. (PPC), Washington, DC, USA, Jun. 2009, pp. 1390-1395.

[4.17] D. Bortis et al., "Optimal Design of a Two-Winding Inductor Bouncer Circuit," IEEE Trans. Plasma Sci., vol. 38, no. 10, pp. 2716-2724, May 2010.

[4.18] S. Blume et al., "Control of an active bouncer for an ultra precise 140 µs-solid state modulator system" in Proc. of 17th European Conf. on Power Electronics and Applications (EPE'15), Geneva, Switzerland, Sept. 2015, pp. 1-11.

[4.19] D. Aguglia, "2 MW active bouncer converter design for long pulse klystron modulators" in Proc. of 14th European Conf. on Power Electronics and Applications (EPE'11), Birmingham, UK, 30. Aug.-1 Sept. 2011, pp. 1-10.

[4.20] S. Maestri et al., "Improved control strategy for active bouncers used in klystron modulators" in Proc. of 14th European Conf. on Power Electronics and Applications (EPE'11), Birmingham, UK, 30. Aug.-1 Sept. 2011, pp. 1-10.

[4.21] X. Bonnin and D. Aguglia, "Evaluation of a hybrid bouncer system for high precision klystron modulators" in Proc. IEEE Int. Power Modulator High Voltage Conf. (IPMHVC), San Francisco, CA, USA, Jul. 2016, pp. 552–557.

[4.22] X. Bonnin and D. Aguglia, "A hybrid bouncer system for highly repeatable and precise klystron modulators" in Proc. IEEE Int. Pulsed Power Conf., Brighton, U.K., Jun. 2017, pp. 1–8.

[4.23] Electronicon AC Power Capacitor E62HC. Accessed: June 24, 2023. [Online]. Available: https://www.electronicon.com/en/products/ac-power-capacitors/e62

[4.24] X. Yang et al., "Analysis and validation of the output current ripple in interleaved buck converter" in Proc. of 43rd Annual Conf. of the IEEE Industrial Electronics Society, Beijing, China, Dec. 2017, pp. 846-851.

[4.25] T. Hegarty, "Benefits of multiphasing buck converters". Accessed: June 24, 2023. [Online]. Available: https://www.eetimes.com/benefits-of-multiphasing-buck-converters-part-1/

[4.26] M. Chen and C. R. Sullivan, “Unified Models for Coupled Inductors Applied to Multiphase PWM Converters”, IEEE Trans. Power Electronics, vol. 36, no. 12, pp. 14155-14174, Jun. 2021.

[4.27] P-L. Wong et al., “Performance improvements of interleaving VRMs with coupling inductors”, IEEE Trans. Power Electronics, vol. 16, no. 4, pp. 499-507, Jul. 2001.

[4.28] P. A. Tipler and G. Mosca, Physics for Scientists and Engineers, 6th ed. New York: W.H. Freeman and Company, 2008.

[4.29] Electronicon DC-Capacitors, E51, E53, E55. Accessed: June 24, 2023. [Online]. Available: https://www.electronicon.com/en/products/dc-capacitors/e51/e53/e55

[4.30] A. Wintrich et al., “Application manual power semiconductors,”

SEMIKRON Int. GmbH, Nuremberg, Germany, Tech. Rep., 2015, pp. 126–129. [Online]. Available: https://www.semikron.com/servicesupport/application-manual.html

[4.31] Hitachi Energy High-power Thyristors. Accessed: June 24, 2023. [Online]. Available: https://www.hitachienergy.com/products-and-solutions/semiconductors/thyristors

[4.32] Hitachi Energy Diodes. Accessed: June 24, 2023. [Online]. Available: https://www.hitachienergy.com/products-and-solutions/semiconductors/diodes

[4.33] Mitsubishi Electric High-Voltage IGBT Modules. Accessed: June 24, 2023. [Online]. Available: https://www.mitsubishielectric.com/semiconductors/products/powermod/hvigbtmod/index.html

[4.34] SEMIKRON IGBT modules. Accessed: June 24, 2023. [Online]. Available: https://www.semikron-danfoss.com/products/product-classes/igbt-modules.html

[4.35] M. Kempkes et al., “Pulsed power systems for ESS klystrons” in Proc. IEEE Int. Pulsed Power Conf., Austin, TX, USA, 31 May-4 Jun. 2015, pp. 1–4.

[4.36] High-Power IGCT Switches - State-Of-The-Art and Future. Accessed: June 24, 2023. [Online]. Available: https://www.power-mag.com/pdf/feature_pdf/1305890223_ABB_Cover_Feature_Layout_1.pdf

[4.37] N. Mohan et al., Power Electronics: Converters, Applications, and Design, 3rd ed. Hoboken, NJ: Wiley, 2002.

[4.38] S. Ashby et al., “CLIA — A compact linear induction accelerator system” in Proc. Int. Conf. on High-Power Particle Beams, Washington, DC, USA, May. 1992, pp. 1855-1860.

[4.39] E. G. Cook et al., “Solid-State Modulator R&D at LLNL” in Proc. Int. Workshop on Recent Progress of Induction Accelerators, Tsukuba, Japan, Oct. 2002, pp. 3-11.

[4.40] D. Bortis et al., “Optimal Design of a DC Reset Circuit for Pulse Transformers” in Proc. IEEE Applied Power Elec. Conf. and Exposition, Anaheim, CA, USA, 25 Feb.-1 Mar. 2007, pp. 1171-1177.

[4.41] D. Aguglia et al., “Design solutions for compact high current pulse transformers for particle accelerators' magnets powering” in Proc. of 17th European Conf. on Power Electronics and Applications (EPE'15), Geneva, Switzerland, Sept. 2015, pp. 1-8.

[4.42] D. Bortis et al., “Design and control of an active reset circuit for pulse transformers,” IEEE Trans. Dielectr. Electr. Insul., vol. 16, no. 4, pp. 940-947, Aug. 2009.

[4.43] KEMET ALS30A222NP500. Accessed: June 24, 2023. [Online]. Available: https://www.kemet.com/en/us/capacitors/aluminum/product/ALS30A222NP500.html

[4.44] Infineon Technologies FZ750R65KE3. Accessed: June 24, 2023. [Online]. Available: https://www.infineon.com/dgdl/Infineon-FZ750R65KE3-DataSheet-v01_10-EN.pdf?fileId=db3a304325afd6e00126461fd3936974

[4.45] - M. Collins and C.A. Martins, “An Integrated Optimal Design Procedure for Pulse Transformer-based Klystron Modulators for Long-Pulse High-Power Applications”. IEEE Trans. Plasma Sci., vol. 51, no. 11, pp. 3358-3367.

[4.46] TDK-Lambda ALE Rack Mount Series. Accessed: June 24, 2023. [Online]. Available: https://www.us.lambda.tdk.com/products/high-voltage-power/capacitor-charging/ale-rackmount.html

[4.47] Technix High Voltage Capacitor Charger. Accessed: June 5, 2023. [Online]. Available: https://technix-hv.com/application-or-function/capacitor-charger/

[4.48] Poynting HV Power Supplies. Accessed: June 24, 2023. [Online]. Available: https://www.poynting.de/en/id-100-kw-and-greater.html

[4.49] ABB Asymmetric Integrated Gate-Commutated Thyristor 5SHY 35L4503 Datasheet. Accessed: June 24, 2023. [Online]. Available: https://library.e.abb.com/public/19c69deb0ada89ddc1256b9f003ebccd/5SHY_35L4503_5SYA1228.pdf

[4.50] ed-k Power Choke Tester DPG10-1000B. Accessed: June 24, 2023. [Online]. Available: https://www.ed-k.de/products/dpg10-series/dpg10-1000b/?lang=en

[4.51] S. Ushkewar et al., “Modeling and analysis of split core pulse transformer for solid state pulse power modulator” in Proc. of 2nd Int. Conf. on Electrical, Computer and Communication Technologies, Coimbatore, India, Feb. 2017, pp. 1-6.

[4.52] D. Gerber and J. Biela, “Design of an Ultraprecise 127-MW/3-µs Solid-State Modulator with Split-Core Transformer”, IEEE Trans. Plasma Sci., vol. 44, no. 5, pp. 829-838, May 2016.

# 5. Optimization of Stacked Multi-Level modulators

## 5.1 Overview

The stacked multi-level (SML) modulator topology was proposed in response to the shortcomings of conventional modulator topologies in considering long pulse high power applications and was described in chapter 3. The goal of this chapter is to develop a comprehensive framework for design optimization and study of the SML modulator. To achieve this, each modulator component is first modelled and studied independently. Here, the European Spallation Source klystron modulator application requirements are used as a representative case to study implications in long pulse high power design. The chapter is disposed as follows-

- Section 5.2 describes modeling and design of the components comprising the input stage chargers of the proposed modulator topology. The design models are then integrated in a unified framework for optimization of a single charger circuit.
- In the same manner, section 5.3 describes modeling and design of the components comprising the output stage pulse generators of the proposed modulator topology. Again, the design models are integrated in a unified framework optimization of a single pulse generator circuit.
- In section 5.4, the developed design frameworks for the input stage charger (section 5.2) and the output stage pulse generators (section 5.3) are combined in developing a single design optimization framework for the complete SML modulator topology.
- Finally, the chapter is concluded in section 5.5 where the developed optimization routine is used to study the case of the European Spallation Source klystron modulator requirements. The obtained klystron modulator design results are later compared to the developed and implemented 660 kVA modulator systems at the European Spallation Source facility.

## 5.2 Modeling and design of input stage converters

### 5.2.1 Overview

The input stage converters supply the main capacitor banks with the energy required in pulsing. Importantly, an active front-end is used in combination with a current controlled DC/DC converter to 1) provide constant power charging despite the pulsed load while 2) ensuring sinusoidal line currents and unitary power factor [5.1]-[5.2]. To further improve input stage power quality, harmonic line filters are implemented. The input stage is modular, allowing the total modulator input power to be split between several charger systems. A complete input stage design therefore requires appropriate selection of the number of charger systems and, subsequently, detailed design and selection of the aforementioned power components. In this section, design models are developed and integrated considering a single charger module handling the power $\bar{P}_m/N_c$, where $\bar{P}_m$ is the total average modulator input power and $N_c$ is the number of parallel charger modules. The advantages and drawbacks as well as the impact on the input charger components as a result of utilizing $N_c$ chargers are analysed in section 5.5.

### 5.2.2 Input stage design and parameter selection

As noted in the preceding section and elaborated in chapter 7, the active rectifier circuit is controlled using pulse width modulation to shape the line current to be sinusoidal and in-phase with the corresponding line voltage, requiring an inductive link. Furthermore, as explained in chapter 2, it must be ensured that the generated harmonics are compatible with applicable standards, e.g. [5.3]-[5.4]. As will be described in chapter 8, the reduced scale technology demonstrator utilized a simple inductive link through which line current harmonics were sufficiently limited by appropriate selection of the inductance value. However, as the ESS klystron modulators require an input power of up to 5 times greater than that of the rated power of the technology demonstrator, this approach would result in an extremely bulky and oversized set of line inductors. Instead, in this work, the classical LCL filter with shunt RC damper has been adopted, Figure 5.1. This filter topology provides sufficient attenuation (-60 dB/decade) and effective damping of the filter resonance. Furthermore, comprehensive design of compact and highly efficient filters is straightforward and simple to understand.

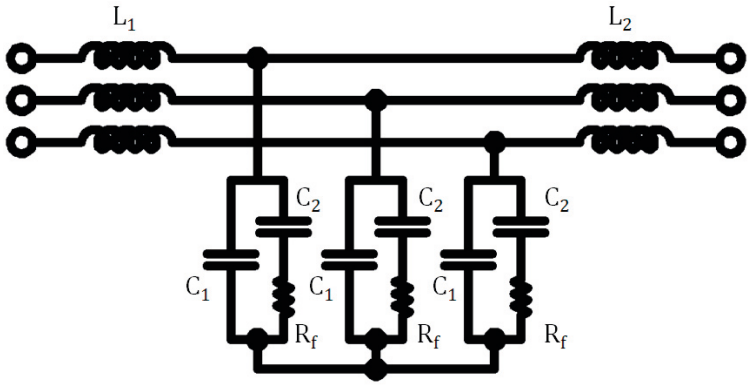



Figure 5.1: Adopted filter topology- classical LCL filter with shunt RC damper branch.

As a matter of fact, several design procedures for this type of filter have been proposed in literature, e.g., [5.5]-[5.7]. The general idea involves first selecting the inner inductance value to limit the converter-side ripple current. Setting the outer inductance value in proportion to the inner inductance value, the filter capacitance may then be calculated such that appropriate filter attenuation is obtained (i.e., that which constrains the line current THD to the limits prescribed by the appropriate standard). Finally, the resistive element is selected in a trade-off between resonant peak damping and filter losses. In generating a suitable filter design, constraints may be put on losses, absorbed reactive power, inductive voltage drop, and so on [5.5]-[5.7].

Despite the apparent simplicity of the outlined design procedure, it should be recognized that there is quite possibly an infinite number of viable filter designs (i.e., combinations of $L_1$, $L_2$, $C_1$, $C_2$ and $R_f$ satisfying the imposed filter requirements and design constraints), though these might be (and likely are) very different in terms of both component and system volume and efficiency. In practice, it is clear that these differences must be accounted for in design. Furthermore, it is clear that the line-side converter switching frequency, determining the required filter cut-off frequency (and thus filter component size) and directly impacting converter losses, should not be selected independently but be taken into account as part of a system optimization. Additionally, in this application, it is convenient to implement the front-end converter on a common heat sink with the output DC/DC converter. Consequently, a design and optimization procedure taking into account the complete input stage is desirable.

In this work, the front-end converter switching frequency $f_{sw,AFE}$, the DC/DC converter switching frequency $f_{sw,DC/DC}$, the permissible converter-side ripple current $\Delta i_{L2}$ and the proportionality constant $L_1 = k_{f,L} L_2$ are considered fundamental design parameters. In addition, as will be described in the subsequent sections, each inductor will be designed individually with four design parameters:

the magnetic core leg width $x_c$, the magnetic core depth $y_c$, the per-air gap length $g$, and the winding current density $J$. Based on the selection of these design parameters, the performance of a given input stage design is assessed using the procedure later depicted in Figure 5.14. The rest of this section details modeling of the different components and their integration into a complete optimization procedure.

### 5.2.3 Inductive filter components

The chosen filter topology requires two three-phase inductors, Figure 5.1. In this work, the converter-side inductor $L_2$ is chosen to limit the converter-side ripple current whereas the grid-side inductor $L_1$ is chosen in direct proportion to $L_2$. Importantly, active rectifier operation is associated with generation of a common mode voltage component on the dc-link. As will be demonstrated in section 5.2.5, implementing $L_2$ using three individual single-phase inductors provides an effective way of mitigating the generated common mode voltage without need of an added common mode filter. Then, since $L_1$ will be chosen to be. e.g., 5…10% of $L_2$, a small standard three-phase inductor is preferred. In this section, sizing models are developed for these inductor types.

*Converter-side inductor*

The converter-side inductor $L_2$ is implemented as three single phase inductors. In the inductance and power range of interest, a standard laminated double C core with foil windings is appropriate. In this work, water cooling is implemented by affixing a cooling plate in-between the magnetic core and the innermost foil winding layer, Figure 5.2.

Having selected $L_2$ in accordance with the above and considering the core leg width $x_c$, the core depth $y_c$, the per air gap length $g$ and the winding current density $J$ as fundamental design parameters, the required number of winding turns may be calculated according to (5.1). Then, the corresponding peak magnetic flux density $\hat{B}$ may be calculated and compared against the maximum allowable peak magnetic flux density $B_{max}$, (5.2). If $\hat{B} > B_{max}$, the design must be considered unfeasible. Here, $\hat{I}_L$ is the peak converter current estimated by $\sqrt{2}\,\bar{P}_m/\left(\sqrt{3}N_c V_{ll}\right)$ and $\sigma_f$ is the fringe field factor. In this work, $\sigma_f$ is calculated using the conformal Schwarz-Christoffel transformation as described in [5.8]-[5.9].

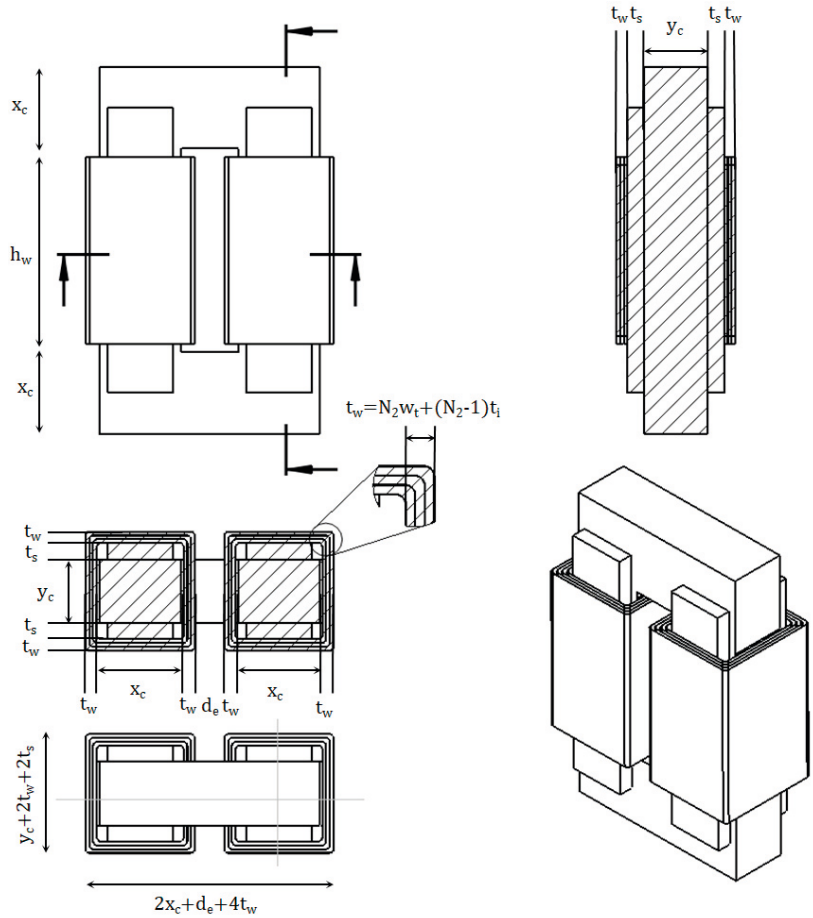



Figure 5.2: Overview of single phase line inductor used to implement converter side inductor $L_2$. The thickness of the foil has been exaggerated for clarity.

$$N_2 = \sqrt{\frac{\sigma_f L_2 g}{2\mu_0 x_c y_c}} \tag{5.1}$$

$$\hat{B} = \frac{L_2 \hat{I}_L}{2N_2 x_c y_c} \leq B_{max} \tag{5.2}$$

With the active rectifier operated at $f_{sw,AFE}$, the foil thickness is selected according to $w_t \leq \delta_s/2$ in order to minimize the losses associated with the skin and proximity

effects. Hence, with winding current density $J$, the foil height is set by (5.3). At this point, the complete geometry depicted in Figure 5.2 is defined.

$$h_w = \frac{\hat{I}_L/\sqrt{2}}{Jw_t} \tag{5.3}$$

In operation, power is dissipated in the inductor windings as well as in the inductor magnetic core. Here, it must be ensured that the hot-spot temperature of the inductor coil does not exceed the rating of the chosen winding material. To allow use of the developed models in a design optimization procedure, a simplified thermal network derived from the geometry in Figure 5.2 is utilized. Noting that the structure of the inductor is highly symmetrical and assuming that the generated core and winding losses are uniformly distributed throughout the respective media, it is sufficient to model only one eighth of the inductor geometry, Figure 5.3. Based on physical reasoning and evaluation of the depicted thermal resistances for typical cases, it is clear that the hot-spot temperature will be found towards the middle of the inductor coil inside the winding window. Here, a simplified worst case representation is obtained by assuming zero natural convection and that the generated losses associated with the hot-spot must be conducted through the coil to the heat sink, Figure 5.3.b.

In this representation, the thermal resistances are given by (5.4)-(5.6), the generated coil and core losses by (5.7)-(5.8), and the denoted network temperatures by (5.9)-(5.11). If the basic constraints $\hat{B} \leq B_{max}$ and $\theta_s \leq \theta_{max}$ are satisfied, the design may be considered feasible. In these equations, $\lambda_{cu}$ is the thermal resistivity of copper, $\lambda_p$ is the equivalent thermal resistivity of layered copper foil and isolating material, $h_c$ is the heat transfer coefficient, $\bar{P}_{cu}$ are the average copper losses, $\bar{P}_{fe}$ are the average magnetic core losses, $\rho_{cu}$ is the density of copper, and $\rho_{fe}$ is the density of the magnetic material.

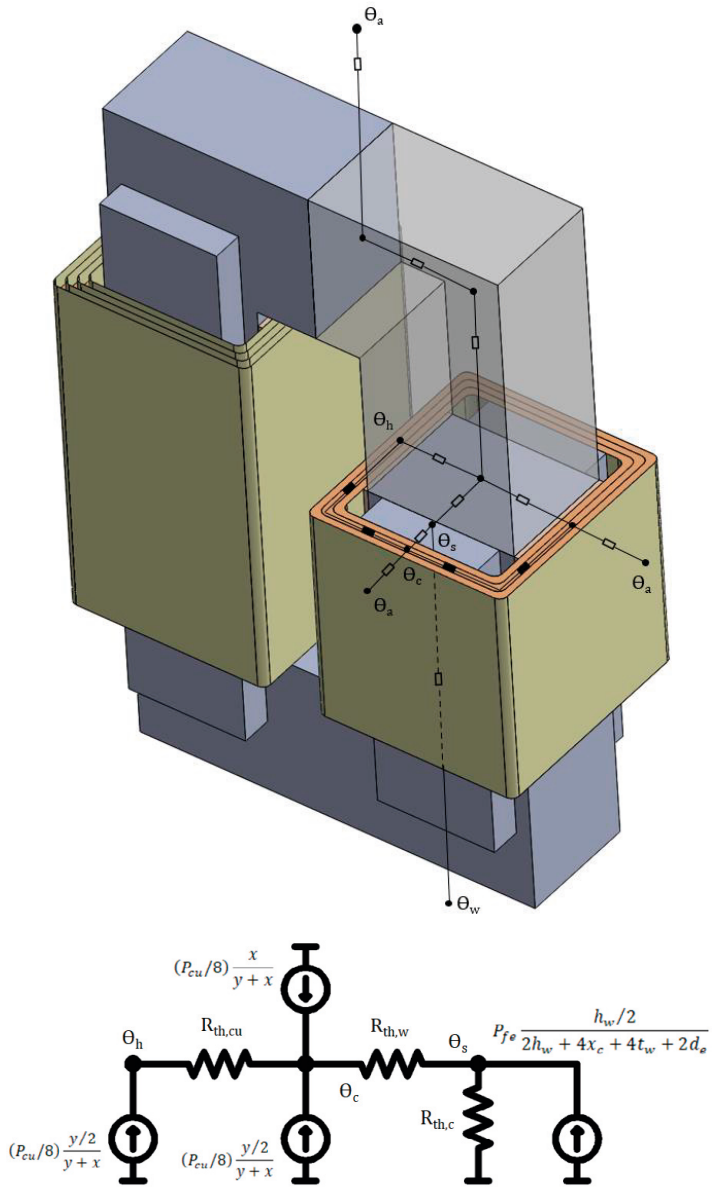



Figure 5.3: Thermal model of single-phase inductor. Symmetry allows modeling of one eight of the inductor geometry. The thickness of the winding foil has been exaggerated for clarity- a) single phase inductor geometry with thermal resistances indicated, b) simplified thermal network for evaluation of worst case scenario.

$$R_{th,cu} = \frac{1}{\lambda_{cu}} \frac{y_c/2 + t_s + t_w + x_c/2}{h_w(N_2 w_t)} \tag{5.4}$$

$$R_{th,w} = \frac{1}{\lambda_p} \frac{t_w/2}{x_c h_w} \tag{5.5}$$

$$R_{th,c} = \frac{1}{h_c} \frac{1}{A_c} \tag{5.6}$$

$$\begin{aligned} \bar{P}_{cu} &= \rho_{cu} F J^2 V_{cu} \\ &= \rho_{cu} F J^2 (2 h_w N_2 w_t [2(x_c + 2t_w/2) + 2(y_c + 2t_s + 2t_w/2)]) \end{aligned} \tag{5.7}$$

$$\begin{aligned} \bar{P}_{fe} &= \rho_{fe} V_{fe} P_{fe,0} \\ &= \rho_{fe} \left(2(x_c y_c h_w) + 2\big(x_c y_c (2x_c + 2w_t + d_e)\big)\right) P_{fe,0} \end{aligned} \tag{5.8}$$

$$\theta_w = \theta_s + \frac{\bar{P}_{cu} + \bar{P}_{fe}}{8} R_{th,c} \tag{5.9}$$

$$\theta_c = \theta_s + (\bar{P}_{cu}/8) R_{th,w} \tag{5.10}$$

$$\theta_h = \theta_c + (\bar{P}_{cu}/8) \frac{y_c/2}{x_c + y_c} R_{th,cu} \tag{5.11}$$

Finally, the losses and volume of the three resulting single-phase inductors implementing $L_2$ are given by (5.12)-(5.13). The design procedure is summarized in the chart depicted in Figure 5.4.

$$\bar{P}_{L2} = 3\big(\bar{P}_{cu} + \bar{P}_{fe}\big) \tag{5.12}$$

$$V_{L2} = 3 W_{L2} H_{L2} D_{L2} = \begin{Bmatrix} W_{L2} = & 2x_c + 4t_w + d_e \\ H_{L2} = & h_w + 2x_c + 2d_i \\ D_{L2} = & y_c + 2t_w + 2t_s \end{Bmatrix} \tag{5.13}$$

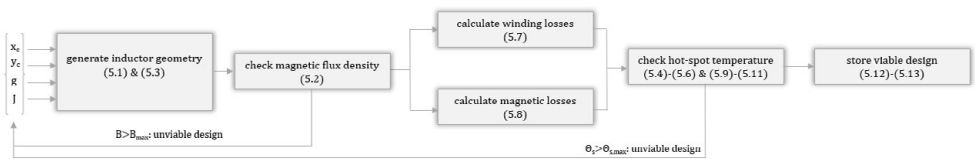



Figure 5.4: Evaluation procedure for single phase inductors implementing converter-side inductor $L_2$

*Grid-side inductor*

The grid-side inductor $L_1$ is implemented as a single three phase inductor. Importantly, if multiple input charger systems are used in parallel, $L_1$ may be common to all chargers in providing line current ripple cancellation and thus lowering the requirements on the remaining components (i.e., the filter values required to obtain the necessary attenuation). As noted, in this work $L_1$ is chosen as a direct function of $L_2$. Here, a magnetic structure based on double E laminations and foil windings is appropriate. In this work, water cooling is implemented by affixing a cooling plate in-between the magnetic core and the innermost foil winding layer, Figure 5.5. With the three windings placed on a common magnetic structure, the constitutive equation of the inductor is conveniently written on the inductance matrix form, (5.14). Considering a balanced three-phase circuit, i.e. $i_R(t) + i_S(t) + i_T(t) = 0$, and the winding configuration shown in Figure 5.5, i.e., ideally $L_R = L_S = L_T = L$ and $M_{RS} = M_{RT} = M_{ST} = M$, (5.15) describes the inductor modeled by (5.14) in differential mode. From Figure 5.5, it is seen that $M = -L/2$, i.e., from a differential mode circuit perspective, the three-phase inductor may be seen as three individual inductors with self-inductance $1.5L$. It is pointed out that, neglecting leakage fields, the corresponding common mode inductance of this configuration is zero which is the main reason why single-phase inductors were preferred for the converter-side inductor, above.

$$v_L = L\frac{di_L}{dt} \rightarrow \begin{bmatrix} v_{L,R} \\ v_{L,S} \\ v_{L,T} \end{bmatrix} = \begin{bmatrix} L_R & M_{RS} & M_{RT} \\ M_{RS} & L_S & M_{ST} \\ M_{RT} & M_{ST} & L_T \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{L,R} \\ i_{L,S} \\ i_{L,T} \end{bmatrix} \tag{5.14}$$

$$\begin{aligned} \begin{bmatrix} v_{L,R} \\ v_{L,S} \\ v_{L,T} \end{bmatrix}_{DM} &= \begin{bmatrix} L-M & 0 & 0 \\ 0 & L-M & 0 \\ 0 & 0 & L-M \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{L,R} \\ i_{L,S} \\ i_{L,T} \end{bmatrix}_{DM} \\ &= \frac{3}{2} \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{L,R} \\ i_{L,S} \\ i_{L,T} \end{bmatrix}_{DM} \end{aligned} \tag{5.15}$$

For $\mu_r \gg \mu_0$, the magnetic reluctance of the inductor core legs $R_L$ is well approximated by the magnetic reluctance of the air gap $R_G$, (5.16). Hence, with the per-phase inductance $L_1$ determined in accordance with the above and considering core leg width $x_c$, the core depth $y_c$, the per air gap length $g$ and the winding current density $J$ as fundamental design parameters, the required number of winding turns may be calculated according to (5.17). Then, the corresponding peak magnetic flux density $\hat{B}$ may be calculated and compared against the maximum allowable peak magnetic flux density $B_{max}$, (5.18). If $\hat{B} > B_{max}$, the design must be considered

unfeasible. Here, $\hat{I}_1$ is the peak modulator input current estimated by $\sqrt{2}\,\bar{P}_m/\left(\sqrt{3}V_{ll}\right)$ and $\sigma_f$ is the fringe field factor. Again, $\sigma_f$ is here calculated using the conformal Schwarz-Christoffel transformation as described in [5.8]-[5.9].

$$R_L \approx R_G = \sigma_f \frac{1}{\mu_0} \frac{g}{x_c y_c} \tag{5.16}$$

$$N_2 = \sqrt{\frac{L_1 \left(\frac{R_G^2}{2R_G} + R_G\right)}{3/2}} \tag{5.17}$$

$$\hat{B} = \frac{L_1 \hat{I}_m}{N_2 x_c y_c} \leq B_{max} \tag{5.18}$$

Again, with the active rectifier operated at $f_{sw,AFE}$, the foil thickness is selected according to $w_t \leq \delta_s/2$ in order to minimize the losses associated with the skin and proximity effects. Hence, with winding current density $J$, the foil height is set by (5.19). At this point, the complete geometry depicted in Figure 5.5 is defined.

$$h_w = \frac{\hat{I}_m/\sqrt{2}}{J w_t} \tag{5.19}$$

In operation, power is dissipated in the inductor windings as well as in the inductor magnetic core. Here, it must be ensured that the hot-spot temperature of the inductor coil does not exceed the rating of the chosen winding material. Again, a simplified thermal network derived from the geometry in Figure 5.5 is utilized. Applying the reasoning presented in the preceding section, it is clear that 1) the windings are essentially thermally isolated from one another, and that 2) the hot-spot temperature will be found in the middle inductor coil inside the winding window. Hence, it is sufficient to model only one eighth of a single inductor winding, Figure 5.6. As with the single-phase inductor, a simplified worst case representation is obtained by assuming zero natural convection and that the generated losses associated with the hot-spot must be conducted through the coil to the heat sink, Figure 5.6.b.

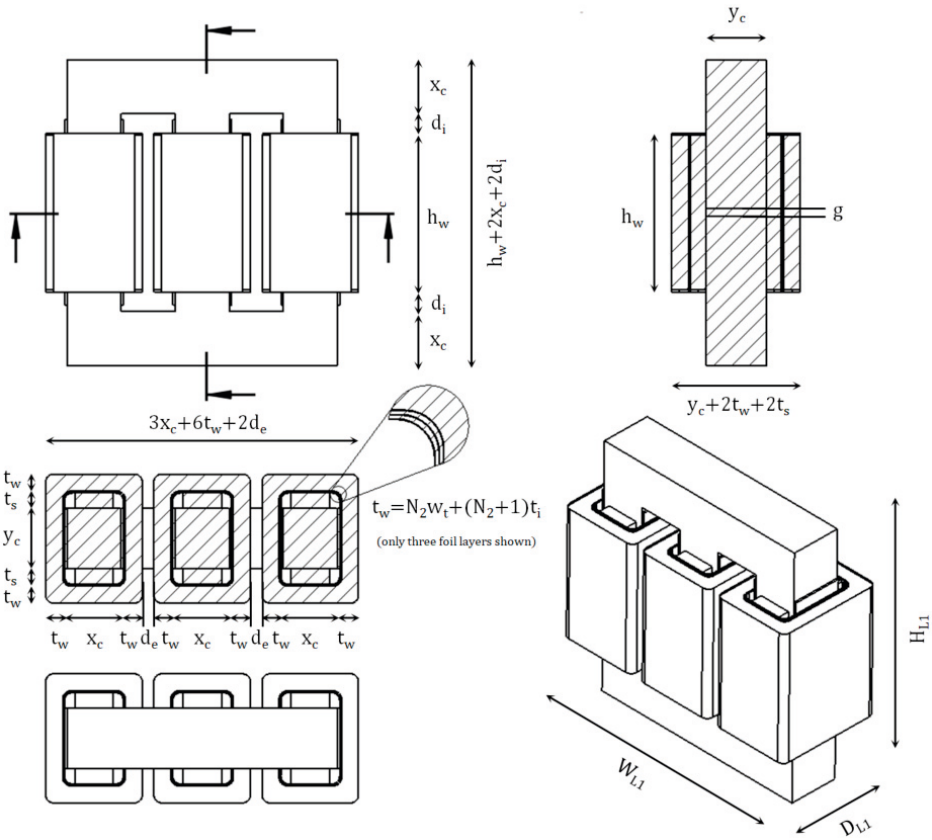



Figure 5.5: Overview of three-phase inductor implementing grid-side inductor $L_1$. Only the three innermost layers of the foil windings are shown in detail.

In this representation, the thermal resistances are given by (5.20)-(5.22), the generated coil and core losses per leg by (5.23)-(5.24), and the denoted network temperatures by (5.25)-(5.27). If the basic constraints $\hat{B} \leq B_{max}$ and $\theta_s \leq \theta_{max}$ are satisfied, the design may be considered feasible. In these equations, $\lambda_{cu}$ is the thermal resistivity of copper, $\lambda_p$ is the equivalent thermal resistivity of layered copper foil and isolating material, $h_c$ is the heat transfer coefficient, $\bar{P}_{cu}$ are the average copper losses, $\bar{P}_{fe}$ are the average magnetic core losses, $\rho_{cu}$ is the density of copper, and $\rho_{fe}$ is the density of the magnetic material.

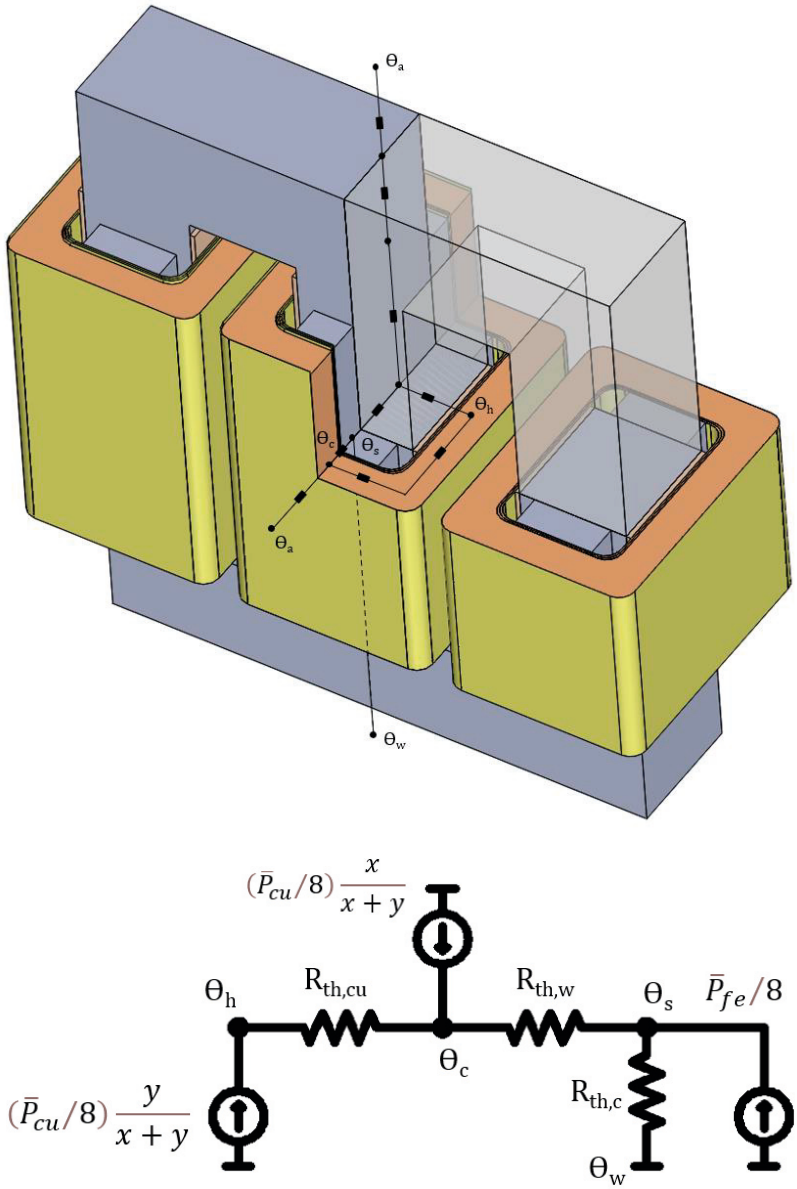



Figure 5.6: Thermal model for three-phase inductor implementing grid-side inductor $L_1$. Only the three innermost layers of the foil windings are shown in detail.

$$R_{th,cu} = \frac{1}{\lambda_{cu}} \frac{y_c/2 + t_s + t_w + x_c/2}{h_w(N_2 w_t)} \tag{5.20}$$

$$R_{th,w} = \frac{1}{\lambda_p} \frac{t_w/2}{h_w\, x_c/2} \tag{5.21}$$

$$R_{th,c} = \frac{1}{h_c} \frac{1}{A_c} \tag{5.22}$$

$$\begin{aligned} \bar{P}_{cu} &= \rho_{cu} F J^2 V_{cu} \\ &= \rho_{cu} F J^2 (2 h_w N_2 w_t [2(x_c + 2t_w/2) + 2(y_c + 2t_s + 2t_w/2)]) \end{aligned} \tag{5.23}$$

$$\bar{P}_{fe} = \rho_{fe} V_{fe} P_{fe,0} = \rho_{fe} \left( x_c y_c h_w + 2\big(x_c y_c (x_c + 2w_t + d_e/2)\big)\right) P_{fe,0} \tag{5.24}$$

$$\theta_s = \theta_w + \frac{\bar{P}_{cu} + \bar{P}_{fe}}{8} R_{th,c} \tag{5.25}$$

$$\theta_c = \theta_s + (\bar{P}_{cu}/8) R_{th,w} \tag{5.26}$$

$$\theta_h = \theta_c + (\bar{P}_{cu}/8) \frac{y_c/2}{x_c + y_c} R_{th,cu} \tag{5.27}$$

Finally, the losses and volume of the resulting three phase inductor implementing $L_1$ are given by (5.28)-(5.29). The design procedure is summarized in the chart depicted in Figure 5.7.

$$\bar{P}_{L1} = 3\big(\bar{P}_{cu} + \bar{P}_{fe}\big) \tag{5.28}$$

$$V_{L1} = W_{L1} H_{L1} D_{L1} = \begin{Bmatrix} W_{L1} = & 3x_c + 6t_w + 2d_e \\ H_{L1} = & h_w + 2x_c + 2d_i \\ D_{L1} = & y_c + 2t_w + 2t_s \end{Bmatrix} \tag{5.29}$$

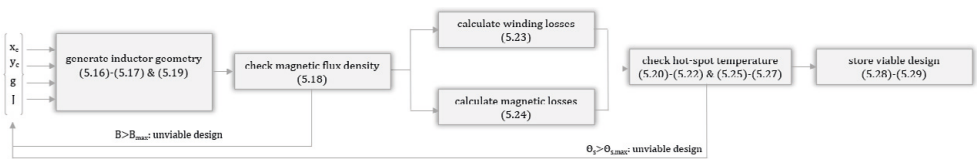



Figure 5.7: Evaluation procedure for single phase inductors implementing converter-side inductor $L_2$

### 5.2.4 Filter capacitors

The converter-side inductor $L_2$ was selected to limit the peak-to-peak current ripple and the grid-side inductor $L_1$ was selected in proportion to $L_2$. Now, the filter capacitors must be selected to ensure proper harmonic attenuation in accordance with applicable standards.

Here, an appropriate design may be found by considering a simplified per-phase high frequency representation of the filter circuit, Figure 5.8. In this circuit, the current source represents the total current harmonics generated by the $N_c$ active rectifier circuits. As $N_c$, $f_{sw,AFE}$ and $L_1$ are known, the required $C_1$ can be calculated such that the part of the harmonic current emitted to the grid is limited to the prescribed limits, as follows.

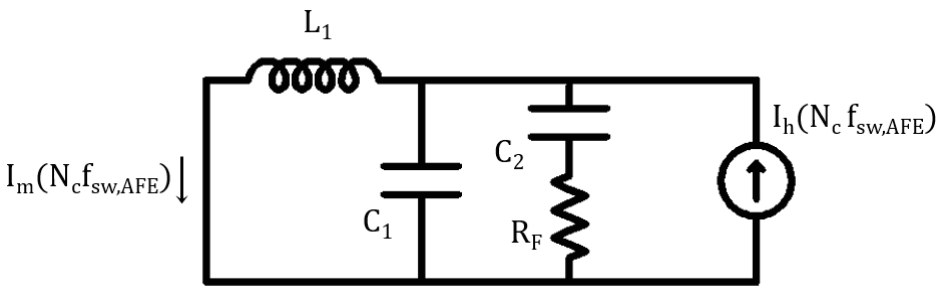



Figure 5.8: Simplified filter circuit

To begin, the resulting worst case line current component at the effective switching frequency $N_c f_{sw,AFE}$ is estimated according to (5.30). Here, $\left|I_h\left(N_c f_{sw,AFE}\right)\right| \approx k_{L2} I_L/(2N_c)$ are the worst-case total generated converter current harmonics evaluated at $N_c f_{sw,AFE}$ as set by $L_2$. Assuming operation along the high frequency asymptote simplifies calculation of $C_1$ but is not necessary.

$$\begin{aligned} I_m\left(N_c f_{sw,AFE}\right) &= I_h\left(N_c f_{sw,AFE}\right) \frac{1/(sL_1)}{1/(sL_1) + sC_1 + 1/(1/(sC_2) + R_F)} \\ \rightarrow \left|I_M\left(N_c f_{sw,AFE}\right)\right| &= \left|\frac{I_L\left(f_{sw,AFE}\right)}{N_c} \frac{1}{1 + s^2 L_1 C_1}\right| \approx \left|\frac{k_{L2} I_L}{2N_c} \frac{1}{s^2 L_1 C_1}\right| \end{aligned} \tag{5.30}$$

Then, the total harmonic distortion (THD) of the line current is defined according to (5.31). Here, the generated harmonics will appear centred around $km_f$, where $m_f$ is the modulation frequency ratio $N_c f_{sw,AFE}/f_g$ and $k$ is a positive non-zero integer,

[5.10]. Hence, with proper attenuation, $I_{m,[1\cdot(N_c\cdot f_{sw}/f_g)]} \gg I_{m,[2\cdot(N_c\cdot f_{sw}/f_g)]} \gg \cdots$, i.e., the THD may be approximated by $\left|I_{m,1(N_c\cdot f_{sw}/f_g)}\right|/\hat{I}_m$.

$$THD(I_m) = \frac{\sqrt{I_{m,2}^2 + I_{m,3}^2 + \cdots + I_{m,n}^2}}{\hat{I}_m} \approx \frac{\left|I_{m,[1\cdot(N_c\cdot f_{sw,AFE}/f_g)]}\right|}{\hat{I}_m} \tag{5.31}$$

Hence, $C_1$ may be calculated directly by combining (5.30)-(5.31) using the effective active rectifier switching frequency at the line $N_c f_{sw,AFE}$, the grid-side inductance value $L_1$, the maximum allowable converter side ripple (by way of $k_{L2}$), and the maximum allowable line side THD as prescribed by the applicable standard, (5.32).

$$\begin{aligned} \left|I_{m,[1\cdot(N_c\cdot f_{sw,AFE}/f_g)]}\right| &= \left|I_M\left(N_c f_{sw,AFE}\right)\right| = \left|\frac{k_{L2} I_L}{2N_c}\frac{1}{s^2 L_1 C_1}\right| \\ &= \hat{I}_m THD_{max} \\ \rightarrow C_1 &= \left|\frac{k_{L2}}{2N_c^2\left(2\pi f_{sw,AFE}\right)^2 L_1 THD_{max}}\right| \end{aligned} \tag{5.32}$$

Finally, $C_2$ is set in proportion to $C_1$ and $R_F$ is selected in a trade-off between damping and filter losses. In this work, $C_1$ and $C_2$ are dimensioned using the capacitor selection procedure developed in Appendix A. Here, it is typically assumed that for practical reasons $C_1$ and $C_2$ will be implemented using the same capacitor reference.

### 5.2.5 Power stack

The input side power stack consists of a three-phase voltage source converter, used as active rectifier, and a current controlled dc/dc converter sharing a common dc-link, Figure 5.9. Here, it is convenient to integrate the power stack as a single unit where the two converters share a heat sink. Furthermore, it is desirable that a single IGBT type is used to reduce the number of spare parts.

Design comes down to selecting an appropriate IGBT module and an appropriate number of parallel modules per converter arm such that the system efficiency is maximized. Here, a slightly altered version of the design procedure described in Appendix B is used.

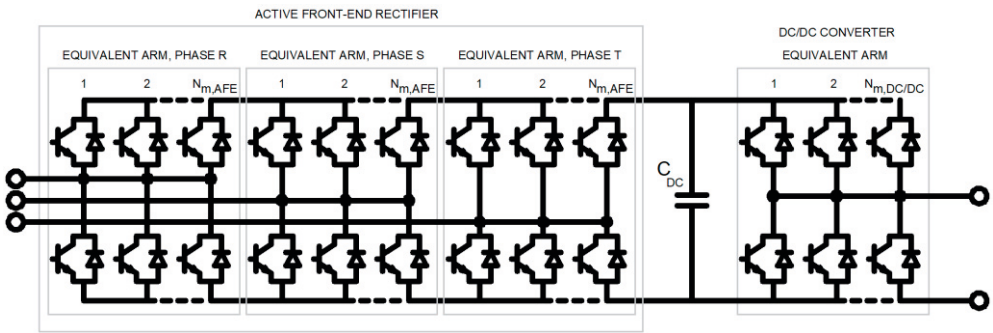



Figure 5.9: Overview of power stack

*DC-link capacitor*

The DC-link capacitor is common to the active rectifier and the DC/DC converter and must be designed for 1) operation at the system primary voltage (in this work, the primary voltage has been fixed to around 1 kV to allow use of 1.7 kV standard off-the-shelf semiconductor components), and 2) to limit the voltage ripple on the DC bus. In modulator applications, hold-up time is generally not an important consideration, i.e., the DC bus voltage ripple is entirely related to the instantaneous power difference between the input and output during the switching period. Generally speaking, a complete analysis requires consideration of the operation of both converters simultaneously in deriving the worst-case DC-link voltage ripple. However, noting that 1) typically $f_{sw,DC/DC} > f_{sw,AFE}$, that 2) typically $L_{dc} \gg L_2$, and that 3) the operational and average duty cycle of the DC/DC converter is between 0.8-0.95 whereas the duty cycle of the active rectifier switches repeatedly varies from 0 to 1, it is understood that it is sufficient to consider only active rectifier operation (i.e., in analysis replacing the DC/DC converter with an ideal current source) in sizing the DC-link capacitor. Under this assumption, the resulting ripple is a function of the chosen DC-link capacitance, the modulation index, the utilized modulation technique, the switching frequency and the converted power.

[5.11] reports a study on DC-link voltage ripple in voltage source inverters used in motor applications. There, the DC-link capacitor under consideration was placed in-between a current source (ideal voltage source with stray inductance) and an ideal balanced three-phase (motor) load. Of course, this examination is entirely reversible (flipping the signs of the currents does not affect the absolute value of the voltage ripple) leading to the same absolute peak-to-peak voltage ripple. The minimum DC-link capacitance is derived as a function of the converter current, the converter switching frequency, the maximum allowable peak-to-peak voltage ripple, (5.33). Here, $k_r$ is the maximum voltage ripple coefficient, and is a function of the

modulation index, the modulation technique, and the power factor. Assuming PWM-based switching with sinusoidal references, ideal power factor (in accordance with the above) and worst-case modulation index ($m = 0.5$), the maximum voltage ripple coefficient $k_r = 0.1875$, [5.11].

$$i_c = C\frac{dv_c}{dt} \rightarrow C_{dc} \geq k_r \frac{\hat{I}_m / N_c}{f_{sw,AFE}(\Delta V_{dc})_{p-p}} \tag{5.33}$$

In this work, $(\Delta V_{dc})_{p-p}$ is set to, e.g., 1% of $V_{dc}$ and the derived capacitance is turned into an appropriate capacitor configuration using the capacitor selection procedure outlined in Appendix A. Here, as the DC-link capacitor and the two power converters are conveniently integrated in a single unit, the capacitor reference minimizing the total power stack volume may be considered optimal.

*Common mode mitigation*

Basic circuit operation of the active rectifier component was discussed in section 3.2.2. It is well known that such S-PWM operation generates a common mode voltage component on the dc-link bus as documented in, e.g., [5.12]-[5.13]. Figure 5.10 shows an example of this. As can be seen, this voltage has a high dv/dt and is repeated at the switching frequency. Taking into account parasitic elements, this may correspond to significant common mode circulating currents through the ground which must be limited Here, it is desirable to add a mitigating component such that the current is contained to the power converter itself, eliminating or minimizing propagation to the load side or to other equipment and related effects.

A common technique used to stabilize the voltage on the dc-link bus is to connect the neutral point of the line filter to the middle point of the dc-link. This technique is discussed in [5.12]-[5.13]. Denoting the resulting common mode voltage as (5.34), and the associated common mode circulating current as (5.35), it was shown in, e.g., [5.13], that the system may be analysed from a common mode perspective using the equivalent circuit shown in Figure 5.11.a. This may then be reduced to that shown in Figure 5.11.b. Here, $C_{cm}$ should be chosen such that the resonance frequency of the equivalent circuit is well below that of $N_c f_{sw,AFE}$. Usually, $C_{cm} \approx C_1$ is an appropriate choice.

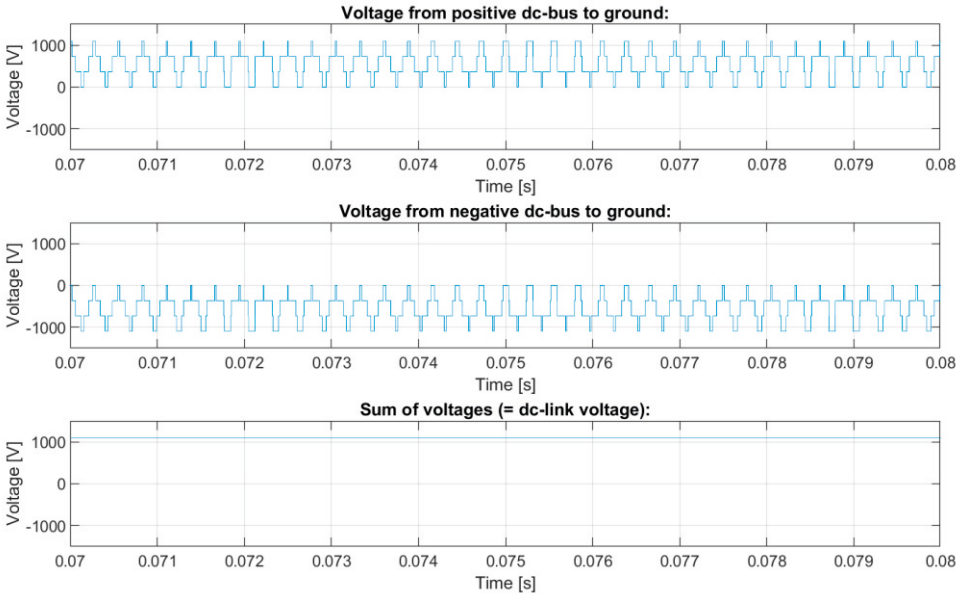



Figure 5.10: Common mode voltage in SPWM operation of three-phase voltage source converter

$$v_{cm,AFE} = \left(\frac{v_{R-g} + V_{S-g} + V_{T-g}}{3}\right) \tag{5.34}$$

$$i_{cm,AFE} = i_R + i_S + i_T \tag{5.35}$$

Importantly, given proper capacitor selection, the voltage across the equivalent capacitor element is essentially constant. Hence, the peak-to-peak CM current ripple may be estimated from (5.36).

$$i_{cm,p-p} = \sim \frac{V_{dc}/2}{(L_2/3) \cdot (3f_{sw})} = \frac{V_{dc}/2}{L_2 f_{sw}} \tag{5.36}$$

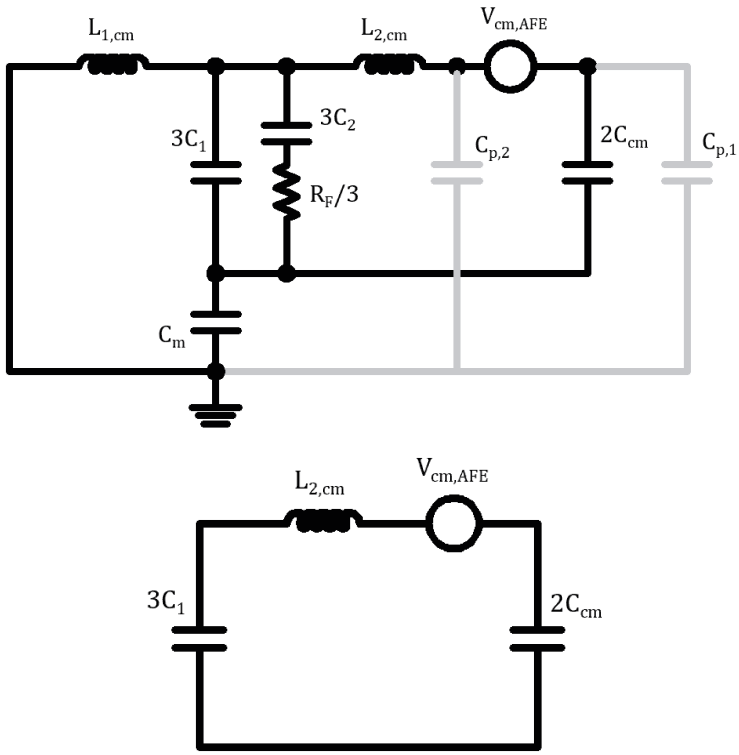



Figure 5.11: Equivalent circuit for common mode analysis of active rectifier system: a) full equivalent circuit, b) reduced equivalent circuit

An example – as will be elaborated in later chapters – the ESS SML klystron modulators were designed for $V_{dc} = 1.1\ kV$, $L_2 = 600\ \mu H$ and $f_{sw} = 3.6\ kHz$, which with $C_{cm} = \sim 100\ \mu H$ yields a per-system common mode current of $\sim 80\ A_{rms}$. Note the agreement with the estimate provided by (5.36). It is here pointed out that, in this example, interleaving three charger systems further reduces the RMS value of the added circulation current to below 30 A, representing less than 1% of the total RMS current. From the perspective of losses and modulator efficiency, this addition may be considered to be negligible. In the context of this work, the resulting capacitor is selected using the capacitor selection scheme discussed in Appendix A.

*Estimation of active rectifier losses*

The loss estimation of the active rectifier circuit is largely based on the methods outlined in, e.g., [5.14]-[5.15] and is summarized in the following. Here, semiconductor switching times are assumed to be negligible (approaching zero) and $f_{sw,AFE} \gg f_g$ such that the line current ripple may be neglected. Furthermore, only

linear modulation is considered. The active rectifier waveforms were earlier shown in Figure 3.8 and the underlying control principle is described in detail in chapter 7.

The modulation index, (5.37), is the ratio between the amplitude of the fundamental harmonic of the converter output voltage and half the dc-link voltage. As outlined in chapter 7, each modulator phase current is controlled to be in phase with the corresponding modulator phase voltage such that the associated reactive power is minimized, i.e., $cos(\varphi) = -1$.

$$m = \frac{V_{LL}\sqrt{2/3}}{V_{dc}/2} \tag{5.37}$$

As pointed out in [5.14], given the symmetry of the active rectifier circuit, the voltage and current waveforms of the rectifier legs will be identical though phase shifted, i.e., it is sufficient to consider the behaviour of a single switch and multiply the estimated power dissipation by the number of converter switches. Considering that both the IGBT forward voltage drop (through the current) and the rectifier leg duty cycle (through the modulation) vary sinusoidally over the fundamental period, the IGBT conduction losses may be estimated according to (5.38), [5.14] and [5.15].

$$\begin{aligned} P_{IGBT,AFE,c} &= \left(\frac{1}{2\pi} + \frac{mcos(\Phi)}{8}\right)\left(\frac{\hat{I}_L}{N_{m,AFE}}\right)V_{ce,0} \\ &+ \left(\frac{1}{8} + \frac{mcos(\Phi)}{3\pi}\right)\left(\frac{\hat{I}_L}{N_{m,AFE}}\right)^2 r_{ce} \end{aligned} \tag{5.38}$$

Then, under the assumption that the switching losses generated during a sinusoidal half wave are approximately equal to the switching losses generated by the equivalent DC current (i.e., the average value of the half wave current) and that $K_{i,IGBT} \approx 1$, the IGBT switching losses may be estimated according to (5.39).

$$\begin{aligned} P_{IGBT,AFE,sw} &= f_{sw,AFE} \\ &\cdot \left(E_{on} + E_{off}\right)\left(\frac{\sqrt{2}}{\pi}\frac{\hat{I}_L/\sqrt{2}/N_{m,AFE}}{I_{c,ref}}\right)^{K_{i,IGBT}}\left(\frac{V_{dc}}{V_{cc,ref}}\right)^{K_{v,IGBT}} \end{aligned} \tag{5.39}$$

The same reasoning may be applied to the anti-parallel rectifier diode, whose conduction and switching losses are then estimated by (5.40) and (5.41), respectively.

$$P_{diode,AFE,c} = \left(\frac{1}{2\pi} - \frac{mcos(\Phi)}{8}\right)\left(\frac{\hat{I}_L}{N_{m,AFE}}\right)V_{f,0} + \left(\frac{1}{8} - \frac{mcos(\Phi)}{3\pi}\right)\left(\frac{\hat{I}_L}{N_{m,AFE}}\right)^2 r_f \tag{5.40}$$

$$P_{diode,AFE,sw} = f_{sw,AFE}E_{rr}\left(\frac{\sqrt{2}}{\pi}\frac{\hat{I}_L/\sqrt{2}/N_{m,AFE}}{I_{c,ref}}\right)^{K_{i,diode}}\left(\frac{V_{dc}}{V_{cc,ref}}\right)^{K_{v,diode}} \tag{5.41}$$

In estimating the thermal performance of the active rectifier power modules, it is convenient to write the total IGBT and diode losses according to (5.42) and (5.43), respectively. The total active rectifier losses are obtained by multiplying the sum of (5.42) and (5.43) by the number of IGBTs in the active rectifier circuit, i.e., $6N_{m,AFE}$, (5.44). Finally, the active rectifier efficiency is given by (5.45).

$$\sum P_{IGBT,AFE} = P_{IGBT,AFE,c} + P_{IGBT,AFE,sw} \tag{5.42}$$

$$\sum P_{diode,AFE} = P_{diode,AFE,c} + P_{diode,AFE,sw} \tag{5.43}$$

$$\sum P_{AFE} = 6N_{m,AFE}\left(\sum P_{IGBT,AFE} + \sum P_{Diode,AFE}\right) \tag{5.44}$$

$$\eta_{AFE} = \frac{P - \sum P_{AFE}}{P} \tag{5.45}$$

*Estimation of DC/DC converter losses*

The loss estimation of the DC/DC converter circuit is standard practice and is summarized in the following. The DC/DC converter waveforms were earlier shown in Figure 3.9 and the underlying control principle is described in detail in chapter 7. Charging the capacitor bank with constant power, the current increases linearly through the pulse event duration $T_p$ and decreases correspondingly throughout the off period $1/f_r - T_p$. For a typical capacitor bank voltage droop of ~15%, the current waveform will exhibit the same variation. Hence, from the perspective of

converter loss estimation, the current is well represented by its average value $I_{DC}$. Considering the average converter duty cycle $\bar{\delta}_c$, the average losses per power module are given for the conducting IGBT, (5.46)-(5.47), and the conducting diode, (5.48)-(5.49). From this, the total DC/DC converter losses and the corresponding converter efficiency are calculated according to (5.50)-(5.51).

$$P_{IGBT,DC/DC,c} = \left[\left(\frac{I_{DC}}{N_{m,DC/DC}}\right)V_{ce,0} + \left(\frac{I_{DC}}{N_{m,DC/DC}}\right)^2 r_{ce}\right]\bar{\delta}_c \tag{5.46}$$

$$P_{IGBT,DC/DC,sw} = f_{sw,DC/DC}\begin{pmatrix} E_{on} \\ +E_{off} \end{pmatrix}\left(\frac{I_{DC}/N_{m,DC/DC}}{I_{c,ref}}\right)^{K_{i,IGBT}}\left(\frac{V_{dc}}{V_{cc,ref}}\right)^{K_{v,IGBT}} \tag{5.47}$$

$$P_{diode,DC/DC,c} = \left[\left(\frac{I_{DC}}{N_{m,DC/DC}}\right)V_{f,0} + \left(\frac{I_{DC}}{N_{m,DC/DC}}\right)^2 r_f\right]\left(1-\bar{\delta}_c\right) \tag{5.48}$$

$$P_{diode,DC/DC,sw} = f_{sw,DC/DC}E_{rr}\left(\frac{I_{DC}/N_{m,DC/DC}}{I_{c,ref}}\right)^{K_{i,diode}}\left(\frac{V_{dc}}{V_{cc,ref}}\right)^{K_{v,diode}} \tag{5.49}$$

$$\sum P_{DC/DC} = N_{m,DC/DC}\begin{pmatrix} P_{IGBT,DC/DC,c} + P_{IGBT,DC/DC,sw} + P_{diode,DC/DC,c} \\ +P_{diode,DC/DC,sw} \end{pmatrix} \tag{5.50}$$

$$\eta_{DC/DC} = \frac{P - \sum P_{AFE} - \sum P_{DC/DC}}{P - \sum P_{AFE}} \tag{5.51}$$

*Thermal network*

In the preceding two sections, the input stage power stack losses have been estimated. As noted, the power modules comprising the active rectifier and the DC/DC converter are to be placed on a common heat sink. Figure 5.12 depicts an equivalent thermal network with $6N_{m,AFE}$ loss sources set up according to (5.37)-(5.44) and $N_{m,DC/DC}$ loss sources setup according to (5.46)-(5.50). Again, as the generated average losses and module properties are assumed to be identical, it is only necessary to consider the details of a single power module in each converter. Then, as noted, all loss sources are connected to a common heat sink with an assumed equivalent temperature $\Theta_s$. The heat sink is water cooled, and is represented by a common thermal resistance $R_{th,s-a}$ connecting to the coolant water temperature $\Theta_a$.

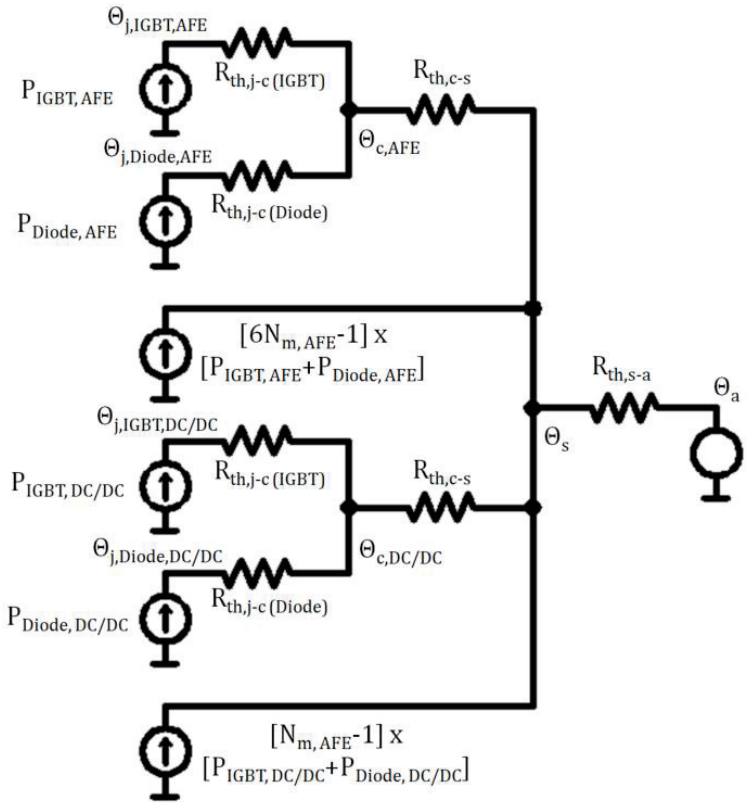



Figure 5.12: Thermal network for power stack

Using (5.44) and (5.50), above, the total power stack losses are given by (5.52). With this, the common heat sink temperature is estimated according to (5.53).

$$\sum P_{stack} = \sum P_{AFE} + \sum P_{DC/DC} \tag{5.52}$$

$$\theta_s = \theta_a + \sum P_{stack}\, R_{th,s-a} \tag{5.53}$$

Then, the junction temperature of the IGBT and diode in the power modules comprising the active rectifier and DC/DC converters may be estimated using (5.54)-(5.57).

$$\theta_{j,IGBT,AFE} = \theta_s + \left(\sum P_{IGBT,AFE} + \sum P_{diode,AFE}\right) R_{th,c-s} + \sum P_{IGBT,AFE}\, R_{th,j-c} \tag{5.54}$$

$$\theta_{j,diode,AFE} = \theta_s + \left(\sum P_{IGBT,AFE} + \sum P_{diode,AFE}\right) R_{th,c-s} + \sum P_{diode,AFE}\, R_{th,j-c} \tag{5.55}$$

$$\theta_{j,IGBT,\frac{DC}{DC}} = \theta_s + \left(\sum P_{IGBT,\frac{DC}{DC}} + \sum P_{diode,\frac{DC}{DC}}\right) R_{th,c-s} + \sum P_{IGBT,DC/DC}\, R_{th,j-c} \tag{5.56}$$

$$\theta_{j,diode,\frac{DC}{DC}} = \theta_s + \left(\sum P_{IGBT,\frac{DC}{DC}} + \sum P_{diode,\frac{DC}{DC}}\right) R_{th,c-s} + \sum P_{diode,DC/DC}\, R_{th,j-c} \tag{5.57}$$

*Power stack design*

The active rectifier, the dc/dc converter and the dc-link capacitors are integrated in a single power stack unit as indicated in Figure 5.13. In design, the volume is given by (5.58) and the power stack efficiency is estimated by (5.59). Power stack design for a given combination of $f_{sw,AFE}$ and $f_{sw,DC/DC}$ is summarized in Figure 5.14.

$$V_{stack} = W_{stack} H_{stack} D_{stack} \tag{5.58}$$

$$\eta_{stack} = \eta_{AFE}\eta_{DC/DC} = \frac{P - \sum P_{AFE} - \sum P_{DC/DC}}{P} \tag{5.59}$$

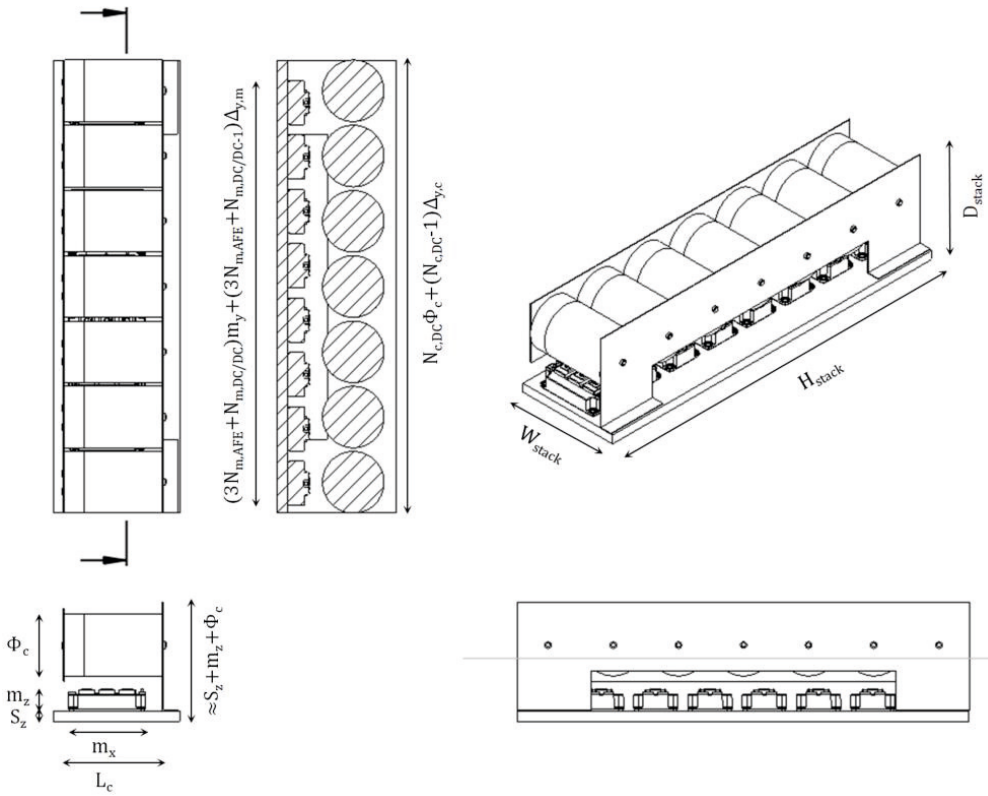



Figure 5.13: Overview of power stack geometry

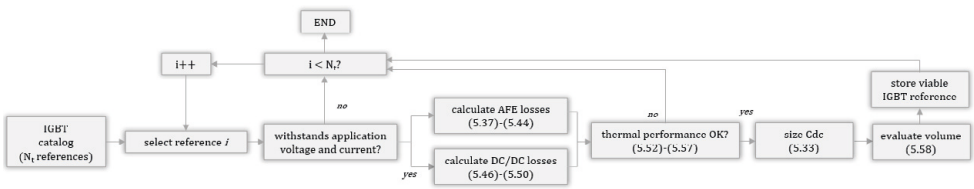



Figure 5.14: Overview of design procedure for input stage power stack

## 5.2.6 DC inductor

The DC/DC converter connects the DC-link to the main capacitor bank through the DC inductor, allowing current control. As noted earlier, the capacitor bank is to be charged with constant power, i.e., the charging current increases linearly through the pulse event duration $T_p$ and decreases correspondingly throughout the off period $1/f_r - T_p$, Figure 3.9. The inductance value $L_{DC}$ is chosen to limit the peak-to-peak converter output current ripple at the worst-case duty cycle. Here, either 1) the

practical worst case duty cycle $\delta(T_p)$ or 2) the theoretical worst case duty cycle (50%) can be used to derive the required inductance.

Again, $L_{DC}$ is implemented by a single-phase inductor based on standard laminated double C core with foil windings. As before, water cooling is implemented by affixing a cooling plate in-between the magnetic core and the innermost foil winding layer as shown in Figure 5.2. Noting that the RMS current experienced by the DC inductor is well estimated by $I_{L,DC} = \frac{P\eta_{stack}}{\frac{(V_1+(V_1-\Delta V))}{2}}$, equations (5.1)-(5.11) may be used to size the inductor. With this, the DC inductor power losses and volume are given by (5.60) and (5.61), respectively.

$$\bar{P}_{L,DC} = 3\left(\bar{P}_{cu} + \bar{P}_{fe}\right) \tag{5.60}$$

$$V_{L,DC} = 3W_{L,DC}H_{L,DC}D_{L,DC} = \begin{Bmatrix} W_{L,DC} = & 2x_c + 4t_w + d_e \\ H_{L,DC} = & h_w + 2x_c + 2d_i \\ D_{L,DC} = & y_c + 2t_w + 2t_s \end{Bmatrix} \tag{5.61}$$

### 5.2.7 Complete optimization procedure for SML input stage

In this section, the design models developed in the preceding sections are integrated in a unified framework for optimization of the complete SML modulator input stage. The complete framework is presented in Figure 5.15 and explained in the following-

As mentioned in the introduction, in this work, the front-end converter switching frequency $f_{sw,AFE}$, the DC/DC converter switching frequency $f_{sw,DC/DC}$, the permissible converter-side ripple current $\Delta i_{L2}$ and the proportionality constant $L_1 = k_{f,L}L_2$ are considered fundamental design parameters. To produce a set of feasible solutions, the full range of combinations of $f_{sw,AFE}$ and $f_{sw,DC/DC}$ are swept. Here, a typical range of $\Delta i_{L2}$ is considered for each value of $f_{sw,AFE}$, in each case yielding the required $L_2$. As depicted, the design of this inductor is treated individually with the magnetic core leg width $x_c$, the magnetic core depth $y_c$, the per-air gap length $g$, and the winding current density $J$ considered to be key design parameters. At this point, either 1) the complete set of line side inductor designs may be stored, or 2) a single inductor design may be chosen based on a pre-defined objective function. Knowing $f_{sw,AFE}$ and $L_2$, the required active front-end modulation index may be calculated. Hence, combined with the selected $f_{sw,DC/DC}$, the complete power stack may be designed. Then, a typical range of $k_{f,L}$ are considered such that $L_1$ may be designed, again with the magnetic core leg width $x_c$, the magnetic core depth $y_c$, the per-air gap length $g$, and the winding current density $J$ considered to be key design parameters. As with $L_2$, either 1) the complete set of dc side inductor designs

may be stored, or 2) a single inductor design may be chosen based on a pre-defined objective function. Finally, the line side filter components and the common mode mitigation capacitance are designed. At this point, all individual charger components have been designed, and constraints are checked to ensure that the complete design(s) is (are) considered feasible. Here, e.g., thermal limitations (on the inductive components and the power stack) and constraints on the resulting line side harmonic distortion are checked. Feasible designs are then scored according to a well-defined objective function and stored for later evaluation and comparison.

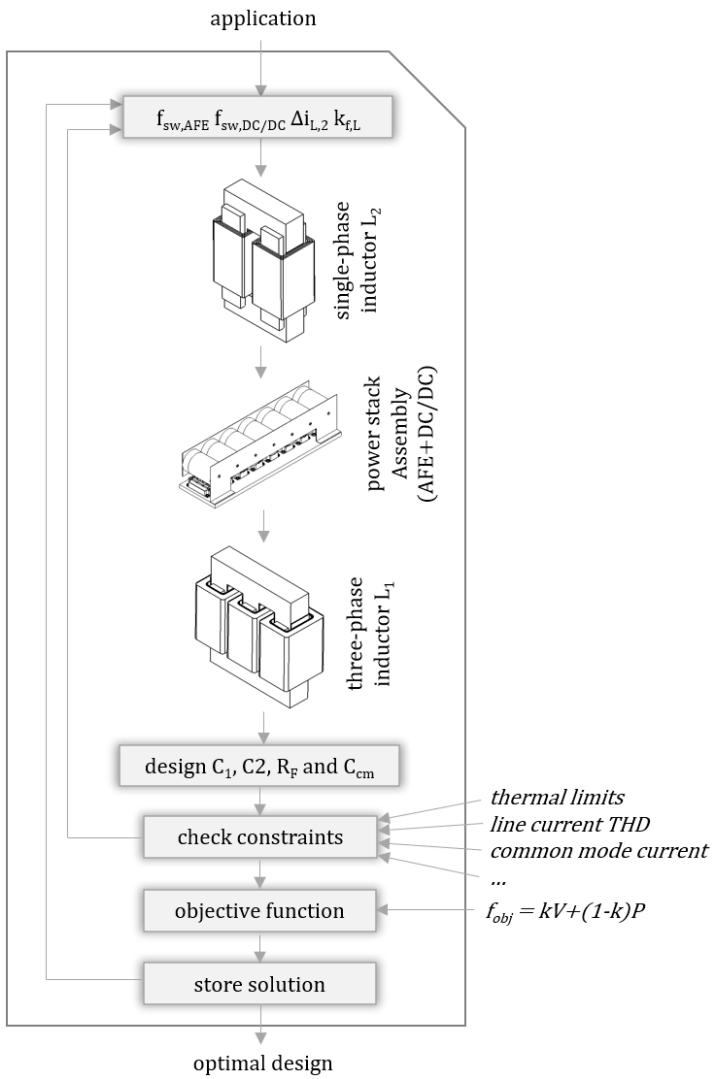



Figure 5.15: Complete optimization procedure for input stage of SML-based modulators

# 5.3 Modeling and design of SML pulse generation stage

## 5.3.1 Overview

The output stage generates the required high voltage output pulse in a converter chain based on the utilization of a modulation/demodulation scheme. Here, the pulse generator H-bridge converter generates a high frequency AC waveform amplified by a HVHF transformer. The HVHF waveform is then rectified and filtered in producing a smooth output pulse. As mentioned in the introduction, though the main capacitor banks represent the interface between the input chargers and the output pulse generators, their impact on input charger design is negligible whereas they significantly affect output stage design. For this reason, they are in this context considered to be part of the output stage. The output stage is modular, being formed by $N_p$ such pulse generators connected in series at their outputs. A complete output stage design therefore requires appropriate selection of the number of pulse generators and, subsequently, detailed design and selection of the aforementioned high-voltage high-power components. In this section, design models are developed and integrated considering a single high-voltage pulse generator module handling the module voltage $V_{mod}$. Here, the high-voltage components are integrated in a high-voltage module (HVM) as shown in Figure 5.49. The reader will frequently be referred to this figure throughout the following text. The advantages and drawbacks as well as the impact on pulse generator components as a result of utilizing multiple output modules are analysed in section 5.5 by sweeping $N_p$.

## 5.3.2 Main capacitor bank

High power modulators utilize several parallel connected capacitor chargers to split the input power. In this work, each capacitor charger supplies an individual capacitor bank. These capacitor banks store the energy needed in pulsing, each capacitor bank supplying one or more pulse generator modules. For a peak pulse power $V_2 I_2$ output over a pulse length $T_p$, the required capacitance per output module is given by (5.62). Here, $V_1$ represents the primary side voltage and $V_x$ the capacitor bank voltage droop.

$$i_C = C\frac{dv}{dt} \rightarrow C_{main} = \frac{V_2 I_2 T_p}{V_1 (V_1 - V_x) N_{mod}} \tag{5.62}$$

As a low voltage dc-link is preferred the required capacitance $C_{main}$ is often significant, requiring parallel connection of multiple high capacitance units. Such

capacitors are often implemented in rectangular casings. Using the capacitor selection procedure outlined in Appendix A and considering capacitors from e.g., the Electronicon series E57-E59, [5.16] and the AVX-Kyocera series FFLC, [5.17], the corresponding capacitor bank volume may be calculated as illustrated in Figure 5.16 and described by (5.63). Here, $N$ rectangular capacitors units have been placed in a single row and parallel connected. The benefits of this particular arrangement will be seen in the following chapter. Finally, in selecting an appropriate capacitor for the proposed configuration, it must be ensured that the configuration can withstand the main capacitor bank RMS current $V_2 I_2 / V_1 \sqrt{T_p f_r}$.

$$V_{cbk} = W_{cbk} H_{cbk} D_{cbk} = \sim W_{cbk} H_{cbk} (N d_{cbk}) \tag{5.63}$$

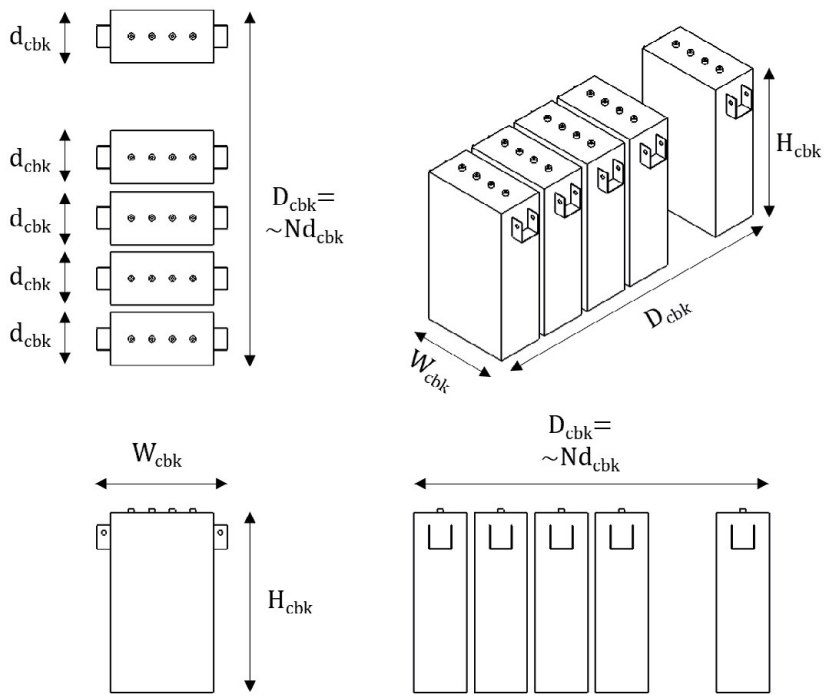



Figure 5.16: Overview of main capacitor bank

## 5.3.3 H-bridge converter

The H-bridge power stack connects to the main capacitor bank and synthesizes the high frequency square wave modulation of the desired output pulse waveform. The

H-bridge is formed by IGBT power modules, and each equivalent IGBT unit is itself composed by $N_{m,hb}$ parallel connected modules for the purpose of current handling, Figure 5.17.

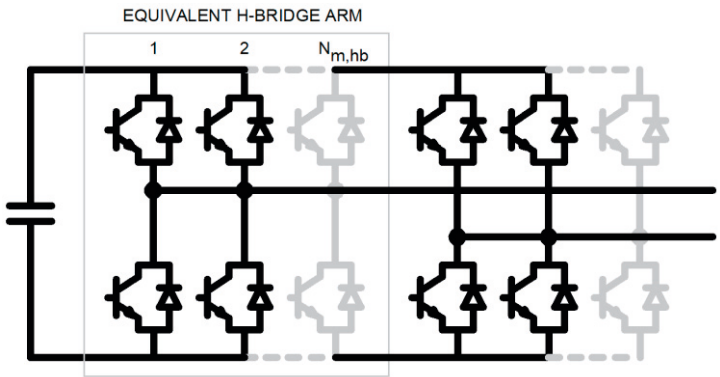



Figure 5.17: Circuit model of H-bridge converter

*Circuit function and loss modeling*

Typical switched output waveforms generated by the H-bridge converter are shown in Figure 5.18. Details on control of the H-bridge converter are described in chapter 7. As described in the preceding section, the capacitor bank voltage decreases (droops) throughout the pulse event. Therefore, in order to supply the output with a constant average voltage, the converter duty cycle must be increased in proportion to the droop. This tendency is clearly seen in Figure 5.18. Under these conditions, the idealized averaged converter output power *during the pulse event* is denoted $\bar{P}(t)$ and may be written as (5.64). From this, the total converter average power is given by (5.65), where $\bar{\delta}_{HB}$ represents the average duty cycle over the pulse event.

$$\bar{P}(t) = \bar{v}_{HB}(t)\bar{\imath}_{HB}(t) = v_{cbk}(t)\delta_{HB}(t)I_2 n = V_p I_2 n \tag{5.64}$$

$$\bar{P}_{HB} = V_p I_2 n \bar{\delta}_{HB} T_p f_r \tag{5.65}$$

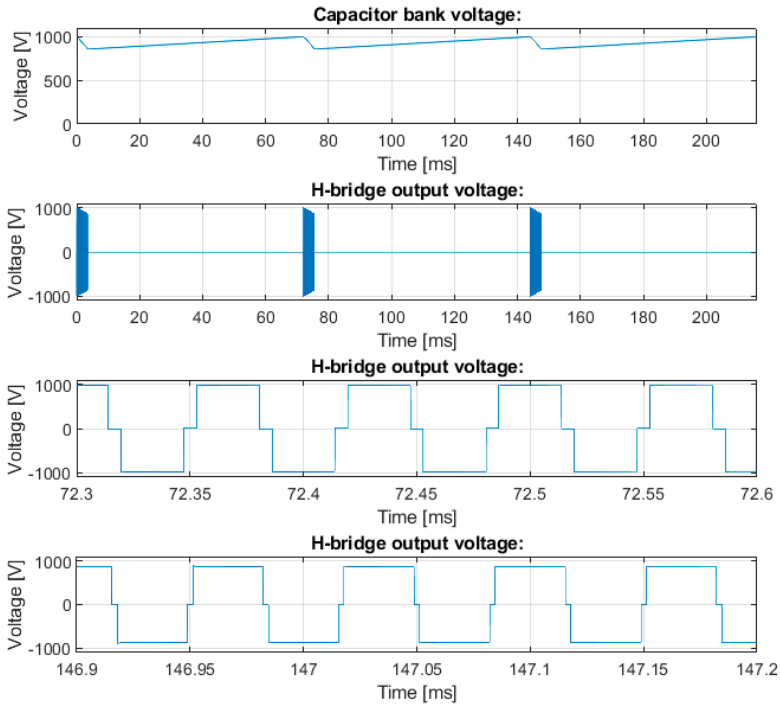



Figure 5.18: Typical H-bridge converter waveforms

Figure 5.19 depicts the corresponding IGBT voltage and current waveforms during the pulse event. Expectedly, each IGBT conducts for a time corresponding to half the converter duty cycle $\delta_{HB}(t)$. Note also that the IGBTs turn on at zero voltage, i.e., partially soft switching is achieved. Furthermore, as aforementioned, each equivalent IGBT unit is comprised by a number of parallel connected IGBT modules, effectively splitting the current between modules. Hence, from the above, the individual IGBT module conduction losses are given by (5.66) and switching losses are given by (5.67). The average IGBT power loss during the pulse event is given by (5.68), whereas the overall average IGBT power loss is given by (5.69). In these equations, $V_{ce,0}$ is the collector-emitter threshold voltage, $r_{ce}$ is the on-state slope resistance, $n$ is the transformer turns-ratio, $f_{sw}$ is the converter switching frequency, $\bar{\delta}_{HB}$ is the average converter duty cycle, and $V_{ce,ref}$ and $I_{c,ref}$ are the reference voltage and current used in switching loss scaling, respectively.

$$P_{IGBT,c} = \left(V_{ce,0} + r_{ce}\frac{I_2 n}{N_{m,HB}}\right)\frac{I_2 n}{N_{m,HB}} \tag{5.66}$$

$$P_{IGBT,sw} = f_{sw} E_{off} \left( \frac{I_2 n / N_{m,HB}}{I_{c,ref}} \right)^{K_i} \left( \frac{V_p \bar{\delta}_{HB}}{V_{ce,ref}} \right)^{K_v} \tag{5.67}$$

$$\hat{P}_{IGBT} = P_{IGBT,c} \bar{\delta}_{HB} / 2 + P_{IGBT,sw} \tag{5.68}$$

$$\bar{P}_{IGBT} = \hat{P}_{IGBT} T_p f_r \tag{5.69}$$

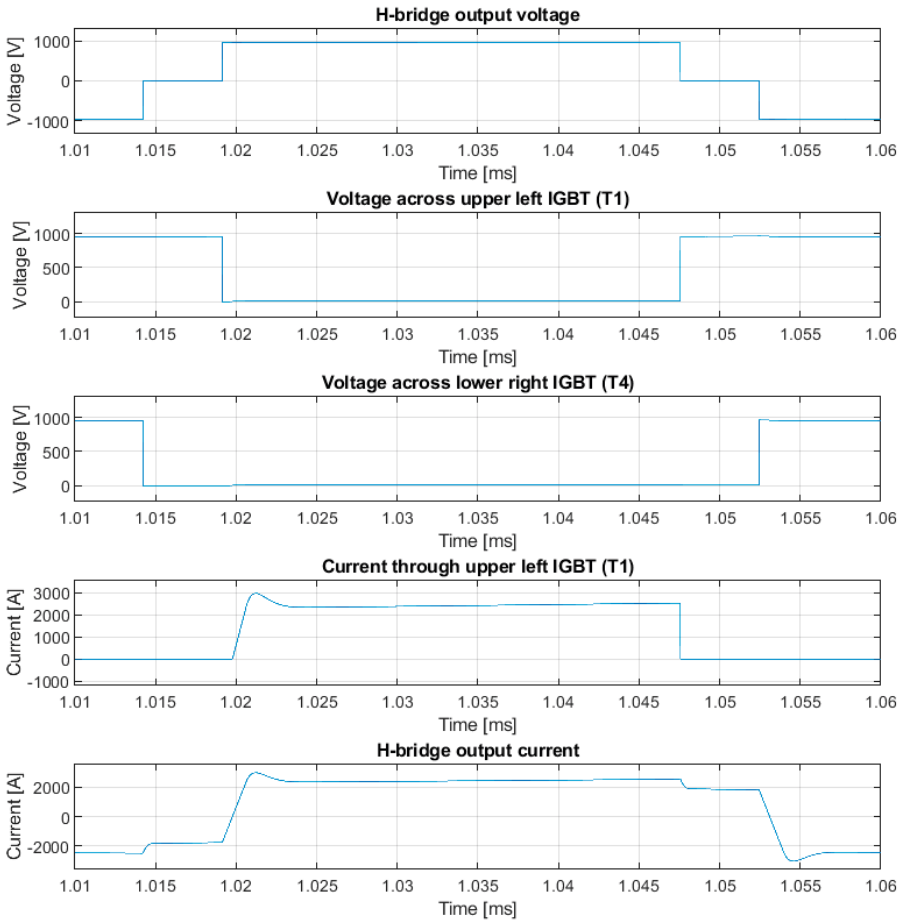



Figure 5.19: Typical H-bridge converter waveforms, zoom across switching events

*Thermal modeling and lifetime estimation*

From the above loss modeling, the averaged equivalent thermal circuit model depicted in Figure 5.20 may be derived. Here, noting that the averaged converter duty cycle $\bar{\delta}_{HB} \rightarrow 1$, the average heat sink temperature is estimated by (5.70), where

$\bar{\theta}_a$ is the coolant water temperature and $R_{th,s-a}$ is the thermal resistance of the heat sink. From this, equation (5.71) yields the average IGBT junction temperature, where $R_{th,j-s} = R_{th,j-c} + R_{th,c-s}$ is the thermal resistance from IGBT junction to module casing to heatsink. Finally, it is noted that the power dissipated throughout the pulse event as estimated by (5.68) corresponds to a transient increase in junction temperature $\Delta\theta_j$, (5.72), where $Z_{th,j}(T_{pc})$ represents the thermal impedance as a function of power cycling period (i.e., here corresponding to the application pulse length $T_p$).

$$\bar{\theta}_s = \bar{\theta}_a + 4N_{m,HB}\bar{P}_{IGBT}R_{th,s-a} \tag{5.70}$$

$$\bar{\theta}_j = \bar{\theta}_s + \bar{P}_{IGBT}R_{th,j-s} = \bar{\theta}_s + \bar{P}_{IGBT}\left(R_{th,j-c} + R_{th,c-s}\right) \tag{5.71}$$

$$\Delta\theta_j = \hat{P}_{IGBT}Z_{th,j}(T_{pc}) = \hat{P}_{IGBT}Z_{th,j}(T_p) \tag{5.72}$$

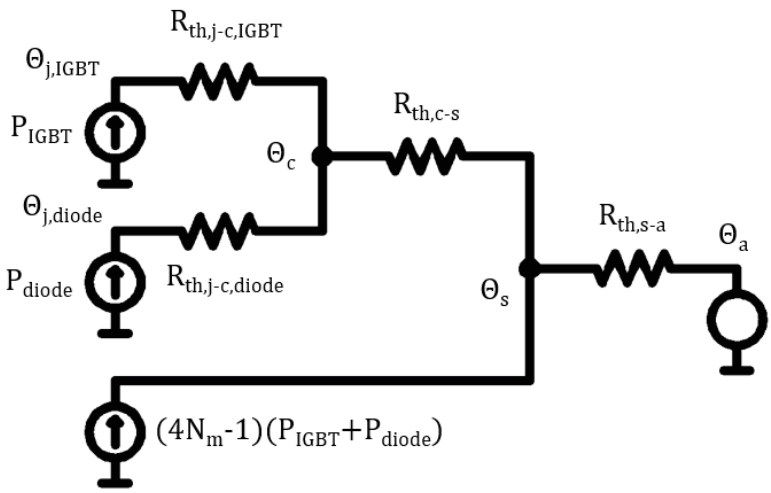



Figure 5.20: Averaged equivalent thermal circuit

The above loss and thermal modeling serve as inputs for the IGBT selection procedure outlined in Appendix B. In this work, a catalogue of high power IGBTs compiled from datasheets from Mitsubishi and Infineon has been utilized. Here, apart from trying to limit the number of IGBT modules $N_{m,HB}$, the converter efficiency given by (5.73) is used as main determinant in choosing among viable IGBT models.

$$\eta_{HB} = 1 - \frac{4N_{m,HB}\bar{P}_{IGBT}}{\bar{P}_{HB} + 4N_{m,HB}\bar{P}_{IGBT}} \tag{5.73}$$

*Modeling of converter geometry*

In accordance with the above, a given IGBT module requires $N_{m,HB}$ parallel IGBT modules per equivalent IGBT to handle the converter current and satisfy converter lifetime requirements. From this, an appropriate converter geometry is presented in Figure 5.21. Here, the $4N_{m,HB}$ IGBTs are mounted in two rows, facilitating module interconnection, on a water-cooled heat sink. In this figure, the chosen module has dimensions $m_x m_y m_z$ and the heatsink has a thickness $S_z$, With horizontal module spacing $\Delta_x$ and vertical module spacing $\Delta_y$, the converter size may be summarized as given by (5.74).

$$V_{HB} = D_{HB}W_{HB}H_{HB} = \begin{Bmatrix} D_{HB} = & M_z + S_z \\ W_{HB} = & 2m_y + \Delta_y \\ H_{HB} = & 2N_{m,HB}m_x + 2\left(N_{m,HB} - 1\right)\Delta_x \end{Bmatrix} \tag{5.74}$$

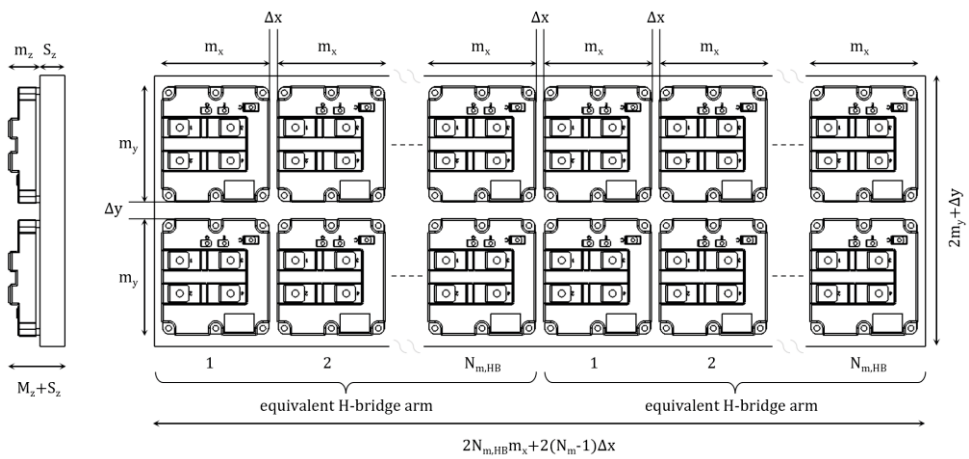



Figure 5.21: Model for estimating the geometry of H-bridge converter.

*Modeling and design of local capacitor bank*

As noted in the introductory section, the H-bridge converter is connected to and supplied by the main capacitor bank. These connections are typically made using busbars. However, given the size of the system these interconnections, despite using low inductance busbars, often represent significant series inductance. For this

reason, it is often preferable to equip each converter with a smaller local capacitor bank. The behaviour of this system is analysed in the following considering the simplified circuit model presented in Figure 5.22.

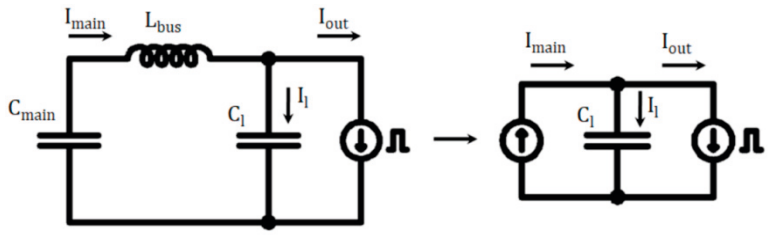



Figure 5.22: Equivalent circuit for sizing local capacitor bank

From the perspective of the capacitor banks, the output circuit may be modelled as a current source with duty cycle $\delta_{HB}$ and amplitude $V_2 I_2 / V_1 / \delta_{HB}$. Here, the output circuit current source is directly connected to the local capacitor bank $C_l$. Again, as the main capacitor bank is connected with relatively long busbars modelled by series inductance $L_{bus}$, the main capacitor bank can be considered to supply the load current component averaged over a switching period, i.e., $V_2 I_2 / V_1$. Consequently, for purposes of sizing the local capacitor bank, the further simplified circuit model shown in Figure 5.22 may be used. Idealized waveforms of this simplified circuit are shown in Figure 5.23. In this figure, $V_2 = 115\ kV$, $I_2 = 100\ A$, $V_1 = 1\ kV$ and $\delta_{HB} = 0.85$.

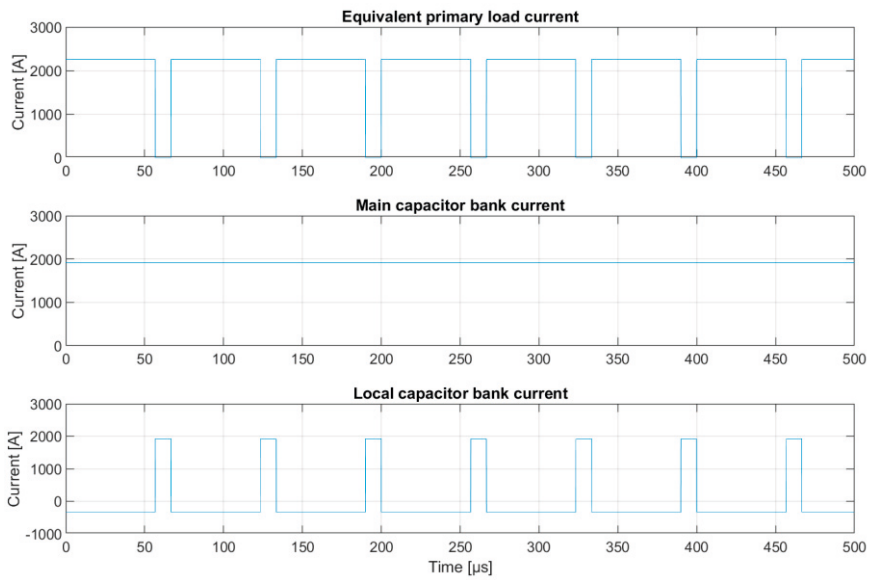



Figure 5.23: Idealized waveforms for simplified capacitor bank circuit

The local capacitor $C_l$ may be sized by considering that the local capacitor supplies the difference between the peak load current and the average load current, Figure 5.23 and (5.75). Here, $C_l$ is set to ensure that $|\Delta V|$ is small with respect to $V_1$ for the worst-case duty cycle $\delta_{HB}$.

$$i_c = C\frac{dv}{dt} \rightarrow C_l = \frac{V_2 I_2(\delta_{HB} - \delta_{HB}^2)}{N_{mod} V_1 |\Delta V| f_{sw}} \tag{5.75}$$

The ideal waveforms of Figure 5.23 are also used to estimate the peak and RMS currents flowing through the local capacitor. Using the notations indicated in Figure 5.23, $I_+$ represents the positive portion of the current (i.e., when the H-bridge converter is temporarily off and the local capacitor is charged directly by the main capacitor bank) and $I_-$ represents the negative portion of the current (i.e., the difference between the instantaneous load current and the average load current). Here, $I_+$ and $I_-$ are given by (5.76) and (5.77), respectively. From this, the corresponding RMS current is calculated from (5.78).

$$I_+ = \frac{V_2 I_2}{V_1 N_{mod}} \tag{5.76}$$

$$I_- = \frac{V_2 I_2}{V_1 N_{mod}}(1/\delta_{HB} - 1) \tag{5.77}$$

$$\begin{aligned} I_l &= \sqrt{f_r \left[\int_0^{\delta_{HB} T_p} I_+^2 \, dt + \int_0^{(1-\delta_{HB})T_p} I_-^2 dt\right]} \\ &= \left(\frac{V_2 I_2}{V_1 N_{mod}}\right)\sqrt{\frac{1}{\delta_{HB}} - 1}\sqrt{T_p f_r} \end{aligned} \tag{5.78}$$

The local capacitor bank is to be fitted as close to the IGBT modules as possible, e.g., as shown in Figure 5.24. Here, the resulting converter geometry is enclosed in a metal casing. Preferably, the enclosure should be semi-open to allow easy access for maintenance and troubleshooting. Furthermore, drivers and/or control electronics may be integrated in the enclosure geometry.

In this case, polypropylene capacitors are considered appropriate and may be selected using the capacitor selection procedure presented in Appendix A. Here,

capacitors from Electronicon series E53 are considered. The volume of the complete power stack unit is estimated by (5.79).

$$V_{HB,stack} = D_{HB,stack} W_{HB,stack} H_{HB,stack}$$
$$= \begin{Bmatrix} D_{HB,stack} = & M_z + S_z + H_c \\ W_{HB,stack} = & max\left(2m_y + \Delta_y\ ;\ N_{c,y}\emptyset_c\right) \\ H_{HB,stack} = & max\left(2N_{m,HB}m_x + 2\left(N_{m,HB} - 1\right)\Delta_x\ ;\ N_{c,x}\emptyset_c\right) \end{Bmatrix} \quad (5.79)$$

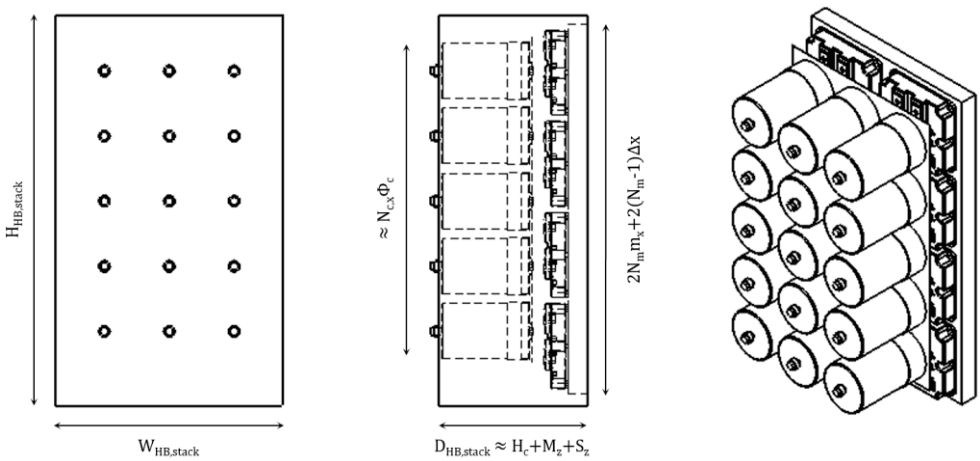



Figure 5.24: Modeling for estimating geometry of complete H-bridge power stack. In the illustrated case, $N_{m,HB} = 2$ and $N_c = 15$. A) b) c) H-bridge converter mounted on water cooled heatsink and local capacitor bank (enclosure hidden for clarity).

## 5.3.4 High voltage high frequency transformer

The HVHF transformer amplifies the voltage waveform generated by the H-bridge inverter circuit. In this work, as will be seen, it may be considered a geometrical special case of the more general pulse transformer geometry described in chapter 4. However, due to the high frequency excitation of the transformer, special attention must be paid to the details regarding both the modeling and impact of 1) the stray capacitive elements, 2) the transformer magnetic core losses, and 3) the skin and proximity effects.

An overview of the HVHF transformer geometry is shown in Figure 5.25. As noted, the similarities to the pulse transformer geometry of chapter 4 are immediately seen. Importantly, as the transformer is excited with AC waveform conical and/or asymmetrical windings are not practical, i.e., $d_{0,a} = d_{0,b} = d_{i,b} = d_{i,a} = d_i$. In addition, given the application and chosen modulator topology, no benefit is derived

from parallel connection of the transformer secondary windings. Hence, $V_{s,0,a} = 0$, $\hat{V}_{s,a} = V_{s,0,b} = V_{mod}/2$ and $\hat{V}_{s,b} = V_{mod}$. Finally, as the transformer is operated with a modulation of the pulse waveform, the transformer leakage inductance must clearly be significantly lower than that of the corresponding pulse transformer. Therefore, practically speaking, considerably fewer winding turns must be used, i.e., single layer transformer windings are appropriate. Details on the modeling and optimization of this transformer geometry are discussed in the subsequent sections.

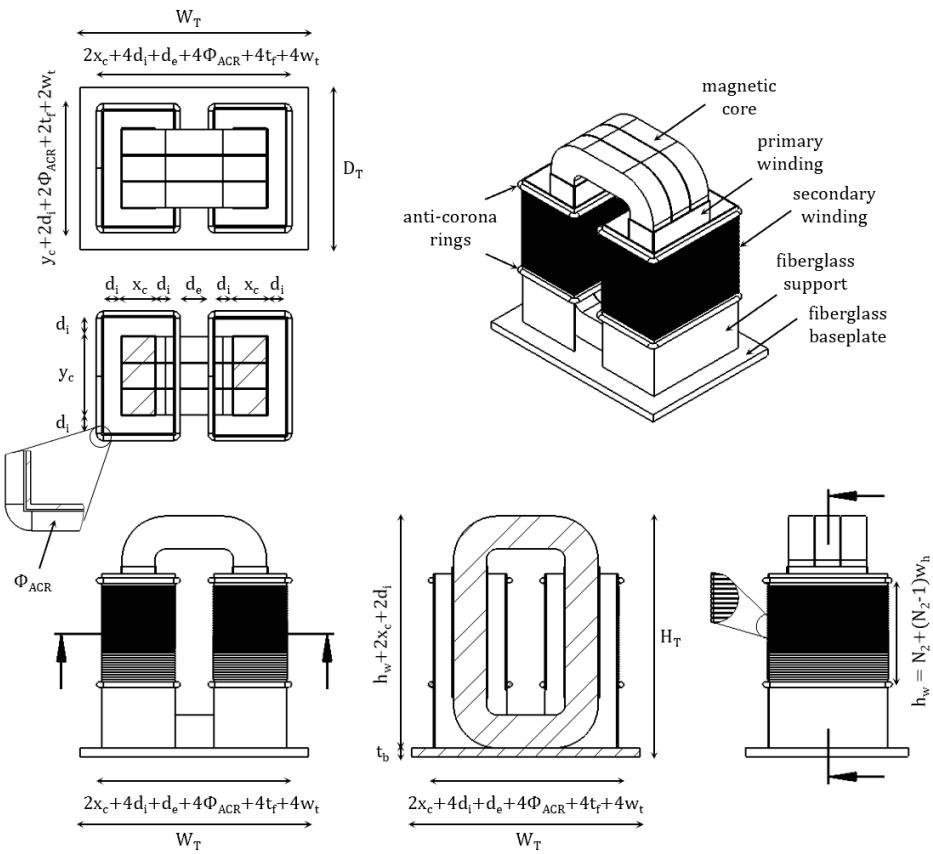



Figure 5.25: Overview of HVHF transformer

*Magnetic core*

In this context, the transformer core should be implemented using tapewound nanocrystalline core material, e.g., VITROPERM 500F, [5.18], due to the following main reasons: 1) a high-frequency waveform with high harmonic content is applied to the transformer, 2) the approximate total size of the transformer in considering

high-voltage, high-power applications, and 3) the requirement on low leakage transformer design. Preferably, uncut cores should be used to minimise the difference between transformer units. A typical AC voltage waveform generated by the H-bridge and applied to the transformer primary windings is shown in Figure 5.26.a. Here, the applied voltage waveform is associated to the transformer core magnetic flux density shown in Figure 5.26.c and given in (5.80). The worst-case magnetic excitation is seen during the pulse rise time, in which both the amplitude of the applied waveform as well as the converter duty cycle are the greatest ($t \approx 0 \rightarrow v_p(t) = V_p$ and $\delta \rightarrow 1$). Considering the transformer core leg width $x_c$, the transformer number of turns per secondary winding $N_2$, the maximum core peak flux density $B_{max}$ and the converter switching frequency $f_{sw}$ to be fundamental design variables, the required magnetic core depth may be calculated from (5.81), conveniently expressed from the perspective of the transformer secondary circuit. In these equations, $\Delta V_p$ is the capacitor bank voltage droop and $k_f$ is the magnetic material fill factor.

$$v_p(t) = \left(V_p - \Delta V_p \frac{t}{T_p}\right) = N \frac{d\emptyset}{dt} = N_1 \frac{(2B_{max}) x_c y_c k_f}{\delta/(2f_{sw})} \tag{5.80}$$

$$y_c = \left\{\begin{matrix} t \rightarrow 0 \\ \delta \rightarrow 1 \end{matrix}\right\} = \frac{\hat{V}_s}{8 x_c k_f N_2 B_{max} f_{sw}} \tag{5.81}$$

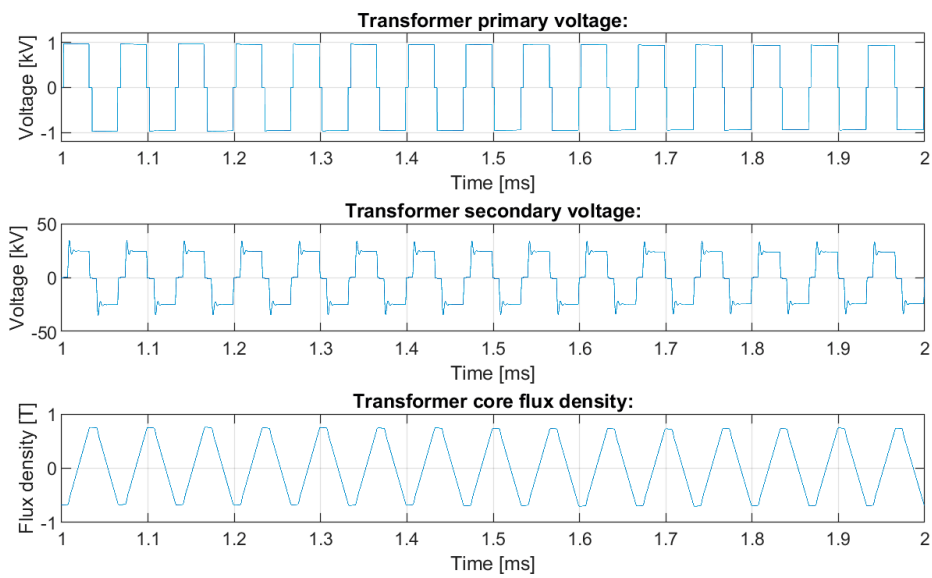



Figure 5.26: Transformer waveforms used in sizing the HVHF transformer magnetic core- a) transformer primary voltage; b) transformer secondary voltage; c) transformer core magnetic flux density

Magnetic core losses are typically given in material datasheets as, e.g., the power loss per unit mass $P_0$ for some reference operating frequency $f_0$, reference waveform factor $F_0$ and reference peak magnetic flux density $B_0$. Here, the published losses are scaled using datasheet parameters $c_x$, $c_y$ and $c_z$, [5.18]. From this, the average transformer magnetic core losses are calculated by multiplication with the magnetic core mass $V_c\rho_{fe}$ and the pulse duty cycle $T_p f_r$, (5.82).

$$P_{fe} = P_0 \left(\frac{f_{sw}}{f_0}\right)^{c_x} \left(\frac{F}{F_0}\right)^{c_y} \left(\frac{B_{max}}{B_0}\right)^{c_z} V_c \rho_{fe} T_p f_r \tag{5.82}$$

*Transformer windings*

As was indicated in Figure 5.25, the HVHF transformer winding geometry is similar to that described for the pulse transformer in chapter 4. However, due to the high frequency excitation, the impact of both the skin effect and the proximity effect must be taken into account in winding design. As noted, the transformer secondary windings are to be based on the single layer winding technique as outlined in section 4.2.7. However, as opposed to round enamelled copper wire, the combination of 1) high modulator average power, 2) the above noted issues related to the skin effect, and 3) constraints on leakage inductance instead suggests use of rectangular enamelled copper wire. Here, the skin depth is given by (5.83), from which [5.10] suggests selecting the winding turn thickness according to (5.84). From this, the imposed maximum RMS current density dictates the necessary winding turn height, (5.85), such that the secondary winding height is given by (5.86). In these equations, $\delta_0$ is the skin depth evaluated at the frequency $f_{sw}$.

$$\delta_0 = \sqrt{\frac{\rho_{cu}}{\mu_0 \pi f_{sw}}} \tag{5.83}$$

$$w_t = 2\delta_0 \tag{5.84}$$

$$w_h = I_2 \sqrt{T_p f_r} / (J w_t) \tag{5.85}$$

$$h_w = N_2 w_h + (N_2 - 1) d_y \tag{5.86}$$

Then, with the copper cross-sectional area and winding mean path length given by (5.87) and (5.88), respectively, the transformer secondary winding losses may be

calculated using (5.89), where $F_{AC}$ is the total ac resistance factor and $V_{cu} = A_{cu}[MPL]$.

$$A_{cu} = w_t w_h \tag{5.87}$$

$$[MPL] = 2\left(x_c + y_c + 4t_f + 2d_i + 2\frac{1}{2}w_t\right) \tag{5.88}$$

$$P_{cu,s} = F_{AC}\rho_{cu}J^2V_{cu} = F_{AC}\rho_{cu}J^2A_{cu}[MPL] \tag{5.89}$$

Of course, the primary windings carry significantly higher current than the secondary windings. Given the described limitation on the number of secondary winding turns, a foil-type winding is appropriate. Here, in addition to skin effect, proximity effect becomes significant. Importantly, as shown in [5.19], using even just a few winding layers significantly increases the AC resistance and thus the associated winding losses. Sizing of foil-type windings in view of skin and proximity effect is discussed at length in, e.g., [5.20]-[5.21] and is briefly summarized in the following.

It is well known that any arbitrary waveform may be represented by its Fourier series, (5.90). Clearly, the corresponding ohmic power losses dissipated in the transformer winding may then be formulated as (5.91). Here, $F_{AC,n}$ is the AC resistance factor at harmonic $n$ and $I_n$ is the current RMS value at the same frequency. Importantly, it was shown in [5.19] that $F_{AC,n}$ may be calculated from (5.92). In this equation, $p$ is the number of winding layers and $\Delta$ is the ratio between the winding layer thickness $w_t$ and the skin depth at the switching frequency $\delta(f_{sw})$.

$$i(t) = I_{dc} + \sum_{n=1}^{\infty}\sqrt{2}I_n\,cos(n\omega t + \varphi_n) \tag{5.90}$$

$$P_{cu,p} = R_{DC}I_{DC}^2 + R_{DC}\sum_{n=1}^{\infty}F_{AC,n}I_n^2 \tag{5.91}$$

$$F_{AC,n} = \sqrt{n}\Delta\left[\begin{array}{c}\dfrac{sinh\left(2\sqrt{n}\Delta\right) + \sin\left(2\sqrt{n}\Delta\right)}{cosh\left(2\sqrt{n}\Delta\right) - cos\left(2\sqrt{n}\Delta\right)} \\ +\dfrac{2(p^2-1)}{3}\dfrac{sinh\left(2\sqrt{n}\Delta\right) - \sin\left(2\sqrt{n}\Delta\right)}{cosh\left(2\sqrt{n}\Delta\right) + cos\left(2\sqrt{n}\Delta\right)}\end{array}\right] \tag{5.92}$$

Noting the importance of Δ on the AC resistance factor and thus losses, [5.22] considers the problem of finding the optimal Δ such that the effective foil-winding resistance is minimized. As demonstrated in [5.22], $\Delta_{opt}$ is strongly dependent on the type of current waveform, the waveform duty cycle, and the number of winding layers. Here, Figure 5.27 shows a simulated typical current waveform expected for the transformer primary windings with $I_2 = 100\ A$, $I_1 = nI_2 = {\sim}2.5\ kA$ such that $I_p = I_1/2$, and $f_{sw} = 15\ kHz$. Approximating this waveform with a pulse waveform with $\delta \to 1$ and rise and fall times $t_r = t_f$, $\Delta_{opt}$ is given by (5.93), [5.22]. Here, the rise time $t_r$ may be estimated from the leakage inductance referred to the primary $L'_s$ according to (5.94). The details of this calculation are explained in further detail in the following section. Importantly, given the definition of Δ, the optimal layer winding thickness $w_{t,opt}$ is immediately given by (5.95). Furthermore, with this choice of $w_t$, the effective AC resistance $R_{AC}$ is given by $(4/3)R_{DC}$, (5.95), [5.22].

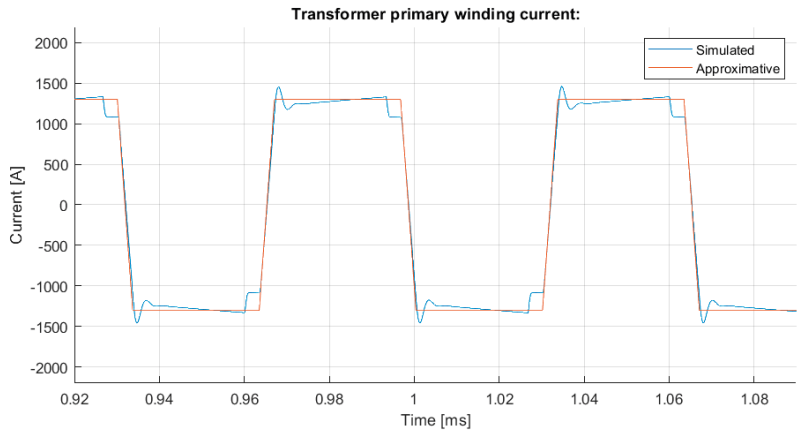



Figure 5.27: Approximated waveform used in sizing transformer primary windings (proximity effect)

$$\Delta_{opt} = \sqrt[4]{\frac{\left[1 - \frac{8t_r}{3T}\right]\pi^2 \frac{t_r}{T}}{\left(\frac{5p^2-1}{15}\right)}} \tag{5.93}$$

$$t_r = \frac{2L'_s I_1}{V_1} \tag{5.94}$$

$$w_{t,opt} = \delta_0 \Delta_{opt} = \delta_0 \sqrt[4]{\frac{\left[1 - \frac{8t_r}{3T}\right]\pi^2 \frac{t_r}{T}}{\left(\frac{5p^2-1}{15}\right)}} \to R_{AC} = \frac{4}{3} R_{DC} \to F_{AC} = 4/3 \tag{5.95}$$

Of course, it must here be ensured that the chosen winding thickness $w_t$ is not too thin to be practical. Thus, in this work, $w_t$ is chosen according to (5.96). Naturally, if $w_t \neq w_{t,min}$ the effective AC resistance must be calculated directly from (5.91)-(5.92).

$$w_t = max\left(w_{t,opt}, w_{t,min}\right) \tag{5.96}$$

With this selection, the primary winding height is given by (5.97). Here, it is desirable to ensure that $h_p \geq h_w$. Finally, with the copper cross-sectional area and winding mean path length given by (5.98) and (5.99), respectively, the transformer primary winding losses may be calculated using (5.100), where $F_{AC}$ is the total ac resistance factor and $V_{cu} = A_{cu}[MPL]$.

$$h_p = I_2\sqrt{T_p f_r}/(Jw_t) \geq h_w \tag{5.97}$$

$$A_{cu} = w_t h_p \tag{5.98}$$

$$[MPL] = 2\left(x_c + y_c + 4t_f\right) \tag{5.99}$$

$$P_{cu} = 2F_{AC}\rho_{cu}J^2V_{cu} \tag{5.100}$$

*Estimation of transformer leakage inductance*

As noted, the HVHF transformer geometry is a special case of the more general pulse transformer geometry presented in chapter 4. Hence, the magnetic energy stored in the leakage field of the HVHF transformer geometry may be calculated according to the procedure outlined in section 4.2.4. Using equation (4.47), setting $d_i = d_o$ and $l_w = 2(x_c + y_c + 2d_i)$, Figure 5.25, the stored magnetic energy is straightforwardly calculated according to (5.101). Then, the corresponding leakage inductance is given by (5.102).

$$W_m = 2\frac{1}{2}\mu_0\mu_r l_w \int_0^{h_w}\left[\left(\frac{N_2 I_2}{h_w}\right)^2 d_i\right]dy = \mu_0\mu_r\left(\frac{l_w d_i}{h_w}\right)(N_2 I_2)^2 \tag{5.101}$$

$$W_m = \frac{1}{2}L_s I_2^2 \rightarrow L_s = 2\mu_0\mu_r\left(\frac{l_w d_i}{h_w}\right)N_2^2 \tag{5.102}$$

The transformer leakage inductance must be limited for two primary reasons. First, as will be described in further detail in section 5.3.5, in switched operation the leakage inductance of the transformer will resonate with the stray capacitance of the high voltage rectifier in generating high voltage spikes seen by (in particular) the high voltage rectifier diodes. In this work, these voltage spikes are mitigated using passive RC snubbers. The corresponding snubber losses may represent a non-negligible part of total modulator losses and should be minimized, [5.23]. Second, the leakage inductance is directly linked to an additional average voltage drop across the rectifier circuit output. This may be understood by representing the output filter with an ideal current source. Due to the leakage inductance, the transformer-side current cannot transition instantly from $+\hat{I}_2$ to $-\hat{I}_2$ and vice versa in converter switching. During this transitory period, all diodes conduct simultaneous, representing an average voltage drop across the rectifier output. Using the method described in [5.10], this voltage drop is estimated by (5.103). This voltage drop is included as part of a module design constraint presented in 5.3.6.

$$\bar{V}_r = 4L_s f_{sw} \hat{I}_2 \tag{5.103}$$

*Estimation of transformer stray capacitance*

The transformer stray capacitance may also be estimated using the techniques developed in chapter 4. However, it is pointed out that as 1) the transformers are in series (i.e., progressively increasing voltage), and that 2) the high voltage box enclosing the associated rectifier and filter is floating, direct application of some of these equations is generally not possible. Still, as will be demonstrated in section 5.3.7, it turns out that – from the perspective of designing for mitigation of stray elements – treating a single high voltage module represents the worst case. In this case, the high voltage box is grounded (due to the fact that the load itself is grounded), allowing direct application of the equations developed in chapter 4 as a starting point for calculation. If for other purposes a more complete model is needed, the equations developed in chapter 4 require (straightforward) modification.

In these considerations, an important difference is that whereas in the case of the pulse transformer all capacitive elements could be lumped together into a single capacitor placed across the transformer secondary, this is no longer possible due to the existence of a significant high frequency common mode (CM) voltage component. Unless properly managed, this CM component may excite resonant modes, corresponding to significant CM currents deteriorating pulse quality, [5.23]. Instead, as was demonstrated in [5.23], the stored electrostatic energy may be modelled by several lumped capacitors placed between 1) the primary windings and the secondary windings and 2) the secondary windings and the oil tank and the high voltage box enclosure (grounded). Here, the energy stored in regions 1 and 6 is

attributed to the equivalent capacitance placed between the primary windings and the secondary windings whereas the energy stored in regions 2, 3, 4 and 5 is attributed to the equivalent capacitance placed between the secondary windings and ground. Thus, from the geometry presented in Figure 5.25 and from the above modeling work, the symmetrical equivalent circuit representation shown in Figure 5.28 may be conceptualized. Here, $R_p$ is the total equivalent primary-side winding resistance, $R_s$ is the total equivalent secondary-side winding resistance, $C_{ps}$ is the stray capacitance between the primary and secondary sides, $C_{sg}$ is the stray capacitance between the secondary side and ground, and $L_s'$ and $L_s''$ represent the transformer leakage inductance referred to the primary and secondary sides, respectively.

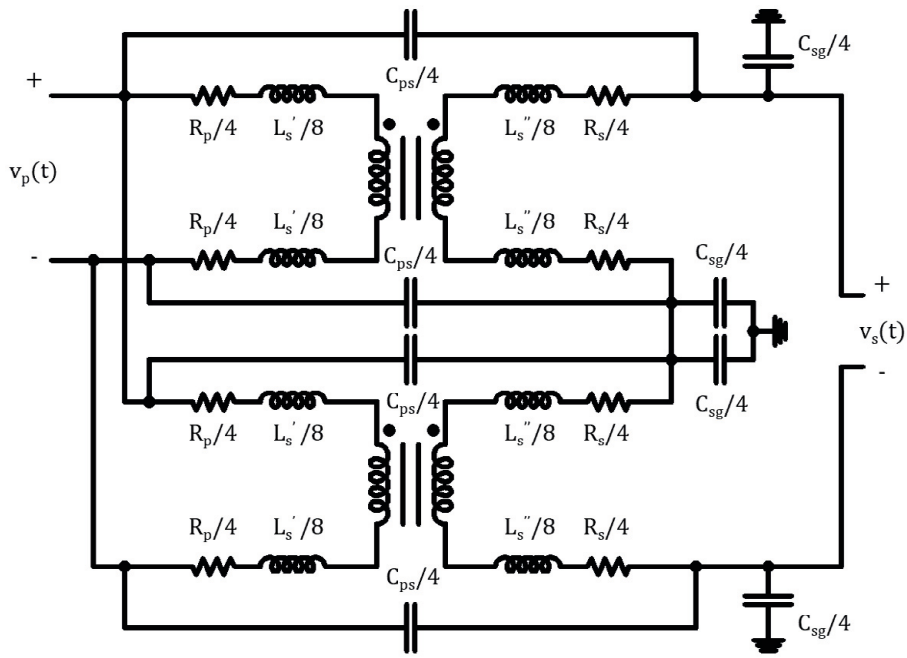



Figure 5.28: Complete equivalent circuit representation of high voltage high frequency transformer

*Transformer evaluation procedure*

For the high voltage high frequency transformer, the magnetic core leg width ($x_c$), the number of turns per secondary winding ($N_2$), the secondary winding height ($h_w$), the switching frequency ($f_{sw}$) and the peak magnetic flux density ($B_{max}$) are considered fundamental design parameters. Again, note that as the high voltage modules are series connected, the transformers experience different voltages with respect to ground. Still, all transformers are here designed with respect to the highest

expected system voltage through appropriate selection of the high voltage isolation distance $d_i$ to minimize the number of unique components. Based on this, the complete high voltage high frequency transformer geometry may be generated and characterized as summarized in Figure 5.29.

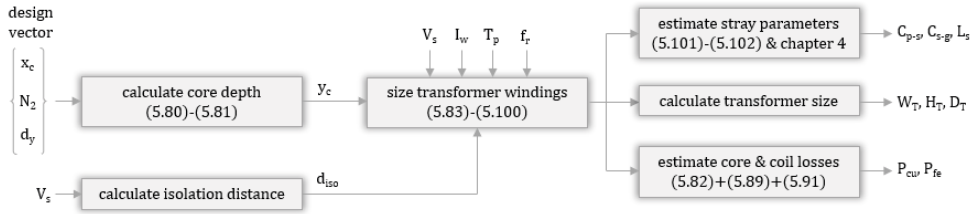



Figure 5.29: Evaluation procedure used in high voltage high frequency transformer design

### 5.3.5 High voltage rectifier

The high voltage rectifier circuit rectifies the square voltage waveform generated by the H-bridge and amplified by the HVHF transformer. In switched operation, the leakage inductance of the transformer resonates with the stray capacitance of the rectifier circuit generating a high voltage overshoot experienced by the reverse biased rectifier diodes. Hence, fast switching diodes (tens of kHz) capable of withstanding high voltage (tens of kV) are needed. To practically satisfy these requirements, a series arrangement of fast Schottky diodes equipped with parallel passive RC snubbers is utilized. In addition, a metal-oxide Varistor (MOV) is added in parallel with each diode unit for protection in case of abnormal overvoltage conditions. Bleeder resistors are also used to ensure complete discharge of the snubber capacitors between pulse events.

*General considerations*

In steady state operation, the reverse biased rectifier diodes experience a voltage $V_{mod}$. Considering an overvoltage margin $k_{HVR}$ ($\approx 2$), the number of series connected diodes making up each equivalent rectifier diode may be calculated according to (5.104), where $V_{d,max}$ is the maximum voltage rating per diode.

$$N_d = ceil\left(\frac{k_{HVR} V_{mod}}{V_{d,max}}\right) \tag{5.104}$$

Considering a per-module output voltage in the range 20…40 kV it is clear that, given the limitations of contemporary high performance fast diodes, several tens of series connected diodes will be required per equivalent rectifier diode, (5.104). Noting that the rectifier bridge requires four equivalent diodes to form a full bridge circuit, beyond a hundred (quite possibly hundreds) diodes and associated components are needed. For instance, limiting the operational voltage per diode to 600-800 V, components rated for 1.2 kV may safely be used. In this voltage range, high performance components are found in standardized packaging, e.g., TO-268A, allowing compact design by placement of the diodes and their associated components on a number of interconnected printed circuit boards (PCB), Figure 5.30.

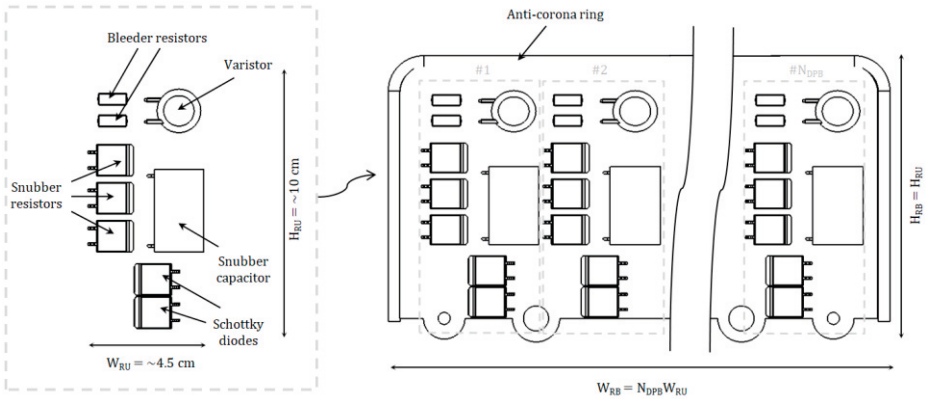



Figure 5.30: Printed circuit board with diodes and associated components. Each PCB is equipped with its own anti-corona ring.

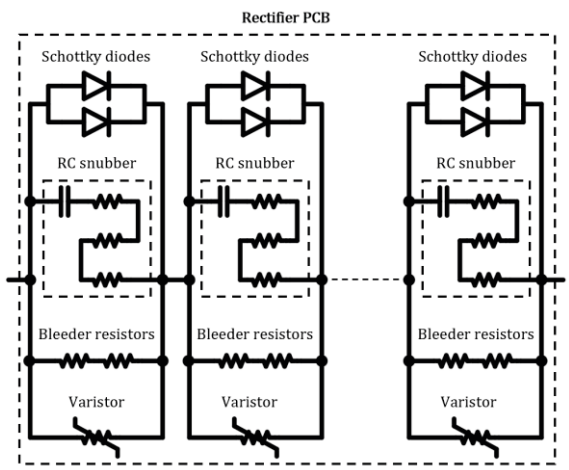



Figure 5.31: Schematic of PCB showing interconnection of rectifier diodes, snubbers, bleeder resistors and varistors.

Figure 5.30.a shows a possible PCB arrangement of a diode with associated snubber capacitor, snubber resistor(s), bleeder resistor(s) and MOV. Note how, in particular, diodes may be connected in parallel to manage the application current. Similarly, the snubber resistor may be split into several resistive elements to manage the RC snubber losses. This arrangement, using standardized component packaging and allowing for conservative isolation and PCB routing, requires approximately $4.5x10\ cm^2$. Then, Figure 5.30.b illustrates how the arrangement may be extended by placing $N_{dpb}$ series connected diode arrangements per PCB. Here, Figure 5.31 shows a schematic of the rectifier PCB showing the interconnection of rectifier diodes, snubbers, bleeder resistors and varistors. Then, with $N_{dpb}$ diodes per PCB, $N_b = ceil\left(N_d/N_{dpb}\right)$ boards need to be series connected per equivalent rectifier diode. This is accomplished by placing the rectifier boards around four isolating fiberglass rods with an appropriate isolation distance $d_{i,RB}$ in-between each board. The stack of rectifier boards begins and ends with a conductive plate equipped with an anti-corona ring, effectively shielding the entire rectifier arrangement, Figure 5.32. The geometrical extents of this volume are given in (5.105).

$$V_{HVR} = W_{HVR}H_{HVR}D_{HVR} = \begin{Bmatrix} W_{HVR} = & 2N_{dpb}W_{RU} \\ H_{HVR} = & 2H_{RB} = 2H_{RU} \\ D_{HVR} = & N_bD_b + (N_b + 2 - 1)d_{i,RB} \end{Bmatrix} \quad (5.105)$$

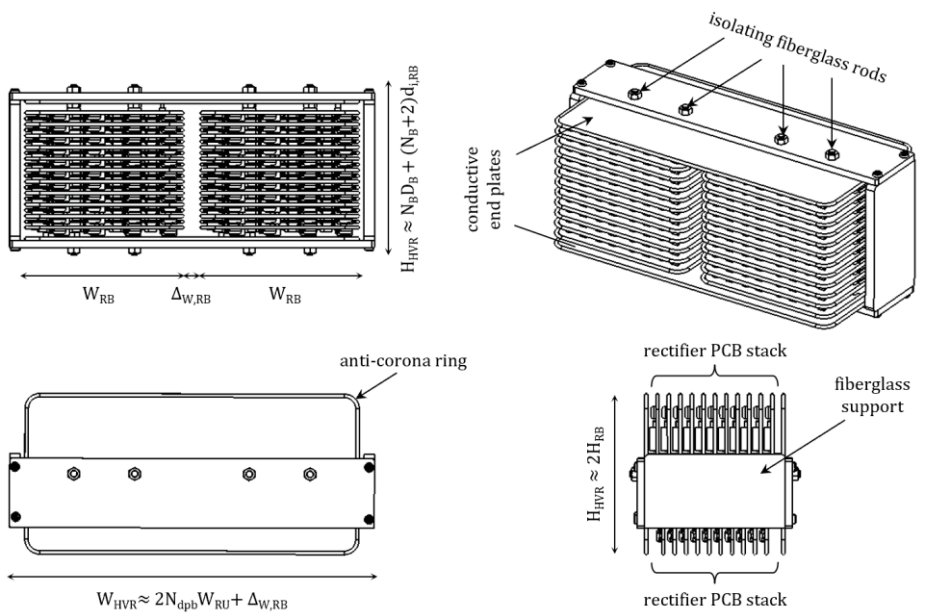



Figure 5.32: High voltage rectifier assembly

*Modeling of stray capacitance*

To estimate the stray capacitance elements associated with the high voltage rectifier geometry, the equivalent circuit representation presented in Figure 5.33 is used. Here, it is considered that the voltage $+V_{mod}$ has been applied to the rectifier input terminals such that, in static operation, the top left and the bottom right rectifier diodes are conducting and may be replaced by equivalent short circuits. Further, in considering a single module, the negative DC-side bus may be assumed to be grounded in generating a worst-case circuit representation. Under these conditions, all PCB anti-corona rings corresponding to the equivalent upper left diode may be seen to be at $+V_{mod}$. Similarly, all PCB anti-corona rings corresponding to the equivalent bottom right diode may be seen to be grounded. Finally, the voltage across the equivalent bottom left and upper right rectifier diodes is distributed among the anti-corona rings from ground to $+V_{mod}$.

Two distinct types of stray capacitive elements may here be identified; between adjacent anti-corona rings, and between each anti-corona ring and the surroundings, Figure 5.33. Here, given that the voltage between adjacent anti-corona rings is relatively low (typically considering tens of kV distributed among several tens of rectifier diodes), the stored energy and the corresponding stray capacitance value are considered negligible and are not further treated in this work. On the other hand, the electrostatic energy stored between the anti-corona rings and the surroundings is not negligible and must be accurately estimated.

In this work, the collection of anti-corona rings associated with a given equivalent rectifier diode is approximated as a conductive plate parallel to the module enclosure. Again, for the equivalent upper left diode, the voltage on each anti-corona ring is $+V_{mod}$ such that the arrangement may be considered an ideal parallel plate capacitor with plate interdistance $d_i$, (5.106). For the equivalent lower left and equivalent upper right rectifier diodes, the voltage is increasing from 0 to $+V_{mod}$ such that the techniques developed in chapter 4 may be directly adopted as summarized in (5.107). Finally, with the stray capacitances appearing in parallel, Figure 5.33, the total equivalent stray capacitance of the high voltage rectifier assembly is given by (5.108).

$$C_x \sim \varepsilon_0 \varepsilon_r \frac{H_{RB}\, N_b/2\left(D_b + d_{i,RB}\right) + 2N_{dpb} W_{RU}\, N_b/2\left(D_b + d_{i,RB}\right)}{d_i} \tag{5.106}$$

$$C_y \sim \frac{1}{3} \varepsilon_0 \varepsilon_r \frac{H_{RB}\, N_b/2\left(D_b + d_{i,RB}\right) + 2N_{dpb} W_{RU}\, N_b/2\left(D_b + d_{i,RB}\right)}{d_i} \tag{5.107}$$

$$C_{HVR} = C_x + 2C_y \tag{5.108}$$

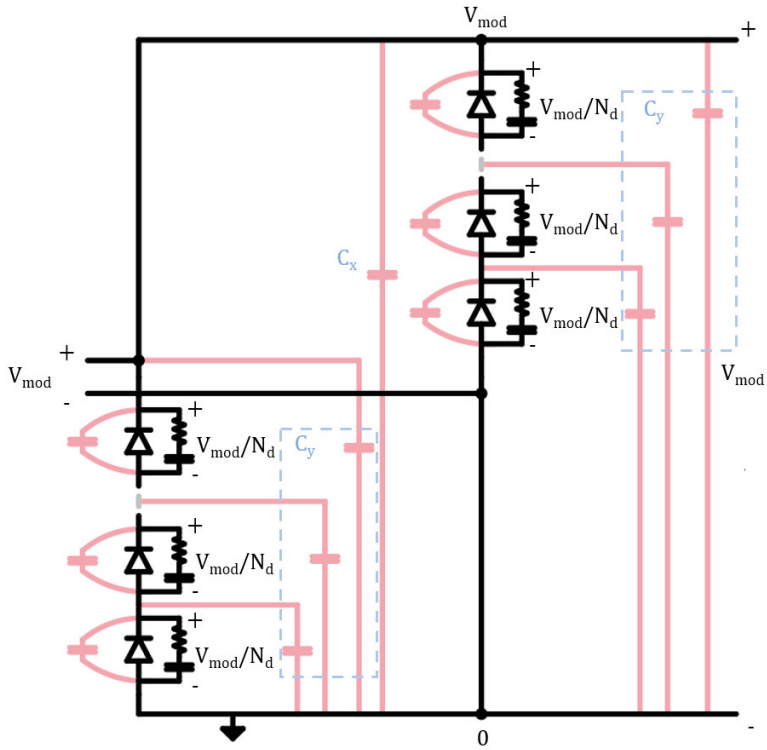



Figure 5.33: Equivalent circuit modeling for estimation of parasitic capacitance elements in high voltage rectifier geometry

*Snubber circuit design*

As mentioned, switched operation generates high voltage overshoots experienced by the reverse biased rectifier diodes. In this work, the overshoot is mitigated by equipping the rectifier diodes with passive RC snubber circuits. As is demonstrated in Figure 5.34, the complete circuit may be reduced to that shown in Figure 5.34.c for the purposes of evaluating the rectifier diode differential mode transient behaviour (the output circuit may be considered to be open in studying the transient response). Here, the pulsed source has amplitude $V_{mod}$ and is repeated at frequency $f_{sw}$. In this model, the snubber circuits of the reverse biased rectifier diodes are represented by $C_1 = 2C_s/N_d$ and $R = R_s N_d/2$. In this representation, $C_s$ and $R_s$ are the physical snubber capacitance and snubber resistance values. The inductor represents the full leakage inductance of the HVHF transformer referred to the secondary. Finally, $C_2 = C_{HVR}/2$ represents the equivalent circuit stray capacitance of the high voltage rectifier assembly as derived in the preceding section.

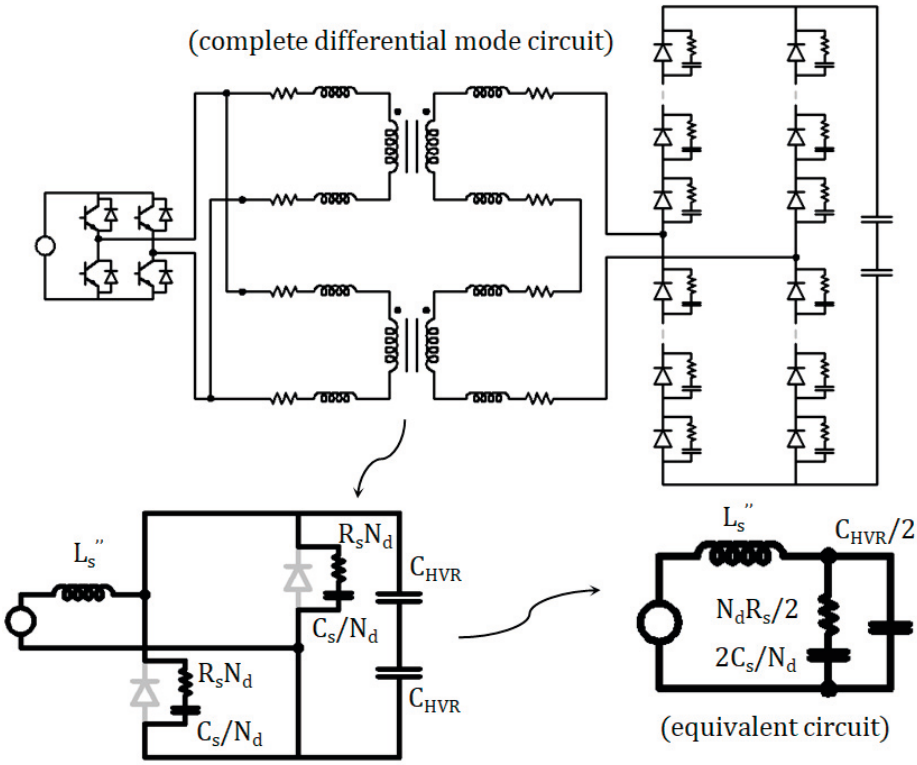



Figure 5.34: Developed equivalent circuit model to evaluate transient rectifier behavior

To permit fast evaluation of the rectifier diode overshoot as well as the corresponding snubber resistance losses, a state space model of the circuit shown in Figure 5.34.c is utilized, (5.109). Here, step excitation of the model may be limited to the transient portion of the switching event, from which the resulting overshoot may be calculated from (5.110), and the corresponding total snubber resistor loss is calculated from (5.111).

$$\begin{pmatrix} \dot{\imath}_{L_s''} \\ \dot{v}_{C1} \\ \dot{v}_{C2} \end{pmatrix} = \begin{pmatrix} 0 & -1/L_s'' & 0 \\ 1/C_1 & -1/(RC_1) & 1/(RC_1) \\ 0 & 1/(RC_2) & -1/(RC_2) \end{pmatrix} \begin{pmatrix} i_{L_s''} \\ v_{C1} \\ v_{C2} \end{pmatrix} + \begin{pmatrix} 1/L_s'' \\ 0 \\ 0 \end{pmatrix} V_{mod} \quad (5.109)$$

$$\hat{V}_d = max\big(v_{C2}(t)\big) \quad (5.110)$$

$$\bar{P}_s = 8 f_{sw} T_p f_r \int (i_{C1}/2)^2 \, R \, dt \quad (5.111)$$

*Evaluation of high voltage rectifier design*

High voltage rectifier design is summarized in Figure 5.35. Here, a catalogue of fast Schottky diodes is evaluated for the intended application. The number of diodes per rectifier board $N_{dpb}$ may be swept to optimize rectifier size. Additionally, the rectifier size is used in calculating the lumped stray capacitance $C_r$ which together with the transformer leakage inductance $L_s$ serves as input for sizing the diode rectifier snubbers. Importantly, $\hat{V}_d \leq V_{d,max} \ll k_{HVR}V_{mod}$.

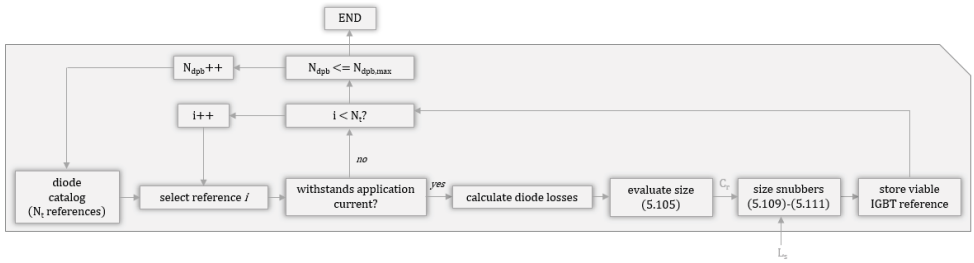



Figure 5.35: High voltage rectifier design procedure

## 5.3.6 High voltage filter

The previous conversion stages have generated a high voltage, high frequency modulation of the desired output pulse. The final component in the SML conversion chain is the high voltage output filter. The purpose of the filter is to demodulate the generated waveform, ensuring formation of a smooth output pulse with a fitting compromise between pulse rise time and pulse flat top ripple.

*Selection of filter topology and configuration*

In selecting an appropriate filter topology and designing the required components it is important to recognize that several filter configurations are possible given the modularity of the SML modulator topology. Three basic filter configurations are shown in Figure 5.36 and are summarized in the following-

- Option A: each module has its own output filter. The module outputs are series connected. Each filter must provide sufficient attenuation at $2f_{sw}$ such that the total output ripple satisfies application requirements.
- Option B: each module has its own inductor (this is necessary as the module voltages are phase shifted). The module outputs are series connected and fed to a common output filter. The filter is designed to provide sufficient attenuation at $2N_m f_{sw}$ such that the total output ripple satisfies application requirements.

- Option C: modules have their own output filters as well as a common output filter, representing a hybrid between options A and B.

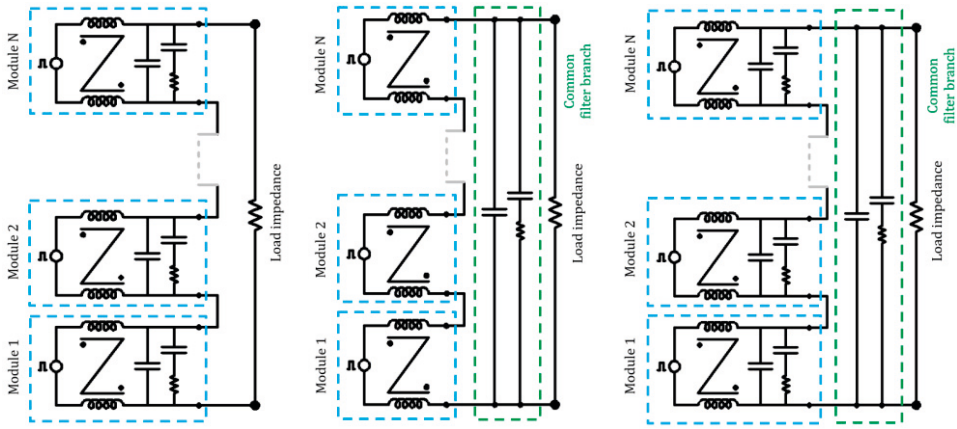



Figure 5.36: Possible filter configurations: a) each HV module has its own output filter; b) each HV module has its own filter inductor connected to a common filter branch shared by all HV modules; c) each HV module has its own output filter and is connected to a common filter branch shared by all HV modules.

Clearly, option B is theoretically advantageous as the common filter is designed for a much higher frequency (due to the interleaving effect between all modules) and as the required inductance may be split between the series connected modules. This solution is also advantageous if closed loop control of the output stage is desired as electronic damping can be provided with a single current measurement. These advantages formed the basis for its selection for the initial version of the technology demonstrator described in chapter 8. In practice, however, severe issues related to high frequency switched waveforms and their effect on the distributed capacitances of the geometry and – in turn – significant deterioration of the output pulse waveform were experienced. These issues were analysed in [5.23], and led to the decision to 1) instead adopt configuration C to mitigate high frequency effects between modules, and to 2) implement common mode filtering components (analysis and design of these components are described in section 5.3.7). Removal of the common output filter and re-design of the high voltage inductors, i.e., reverting to option A, proved to maintain effective filtering with reasonable pulse rise time and without significant increases to system size. Based on these experiences, filter configuration A has been chosen as the basis for the analysis in this chapter. Note that the developed analysis and design procedures may straightforwardly be adapted to either of the above filter configurations as needed.

As described, for this configuration each module output filter is to be designed to provide sufficient attenuation at $2f_{sw}$. Given 1) the limitations on the converter switching frequency, and 2) the imposed application flat top ripple constraint, the

classical LC filter with damped capacitor branch is used, Figure 5.37. This filter topology provides sufficient attenuation (-60 dB/decade) and effective damping of the filter resonance. Furthermore, as will be shown in the following sections, suitably compact and easy-to-construct filter arrangements may readily be developed.

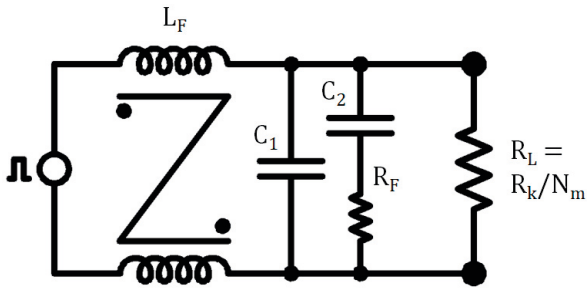



Figure 5.37: Classical LC filter with damped capacitor branch. The klystron load impedance is written on a per-module basis for convenience in filter analysis and design.

*Evaluation of filter circuit performance*

Filter design must be based on and ensure that modulator output pulse requirements are met. Here, it is convenient to treat filter analysis and design on a per-module basis, noting that for the chosen filter configuration, Figure 5.36.a, the complete modulator output pulse voltage may be obtained by adding the filtered output of $N_m$ modules.

The filter consists of an inductor $L_F$, a capacitor branch $C_1$ and a capacitor branch $C_2$ damped with resistor $R_F$. For a symmetrical module arrangement, each module may be considered responsible for $1/N_m$ of the modulator output, i.e., the equivalent klystron load impedance per module is given by $R_L = R_k/N_m$. From this, the per-module filter transfer function $G_F(s)$ is given by (5.112). Note that though this is a third order system, it is – in the interesting parameter region – strongly dominated by a pair of complex poles and may therefore be represented by an equivalent second order system. If $p_1$ and $p_2$ are the complex pole pair of $G_F(s)$, $\omega_n = \sqrt{p_1 p_2}$ and $\zeta = \frac{|p_1+p_2|}{2\omega_n}$, and the system may be written on the standard form of the second order system, (5.113).

$$G_F(s) = \frac{s\left[\frac{1}{L_F C_1}\right] + \left[\frac{1}{L_F C_1 C_2 R_F}\right]}{s^3 + s^2\left[\frac{R_L C_1 + R_L C_2 + R_F C_2}{C_1 C_2 R_L R_F}\right] + s\left[\frac{R_L R_F C_2 + L_F}{L_F C_1 C_2 R_L R_F}\right] + \left[\frac{1}{L_F C_1 C_2 R_F}\right]} \qquad (5.112)$$

$$G_F(s) \rightarrow \frac{\omega_n^2}{(s^2 + 2\zeta\omega_n s + \omega_n^2)} \tag{5.113}$$

As was shown in the preceding section, the filter input is a rectangular voltage waveform with amplitude $v_p(t) = \left(\left(V_p - \Delta V_p \frac{t}{T_p}\right)\left[\frac{2N_2}{N_1}\right] - V_{drop}\right)$, duty ratio $\delta$ and frequency $2f_{sw}$. For a given duty ratio, this waveform may be written as an even pulse function and is thereby represented by a cosine Fourier series, (5.114). Fourier analysis of this waveform reveals the Fourier coefficients $a_0$ and $a_n$ as (5.115)-(5.116). Here, $\omega_0 = 2\pi(2f_{sw})$ and $V_{drop} = V_i - 2V_{f,0}N_d - I_2 \sum R_{cu}$.

$$v_{F,in}(t) = a_0(t) + \sum_{n=1}^{\infty} a_n(\mathrm{t})\cos(n\omega_0 t) \tag{5.114}$$

$$a_0(t) = \delta v_p(t) \tag{5.115}$$

$$a_n = 2\frac{v_p(t)}{n\pi} sin(n\pi\delta) \tag{5.116}$$

Expectedly, the waveform average $a_0 = \delta v_p(t) = \delta\left(V_p - \Delta V_p \frac{t}{T_p}\right)$, i.e., the duty ratio must be increased throughout the pulse event to counteract the capacitor bank droop. This is important as the harmonic amplitudes are characterized by the factor $sin(n\pi\delta)$, i.e., as $\delta \rightarrow 1$ the harmonic coefficient $a_n \rightarrow 0$, Hence, in evaluating the worst case flat top ripple, only the minimum duty ratio $\delta_0$ – the duty ratio at the beginning of the pulse flat top – needs to be considered. Furthermore, as has been shown throughout the preceding sections, the major voltage drops depend primarily on load current, i.e., the minimum duty ratio and the corresponding voltage amplitude may conservatively be estimated from (5.117)-(5.118), respectively.

$$\delta_0 = \frac{V_2}{N_m\left[V_1\left[\frac{2N_2}{N_1}\right] - V_i - 2V_{f,0}N_d - I_2\sum R_{cu}\right]} \tag{5.117}$$

$$V_p(0) = \left(V_p\left[\frac{2N_2}{N_1}\right] - V_i - 2V_{f,0}N_d - I_2\sum R_{cu}\right) \tag{5.118}$$

To evaluate the worst case flat top ripple, a sum is taken over all waveform harmonics, attenuating each harmonic amplitude by the filter transfer function at the corresponding harmonic frequency. Here, it is noted that in the high frequency asymptotic region of the transfer function given by (5.112), the phase shift is approaching -180 degrees and is approximately constant. For this reason, the calculated voltage ripple values may be added algebraically. The peak-to-peak flat top ripple is then obtained by multiplying the evaluated sum by two, (5.119).

$$\Delta V_{pp} = 2\sum_{n=1}^{\infty} 2\frac{V_p(0)}{n\pi} sin(\pi n\delta_0)|G_F(j\omega)| \tag{5.119}$$

Finally, to evaluate the pulse rise time, a step response of (5.113) is studied. During the pulse rise, control is used to set $\delta \to 1$ in order to reach the flat top amplitude as fast as possible. Furthermore, with $t_r \ll T_p$, $V_p - \Delta V_p \frac{t_r}{T_p} \approx V_p$, and the pulse rise time may be evaluated according to (5.120).

$$t_r = \min\left(t : L^{-1}\left\{N_m\left(V_p\left[\frac{2N_2}{N_1}\right] - V_i - 2V_{f,0}N_d - I_2\sum R_{cu}\right)\theta(s)G_F(s)\right\} \geq 0.99V_2\right) \tag{5.120}$$

*Modeling of high voltage inductor*

To be compact and simple to manufacture, the filter inductor is based on a tapewound double C core with magnetic cross-section $x_c y_c$. The cores are cut and $K_g$ air gap spacers are introduced per core leg to control the inductance. Two windings, each with $N_2$ winding turns, are used and connected in series to boost the differential mode inductance. Here, single layer windings are preferred given the high voltage. Note that since the filter inductor forms the output of the high voltage module, a distance $d_o$ is introduced above the winding sets to facilitate connection.

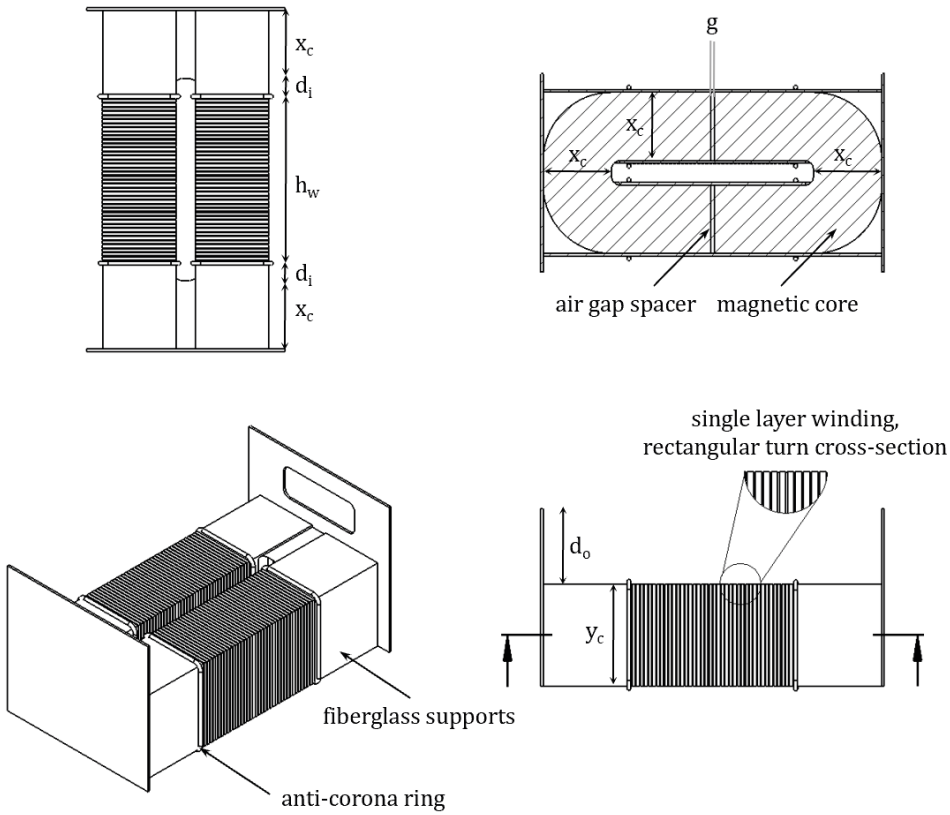



Figure 5.38: Overview of high voltage inductor geometry

As with the high voltage high frequency transformer, rectangular winding turns are used and the winding turn thickness is set in relation to the skin depth, (5.83) and (5.121). Again, setting the winding turn height according to (5.122) allows use of the same copper strip. For a per-turn isolation distance $d_y$, this choice results in a winding height according to (5.123).

$$t_w = 2\delta_d \tag{5.121}$$

$$w_h = \frac{I_2\sqrt{T_p f_r}}{J t_w} \tag{5.122}$$

$$h_w = N_2 w_h + d_y(N_2 - 1) \tag{5.123}$$

In this formulation, the core leg width ($x_c$), the number of turns per winding ($N_2$), the length per air gap ($g$), and the filter inductance value ($L_f$) are considered fundamental design parameters. This choice of design parameters is further discussed in the conclusion of this subsection. With this formulation, the required magnetic core depth is given by (5.124). In addition, the resulting peak magnetic flux density is given by (5.125), and must be limited to some value $B_{max}$. Here, $\sigma_f$ is the fringe field factor. In this work, $\sigma_f$ is calculated using the conformal Schwarz-Christoffel transformation as described in [5.8]-[5.9].

$$L_F = \frac{2\mu_0 k_f x_c y_c N_2^2}{\sigma_f K_g g} \rightarrow y_c = \frac{L_f \sigma_f K_g g}{2\mu_0 k_f x_c N_2^2} \tag{5.124}$$

$$\hat{B} = \frac{\mu_0 N_2}{\sigma_f K_g g} I_2 \leq B_{max} \tag{5.125}$$

From the above definitions, the winding turn cross-sectional area is given by (5.126) and the winding turn mean path length is given by (5.127). From this, the average inductor losses are estimated according to (5.128).

$$[A_{cu}]_L = t_w w_h \tag{5.126}$$

$$[MPL]_L = 2x_c + 2y_c \tag{5.127}$$

$$\bar{P}_{Lf} = \rho_{cu} F J^2 (2N_2)[MPL]_L [A_{cu}]_L \tag{5.128}$$

Finally, the extents volume of the filter inductor unit is given by (5.129)-(5.131) according to the definitions made in Figure 5.38.

$$W_{Lf} = h_w + 2x_c + 2d_i \tag{5.129}$$

$$D_{Lf} = 2x_c + 5d_i \tag{5.130}$$

$$H_{Lf} = y_c + 2d_i \tag{5.131}$$

To model the parasitic capacitances associated with the high voltage inductor and its surroundings, it is noted that, as indicated in Figure 5.49, the inductor is placed in-between the filter capacitor arrangement and the HV rectifier and common mode choke inductor. A worst-case estimate of the associated stray capacitance is thereby

assuming that the adjacent components as well as the module enclosure are at ground potential. Here, the overview presented in Figure 5.39 may be used. As can be seen, three distinct capacitances are of interest- 1) the capacitance between the inductor windings and the surroundings; 2) the capacitance between the inductor windings and the grounded magnetic core; and 3) the capacitance between the two inductor windings.

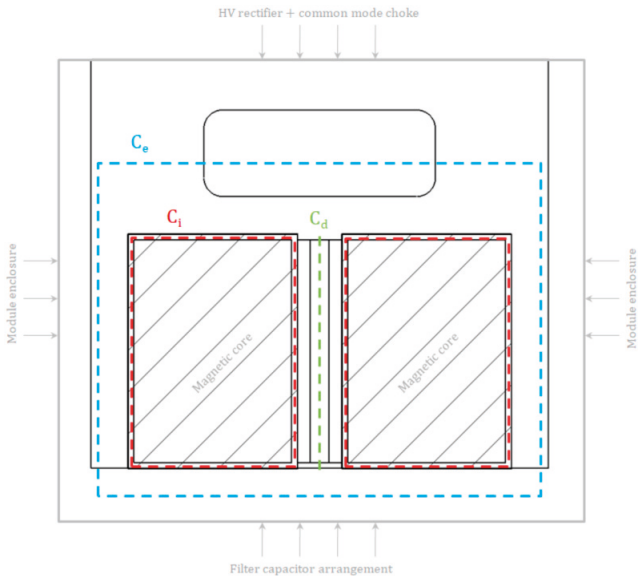



Figure 5.39: Cross-section of high voltage inductor arrangement used in modeling of stray capacitance

The capacitances between the inductor windings and the enclosure, Figure 5.49, and between the inductor windings and the grounded magnetic core are geometrically similar and may generally be estimated according to (5.132). Noting that, similar to the HVHF transformer, the inductor windings are series connected, the capacitances may be estimated from (5.133)-(5.134).

$$W_e = \frac{1}{2}\varepsilon_0\varepsilon_r \frac{l}{h_w}\int_0^{h_w} \frac{\left(V_{s,0}h_w + \left(\hat{V}_s - V_{s,0}\right)y\right)^2}{d_i h_w} dy \tag{5.132}$$

$$C_e = \frac{2W_{e,e,a}}{\hat{V}_a} + \frac{2W_{e,e,b}}{\hat{V}_b} = \frac{1}{2}\left(\frac{4}{3}\right)\varepsilon_0\varepsilon_r\left(\frac{h_w l_e}{d_i}\right) \tag{5.133}$$

$$C_i = \frac{2W_{e,i,a}}{\hat{V}_a} + \frac{2W_{e,i,b}}{\hat{V}_b} = \frac{1}{2}\left(\frac{4}{3}\right)\varepsilon_0\varepsilon_r\left(\frac{h_w l_i}{d_t}\right) \tag{5.134}$$

Then, the region between the two inductor windings is geometrically equivalent to region 5 of the pulse transformer geometry. Using that $d_i = d_0$, the stored electrical energy and the corresponding capacitance may be estimated by (5.135)-(5.136).

$$W_{e,d} = \frac{1}{2}\varepsilon_0\varepsilon_r h_w l_d \left(\hat{V}_s/2\right)^2 \int_0^{h_w} \frac{1}{d_i h_w} dy \tag{5.135}$$

$$C_d = \frac{1}{8}\varepsilon_0\varepsilon_r \left(\frac{h_w l_d}{d_i}\right) \tag{5.136}$$

The complete equivalent circuit representation of the HV inductor integrates the differential mode inductance $L_f$ with the estimated capacitive elements $C_e$, $C_i$ and $C_d$ as well as with the estimated winding resistance, Figure 5.40.

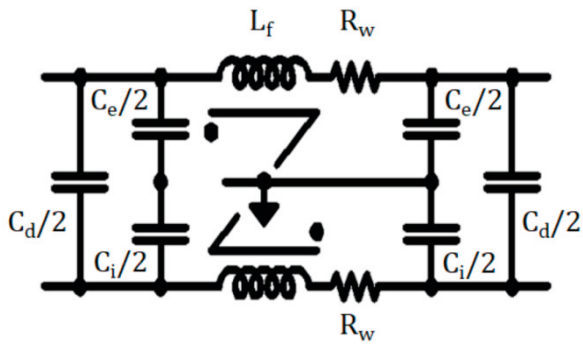



Figure 5.40: Complete equivalent circuit representation of high voltage inductor

*Modeling of filter capacitor arrangement*

As discussed, and as shown in Figure 5.49, the filter capacitor arrangement is placed underneath the filter inductor, towards the bottom of the enclosure. The filter capacitors $C_1$ and $C_2$ are implemented by an arrangement of parallel connected high voltage capacitors with nominal capacitance $C_n$. Since $C_1$ and $C_2$ have a common high voltage terminal, the comprising capacitors are all connected to a common upper copper plate. Then, individual copper plates are used to connect the capacitors comprising $C_1$ and $C_2$, respectively. The copper plate connecting to $C_1$ is grounded, whereas the copper plate connecting to $C_2$ is connected to ground via an assembly of resistors comprising $R_F$. In addition, a number of high voltage bleeder resistors are fixed between the upper and lower copper plates. Since $R_F$ and the bleeder

resistors virtually do not impact the geometry of the arrangement, they have been excluded from the overview presented in Figure 5.41.

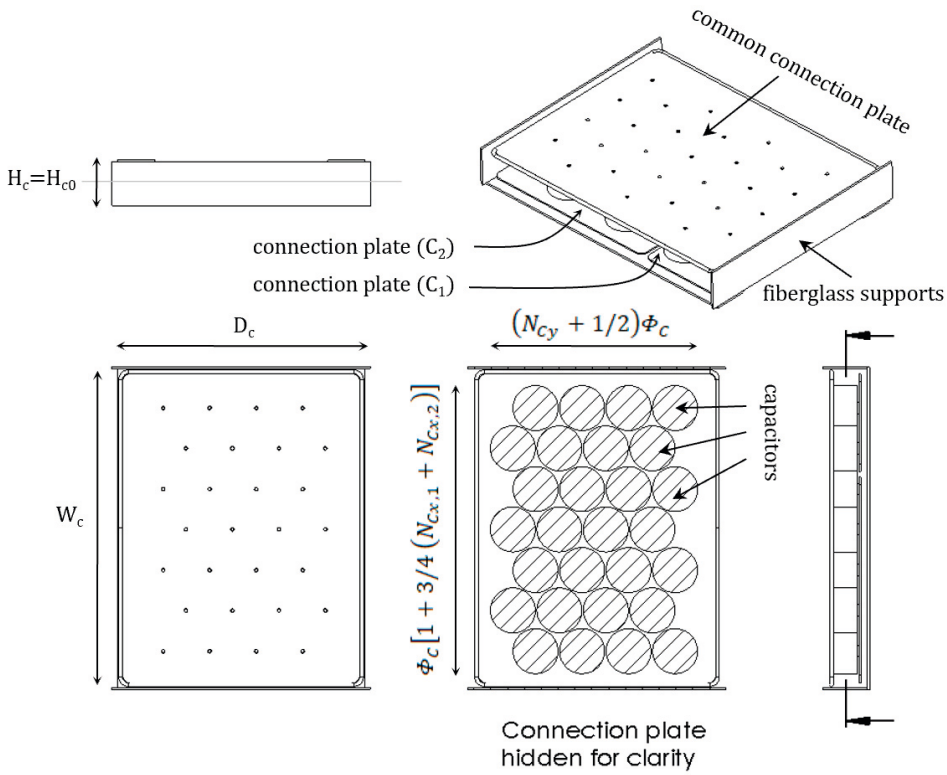



Figure 5.41: Overview of capacitor arrangement (resistors are hidden for clarity).

In this formulation, the number of capacitor rows per group in the widthwise direction, i.e., $N_{Cx,1}$ and $N_{Cx,2}$, as well as the number of capacitor columns $N_{Cy}$, constitute the main design parameters. Selecting these design parameters yields the effective capacitances $C_1$ and $C_2$ according to (5.137)-(5.138).

$$C_1 = N_{Cx,1} N_{Cy} C_n \tag{5.137}$$

$$C_2 = N_{Cx,2} N_{Cy} C_n \tag{5.138}$$

In addition, the extents volume is given by (5.139). Here, $\emptyset_c$ and $H_{C0}$ are the diameter and height of the capacitor unit, respectively.

$$V_C = D_C W_C H_C$$

$$= \begin{cases} N_{Cx,1} \vee N_{Cx,2} > 1: & \begin{pmatrix} D_C = (N_{Cy} + 1/2)\Phi_C \\ W_C = \Phi_C[1 + 3/4\,(N_{Cx,1} + N_{Cx,2})] \\ H_C = H_{C0} \end{pmatrix} \\ N_{Cx,1} \wedge N_{Cx,2} = 1: & \begin{pmatrix} D_C = N_{Cy}\Phi_C \\ W_C = \Phi_C[1 + N_{Cx,2}] \\ H_C = H_{C0} \end{pmatrix} \end{cases} \tag{5.139}$$

*Design of high voltage output filter*

In summary, design of the high voltage output filter involves selecting the value of 7 design parameters: the inductor core leg width ($x_c$), the inductor number of turns per winding ($N_2$), the length per inductor air gap ($g$), the filter inductance ($L_f$); the number of capacitor rows per group in the widthwise direction, i.e. $N_{Cx,1}$ and $N_{Cx,2}$, the number of capacitor columns $N_{Cy}$, and the filter damping resistance $R_F$. Following selection of the above design parameters, the filter component extents volume, losses, and corresponding filter performance is evaluated as described in the preceding sections and as summarized in Figure 5.42.

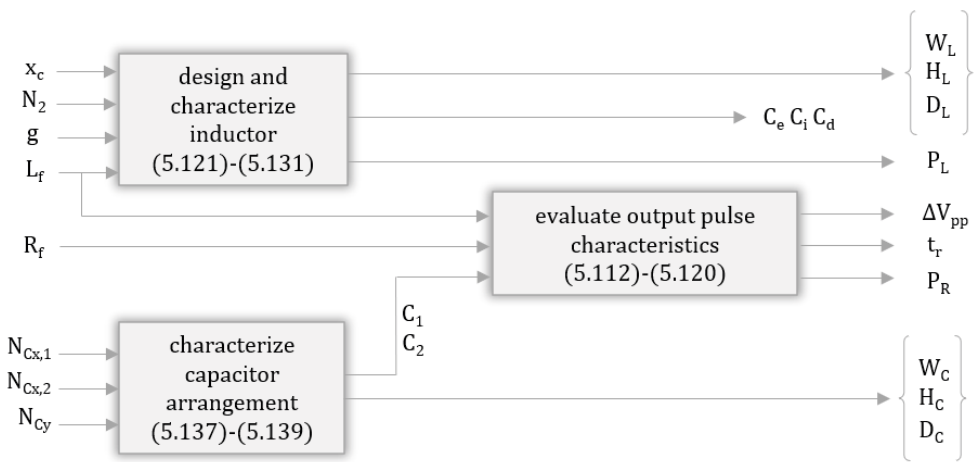



Figure 5.42: High voltage output filter evaluation procedure

*Discussion on filter design objectives*

In the above formulation of the filter design problem, the geometrical properties of the output filter components are considered design parameters and their impact on the output pulse waveform are assessed with respect to imposed application

requirements. It should be noted that it is also possible to reverse the formulation, i.e., by defining a given filter performance, one could calculate viable combinations of the filter circuit parameters for which an optimal geometry could be derived. Also note that, given the nature of the intended application, focus is put on minimizing system volume and dissipated power whereas, e.g., pulse rise time and flat top ripple are constrained, though these could be also included in a weighted objective function.

### 5.3.7 Common mode mitigation

In the preceding sections, detailed models of the stray capacitive elements of each main pulse power generator component have been derived. As indicated in Figure 5.43.a, depicting the complete output stage circuit representation including stray elements, these parasitic elements form paths for capacitive currents excited by the common mode voltage component of the high frequency waveform generated by the H-bridge power converters. Here, the complete output stage circuit representation may be transformed into an equivalent circuit appropriate for common mode analysis, Figure 5.43.b. This circuit is used in the following to develop a procedure for selection and design of an appropriate common mode inductor $L_{cm}$, representing a common mode impedance to be placed in the main path of propagation.

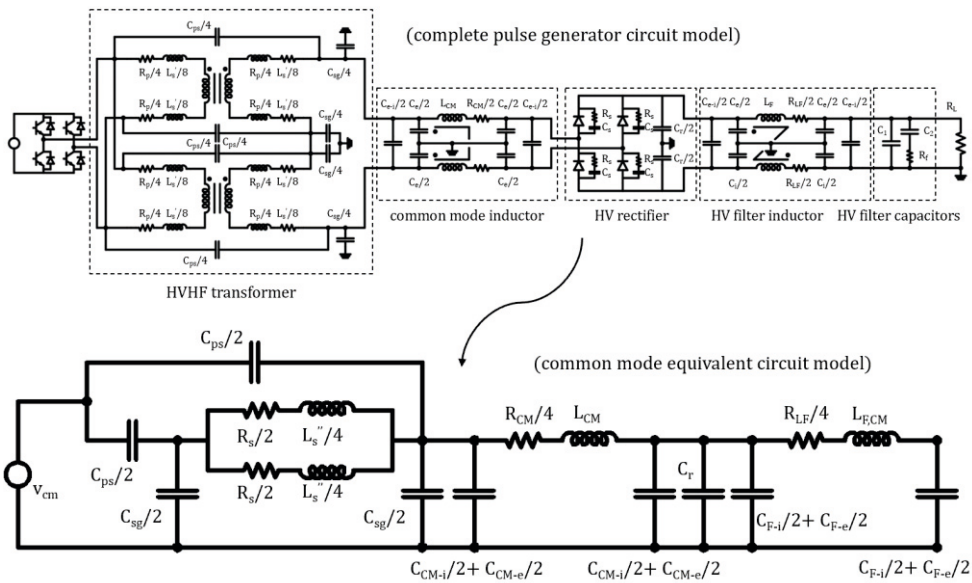



Figure 5.43: a) complete output stage circuit representation including stray elements; b) equivalent circuit representation from common mode perspective.

First, the common mode component of the H-bridge converter output voltage waveforms is given by (5.140). Considering the voltage from each H-bridge converter output leg to ground, Figure 5.44, it is immediately clear that (5.140) yields a voltage component with half the amplitude $(V_1/2)$ and twice the frequency $(2f_{sw,HB})$. Importantly, $L_{cm}$ is to be designed such that, under this common mode excitation, the resulting common mode current through the inductor, i.e., entering the system output, is appropriately attenuated.

$$v_{cm} = \frac{v_{a-g} + v_{b-g}}{2} \tag{5.140}$$

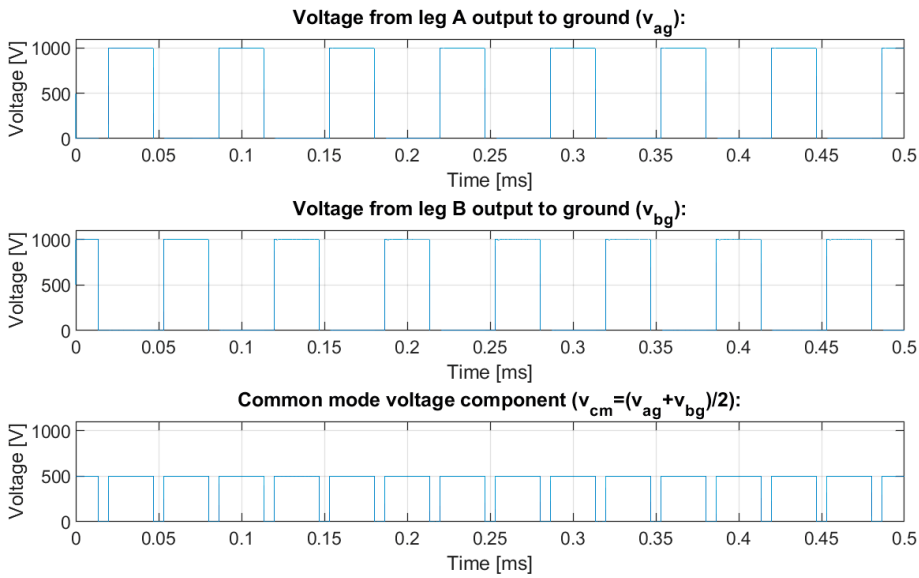



Figure 5.44: Common mode voltage

Now, considering the equivalent circuit presented in Figure 5.43, a unique transfer function from the exciting common mode voltage to the common mode current through the mitigating inductor cannot be found. However, as indicated in Figure 5.45, it may be demonstrated that by placing the lumped capacitance corresponding to the stored energy between the secondary windings and the transformer magnetic core in parallel with the lumped capacitance representing part of the stored energy between the primary and secondary windings, a close to identical frequency response is attained. Fortunately, the resulting circuit enables straightforward derivation of the above-described transfer function from exciting common mode voltage to resulting system common mode current, (5.141)-(5.144).

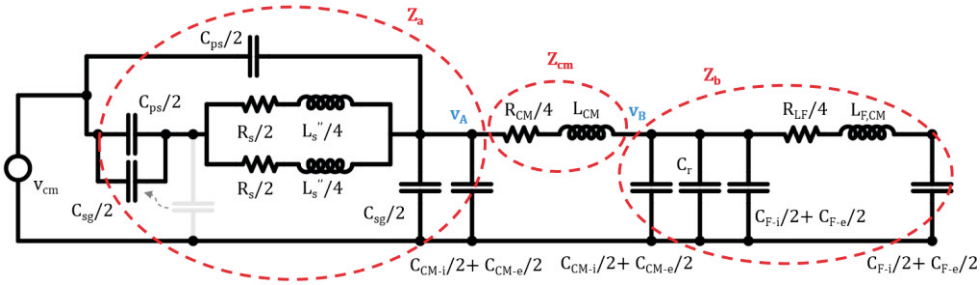



Figure 5.45: Further simplification of equivalent circuit to permit calculation of system common mode current

$$Z_{Lcm} = R_{cm}/4 + sL_{cm} \tag{5.141}$$

$$v_A = v_{cm}\frac{Z_a + Z_{cm}}{Z_a + Z_{cm} + Z_b} \tag{5.142}$$

$$v_B = v_{cm}\frac{Z_b}{Z_a + Z_{cm} + Z_b} \tag{5.143}$$

$$i_{Lcm} = \frac{v_A - v_B}{Z_{cm}} = v_{cm}\frac{Z_a + Z_{cm} - Z_b}{Z_{Lcm}(Z_a + Z_{cm} + Z_b)}$$
$$\rightarrow G_{cm}(s) = \frac{i_{Lcm}}{v_{cm}} = \frac{Z_a + Z_{cm} - Z_b}{Z_{Lcm}(Z_a + Z_{cm} + Z_b)} \tag{5.144}$$

The frequency response of a sample $G_{cm}(s)$ is studied in Figure 5.46. Here, $L_{cm}$ is to be designed such that 1) the resonant peak is below the exciting frequency, and that 2) the resulting common mode current is below some value $\hat{\imath}_{cm}$. The reasoning for this is as follows. The resonance frequency of $G_{cm}(s)$, as indicated in Figure 5.46, has a tendency to decrease with both increasing $L_{cm}$ and increases to any of the above modeled stray capacitive elements. Following design, the actual value of $L_{cm}$ is known with relatively good accuracy, typically within, e.g., ~5%. The stray capacitance values, on the other hand, are significantly more difficult to estimate accurately as, e.g., they depend strongly on their surroundings. Still, experience shows that these values are more often than not underestimated, i.e., it appears advantageous to place the resonance frequency below that of the exciting frequency such that potential estimation inaccuracies imply that the resonance frequency diverges from the exciting frequency as opposed to the other way around.

Based on the above analysis, the following procedure is proposed in selecting $L_{cm}$. Once the other main power components of the pulse generator circuit have been designed, the associated parasitic elements are estimated using the methods developed in the preceding sections. Then, $L_{cm}$ is chosen through iteration such that

(5.145) and (5.146) are satisfied. Here, Δ represents assurance that a proper margin between the exciting frequency and the circuit resonance frequency is maintained.

$$f_0(G_{cm}) \leq 2f_{sw,HB}(1-\Delta) \tag{5.145}$$

$$i_{Lcm} \leq \hat{\imath}_{cm} \tag{5.146}$$

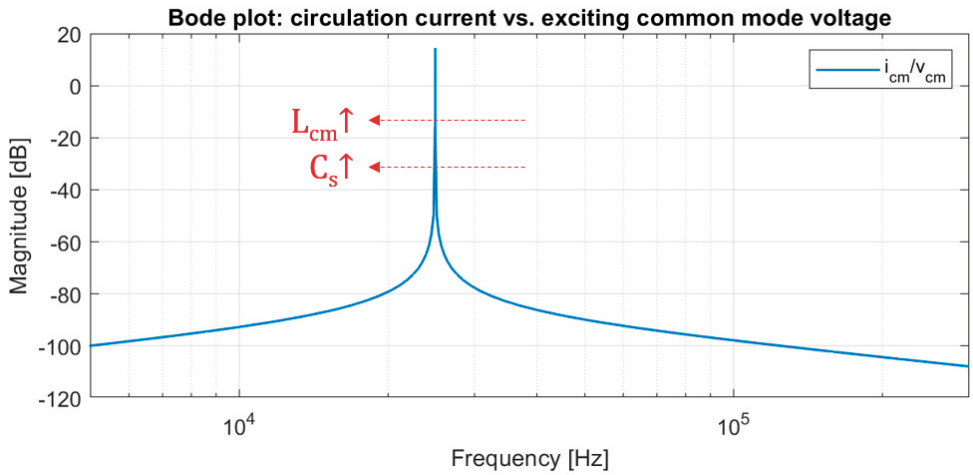



Figure 5.46: Bode plot of $G_{cm}(s)$

Then, once the circuit value $L_{cm}$ has been selected, the component itself must appropriately be designed. Here, a design based on high permeability nanocrystalline core material is proposed to ensure good performance at high frequency excitation, Figure 5.47. Uncut cores with magnetic cross-section $x_c y_c$ may straightforwardly be used to boost the resulting inductance as the exciting current is limited to some small value $\hat{\imath}_{cm}$. Two windings, each with $N_2$ winding turns, are used. As with the high voltage high frequency transformer, rectangular winding turns are used and the winding turn thickness is set in relation to the skin depth, (5.147). Again, setting the winding turn height according to (5.148) allows use of the same copper strip. For a per-turn isolation distance $d_y$, this choice results in a winding height according to (5.149).

$$t_w = 2\delta_d \tag{5.147}$$

$$w_h = \frac{I_2\sqrt{T_p f_r}}{J t_w} \tag{5.148}$$

$$h_w = N_2 w_h + d_y(N_2 - 1) \tag{5.149}$$

In this formulation, the core leg width ($x_c$) and the number of turns per winding ($N_2$) are considered fundamental design parameters. With this formulation, the required magnetic core depth is given by (5.150). In addition, the resulting peak magnetic flux density is given by (5.151), and must be limited to some value $B_{max}$.

$$L_F = \frac{\mu_0 \mu_r k_f x_c y_c N_2^2}{l_c} \rightarrow y_c = \frac{L_f \left(2h_w + 2d_i + \frac{4}{2}\pi(x_c/2) + d_i\right)}{\mu_0 \mu_r k_f x_c N_2^2} \tag{5.150}$$

$$\hat{B} = \frac{\mu_0 \mu_r N_2}{\left(2h_w + 2d_i + \frac{4}{2}\pi(x_c/2) + d_i\right)} i_{Lcm} \leq B_{max} \tag{5.151}$$

From the above definitions, the winding turn cross-sectional area is given by (5.152) and the mean path length of the turns of the two windings is given by (5.153)-(5.154), respectively. From this, the average inductor losses are estimated according to (5.155).

$$[A_{cu}]_{Lcm} = t_w w_h \tag{5.152}$$

$$[MPL]_{Lcm,a} = 2x_c + 2y_c \tag{5.153}$$

$$[MPL]_{Lcm,b} = 2(x_c + 2d_i) + 2(y_c + 2d_i) \tag{5.154}$$

$$\bar{P}_{Lcm} = \rho_{cu} F J^2 N_2 [A_{cu}]_{Lcm} \left([MPL]_{Lcm,a} + [MPL]_{Lcm,b}\right) \tag{5.155}$$

Finally, the extents volume of the common mode inductor is given by (5.156)-(5.158) according to the definitions made in Figure 5.47.

$$W_{Lcm} = h_w + 2x_c + 2d_i \tag{5.156}$$

$$D_{Lcm} = y_c + 4d_i \tag{5.157}$$

$$H_{Lcm} = 2x_c + 5d_i \tag{5.158}$$

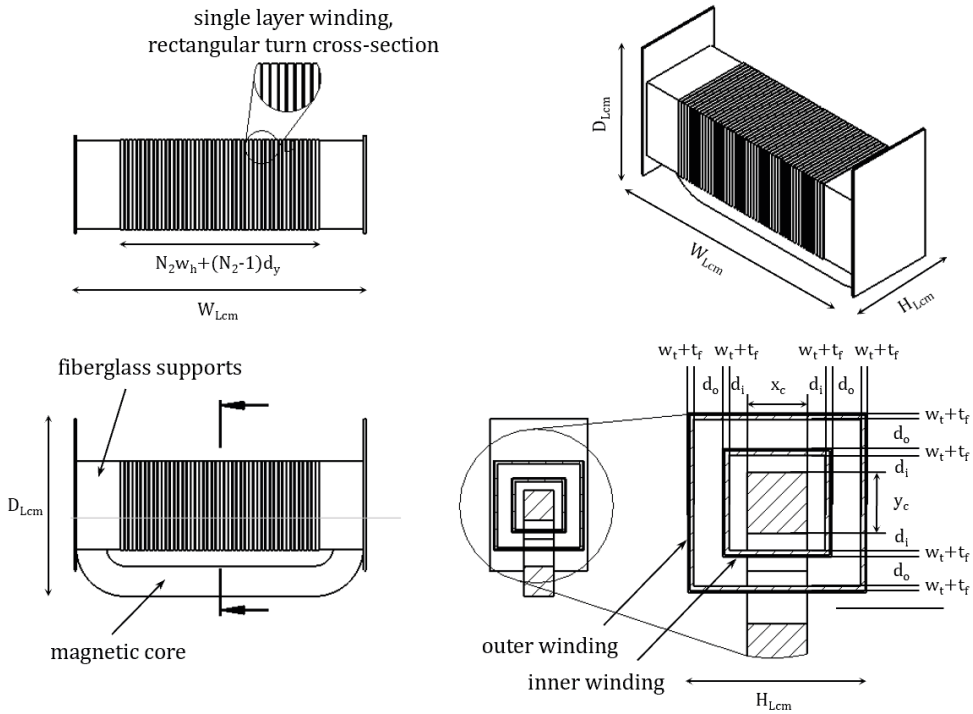



Figure 5.47: Common mode inductor design drawing.

### 5.3.8 Complete optimization procedure for SML pulse generation stage

In this section, the design models developed in the preceding sections are integrated in a unified framework for optimization of the complete SML modulator output stage. The complete framework is presented in Figure 5.48 and is discussed in the following. It is pointed out that the depicted overview may appear deceptively simple. Importantly, it should be noted that-

- Several of the chosen design parameters affect multiple components in different ways. It is not always evident what the consequence of a given change will be in terms of, e.g., system volume or system efficiency.
- The common objective function is highly coupled to each of the comprising components. Furthermore, as multiple components are to be geometrically stacked on one another, Figure 5.49, slight increases in one dimension of a single component may lead to significant/non-negligible increases in system volume.
- Multiple constraints require complete assessment of each output stage component. Again, due to their impact on multiple components, it is not

always evident which (or how) design parameter(s) should be changed to best ensure solution feasibility.

- Satisfying all of the above while ensuring convergence, in particular towards optimality, is non-trivial.

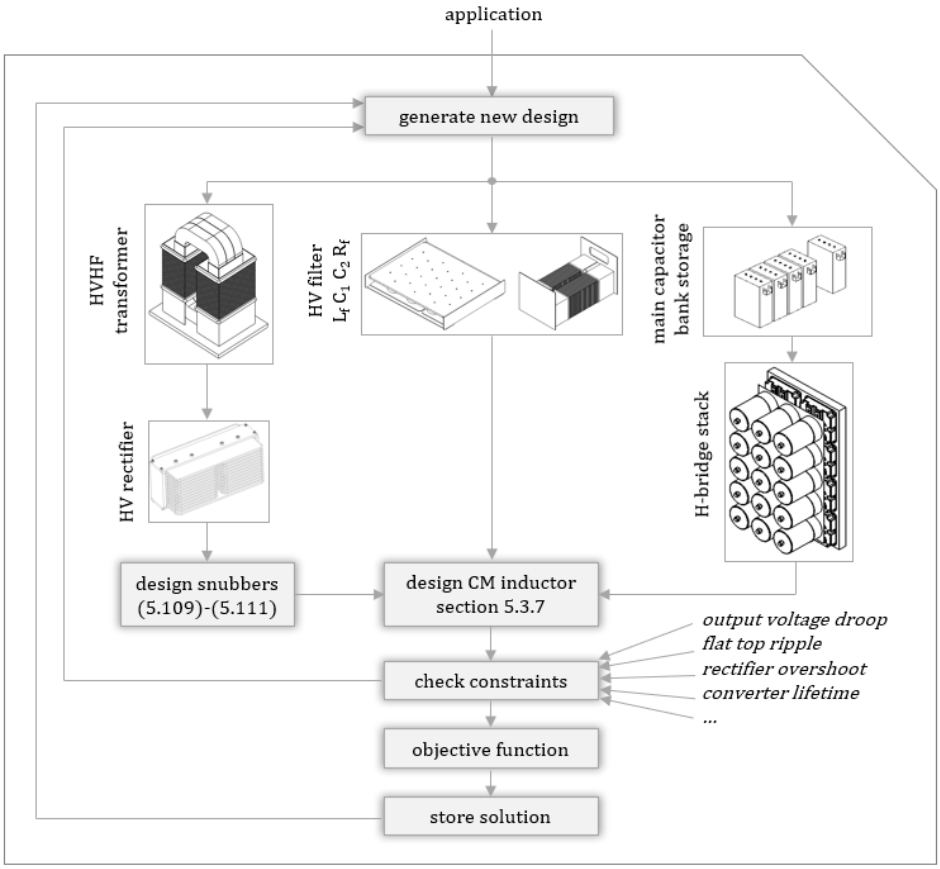



Figure 5.48: Optimization routine for SML-based pulse generator

In this work, high voltage module integration as proposed in Figure 5.49 has been considered. Here, the high voltage rectifier, the high voltage output filter and the high voltage common mode inductor are enclosed in a metallic box (termed high voltage box) placed next to the high voltage high frequency transformer. In such a configuration, it is clear that, e.g., minimizing the volume of each component independently does not ensure a globally optimal solution. Instead, the objective function must properly incorporate the dimensions of each component, (5.159)-(5.162).

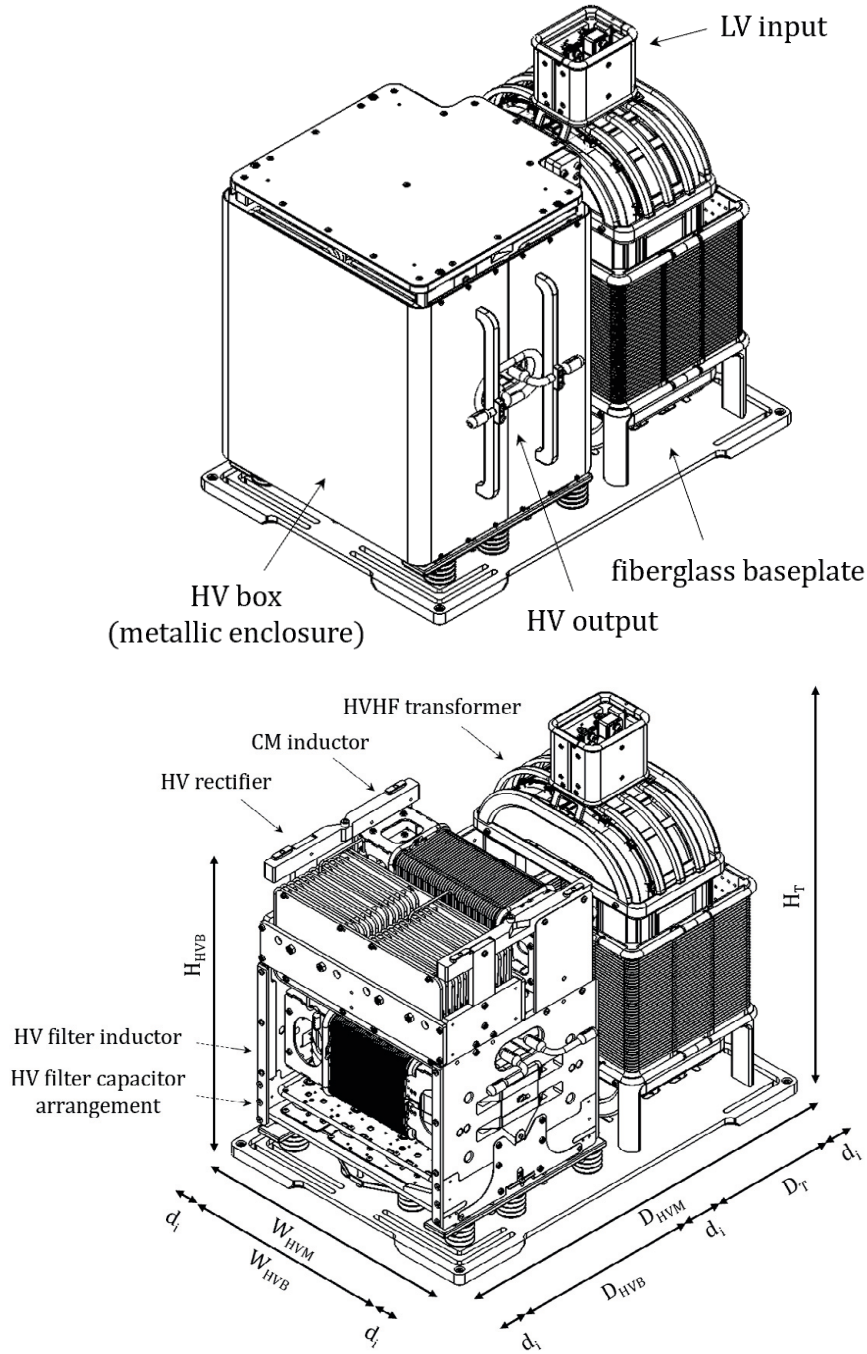



Figure 5.49: Proposed integration of high voltage module

$$W_{HVB} \approx \max\left(W_C, W_{Lf}, W_{HVR}, W_{Lcm}\right) \tag{5.159}$$

$$D_{HVB} \approx max\left(D_c, D_{Lf}, D_{HVR}, D_{Lcm}\right) \tag{5.160}$$

$$H_{HVB} \approx H_C + H_{Lf} + max(H_{HVR}, H_{Lcm}) \tag{5.161}$$

$$V_{HVM} = W_{HVM} D_{HVM} H_{HVM} = \begin{Bmatrix} W_{HVM} & max(W_{HVB}, W_T) + 2d_i \\ D_{HVM} & D_{HVB} + D_T + 3d_i \\ H_{HVM} & max(H_{HVB}, H_T) \end{Bmatrix} \tag{5.162}$$

Of course, the volume of the high voltage module – placed in oil – must then be appropriately weighed against the volume of the components placed in air, i.e., the H-bridge converter and the main capacitor bank. Here, this is arranged by introducing a weighting factor $k_v$. Finally, the total adjusted volume is weighed against the total system losses in formulating the objective function, (5.163). Here, the sweeping factor $K$ is again included to study trade-offs between volume and efficiency.

$$f_{obj} = K[V_{HVM} + k_v(V_{HB} + V_{cbk})] + (1 - K) \cdot \left[4N_{m,HB}\bar{P}_{IGBT} + \left(\bar{P}_{t,fe} + \bar{P}_{t,cu,p} + \bar{P}_{t,cu,s}\right) + \bar{P}_{HVR} + \bar{P}_s + \bar{P}_{Lf} + \bar{P}_{Lcm}\right] \tag{5.163}$$

## 5.4 Complete optimization routine for SML modulators

The previous two sections have independently treated modeling and design of the components comprising a single input charger stage and a single output pulse generation stage of the SML modulator topology, respectively. As usual, this functional division is possible due to the decoupling provided by the main capacitor bank. It is noted that, here, the main capacitor bank has been considered part of the pulse generation stage. Of course, selection of the main capacitor bank voltage $V_1$ has important consequences for both modulator stages and thus the entire modulator design. However, in this work, $V_1$ has been set to ~1 kV in – primarily – permitting use of standardized off-the-shelf semiconductor components. Hence, as 1) the capacitor bank droop has minimal impact on input charger design while 2) imposing fundamental constraints on pulse generator circuit design, it is practical to include aspects of capacitor bank modeling in the latter without loss of generality. Still, it should be clear that – in attempting to derive a globally optimal complete modulator

system – the impacts and limitations of both systems should be taken into account concurrently despite the aforementioned division of the design problem. As an example, if the input stage in some application by nature is an order of magnitude smaller than the corresponding output stage, it makes little sense to independently optimize the input stage for volume and combining the results.

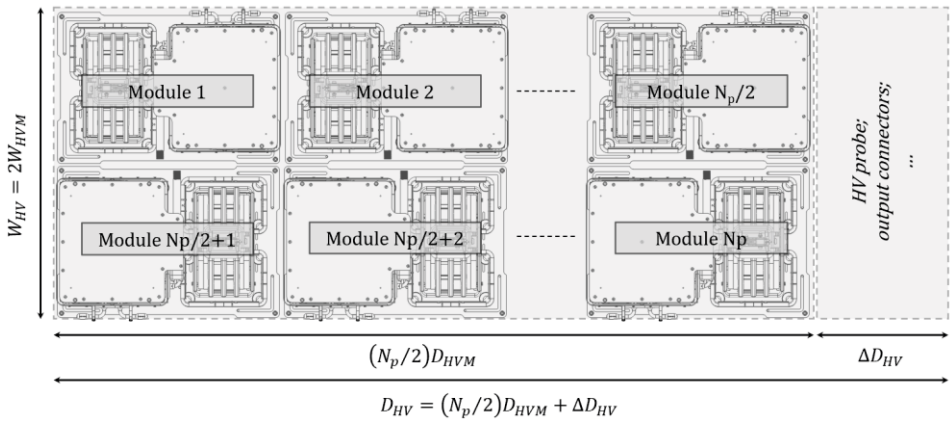
In this section, a complete modulator layout and design procedure is proposed based on 1) the relative contributions of the comprising components to, e.g., system size and efficiency, as derived in 2) attempting to logically position the components with respect to their respective circuit function. In addition, the fundamental aspects of modularity, i.e., selecting the number of input charger and output pulse generator circuits are discussed. Finally, the developed optimization routine is used in studying the case of the ESS klystron modulator application. This design work forms the basis for the practical implementation of the SML modulator topology as outlined in chapters 8-9. The optimization routine is also used in comparing the proposed and developed modulator topology to the conventional pulse transformer-based modulator topology in chapter 6.

### 5.4.1 Proposed modulator layout

In this section, a possible layout integrating the input charger stage and the output pulse generator stage in forming a complete modulator system is proposed-

It is first pointed out that the layout of the high voltage assembly is relatively fixed. Here, $N_p$ high voltage modules, Figure 5.49, are to be interconnected in forming a common high voltage output. From a practical standpoint, these modules should be placed in a rectangular grid. Then, considering a reasonable level of modularity with, e.g., $N_p = 4 \ldots 8$, this implies an arrangement with either one or two columns comprising the $N_p$ modules. In addition, a small high voltage output stage providing connection of the modulator system to the load klystrons, room for the high voltage sensor, etc., is necessary. The above considerations and the resulting high voltage system dimensions are summarized in the proposed high voltage oil tank layout suggested in Figure 5.50.

a)




b)

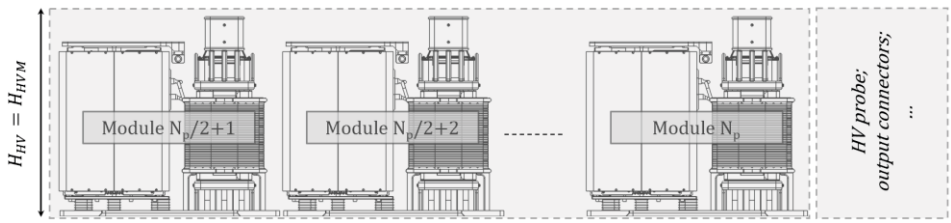



Figure 5.50: Proposed layout of high voltage oil tank assembly- a) top-down view; b) side-view

Given the limited height of the proposed oil tank assembly (essentially equal to the height of the high voltage module, Figure 5.49), it is suitable to place the corresponding low voltage system on top of the high voltage oil tank assembly. Here, it is preferable to place the H-bridge power stacks just above each high voltage module in minimizing the length of the busbars interconnecting the H-bridge power stacks to their corresponding high voltage module, Figure 5.51. Here, low inductance busbars are to be utilized, and are to be fed-through to the high voltage oil tank assembly using low voltage feedthroughs.

Then, the H-bridge power stacks are sourced from the main capacitor bank energy storage. Importantly, as was shown in section 5.3.2, the energy storage is based on rectangular capacitor units in maximizing stored energy per unit volume.

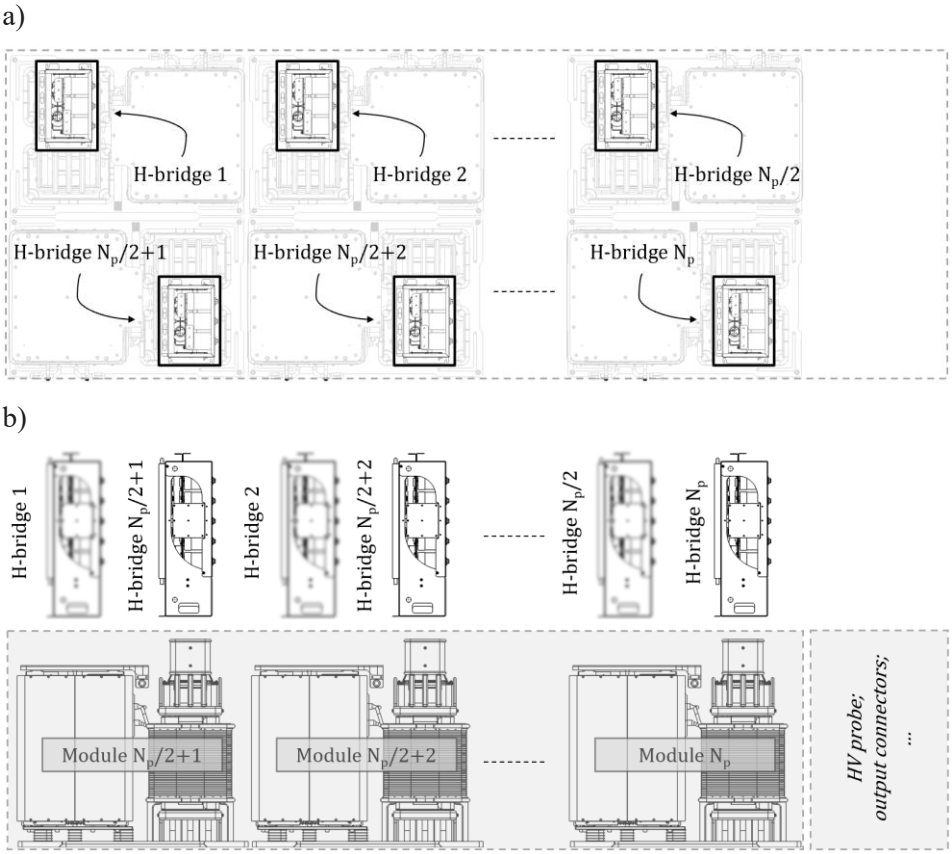



Figure 5.51: Proposed placement of H-bridge stacks on top of high-voltage modules- a) top-down view; b) side-view

Using the ESS klystron modulator requirements as illustration, designing a capacitor bank energy storage for a nominal primary voltage of ~1 kV and considering a capacitor bank between 10…20% would require a total capacitor bank (i.e., shared between the $N_p$ pulse generators) of (several) hundreds of mF. With state-of-the-art commercially available high energy density capacitors, e.g., [5.17], this corresponds to ~20 capacitor units, each with size ~575x430x175 mm$^3$. Clearly, the main capacitor bank energy storage plays a significant part in defining the size of the modulator. In this work, it is proposed that these capacitor units are to be placed in columns in the space provided in-between the H-bridge power stacks as shown in Figure 5.52. Should additional space be required to fit the necessary capacitors, additional columns of capacitors may be placed – potentially in geometrically alternative configuration – either 1) on either side of each column of H-bridges, or 2) in another layer on top of the first column of capacitors.

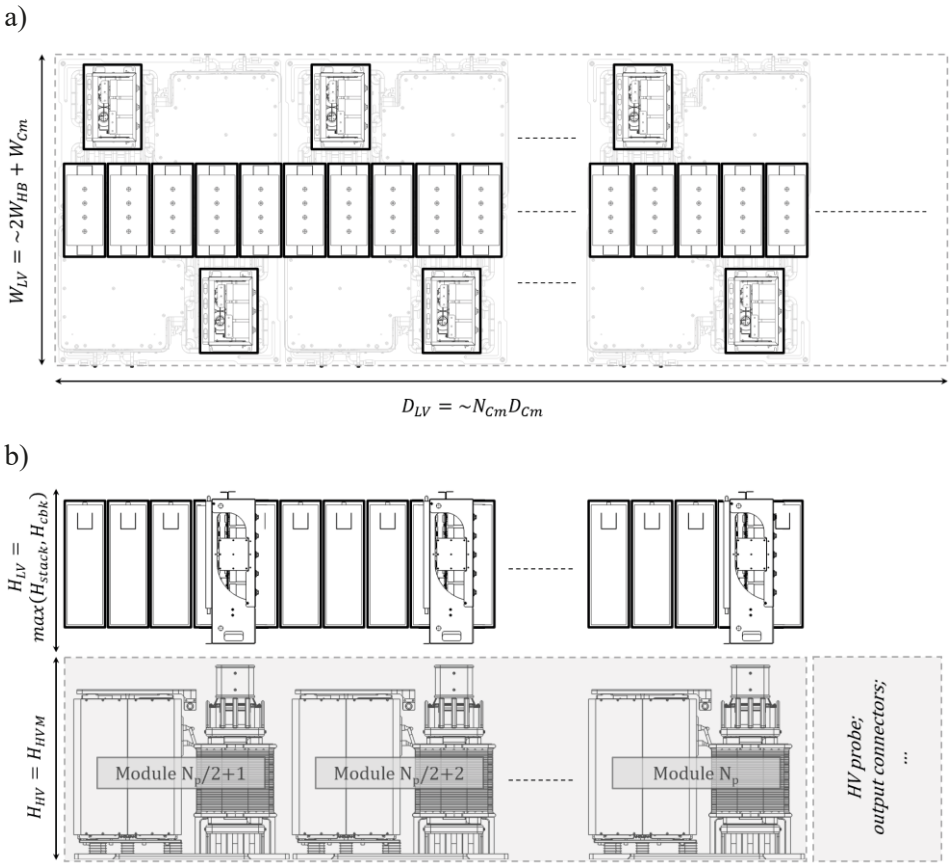



Figure 5.52: Proposed placement of capacitor bank storage connecting to H-bridges- a) top-down view; b) side-view

Finally, the input capacitor charger systems are each rated and designed for part of the average power of the modulator system. Based on this, it is suggested that these could be designed to fit in the space in-between the H-bridges and the main capacitor bank units, Figure 5.53. Here, it may be seen that – though this selection is not obvious - $N_c = N_p/2$ does provide a certain symmetry while leaving room for, e.g., the control system, signal acquisition systems, and so on. Of course, the ratio between the modulator average power and peak power ratings, e.g., could greatly influence the practicality of this arrangement, and should be carefully considered in view of each application. Finally, a common input stage containing, e.g., the main circuit breaker, EMC filtering, etc., is included.

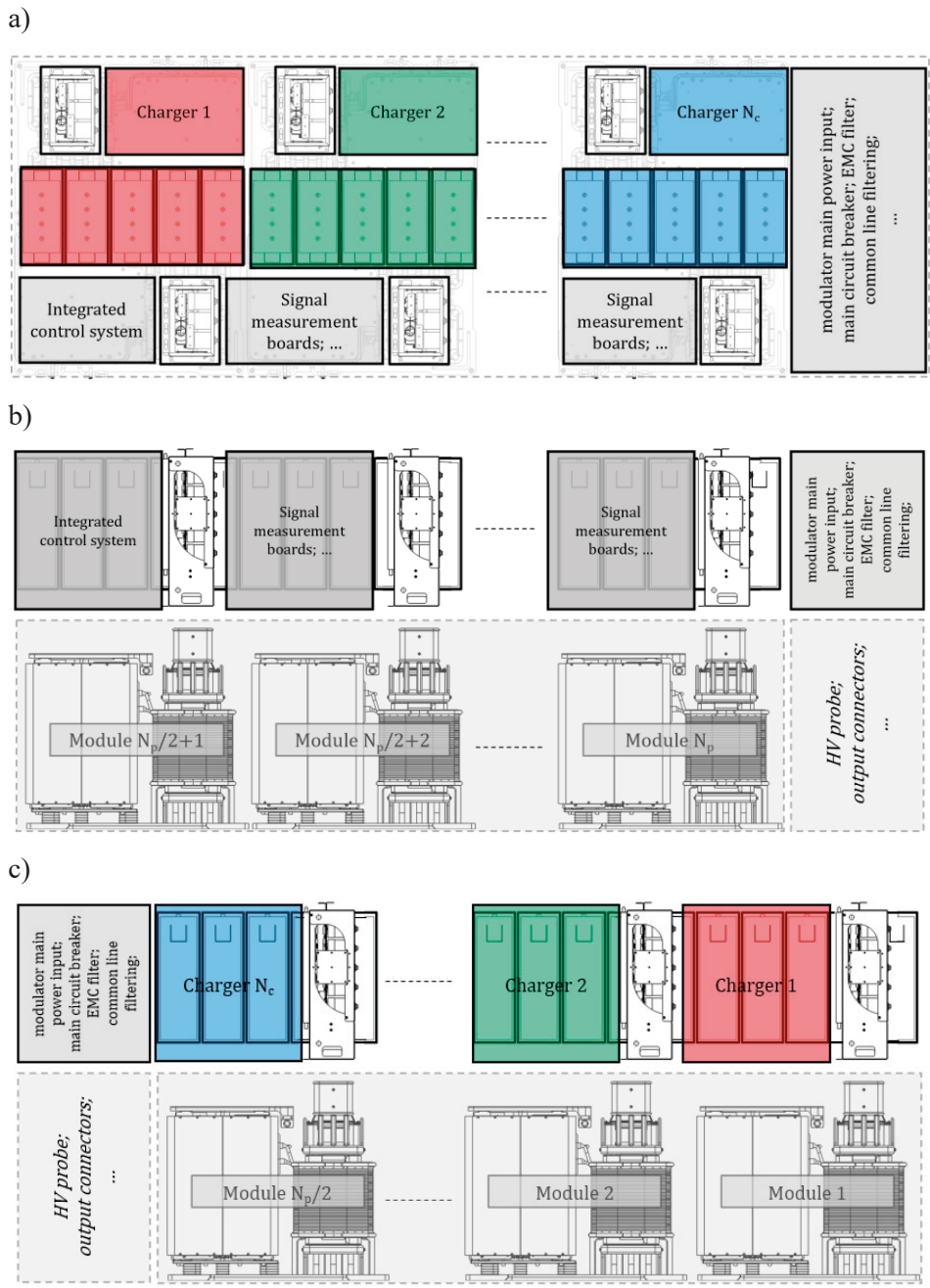



Figure 5.53: Proposed layout of complete low voltage power stage on top of high voltage assembly- a) top-down view; b) front view; c) rear view

## 5.4.2 Unified optimization procedure

Sizing models for the components comprising the input capacitor charger stage and the output pulse generator stage were discussed in sections 5.2 and 5.3, respectively. The preceding section proposed a layout to practically integrate these components in forming a complete modulator system. In this section, these ideas are combined in formulating a unified optimization procedure treating design and implementation of the complete SML modulator topology. Though it is demonstrably possible to include and integrate the entirety of the models derived in this chapter thus far in calling the optimization routine, finding an appropriate set of solutions is extremely time consuming and, occasionally, optimizer convergence becomes an issue. Instead, the iterative step-by-step optimization routine presented in Figure 5.54 is proposed and discussed in the following-

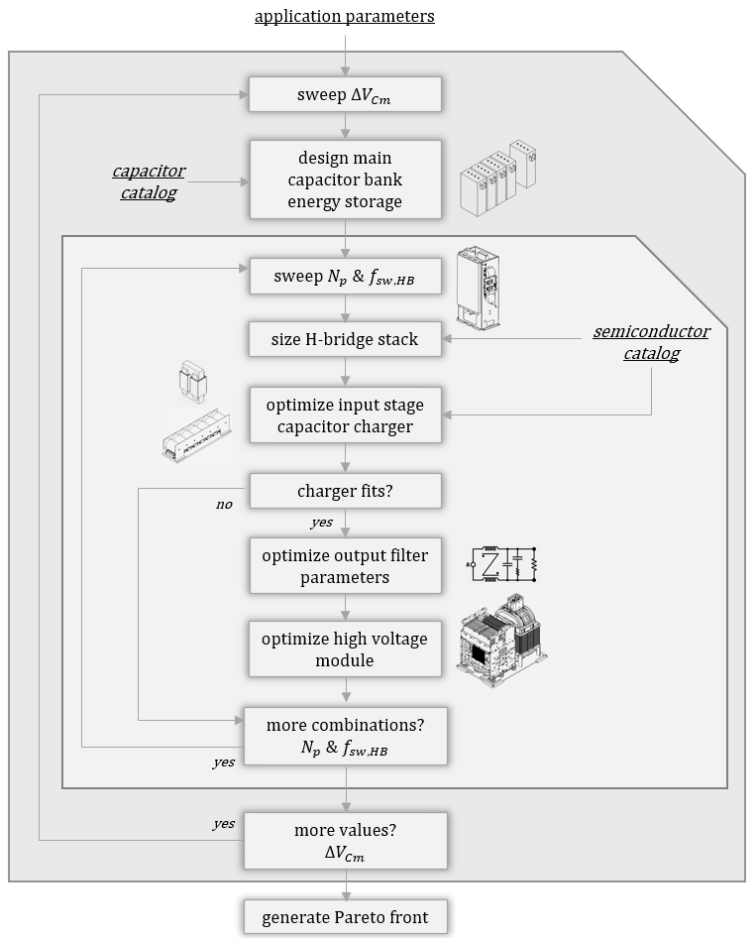



Figure 5.54: Integrated optimization procedure for complete SML modulator

First, as mentioned above and especially in relation to Figure 5.16, the capacitor bank energy storage is (given the application and the strategic pre-selection of $V_1$) defined by the capacitor bank voltage droop $\Delta V_{Cm}$. As will be seen in the subsequent sections, the allowable range of $\Delta V_{Cm}$ is typically quite limited. On the one hand, a smaller capacitor bank voltage droop results in an excessively long modulator, Figure 5.52. On the other hand, with a greater capacitor bank voltage droop it becomes difficult to 1) manage the flat top droop requirement, and to 2) fit the capacitor charger and auxiliary systems as suggested in Figure 5.53. Given the importance and the limited range of the capacitor bank energy storage, it is appropriate to sweep the capacitor bank voltage droop as a first step in design. This way, as will be seen in the following, it is possible to immediately identify and discount unfeasible modulator solutions without expensive optimizer function calls.

Following sizing of the capacitor bank energy storage, the combination of the number of pulse generator circuits, $N_p$, and the H-bridge power stack switching frequency, $f_{sw,HB}$ are swept. Of course, it is appropriate to sweep $N_p$ given that it is an integer number of very limited scope, e.g., $N_p = 4 \dots 8$ in accordance with the above. Additionally, it is desirable to sweep $f_{sw,HB}$ as it allows complete sizing of the H-bridge power stacks. This is very important, as it 1) immediately characterizes the range of feasible switching frequencies from the perspective of power cycling, and as it 2) directly sets the geometrical constraints for the capacitor charger systems, Figure 5.53 and equations (5.164)-(5.165).

$$W_{charger} \leq W_{stack} \tag{5.164}$$

$$D_{charger} \leq D_{cbk}/N_c - D_{stack} \tag{5.165}$$

Hence, as explained in the above, the capacitor charger systems may now independently be optimized through the principles developed in section 5.2. If it turns out that the comprising components cannot fit within the constraints posed by (5.164)-(5.165), the design is immediately abandoned, avoiding computationally expensive optimizer function calls, and a new combination of $N_p$ and $f_{sw,HB}$ is considered. On the other hand, if the capacitor charger design does fit, this completes the design of the low voltage part of the modulator system, Figure 5.53. Here, the volume of the low voltage stage is summarized in (5.166).

$$V_{LV} = W_{LV} D_{LV} H_{LV} = \begin{Bmatrix} W_{LV} = \sim & W_{cbk} + 2W_{stack} \\ D_{LV} = \sim & D_{cbk} \\ H_{LV} = \sim & max(H_{cbk}, H_{stack}) \end{Bmatrix} \tag{5.166}$$

Following successful design of the low voltage stage, an appropriate and compatible high voltage stage (i.e., correspondingly, high voltage module) should be developed. Section 5.3 discussed design of the high voltage module from a rather open perspective, i.e., the comprising components were characterized in terms of their design parameters but without much discussion of how the design parameters themselves could be appropriately selected in the first place. Of course, free selection of the design parameters by the solver is entirely possible as indicated in Figure 5.54. On the other hand, intelligent pre-selection of key design parameters often increases solver convergence and may significantly reduce solution time. In this work, the output filter circuit parameters are pre-defined according to the following-

First, it is repeated that the output filter is to be designed to ensure both a maximum pulse rise time and a maximum flat top ripple. At the same time, it is often good engineering practice to limit the peak-to-peak current ripple associated with the filter inductor $L_F$. Hence, for a given H-bridge converter switching frequency, a small peak-to-peak inductor current ripple is first imposed in calculating the required $L_F$. Based on this, the filter capacitors $C_1$ and $C_2 = 4C_1$ are chosen to limit the flat top ripple to be within application requirements, whereas the damping resistor is chosen to appropriately place the associated transfer function zero, (5.112). At this point, the resulting rise time is evaluated. If it is greater than the maximum rise time prescribed by the application, the peak-to-peak inductor current ripple is increased (resulting in a smaller inductor, generally decreasing the associated rise time), and the filter design procedure repeated. The procedure runs iteratively until either 1) both the flat top ripple and rise time requirements are met, at which point the filter parameters are considered optimal, or 2) the inductor current ripple is considered too great, e.g., beyond ~20%. If an appropriate filter design cannot be found, the design is abandoned. Then, typically, a greater switching frequency is necessary to solve the design problem. The above procedure significantly reduces the complexity of the optimization problem, both minimizing the number of solver functional calls as well as the number of free design parameters. The volume of a feasible high voltage stage design is then expressed as (5.167).

$$V_{HV} = W_{HV} D_{HV} H_{HV} = \begin{Bmatrix} W_{HV} = \sim & 2W_{HVM} \\ D_{HV} = \sim & (N_p/2) D_{HVM} \\ H_{HV} = \sim & H_{HVM} \end{Bmatrix} \tag{5.167}$$

Importantly, the associated volume and electrical losses and efficiency of the complete modulator system are given by (5.168), (5.170) and (5.169), respectively.

$$V_M = W_M D_M H_M = \begin{Bmatrix} W_M = \sim & max(W_{LV}, W_{HV}) \\ D_M = \sim & \max(D_{LV}, D_{HV}) \\ H_M = \sim & H_{LV} + H_{HV} \end{Bmatrix} \tag{5.168}$$

$$\begin{aligned} \bar{P}_{L,M} &= N_c\left[\bar{P}_{L2} + \bar{P}_{L1} + \bar{P}_{AFE} + \bar{P}_{DC/DC} + \bar{P}_{L,dc}\right] \\ &+N_p \begin{bmatrix} 4N_{m,HB}\bar{P}_{IGBT} + \left(\bar{P}_{t,fe} + \bar{P}_{t,cu,p} + \bar{P}_{t,cu,s}\right) \\ +\bar{P}_{HVR} + \bar{P}_s + \bar{P}_{Lf} + \bar{P}_{Lcm} \end{bmatrix} \end{aligned} \tag{5.169}$$

$$\eta_{m,e} = 1 - \frac{\bar{P}_{L,M}}{V_2 I_2 T_p f_r + \bar{P}_{L,M}} \tag{5.170}$$

Finally, a common Pareto front is generated from which an appropriate candidate solution may be selected. Here, as will be exemplified in the subsequent section, it is often practical to display the corresponding per-system (i.e., to separately consider the low voltage and high voltage systems) Pareto fronts expressed in terms of footprint and efficiency. This way, a practical high-efficiency modulator system may be selected such that the footprints of the low voltage and high voltage systems match.

## 5.5 Case study: SML modulator for ESS pLinac

In this section, the optimization routine developed in section 5.4 is applied to the case of the ESS klystron modulator requirements, Table 5.1. First, in section 5.5.1, the steps of the optimization routine are studied in detail to develop an understanding of the reasonability and scope of solutions. Then, in section 5.5.2, the integrated optimization routine is set-up for the problem summarized in Table 5.1 based on the preliminary results derived in section 5.5.1 in generating a set of possible solutions.

**Table 5.1: Required output pulse performance for European Spallation Source klystron modulator systems**

| Symbol | Quantity | Value |
|---|---|---|
| $V_2$ | Rated output voltage | 115 $kV$ |
| $I_2$ | Rated output current | 100 $A$ |
| $T_p$ | Pulse length | 3.5 $ms$ |
| $t_r$ | Rise time (0-99%) | 120 $\mu s$ |
| $T_{max}$ | Pulse repetition rate | 14 $Hz$ |

### 5.5.1 Preliminary considerations

*Step 1: Main capacitor bank energy storage*

The first step of the integrated design routine is intended to consider a range of capacitor bank voltage droop, corresponding to a set of capacitor bank designs. This design step is studied for the imposed requirements in Figure 5.55. Here, the capacitor bank droop is considered to be between 10% and 20% of the nominal primary voltage of 1 kV. Obviously, greater voltage droop is associated with smaller capacitance, (5.62), such that fewer capacitor units are needed. Hence, though the height and width of the resulting capacitor bank remain the same, the length of the modulator may be considerably reduced. It is noted that, from this, there is a minimum allowable droop derived from the maximum allowable modulator length as indicated in Figure 5.56. Here, it may be seen that – in the imposed RF gallery layout – the maximum modulator length is ~4.5 m. A longer modulator would prohibitively extend into the gallery walkway, Figure 5.56. Hence, considering the added length associated with the common modulator input stage as well as similar system overheads, the capacitor bank should be limited to be less than, e.g., ~4 m. As shown in Figure 5.55, this corresponds to a minimum droop of ~13%. As will be seen in later design steps, there are also corresponding maximum levels of droop, derived from 1) the inability to appropriately meet the flat top droop constraint (generally towards the end of the pulse event), and 2) the inability to fit the charger circuits in the remaining space provided by the low voltage cabinet.

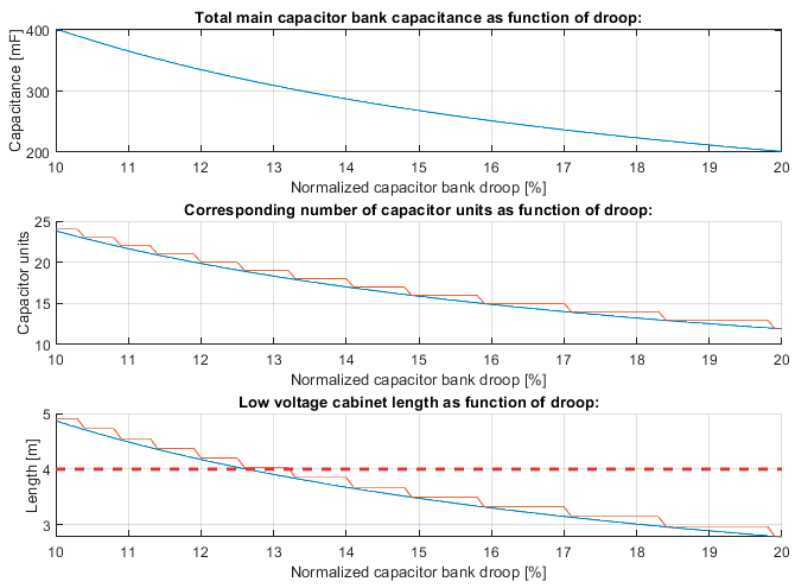



Figure 5.55: Modulator capacitor bank size as function of capacitor bank droop. The lower limit of capacitor bank voltage droop is derived from RF gallery size limitations.

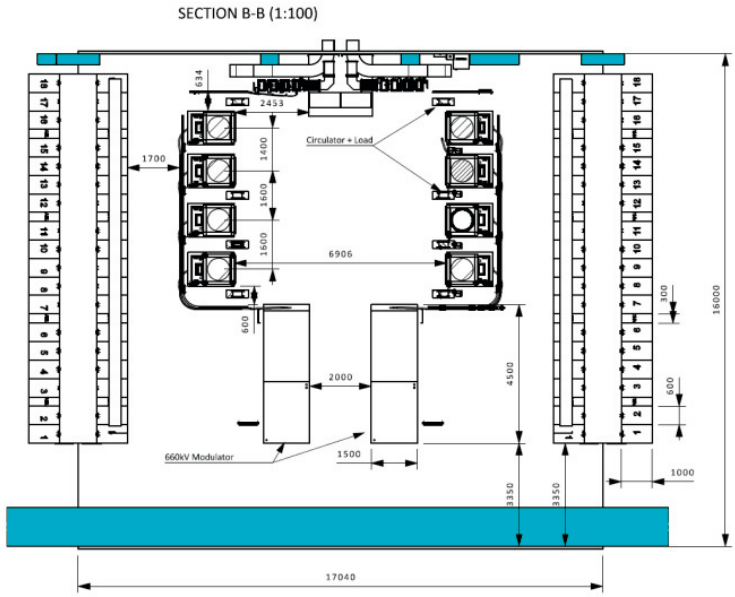



Figure 5.56: Imposed RF gallery cell layout – klystron modulator length is limited to ~4.5 m, directly constraining capacitor bank voltage droop.

*Step 2: H-bridge power stack*

For a given capacitor bank, the H-bridge power stack may be completely defined and characterized following the selection of the number of pulse generator circuits, $N_p$, and the H-bridge converter switching frequency, $f_{sw,HB}$. Some important H-bridge design results for the application requirements of Table 5.1 are shown in Figure 5.57 as function of the converter switching frequency and with the number of pulse generator circuits as parameter-

As discussed in section 5.3.3, parallel IGBT power modules are installed in handling the power cycling associated with pulsed operation to ensure converter lifetime. In this context, the number of required parallel modules are chiefly determined by two factors. First, the number of pulse generator circuits directly dictates the power handled by each converter. Hence, with fewer pulse generators, a greater portion of the load power is converted by each pulse generator, corresponding to greater absolute power losses per pulse generator system. Second, increasing the switching frequency implies additional converter losses, enhancing the power cycling effect. These effects are directly seen in Figure 5.57. As the switching frequency is increased, parallel modules are added to handle the correspondingly increasing power cycling. However, using only four pulse generators, a second parallel IGBT module is needed already at a switching frequency around 7 kHz. With six pulse generators, a second parallel module is added only at 14 kHz. Then, for eight pulse generators, addition of a second IGBT module is not necessary for switching

frequencies below that of 20 kHz. This is important, as the required number of IGBT modules greatly affects the size of the individual power stack, Figure 5.57. For example, at a switching frequency of around 18 kHz, a third parallel IGBT module is required for a system based on four pulse generators. This extends the height of the power stack to beyond that of 1.2 m, resulting in 1) the complication of heat sink design, 2) added complexity due to the need of additional driver circuits, and 3) reduced system maintainability. In this respect, considering a system with a greater number of pulse generator circuits is beneficial. On the other hand, given the greater number of circuits, the total number of IGBT modules (and thus drive circuitry) is still relatively similar. Note particularly that the full system size, (5.168), and total converter losses do not depend particularly on the number of pulse generator circuits. Hence, $N_p$ should be selected in a way that facilitates system design, enhances maintainability and limits complexity.

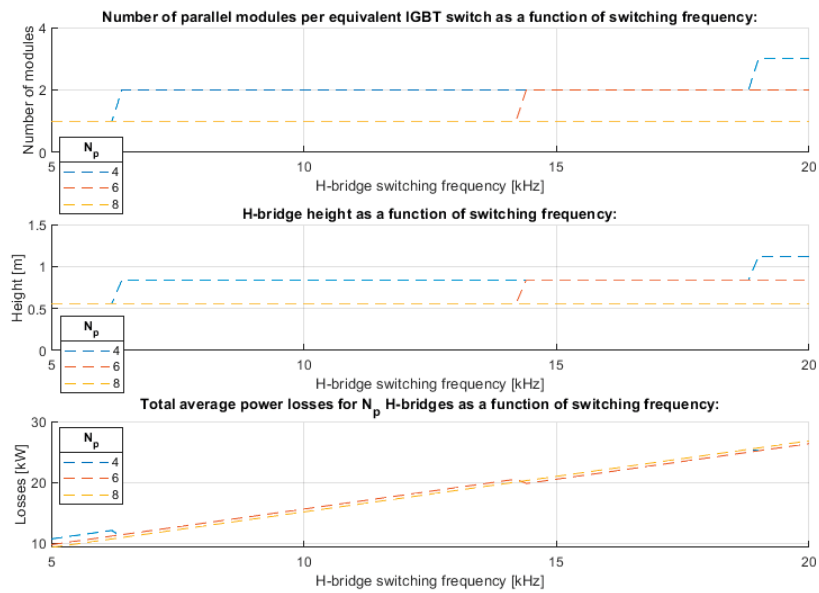



Figure 5.57: Design results of H-bridge power stack as function of switching frequency and with the number of pulse generator circuits ($N_p$) as parameter.

*Step 3: Input capacitor chargers*

Once the capacitor bank and the H-bridge power stack have been dimensioned, the space (footprint) available for the capacitor charger circuits is determined. The definitions are reviewed in Figure 5.58. From section 5.3.3, the footprint of the H-bridge power stacks may be considered to be essentially constant such that the footprint available for the capacitor charger may be studied as a direct function of capacitor bank droop, (5.164)-(5.165). This is depicted in Figure 5.59, where the

available width and depth per charger unit is shown in terms of normalized droop and with the number of charger systems as parameter. Here, $N_c = N_p/2$ is considered in accordance with the above. Whereas Figure 5.55 indicated a lower limit on capacitor bank voltage droop, Figure 5.59 implies an upper limit on capacitor bank voltage droop. This limit may be understood from Figure 5.53; in the proposed modulator layout, reducing the capacitor bank size to minimize system volume implies less space is left for the charger circuits. In addition, a larger number of charger circuits implies less space per charger. This is an important consideration, as the size per charger system does not necessarily reduce in proportion.

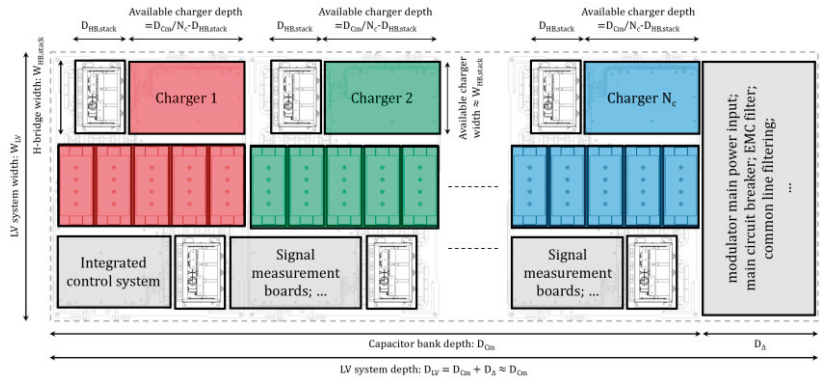



Figure 5.58: Definition of available footprint per charger unit for proposed low-voltage power stage layout.

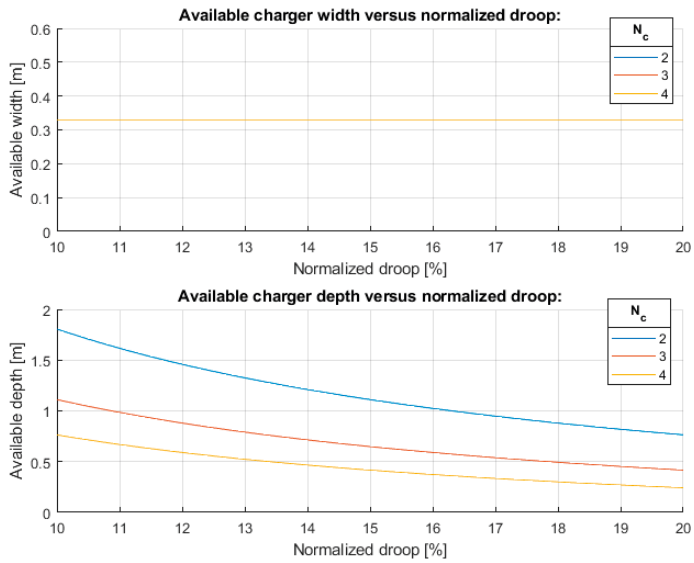



Figure 5.59: Available footprint per charger unit as function of capacitor bank voltage droop with number of charger systems ($N_c$) as parameter.

In the following, the design procedure developed in section 5.2.7 is utilized considering the added constraints of (5.164)-(5.165). In this case, an efficient system is considered a better system provided the constraints are met. Figure 5.60 shows optimization results under these conditions as function of available width and available depth and with the number of charger systems as parameter-

First, Figure 5.60.a shows the available charger width and the corresponding total width of the low voltage system. As can be seen – and as was indicated in relation to Figure 5.59 – this is represented by a single value which does not depend on the number of charger circuits. Then, Figure 5.60.b shows optimization results in terms of their required width and total charger losses. Comparison to Figure 5.60.a demonstrates that the developed solutions represent a compact fit on the width. Interestingly, the solution for $N_c = 4$ represents approximately twice the losses compared to the other solutions.

Then, Figure 5.60.c similarly shows the available charger depth and corresponding total depth of the low voltage system. Clearly, and as was indicated in relation to Figure 5.59, the available depth per charger system depends directly on the number of charger systems. Figure 5.60.d shows the same solutions described in Figure 5.60.b, but in terms of required depth. Whereas the solutions for $N_c = 2$ and $N_c = 3$ are similar in terms of efficiency and in terms of size, there is a significant amount of unused space for $N_c = 2$. For $N_c = 4$, the maximum droop is limited in ensuring sufficient space for the charger systems, resulting in a longer low voltage system. Furthermore, a higher switching frequency is required in correspondingly reducing component size, explaining the added losses. As can be seen, $N_c = 3$ results in a system with high efficiency, minimum volume and with compact fit.

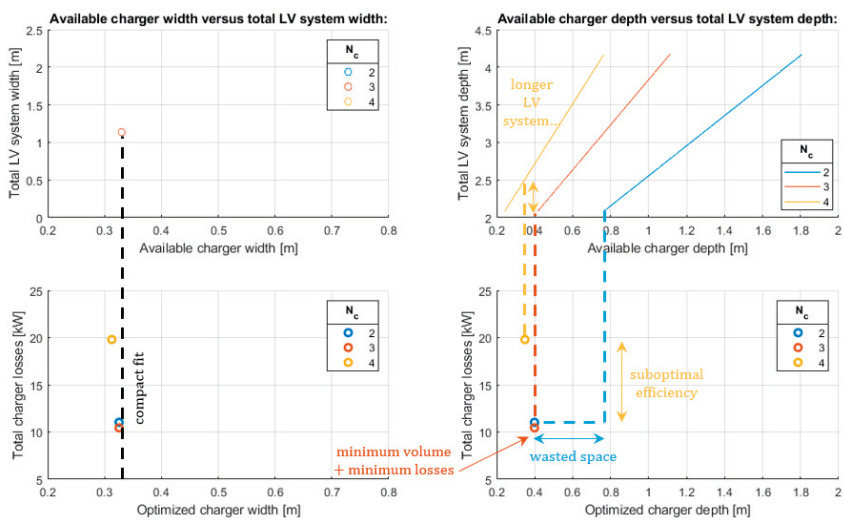



Figure 5.60: Considerations in charger design

*Step 4: Output filter*

The output filter circuit is designed in ensuring the required pulse rise time and that the flat top ripple constraint is satisfied. The procedure used in pre-selecting the filter circuit parameters was described in the above. Figure 5.61 and Figure 5.62 show important filter performance results as function of the switching frequency and the normalized inductor current peak-to-peak ripple, respectively, with the number of pulse generator circuits as parameter-

In Figure 5.61, the current peak-to-peak ripple is imposed to be 20% of the nominal current amplitude. As has been explained, the filter is designed to always meet the flat top ripple constraint. Thus, as the switching frequency is increased, the corresponding filter inductance is proportionally reduced, decreasing pulse rise time. As can be seen, to achieve a pulse rise time on the order of ~120 µs, a switching frequency of ~15 kHz is required. Importantly, considering $N_p = 4$, the filter capacitor arrangement discussed in section 5.3.6 is made up of ~100 capacitor units per output filter.

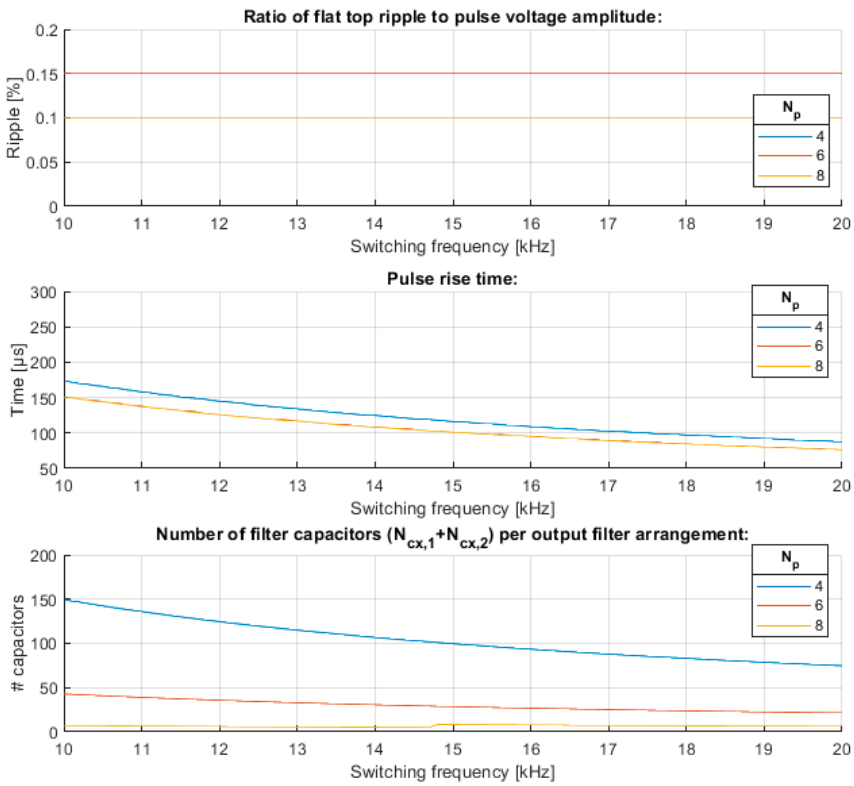



Figure 5.61: Filter design study considering a range of H-bridge switching frequencies with the number of pulse generators ($N_P$) as parameter

Then, in Figure 5.62, the switching frequency is set to be 15 kHz. Again, allowing a greater current peak-to-peak ripple corresponds to a smaller filter inductance, improving pulse rise time. Again, $N_p = 4$ is seen to require an enormous number of output filter capacitors in maintaining the required pulse flat top ripple. On the other hand, Figure 5.61 and Figure 5.62, $N_p = 8$ may be seen to correspond to over-design, resulting in lower-than-necessary flat top ripple. While this may be considered an advantage, issues of added complexity and system maintainability must also be considered.

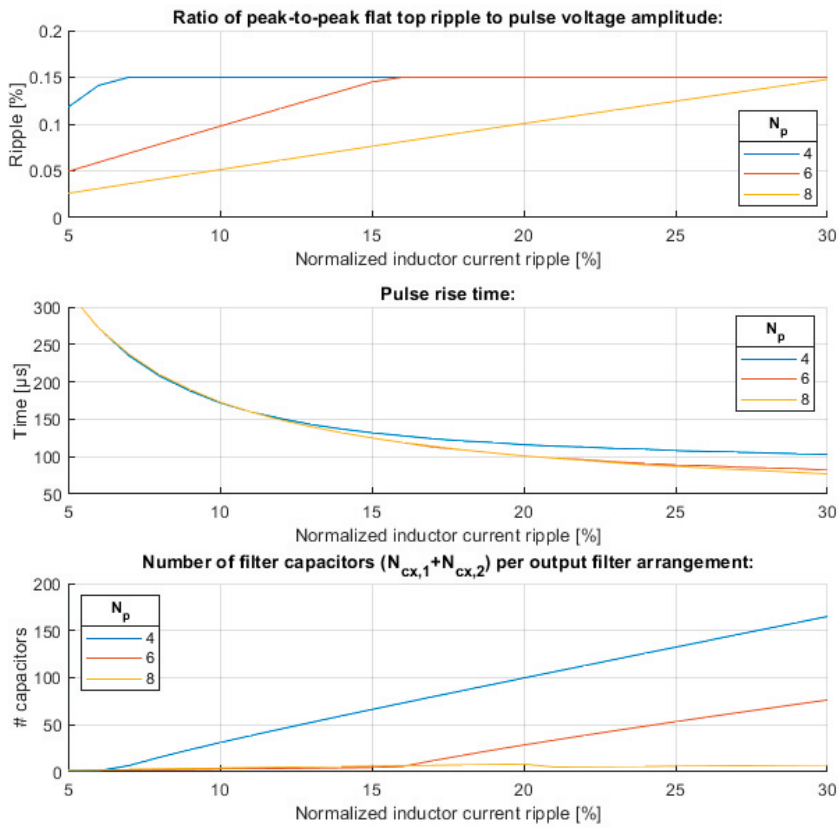



Figure 5.62: Filter design study considering the ratio between the inductor peak-to-peak current ripple and the nominal converter output current amplitude with the number of pulse generator circuits as parameter

*Preliminary conclusions*

The preceding sections have treated preliminary modulator design, in particular considering the number of pulse generator circuits $N_p$ and the number of charger circuits $N_c = N_p/2$. Though all possibilities have been shown to result in viable solutions, it has been demonstrated that $N_p = 6$ and $N_c = 3$ appear to result not only

in the appropriate minimization of system volume and system losses, but also an appropriate trade-off between performance and system complexity and maintainability. For these reasons, optimization of the complete modulator system is treated considering $N_p = 6$ and $N_c = 3$. It is pointed out that a different modulator layout, configuration or, particularly, different application could result in a distinctly different optimum.

### 5.5.2 Complete optimization results

The developed optimization procedure, Figure 5.54, is now set up and run for the application requirements of Table 5.1 and considering $N_p = 6$ and $N_c = 3$, generating the optimization results presented in Figure 5.63. As was described in the concluding part of section 5.4, the resulting footprint of the low voltage and high voltage systems, respectively, are individually plotted with respect to total system efficiency. As can be seen, the footprint of the low voltage system, defined by the length of the main capacitor bank energy storage and the width of the H-bridge converters as well as the main capacitor bank units, is constant. On the other hand, for the high voltage system, there is a rather large trade-off region, where viable solutions with footprints from as low as 3 $m^2$ up to beyond 6 $m^2$ exist. In this region, efficiency varies from approximately 90% up to 91.5%. Importantly, the calculated efficiency, (5.170), does not include power cabling, control systems (e.g., driver circuitry, control systems, etc.), oil circulation pumps, and other auxiliary equipment, and should be selected with comfortable margin with respect to the required efficiency level. In this case, a total system efficiency of at least 90% was desired. Here, a design in which the footprint of the low voltage and high voltage systems matched with an efficiency of ~90.7% was selected in 1) minimizing total system volume and in 2) providing sufficient margin to the limit efficiency. Pertinent design parameters and results of this solution are summarized in Table 5.2.

A detailed account on the development and practical implementation of each of the comprising components as well as the complete modulator system is described in chapter 9. In addition, a complete set of simulation results are presented in relation to the corresponding experimental results.

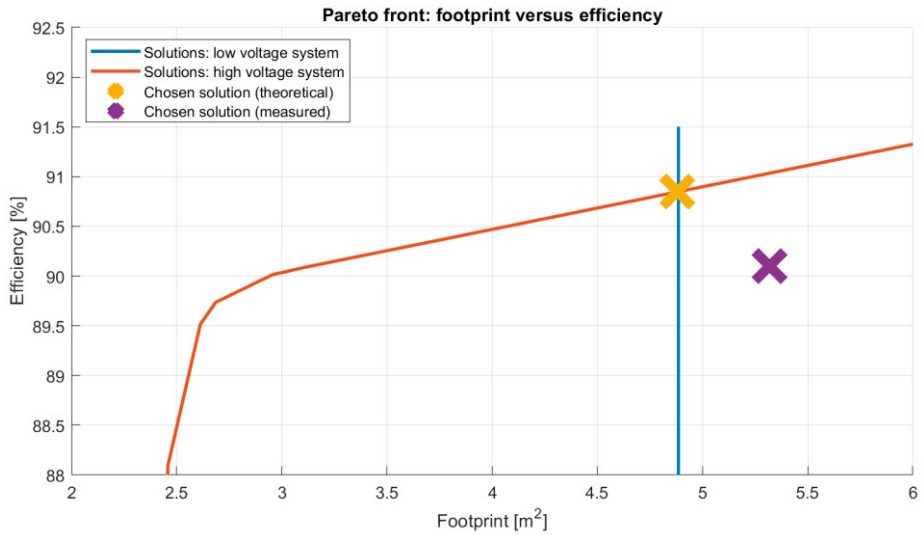



Figure 5.63: Optimization results for complete SML modulator for ESS klystron modulator application

Table 5.2: Overview of chosen SML modulator design for ESS application

| Symbol | Quantity | Value |
|---|---|---|
| | *Capacitor charger* | |
| $N_c$ | Number of parallel charger systems | 3 |
| $L_2$ | Line filter inductance | 600 µH |
| $C_1$ | Line filter capacitances | 100 µ$F$ |
| $C_2$ | | 400 µ$F$ |
| $R_F$ | Line filter damping resistors | 50 $m\Omega$ |
| $f_{sw,AFE}$ | Active rectifier switching frequency | 3.6 kHz |
| $N_{m,AFE}$ | Parallel IGBT modules per rectifier arm | 2 |
| $f_{sw,DC/DC}$ | DC/DC converter switching frequency | 5 kHz |
| $N_{m,DC/DC}$ | Parallel IGBT modules per dc/dc converter arm | 2 |
| - | Charger IGBT module reference | SKM400GB17E4 |
| $C_{dc}$ | DC-link capacitance | 1 mF |
| | *Capacitor bank* | |
| $V_1$ | Nominal capacitor bank voltage | 1 kV |
| $\Delta V_{Cm}$ | Capacitor bank voltage droop | 15% |
| $C_m$ | Capacitor bank capacitance | 300 mF |
| | *Pulse generator* | |
| $N_p$ | Number of series pulse generators | 6 |
| $L_F$ | Output filter inductance | 10 $mH$ |
| $C_1$ | Output filter capacitances | 4 $nF$ |
| $C_2$ | | 16 $nF$ |
| $R_F$ | Output filter damping resistor | 270 $\Omega$ |
| $N_p$ | H-bridge converter switching frequency | 15 kHz |
| $N_{m,HB}$ | Parallel IGBT modules per H-bridge arm | 2 |
| - | H-bridge module reference | CM1800HC-34N |

## 5.6 References

[5.1] M. Collins and C. A. Martins, “A constant power capacitor charging structure for flicker mitigation in high power long pulse klystron modulators,” in Proc. IEEE Int. Pulsed Power Conf., Brighton, U.K., Jun. 2017, pp. 1–8.

[5.2] M. Collins and C. A. Martins, “Evaluation of a novel capacitor charging structure for flicker mitigation in high-power long-pulse modulators,” IEEE Trans. Plasma Sci., vol. 47, no. 1, pp. 985–993, Jan. 2019.

[5.3] International Electrotechnical Commission. EMC Product Family Standards: Emission. Accessed: Jun. 16, 2018. [Online]. Available: http://www.iec.ch/emc/emc_prod/prod_emission.htm

[5.4] IEEE Standard for Harmonic Control in Electric Power Systems. Accessed: June 24, 2023. [Online]. Available: https://standards.ieee.org/ieee/519/10677/

[5.5] M. Liserre et al., “Design and control of an LCL-filter-based three-phase active rectifier,” IEEE Trans. Ind. Appl., vol. 41, no. 5, pp. 1281-1291, Sept. 2005.

[5.6] K.B. Park et al., “Weight Minimization of LCL Filters for High-Power Converters: Impact of PWM Method on Power Loss and Power Density,” IEEE Trans. Ind. Appl., vol. 53, no. 3, pp. 2282-2296, Jan. 2017.

[5.7] J. Mühlethaler et al., “Optimal Design of LCL Harmonic Filters for Three-Phase PFC Rectifiers,” IEEE Trans. Magn., vol. 14, no. 5, pp. 927-929, Sept. 1978.

[5.8] E. Levi et al., “Computer-aided conformal mapping of magnetic fluxes in saturated inductor motors,” IEEE Trans. Power. Elec., vol. 28, no. 7, pp. 3114-3125, Jul. 2013.

[5.9] A. Balakrishnan et al., “Air-gap reluctance and inductance calculations for magnetic circuits using a Schwarz-Christoffel transformation,” IEEE Trans. Power. Elec., vol. 12, no. 4, pp. 654-663, Jul. 1997.

[5.10] N. Mohan et al., Power Electronics: Converters, Applications, and Design, 3rd ed. Hoboken, NJ: Wiley, 2002.

[5.11] T. Chen et al., “Analysis of DC-Link Voltage Ripple in Voltage Source Inverters without Electrolytic Capacitor,” in Proc. IECON2018 - 44th Annual Conference of the IEEE Industrial Electronics Society, Washington, DC, USA, Oct. 2018, pp. 1041-1048.

[5.12] A.K. Julian et al., “Elimination of common-mode voltage in three-phase sinusoidal power converters,” IEEE Trans. Power. Elec., vol. 14, no. 5, pp. 982-989, Sept. 1999.

[5.13] B. Anirudh Acharya, “Common Mode DC Bus Filter for Active Front-End

Converter” in Proc. 2010 Joint Int. Conf. on Power Electronics, Drives and Energy Systems, New Delhi, India, Dec. 2010, pp. 1-6.

[5.14] A. Wintrich et al., “Application manual power semiconductors,”

SEMIKRON Int. GmbH, Nuremberg, Germany, Tech. Rep., 2015, pp. 126–129. [Online]. Available: https://www.semikron.com/servicesupport/application-manual.html

[5.15] D. Graovac and M. Pürschel, "IGBT Power Losses Calculation Using the Data-Sheet Parameters". Accessed: June 24, 2023. [Online]. Available: https://community.infineon.com/gfawx74859/attachments/gfawx74859/IGBT/1341/1/

[5.16] Electronicon E57 DC-Capacitors. Accessed: June 24, 2023. [Online]. Available: https://www.electronicon.com/en/products/dc-capacitors/e57

[5.17] Kyocera AVX DC Filtering Capacitors (FFLC). Accessed: June 24, 2023. [Online]. Available: https://www.kyocera-avx.com/products/film-capacitors/medium-power-film-caps/fflc/

[5.18] Vacuumschmelze Amorphous and Nanocrystalline Cores. Accessed: June 24, 2023. [Online]. Available: https://vacuumschmelze.com/products/inductive-components-and-cores/amorphous-and-nanocrystalline-cores

[5.19] P.L. Dowell, "Effects of eddy currents in transformer windings", Proceedings of the IEE, vol. 113, no. 8, pp. 1387-1394, Aug. 1966.

[5.20] J.D. Pollock and C. R. Sullivan, “Gapped-inductor foil windings with low AC and DC resistance” in Proc. of 2004 IEEE Industry Applicatios Conference, Seattle, WA, USA, Oct. 2004, pp. 552-557.

[5.21] J.D. Pollock et al., “Modelling Foil Winding Configurations with Low AC and DC Resistance” in Proc. of 2005 IEEE 36th Power Electronics Specialist Conference, Dresden, Germany, Jun. 2005, pp. 1507-1512.

[5.22] W.G. Hurley et al., “Optimizing the AC resistance of multilayer transformer windings with arbitrary current waveforms” IEEE Trans. Power Elec., vol. 15, no. 2, pp. 369-376, Mar. 2000.

[5.23] M. Collins and C. A. Martins, “A modular and compact long pulse modulator based on the SML topology for the ESS Linac” IEEE Trans. Dielectr. Electr. Insul., vol. 24, no. 4, pp. 2259-2267, Sept. 2017.

# 6. Comparison of modulator topologies

Chapter 2 presented a comprehensive literature review of state-of-the-art pulse power modulator technology. Considering long-pulse high-power applications, topological issues related to modularity – basing the modulator on either very large monolithic components or a large number of small components – were identified and associated with complications with respect to system maintainability and system size. Chapter 3 introduced the SML modulator as a compact, high-efficiency alternative based on industrial grade off-the-shelf power semiconductors, tailored to the problems of long-pulse high-power applications. Chapter 4 and 5 have developed detailed mathematical models of the main power components of the pulse transformer-based modulator topology and the SML modulator topology, respectively. Additionally, unified design optimization procedures for complete, integrated modulator systems were proposed. Application of the developed design procedures to ESS modulator application requirements demonstrated the significant benefits of the proposed SML modulator topology with respect to system manufacturability and maintainability as well as to system efficiency and power density. Furthermore, the added flexibility in modulator design and control (studied in detail in chapter 7) is emphasized. Keeping the derived benefits in mind, it is now of interest to conduct a more general comparison of the modulator topologies in view of generic long-pulse high-power applications. In this study, the modulator output voltage and output current are assumed to be 115 kV and 100 A, respectively, in accordance with typical high-power requirements. Using the developed design optimization frameworks for the pulse transformer-based modulator and the SML modulator topologies, respectively, a parametric study of application pulse length and pulse repetition rate is carried out in comparing the topologies.

## 6.1 Parametric study: pulse transformer-based modulator

In this section, the developed design optimization framework for the pulse transformer-based modulator topology described in section 4.6 is set up for the described parametric study. Accordingly, in this section, the modulator is assumed to be based on the utilization of the electronic bouncer circuit and the active pulse

transformer auxiliary circuit. First, the particularities of each main power component of the pulse transformer-based modulator topology are discussed separately as part of a preliminary study. Then, the obtained modulator optimization results for the complete parametric study are treated. These results are compared directly to the corresponding results of the SML modulator topology in section 6.3.

### 6.1.1 Preliminary study

*Main capacitor charger*

The main capacitor charger of the modulator system is sized according to section 4.6.1 and Figure 4.85. Thus, utilizing standard 800x800x2000 electrical cabinets to house the capacitor charger units and assuming the correspondingly developed power density of ~150 kW/cabinet, these considerations may immediately be used to study, e.g., required capacitor charger footprint as function of application pulse length and pulse repetition rate. Here, capacitor charger is limited to 1 MW in accordance with the currently available offering, [6.1]-[6.3]. From this, neglecting the requirements of other modulator components and sweeping the pulse length from 1-10 ms and the pulse repetition rate from 1-50 Hz, the capacitor charger footprint shown in Figure 6.1 is obtained. Importantly, as capacitor charger power is increased by adding more charger modules in parallel, capacitor charger footprint grows linearly with both pulse length and pulse repetition rate.

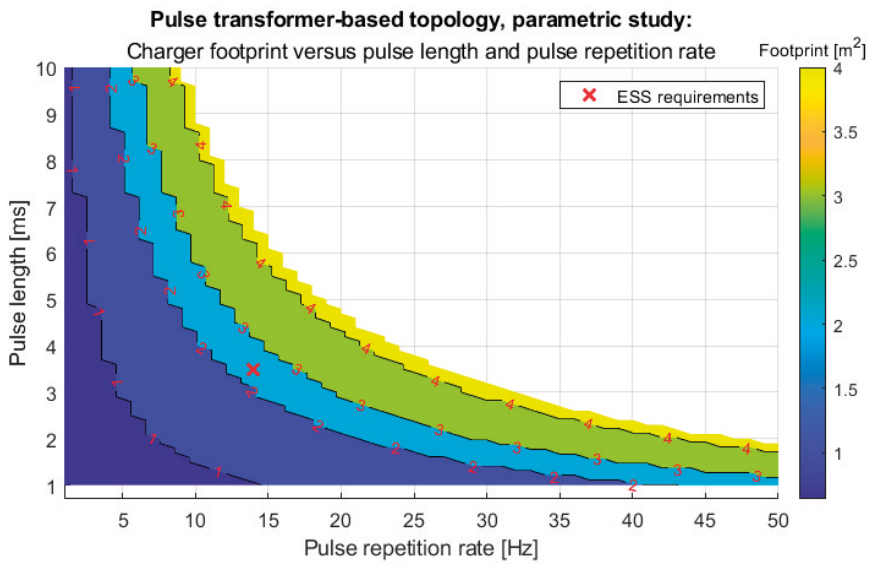



Figure 6.1: Pulse transformer-based topology: capacitor charger footprint as function of application pulse length and pulse repetition rate (power limited to 1 MW in accordance with available offering)

It is illustrative to, using ESS application requirements as a starting point, consider the consequences of doubling the pulse length or the pulse repetition rate. This step requires the addition of 4 charger cabinets, correspondingly increasing the footprint from ~2.5 $m^2$ to ~5 $m^2$. Placing the charger cabinets in a single row corresponds to a charger length of 6.25 m. Alternatively, placing the cabinets in two rows of four cabinets corresponds to a charger width of 1.6 m and a charger length of 3.2 m. Considering the addition of the remaining main power cabinets as well as the high-voltage oil tank assembly, it is clear that this arrangement is most likely unfeasible.

*Capacitor bank energy storage*

The main capacitor bank is based on medium-voltage capacitors and is integrated in cabinets according to the principle outlined in section 4.6.2. The required capacitance is expressed as function of application pulse power requirements as well as capacitor bank droop in (4.97). Unsurprisingly, the pulse repetition rate does not impact the selection of the capacitance value. Furthermore, parallel connecting a large number of high-power capacitors, the added RMS current may comfortably be neglected in selecting an appropriate capacitor. The capacitor bank cabinet footprint obtained using the procedure of Figure 4.86 under the described conditions is shown in Figure 6.2 with normalized capacitor bank droop as parameter. Here, the selection of a higher primary-side voltage (~5 kV) allows high-energy capacitor units, thereby resulting in a relatively compact capacitor bank volume provided reasonable selection of the capacitor bank droop.

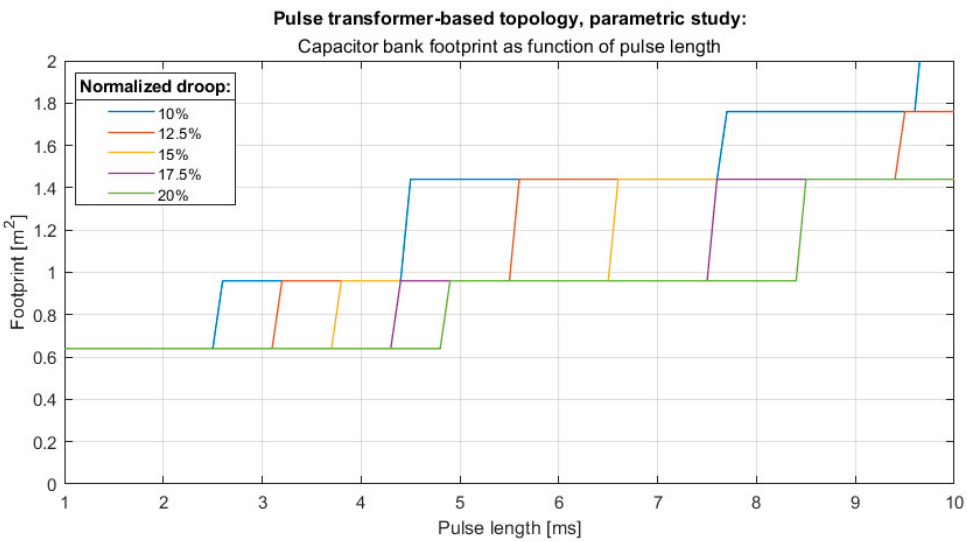



Figure 6.2: Pulse transformer-based topology: capacitor bank cabinet footprint versus pulse length with normalized droop as parameter

*Electronic bouncer circuit*

As described in section 4.6, electronic bouncer circuit size is chiefly determined by 1) the capacitor charger (also a high-power charger in this class of applications), 2) the bouncer input capacitor, and 3) the bouncer multi-phase dc/dc converter (largely defined by peak power requirements). In this study, the electronic bouncer circuit is assumed to be housed in a single 1200x800 cabinet in accordance with that discussed in section 4.6. It is noted that, clearly, exceptions to this assumption may be found in low-power and very high-power applications. Though neglected in the present work, these considerations may straightforwardly be added as needed.

*Remaining primary-side components*

As explained in section 4.4, the solid-state switch assembly is largely defined by application pulse power requirements and the chosen primary-side voltage. While increasing the pulse length or the pulse repetition rate increases average component loss, the adopted high-power IGCT units – especially considering forced cooling – easily handle the associated thermal stress. Here, the worst-case scenario might involve selection of a larger IGCT model, still barely affecting total switch volume. Similarly, the active auxiliary circuit described in section 4.5 is comparatively small, and does not impact cabinet sizing. Hence, it is believed that the cabinet layout proposed in section 4.6 is suitable in view of this scope of application requirements.

*Pulse transformer assembly*

The influence of application pulse length and pulse repetition rate (i.e., by way of increased RMS current) on pulse transformer size was studied in detail in section 4.2. There, in particular, magnetic core volume was minimized in developing an optimal transformer design. Given the results presented in chapter 4, this is still highly relevant. Translating the results to that expressing high-voltage oil tank footprint and height, (6.1), yields the results presented in Figure 6.3. Expectedly, the allowable pulse transformer height is utilized in minimizing transformer volume. Extending pulse length thus has proportional impact on oil tank footprint. Again, it is pointed out that the maximum attainable pulse length and pulse repetition rate are directly related, presenting a fundamental limit to the pulse transformer-based modulator topology.

$$V_{HV} = W_{HV} H_{HV} D_{HV} = \begin{Bmatrix} W_{HV}: & \left(2x_c + 2d_{i,b} + 2_{i,a} + d_e + d_{u,t} + d_{l,t}\right) \\ H_{HV}: & \sim\left(2x_c + 2d_i + h_w + d_y\right) \\ L_{HV}: & \sim\left(y_c + 2d_{i,b} + 2d_{u,t}\right) \end{Bmatrix} \tag{6.1}$$

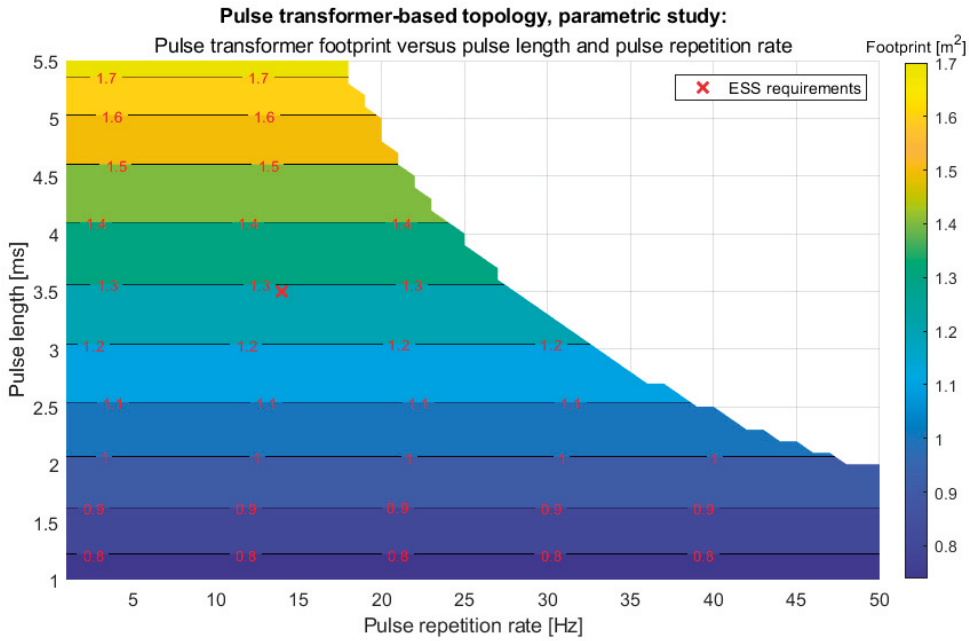



Figure 6.3: Optimization results (pulse transformer)

*Summary: power component scaling*

In concluding this preliminary study, the developed scaling relationships are summarized in Table 6.1. First, as was also seen throughout chapter 4, the main capacitor charger, the main capacitor bank, and the pulse transformer assembly largely define modulator footprint and efficiency. The electronic bouncer, the main switch and the auxiliary circuit, though obviously functionally very important, can largely be neglecting in estimating system size. Importantly, the capacitor charger, the main capacitor bank and the pulse transformer scale (at least) directly with application pulse length. As earlier indicated and here emphasized, this must be carefully examined in considering further scaling of the pulse transformer-based modulator topology given the literature review presented in chapter 2 and the results presented in, e.g., chapter 4.

Table 6.1: Scaling pulse transformer-based modulator main component size to application pulse length and pulse repetition rate in view of long-pulse high-power applications

| Component | Pulse length | Pulse repetition rate |
|---|---|---|
| Capacitor charger | Proportional | Proportional |
| Capacitor bank | Proportional | Virtually unaffected |
| Electronic bouncer | Weakly affected | Weakly affected |
| Main switch | Virtually unaffected | Virtually unaffected |
| Auxiliary circuit | Virtually unaffected | Virtually unaffected |
| Pulse transformer | At least proportional | Proportional |

## 6.1.2 Optimization results

Evaluating the complete optimization framework presented in section 4.6 for the above-described conditions yields the results shown in Figure 6.4. Here, modulator footprint, absolute volume, and weighted volume are studied. In this case, considering weighted volume, the volume of the high-voltage oil tank assembly is set to be valued five times more than that of the low-voltage systems. Clearly, with the height of the primary-side cabinets fixed at ~2m and the high-voltage oil tank assembly similarly representing a fixed height, section 4.6, the three quantities are directly related. Comparing the results to that of Figure 6.1 and Figure 6.3 it is clear that – in accordance with Table 6.1 – the capacitor charger and the pulse transformer oil tank assembly have significant impact on the size of the integrated modulator system. Just as was tentatively indicated in section 6.1.1, considering the ESS application requirements and doubling the pulse repetition rate to ~28 Hz would require a total modulator footprint of ~10 $m^2$ and a modulator length of more than 5 m.

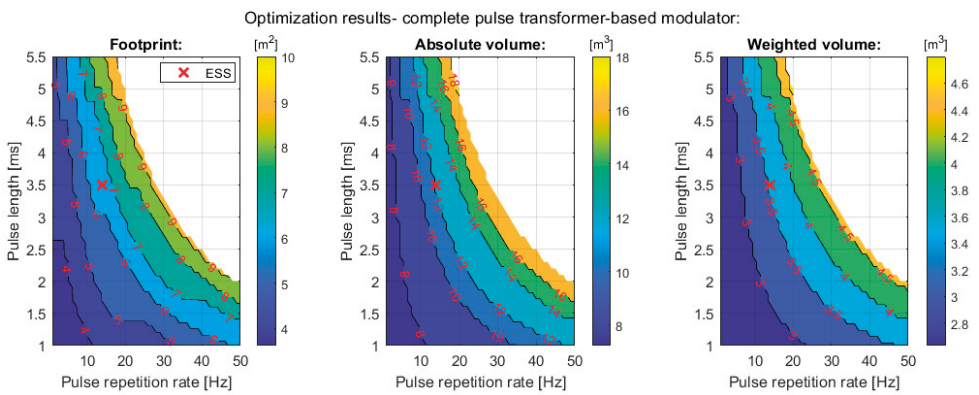



Figure 6.4: Parametric study – footprint, absolute volume and weighted volume of complete pulse transformer-based modulator as function of application pulse length and pulse repetition rate

## 6.2 Parametric study: SML modulator

In this section, the developed design optimization framework for the stacked multi-level modulator topology described in section 5.4.2 is set up for the described parametric study. Here, the case of three parallel input charger capacitors and six series output pulse generators is considered. Additionally, in keeping with the results summarized in Table 5.2, the front-end power stacks are assumed to be based on the SKM400GB17E4 IGBT module, [6.4], whereas the pulse generator H-bridge power stacks are assumed to be based on the CM1800HC-34N IGBT module, [6.5]. First, the particularities of each main power component of the topology are discussed separately as part of a preliminary study. Then, the obtained modulator optimization results for the complete parametric study are treated. These results are compared directly to the corresponding results of the pulse transformer-based modulator topology in section 6.3.

### 6.2.1 Preliminary study

*Line filter*

In this work, the input line filter of the SML modulator topology is based on the classical LCL filter with shunt RC damper. As application pulse length or pulse repetition rate increases, modulator input average power and, for a given grid voltage, the input line current increase proportionally. In section 5.2.3, it was proposed that the converter-side inductance $L_2$ should be set in limiting the peak-to-peak current limit in relation to the line current peak value. Thus, the maximum stored inductor energy, generally linked to inductor size and loss, may be expected to increases in proportion to both pulse length and pulse repetition rate. This is demonstrated in Figure 6.5, showing the converter-side inductor size and losses as given by the model developed in section 5.2.3, varying pulse length and pulse repetition rate between 1-10 ms and 1-50 Hz, respectively.

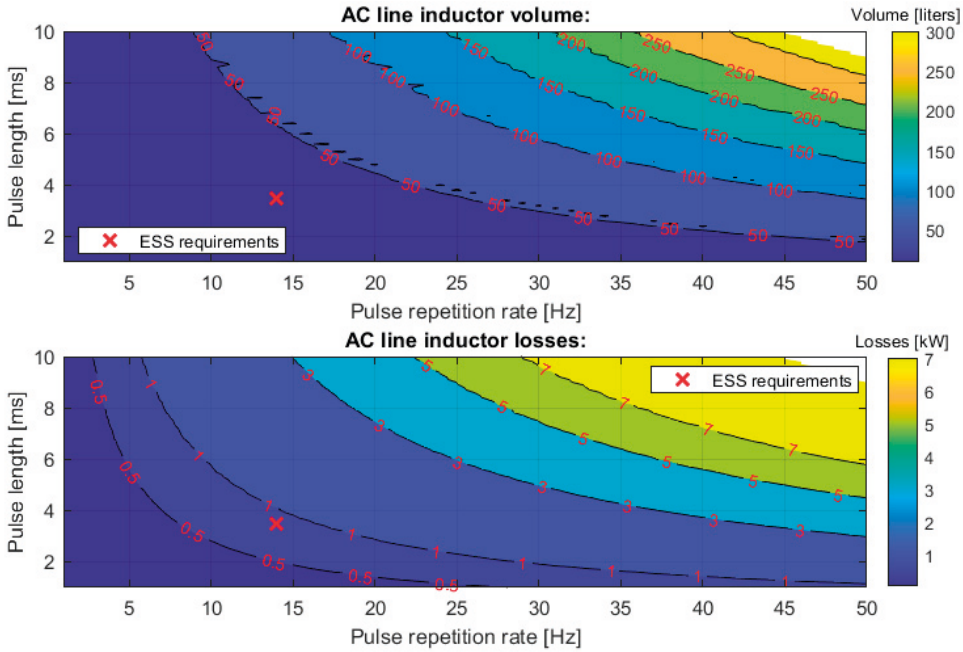



Figure 6.5: Converter-side inductor volume and loss as function of application pulse length and pulse repetition rate

In section 5.2.3, it was also explained that the grid-side inductance $L_1$ and the filter capacitors should be set in proportion to $L_2$ in limiting the maximum line current THD. On the other hand, these components are relatively small and, in many cases, size may be maintained through appropriate component selection. For these reasons, this part of the filter is not further considered in this part of the study.

*Front-end power stack*

The front-end power stack comprises the IGBT modules of both the active rectifier circuit and the dc/dc converter circuit integrated on a common heatsink, as well as the dc-link capacitors. In the front-end power stack layout proposed in section 5.2.5, it is clear that power stack width is essentially defined by the width of the IGBT module whereas power stack depth is defined by the length of the dc-link capacitors as well as, though to a lesser extent, the height of the IGBT modules and the heatsink. In the given scope of application requirements, these parameters are largely invariable. Hence, in the application range under consideration, it is to a great extent the number of parallel IGBT modules required to handle the average power requirements that define power stack design. Here, it is typically desirable to limit the number of parallel IGBT modules per equivalent IGBT to be less than or equal to three in limiting system complexity. This situation is studied in Figure 6.6, depicting the number of parallel IGBT modules per equivalent IGBT for both converters as function of pulse length and pulse repetition rate, and in Figure 6.7,

showing the associated front-end power stack height as function of pulse length with pulse repetition rate as parameter. Here, the ESS application requirements are seen to correspond to two parallel IGBT modules per equivalent IGBT for both converters, representing a manageable front-end power stack height of ~0.55 m. However, as may be seen, there are certain limitations to increasing system average power. These limitations are due to 1) limitations of the heatsink due to increased losses and 2) front-end power stack height. This will be addressed further in connection to design of the H-bridge power stacks. There, it will be argued that it is of interest to increase the number of output pulse generation modules in considering very high-power problems. In that case, the number of input stage chargers would be increased accordingly. This possibility has not been considered in detail as part of this work.

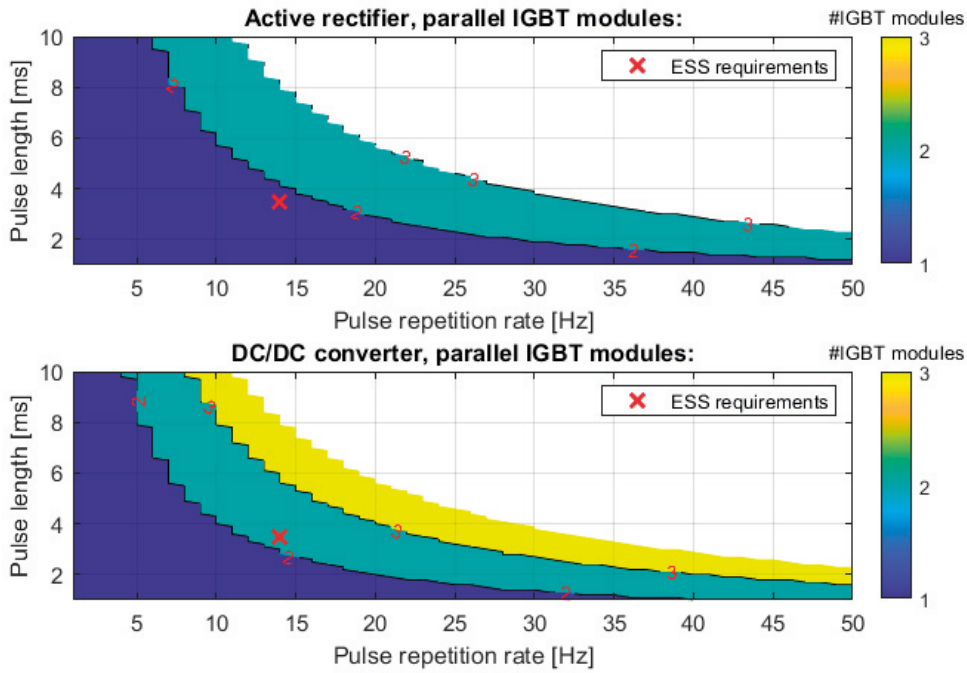



Figure 6.6: Number of required parallel IGBT modules per equivalent IGBT for the active rectifier and dc/dc converters of the input capacitor chargers as function of application pulse length and pulse repetition rate

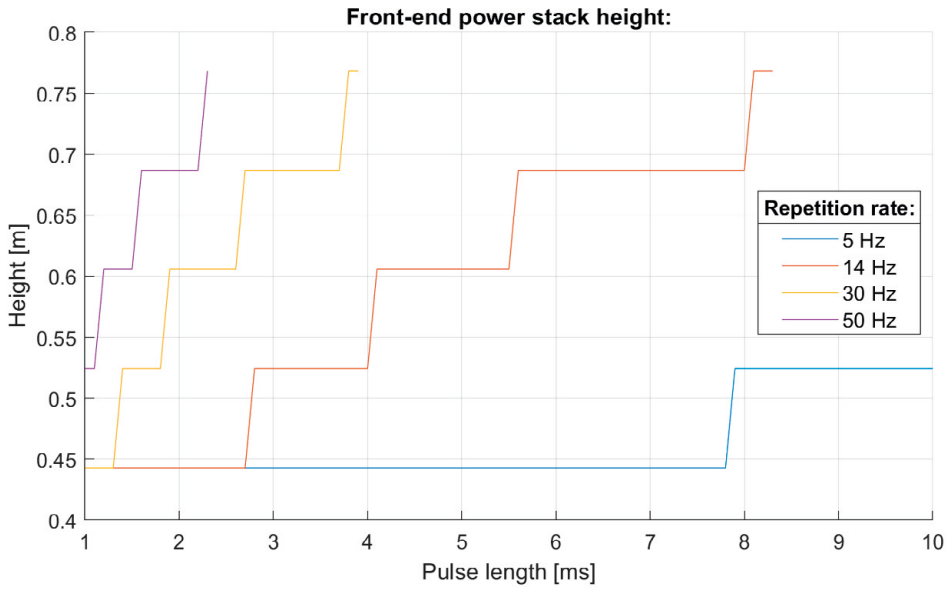



Figure 6.7: Front-end power stack height as function of pulse length with pulse repetition rate as parameter

*DC-side inductor*

As discussed in section 5.2.6, the DC-side inductance $L_{dc}$ should, similar to the converter-side inductor, be set to limit the peak-to-peak current ripple with respect to the peak charging current. Accordingly, then, as average power increases, $L_{dc}$ may be decreased proportionally. Therefore, the maximum stored inductor energy – again linked to inductor size and losses – may therefore be expected to increase linearly with application pulse length and pulse repetition rate. This is demonstrated in Figure 6.8, depicting DC-side inductor size and losses as function of application pulse length and pulse repetition rate. This relationship is very important because the size available for the DC-side inductor in the proposed modulator layout is strongly dependent on 1) the main capacitor bank, 2) the H-bridge power stacks, and 3) the front-end power stacks. As an example, if the average modulator power is increased while the above components remain fixed (e.g., as is typically the case if the pulse repetition rate is increased), the resulting DC-side inductor will at some point be too large to fit the allotted space. There are different ways of addressing this situation, one of which is to consider use of a different modulator layout. These considerations are not treated in this work.

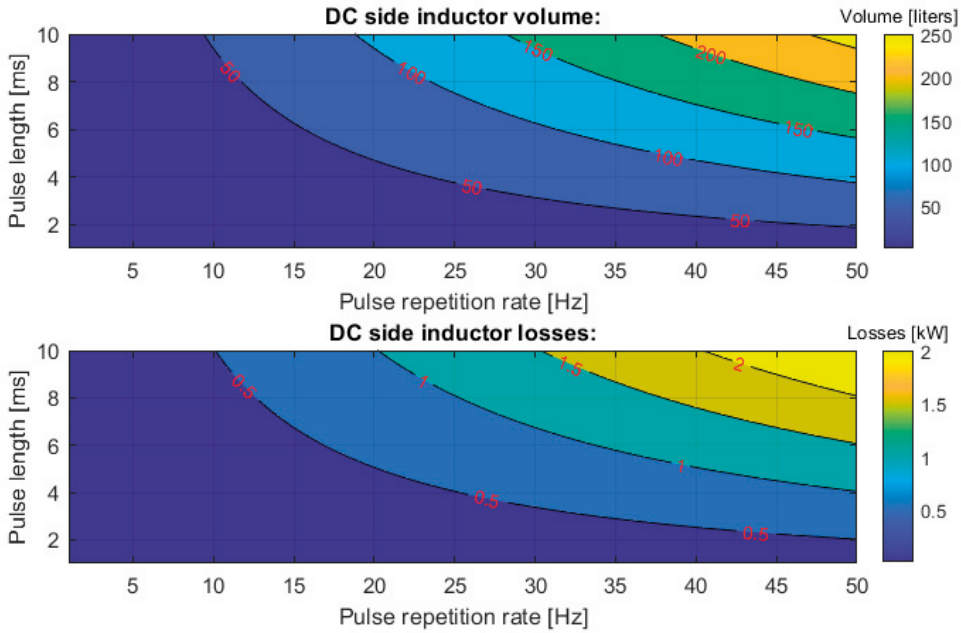



Figure 6.8: DC-side inductor size and losses as function of application pulse length and pulse repetition rate

*Main capacitor bank*

As explained in section 6.1.1, sizing of the main capacitor bank is done almost entirely with respect to peak power requirements and the pulse length in maintaining a given droop. As a large number of high-power capacitors are parallel connected in obtaining the required capacitance, the added RMS current seen in increasing pulse repetition rate may be neglected in selecting a suitable capacitor arrangement. In Figure 6.9, given the specific arrangement of the SML modulator capacitor bank shown in Figure 5.52, the resulting modulator length is studied as function of application pulse length and normalized capacitor bank droop. Here, the minimum capacitor bank droop justified with respect to Figure 5.55 and Figure 5.56 may again be seen. Additionally, as exemplified by the case study presented in section 5.5 (considering a maximum modulator length of ~4 m), it may be seen that a capacitor bank droop of ~15% limits the attainable pulse length to around 4 ms.

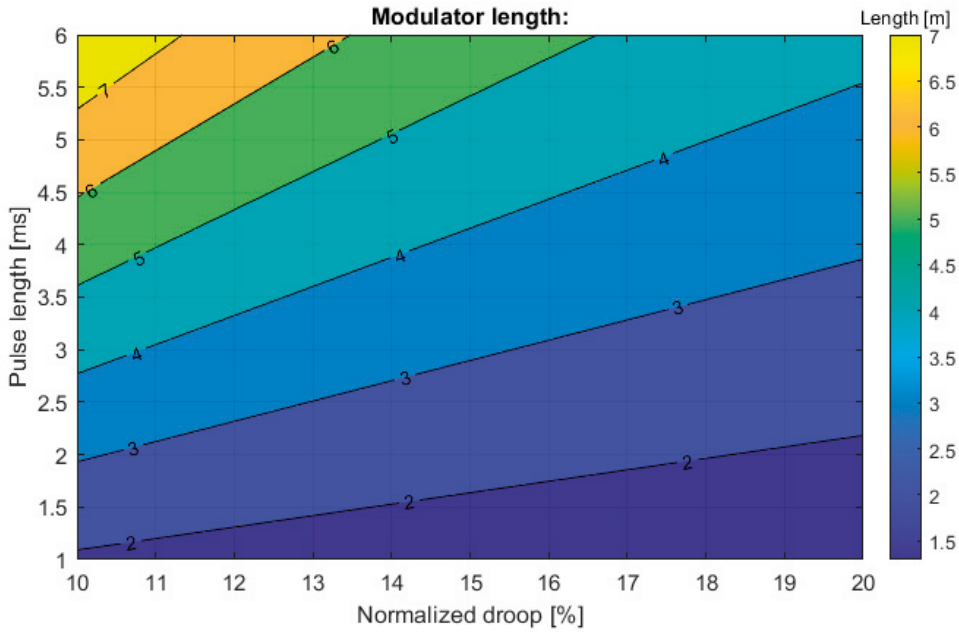



Figure 6.9: Estimated modulator length as function of application pulse length and normalized capacitor bank droop

*H-bridge power stack*

The IGBT modules comprising the H-bridge power stacks are selected considering peak power requirements in managing converter lifetime. However, appropriate selection of the IGBT module as well as the number of parallel IGBT modules per equivalent IGBT typically significantly limits the swing of the IGBT junction temperature. Therefore – similar to the case of the front-end power stacks discussed earlier – increasing application pulse length or pulse repetition rate more importantly increases average power losses that must be handled by the power stack heatsink. This is shown in Figure 6.10, where it may be seen that for six pulse generator circuits operated at an assumed switching frequency of 15 kHz, use of one or two IGBT modules per equivalent IGBT is sufficient in handling the power requirements of most applications under study. However, for combinations of large pulse length and pulse repetition rate, attempts to add additional modules in handling the maximum junction temperature barely works given the great heatsink temperature. This is a fundamental power limitation that is best handled by, as aforementioned, selecting a greater number of pulse generator circuits. This way, the increased losses corresponding to the greater average power is split among a greater number of modules, alleviating the heatsinks. It is further pointed out that a greater number of pulse generators would allow a decrease in converter switching frequency while maintaining pulse flat top ripple, further reducing thermal stress while increasing efficiency. This possibility is not further considered in this work.

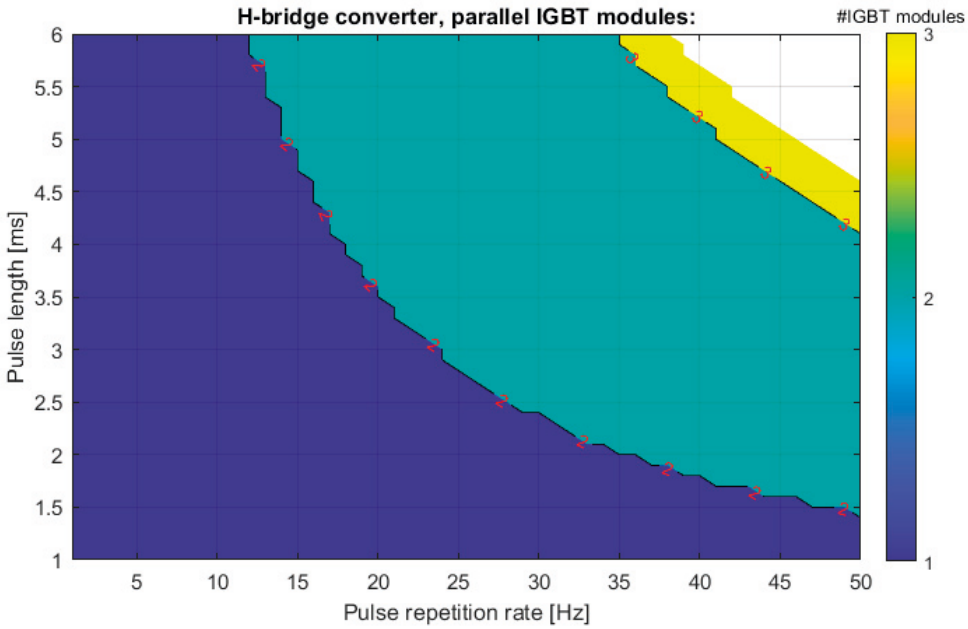



Figure 6.10: Number of required parallel IGBT modules per equivalent IGBT for H-bridge power stacks as function of application pulse length and pulse repetition rate assuming six pulse generators and a switching freqeuncy of 15 kHz.

*High-voltage components*

As demonstrated throughout section 5.3, the high-voltage components comprising the SML modulator output stage are designed respecting peak power requirements and high-voltage isolation requirements. While compact, the high-voltage components are comparatively speaking quite large with respect to the average power they convert. Furthermore, all loss sources (e.g., windings, magnetic cores, rectifier diodes, …) are immediately exposed to the surrounding oil. Here, given the distance required in maintaining isolation forms an effective cooling channel, especially as the oil is circulated. While increasing the application pulse length and pulse repetition rate does increase absolute losses, it is believed that the components themselves may easily handle the increased thermal load. Still, in significantly increasing modulator average power, it must be verified that, e.g., the resulting oil temperature is manageable. These aspects are not considered as part of this work in accordance with the above.

*Scaling laws*

In concluding this preliminary study, the developed scaling relationships are summarized in Table 6.2 and Table 6.3. As may be seen, the size of the majority of components are largely unaffected (though the corresponding aggregated losses

must clearly be managed in considering high-power applications) as application pulse length and pulse repetition rate increase. Importantly, the size of the main capacitor bank increases linearly with pulse length. The volume and losses associated with the converter-side and DC-side inductors increase in proportion to both application pulse length and pulse repetition rate. Finally, the size of the modulator power stacks remains virtually unaffected (though the height may increase somewhat) by increasing application pulse length and pulse repetition rate, except in considering very high-power applications where the dissipated losses managed by individual heatsinks become excessive. It is here proposed that these application requirements are to be handled by increasing the number of charger modules and pulse generator modules, respectively, in alleviating the heatsink thermal load.

**Table 6.2: Scaling SML modulator capacitor charger component size to pulse length and pulse repetition rate in view of long-pulse high-power applications**

| Component | Pulse length | Pulse repetition rate |
|---|---|---|
| Line filter arrangement | Weakly affected | Weakly affected |
| Converter-side inductor | Proportional | Proportional |
| Front-end power stack | Weakly affected | Weakly affected |
| DC-side inductor | Proportional | Proportional |

**Table 6.3: Scaling SML modulator pulse generator component size to pulse length and pulse repetition rate in view of long-pulse high-power applications**

| Component | Pulse length | Pulse repetition rate |
|---|---|---|
| Main capacitor bank | Proportional[1] | Virtually unaffected |
| H-bridge power stack | Weakly affected | Weakly affected |
| HVHF transformer | Virtually unaffected | Virtually unaffected |
| CM inductor | Virtually unaffected | Virtually unaffected |
| HV rectifier | Virtually unaffected | Virtually unaffected |
| HV inductor | Virtually unaffected | Virtually unaffected |
| Output filter | Virtually unaffected | Virtually unaffected |

[1] The size of the capacitor bank increases with pulse length in accordance with (5.62). However, as will be demonstrated in section 6.2.2, this increase may often be counteracted with little penalty by correspondingly increasing the capacitor bank droop.

### 6.2.2 Optimization results

Evaluating the complete optimization framework presented in section 5.4 for the above-described conditions yields the results shown in Figure 6.11. Here, in accordance with Table 6.2, the high-voltage stage of the SML modulator is essentially unaffected by increasing pulse length or pulse repetition rate. Similarly, the footprint of the H-bridge power stack is largely unaffected. As, in accordance with the modulator layout proposed in Figure 5.51, the power stack is placed just above the high-voltage module, this yields a relatively rigid layout of the modulator. Therefore, if the application pulse length is reduced the size of the main capacitor bank and the DC-side inductors is reduced proportionally, but the effective modulator footprint remains fixed. Conversely, if the application pulse length is increased, the capacitor bank size would normally increase proportionally. However, if possible, the optimization framework counteracts this increase by proportionally increasing the capacitor bank droop in keeping capacitor bank size constant, (5.165). Consequently, modulator footprint is retained at ~4.6 $m^2$ irrespective of application pulse length and pulse repetition rate. As proposed in chapter 3 and as will be seen in the following section, this property is very beneficial in considering applications of greater pulse lengths and pulse repetition rates, representing an efficient modulator design of extremely high-power density. On the other hand, for applications of shorter pulse length and pulse repetition rate, the identical peak power requirements (setting the design requirements for the high-voltage assembly) results in a greatly oversized modulator design.

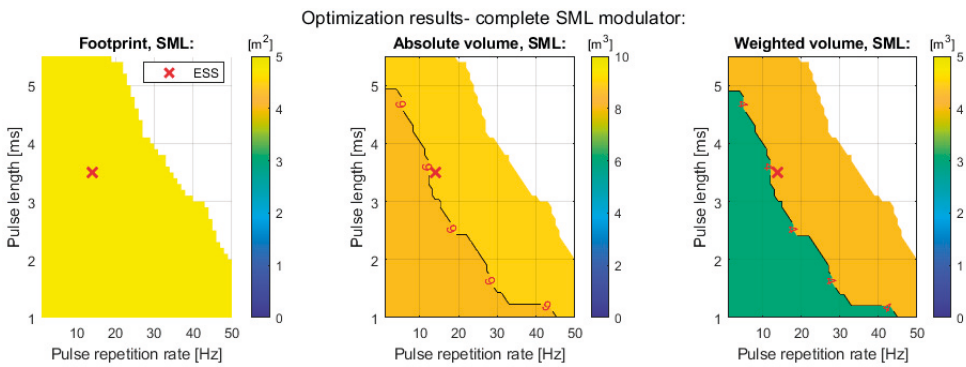



Figure 6.11: Parametric study – footprint, absolute volume and weighted volume of complete stacked multi-level modulator as function of application pulse length and pulse repetition rate

## 6.3 Parametric study: comparison between topologies

The results of the parametric studies presented in Figure 6.4 and Figure 6.11 are shown side by side in Figure 6.12 and combined in Figure 6.13 and Figure 6.14 in providing a comparison between the pulse transformer-based modulator topology and the stacked multi-level modulator topology in view of long-pulse high-power applications. Figure 6.13, first, depicts a direct comparison between the two topologies. Here, the areas shaded in red indicate a comparatively smaller pulse transformer-based modulator, whereas the areas shaded in blue indicate a comparatively smaller stacked multi-level modulator. Here, the compact layout of the SML topology results in a smaller modulator footprint and absolute volume, except in those cases where the average power (or product of pulse length and pulse repetition rate) is low. In those cases, just as discussed in the preceding section, the fixed size of the modulator output stage essentially results in an oversized modulator design (i.e., one that is capable of handling significantly greater average power). Still, it is worth pointing out that the absolute oil volume of the pulse transformer-based modulator generally is smaller than that of the corresponding stacked multi-level modulator. On the other hand, it is emphasized that the required height of the pulse transformer oil tank assembly, here typically upwards of 2 meters, largely offsets this benefit. Then, Figure 6.14 presents the ratio of the same quantities between the stacked multi-level modulator and the pulse transformer-based modulator. First, comparing results for ESS application requirements, the SML modulator permits reduction in modulator footprint and absolute volume of up to ~30% with respect to the conventional pulse transformer-based modulator. Considering applications with considerably longer pulse length or higher pulse repetition rate, greater benefits are seen. As an example, considering applications with twice the pulse length or twice the pulse repetition rate, stacked multi-level modulator footprint and absolute volume approaches only half that of the corresponding pulse transformer-based modulator. Additionally, taking into account also the aforementioned issues of, e.g., manufacturability and maintainability, this comparison draws an approximate delineation indicating both theoretical and practical limits of the pulse transformer-based modulator as well as the range of applications where the added complexity of the stacked multi-level modulator topology is justified.

Finally, it is noted that only application manageable by the pulse transformer-based topology (i.e., those within the maximum attainable pulse length and pulse repetition rate in accordance with the above) have been considered. It is here emphasized that the stacked multi-level modulator has no such fundamental limitation and may, in principle, be extended to handle any combination of pulse length and pulse repetition rate as long as the resulting dimensions are considered feasible.

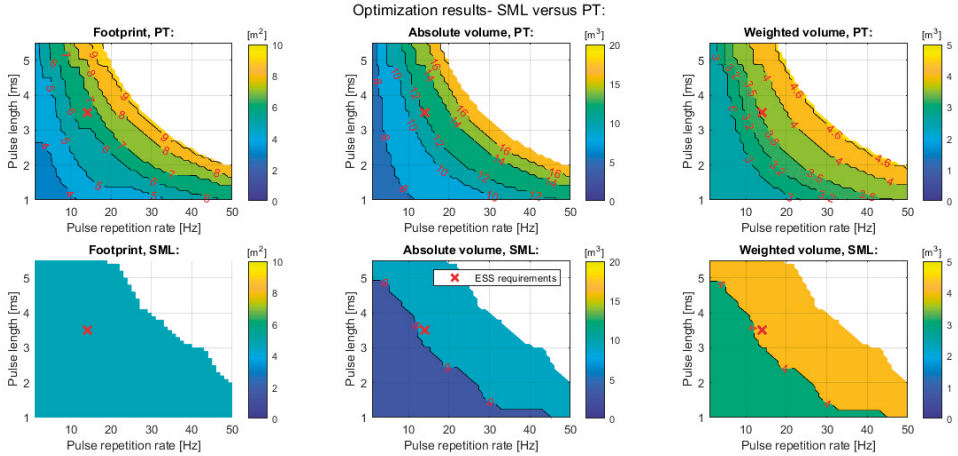



Figure 6.12: Parametric study – optimization results for PT- and SML-based modulators.

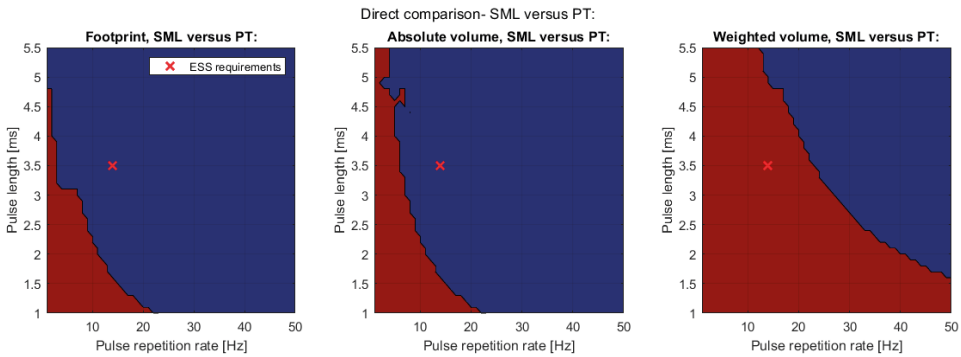



Figure 6.13: Parametric study – direct comparison between pulse transformer-based modulator and stacked multi-level modulator. Areas shaded in red indicate a comparatively smaller pulse transformer-based modulator. Areas shaded in blue indicate a comparatively smaller stacked multi-level modulator.

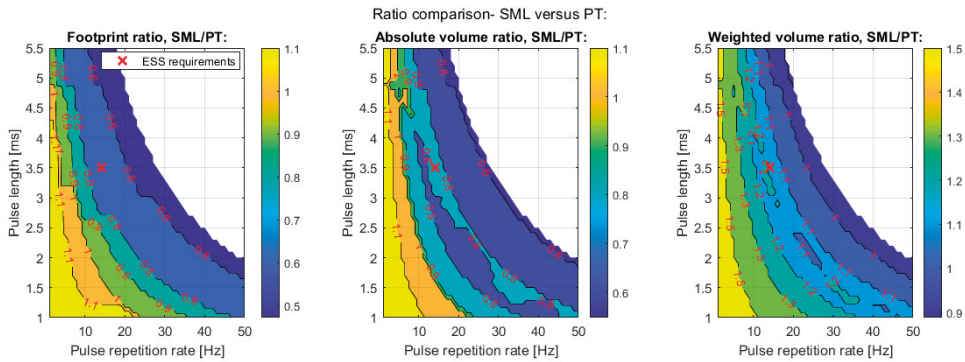



Figure 6.14: Parametric study – relative comparison between pulse transformer-based modulator and stacked multi-level modulator. The plots indicate the ratio between the footprint, absolute volume and weighted volume of the stacked multi-level modulator versus the pulse transformer-based modulator, respectively.

## 6.4 References

[6.1] TDK-Lambda ALE Rack Mount Series. Accessed: June 24, 2023. [Online]. Available: https://www.us.lambda.tdk.com/products/high-voltage-power/capacitor-charging/ale-rackmount.html

[6.2] Technix High Voltage Capacitor Charger. Accessed: June 5, 2023. [Online]. Available: https://technix-hv.com/application-or-function/capacitor-charger/

[6.3] Poynting HV Power Supplies. Accessed: June 24, 2023. [Online]. Available: https://www.poynting.de/en/id-100-kw-and-greater.html

[6.4] SEMIKRON SKM400GB17E4 IGBT Module. Accessed: June 24, 2023. [Online]. Available: https://www.semikron-danfoss.com/products/product-classes/igbt-modules/detail/skm400gb17e4-22895010.html

[6.5] Mitsubishi Electric CM1800HC-34N IGBT Module. Accessed: June 24, 2023. [Online]. Available: https://www.mitsubishielectric.com/semiconductors/php/eTypeNoProfile.php?TYPENO=CM1800HC-34N&FOLDER=/product/powermodule/hvigbt_ipm/n_series

# 7. Control of high-power modulators

## 7.1 Overview

As described in chapter 2, solid state modulators can typically be divided into an input capacitor charging stage and an output pulse generation stage, decoupled by the capacitor bank energy storage. The capacitor charging stage must be designed and controlled to draw the required energy in-between pulse events without disturbing the grid, i.e., generation of current harmonics, reactive power and flicker must be kept to a minimum. Analogously, the pulse generation stage must be designed and controlled to repeatedly and accurately deliver high quality pulse waveforms. Here, pulse rise time and pulse overshoot must both be minimized while ensuring high pulse flat top quality. This chapter is devoted to the analysis and design of practical high-performance controllers for use in high-power modulators. The chapter is disposed as follows-

- Chapter 7.2 focuses on control of the input capacitor charging stage. First, a review and assessment of the control of conventional capacitor chargers is carried out. Given the issues with conventional technology in view of high-power applications, a novel capacitor charging technique for flicker mitigation is proposed. The method is simulated and assessed in view of power quality in both steady state and dynamic pulsing modes. The chapter ends with two brief sections proposing and assessing 1) a single stage flicker-free capacitor charging topology, and 2) improvements to the conventional capacitor charging control strategy based on the addition of an external controller in mitigating flicker and improving power quality.
- Chapter 7.3 discusses control of the SML modulator topology output stage. The models developed in chapter 5 are first translated into an equivalent transfer function-based model for control system analysis. Then, a controller based on the traditional PI control scheme is derived and designed using computational optimization methods. Using the performance of the PI-based controller as benchmark, a simple open loop controller is developed in ensuring pulse-to-pulse repeatability. The performance and properties of the two control methodologies are assessed and compared.

- Finally, chapter 7.4 explores the possibility of using the flexibility and controllability of the SML modulator topology in generating alternating pulsing schemes, i.e., pulse trains in which each pulse may vary in terms of amplitude, pulse length, and frequency. Such schemes may be required in accelerators used in serving several end purposes, and would conventionally require use of multiple parallel modulator systems. In this chapter, SML modulator output pulse quality is studied over the entire range of operation in developing a framework used in assessing such alternating pulsing schemes. The chapter ends with a case study on the proposed European Spallation Source Neutrino Superbeam project, constituting an upgrade of the ESS linac in delivering up to four additional high-power pulses to each nominal 14 Hz cycle.

It is here emphasized that this chapter mainly treats theoretical and simulation work. The corresponding experimental results are detailed mainly in chapters 8 and 9. References to the relevant corresponding sections and published literature are given throughout the chapter.

# 7.2 Input stage converter control

## 7.2.1 Review of performance of conventional capacitor chargers

As was discussed in chapter 4 and as shown in overview in Figure 7.1, commercial high power capacitor chargers are constructed from multiple off-the-shelf charger units operated in parallel. Typically, the front-end of such units are based on passive three-phase six-pulse diode rectifiers. Without compensation, the power factor of such rectifiers is on the order of 0.9 and the THDi of the line current exceeds 30% [7.1]. As described at length throughout this thesis, conventional high power modulator systems typically operate at a relatively high primary-side voltage in reducing the corresponding currents. Clearly, the voltage provided by the rectifier units is insufficient, and resonant transformer-based dc/dc converters are used in stepping up the voltage in charging the capacitor bank energy storage. The associated impact on system volume and efficiency of this type of charger solution was treated in chapter 6. In this section, the corresponding aspects of power quality will be studied in detail through simulation. For these purposes, the functionally equivalent circuit shown in Figure 7.2 is utilized. Here, as all charger units are based on passive front-ends and are connected to a common point of connection, the corresponding line-side quantities of all modules are in phase and may be therefore be added up in forming an equivalent system. Furthermore, the resonant dc/dc converters have been replaced by a simplified equivalent dc/dc converter.

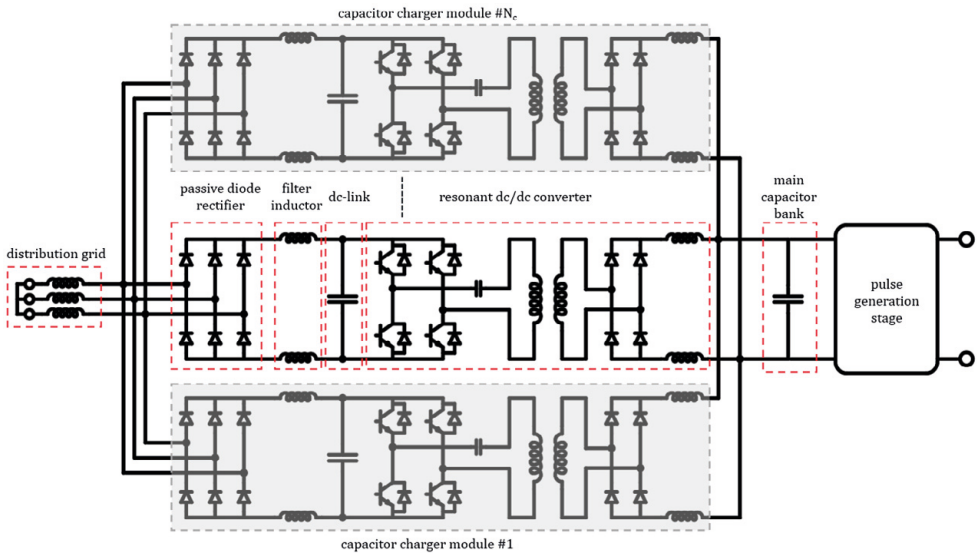



Figure 7.1: High power capacitor charger formed by parallelizing multiple conventional off-the-shelf charger units

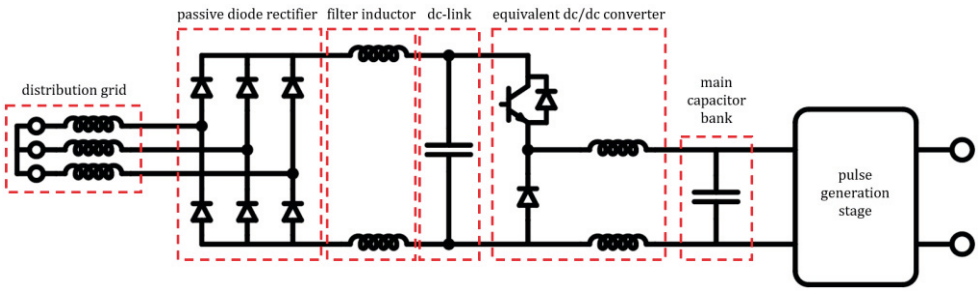



Figure 7.2: Functionally equivalent charger circuit used in simulation

The operation of the dc/dc converters in view of this type of capacitor charger circuit is described in, e.g., [7.2] and is briefly summarized in the following referring to Figure 7.3-

The user sets the desired charging current $I^*$ and the maximum capacitor voltage $V_{Cm}^{max}$ through, e.g., an Ethernet or D-sub interface accessible on the charger front panel. In charging, the (resonant) dc/dc converter is operated in constant current mode in controlling the charging current to be $I^*$. Then, when the capacitor bank voltage reaches $V_{Cm}^{max}$, capacitor charging is interrupted by setting the current reference $I^* = 0$.

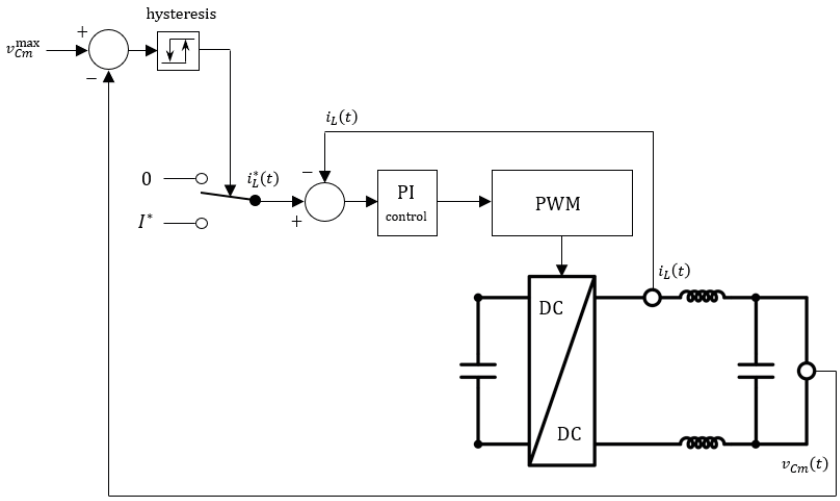



Figure 7.3: Typical control scheme utilized in conventional capacitor charger units

To study the impact on input power quality as a result of this type of capacitor charger control, the equivalent charger shown in Figure 7.2 was set up for ESS modulator operating conditions. Here, the pulse load power was set to 11.5 MW and the distribution grid was represented by a line-to-line voltage of 600 V with a typical short circuit impedance of ~5%. The obtained simulation results are shown in overview in Figure 7.4 and Figure 7.5 and are discussed in the following-

During the pulse event, the capacitor bank voltage droops from the equivalent ~750 V to ~640 V, and must be replenished before the next pulse event. In accordance with the control scheme outlined in Figure 7.3, the dc/dc converter is operated to control the charging current to be $I^*$. The dc/dc converter is operated in constant current mode, i.e., the capacitor bank voltage linearly increases until reaching the voltage $V_{Cm}^{max} = \sim 750\,V$ where capacitor charging is interrupted. Note that this implies that the front-end rectifier output is open circuited, i.e., rectification is also interrupted with the line currents quickly dropping from $I_{L,nom}$ to 0. As the following pulse event takes place, the charging procedure is repeated. Consequently, the line current alternates between 0 and $I_{L,nom}$ at the pulse repetition rate, for high power chargers resulting in significant fluctuations in the voltage at the point of common connection as discussed in chapter 2.

These effects are further studied in Figure 7.5, showing the half-cycle RMS voltage at the point of common connection. As discussed in relation to Figure 2.2, the maximum allowable flicker at the ESS pulse repetition rate of 14 Hz is only 0.3%. Unfortunately, as may be seen, the flicker is in this case more than five times this prescribed limit. Furthermore, as discussed in the above and indicated in Figure 7.4,

the line side current THDi and power factor are poor, matching that typically seen in datasheets for available commercial capacitor chargers.

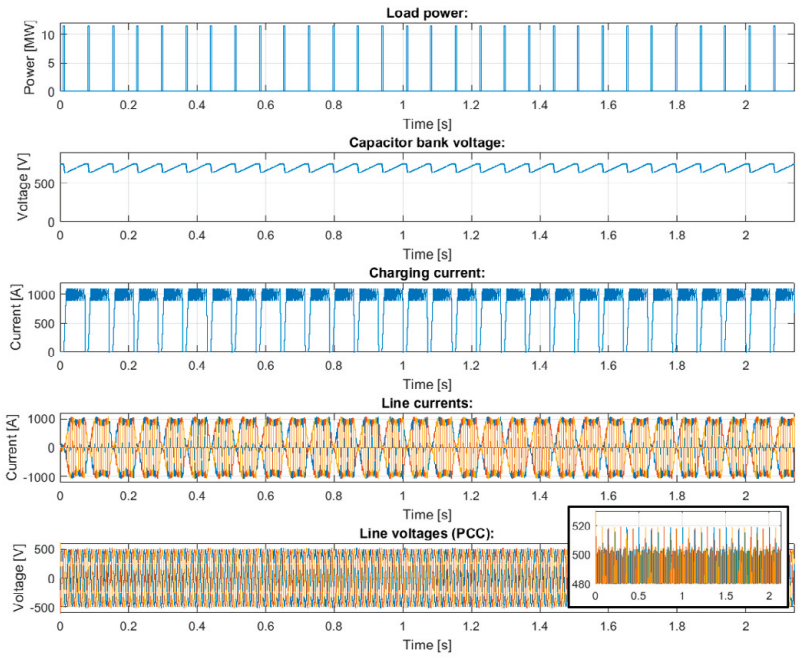



Figure 7.4: Simulation results for equivalent conventional capacitor charger circuit for ESS application requirements

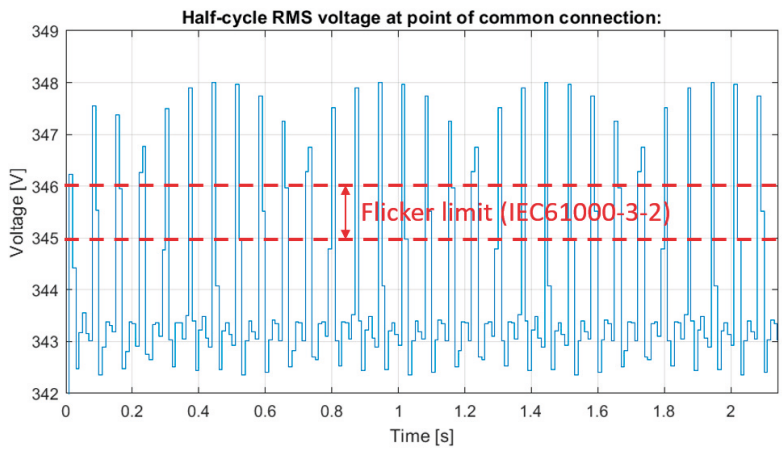



Figure 7.5: Simulated half-cycle RMS voltage at the point of common connection for conventional capacitor charger

It may here be pointed out that a different selection of $I^*$ could eliminate the off-time (i.e., the period of time after $V_{Cm}^{max}$ has been reached and during which charging is interrupted) in minimizing flicker. Practically, however, tuning the reference values of the capacitor charger circuits is non-trivial. Of course, it must be ensured that the charging current is such that the required capacitor bank voltage is available in time for the pulse event. Note also that the corresponding greater or smaller value of the charging current $I^*$ may result in the tendency of the capacitor bank voltage to drift over time when tuned manually. Other drifts originating from, e.g., thermal effects may also exacerbate the issue. A remedy to the shortcomings of control of conventional charger circuits, significantly improving pulse quality, is presented in the addendum given in section 7.2.5.

The issues of poor pulse quality of conventional capacitor charger circuits, in addition to those of size and efficiency presented in chapter 6, are the main reasons this type of charger circuit was not acceptable in view of the ESS application, [7.2]-[7.3]. Chapter 5 discussed designed of the developed SML modulator input capacitor chargers. The subsequent section details a new type of capacitor charging scheme in achieving flicker-free and highly dynamic charger performance.

### 7.2.2 Proposed capacitor charging scheme for constant power charging

The working principle of the SML modulator input charger units was introduced in chapter 3. A schematic overview of a single charger module to be considered from the perspective of control is shown in Figure 7.6. Note the functional equivalency to that presented in Figure 7.2. Here, the main difference lies in 1) the utilization of an active front-end rectifier circuit, permitting shaping of the line current in improving the THDi and the power factor; and 2) the utilization of a different capacitor charging scheme used in controlling the dc/dc converter in mitigating flicker. Control of these circuits is discussed in the following.

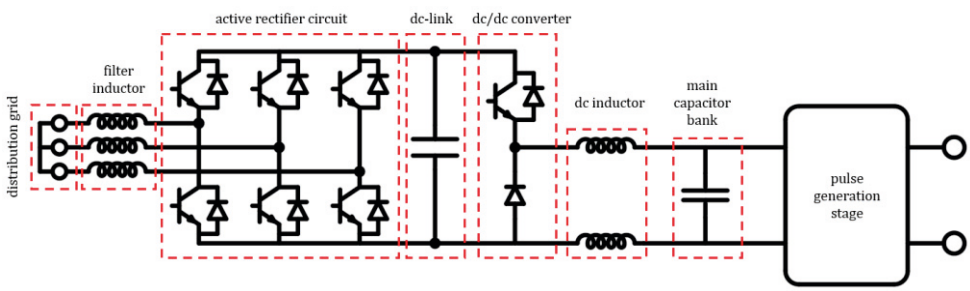



Figure 7.6: Schematic overview of single capacitor charger module used in the developed SML modulators

*Active rectifier control*

The basic procedure used in controlling the active rectifier circuit is summarized in Figure 7.7. The goals of this control procedure are twofold. First, to obtain the desired dc-link voltage $v_{dc}^{*}$ serving as input to the dc/dc converter stage. Second, to shape the line currents to be sinusoidal and in phase with the corresponding line voltages. As shown in Figure 7.7, control is handled in a synchronous frame $dq$, where the q-axis has been aligned with the grid voltage space vector $\vec{e}$.

The current controller is designed and implemented using the methods outlined in [7.4]. There, and as can be seen in Figure 7.7, a PI controller with active damping is proposed. The controller parameters are selected according to the principles of internal model control (IMC), [7.4]-[7.6], (7.1)-(7.3). Here, $\langle L_2 \rangle$ represents an estimate of the converter-side inductance value $L_2$, $\langle R_{L2} \rangle$ represents an estimate of the series resistance associated with the converter-side inductor $L_2$, $\alpha_c$ is the desired bandwidth of the current controller, and $R_d$ is the active damping gain

$$k_p = \alpha_c \langle L_2 \rangle \tag{7.1}$$

$$k_i = {\alpha_c}^2 \langle L_2 \rangle \tag{7.2}$$

$$R_d = \alpha_c \langle L_2 \rangle - \langle R_{L2} \rangle \tag{7.3}$$

The input to the current controller is formed by $i^* = i_d^* + j i_q^* = j i_q^*$ in accordance with the above in minimizing reactive power.

The q-axis current reference $i_q^*$ is formed by the dc-link voltage controller in addition to a current feed-forward term supplied by the dc/dc converter control scheme, to be discussed in the following section. As seen, the dc-link voltage controller takes the same form as the proposed current controller, but is designed for a different bandwidth $\alpha_v \leq \sim \alpha_c/10$, [7.4].

Simulation of the equivalent charger circuit shown in Figure 7.6 for the ESS modulator design developed in chapter 5 is shown in overview in Figure 7.8. As can be seen, during the pulse event, the dc-link voltage varies somewhat but is kept stable, well within 1% of the nominal dc-link voltage value, by the dc-link controller hence serving as a stiff voltage input to the dc/dc converter. Importantly, as desired, the line currents are sinusoidal and in phase with the corresponding line voltages. The resulting power quality, i.e., the line current $\text{THD}_\text{i}$, the power factor and the voltage flicker are assessed in simulation in section 7.2.3 and experimentally in chapters 8 and 9.

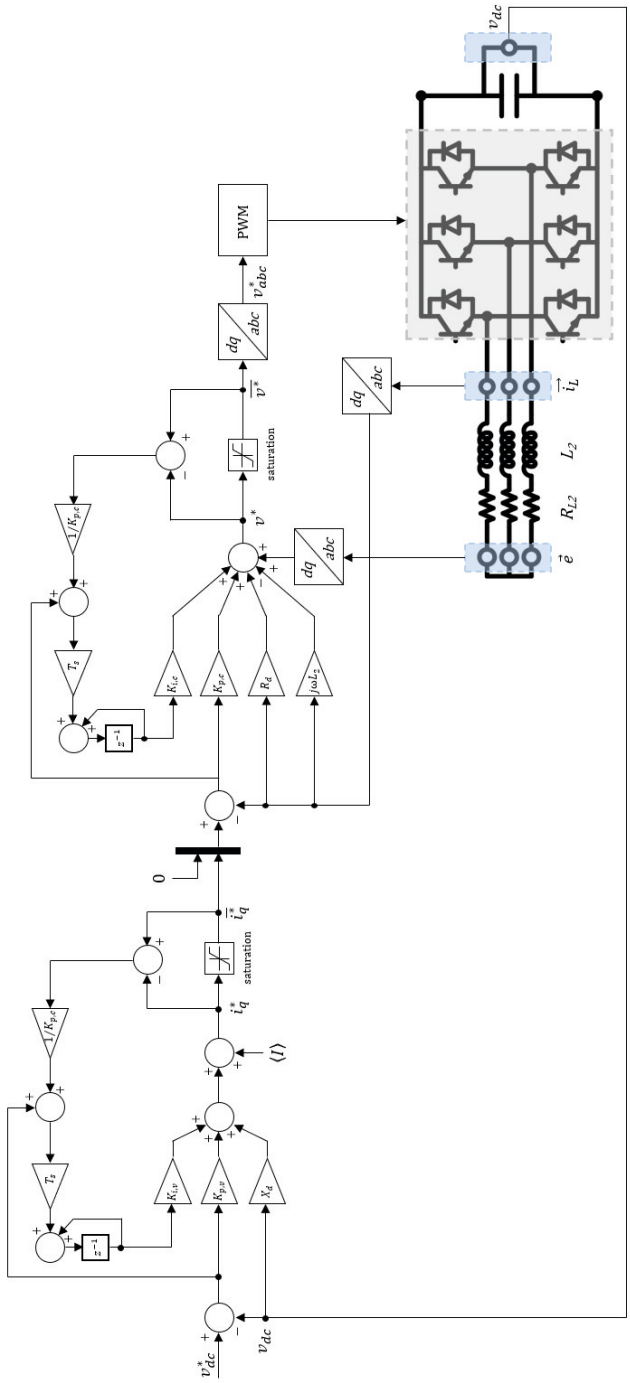



Figure 7.7: Active rectifier control

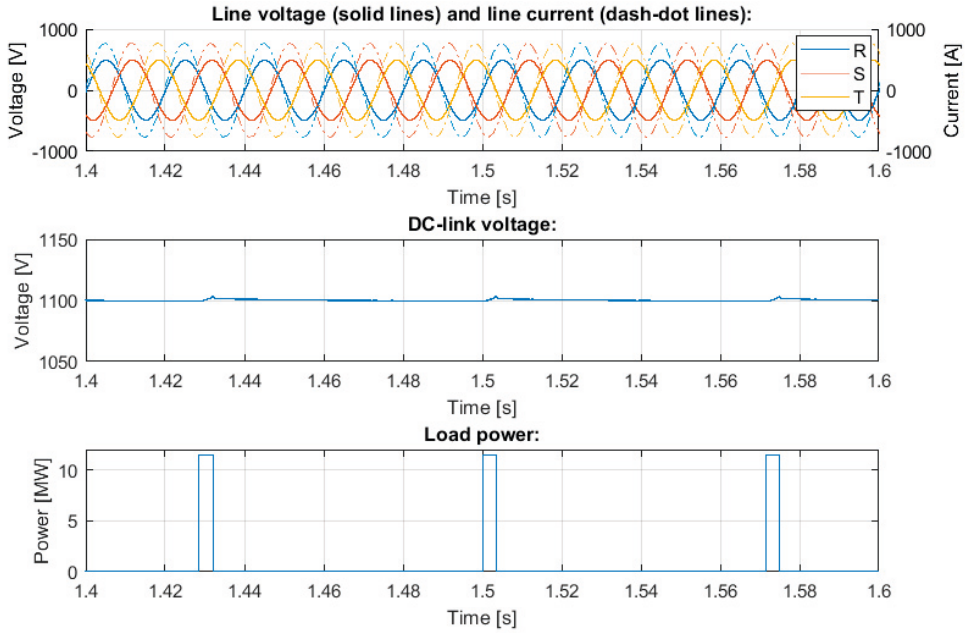



Figure 7.8: Active rectifier operation

*DC/DC converter control*

The dc/dc converter charges the main capacitor bank. As indicated in the preceding section, it is desirable to charge the capacitor bank to, first and foremost, avoid interruption in the charging cycle as exemplified in, e.g., Figure 7.4. Additionally, it is preferable to also continuously adjust the charging current reference in relation to the increasing capacitor bank voltage throughout the charging cycle in maintaining constant power charging, [7.2]-[7.3]. A practical implementation of such a control scheme is discussed in the following referring to Figure 7.9. The method is summarized in Figure 7.10.

- An inner current controller regulates the instantaneous value of the charging current, i.e., the current at the output of the dc/dc converter $i_L(t)$. The error between the current reference, $i_L^*(t)$, and $i_L(t)$ is injected into a PI controller. The output of the PI controller is the reference signal for the pulse width modulation block generating the gating signals for the dc/dc converter IGBT modules.
- The signal $i_L^*(t)$ takes one of two values, chosen by a two-state switch depending on the mode of operation. In steady state pulsing, the capacitor bank voltage is expected to always be significantly lower than absolute maximum voltage allowed at the capacitor bank $v_{Cm}^{max}$. In this condition, the

switch selects the signal $i_L^*(t) = P_c^*/v_{Cm}(t)$, where $P_c^*$ is the charging power reference and $v_{Cm}(t)$ is the instantaneous capacitor bank voltage. Assuming the dc/dc converter current controller has an appropriately selected bandwidth, $i_L(t) \approx i_L^*(t)$ such that $p_c(t) = v_{Cm}(t)i_L(t) = v_{Cm}(t)i_L^*(t) = P_c^*$. On the other hand, if the capacitor bank voltage exceeds $v_{Cm}^{max}$, the switch instead selects the signal $i_L^*(t) = 0$ to interrupt charging.

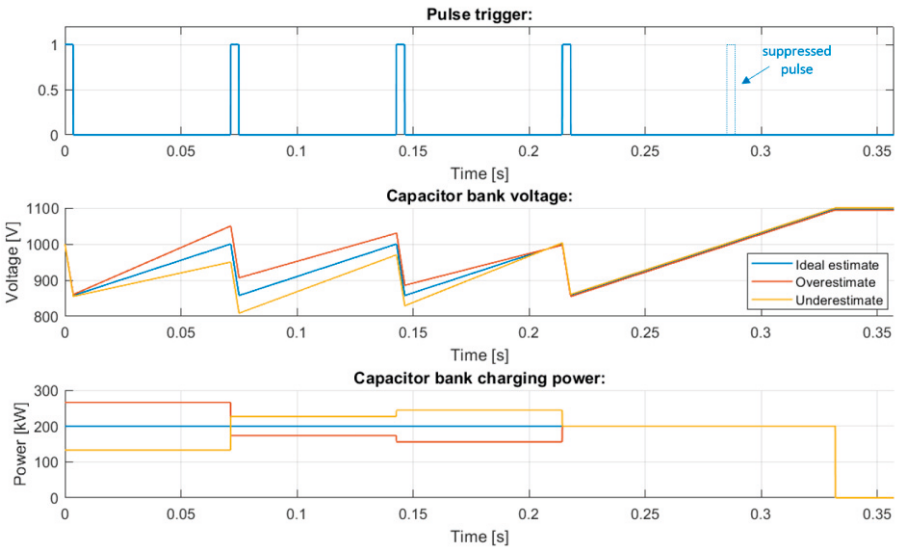



Figure 7.9: Proposed control principle to stabilize the capacitor bank voltage through regulation of the charging power

The charging power reference $P_c^*$ is calculated using a discrete power regulation loop, as follows-

1) At the instant pulse number $k$ ends, $t_{kp}$, the value of the capacitor bank voltage $v_{Cm}(t_{kp})$ is sampled and held.
2) Ideally, the capacitor bank voltage should reach its reference value $v_{Cm}^*$ precisely the instant the next pulse $k+1$ begins. Hence, under ideal conditions, (7.4) holds.

$$v_{Cm}(t_{k+1}) = v_{Cm}^* \tag{7.4}$$

3) The amount of energy to be injected into the capacitor bank to, ideally, achieve the condition given by (7.4) may be calculated according to (7.5).

$$\Delta E_{kp} = \frac{1}{2} C_m \left[ (v_{Cm}^*)^2 - v_{Cm}(t_{kp})^2 \right] \tag{7.5}$$

4) To achieve constant power charging, this energy should be delivered evenly throughout the period of time between $t_{kp}$ and $t_{k+1}$, i.e., the duration given by $1/f_r - T_p$. Hence, the charging power may ideally be predicted to be $P_c^* = (P_c^*)_{PR}$ according to (7.6).

$$(P_c^*)_{PR} = \frac{\Delta E_{kp}}{1/f_r - T_p} = \frac{1}{2(1/f_r - T_p)} C_m \left[ (v_{Cm}^*)^2 - v_{Cm}(t_{kp})^2 \right] \tag{7.6}$$

5) Under ideal conditions, i.e., neglecting system losses and assuming perfect parameter estimation, (7.6) is sufficient to calculate the required power reference $P_c^*$ in accordance with the above. However, in practice, these uncertainties would lead to a recurrent steady state offset error.

6) In order to correct this error, an additional correction term based on feedback error accumulated from preceding pulse periods is added. In this case, a discrete PI controller is utilized where the corrective power reference term $(P_c^*)_{CR}$ corresponding to pulsing period $k$ is given by (7.7). Here, $k_p$ and $k_i$ are the PI controller parameters and $v_{Cm}(t_{k-1})$ is the sampled and held capacitor bank voltage value for the former pulsing period $k-1$.

$$(P_c^*)_{CR} = k_p [v_{Cm}^* - v_{Cm}(t_{k-1})] + k_i \int_z [v_{Cm}^* - v_{Cm}(t_{k-1})] \, dt_z \tag{7.7}$$

7) Finally, the required charging power $P_c^*$ is the sum of the predicted charging power $(P_c^*)_{PR}$, according to (7.6), and the corrective charging power $(P_c^*)_{CR}$, according to (7.7), (7.8).

$$P_c^* = (P_c^*)_{PR} + (P_c^*)_{CR} \tag{7.8}$$

The proposed control scheme is validated and assessed in the following section.

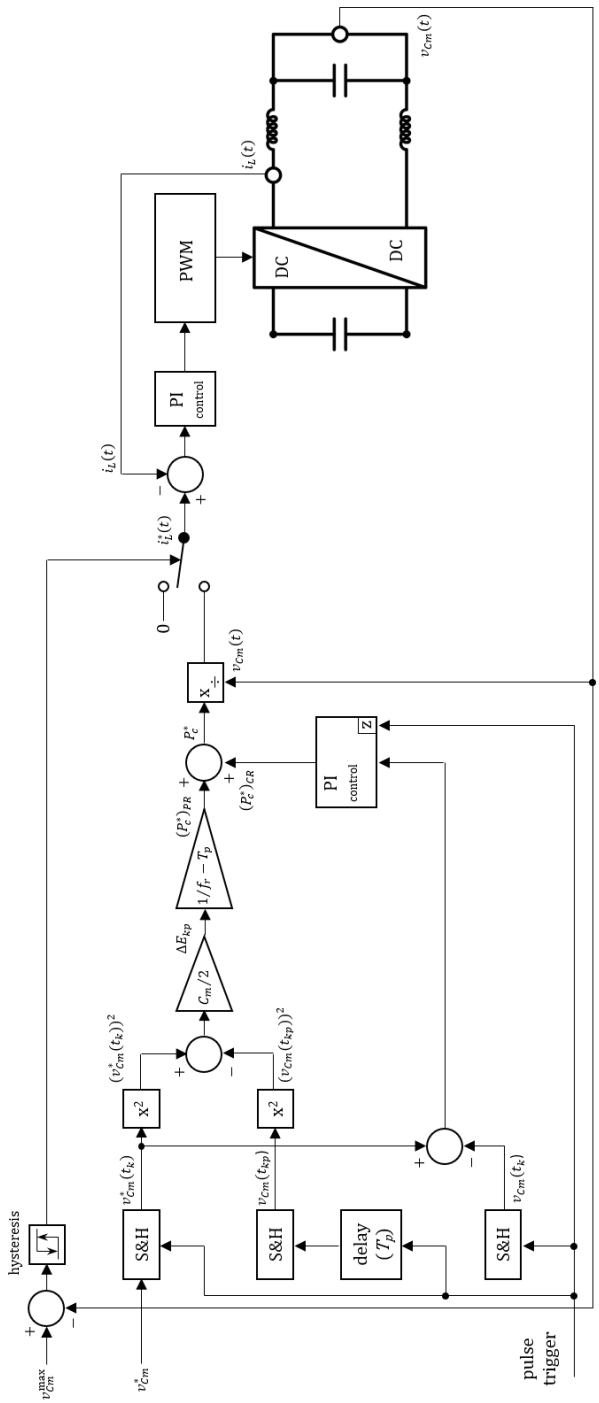



Figure 7.10: Diagram of proposed capacitor charging algorithm for flicker mitigation

### 7.2.3 Simulation results

The equivalent charger circuit shown in Figure 7.6 is simulated with the circuit parameter values derived considering the ESS application requirements in chapter 5 and using the proposed control scheme presented in section 7.2.2. Here, as explained in chapters 3 and 5, three active rectifier circuits are operated in parallel with phase shifted PWM carrier waves to obtain line side current ripple cancellation. Note that this does not affect the control principles outlined in Figure 7.7 and Figure 7.10. In this simulation – in order to correspond to that discussed in section 7.2.1 – the three active rectifiers are connected in parallel at their outputs in sourcing a single dc-link, dc/dc converter, and capacitor bank.

*Steady state operation*

First, operation in steady state pulsing is discussed, Figure 7.11 and Figure 7.12. During the pulse event, the capacitor bank voltage droops from the nominal 1 kV to ~850 V, in accordance with the design presented in chapter 5. Now, the predicted required charging power is calculated according to (7.6), yielding $i_L^*(t) = P_c^*/v_{Cm}(t)$. The dc/dc converter is controlled to quickly output the desired charging current. Importantly, as the capacitor bank voltage $v_{Cm}(t)$ increasing during the charging cycle, the reference current $i_L^*(t)$ and, consequently, the charging current are adjusted in ensuring constant power charging. Note that in this ideal case where $P_c^* = (P_c^*)_{PR}$, steady state constant power charging is immediately achieved after a single pulsing cycle. The robustness of this controller is assessed experimentally in section 8.3.3.

Importantly, note the line current THD, below 1%, and the power factor approaching 1. In particular, the half cycle RMS value of the voltage at the point of common connection is now on the order of ~0.1 V, an order of magnitude below the limit prescribed by applicable standards, Figure 7.12, representing an improvement with respect to conventional charger circuitry on the order of 50 times.

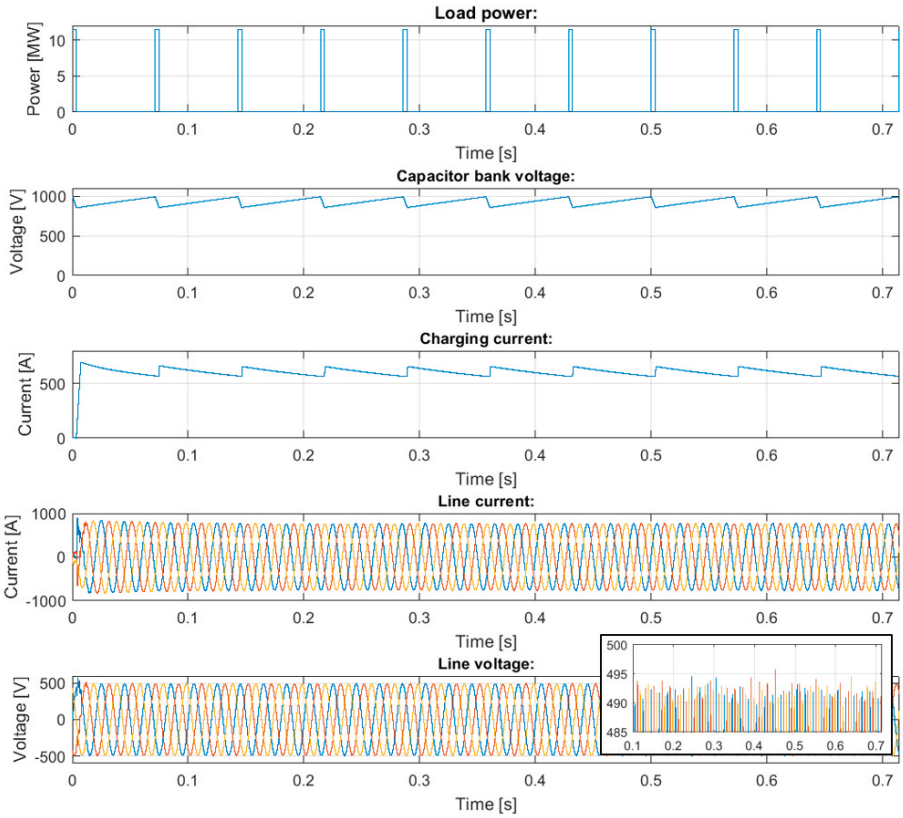



Figure 7.11: Simulated waveforms for equivalent charger circuit operated with proposed control procedure

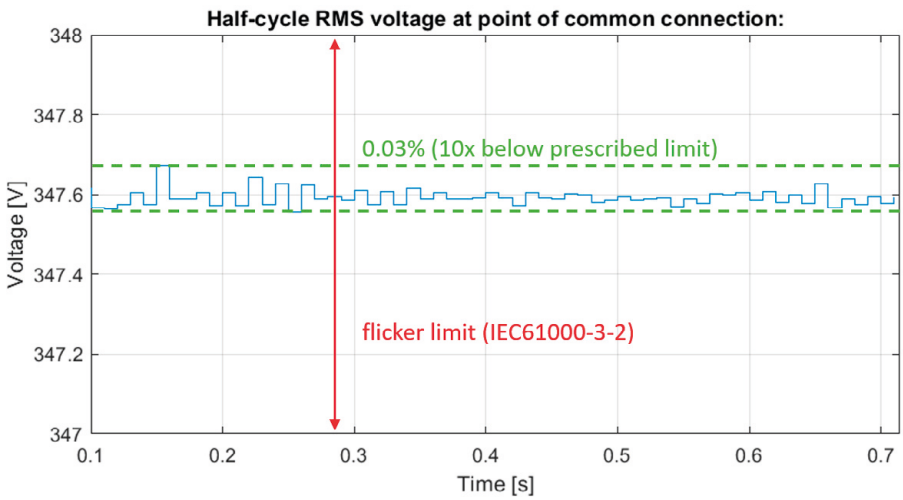



Figure 7.12: Simulated half-cycle RMS voltage at the point of common connection for proposed capacitor charger

*Dynamic performance*

Now, the dynamic performance of the proposed capacitor charger and control procedure will be assessed.

First, Figure 7.13 shows simulation results in pulsed mode with start and stop transients. In the period of time labelled 'A', the modulator is operating in steady state nominal pulsed mode as shown in Figure 7.11. Then, at some point after the third pulse event, the pulse trigger signal is no longer being sent. Hence, following completion of the third charging cycle, $v_{Cm} = v_{Cm}^* \rightarrow P_c^* = 0$, and charging stops. At this point in time, as the line current is decreased, there is an unavoidable permanent increase in the RMS voltage at the point of common connection seen during the period labelled 'B'. In this case, however, there is also a transient increase in the voltage at the point of common connection in avoiding overcharging the dc-link capacitor. This transient can be mitigated by tuning of the dc-link voltage controller. On the other hand, as the transient is both limited, lasts only half a grid period and only occurs during very specific and irregular events not covered by applicable standards, this may be considered permissible.

Finally, at $t = 0.5\ s$, pulsing begins again, and the voltage at the point of common connection again decreases slightly. Especially note that steady state is reached within one cycle such that no real disturbance on the grid may be observed.

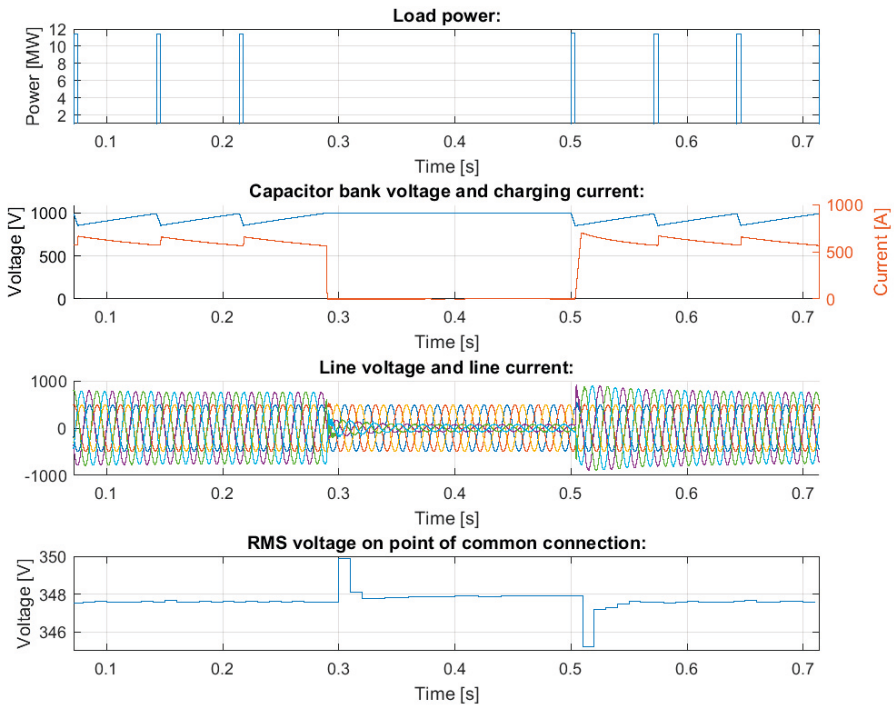



Figure 7.13: Operation of proposed capacitor charger in pulsed mode with start-stop transients

Then, Figure 7.14, shows simulation results in pulsed mode with changes to the pulse repetition rate. Again, the simulation begins with a period of time labelled 'A' during which the modulator is pulsing in steady state at nominal operating conditions. Then, prior to $t = 0.5\ s$, the pulse repetition rate is changed from the nominal 14 Hz to 4 Hz. Thus, immediately following the pulse event at $= 0.5\ s$, the predicted power reference is recalculated according to the new pulsing conditions, (7.6). Consequently, the charging power is significantly reduced and the desired capacitor bank voltage is again reached just in time for the following pulse event.

The pulse repetition rate is similarly changed back from 4 Hz to the nominal 14 Hz at some point prior to $t = 1.0\ s$. Again, the controller adjusts within a single charging cycle.

It is pointed out that, in these cases, the properties of the pulsing signal are known by the controller. However, it is also possible to operate the capacitor chargers in this charging scheme with an external pulse trigger signal. In such a case, the time between consecutive triggers can be counted and used to adjust the predicted power reference, (7.6). In this case, one pulse period (and, thus, charging period) is required to calculate the pulse repetition rate, such that the charger adjusts within two cycles. This is described and studied experimentally in section 8.3.3.

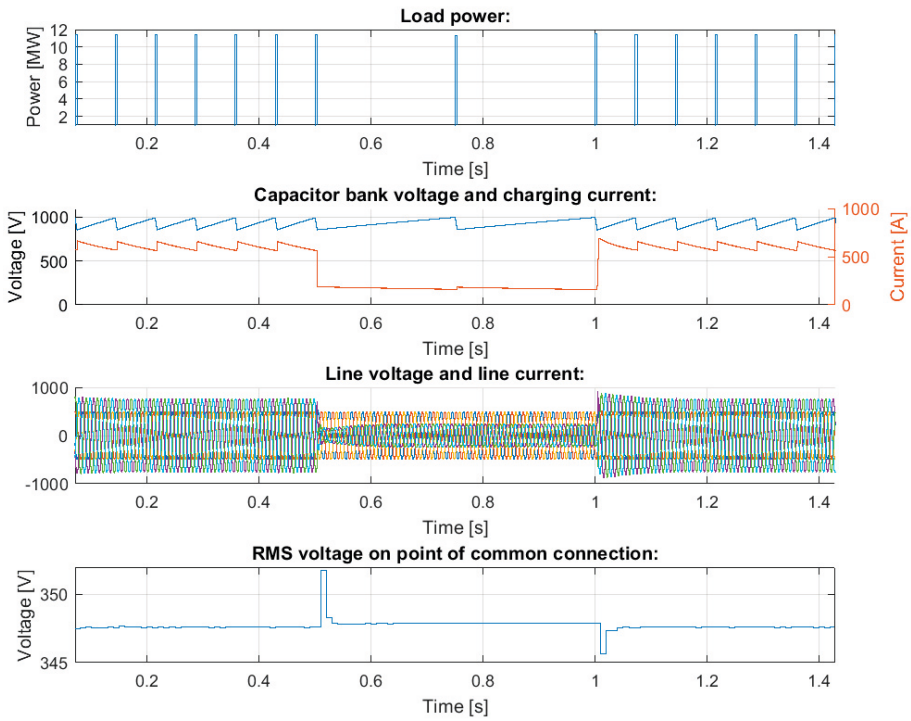



Figure 7.14: Operation of proposed capacitor charger in pulsed mode with sudden changes in pulse repetition rate

Similar to the preceding case, Figure 7.15 shows simulation results in pulsed mode with sudden changes to the output pulse width. Again, the simulation begins with a period of time labelled 'A' during which the modulator is pulsing in steady state at nominal operating conditions. Then, prior to $t = 0.5\ s$, the desired pulse length is changed from the nominal 3.5 ms to 0.5 ms. Thus, immediately following the pulse event at $t = 0.5\ s$, the predicted power reference is recalculated according to the new pulsing conditions, (7.4)-(7.6). Consequently, the charging power is significantly reduced and the desired capacitor bank voltage is again reached just in time for the following pulse event.

Then, for the periods labelled 'C' and 'D', the desired pulse length is increased to 2 ms and, finally, 3.5 ms, respectively. As may be seen, the charger reaches steady state within a single cycle. Note that if an external pulse trigger signal is used in this case, the charger would still react and reach steady state within a single charging period. This is because, in this case, the considerable change to $(P_c^*)_{PR}$ is given by the measured change in the capacitor bank voltage, (7.4). This is also demonstrated in the later chapters on experimental validation.

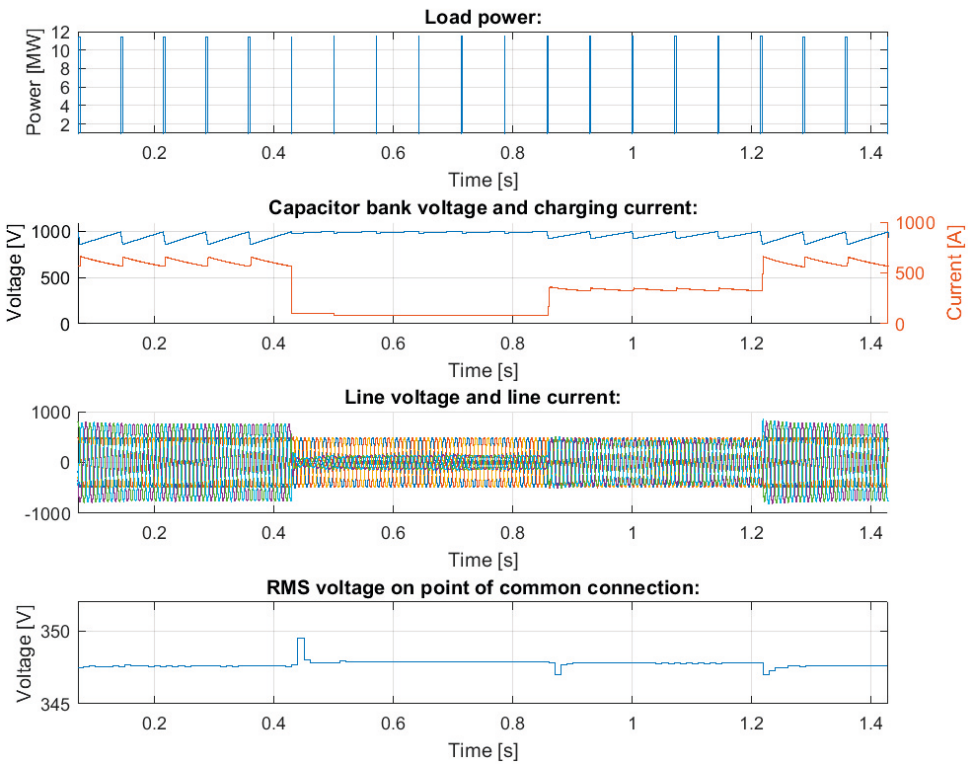



Figure 7.15: Operation of proposed capacitor charger in pulsed mode with sudden changes in pulse width

Finally, Figure 7.16 shows simulation results in pulsed mode with sudden changes to the capacitor bank voltage setpoint. Again, the simulation begins with a period of time labelled 'A' during which the modulator is pulsing in steady state at nominal operating conditions. Then, prior to the pulse event at $t = 0.5\ s$, the capacitor bank voltage setpoint is reduced from the nominal 1 kV to 700 V. In this case, as the dc/dc converter in Figure 7.6 is implemented as a one-quadrant converter (in practice, the converter itself is a two-quadrant converter, but is effectively limited to operation in a single quadrant due to the inclusion of series diodes; see chapters 8 and 9), $v_{Cm}(t_{kp}) > v_{Cm}^{*}$, and charging stops. Hence, during the period of time labelled 'B', charging is inhibited for a series of pulses until again $v_{Cm}(t_{kp}) < v_{Cm}^{*}$ and charging may commence. This is exemplified in the period of time labelled 'C'.

Then, for $t = 0.8\ s$ and $t = 1.2\ s$, the voltage setpoint is increased to 850 V, and back to the nominal 1000 V, respectively. In these cases, importantly, the dc/dc converter charging current is saturated by the current controller in attempting to raise the capacitor bank voltage in a single charging cycle. Hence, during these charging periods, the charging power is not constant. Still, after a couple of cycles of constant current charging, the desired capacitor bank voltage is reached and constant power charging resumes. Note that, in practice, this issue is often avoided by ramping the capacitor bank voltage setpoint at a rate much slower than that of the corresponding pulse repetition rate.

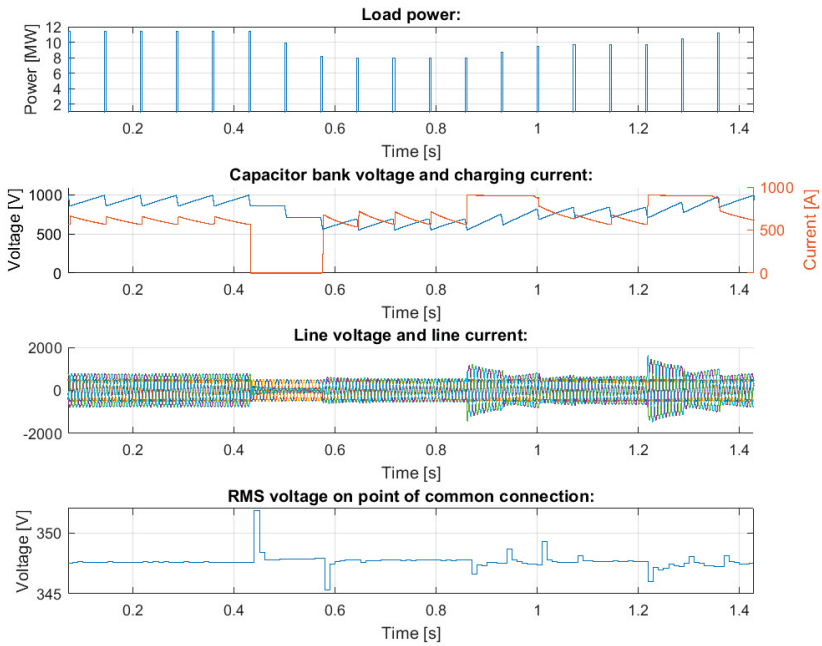



Figure 7.16: Operation of proposed capacitor charger in pulsed mode with sudden changes in voltage setpoint

### 7.2.4 Addendum: constant power charging for single-stage topology

Comparing the simulation results obtained for conventional charger control, Figure 7.4 and Figure 7.5, to those correspondingly obtained using the proposed charging method, Figure 7.11 and Figure 7.12, it is clear that the latter represents significant improvements with respect to input power quality. It is here pointed out that similar performance could, in principle, be attained despite removing the dc/dc converter in forming a single stage capacitor charging topology. In this case, the dc-link of the active rectifier would be merged with that of the capacitor bank. This type of operation is possible as, first, the active rectifier may be operated for a range of dc-link voltages, [7.7], and as the bandwidth of the active rectifier current controller may (in this case easily) be selected such that it can operate despite the continuously albeit slowly varying dc-link voltage (i.e., capacitor bank voltage). In this case, the modulation index of the converter would simply be varied in response to the varying dc-link voltage in ensuring constant power charging.

The proposed adapted circuit and corresponding control loop is presented in Figure 7.17. Importantly, the dc-link voltage regulator has now been removed. Instead, the q-axis current reference is set only by the current feed-forward derived from the power controller presented in Figure 7.10.

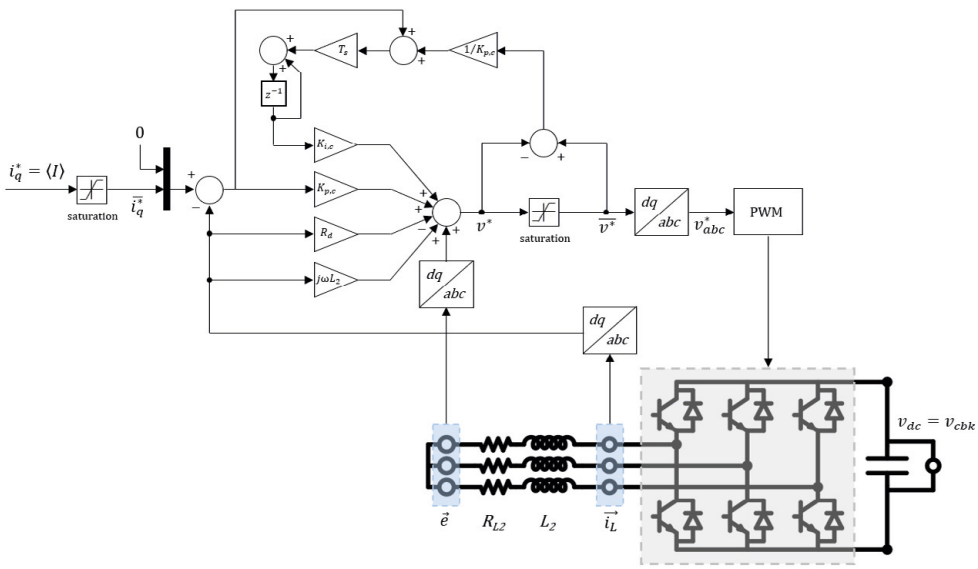



Figure 7.17: Proposed single stage capacitor charger architecture for constant power charging

Running a simulation of a single charger circuit such as that proposed in Figure 7.17, i.e., adjusting the modulator output power to one third of that shown in Figure 7.4 and Figure 7.11, yields the simulation results presented in Figure 7.18. Note that

though results equivalent to those presented in Figure 7.11 are mostly obtained, there are instances in time at which the line current is distorted, resulting in brief (though still within the limits prescribed by applicable standards) variations in the half-cycle RMS value of the voltage at the point of common connection. This is explained by the fact that the capacitor bank voltage, during the pulse, has decreased sufficiently such that the active rectifier is overmodulated, i.e., the modulation index exceeds 1. This may be remedied by increasing the capacitance of the capacitor bank somewhat. This is exemplified in Figure 7.19, for which the capacitor bank has been increased by 50% in limiting the capacitor bank droop somewhat. Here, as can be seen, the line current is fully sinusoidal and again comparable to that seen in Figure 7.11. Again, the generated flicker is an order of magnitude below that prescribed by applicable standards.

It is noted that these results have been obtained for the circuit parameters developed for the circuit presented in Figure 7.6. In practice, optimization would have to be carried out for the circuit in Figure 7.17 to be fully comparable. At the same time, as clearly demonstrated by Figure 7.18, it shall be pointed out that this type of circuit imposes a clear and non-negligible boundary on the capacitor bank voltage and thus, in a sense, the range of operation of the modulator.

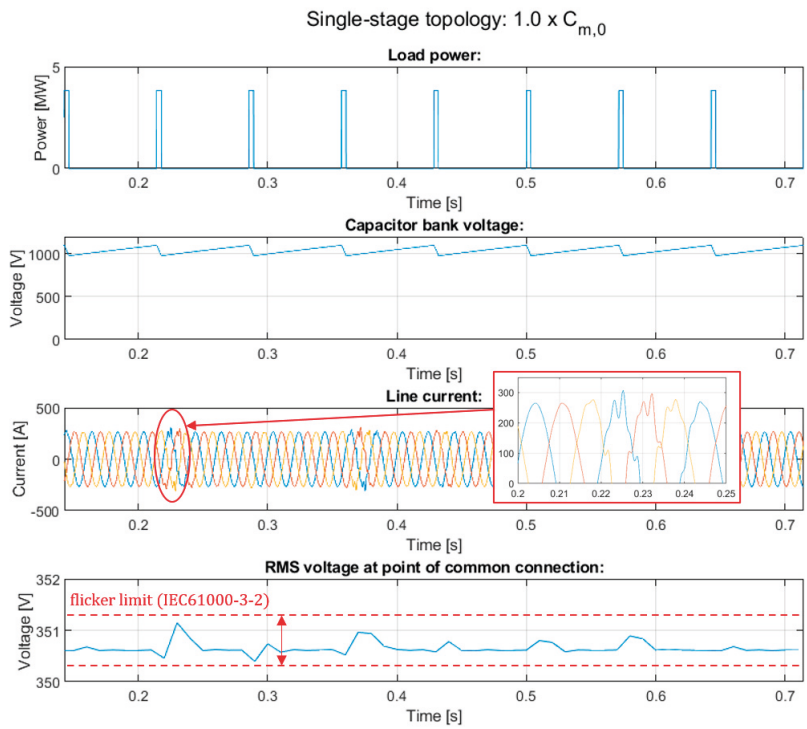



Figure 7.18: Simulation results for single stage capacitor charger topology

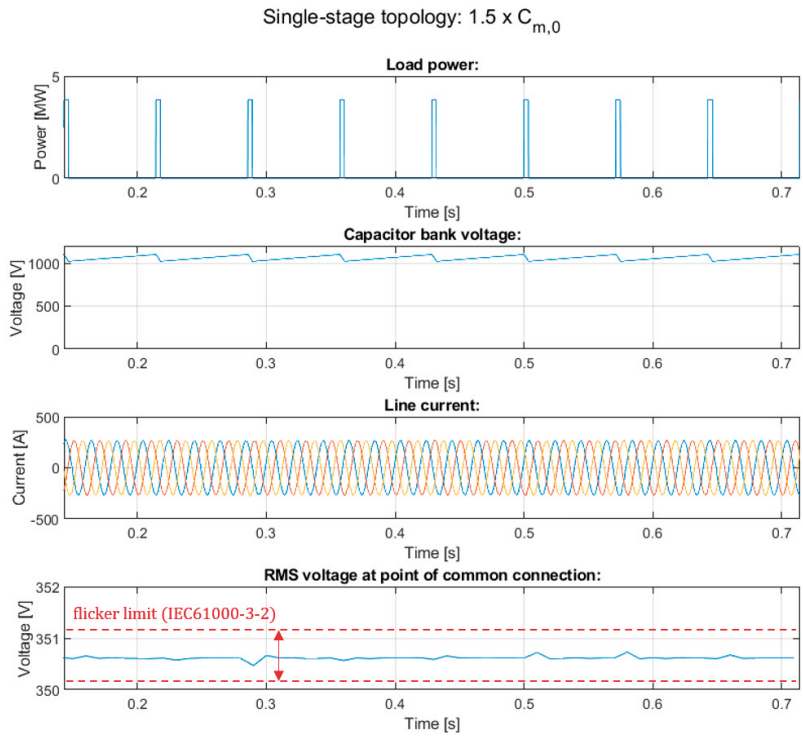



Figure 7.19: Simulation results for single stage capacitor charger topology with increased capacitor bank

### 7.2.5 Addendum: improvement to conventional capacitor chargers

As discussed in section 7.2.1, conventional capacitor chargers are inherently controlled in constant current mode, with charging being interrupted each pulse cycle as the capacitor bank reaches the imposed voltage setpoint. As was demonstrated in Figure 7.4 and Figure 7.5, this type of operation is undesirable, in particular with flicker exceeding an order of magnitude beyond that prescribed by applicable standards. In this section, a simple external controller is proposed in improving the performance of conventional capacitor chargers-

As shown in Figure 7.3, the user sets the desired charging current $I^*$ and the maximum capacitor voltage $V_{Cm}^{max}$. In this method, Figure 7.20, the user instead externally sets the desired capacitor bank voltage $v_{Cm}^*$, from which the maximum capacitor bank voltage is calculated to be $V_{Cm}^{max} = v_{Cm}^* + \Delta V_{max}$. Here, $\Delta V_{max}$ is some value set to ensure that $V_{Cm}^{max}$ is 1) comfortably above $v_{Cm}^*$ such that uninterrupted charging may be obtained, yet 2) within the maximum voltage handling capability of the capacitor bank for safe operation. Then, $v_{Cm}^*$ is compared to the instantaneous capacitor bank voltage $v_{Cm}(t)$ in forming the reference for an external PI controller setting $I^*$. It is here pointed out that there is often considerable

delay in setting $I^*$ such that constant current charging is still attained throughout the charging cycle. Still, as complete on/off operation of the capacitor charger units may be avoided, flicker may be significantly reduced.

The procedure is exemplified in Figure 7.21, showing simulation results obtained using the circuit shown in Figure 7.2 and for the conditions used in obtaining Figure 7.4 and Figure 7.5, but implementing the control method summarized in Figure 7.20. As can be seen, in steady state pulsed mode, the capacitor charging current is constant. Consequently, the capacitor bank voltage increases linearly during the charging cycle. Hence, the charging power varies throughout the cycle. Clearly, from the above description and as seen in Figure 7.21, the charging power varies to the extent given by $\Delta V_{Cm}/V_1$. Hence, for a typical capacitor bank droop $\Delta V_{Cm}$ ~20% of $V_1$, it should be possible to reduce the variations in the half cycle RMS voltage at the point of common connection by at least a factor 5; reducing the ~5 V variation demonstrated in Figure 7.5 to just below ~1 V, or precisely within the limits prescribed by applicable standards. This is demonstrated in Figure 7.22 in which the simulation results presented in Figure 7.5, Figure 7.12 and Figure 7.21 are compared. As can be seen, the method proposed in Figure 7.20 considerably reduced the variation in the half cycle RMS voltage at the point of common connection by more than 5 times. Still, the method proposed in Figure 7.10, represents yet another tenfold improvement. Hence, if conventional capacitor charging solutions must be used, the proposed method represents a possible solution in mitigating flicker.

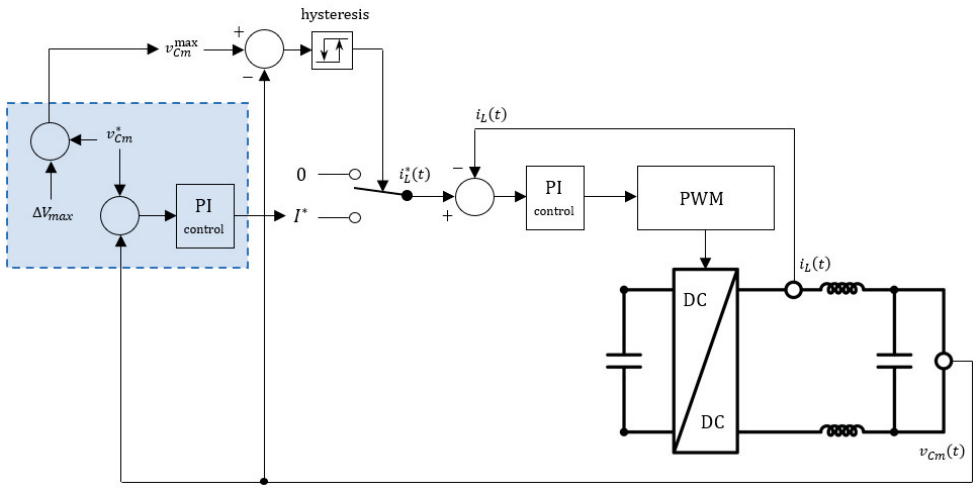



Figure 7.20: Adjusted control loop. The block in blue represents the addition of an external controller setting the inputs at the interface of the conventional capacitor charger according to an externally set capacitor bank voltage setpoint in mitigating flicker.

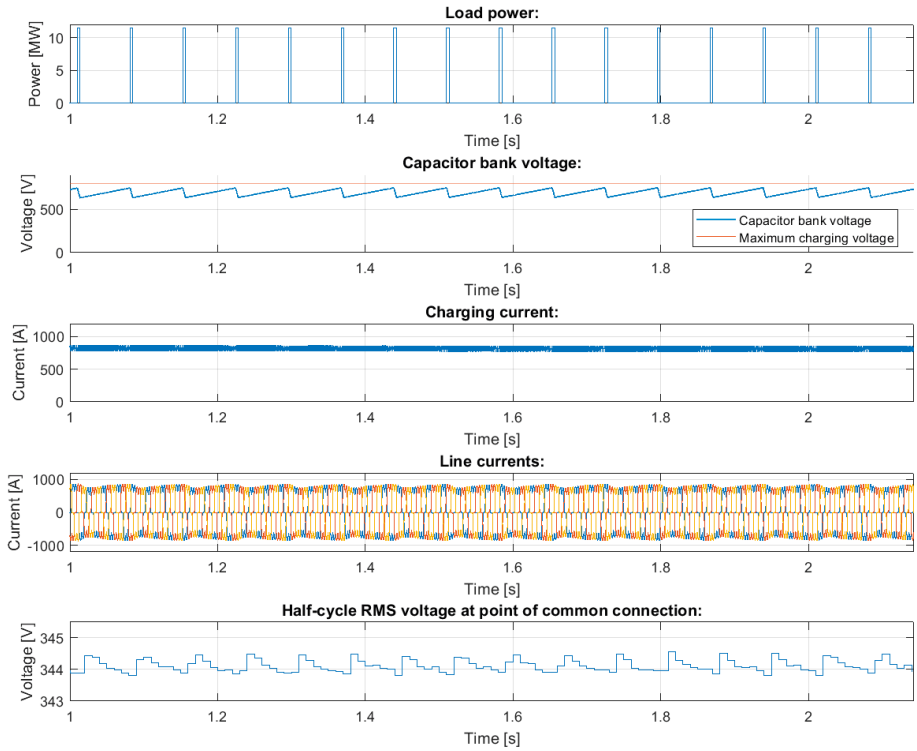



Figure 7.21: Simulation results for conventional charger circuit controlled by proposed method for flicker mitigation

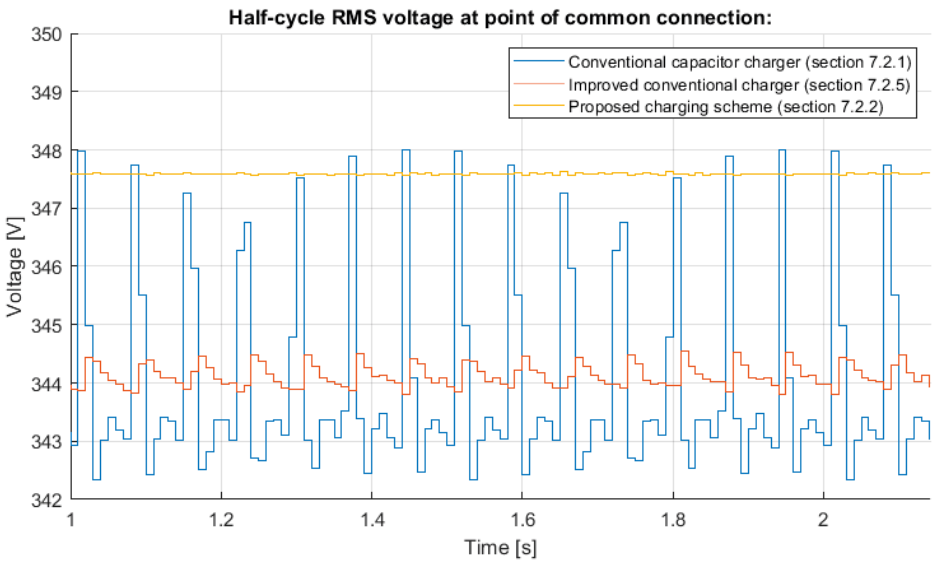



Figure 7.22: Comparison of simulated variation in half cycle RMS voltage at point of common connection for different charging techniques

# 7.3 SML pulse generator control

## 7.3.1 Modeling, boundaries and scope

On one hand, modularized switched systems open additional degrees of freedom in control. As an example, different modulation schemes may be considered and, at least in principle, each pulse generation module may be controlled and - if desirable - switched in or out independently in producing an ideal output pulse waveform. On the other hand, it is at the same time desirable to secure good pulse quality operating with simple controllers that are applicable to a wide range of operating points and load conditions, and that are easily understood and tuneable in-field. With this latter requirement in mind, it is here considered that all pulse generator modules are to be controlled by a single reference waveform.

In addition to the above, it is also noted that - though evidently possible - simulating the complete modulator system in a circuit simulation tool is a relatively expensive computational task, requiring up to several minutes per pulse event. While this is feasible in, e.g., validating a modulator design, it is not suitable in optimizing controller design through iterative characterization of controller performance. Instead, it is desirable to find a suitable transfer function-based model largely retaining the accuracy of the complete system model in view of, e.g., pulse flatness, pulse rise time, and pulse overshoot. Hence, rather than modeling only the dynamic performance of the output stage, such a model must include the effects of the various types of voltage drops as well as capacitor bank droop. Consequently, for these purposes, the transfer functions given in (5.112)-(5.113) are no longer sufficient. Instead, considering first a single pulse generator module (i.e., comprised by a capacitor bank, an H-bridge power stack, a HVHF transformer, a HV rectifier and a HV filter; extension to the full modulator circuit is straightforward and is considered in Figure 7.30), the transfer function-based model depicted in Figure 7.23 is proposed. Here, $R(t)$ is the reference waveform (generated by the controller) taking values between 0 and 1 – essentially corresponding to the instantaneous effective H-bridge duty cycle – and $v_2(t)$ is the module output voltage waveform. In this formulation, $G_o(s)$ is the transfer function representation of the output stage as given in (5.112). Here, however, the input to $G_o(s)$ is formed by the effective average rectifier output voltage over time, i.e., $R(t)V_{cbk}(t)n - V_{drop}(i_2(t), t)$. The effective capacitor bank is modelled by the integrator $1/\big(s(C_m + C_n)\big)$ and has an initial voltage condition $V_1$. As may be seen, the integrator is fed a signal representing the required output current and the typically significant snubber losses. Further losses may similarly be straightforwardly included if desirable. The major voltage drops included in the below model in some way depend on the load current over time. Again, other sources of voltage drop may be added as needed.

Running both 1) the transfer function-based model shown in Figure 7.23 and 2) the corresponding complete circuit model for a set of constant reference waveforms yields the results shown in Figure 7.24. As can be seen, good static and dynamic model accuracy is obtained over a wide range of operation. This simplified model will be the main tool for evaluating controller performance in subsequent sections. In the following, design and optimization of PI-based controllers is treated.

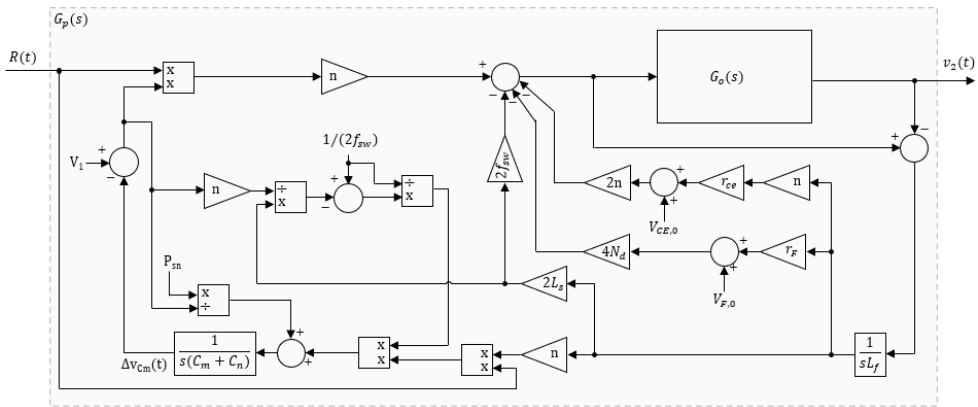



Figure 7.23: Transfer function-based model for single pulse generator module

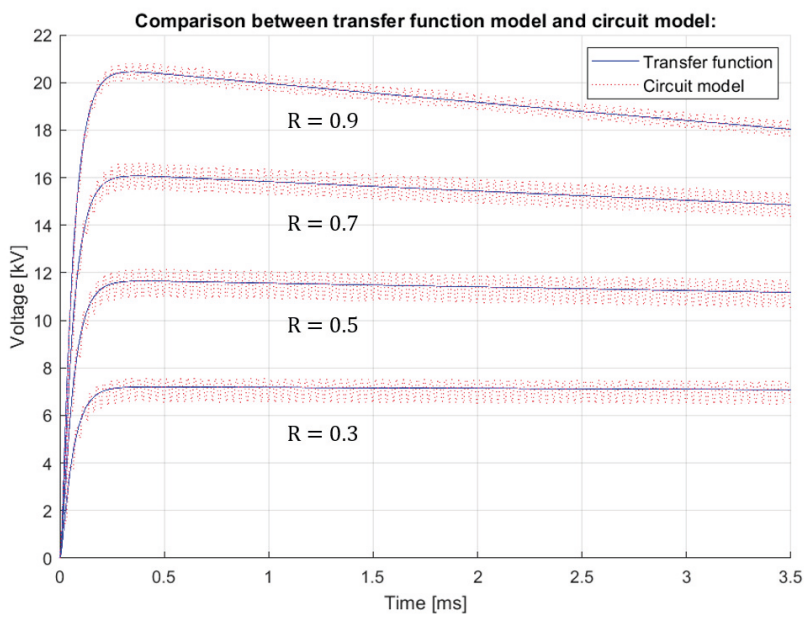



Figure 7.24: Comparison of output from transfer function-based model to output from complete circuit model

### 7.3.2 Pulse generation with traditional PI controller

The majority of industrial controllers in use today are based on some variation of the traditional PID control scheme, [7.4] and [7.8]. Such controllers are generally applicable, often offer more than satisfactory control performance, and may typically be straightforwardly tuned in-situ. While it was decided early on that an open loop control concept would be beneficial in operating the ESS klystron modulators, the traditional PI controller serves as a both important and instructive benchmarking tool. The adopted scheme is shown in Figure 7.25. The PI controller is characterized by the controller parameters $k_p$ and $k_i$. In addition, the damped filter branch current is here modelled (measured in practice) and included in an inner feedback loop with gain $k_c$ to add electronic damping, representing a two-degrees-of-freedom controller [7.4]. Again, the controlled parameter is the instantaneous effective H-bridge duty cycle represented by $R(t)$. In the following, selection and optimization of the controller parameters $k_p$, $k_i$ and $k_c$ in view of a single pulse generator system will be treated. Then, extension to the full modulator circuit is considered. As the PI controller is well known and is mainly intended to serve as a benchmarking tool, presentation is kept brief.

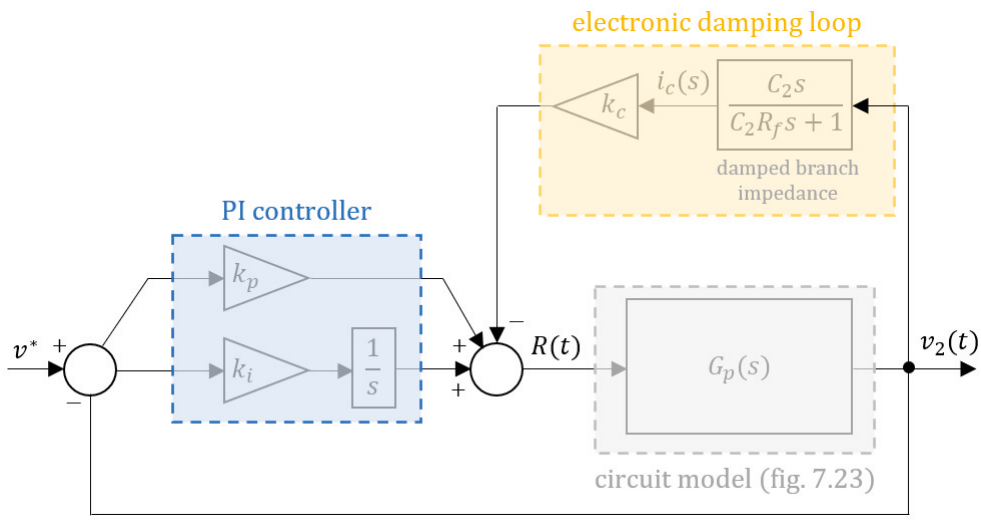



Figure 7.25: Simplified model with PI controller and inner electronic damping feedback loop

*Design of PI controller for single pulse generator module*

Despite the fact that the complete model described in Figure 7.23 is required to accurately evaluate controller performance, it should be recognized that the basic dynamics of the total plant model is still greatly governed by $G_o(s)$. Hence, to begin to find an appropriate set of controller parameters, the Bode diagram of 1) the open

loop system $G_o(s)$, 2) the open loop system $G_o(s)$ with electronic damping, and 3) the closed loop system for some set of controller parameters $\langle k_p, k_i, k_c \rangle$ may be plotted. From this, $k_c$ is first chosen to appropriately damp the resonance frequency of the open loop system $G_o(s)$. Then, $k_p$ and $k_i$ are varied to provide a suitable compromise between damping and dynamic response. As an example, the closed loop system given in Figure 7.25 is simulated using the transfer function-based model described in Figure 7.23. Here, a pulse rise time of ~160 µs and a slight pulse overshoot is featured.

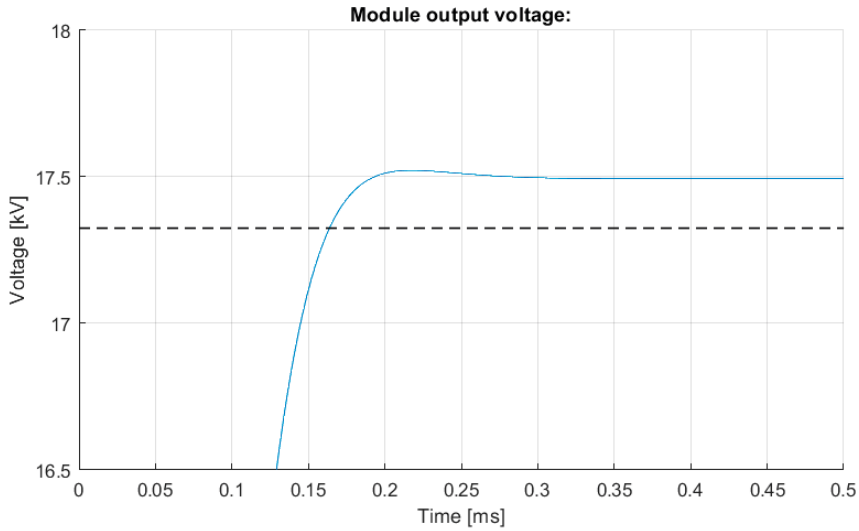



Figure 7.26: Basic pulse performance for PI controller designed using Bode diagram approach

Though unlikely to be optimal, the derived controller parameters serve as a suitable starting point for optimization. Here, given the relative simplicity of the developed plant model, Figure 7.23, a computational (iterative) optimization method (e.g., that developed in [7.8]) is appropriate. As the integral action of the proposed controller most likely will be able to correct for the relatively slow dynamics presented by capacitor bank voltage droop, these effects may be neglected in optimization, instead focusing on the typical trade-off between pulse rise time and pulse overshoot.

Figure 7.27 shows optimization results obtained from a variation of the method described in [7.8], searching around the above-described starting point, as applied to the systems described in Figure 7.23 and Figure 7.25. Imposing, e.g., a limit of ~125 µs on pulse rise time and a 1% limit on pulse overshoot allows straightforward selection of an appropriate controller design. As an example, three controller designs close to the Pareto front have been selected and are evaluated in comparison

to the earlier derived and studied controller in Figure 7.28. As can be seen, the obtained controller designs feature similar pulse overshoot and pulse settling time, and much reduced pulse rise time.

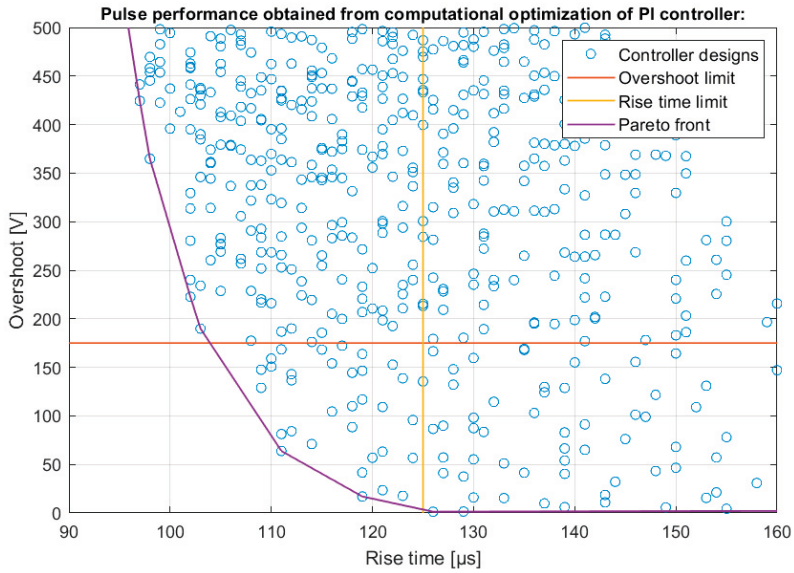



Figure 7.27: Performance of PI controller designs derived from computational optimization procedure as applied to single modulator pulse generator circuit

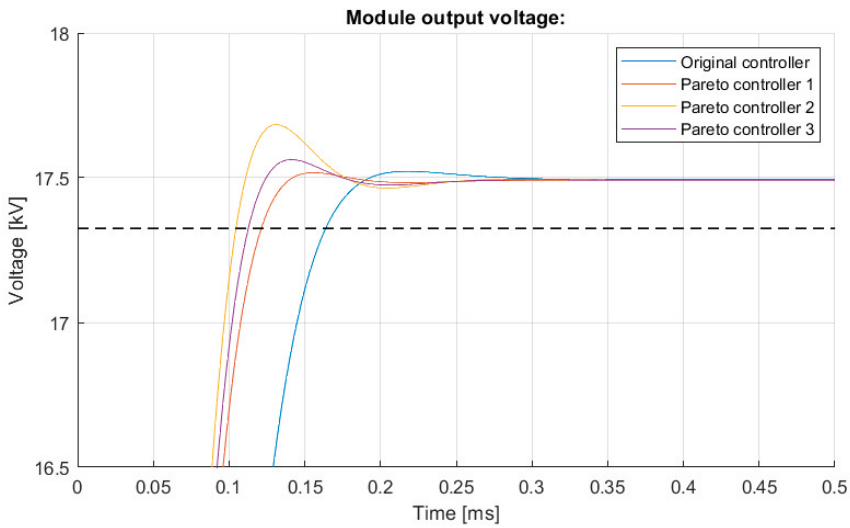



Figure 7.28: Pulse quality for a selection of optimized controller designs in comparison with original controller design derived from Bode diagrams

In this case, the controller termed ‘Pareto controller 1’ seems appropriate, and is characterized in circuit simulation, Figure 7.29. Again, note the agreement between the simplified transfer function-based model and the circuit model. It is emphasized that the developed controller and associated system represent pulse performance well in line with ESS klystron modulator requirements.

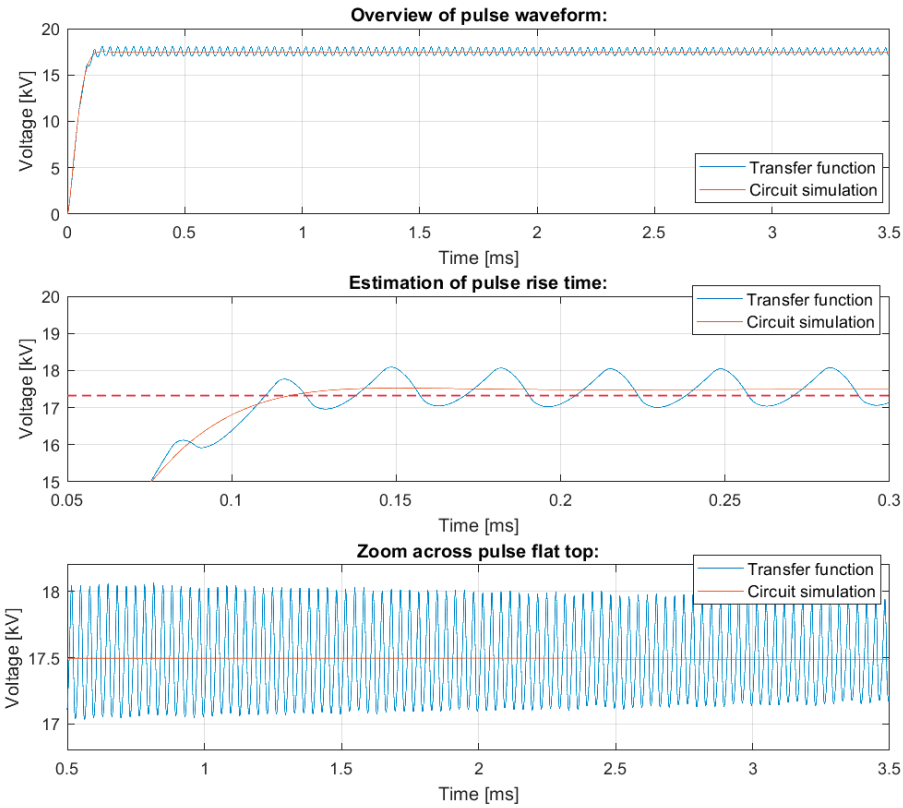



Figure 7.29: Circuit simulation of pulse generator module controlled by optimized PI controller

*Design of PI controller for complete modulator output stage*

It is now of interest to apply the developed optimization procedure to the full modulator output stage circuit, i.e., including $N_p$ pulse generator modules. To accomplish this, the model presented in Figure 7.23 may for these purposes be extended as indicated in Figure 7.30. Of course, this is due to the fact that the model described in Figure 7.23 generates a time-average of the output voltage waveform. Considering that a single reference waveform controls all modules, the time-average output of all modules is identical, justifying the extended model of Figure 7.30.

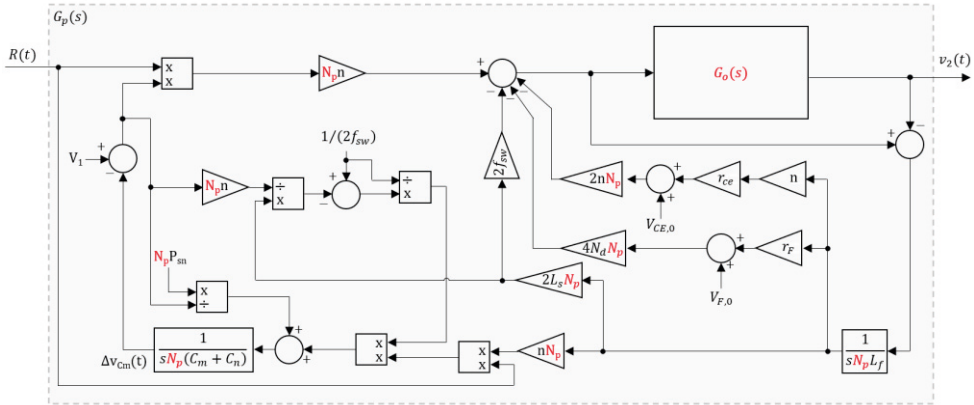



Figure 7.30: Extension of transfer function-based model to complete modulator output stage

Clearly, then, the above developed computational optimization procedure may immediately be applied. Optimized pulse performance is studied in comparison to that generated by the equivalent open loop controller in section 7.3.4.

### 7.3.3 Optimized pulse generation with open loop controller

It was determined in the preceding section that the performance of the developed PI controller is satisfactory from the perspective of ESS application requirements. Still, as mentioned, for reasons related to mainly pulse-to-pulse repeatability it was decided early on to adopt an open loop controller concept[2]. Naturally, the performance should at least match that associated with the conventional PI controller scheme. Furthermore, the controller must be applicable over the whole operational range of the modulator circuit, and should be easy to understand and tune in-situ. These requirements suggest defining the reference waveform as a piecewise linear (PWL) function. Here, the number and defining values of the PWL breakpoints must somehow appropriately be defined in generating the desired pulse waveform. While it is possible to optimize such a waveform completely from scratch, this is inconvenient, especially considering a large number of operating points and varying load conditions. Instead, the following section proposes a method to accurately estimate a prototype reference waveform that may then be used in optimizing the PWL breakpoints.

[2] It is noted that, in practice, a slow pulse-to-pulse correction mechanism was also implemented. In this method, the pulse amplitude is sampled in the middle of the pulse flat top duration and compared to the reference amplitude. Here, a slow PI controller offsets the defined PWL function (described below) in ensuring stable pulse performance despite thermal drifts, aging effects, and so on. This method is straightforward and not discussed in detail in this thesis. Pulse-to-pulse reproducibility of the developed modulator is assessed experimentally in sections 9.6.1 and 9.6.4.

*Generation of prototype reference waveform*

The basic problem discussed in the above is demonstrated in Figure 7.31. The question is, 'what should $R(s)$ be in order to produce a desirable output waveform $v_2(t) = L^1(V_2(s))$?'. In principle, the required $R(s)$ can be calculated directly from $R(s) = V_2(s)/G_p(s)$. Unfortunately, it is not immediately obvious what $V_2(s)$ is or should be. Still, a suitable $V_2(s)$ may be calculated from the system shown in Figure 7.31.b, i.e., $V_2(s) = \Theta(s)G_2(s)$. Based on the presented modeling work, $G_2(s)$ may appropriately be set to be a second order system. Then, $G_2(s)$ may be tuned to yield $V_2(s)$, e.g., corresponding to that generated by the corresponding PI controller, Figure 7.32.

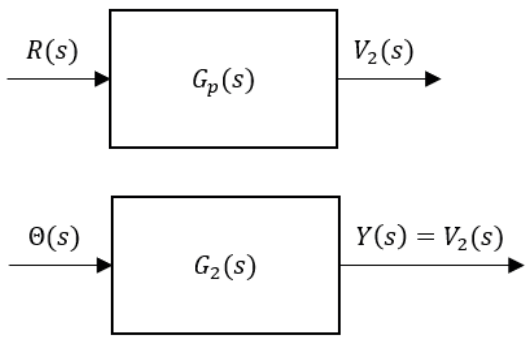



Figure 7.31: Calculation of the reference waveform

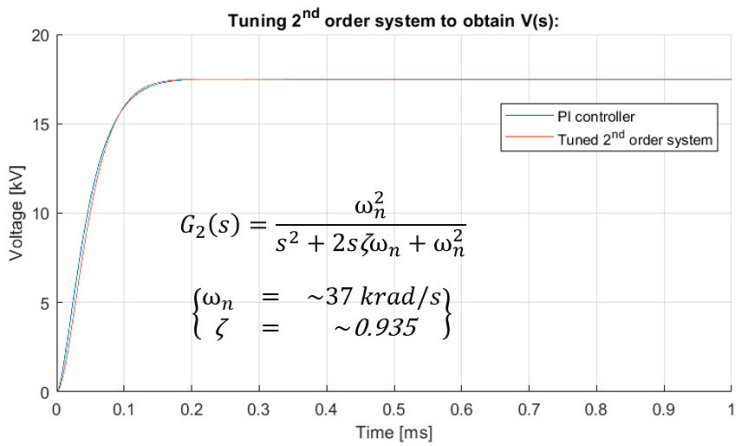



Figure 7.32: Example of tuning the second order system $G_2(s)$ in calculating an appropriate reference waveform

Then, in keeping with the above, the reference waveform is given by (7.9), where $\langle G_p(s) \rangle$ is an estimation of the plant transfer function. However, as mentioned, it is

desirable to obtain a controller that is easily tuneable, preferably with only 2 parameters to be comparable to that of the above developed PI controller. Hence, instead of adjusting each parameter in $\langle G_p(s) \rangle$, two tuning constants $k_{vd}$ and $k_{Cm}$ are introduced. In this formulation, $k_{vd}$ is used to account for inaccuracies in voltage drop modeling, and $k_{Cm}$ is used to account for inaccuracies in capacitor bank voltage droop modeling. This both 1) significantly simplifies the practical process of tuning the controller, and 2) makes the process physically accessible. The process of calculating $R(s)$ is summarized in Figure 7.33.

$$R(s) = \frac{V_2(s)}{\langle G_p(s) \rangle} = \Theta(s) \frac{G_2(s)}{\langle G_p(s) \rangle} \tag{7.9}$$

Simulation results derived using the proposed procedure are shown in Figure 7.34 and Figure 7.35. First, Figure 7.34 shows the calculated reference waveform and the associated module output voltage waveform for both the transfer function-based model described in Figure 7.23 as well as for the complete circuit simulation model. Expectedly, given the tuning of $G_2(s)$ performed in Figure 7.32, controller performance is extremely similar to that shown for the corresponding PI controller. Then, Figure 7.35 shows the results of the procedure as applied to a number of voltage references. As can be seen, the proposed open loop controller produces a satisfactory result in all of these cases.

Of course, as it stands, the calculated reference waveform is given directly by the procedure shown in Figure 7.33. However, as mentioned, it is desirable to practically base the open loop controller on PWL-type functions. The prototype reference waveform calculated by Figure 7.33 and exemplified in Figure 7.34 and Figure 7.35 will now be used as basis for optimizing the required PWL function. Note from Figure 7.35 that the calculated reference waveform has a clearly identifiable pattern, such that it may be divided into three ‘zones’, Figure 7.36. In zone I, the reference waveform is strictly and quickly increasing. In zone II, the reference waveform is strictly decreasing. Finally, in zone III, the reference waveform is again strictly increasing, though significantly slower than that seen in zone I.

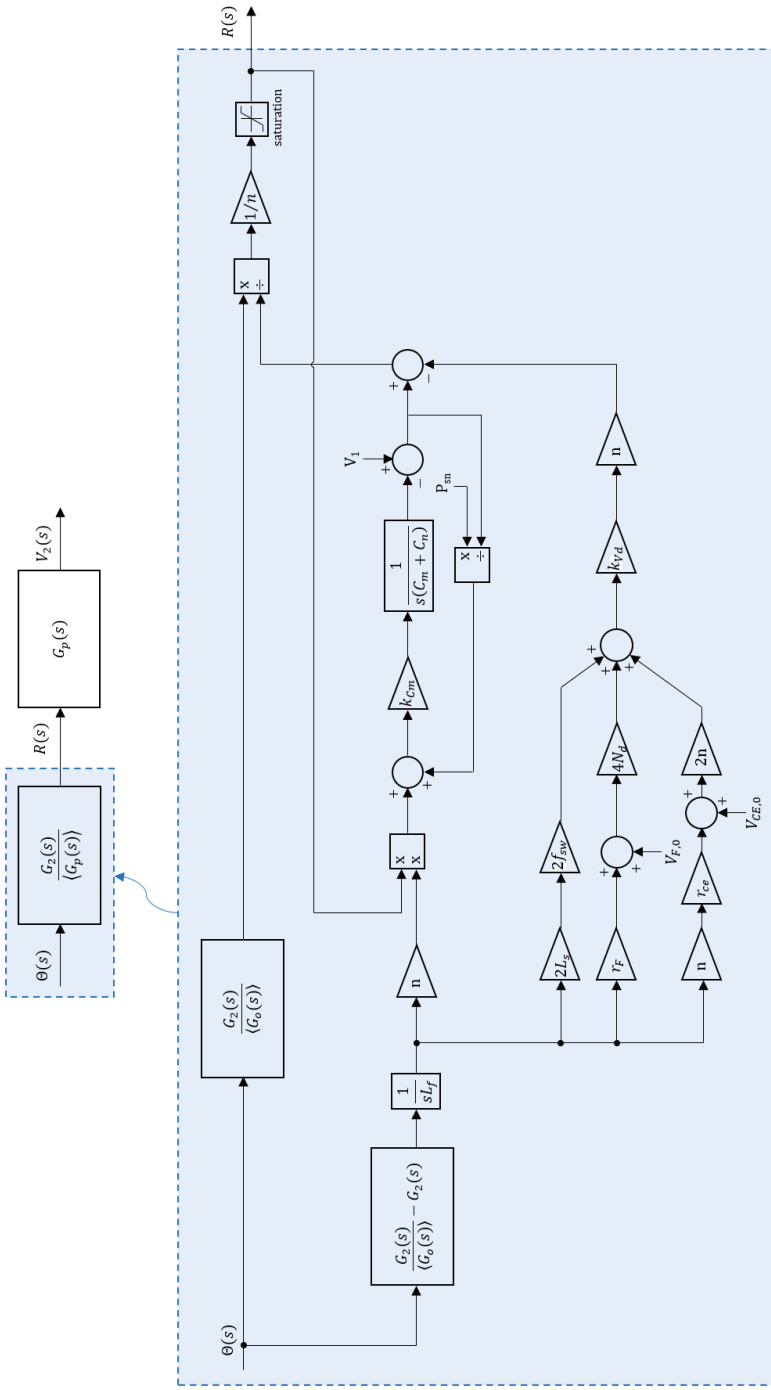



Figure 7.33: Procedure for calculating the required $R(s)$ producing the desired $V_2(s) = \Theta(s)G_2(s)$ for some plant $G_p(s)$

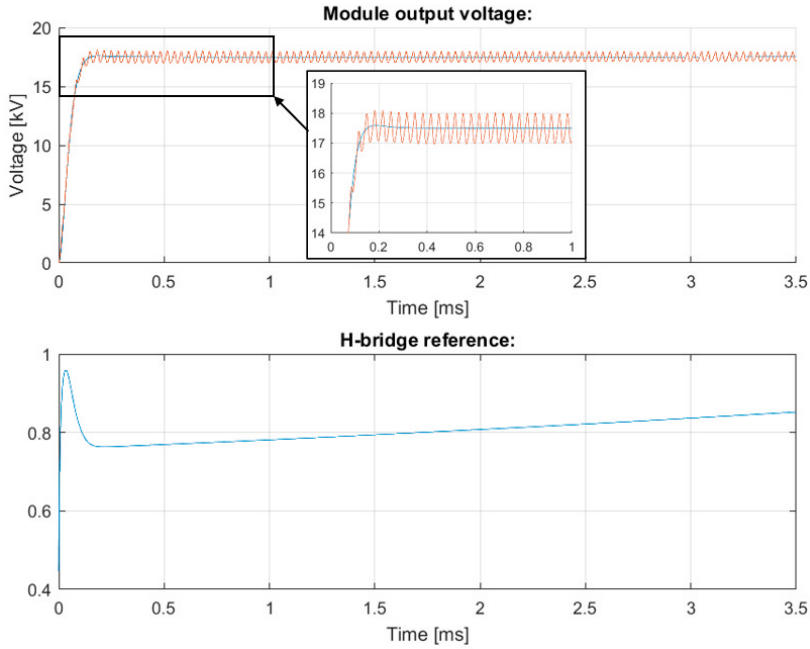



Figure 7.34: Calculated reference waveform and associated pulse generator module output voltage

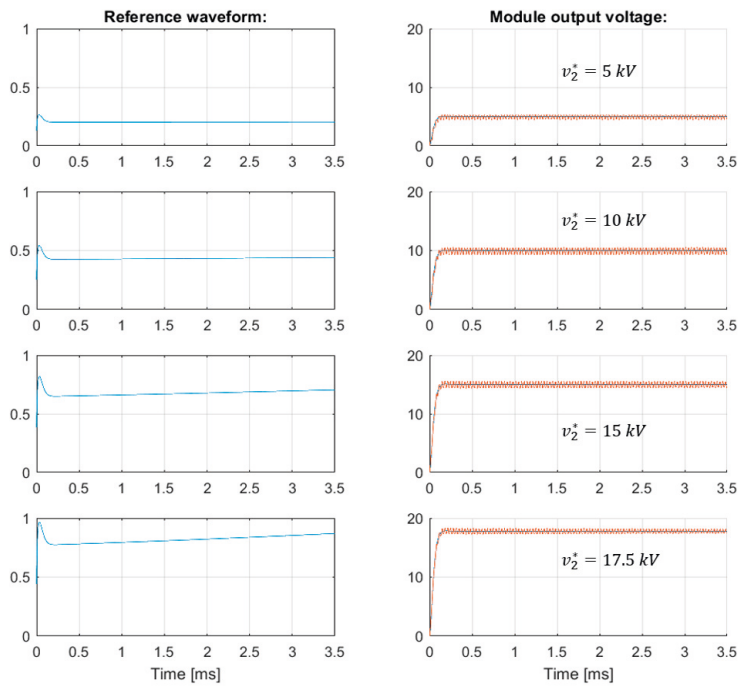



Figure 7.35: Calculated reference waveform for a set of desired module output voltages

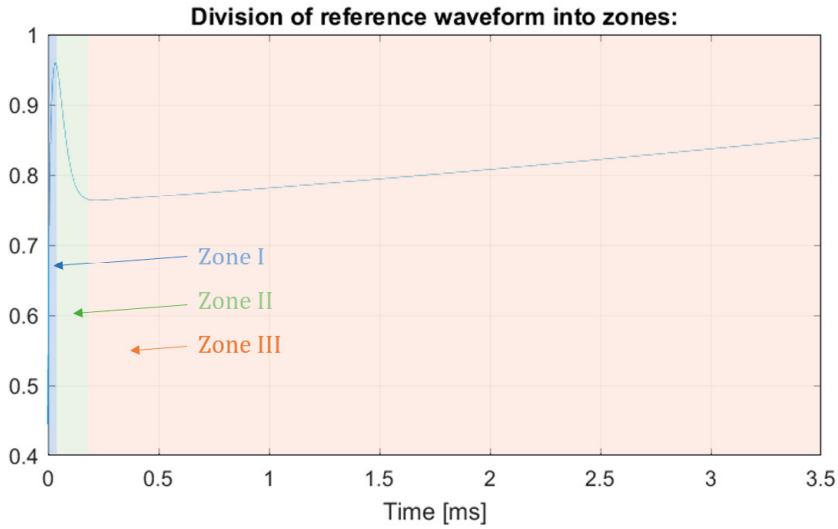



Figure 7.36: Division of calculated reference waveform into zones to facilitate generation of corresponding piecewise linear function

A suitable PWL reference waveform may now be constructed from Figure 7.36 by considering $N_{s,1}$ segments for zone I, $N_{s,2}$ segments for zone II, and $N_{s,3}$ segments for zone III. Clearly, for $N$ segments, $N + 1$ breakpoints are required. Hence, $N_{s,1} + N_{s,2} + N_{s,3}$ should be reduced as much as possible in developing a practically tuneable controller. Note here that it is possible (in reducing problem complexity) to assume that the starting point, the end point, and all points interconnecting the zones to be known from the calculated reference waveform. The required breakpoints are then to be appropriately distributed. In this work, the required breakpoints per zone have been linearly distributed over the period defined by the zone (this choice is discussed in the later section on future work). Then, the function values of the breakpoints are optimized by least square fitting such that the difference between the calculated reference waveform and the chosen PWL function is minimized.

In the following, the impact of different choices of $N_{s,1}$, $N_{s,2}$ and $N_{s,3}$ on pulse quality is studied using the described method. The explanation is given using Figure 7.37 as a starting point. In this case, $N_{s,1} = 2$, $N_{s,2} = 3$ and $N_{s,3} = 3$ for a total of 8 segments. In accordance with the above, this selection requires the addition of a minimum of 5 unknown breakpoints to fully define the complete PWL function. Also, in Figure 7.37, note the general agreement and correspondence in module output voltage waveform in applying the ideal and the PWL function-based waveforms.

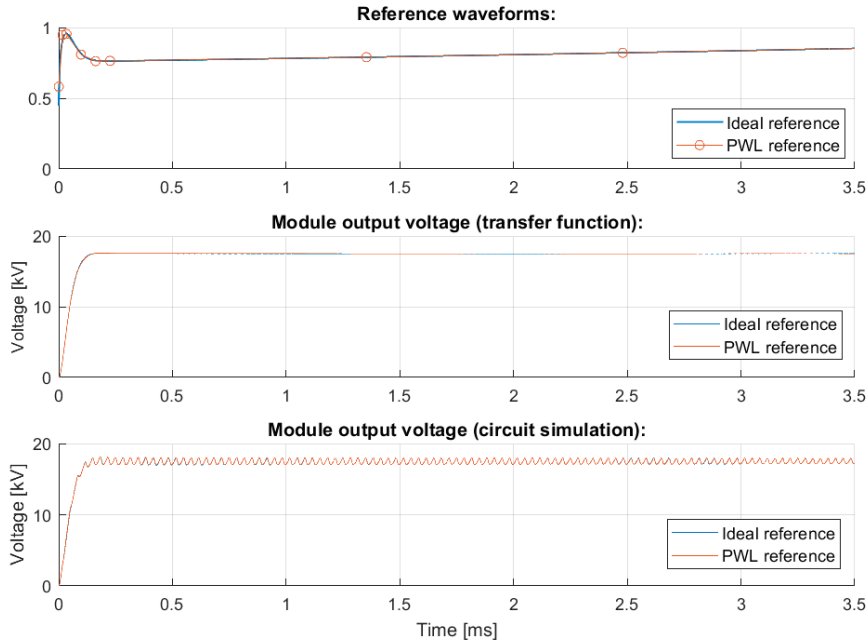



Figure 7.37: Simulated module output voltage waveform (transfer function-based model and circuit simulation) for calculated reference waveform and PWL function-based reference waveform

Based on the above, Figure 7.38 presents a study on the impact of the number of PWL segments for the different zones described in Figure 7.36. Conceivably, zone I is related mostly to pulse overshoot and pulse rise time, Figure 7.38.a. Here, using only a single segment results in a too aggressive pulse rise corresponding to a somewhat excessive pulse overshoot. On the other hand, with two or more segments, the pulse waveform corresponds very well to the waveform generated by use of the ideally calculated reference waveform. For this reason, $N_{s,1} = 2$ in minimizing the number of segments. Similarly, $N_{s,2} = 3$ in obtaining a reasonably well-matched pulse settling time. Finally, for zone III, the number of segments directly corresponds to the number of times the reference waveform slope is changed during the flat top. Thereby, this corresponds to the addition of a form of flat top droop generated in adjusting the waveform for the generated capacitor bank voltage droop. This effect, however, is appropriately limited by selection of $N_{s,3} = 3$.

With this selection, the system with the open loop controller defined by $N_{s,1} = 2$, $N_{s,2} = 3$ and $N_{s,3} = 3$ is again simulated, Figure 7.39. Particularly note 1) the agreement between the pulse waveforms generated by the calculated and PWL function-based reference waveforms, and 2) the agreement to the controller performance displayed by the optimized PI controller.

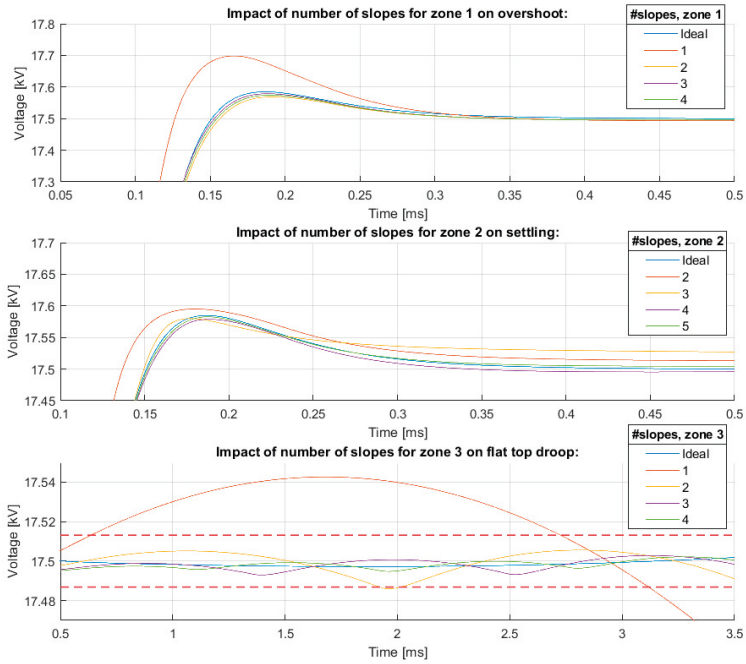



Figure 7.38: Study on the impact of the number of PWL function segments on output pulse waveform quality

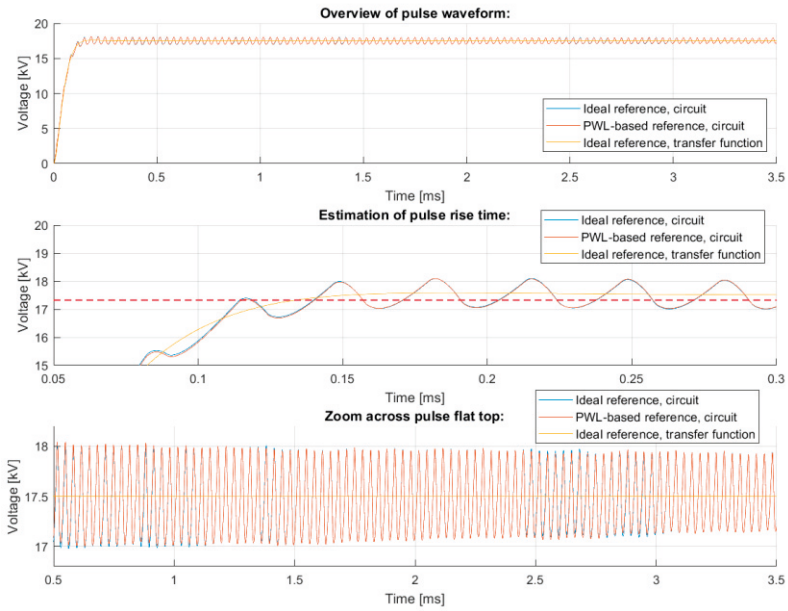



Figure 7.39: Comparison and assessment of pulse quality for calculated and PWL function-based reference waveforms

### 7.3.4 Summary and comparison of methods

This section has developed two methods for controlling the SML output stage modules. Output pulse waveform quality generated in operating a single output module was shown, particularly, in Figure 7.29 and Figure 7.34 and is shown in comparison in Figure 7.39. Extending the developed transfer function-based model in accordance with that discussed in relation to Figure 7.30, the proposed methods may straightforwardly be applied in controlling the entire SML output stage. A comparison for this scenario is shown in Figure 7.41.

Figure 7.40 and Figure 7.41 demonstrate that use of both controllers generates high quality output pulse waveforms in accordance with that required of the ESS klystron modulator systems. An appropriate PI controller design may be found using the methodology described in section 7.3.2. As usual, the chosen controller may then straightforwardly be tuned in-situ. Still, an open loop controller was desirable in promoting pulse-to-pulse repeatability. As demonstrated, the developed open loop controller matches the performance of that of the PI controller. In practice, the proposed controller is easy-to-use, and may be tuned as described in section 7.3.3 using either 1) the two controller parameters, or 2) by directly updating the resulting intuitive PWL breakpoints. Additionally, as will be discussed in chapter 9, an automatic tuning procedure operating directly on the PWL breakpoints has been implemented and validated in optimizing the pulse waveform.

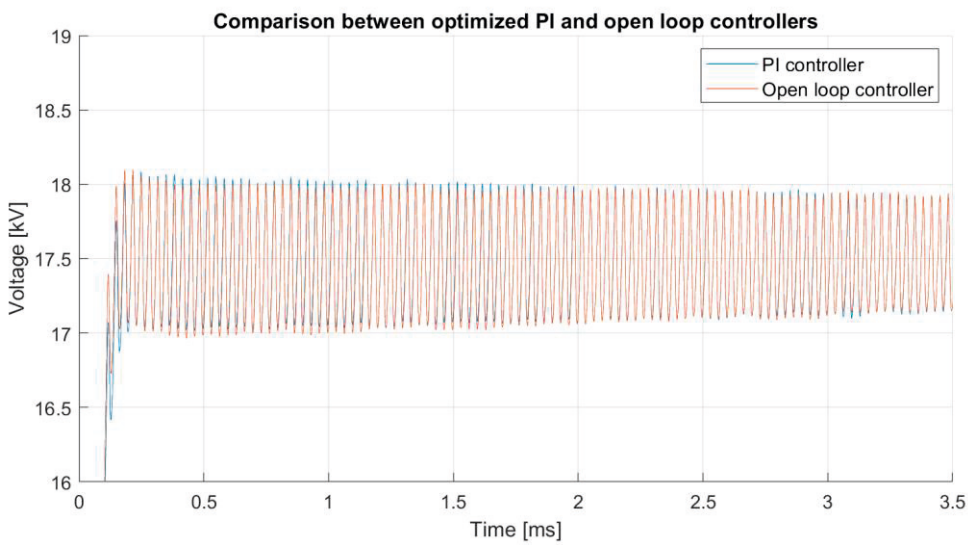



Figure 7.40: Comparison of pulse waveforms for single module system operated by PI and open loop controllers

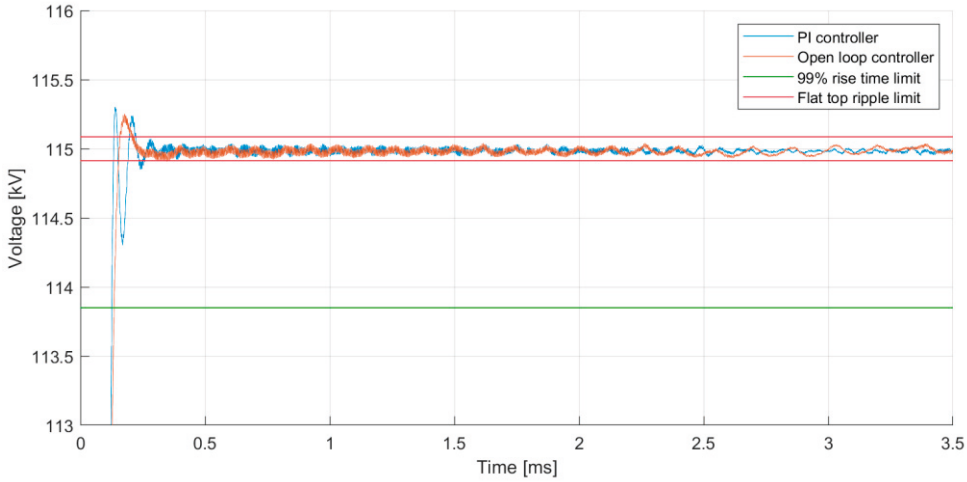



Figure 7.41: Comparison of pulse waveforms for complete modulator system operated by PI and open loop controllers

### 7.3.5 Future work

There are several interesting opportunities in expanding the work discussed in this chapter-

- As described in section 7.3.1, the developed methods are explicitly based on the assumption that all output stage modules are operated using the same reference waveform. Though this choice is – for many reasons – practically justifiable, it is not inconceivable to consider operation with independent reference waveforms. Such a controller (or set of controllers) could enhance dynamic performance, particularly in improving and optimizing the compromise between pulse rise time, pulse overshoot and pulse settling time. Analysis and design of such a controller would require a significantly more detailed model than that shown in Figure 7.23. In particular, the corresponding open loop controller(s) would be significantly more complex to tune in generating an optimal output stage pulse waveform.
- In section 7.3.3, the PWL function was constructed by linearly distributing the PWL breakpoints across each of the identified zones. Using an optimized time distribution, improved performance for the same number of breakpoints should be possible. Conversely, it could be possible to obtain the same performance as that shown in the above for a reduced number of breakpoints, simplifying the controller.

- The open loop controller developed in section 7.3.3 was designed to match the performance of the benchmark PI controller. It is clearly of interest to consider other functions $G_2(s)$ in optimizing controller performance.

## 7.4 Generation of alternating pulsing schemes

So far in this thesis – and this is the overwhelmingly most common, if not the only, mode of operation – it has been assumed that, in steady state, the power modulators are set to deliver pulses at a single modulator operating point, i.e., a single combination of pulse amplitude, pulse length and pulse repetition rate. However, given the inherent flexibility and controllability of the SML modulators, it is possible to generate 'alternating pulsing schemes'. For such schemes, pulse trains in which each pulse may vary (though repeatedly) in terms of amplitude, pulse length and frequency are to be generated. This type of pulse generation scheme may be required in accelerators used in serving several end purposes. One such example is the proposed European Spallation Source Neutrino Superbeam (ESSnuSB) project, [7.9]-[7.15], entailing a linac upgrade in interleaving the baseline proton pulses used for spallation neutron production with additional $H^-$ ion pulses to be used in producing a high intensity neutrino beam. At the time of writing, several such interleaved pulsing schemes (here denoted A, A2, B and C) are under consideration for the ESSnuSB, Figure 7.42. This section evaluates the possibility to exploit the flexibility of the SML modulators in facilitating the required linac upgrade.

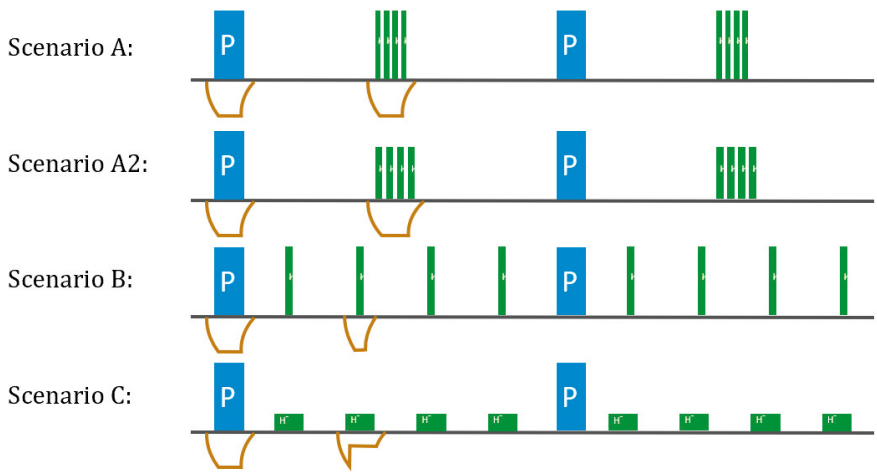



Figure 7.42: Sample alternating pulsing schemes proposed in for the ESSnuSB project

### 7.4.1 Study of pulse quality over modulator range of operation

To verify the feasibility of utilizing an upgraded version of the developed SML klystron modulators, it is necessary to perform a detailed study of modulator pulse quality over the entire practical range of operation. This is because, whereas some of the interleaved pulsing schemes proposed in Figure 7.42 indicate adding pulses of the same amplitude as that produced in nominal modulator operation, two of the pulsing schemes require operation at lowered modulator output voltage. While, e.g., Figure 7.24 and Figure 7.35 indicate that the pulse rise time and pulse overshoot may indeed be maintained over the entire range of operation, flat top ripple is a direct function of 1) the H-bridge duty cycle, i.e., the instantaneous value of the reference waveform, and 2) the number of pulse generation modules.

In, e.g., section 4.3 and section 5.3.6, flat top ripple was conservatively managed in design by limiting the worst-case flat top ripple at the nominal operating point. Here, the worst-case ripple over the operating range of the modulator is investigated by simulating the complete modulator model utilizing the controllers developed in the preceding section to output pulse voltages from ~50 kV up to the nominal 115 kV, Figure 7.43. In accordance with the above, the simulated peak-to-peak flat top ripple is a strong function of the requested flat top voltage. Of course, for comparatively low flat top voltages, the relative peak-to-peak flat top ripple increases and, around ~65 kV, exceeds the imposed limit. Still, practical operation at such low voltages is likely inconceivable given the dramatic associated decrease in klystron efficiency. Nevertheless, should 1) such an operating point be required in implementing a given pulsing scheme and should 2) the imposed nominal flat top ripple requirement be directly applicable to also lower voltage amplitudes, the generated flat top ripple may promptly be improved by slightly increasing the H-bridge switching frequency (the added losses are comfortably managed given the reduced output power).

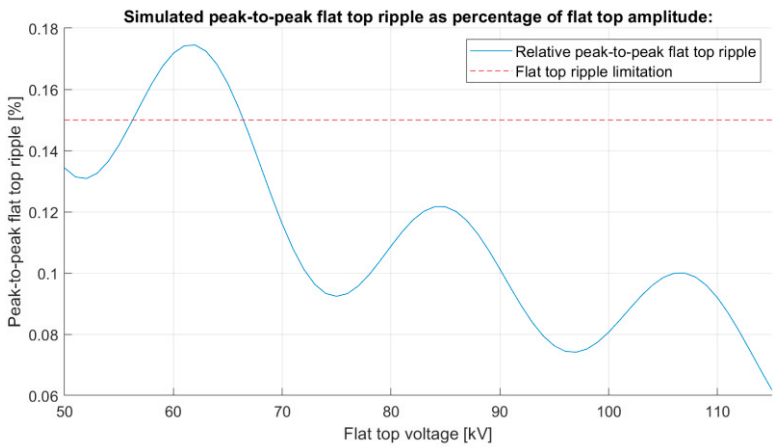



Figure 7.43: Simulated peak-to-peak flat top ripple (curve fit) as percentage of the flat top amplitude

### 7.4.2 Framework for evaluating alternating pulsing schemes

The study presented in section 7.4.1 demonstrates the technical feasibility to utilize an upgraded version (i.e., in handling the increased average power) of the developed SML modulators in producing interleaved, alternating pulsing schemes such as those described by Figure 7.42. At this point, it is interesting to develop a generalized framework to evaluate such schemes from the perspective of operating the power modulators and associated klystrons.

To begin, Figure 7.44 shows the power transfer curves with the applied cathode voltage as parameter for the adopted 704 MHz klystrons. Here, the nominal operating point is denoted $O_1$. For this operating point, the output energy per pulse, assuming a pulse beam time $T_{p,1}$, may be written according to (7.10). Importantly, this operating point was selected in a compromise between klystron efficiency and dynamic gain as required for LLRF (low-level RF) controllability. In considering the pulsing schemes of, e.g., Figure 7.42, similar operating points have to be selected. In this work, it is assumed that a set of added pulses for some operating point $O_x$ should 1) represent similar dynamic gain to be comparable in terms of LLRF controllability, and 2) represent the same total output RF energy, (7.11)-(7.12). These assumptions are practical but not necessary.

To find potential operating points in constructing viable pulsing schemes in accordance with the above, the klystron power transfer curves shown in Figure 7.44 were curve fitted. From this, the point on each transfer curve representing identical dynamic gain may straightforwardly be found, Figure 7.45. Clearly, any point along the identified line may be used in forming an equivalent pulsing scheme through combining 1) the number of added pulses, and 2) the pulse length for each of the added pulses. Under the assumption that the added set of pulses are identical to one another (though not necessarily to the baseline proton pulse), (7.13) is obtained.

$$E_p(O_1) = P_{RF}(O_1)T_{p,1} \tag{7.10}$$

$$E_p(O_1) = E_p(O_x) \tag{7.11}$$

$$P_{RF}(O_1)T_{p,1} = P_{RF}(O_{x1})T_{p,x1} + P_{RF}(O_{x2})T_{p,x2} + \cdots \tag{7.12}$$

$$O_{x1} = O_{x2} = \cdots ; T_{p,x1} = T_{p,x2} = \cdots \rightarrow P_{RF}(O_1)T_{p,1} = P_{RF}(O_x)N_p \tag{7.13}$$

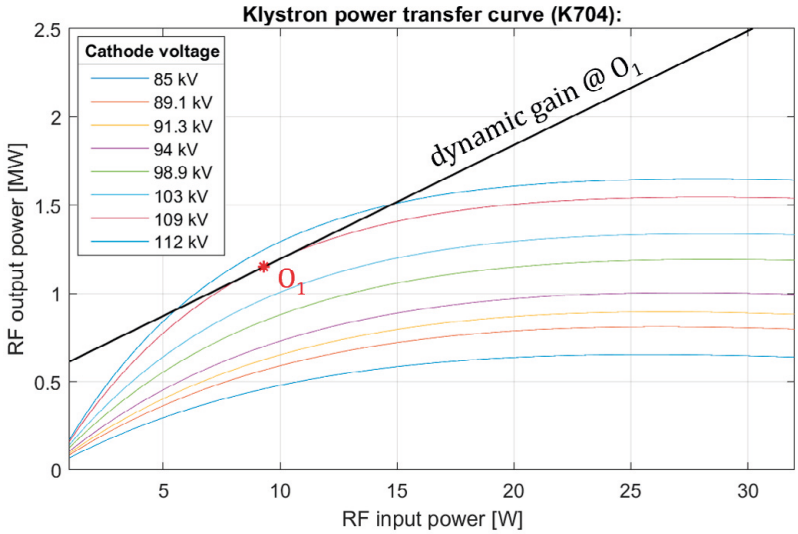



Figure 7.44: Klystron power transfer curves from datasheet of the adopted 704 MHz klystron

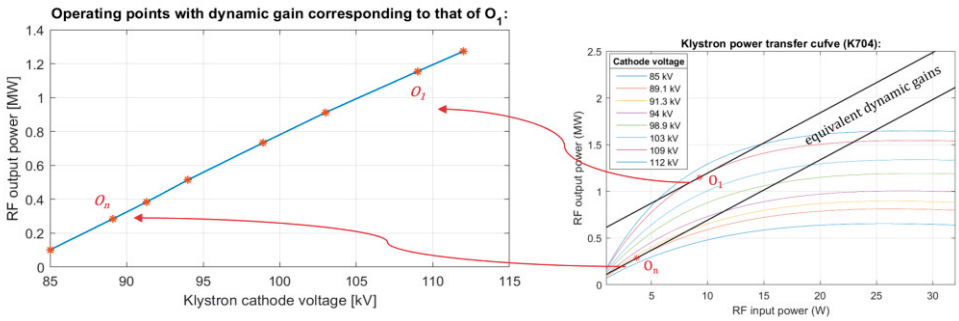



Figure 7.45: Identification of operating points with dynamic gain matching that of the nominal operating point

Whereas (7.12) establishes that the schemes shown in Figure 7.42 are identical in terms of output RF energy, they are clearly not identical from the perspective of the modulator input. This is because 1) as explained in chapter 2, useful RF power is output only during the pulse beam time $T_p$, but to output each pulse, the modulator expends energy in going through the pulse rise time, the pulse stabilization time and the RF cavity filling time; and 2) as klystron efficiency is a strong function of the applied cathode voltage, (7.14)-(7.15).

$$E_1 = P_k\big(V_k(O_1)\big)\big(T_{p,1} + K_1 t_{r,1} + t_s + t_c\big) \tag{7.14}$$

$$E_x = P_k\big(V_k(O_x)\big)\big(T_{p,x} + K_x t_{r,x} + t_s + t_c\big) \tag{7.15}$$

In summary, the average useful output power of the modulator, i.e., the average output RF power, may be written according to (7.16). The corresponding modulator input power may be written according to (7.17). The ratio between these quantities is given in (7.18), and is termed the 'grid-to-RF' efficiency. Clearly, in considering interleaved pulsing schemes, the effective modulator efficiency depends strongly on the number of added pulses as well as the chosen operating point.

$$\bar{P}_{RF} = f_r N_k \left[ P_{RF}(O_1) T_{p,1} + P_{RF}(O_x) T_{p,x} N_p \right] \tag{7.16}$$

$$\bar{P}_{mod} = f_r N_k \left( \frac{E_1}{\eta_{m,1}} + \frac{N_p E_x}{\eta_{m,2}} \right) \cong \frac{f_r N_k}{\eta_m} \left( E_1 + N_p E_x \right) \tag{7.17}$$

$$\eta_{g-rf} = \frac{\bar{P}_{RF}}{\bar{P}_{mod}} = \eta_m \frac{P_{RF}(O_1) T_{p,1} + P_{RF}(O_x) T_{p,x} N_p}{E_1 + N_p E_x} \tag{7.18}$$

### 7.4.3 Case study: European Spallation Source Neutrino Superbeam

In the baseline ESS design, the linac will accelerate protons to the energy of 2 GeV in 2.86 ms, 62.5 mA pulses repeated at 14 Hz; to be used for spallation neutron production. It has been pointed out that the low duty cycle, only around 4%, of the baseline design could be extended in allowing acceleration of additional pulses. The ESSnuSB project is one such proposal, in which the baseline proton pulses would be interleaved with additional $H^-$ ion pulses to be used in producing a high intensity neutrino beam. This proposal aims to make full use of the linac, i.e., requiring significant upgrades in delivering twice the output power, and requires the addition of an accumulator ring and additional target stations, Figure 7.46.


Figure 7.46: Overview of the proposed ESSnuSB project

Whereas the ESS utilizes a rotating target wheel to handle the average power of the beam, the ESSnuSB plans to divide the equivalent average power between four stationary target stations. For this reason, four pulses are required. As indicated in Figure 7.42, this can be accomplished either by generating a single modulator pulse, chopping it into four smaller pulses, or by simply generating four smaller modulator pulses. On the one hand, as is evident from (7.16)-(7.18), generation of a single modulator pulse would be beneficial from the perspective of grid-to-RF efficiency. On the other hand, this type of operation would require a significant and costly re-design of the already existing magnetic horn power supply. However, generation of four smaller pulses, as mentioned, significantly degrades the grid-to-RF efficiency, and furthermore requires a significant upgrade of the cryogenics distribution system. Finally, the selection of pulse amplitude and pulse length of the added pulses is of importance. Operation at nominal amplitude is complicated due to the added effect of $H^-$ ion stripping, resulting in beam loss. On the other hand, lowering the amplitude requires a longer pulse length in conserving the output RF energy. Here, the longer pulse length is problematic from the perspective of the accumulator ring as the longer ring filling time potentially may lead to ring instabilities.

With the above considerations in mind, (7.17) and (7.18) are evaluated for the outlined conditions of the ESSnuSB project. The resulting grid-to-RF efficiency is presented in Figure 7.47, and the corresponding modulator input power is shown in Figure 7.48. As can be seen, the grid-to-RF efficiency is degraded in proportion to the number of added pulses. This is expected, as in delivering the same amount of output RF energy, $N_p - 1$ additional pulse initialization periods are required. Note in particular the significant reduction in grid-to-RF efficiency between pulsing schemes A and B.

Pulsing scheme C, then, corresponds to even worse grid-to-RF efficiency in representing 1) four additional pulse events, and 2) operation at a significantly reduced klystron cathode voltage. Here, the grid-to-RF efficiency has degraded from 41.5% in the baseline case (scenario A) to only 27.7%.

A complete comparison of the pulsing schemes is given in

Table 7.1. This comparison was presented in [7.13]-[7.15], and provided the grounds for rejecting pulsing schemes B and C. In particular, pulsing scheme A2 has emerged as an interesting version of the baseline scenario in representing only slightly decreased grid-to-RF efficiency (due to the lowered klystron cathode voltage) but significant reductions in $H^-$ ion stripping, corresponding to greatly improved system performance. In addition to the material presented in [7.13], a complete assessment of the impact on the developed modulator circuits in terms of cost, size, required upgrade time, etc., was presented in [7.14]-[7.15].

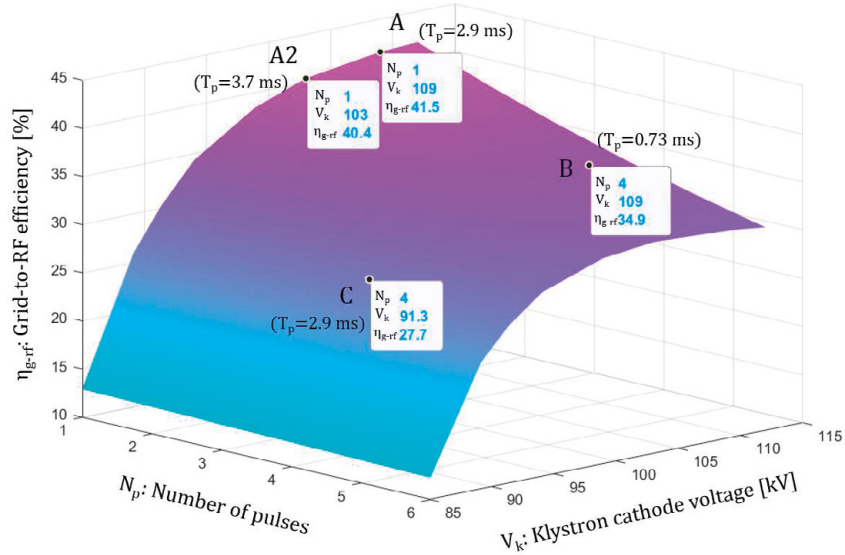



Figure 7.47: Grid-to-RF efficiency in considering interleaved pulsing schemes for the ESSnuSB project

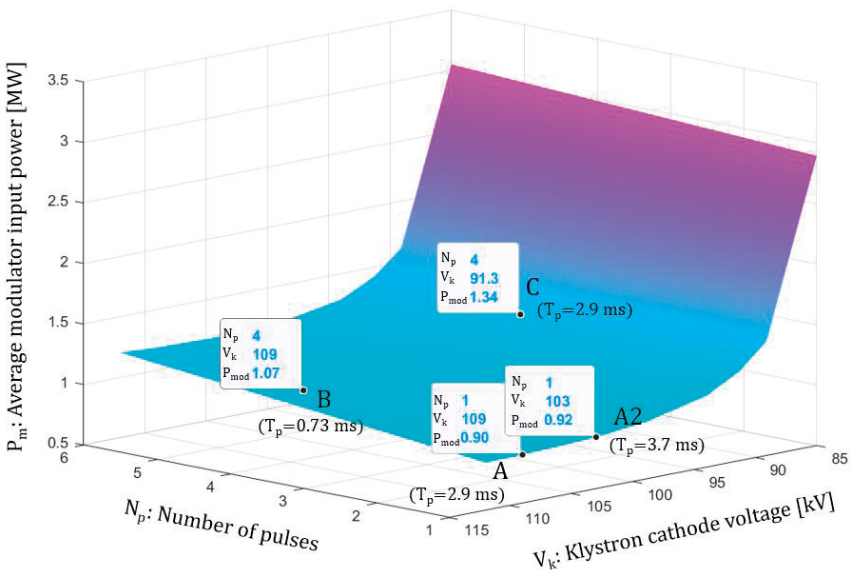



Figure 7.48: Required modulator input power in considering interleaved pulsing schemes for the ESSnuSB project

Table 7.1: Analysis of proposed interleaved pulsing schemes for the ESSnuSB project

| **Scenario A** | **Scenario A2** |
|---|---|
| + Addition of a single pulse at baseline pulse length and voltage<br>+ Fully retains baseline efficiency<br>+ Modest upgrade of cryogenics distribution<br>+ Short ring filling time<br>-- Requires re-design of horn power supply | + Addition of a single pulse, at increased pulse length but decreased klystron cathode voltage<br>- Slightly decreased grid-to-RF efficiency<br>+ Modest upgrade of cryogenics distribution<br>+ Short ring filling time<br>+ Improved performance with respect to $H^-$ ion stripping<br>-- Requires re-design of horn power supply |
| **Scenario B** | **Scenario C** |
| - Requires addition of 4x pulses, each at ¼ pulse length at baseline voltage<br>-- Significantly reduced grid-to-RF efficiency (4 extra initialization periods)<br>-- Requires significant upgrades of cryogenics distribution<br>+ Short ring filling time<br>+ Minimum changes to horn power supply | --- Requires addition of 4x pulses, each at baseline pulse length at ~85% of the baseline voltage (oversizing)<br>--- Severely reduced grid-to-RF efficiency: only 27.7% (4 extra initialization periods, reduced cathode voltage)<br>-- Requires significant upgrades of cryogenics distribution<br>--- Large ring filling time likely to lead to instabilities<br>++ Improved performance with respect to $H^-$ ion stripping |

*Circuit simulation of selected scenarios*

The scenarios selected for further considerations are simulated and discussed in the following-

As shown in Figure 7.42, pulsing scheme A implies operation at the baseline operating point but with twice the pulse repetition rate (i.e., 28 Hz as opposed to the nominal 14 Hz). Correspondingly, the capacitor charging power is doubled, i.e., representing a doubling in the charging current. As can be seen, flicker free operation is obtained according to the principles developed in section 7.2.2. Finally, the flat top ripple is limited to below 0.1% of the flat top amplitude, well below the imposed limit.

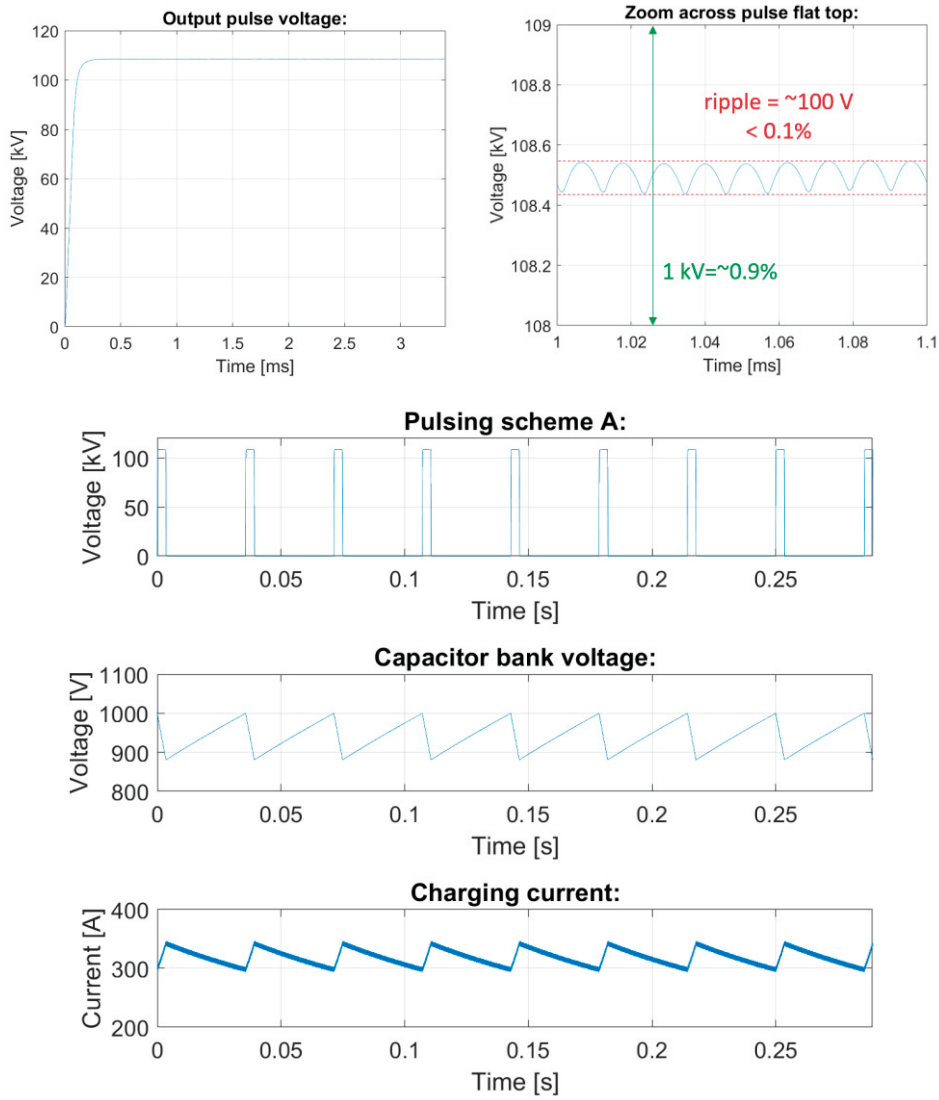



Figure 7.49: Circuit simulation results for interleaved pulsing scheme A

Simulation results for scenario A2 are presented in Figure 7.50. Here, every other pulse has slightly reduced amplitude and slightly prolonged pulse length. Clearly, the baseline pulse exhibits the performance shown in Figure 7.49. The added pulse event, on the other hand, exhibits somewhat reduced flat top ripple in accordance with the voltage ripple cancellation principle developed in relation to Figure 7.43. Additionally, representing very similar grid-to-RF efficiency and, thus, modulator input power (the difference is on the order of ~2% of the total charging power), operation from the perspective of the capacitor charger is virtually identical.

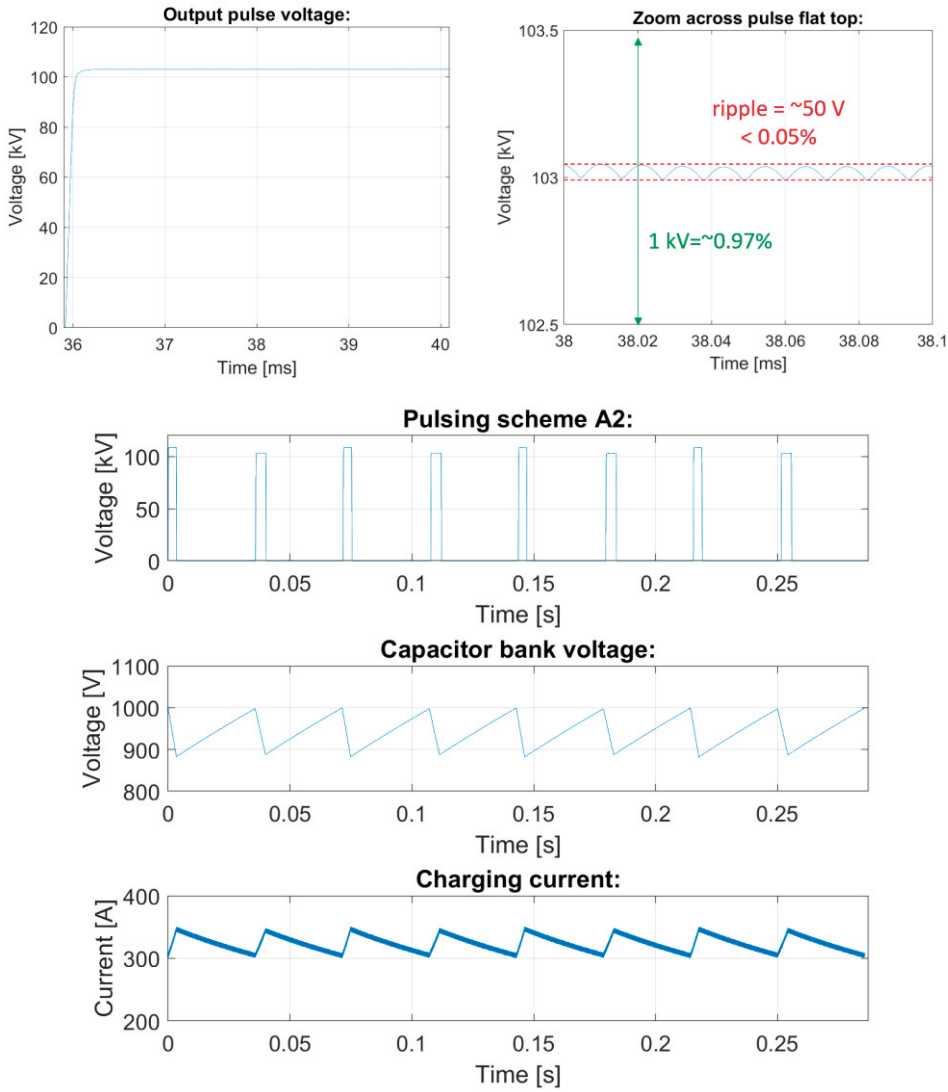



Figure 7.50: Circuit simulation results for interleaved pulsing scheme A2

Finally, Figure 7.51 shows simulation results for an improbable yet interesting sample 'mixed' interleaved pulsing scheme. In addition to one baseline proton pulse (109 kV, 3.5 ms), this pulsing scheme features the following pulses interleaved with each baseline pulse event. Each pulse event is repeated at 14 Hz, for a total pulse repetition rate of 70 Hz.

- 1x baseline proton pulse; 109 kV, 3.5 ms
- 1x ‘scenario A2 pulse’; 103 kV, 4.2 ms
- 1x ‘scenario B pulse’; 109 kV, 1.2 ms
- 1x ‘scenario C pulse’, 90 kV, 3.5 ms
- 1x additional pulse; 25 kV, 10 ms

Importantly, the capacitor charging scheme developed in section 7.2.2 is here operated as described, but predicting twice the average power. Consequently, the capacitor bank voltage fluctuates in-between baseline pulse events, eventually reaching the desired setpoint just in time for the next baseline pulse event. Hence, constant power flicker free charging is attained despite the heavily pulsed and varied load displayed in Figure 7.51. Note that the output stage controllers developed in section 7.3 straightforwardly handles the varying capacitor bank voltage in generating the required pulses.

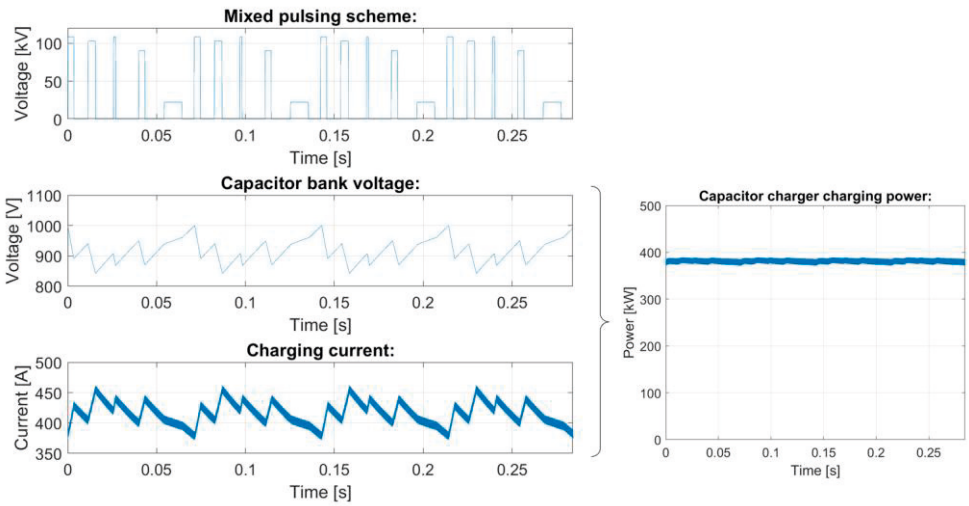



Figure 7.51: Circuit simulation results for sample ‘mixed’ interleaved pulsing scheme

## 7.5 References

[7.1] D. A. Paice, Power Electronics Converter Harmonics. Hoboken, NJ: Wiley, 1999.

[7.2] M. Collins and C. A. Martins, “A constant power capacitor charging structure for flicker mitigation in high power long pulse klystron modulators,” in Proc. IEEE Int. Pulsed Power Conf., Brighton, U.K., Jun. 2017, pp. 1–8.

[7.3] M. Collins and C. A. Martins, “Evaluation of a novel capacitor charging structure for flicker mitigation in high-power long-pulse modulators,” IEEE Trans. Plasma Sci., vol. 47, no. 1, pp. 985–993, Jan. 2019.

[7.4] L. Harnefors et al., Control of Voltage-Source Converters and Variable-Speed Drivers. Stockholm: US-AB Digitaltryck, 2014.

[7.5] L. Harnefors and H.-P. Nee, “Robust current control of AC machines using the internal model control method,” in Proc. IEEE Industry Applications Conference Thirtieth IAS Annual Meeting., Orlando, FL, USA, Oct. 1995, pp. 303-309.

[7.6] L. Harnefors and H.-P. Nee, “Model-based current control of AC machines using the internal model control method,” IEEE Trans. Ind. Appl., vol. 34, no. 1, pp. 133-141, Jan.-Feb. 1998.

[7.7] N. Mohan et al., Power Electronics: Converters, Applications, and Design, 3rd ed. Hoboken, NJ: Wiley, 2002.

[7.8] K. Ogata, Modern Control Engineering, 5th ed. Hudson, NY: Pearson, 2009.

[7.9] G. Gokbulut, “Combining forces for a Novel European Facility for Neutrino-Antineutrino Symmetry-Violation Discovery”, in Proc. Of NuPhys 2017, London, UK, Dec. 20-22, 2017.

[7.10] A. Alekou and E. Baussan and N. Blaskovic Kraljevic and M. Blennow and M. Bogomilov and E. Bouquerel and A. Burgman and C. J. Carlile and J. Cederkall and P. Christiansen and M. Collins and E. Cristaldo Morales and P. Cupial and L. D Alessi and H. Danared and J. P. A. M. de Andre and J. P. Delahaye and M. Dracos and I. Efthymiopoulos and T. Ekelof and M. Eshraqi and G. Fanourakis and E. Fernandez-Martinez and B. Folsom and N. Gazis and Th. Geralis and M. Ghosh and G. Gokbulut and L. Halic and A. Kayis Topaksu and B. Kildetoft and B. Klicek and M. Koziol and K. Krhac and L. Lacny and M. Lindroos and M. Mezzetto and M. Oglakci and T. Ohlsson and M. Olvegard and T. Ota and J. Park and D. Patrzalek and G. Petkov and P. Poussot and R. Johansson and S. Rosauro-Alcaraz and B. Szybinski and J. Snamina and G. Stavropoulos and M. Stipcevic and F. Terranova and J. Thomas and T. Tolba and E. Trachanas and R. Tsenov and G. Vankova-Kirilova and N. Vassilopoulos and E. Wildner and J. Wurtz and O. Zormpa and Y.

Zou, "The European Spallation Source neutrino Super Beam", in Proc. of Snowmass 2021.

[7.11] E. Baussan, N. Blaskovic Kraljevic, M. Blennow, M. Bogomilov, E. Bouquerel, A. Burgman, C. J. Carlile, J. Cederkall, P. Christiansen, M. Collins, E. Cristaldo Morales, L. D'Alessi, H. Danared, J. P. A. M. de André, J. P. Delahaye, M. Dracos, I. Efthymiopoulos, T. Ekelöf, M. Eshraqi, G. Fanourakis, E. Fernandez-Martinez, B. Folsom, M. Ghosh, G. Gokbulut, L. Halić, A. Kayis Topaksu, B. Kliček, K. Krhač, M. Lindroos, M. Mezzetto, M. Oglakci, T. Ohlsson, M. Olvegård, T. Ota, J. Park, G. Petkov, P. Poussot, S. Rosauro-Alcaraz, G. Stavropoulos, M. Stipčević, F. Terranova, J. Thomas, T. Tolba, R. Tsenov, G. Vankova-Kirilova, N. Vassilopoulos, E. Wildner, J. Wurtz, O. Zormpa, Y. Zou, "Update physics performance of the ESSνSB Experiment", The European Physical Journal C, vol. 81, pp. 1-12, 2021.

[7.12] M. Ghosh, "Physics reach of the ESSnuSB experiment", in Proc. of the 17th International Conference on Topics in Astroparticle and Underground Physics (TAUP 2021), IFIC Valencia, Valencia, Spain, Aug. 26 to Sept. 3, 2021, pp. 1-5.

[7.13] A. Alekou, E. Baussan, A.K. Bhattacharyya, N. Blaskovic Kraljevic, M. Blennow, M. Bogomilov, B. Bolling, E. Bouquerel, O. Buchan, A. Burgman, C.J. Carlile, J. Cederkall, P. Christiansen, M. Collins, E. Cristaldo Morales, P. Cupiał, L. D'Alessi, H. Danared, D. Dancila, J. P. A. M. de André, J.P. Delahaye, M. Dracos, I. Efthymiopoulos, T. Ekelöf, M. Eshraqi, G. Fanourakis, A. Farricker, E. Fernandez-Martinez, B. Folsom, T. Fukuda, N. Gazis, B. Galnander, Th. Geralis, M. Ghosh, G. Gokbulut, L. Halić, M. Jenssen, A. Kayis Topaksu, B. Kildetoft, B. Kliček, M. Kozioł, K. Krhač, Ł. Łacny, M. Lindroos, C. Maiano, C. Marrelli, C. Martins, M. Mezzetto, N. Milas, M. Oglakci, T. Ohlsson, M. Olvegard, T. Ota, J. Park, D. Patrzalek, G. Petkov, P. Poussot, R. Johansson, S. Rosauro-Alcaraz, D. Saiang, B. Szybiński, J. Snamina, G. Stavropoulos, M. Stipčević, R. Tarkeshian, F. Terranova, J. Thomas, T. Tolba, E. Trachanas, R. Tsenov, G. Vankova-Kirilova, N. Vassilopoulos, E. Wildner, J. Wurtz, O. Zormpa, Y. Zou, "The European Spallation Source neutrino Super Beam Conceptual Design Report", The European Physical Journal ST, vol. 231, no. 21, 2022.

[7.14] B. Gålnander et. al., "H- source design, integration into ESS and RF

upgrade studies". Technical report. May 2019, pp. 1-37

[7.15] M. Collins et. al, "Evaluation of Klystron Modulator Performance in Interleaved Pulsing Schemes for the ESS Neutrino Super Beam Project", in Proc. IEEE Int. Power Modulator and High Voltage Conf., Knoxville, TN, USA, Jun. 2022, pp. 60-63.

# 8. Development of reduced-scale technology demonstrator

## 8.1 Background

Chapter 5 treated mathematical modeling and design optimization of the Stacked Multi-Level modulator topology, concluding with a presentation of a complete design considering European Spallation Source klystron modulator requirements. A detailed account of the implementation of this modulator design is treated in the immediately following chapter. However, to demonstrate the developed technology, it was of interest to first implement a reduced-scale version of the proposed modulator design. Consequently, it was decided to construct a technology demonstrator rated for $1/5^{th}$ of the ESS modulator power requirements (115 kV, 20 A, 3.5 ms, 14 Hz), [8.1]. While it would have been possible to perform system optimization in generating a modulator design for these specific system requirements, it was preferable to instead directly scale the design proposed in chapter 5 in ensuring topological compatibility and validity of results. Hence, the demonstrator should be based on the same module configuration as the full-scale system (i.e., three parallel charger systems sourcing six series-connected pulse generator circuits) and, importantly, each conversion stage should be designed to handle the same voltage level as the corresponding full-scale system. The development of this technology demonstrator is treated in this chapter-

- Section 8.2 describes the developed technology demonstrator. Here, a semi-detailed electrical schematic identifies the main modulator components. Each component and their ratings are discussed. Considering a reduced-scale version of the modulator, details on design are kept brief.
- Section 8.3 presents some experimental results obtained on the technology demonstrator. Most importantly, the resulting output pulse waveforms are shown and described. In addition, the novel capacitor bank charging scheme proposed in chapter 7 is demonstrated.

## 8.2 Development of reduced-scale modulator prototype

An overview of the developed and integrated reduced-scale modulator prototype is shown in Figure 8.1. The corresponding electrical schematics are shown in Figure 8.2. Referring to these figures, the modulator system may be divided into three main subsystems-

- The standing electrical cabinet serves as the electrical input to the klystron modulator, housing the three capacitor charger systems.
- The horizontal electrical cabinet on top of the oil tank assembly contains the main capacitor bank energy storage as well as the six H-bridge converters.
- The oil tank assembly contains all high-voltage components, including the high-voltage modules (transformer, rectifier, filters) and sensors.

The contents of the main subsystems are described in detail in the following subsections.

Figure 8.1: Overview of developed reduced-scale technology demonstrator

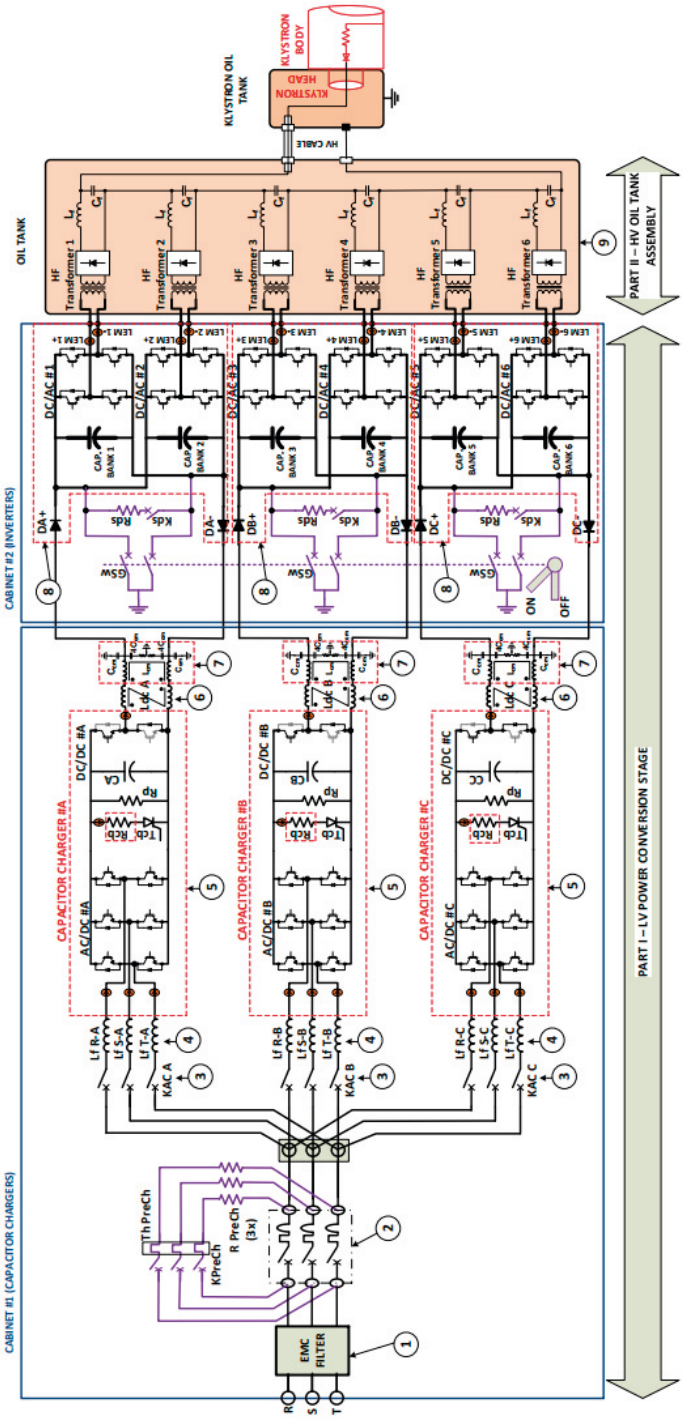



Figure 8.2: Semi-detailed electrical schematic of developed reduced-scale technology demonstrator

### 8.2.1 Cabinet #1: capacitor chargers

The input cabinet housing the capacitor chargers is made from two back-to-back standard 1000x600x2000 electrical cabinets and includes the components labelled (1) to (7) in Figure 8.2. A detailed overview of the contents of these cabinets is shown in Figure 8.3 and is discussed in the following.

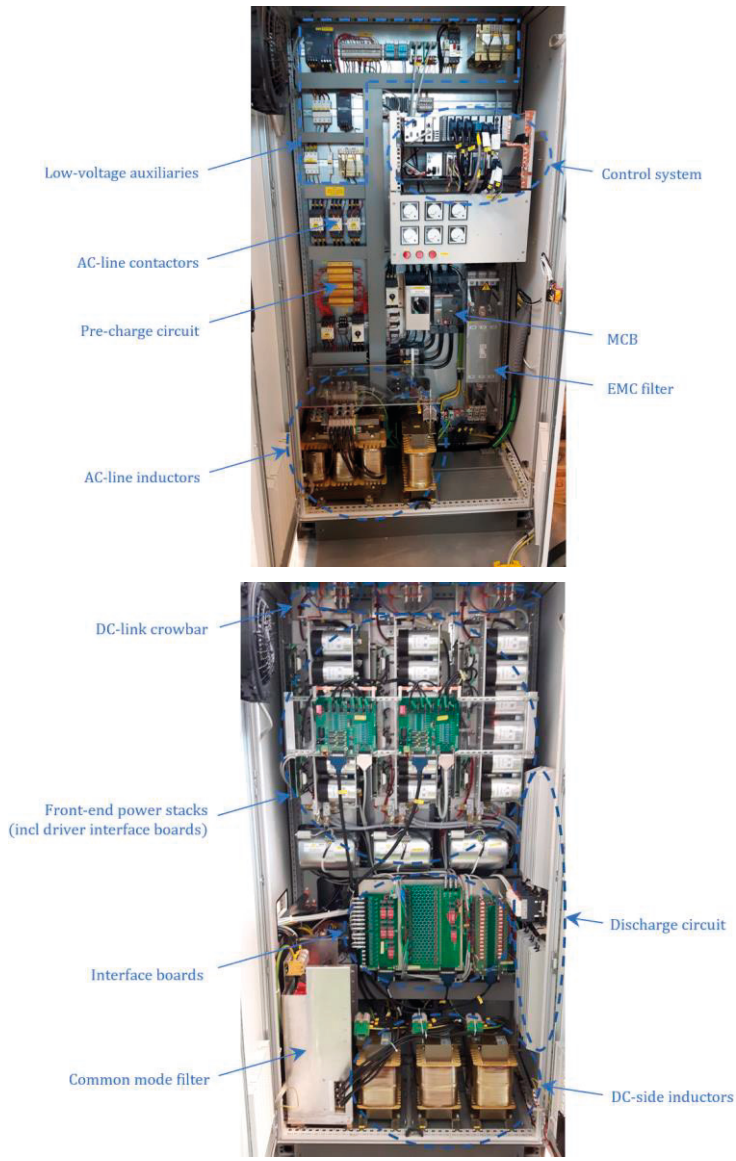



Figure 8.3: Contents of the standing electrical cabinet comprising the input stage capacitor charger systems

*(1) EMC filter*

Emission of EMC is in part mitigated through installation of an EMC filter at the input AC power port. Here, an off-the-shelf 3-phase EMC filter from FUSS-EMV was selected, [8.2]. The chosen filter is designed for use with industrial power converters connected to 400 V electrical grid with phase currents up to 200 A. Further details are omitted as this topic has not been discussed in detail in this dissertation.

*(2) Main circuit breaker and pre-charge system*

The main circuit breaker (MCB) connects/disconnects the entire modulator system to/from the electrical grid (with the notable exception of the control system and certain auxiliaries). The MCB is controllable (i.e., not manually operated) and operated directly by the main control system (described below). Here, the NSX100 breaker from Schneider Electric was chosen, [8.3]. This breaker is rated for operation at 600 V, 400 A with short-circuit breaking capacity of up to 10 kA. Additionally, a circuit formed by a three-phase contactor (rated 400 V, 10 A) and three resistors (47 Ω with power surge capability of 1.2 kW for 5 s) is connected in parallel with the MCB to allow pre-charging of the front-end power stack dc-link capacitors. As will be described in the following chapter, the final modulator configuration utilizes a different pre-charging method.

*(3) AC-line contactors*

The capacitor charger circuits are connected and disconnected by separate AC-line contactors controlled by the main control system, providing redundancy and permitting reduced-power operation. Here, a TeSys contactor from Schneider Electric was chosen, [8.4]. This contactor is rated 400 V and 60 A (AC3).

*(4) AC-line inductors*

The active rectifiers forming the front-end of the capacitor charger power stacks are connected to the electrical grid via the AC-line inductors. In keeping with the above, each rectifier is associated with an individual AC-line inductor. As noted in section 5.2.2, this reduced scale prototype relies completely on these inductors (direct inductive link) to provide the required line current harmonic attenuation. Hence, a relatively large inductance value of ~8 mH was necessary (coupled with a relatively high converter switching frequency). With the rated per-system AC line current of ~65 A, discussions with local magnetics company TRAMO ETV, [8.5], led to the development and subsequent procurement of the indicated three-phase inductors indicated in Figure 8.3.

*(5) Capacitor charger power stack*

The capacitor charger power stack was developed in collaboration with SEMIKRON, [8.6], and comprises the active rectifier and the dc/dc converter

(including drivers and auxiliaries), the dc-link capacitor as well as sensors for voltage and current measurement used for control and protection. An overview of the developed power stack is shown in Figure 8.4. Both converters are based on the SKM400GB17E4 half-bridge IGBT module, [8.7]. Though this module may be considered to be oversized given the application current level, it was preferred as it 1) ensured compatibility with the developed full-scale design, and 2) permitted simplified cooling solutions (a single off-the-shelf fan straightforwardly cools the entire power stack). The dc-link is implemented by six 300 µF capacitors rated 1250 V from Electronicon, resulting in a 1.8 mF dc-link in effectively limiting the dc-link voltage ripple.

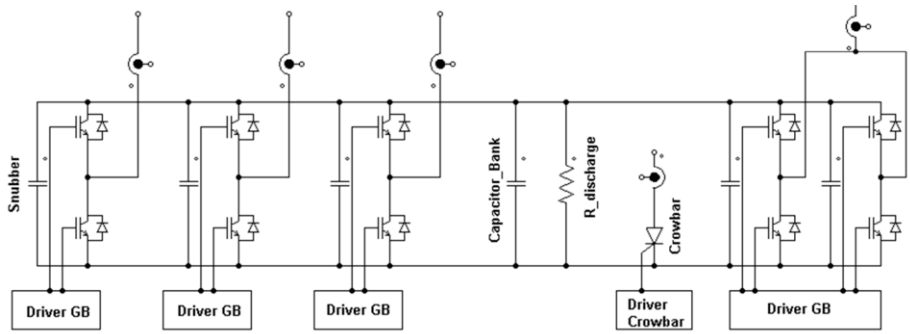



Figure 8.4: Electrical schematics of capacitor charger power stack (courtesy of SEMIKRON)

*(6) DC-side inductors*

The DC-side inductors connect the output of the dc/dc converter to the main capacitor bank. With each charger system operating independently, each inductor is rated 50 A. Here, an inductance value of ~16 mH was chosen in minimizing the current ripple. Discussions with local magnetics company TRAMO ETV led to the development and subsequent procurement of the indicated single-phase inductors indicated in Figure 8.3.

*(7) Common mode filter*

In grid-connected power converters, common mode signals are typically mitigated using the technique described in section 5.2.5. However, this technique relies on the presence of grid-side common mode inductance, typically as part of the grid-side inductor, either by adoption of single-phase inductors or three-phase inductor with fourth magnetic leg. Unfortunately, the decision to add this functionality was reached after the majority of the low-voltage system had been specified and procured. Hence, the developed AC-line inductors exhibit no common mode inductance and therefore cannot be used in common mode rejection. Additionally, available space in the electrical cabinets had to be respected, leading to the development of another method of common mode filtering. It is emphasized that this development was strongly influenced by the existing circumstances and is

generally not a cost- or space-effective solution. For these reasons, the details of the developed design are covered briefly in the following.

As shown in Figure 8.3, available space in the electrical cabinets was limited and it was decided to place the low-pass filter configuration at the output of the DC/DC converter. The cut-off frequency of the filter should be sufficiently greater than that of the third harmonic of the grid (i.e., 150 Hz) but still significantly lower than the switching frequency to provide adequate attenuation. The main cost and size driver of this filter are the common mode inductors. Here, inductors based on stacked toroidal nanocrystalline cores were considered. A design procedure based on a catalogue of available toroidal cores, generating inductor designs exhibiting a minimum common mode inductance while ensuring linear magnetic operation, physical fit of the winding turns as well as appropriate thermal response, was written. Note that the inductor windings have to carry the rated charger dc-side current. For this reason, thermal modeling included the possibility to add a small fan underneath each inductor stack to facilitate cooling. The corresponding required capacitors and damping resistors were calculated and chosen to yield the desired cut-off frequency and providing suitable damping. The associated filter attenuation is shown in the Bode plot of Figure 8.5. A summary of the developed design is shown in Table 8.1, and a photograph of the developed filter assembly is shown in Figure 8.6. It is again emphasized that the development was driven by 1) availability of cores with established performance and 2) the fact that only a single filter assembly was needed. The filter assembly is validated experimentally in the following section.

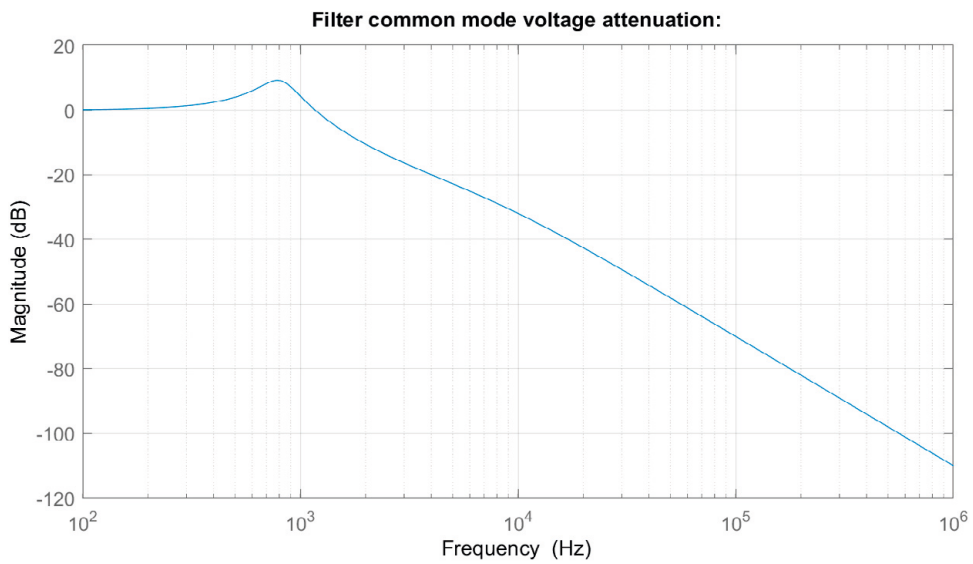



Figure 8.5: Bode plot showing common mode voltage attenuation of developed filter assembly

Figure 8.6: Developed common mode filter assembly

**Table 8.1: Overview of developed common mode filter design**

| Quantity | Value |
|---|---|
| Magnetic core type | T600006-L2102-W947 |
| Stacked cores per inductor | 6 |
| Number of turns per winding | 27 |
| Common mode inductance | 20 mH |
| Filter capacitance | 0.2 µF |
| Damping resistance | 120 |

*Control system*

The main control system is based on the CompactRIO platform including an FPGA backplane for fast and deterministic control, a CPU handling remote control interfacing and modulator state machine functionality and a set of directly interfacing I/O modules, [8.8]. All devices are reprogrammable using LabVIEW software and I/O modules may be replaced and interchanged as needed. This platform was particularly favoured from the perspective of prototyping given its flexibility and versatility. Additionally, its high performance and reliable deterministic operation was valued. In this case, the functionality of the central CompactRIO controller was extended with a second expansion chassis. The configuration is shown in overview in Figure 8.7. Here, in the main controller, modules 1, 2 and 3 are 100 kHz, 16-bit analog voltage input modules connected to the interface boards collating all voltage and current measurements (see Figure 8.2). Module 4 provides a fast bidirectional communication link to the expansion chassis permitting exchange of critical information such as fault conditions. Finally, modules 5 and 6 are 5V, 100 ns, 8-channel digital input/output modules (configured to provide 8 independent output channels) sending the gating signals to the half-bridge modules comprising the active rectifiers and dc/dc converters, Figure 8.2. Note that these modules connect to intermediary interface boards generating the required complementary IGBT gating signals and providing the +/- 15 V required by the IGBT driver circuits. The two remaining module spots are not used in the final modulator configuration but are considered useful (especially in prototyping) should the need to add extra functionality arise.

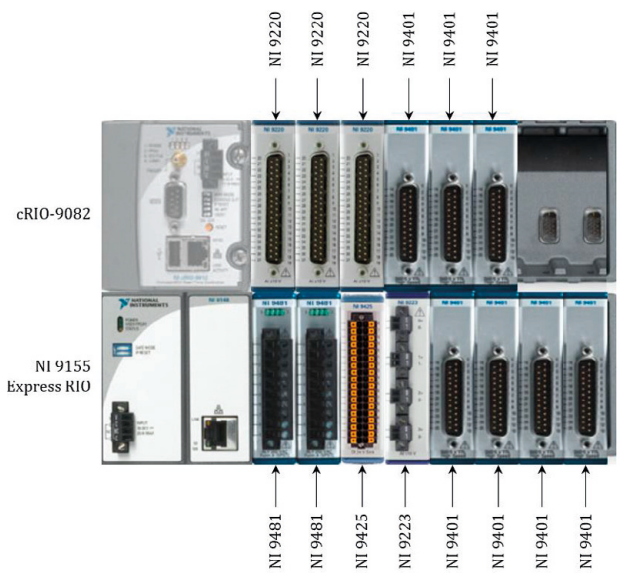



Figure 8.7: Overview of modulator main control system based on the CompactRIO platform

Then, for the expansion chassis, modules 1 and 2 are relay control modules used to (directly or indirectly) control the main circuit breaker, power contactors and discharge contactors, Figure 8.2. Module 3 is a 24 V, 32 channel digital input module connected to the interface board collating all logic interlock signals. In essence, this interface board contains digital readback (status signals) from, e.g., auxiliary contacts of relays/contactors and water flow-/thermoswitches to allow fault detection. Module 4 is a 1 MHz, 16-bit analog voltage input module for fast and precise measurement of the high-voltage pulse output signal. Module 5 is directly connected to module 4 of the main cRIO controller as described above. Module 6 is a digital input/output module used for remote control and interlocking. Finally, modules 7 and 8 are 5 V, 100 ns, 8-channel digital input/output modules (configured to provide 8 independent output channels) sending the gating signals to the half-bridge modules comprising the H-bridge converters, Figure 8.2. Again, note that these modules connect to intermediary interface boards generating the required complementary IGBT gating signals and providing the +/- 15 V required by the IGBT driver circuits.

*Auxiliary systems*

As shown in Figure 8.2 and Figure 8.4, each capacitor charger power tack is equipped with a discharge system comprised of a normally-closed contactor and a set of resistors. In case of fault, all converter gating signals are supressed and the contactor is closed, effectively discharging the dc-link capacitor. Here, rugged high-power resistors (CJT80047RJJ from TE Connectivity, [8.9]) are chosen to ensure compliance with the power corresponding to complete dc-link capacitor discharge over short time periods. It is also taken into account that it should be possible to handle multiple consecutive discharge events. As a second level of protection, a dc-link crowbar circuit comprising a thyristor in series with a discharge resistor is connected across the dc-link. The thyristor is triggered by a passive BOD (break-over diode) such that the dc-link is automatically discharged in case the dc-link voltage exceeds the BOD threshold voltage. The crowbar circuit also includes a current sensor to detect discharge events in generating fault signals in the main control systems to take appropriate action.

### 8.2.2 Cabinet #2: H-bridge converters

The second cabinet is a standard 1200x800x2000 electrical cabinet placed horizontally on top of the oil tank assembly, housing the main capacitor banks and the H-bridge power converters, Figure 8.8. In this case, labelled as (8) in Figure 8.2, the main capacitor bank was integrated as part of the H-bridge power stack assemblies.

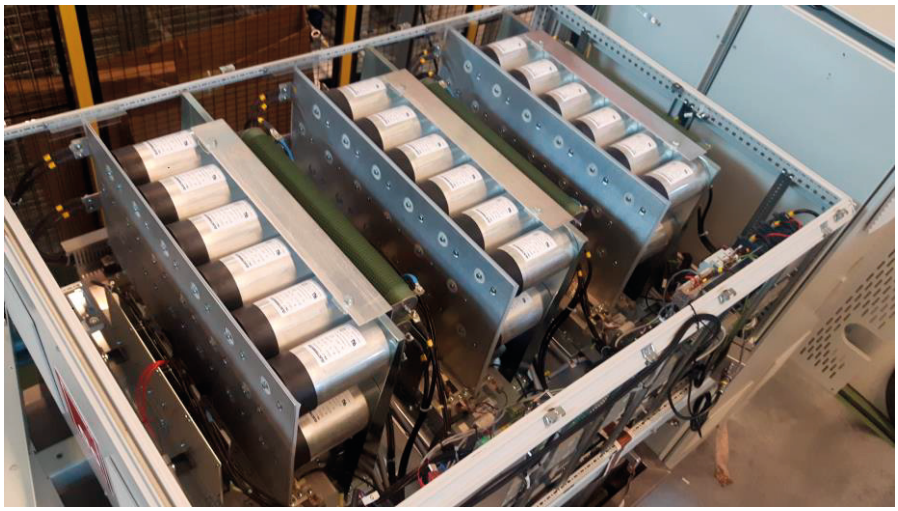


Figure 8.8: Contents of the horizontal cabinet comprising the main capacitor bank and the H-bridge converters

*(8) H-bridge converter power stack*

Similar to the capacitor charger power stack, the H-bridge power stack was also developed in collaboration with SEMIKRON. As mentioned, and as shown in Figure 8.8, the main capacitor bank was integrated as part of the power stack assemblies. Here, each power stack includes two individual H-bridge converters. The converters are based on the SKM400GB17E4 half-bridge IGBT module, [8.7], with two modules connected in parallel per equivalent half-bridge to ensure that peak power requirements are met. Again, this choice permits adoption of forced air-cooling solutions. It is also pointed out that somewhat oversizing the power stacks also allowed flexibility in choosing the converter operating frequency. This was particularly advantageous as the performance of, e.g., the magnetic cores were not certain at the time of design. Note that each converter also includes a pair of diodes to ensure unidirectionality of the power flow (this is not mandatory and may be omitted). It is emphasized that the two converters comprising the power stack share the same capacitor bank. Here, each capacitor bank is implemented by eighteen 1200 µF capacitors rated 1100 V from Electronicon, resulting in an equivalent ~65 mF system capacitor bank in limiting the total capacitor bank voltage droop to be below that of 150 V.

*Discharge system*

As shown in Figure 8.2, each H-bridge converter power stack is equipped with a discharge system comprised of a normally-closed contactor and a set of resistors. In case of fault, all converter gating signals are supressed and the contactor is closed, effectively discharging the energy storage. Here, rugged pulsed-power resistors are chosen to ensure compliance with the power corresponding to complete capacitor

bank discharge over short time periods (i.e., more than 10 kJ per stack discharging over a few hundreds of milliseconds). Additionally, it is taken into account that it should be possible to handle multiple consecutive discharge events.

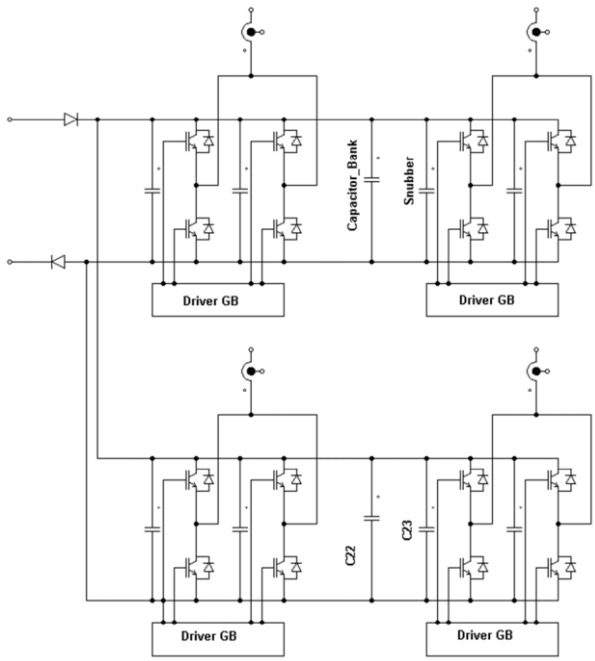



Figure 8.9: Electrical schematics of H-bridge power stack (courtesy of SEMIKRON)

### 8.2.3 High-voltage oil tank assembly

An overview of the developed high-voltage assembly is shown in Figure 8.10. Here, the assembly is being lowered into the associated oil tank. Especially note the resemblance to the assembly layout proposed in section 5.4. The assembly comprises six high-voltage modules, each including a high-voltage high-frequency transformer, common mode inductors, high-voltage rectifier, and filter, Figure 8.11. A brief description of the high-voltage components is given in the following.

Figure 8.10: High-voltage assembly being lowered into oil tank

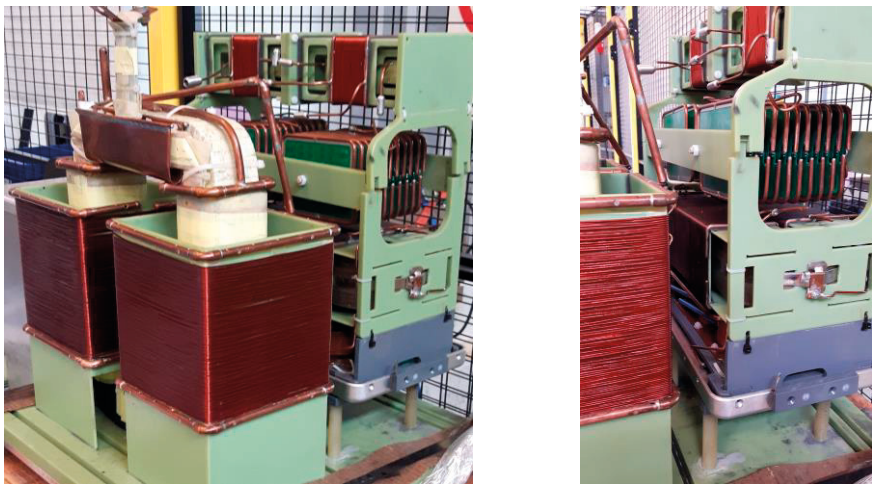


Figure 8.11: Overview of early prototype high-voltage module (enclosure removed for clarity)

*High-voltage high-frequency transformer*

Figure 8.12 depicts early construction and low-voltage testing of the first high-voltage high-frequency transformer prototype. This may be compared to Figure 5.25. The first design was based on a single uncut VITROPERM 500F nanocrystalline core with magnetic cross-sectional area ~54x54 $mm^2$. In early

prototyping work, the use of cut cores were considered to facilitate transformer winding but the material proved to be brittle and started to disintegrate, e.g., at touch. Hence, both primary and secondary windings had to be wound with the core in place. As explained in section 5.3.4, the primary windings are parallel connected, here with five turns per primary winding. The thickness of the foil is ~300 µm and the height is ~200 mm for an effective current density of 1.8 A/mm$^2$. The secondary windings are series connected with ~156 turns per secondary winding. In this case, round enamelled copper wire with a diameter of ~1.5 mm was used. In a second version of the prototype transformer (i.e., those seen in Figure 8.10), it was decided to use two magnetic cores in increasing the effective magnetic cross-sectional area to allow reduction of the number of turns per secondary winding to ~78. Later, in scaling the transformer design for the greater load current of the real ESS application, the cross-sectional area was again increased (with a proportional reduction of the number of winding turns) in further reducing the resulting voltage drop.

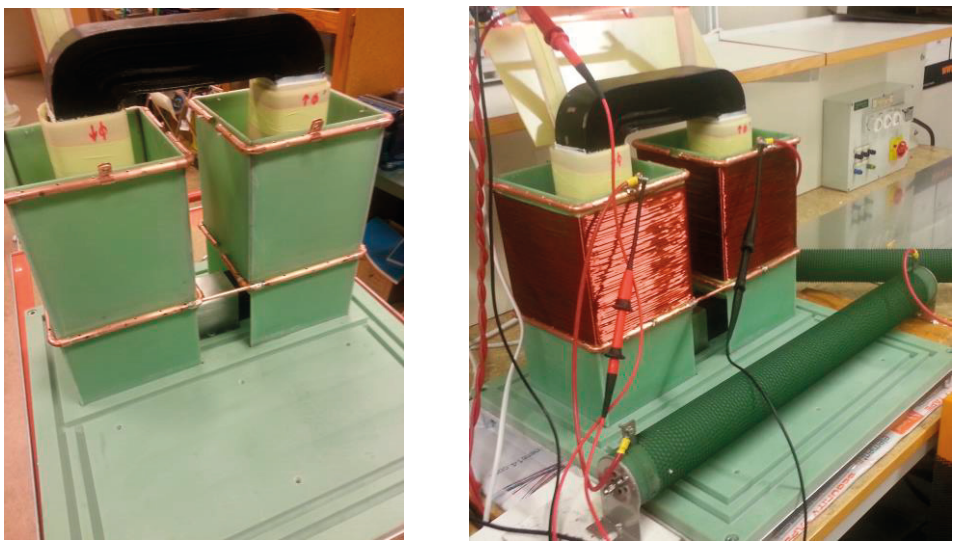


Figure 8.12: Construction of first high-voltage high-frequency transformer prototype

*High-voltage box*

With the exception of the high-voltage transformers, all module components are placed in an aluminium enclosure (box). The box is floating with respect to the oil tank walls (i.e., ground) with the capacity to withstand 160 kV$_{dc}$ for 1 minute. The components inside the box operate at 26 kV with respect to the enclosure and are designed to handle 50 kV$_{dc}$ for 1 minute. Consequently, the enclosure works as an

effective shield and floating ground. In particular, the electric field associated with the sharp edges of the components are hidden with respect to the outer tank walls.

*Common mode inductors*

A set of two series connected inductors are placed between the secondary windings of the transformer and the high-voltage rectifier in providing common mode filtering. Practically speaking and as proposed in section 5.3.7, it is preferable to implement this inductance as a single component. However, design of these prototype inductors was heavily influenced by the availability of off-the-shelf high-permeability magnetic cores at the time. Here, the resulting design feasibly provides the required common mode inductance while reasonably matching the size of the other high-voltage components. The magnetic cores are again based on VITROPERM 500F nanocrystalline material, here with magnetic cross-sectional area of ~25x20 $mm^2$ and a magnetic length of ~390 mm. The permeability of these cores is on the order of ~30000, [8.10]. Then, as described in section 5.3.7, each inductor has two windings wound in the same direction. Each winding has 39 turns, and are wound using the same type of copper wire used in winding the high-voltage high-frequency transformer secondary windings. Consequently, the resulting common mode inductance is ~80 mH.

*High-voltage rectifier*

Figure 8.13 shows the first batch of rectifier PCBs and the first proof-of-concept rectifier prototype. Each rectifier board contains four fast-switching diodes (IDB30E120; 1.2 kV, 50 A) from Infineon, [8.11]. Additionally, each diode is equipped with RC snubber (270 Ω, 3.6 nF), bleeder resistor (1 MΩ) and MOV according to the description given in section 5.3.5. The prototype rectifier is formed by a total of 42 rectifier boards mounted around a central insulating rod. Note also that the outer edges of each rectifier board are equipped with 4 mm copper anti-corona ring for field control.

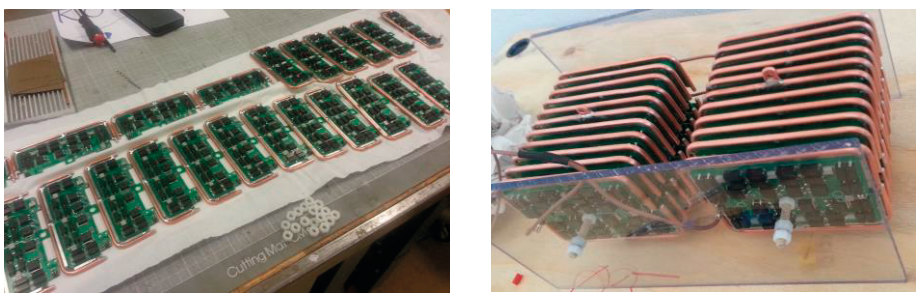


Figure 8.13: High-voltage rectifier: left) first batch of rectifier PCBs; right) proof-of-concept rectifier bridge

*High-voltage filter inductor*

The high-voltage filter inductor is based on conventional silicon electrical steel. The core is tape-wound using typical thickness of 0.25 mm and the magnetic cross-sectional area is ~55x50 $mm^2$. The core is cut in two U-shaped sections in facilitating inductor winding. Here, spacers of ~5.6 mm are introduced between the two core sections in defining the inductor air gap. The cores are mounted on and strapped to the fiberglass frames. The two windings are series connected, and each winding is made up of ~200 turns. Again, the same type of copper wire used in winding the high-voltage high-frequency transformer secondary windings is used. The resulting differential-mode inductance is on the order of ~50 mH.

*High-voltage filter capacitor branches*

The capacitor branches of the output filter are based on the capacitor UHV-12A (50 kV, 1700 pF) from TDK, [8.12]. The undamped branch is comprised of two capacitors and the damped branch is comprised of six capacitors. The filter damping resistors were selected from the Metallux high-voltage resistor series, [8.13]. Additionally, each branch is equipped with bleeder resistors (MOX-5-13) from Ohmite, [8.14].

## 8.3 Experimental results

The reduced-scale modulator was experimentally validated by measurement using the Tektronix TDS 3014C oscilloscope, [8.15]. Low-voltage measurements (i.e., not exceeding that of ~1 kV) were carried out using differential probes P5200A from Tektronix, [ref]. High-voltage measurements were carried out with the VD-100 high-voltage probe from North Star, [8.16]. This probe has a DC accuracy better than 0.1%, and better than 1% considering frequencies up to 1 MHz, [8.16]. Finally, current measurements were carried out using the TCP404XL current sensors from Tektronix, [8.17]. This sensor features accuracy on the order of 1%, [8.17].

### 8.3.1 High-voltage pulse quality

A measurement of the high-voltage output pulse as well as the corresponding primary-side H-bridge waveforms are shown in Figure 8.14. The pulse waveform is seen to feature a pulse rise time of ~120 μs.

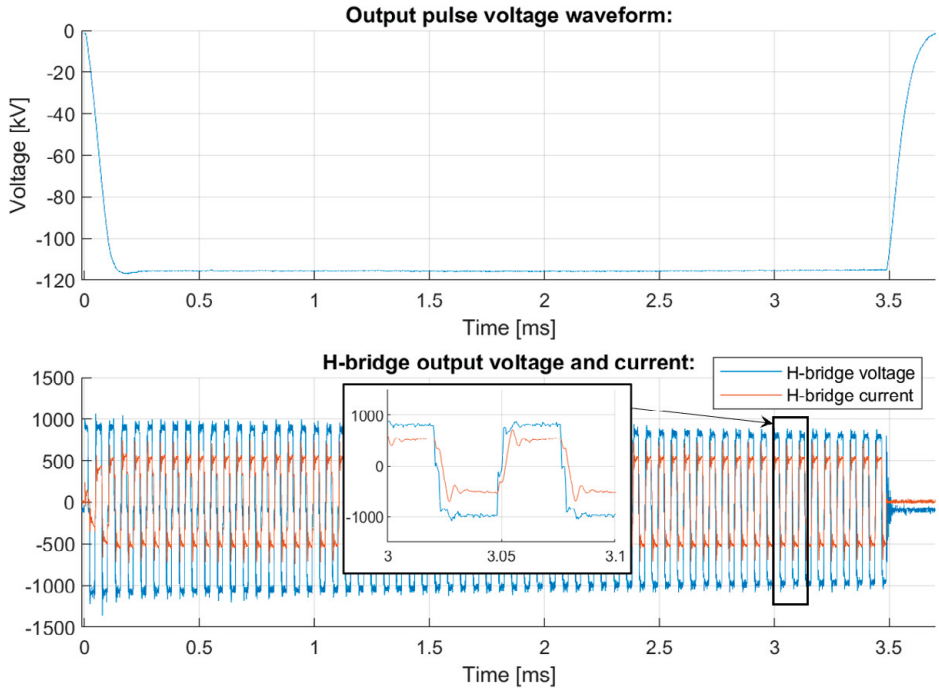



Figure 8.14: Output stage waveforms- a) high-voltage pulse waveform; b) H-bridge output voltage and current.

## 8.3.2 AC power quality

Figure 8.15 shows obtained input-stage measurements, [8.1]. The line voltage and the corresponding line current of a single phase is shown in Figure 8.15.a. As can be seen, the line current is sinusoidal with extremely low distortion, and is in phase with the associated line voltage. Additionally, the current amplitude is constant over time despite pulsed operation, i.e., representing flicker-free operation. This is obtained due to the constant power charging method proposed in section 7.2.2 and exemplified in Figure 8.15.b. As can be seen, the capacitor bank voltage droops from 1 kV to ~850 V during each pulse event. The capacitor bank is then charged back to 1 kV precisely before the next pulse event begins. Here, the associated charging current is controlled to exhibit inverse behaviour in representing constant power. The proposed charging method is evaluated under transient conditions in the following section.

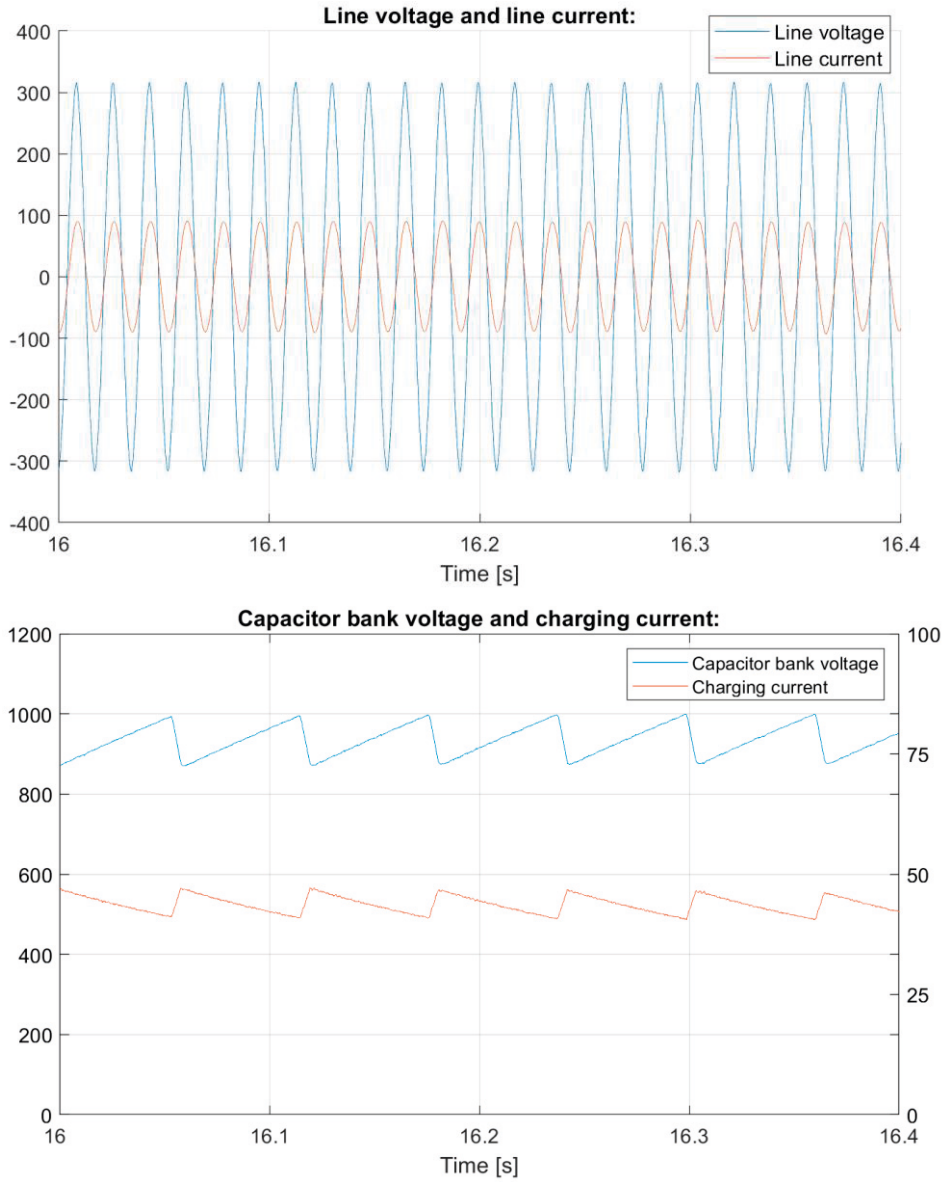



Figure 8.15: Input stage waveforms- a) line voltage and line current; b) capacitor bank voltage and charging current.

### 8.3.3 Verification of constant power charging control method

In this section, the method for constant power charging proposed in section 7.2.2 is evaluated and verified. Note that modulator pulsing is triggered externally in all of these experiments. This is important as it requires calculation of the pulse repetition

rate, i.e., requiring information from at least two consecutive pulse events such that externally changing the pulse repetition rate implies miscalculation of the charging reference during one charging period, [8.18]-[8.19].

Figure 8.16 shows the modulator first in standby mode. Pulsing begins at approximately $t = 2.2\ s$. The capacitor bank voltage drops from its standby value, here ~610 V, and the charger immediately responds with the charging current calculated according to the scheme described in section 7.2.2. Especially note that steady state is reached in one pulsing cycle, i.e., no disturbance on the grid is observed. Then, at approximately $t = 3.95\ s$, i.e., between two pulses, the modulator receives the signal to stop pulsing, responding by quickly charging the capacitor banks to their standby value.

Figure 8.17 takes place roughly half a second after the events in Figure 8.16 have ended. The modulator is again initially in standby mode. At approximately $t = 4.2\ s$, pulsing is restarted and steady state is achieved. This sequence is identical to the beginning of that shown in Figure 8.16. Then, at approximately $t = 6.8\ s$, the pulse repetition rate is externally changed from 6 Hz to 3 Hz. As mentioned, this change is unknown to the modulator control system which, as explained, will continue charging with the old reference. No pulse appears at the expected time, and the charger stops charging when the capacitor bank voltage reaches the standby value. When finally triggered to pulse, the frequency change has been detected and the modulator immediately assumes steady state operation in one cycle as described in the preceding case. Here, since the time between pulses has been elongated, the charging power may be seen to have been reduced. Finally, at approximately $t = 9.2\ s$, the pulse repetition rate is externally changed back from 3 Hz to 6 Hz. Here, the inverse problem is experienced. A lower charging reference is used, expecting the following pulse trigger at a much later time. Here, however, an additional charging cycle is needed to detect the frequency change. This is due to an unfortunately signal delay between the pulse generation circuit and the control system of the capacitor charger, which, receiving the external trigger, also performs the calculation of the pulse repetition rate. This problem was eliminated in the full-scale modulator by implementing a faster link between the two subsystems.

Figure 8.18 follows Figure 8.17 and is already pulsing when at approximately $t = 11.8\ s$, the pulse length is reduced from 3.49 ms to 1.99 ms. This is difficult to see in the plot of the pulsing condition but may be inferred from the reduction in capacitor bank voltage drop. Importantly, as this change is internal (i.e., set locally in the modulator control system), no additional calculation based on external signals is required. Hence, steady state is achieved in one charging cycle. Then, at approximately $t = 15.2\ s$, the pulse length is changed back from 1.99 ms to 3.49 ms, and steady state is achieved in one charging cycle.

Finally, in Figure 8.19, the voltage setpoint is changed in a step from 600 to 450 V at approximately $t = 16\ s$. Since the capacitor charger in its current configuration

cannot sink current, several pulsing cycles are required for the output to deplete the capacitor banks. However, as soon as the capacitor bank voltage drops beneath the setpoint, at approximately $t = 16.3\ s$, charging commences and steady-state charging is attained. Then, at approximately $t = 19\ s$, the voltage setpoint is changed back to 600 V and the capacitor charger accommodates the request in one charging cycle.

The results presented in Figure 8.16, Figure 8.17, Figure 8.18 and Figure 8.19 reveal excellent performance under transient conditions with the algorithm being able to respond to changes in the desired pulse length and load voltage setpoint (provided that the desired voltage is not decreased as the charger in its current configuration cannot sink current) in one charging cycle, as well as to changes in pulse repetition rate in as few as two charging cycles (one cycle being lost in detecting the change in external trigger frequency). It has also been demonstrated that the proposed charging method can perfectly well regulate the capacitor bank voltage, recharging the capacitor bank to precisely the requested value at the precise time the next pulse event is started. The capacitor bank charging current waveform, i.e., the current at the output of the dc/dc converter is also regulated as expected, with a sawtooth pattern inverse to that of the capacitor bank voltage. This way, the charging power waveform, i.e., the multiplication of the former waveforms is constant over time. Hence, absence of flicker is demonstrated. This may also be confirmed by the fact that also the ac line current amplitude is quite constant at every ac grid half cycle, i.e., it being almost impossible to perceive any difference between the time periods when the output pulse is generated and the time periods between pulses.

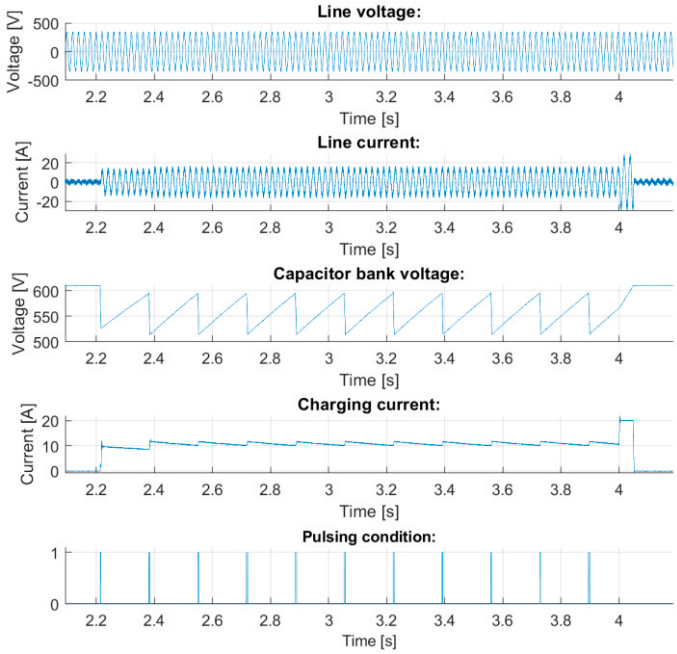



Figure 8.16: Experimental results for capacitor charger in pulsed mode—start and stop transients.

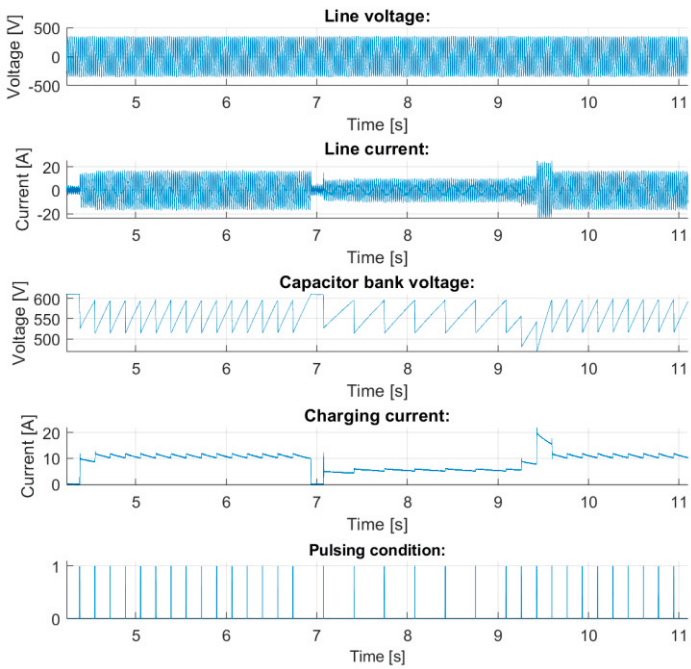



Figure 8.17: Experimental results for capacitor charger in pulsed mode—changing of external trigger frequency.

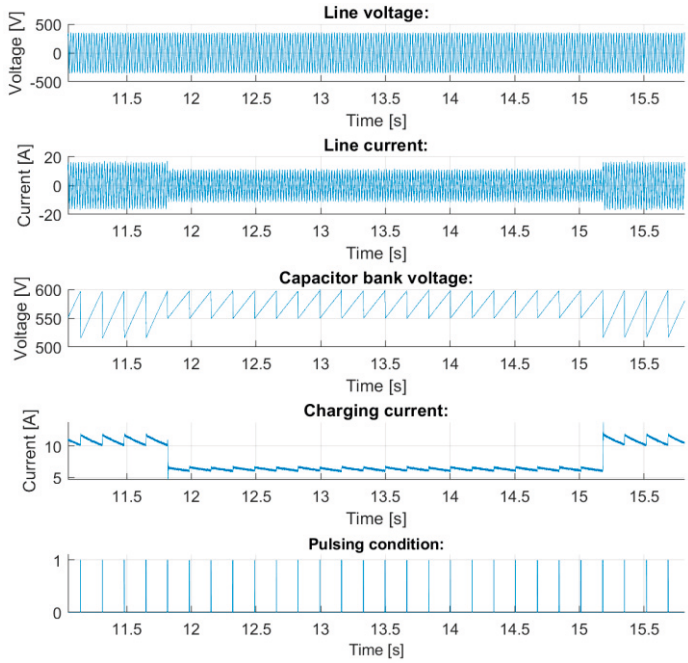



Figure 8.18: Experimental results for capacitor charger in pulsed mode—change of pulsewidth.

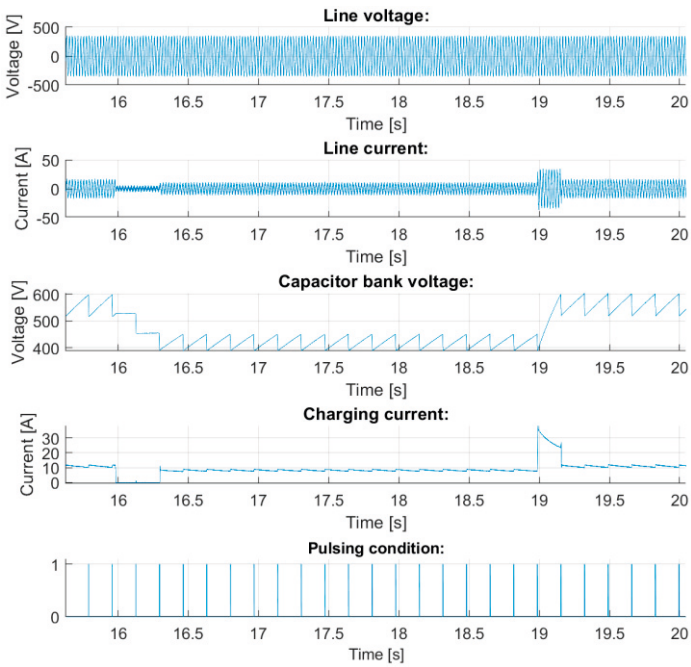



Figure 8.19: Experimental results for capacitor charger in pulsed mode—change of voltage set point.

## 8.4 References

[8.1] M. Collins et al, "Stacked multi-level long pulse modulator topology for ESS," in Proc. IEEE Int. Power Modulator High Voltage Conf. (IPMHVC), San Francisco, CA, USA, Jul. 2016, pp. 552–557.

[8.2] FUSS-EMV EMC filters and chokes. Accessed: June 24, 2023. [Online]. Available: https://www.fuss-emv.de/en/products/emc-filters

[8.3] Schneider Electric Circuit Breakers. Accessed: June 24, 2023. [Online]. Available: https://www.se.com/us/en/product-category/4200-circuit-breakers/

[8.4] Schneider Electric Contactors. Accessed: June 24, 2023. [Online]. Available: https://www.se.com/us/en/product-subcategory/1510-contactors-reversing-contactors/?filter=business-4-low-voltage-products-and-systems

[8.5] TRAMO ETV. Accessed: June 24, 2023. [Online]. Available: https://tramoetv.se/

[8.6] SEMIKRON. Accessed: June 24, 2023. [Online]. Available: https://www.semikron-danfoss.com/

[8.7] SEMIKRON SKM400GB17E4 IGBT Module. Accessed: June 24, 2023. [Online]. Available: https://www.semikron-danfoss.com/products/product-classes/igbt-modules/detail/skm400gb17e4-22895010.html

[8.8] NI CompactRIO Systems. Accessed: June 24, 2023. [Online]. Available: https://www.ni.com/sv-se/shop/compactrio.html

[8.9] TE Connectivity Resistors. Accessed: June 24, 2023. [Online]. Available: https://www.te.com/usa-en/plp/resistors/Y30xv.html

[8.10] Vacuumschmelze Amorphous and Nanocrystalline Cores. Accessed: June 24, 2023. [Online]. Available: https://vacuumschmelze.com/products/inductive-components-and-cores/amorphous-and-nanocrystalline-cores

[8.11] Infineon Technologies IDB30E120. Accessed: June 24, 2023. [Online]. Available: https://www.infineon.com/cms/en/product/power/diodes-thyristors/silicon-diodes/idb30e120/

[8.12] TDK UHV-12A. Accessed: June 24, 2023. [Online]. Available: https://product.tdk.com/en/search/capacitor/ceramic/uhv/info?part_no=UHV-12A

[8.13] Metallux AG High-voltage Resistors. Accessed: June 24, 2023. [Online]. Available: https://www.metallux.ag/products/high-voltage-resistors/

[8.14] Ohmite Maxi-Mox Series. Accessed: June 24, 2023. [Online]. Available: https://www.ohmite.com/catalog/maxi-mox-series

[8.15] Tektronix Oscilloscopes. Accessed: June 24, 2023. [Online]. Available: https://www.tek.com/en/products/oscilloscopes

[8.16] North Star High Voltage VD-100. Accessed: June 24, 2023. [Online]. Available: https://www.highvoltageprobes.com/product/vd-100/

[8.17] Tektronix AC/DC Current Measurement Systems. Accessed: June 24, 2023. [Online]. Available: https://www.tek.com/en/datasheet/ac-dc-current-measurement-systems

[8.18] M. Collins and C. A. Martins, “A constant power capacitor charging structure for flicker mitigation in high power long pulse klystron modulators,” in Proc. IEEE Int. Pulsed Power Conf., Brighton, U.K., Jun. 2017, pp. 1–8.

[8.19] M. Collins and C. A. Martins, “Evaluation of a novel capacitor charging structure for flicker mitigation in high-power long-pulse modulators,” IEEE Trans. Plasma Sci., vol. 47, no. 1, pp. 985–993, Jan. 2019.

# 9. Design and development of SML klystron modulator for ESS

The preceding chapter described the development and experimental validation and evaluation of a reduced-scale technology demonstrator. This chapter aims to similarly describe the development and validation of the corresponding full-scale modulator system. An overview of the complete klystron modulator is shown in Figure 9.1 and the corresponding semi-detailed electrical schematics are shown in Figure 9.2. With design and system optimization treated in chapter 5, this chapter emphasizes description, integration, simulation and experimental validation of the designed components and systems. This is carried out in two stages. First, the development of a prototype (though full-scale) converter chain is described. Here, sections 9.1-9.2 describe each component and their integration in detail. Finite element simulation results are presented where applicable in justifying design. Section 9.3 presents experimental results obtained on the prototype. Aspects of pulse quality, model validation, pulse control, efficiency and power quality are emphasized. Secondly, the development of the full-scale modulator system is described. With the majority of modulator components being identical to those described in the preceding sections, section 9.4 is focused on system integration. Finally, section 9.5 presents simulation results and section 9.6 presents final experimental results obtained on the full-scale modulator system.

Figure 9.1: Overview of complete SML modulator developed for ESS klystron requirements

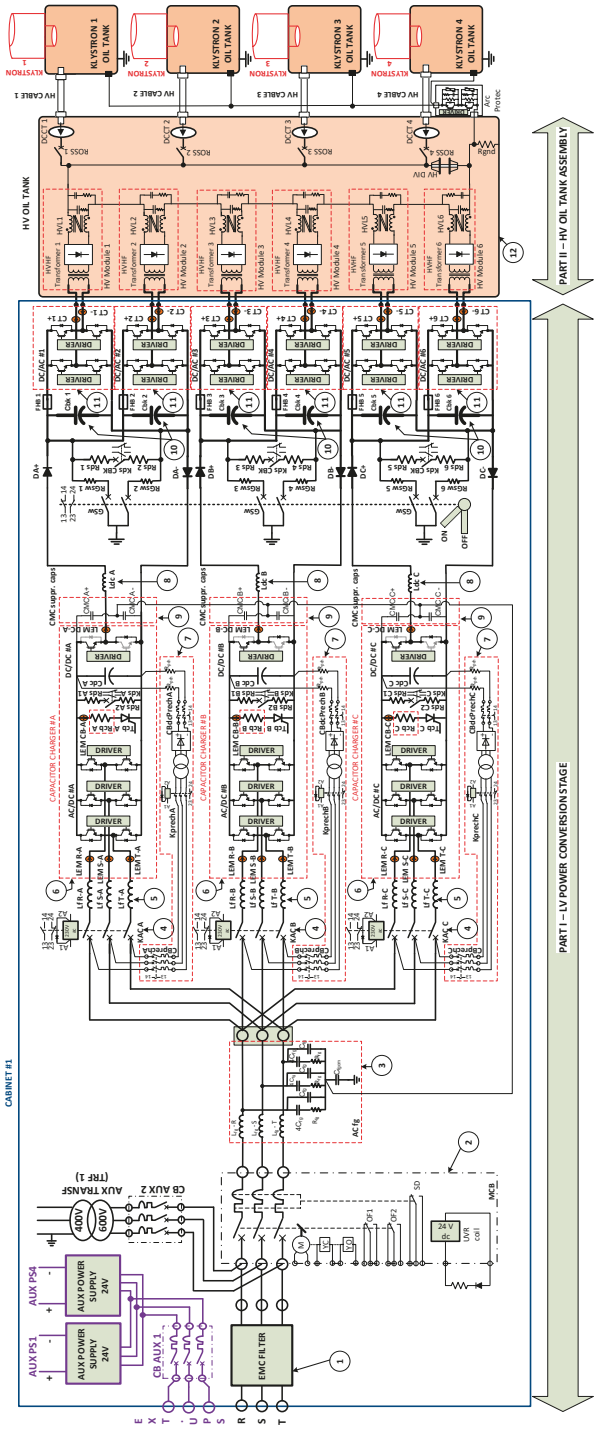



Figure 9.2: Semi-detailed electrical schematic of full-scale SML modulator

# 9.1 Development of prototype converter chain

The purpose of developing the prototype converter chain was twofold. First, since several components were custom-made or developed specifically for this system, it was desirable to evaluate and ensure the performance of each component before committing to a complete modulator design and eventual series production. Additionally, it was recognized that the developed prototype could be designed to be useful post series production. As an example, it is strategically important to secure secondary sources of several modulator components in ensuring system compatibility over 30+ years of operation. Here, the prototype could be (and was) made to facilitate exchange of key components without particular constraints on system power density. Hence, existing components could expeditiously be swapped for new secondary source components to be tested and evaluated in full power testing. The prototype could similarly be used in maintenance, e.g., with repaired components being functionally tested before being reinstalled in a modulator.

The developed prototype comprises one complete converter chain as shown in Figure 9.2, from the electrical grid at the input to a high-power resistive load at the output via one capacitor charger power stack and one H-bridge power stack. Correspondingly, the output pulse voltage is $1/6^{th}$ of the rated modulator voltage. Due to limited access of power connections and component availability, system auxiliaries were chosen considering a 400 V grid. An overview of the developed prototype is shown in Figure 9.3, and may be divided into three main systems:

- Low voltage cabinet; including subsystems (1)-(11) up to the HV interface.
- Oil tank assembly, comprising one high-voltage module
- High-power resistive dummy load.

The development and integration of these subsystems are described in the following sections.

Figure 9.3: Overview of prototype converter chain including high-voltage oil tank assembly and load cabinets. Three resistive load cabinets are obscured by the low-voltage cabinet.

### 9.1.1 Low-voltage cabinet

The low-voltage cabinet is made from two side-by-side standard 800x800x2000 electrical cabinets and includes one set of components labelled (1) to (11) in Figure 9.2. These components are described in the following.

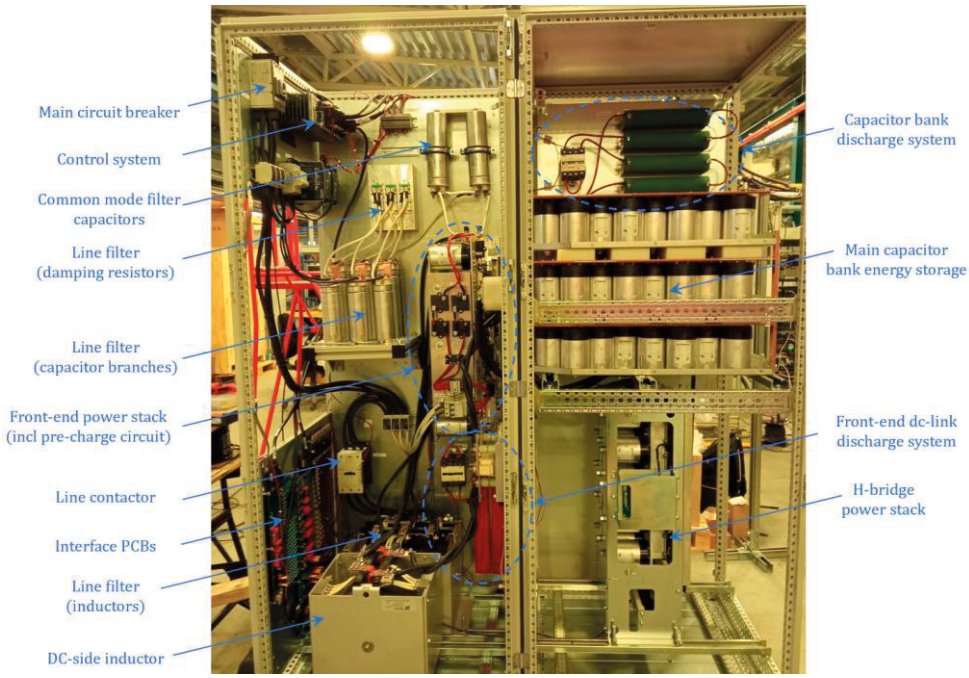



Figure 9.4: Overview of low-voltage cabinet. Cabinet doors and side walls have been removed for clarity.

*(1) EMC filter*

As the prototype system would operate only sporadically and at reduced power level, it was decided to omit the EMC filter in prototype development.

*(2) Main circuit breaker*

The main circuit breaker (MCB) connects/disconnects the entire modulator system to/from the electrical grid. In this case, the MCB is manually operated. Here, the 1SDA068208R1 XT1D from ABB was chosen, [9.1]. This breaker is rated for operation at 400 V, 250 A with short-circuit breaking capacity of up to 36 kA. As noted, in contrast to that of the reduced scale technology demonstrator, the dc-link pre-charge system is here a separate system and is discussed later.

*(3) Line filter capacitor branches*

As explained above, the prototype converter chain contains a single front-end capacitor charger. Hence, line current ripple cancellation due to converter interleaving is clearly not possible. In developing the prototype converter chain, it was decided to still use the same filter capacitance values in obtaining similar capacitor loading conditions even though the resulting line current THD would be higher (though still acceptable). Here, from Table 5.2, considering the reduced line-to-line voltage (400 V instead of 600 V), capacitors C44PKGR6100RBSJ (100 µF) and C44PLGR6200RASJ (200 µF) from KEMET were chosen, [9.2] and [9.3]. The damping resistors were designed and built in-house to exhibit a resistance of 50 mΩ and to compactly be able to dissipate significant power. As can be seen, the resistors were mounted on a heat sink to aid heat transfer. As shown in Figure 9.5, the capacitor terminals were interconnected using copper busbars in effectively forming $C_1 = 100\ \mu F$ and $C_2 = 400\ \mu F$. The capacitors were then connected to the filter damping resistors and the rest of the circuit using cables.

Figure 9.5: Overview of line filter capacitor branches. The capacitors in the damped branch of the filter are connected to custom-made damping resistors. Power dissipation is aided by the heatsink.

*(4) Line contactors*

The capacitor charger circuit is connected and disconnected by a normally-open AC-line contactor controlled by a 24 V coil operated by the main control system. Here, the contactor XTCE150G00TD from Eaton was chosen, [9.4], rated for 400 V and 150 A.

*(5) Line filter inductors*

The line filter inductor used in the prototype converter chain are based on the same design and configuration intended for the complete modulator system and is shown in Figure 9.6. These inductors were developed in collaboration with MagComp, [9.5]. Note that these inductors are based on a different technology than that described in section 5.2.3. Here, the $SM^2C$ mouldable core material permits almost noiseless inductor designs, [9.6]-[9.7], considered an important feature in the ESS accelerator RF gallery. Furthermore, the inductor windings are wound together and in close proximity to the cooling circuit, facilitating cooling and maximizing inductor power density. These inductors are designed to exhibit an inductance of 600 μH at the rated per-charger RMS current of 245 A. Furthermore, the coil temperature was not to exceed that of ~120 °C under steady-state operation with the inductor current waveform comprising a fundamental 50 Hz component of 245 A as well as a superimposed 3.6 kHz triangular with peak amplitude 25 A (representing switching ripple) and considering a cooling circuit liquid flow of ~6 l/min. The resulting inductor unit is shown in Figure 9.6 and weighs ~125 kg. As it was desirable to be able to switch inductors relatively quickly (e.g., for evaluation purposes), they were placed on the bottom of the cabinet where they can be easily manoeuvred (i.e., manually slid) on the metal railing.

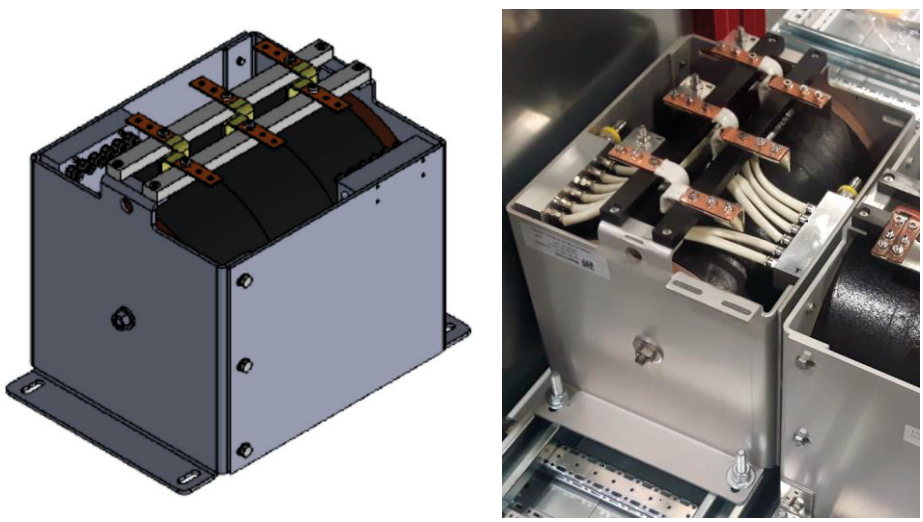


Figure 9.6: Overview of line filter inductors from MagComp, left) 3D conceptual drawing; right) component installed in low-voltage electrical cabinet. Note that the power terminals and water lines have not yet been connected.

*(6) Capacitor charger power stacks*

The capacitor charger power stack was again developed in collaboration with SEMIKRON, and comprises the active rectifier and the dc/dc converter (including drivers and auxiliaries), the dc-link capacitor as well as sensors for voltage and current measurement used for control and protection. Importantly, note that this power stack is based on the precisely the same components and is in precisely the same configuration as intended for the complete modulator system. Both converters are again based on the SKM400GB17E4 half-bridge IGBT module, [9.8]. In this case, each converter leg comprises two half-bridge modules. Furthermore, the power stack heat-sink is water cooled as described in section 5.2.5. The dc-link is based on the capacitor E50N13424N50P (420 µF, 1.1 kV) from Electronicon, [9.9]. Here, seven capacitors are used for a total dc-link capacitance of ~2.9 mF.

*(7) DC-link pre-charge system*

Each front-end capacitor charger system is equipped with an individual dc-link pre-charge system labelled (7) as shown in Figure 9.2. The same type of pre-charge system was implemented for this prototype converter chain and is shown in overview in Figure 9.7. This circuit comprises a contactor, a three-phase diode rectifier and a set of pre-charge resistors. Additionally, a circuit breaker is used for safety. Closing the contactor charges the dc-link through the resistors. The contactor is then opened and the system may be operated as usual through the main ac-line contactors, (4). Here, the resistor RPS0500DH47R0JB (47 Ω, 500 W) from Vishay, [9.10], and the diode rectifier VUO52-16NO1 (1600 V, 52 A) from IXYS, [9.11], were chosen. The contactor 3TG1001-0BB4 (400 V, 8.4 A, operated by 24 V coil), [9.12], and the circuit breaker 5SY4316-8, [9.13], from Siemens were selected.

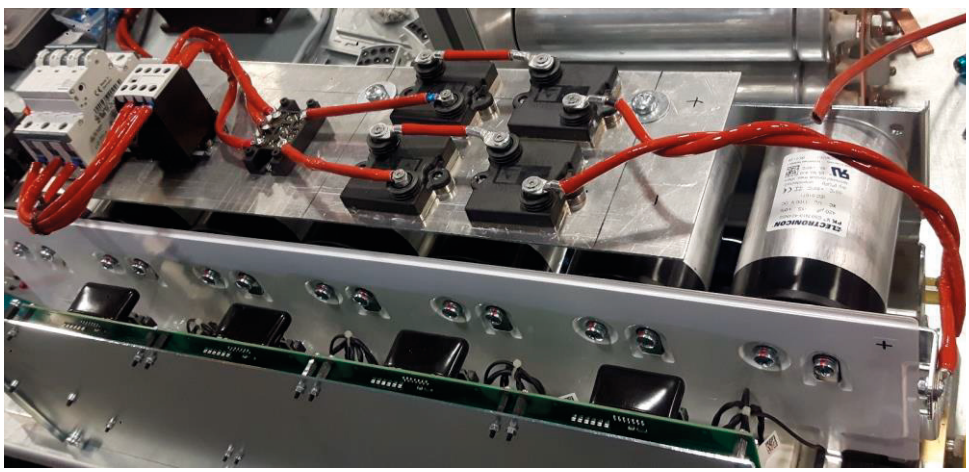


Figure 9.7: Capacitor charger power stack dc-link pre-charge system

*(8) DC-side inductor*

Similar to the line filter inductor, the DC-side inductor used in the prototype converter chain is also based on the same design and configuration intended for the complete modulator system, Figure 9.8. These inductors were also developed in collaboration with MagComp, and again based on a different technology than that described in section 5.2.3. The DC-side inductors are designed to exhibit an inductance of 4 mH at the rated per-charger RMS current of 240 A. Furthermore, the coil temperature was not to exceed that of ~120 °C under steady-state operation with the inductor current waveform comprising a 240 A dc-component as well as a superimposed 5 kHz triangular with peak amplitude 7.5 A and considering a cooling circuit liquid flow of ~4 l/min. The resulting inductor unit is shown in Figure 9.8 and weighs ~130 kg. As may be seen, the inductor is actually comprised of two inductor units connected in series. Again, to be able to switch inductors quickly, the DC-side inductor was placed on the bottom of the cabinet next to the line-side inductor, where they can be easily manoeuvred on the metal railing.

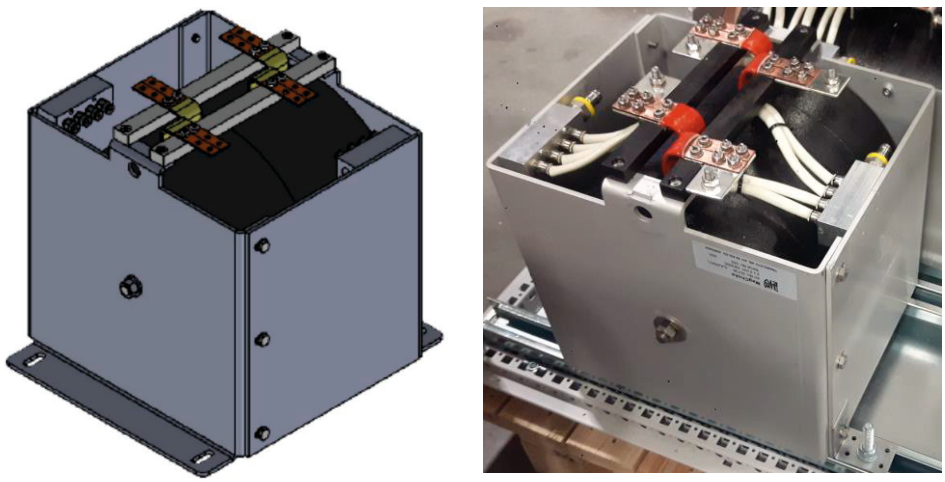


Figure 9.8: Overview of DC-side inductors from MagComp, left) 3D conceptual drawing; right) component installed in low-voltage electrical cabinet. Note that the power terminals and water lines have not yet been connected.

*(9) Common mode filter capacitors*

In contrast to the reduced scale prototyping work presented in chapter 8, the above-described line inductors are implemented as single-phase components and therefore exhibit common mode inductance. Hence, the common mode mitigation technique described in section 5.2.5 is directly applicable. Here, the parallel dc-link capacitors used in common mode mitigation were implemented by the polypropylene capacitor C20AKGR6100AASK (100 µF, 750 V) from KEMET, [9.14], was chosen.

*(10) Main capacitor bank*

The prototype capacitor bank was based on 420 µF, 1.1 kV polypropylene capacitors from Electronicon, [9.15], and is shown in Figure 9.9. Note that this is not the same type of capacitor or configuration discussed in chapter 5. This capacitor bank is built and stacked in three layers, with each layer comprising eight rows of five capacitors. The capacitors of each layer are connected in parallel with a copper sheet. The three layers are then connected in parallel by a copper busbar (not shown in Figure 9.9). The total capacitance is thus ~50.4 mF, representing one sixth of the total capacitance proposed in Table 5.2 such that the resulting capacitor bank voltage droop should match that of the full modulator system.

Figure 9.9: Overview of main capacitor bank.

*(11) H-bridge power stack*

The H-bridge power stack was again developed in collaboration with SEMIKRON, and comprises the H-bridge converter as well as a local dc-link capacitor and sensors for voltage and current measurement used for control and protection. The inclusion of a local capacitor bank in addition to the main capacitor bank, (10), is discussed in detail in section 5.3.3. Importantly, note that this power stack is based on the precisely the same components and is in precisely the same configuration as intended for the complete modulator system. As presented in Table 5.2, the H-bridge

converters are based on the CM1800HC-34N IGBT power module from Mitsubishi, [9.16]. Note that each power module represents a single IGBT switch, and that here two modules are parallel connected in forming an equivalent converter switch. Consequently, the H-bridge converter requires eight such modules. All modules are placed on a common water-cooled heat sink as described in section 5.3.3. The local capacitor bank is based on the capacitor E50N13424N50P (420 µF, 1.1 kV) from Electronicon, [9.17]. Here, fifteen capacitors are used for a total dc-link capacitance of ~6.3 mF. As with the other main power components, it was desirable to be able to quickly interchange power stacks. Therefore, the power stack was placed on the bottom of the electrical cabinet where it can be easily manoeuvred (i.e., manually slid) on the metal railing. The H-bridge power stack is connected to the main capacitor bank using power cables, and is connected to high-voltage module using special-made low-inductance busbars.

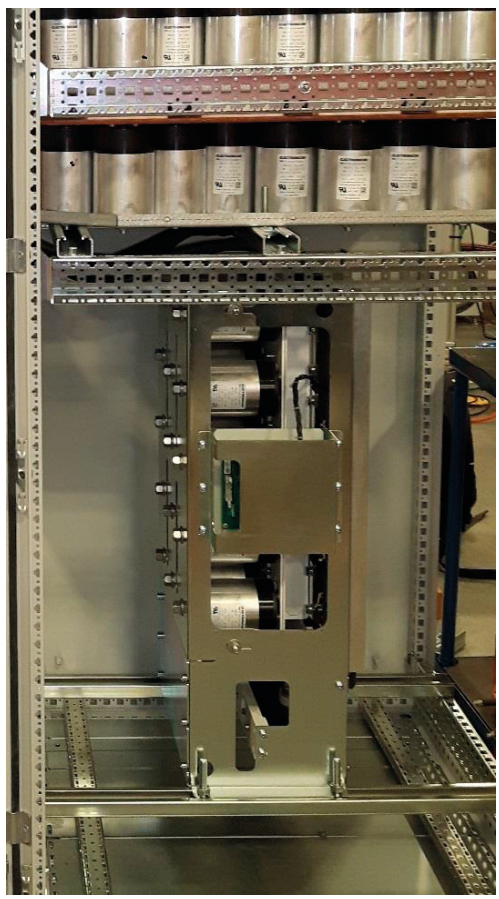


Figure 9.10: Overview of H-bridge power stack. Note the placement of the power stack on top of two sheet metal profiles, permitting fast exchange of components by sliding the power stack across the profiles and out of the cabinet.

*Capacitor bank discharge system*

The energy storage discharge system comprises a normally-closed contactor and a set of resistors, Figure 9.11. In case of fault, all converter gating signals are supressed and the contactor is closed, effectively discharging the main capacitor bank. Here, four resistors, TE1000B22RJ (22 Ω, 1000 W) from TE Connectivity, [9.18], were chosen. Two of these resistors are connected in parallel, and two such sets of resistors are connected in series, resulting in a total discharge time constant of ~1 s. Finally, the contactor LP1D65008BD from Schneider Electric was chosen, [9.19]. Here, two contactor poles were series connector to ensure proper handling of the imposed capacitor bank voltage.

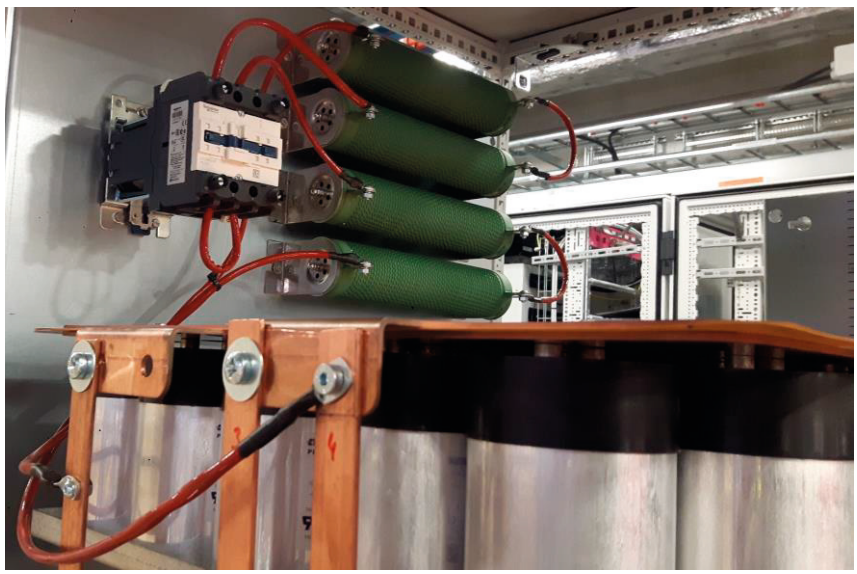


Figure 9.11: Overview of main capacitor bank discharge system

## 9.1.2 High-voltage module and oil tank

As described in section 5.3.1, the high-voltage module comprises a high-voltage high-frequency transformer, a high-voltage common mode inductor, a high-voltage rectifier and a high-voltage filter. Figure 9.12 shows an overview of the first full-scale prototype high-voltage module. Figure 9.12.a shows a close-up on the HVHF transformer where the box encloses the other components. In Figure 9.12.b, the box enclosure has been removed, providing a view of, particularly, the high-voltage rectifier, the high-voltage filter inductor and the high-voltage filter capacitor branches.

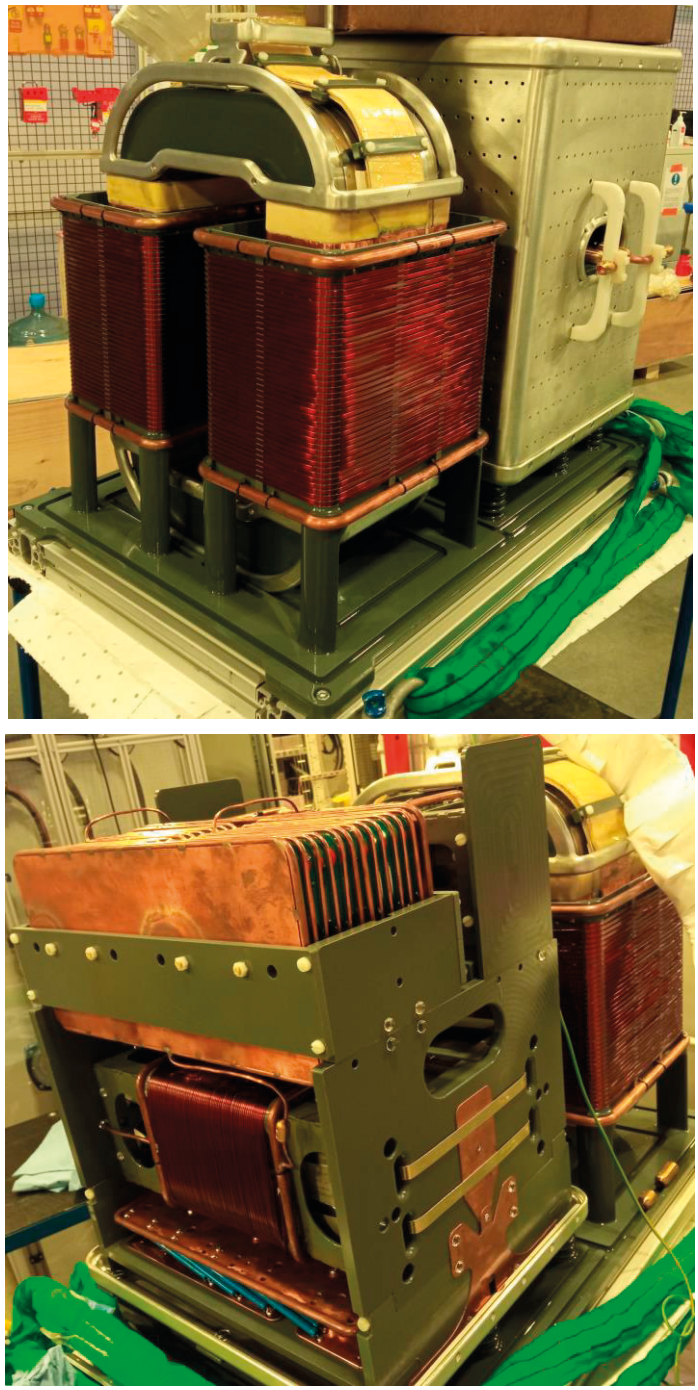


Figure 9.12: Overview of high-voltage module

*High-voltage high-frequency transformer*

This transformer design is based on three uncut VITROPERM 500F nanocrystalline cores with magnetic cross-sectional area 58x75 $mm^2$. Note that this clearly represents a significantly greater magnetic core than that of the corresponding reduced-scale prototype transformer despite the same voltage level. As described in section 8.2.3, this increase was necessary to proportionally maintain the inductive voltage drop despite the increasing load current. Correspondingly, the number of turns per secondary was reduced to 39. However, whereas for the reduced-scale transformer it was possible to use round wire of relatively small diameter in handling the RMS current density while sufficiently limiting skin effect, rectangular enamelled copper wire must be used in constructing the full-scale transformers. Here, a conductor cross-sectional area of ~4.6x1.3 $mm^2$ was used in limiting the current density to below that of 4 $A/mm^2$. Then, the primary windings are made with three turns to yield an effective transformation ratio of 26. The primary windings are of foil type, and the foil cross-section is ~315x0.22 $mm^2$ in handling the current density while effectively limiting the proximity effect. The high-voltage high-frequency transformer is studied in magnetostatic and electrostatic conditions using finite element analysis in section 9.2.

*High-voltage box*

Precisely as in the case of the reduced-scale high-voltage prototype described in the preceding chapter, all high-voltage module components with the exception of the high-voltage transformer are placed in an aluminium enclosure (box). Again, the box is floating with respect to the oil tank walls (i.e., ground) with the capacity to withstand 160 $kV_{dc}$ for 1 minute. The components inside the box operate at 26 kV with respect to the enclosure and are designed to handle 50 $kV_{dc}$ for 1 minute. The effects of the box are evaluated through finite element analysis in section 9.2.

*Common mode inductor*

As described in section 8.2.3, in contrast to the reduced-scale prototype module, the common mode inductor is here implemented as a single component. Again, a VITROPERM 500F nanocrystalline core is used. Here, the magnetic cross-sectional area is ~40x40 $mm^2$, the magnetic length is ~780 mm, and the relative permeability is on the order of ~30000, [9.20]. Each winding comprises 44 turns, wound with the same type of rectangular enamelled copper wire used in winding the high-voltage high-frequency transformer secondary windings, above. The resulting common mode inductance is ~100 mH. The common mode inductor is studied in magnetostatic and electrostatic conditions using finite element analysis in section 9.2.

*High-voltage rectifier*

Each rectifier board contains four fast-switching diodes (DSEP90-12AZ; 1.2 kV, 90 A) from IXYS, [9.21]. Additionally, each diode is equipped with RC snubber (3x10 Ω, 33 nF), bleeder resistor (2x240 kΩ) and MOV according to the description given in section 5.3.5. The rectifier is formed by a total of 42 rectifier boards mounted around a central insulating rod. Again, note that the outer edges of each rectifier board are equipped with 4 mm copper anti-corona rings for field control. The high-voltage rectifier is studied in electrostatic conditions using finite element analysis in section 9.2.

*High-voltage filter inductor*

As in the reduced-scale prototype, the high-voltage filter inductor core is based on conventional silicon electrical steel. The core is tape-wound using typical thickness of 0.25 mm and the magnetic cross-sectional area is ~85x120 $mm^2$. The core is cut in two U-shaped sections in facilitating inductor winding. Here, spacers of ~7.0 mm are introduced between the two core sections in defining the inductor air gap. The cores are mounted on and strapped to the fiberglass frames. The two windings are series connected, and each winding is made up of 42 turns. Again, the same type of copper wire used in winding the high-voltage high-frequency transformer secondary windings is used. The resulting differential-mode inductance is ~8.2 mH. The high-voltage filter inductor is studied in magnetostatic and electrostatic conditions using finite element analysis in section 9.2.

*High-voltage filter capacitor branches*

The capacitor branches of the output filter are again based on the UHV-12A (50 kV, 1700 pF) from TDK, [9.22]. In this case, the undamped branch is comprised of eight capacitors and the damped branch is comprised of 20 capacitors. The filter damping resistors, HVI 968.3, were selected from the Metallux high-voltage impulse resistor series, [9.23]. Additionally, each branch is equipped with bleeder resistors (MOX-5-13) from Ohmite, [9.24].

### 9.1.3 High-power resistive load

To evaluate the developed prototype converter chain at rated conditions, a high-power resistive load was required. In this case, with system output voltage on the order of 20 kV (i.e., taking into account voltage drops) and rated current of 100 A, a load resistance of ~200 Ω was needed. Of course, such a load would be required to handle the imposed high-voltage requirements as well as the associated load power dissipation of ~100 kW. Due to time constraints, it was decided to design and construct the load in-house. It was also decided that the load should be designed considering forced air cooling. Finally, two pre-existing load resistors of 100 Ω with the capacity of dissipating up to ~20 kW each were at disposal.

Based on the above and considering the availability of high-power resistors, the load design presented in Figure 9.13 was proposed. This design includes the two pre-existing resistive loads. The rest of the load is made up of a bank of resistors housed in standard electrical cabinets. Here, sixteen power resistors (TE1500B47RJ; 47 Ω, 1.5 kW) from TE Connectivity are mounted between fiberglass pieces affixed to the cabinet mounting plate as well as aluminium profiles close to the cabinet floor and roof by high-voltage isolators (ISORES 3120351; rated 24 kV). The fiberglass pieces are machined with large holes to facilitate air flow and electrical interconnection of resistor terminals, and with small holes to permit mechanical connection of the resistors. As shown in Figure 9.14, the cabinet doors are fitted with industrial fans (W2E250-HQ52-12 from ebm-papst). Additionally, the roof itself is removed to facilitate cooling. Finally, the resistors were interconnected with silicon-based high-voltage cable. The cabinets were interconnected by feedthroughs installed in the cabinet walls, Figure 9.14.

Interconnecting the resistor banks of these cabinets as shown in Figure 9.13 results in two cabinets with equivalent resistance ~35 Ω and one cabinet with equivalent resistance ~47 Ω. Hence, the total resistance would be the required ~197 Ω. Here, the power dissipation per 47 Ω resistor is ~1470 W, corresponding to a total cabinet power dissipation of ~17.6 kW for cabinets 3 and 4, and to ~23.5 kW for cabinet 5.

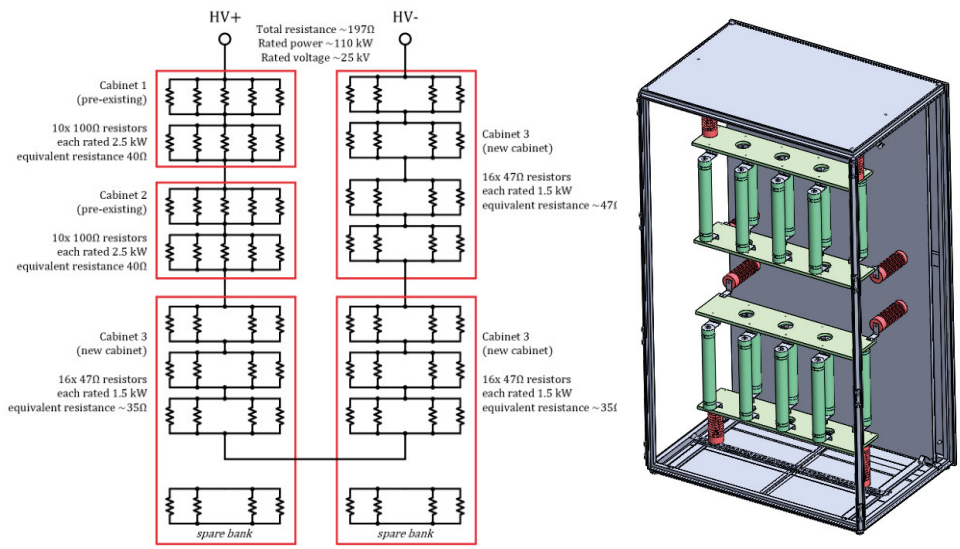
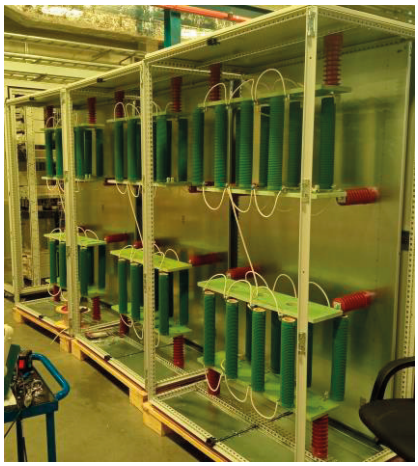



Figure 9.13: Overview of high-power resistive load, left) conceptual schematics; right) conceptual 3D drawing



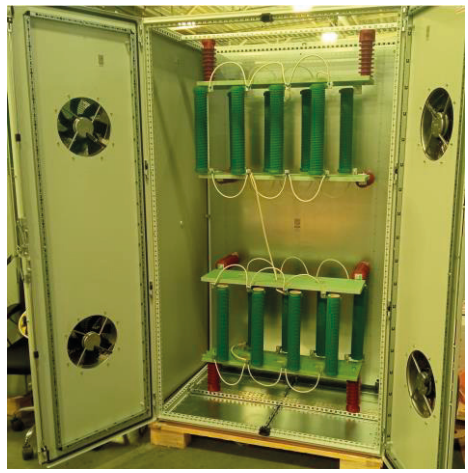


Figure 9.14: Construction of high-power resistive loads, left) assembly in test stand at ESS; right) complete interconnected load assembly with industrial fans for cooling and high-voltage feedthroughs.

## 9.2 Simulation of prototype converter chain

This section is divided into two main parts. The first part, comprising sections 9.2.1-9.2.4, treats finite element analysis of the components comprising the high-voltage module. Component modeling including meshing and physics set-up is described in detail for each component. Both electrostatic and magnetostatic conditions are considered, and the derived results are linked back to the equivalent circuits models developed in chapter 5. Then, the second part, section 9.2.5, integrates the derived circuits with power electronic converter models in developing a complete system model suitable for circuit simulation. Simulated circuit performance is assessed, and validated experimentally in section 9.3.

### 9.2.1 High-voltage high-frequency transformer

*Electrostatic simulation: model setup*

The HVHF transformer is first simulated in electrostatic condition. The purpose of this simulation is to 1) ensure that proper isolation distance is maintained internally as well as with respect to surrounding components, and to 2) quantify the parasitic capacitive elements. In this case, both the HV box as well as a surrounding enclosure (representing the surroundings, e.g., oil tank walls, adjacent modules, etc) must be included. These simulations are based on a complete 3D representation of the developed high-voltage module. To reduce complexity and improve simulation time, the 3D model was simplified in accordance with Figure 9.15. Here, all

components inside the HV box have been removed. Furthermore, both primary and secondary windings have been replaced with sheets. All other non-essential components have also been removed. Model materials were then defined as indicated in Figure 9.16. Here, considering electrostatic conditions, all 'metallic parts', including the surrounding enclosure and box (aluminium) and the magnetic cores (nanocrystalline), have been defined as copper. Finally, the meshed geometry shown in Figure 9.17 was created. Here, care was taken in defining a mesh fine enough to enable detailed analysis of the electrostatic field close to points of interest such as winding edges, core corners and wires of small diameters while representing reasonable simulation time. To accomplish this, the mesh has deliberately been made significantly coarser for insulating materials (e.g., fiberglass) and in areas where the field may be expected to be either low or constant.

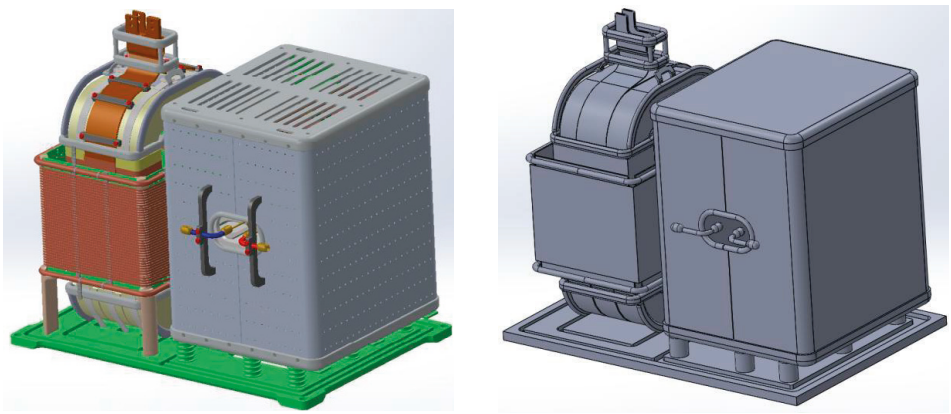


Figure 9.15: Simplification of HVHF transformer geometry for finite element analysis in electrostatic condition

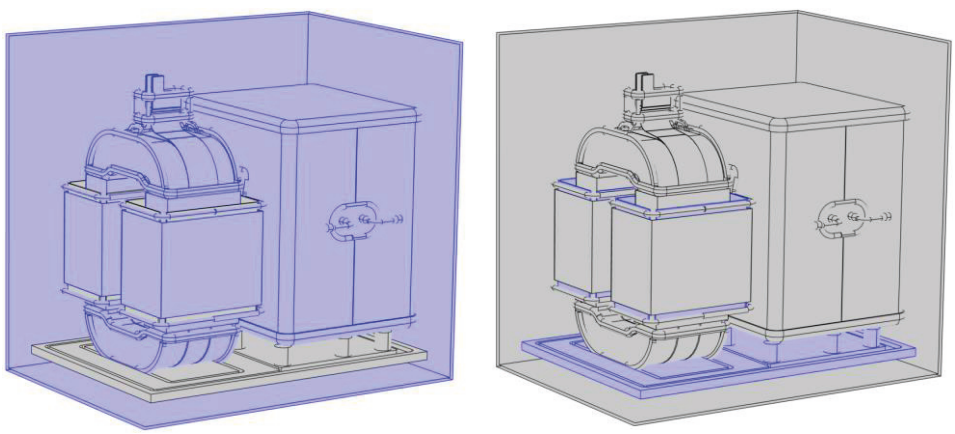


Figure 9.16: Material setup for HVHF transformer for finite element analysis in electrostatic condition

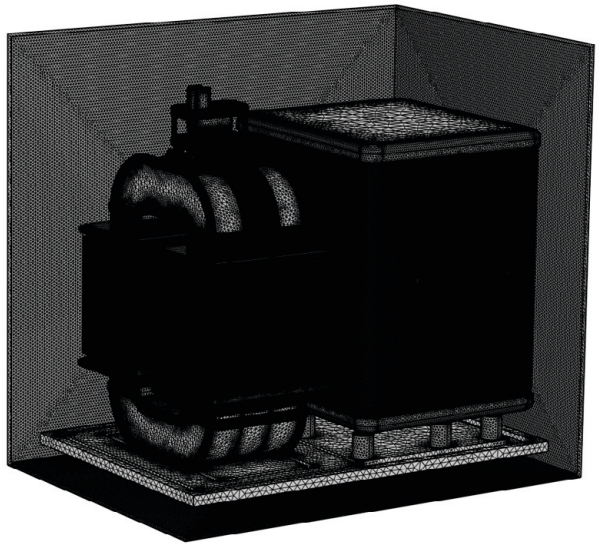


Figure 9.17: Meshed HVHF transformer geometry for finite element analysis

*Electrostatic simulation: worst-case field distribution*

First, while in reality the electrostatic potential varies along the transformer windings, it was of interest to study the electrostatic field distribution under 'worst-case' conditions in which the transformer secondary windings, the anti-corona rings, connecting wires and connectors as well as the high-voltage box are all placed at nominal output voltage (i.e., 115 kV). The primary windings, anti-corona cages and connectors, as well as the magnetic cores and surrounding oil tank enclosure are placed at ground potential. All insulators, e.g., the fiberglass baseplate and winding supports are left floating. This set-up is depicted in Figure 9.18.

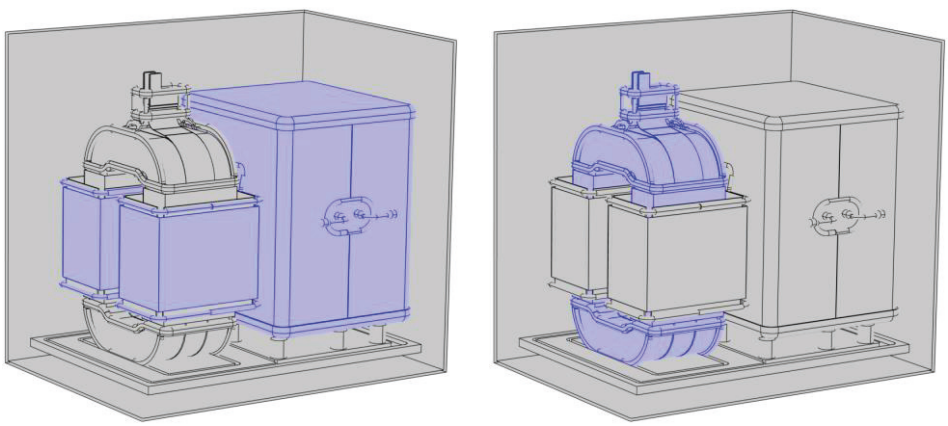


Figure 9.18: Electrostatic potential setup for HVHF transformer in calculating worst-case electrostatic field distribution

Simulation of the above-described model yields results exemplified in Figure 9.19. Here, the simulated electrostatic field distribution in the plane defined by the upper anti-corona ring on the secondary winding in top-down view is shown. From this figure, it may be verified that the electrostatic field strength – in this part of the geometry – never exceeds that of 8 kV/mm. The corresponding electrostatic field distribution was visualized at multiple points of interest as indicated in Figure 9.20 and summarized in Table 9.1. Most importantly, keeping in mind that this model represents the 'worst-case' condition, this analysis verifies that the electrostatic field strength never exceeds the limiting value of 10 kV/mm. Based on these results, it was concluded that the design was satisfactory from the perspective of electrostatics.

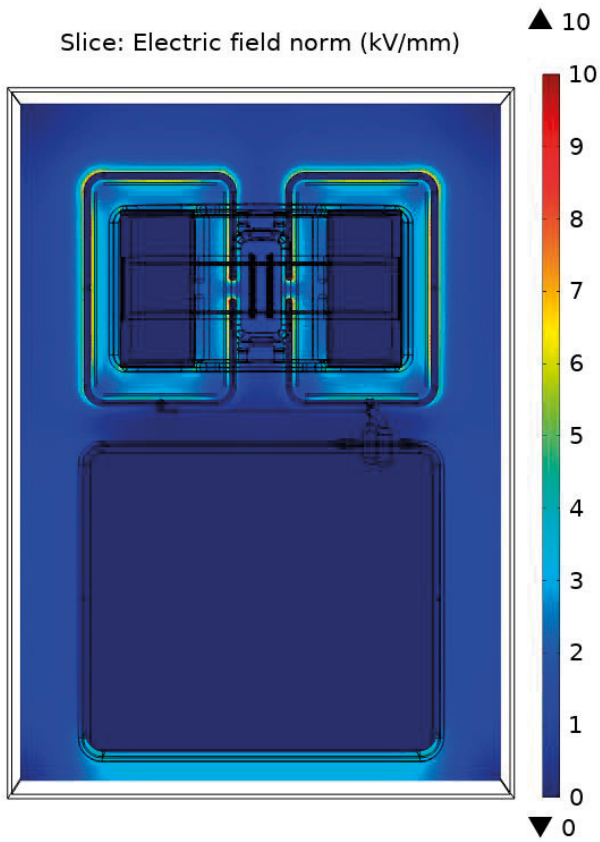



Figure 9.19: Example of field simulation

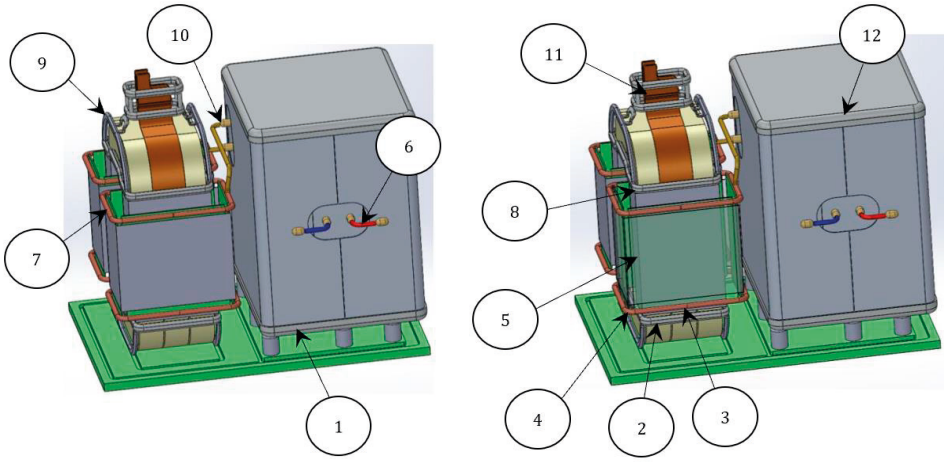



Figure 9.20: Points of interest

**Table 9.1: Electrostatic field strength at points of interest identified in Figure 9.20**

| Point | Description | Field strength [kV/mm] |
|---|---|---|
| 1 | Lower end of high-voltage box | ~2 |
| 2 | Lower anti-corona cage | < 5 |
| 3 | Lower edge of primary winding | ~4 |
| 4 | Lower anti-corona rings | < 8 |
| 5 | Middle of primary windings | 8-10 |
| 6 | Connectors at output of high-voltage module | ~9 |
| 7 | Upper anti-corona rings | ~7-8 |
| 8 | Upper edge of primary windings | ~6-7 |
| 9 | Upper anti-corona cage | ~5 |
| 10 | Connectors at input of high-voltage box, straight section | ~6 |
| 11 | Connectors to primary stage | < 1 |
| 12 | Upper end of high-voltage box | ~2 |

*Electrostatic simulation: calculation of parasitic capacitance*

The procedure to analytically calculate the stray capacitive elements of the high-voltage high-frequency transformer geometry was described in section 5.3.4 and the

derived equivalent circuit model was shown in Figure 5.28. There, the stray capacitive elements were divided between those derived from the electrical field present between 1) the secondary and primary transformer windings and 2) the secondary transformer winding and ground, e.g., the surrounding tank walls. To verify these calculations, the electrostatic potential setup shown in Figure 9.18 was modified such that, primarily, the potential varies along the transformer windings (as is the case in practice). Then, the electrostatic energy stored in the volumes associated with the identified capacitive elements was calculated by integration. The analytically calculated values are compared to those derived from finite element analysis in Table 9.2.

**Table 9.2: Comparison of high-voltage high-frequency transformer capacitance values derived from analytical equations and using finite element analysis**

| Capacitive element | Capacitance (analytic) [pF] | Capacitance (FEA) [pF] | Estimation error [%] |
|---|---|---|---|
| $\sum C_{ps}$ | 61.2 | 65.8 | -7.0 |
| $\sum C_{sg}$ | 29.9 | 33.2 | -9.9% |

*Magnetostatic simulation: model setup*

The HVHF transformer was then simulated in magnetostatic condition. The purpose of this simulation is to 1) ensure that the magnetic flux density never exceeds the limits of the core material, and to 2) quantify the leakage and magnetization inductance values. In this case, it is sufficient to model only the transformer. Additionally, all objects not constituting either a winding arrangement or magnetic material may be removed. However, the transformer windings were modelled in full detail in ensuring maximally accurate field descriptions. Finally, a part of each magnetic core was removed in accounting for magnetic fill factor in accordance with that specified in the datasheet. The resulting simplified transformer geometry is shown in Figure 9.21. Model materials were then defined as indicated in Figure 9.21, and the meshed geometry is shown in Figure 9.22. Note that the developed mesh is significantly coarser than that shown in Figure 9.17. This is possible due to the very high relative permeability of the magnetic core material. Still, a fine mesh was developed in the vicinity of transformer windings in capturing the details of the generated flux leakage.

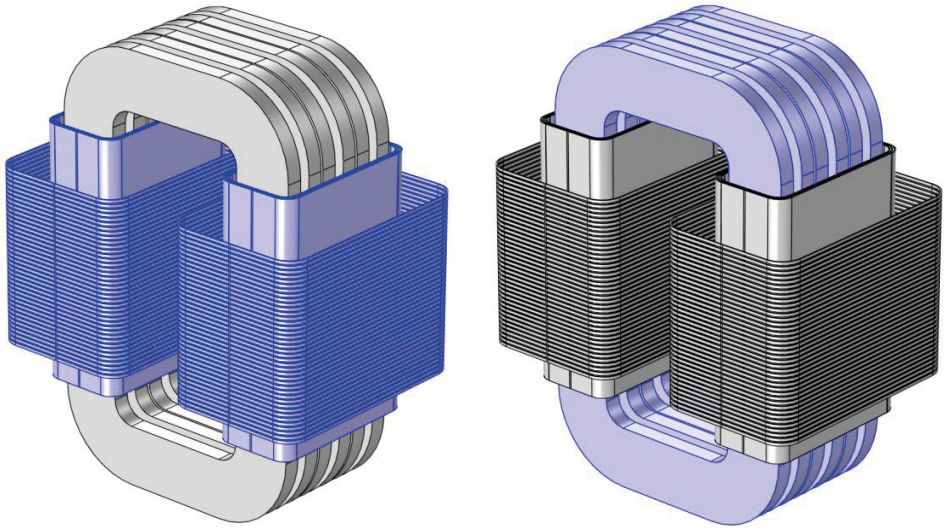


Figure 9.21: Material setup for HVHF transformer for finite element analysis in magnetostatic condition

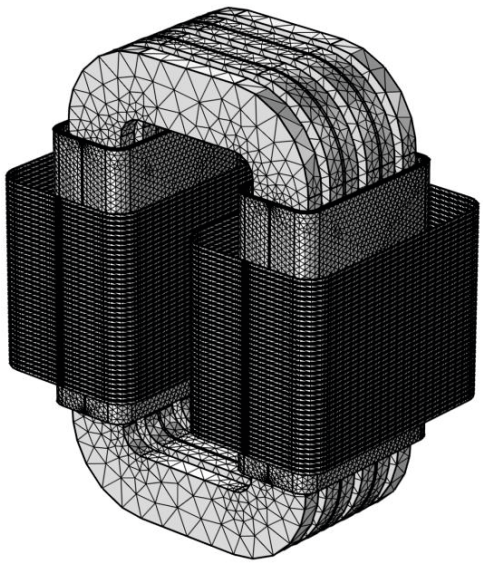


Figure 9.22: Meshed HVHF transformer geometry for finite element analysis

*Magnetostatic simulation: open circuit condition*

Open circuit condition is simulated by setting the secondary winding current to zero. The magnetization inductance is estimated as follows. First, for a linear core material, the primary winding current may be set arbitrarily. Then, integration of the magnetic energy density over the core volume yields the magnetization inductance

through the relationship $L'_m = \left(2/I_p^2\right) \cdot \int \rho_m dV$, where $\rho_m$ is the magnetic energy density. The associated 'true' primary-side magnetization current may then be estimated through $i'_m = V_p/\left(4L'_m f_{sw,HB}\right)$. Re-simulating the model, applying $I_p = i'_m$ yields the simulation results presented in Figure 9.23. Here, $L'_m = 1.15\,mH$, $i'_m = 11.1\,A$ and the corresponding $\hat{B} = 0.62\,T$. The estimated magnetic flux density is well in agreement with the simulated value. Importantly, the simulated peak magnetic flux density is within the range of linearity according to core material datasheets provided by the manufacturer, and is well below saturation.

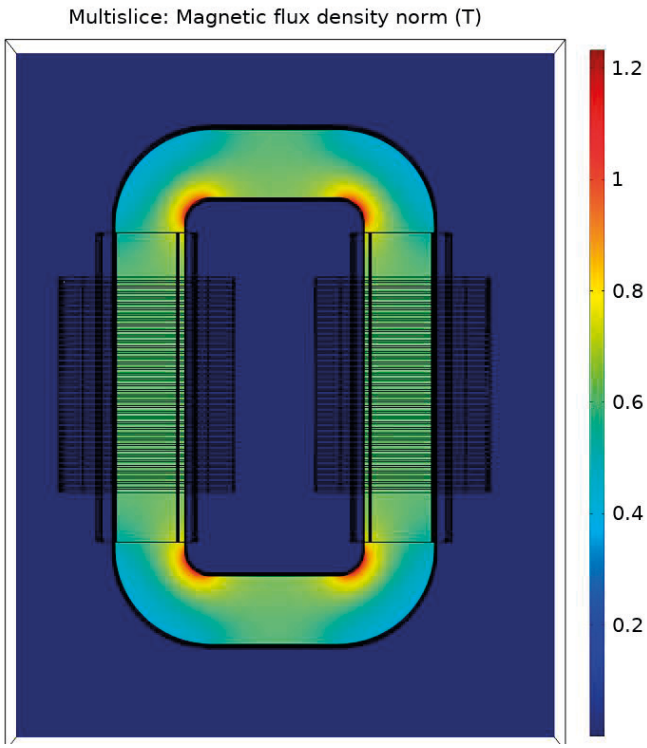



Figure 9.23: Transformer magnetic flux density distribution in open circuit condition calculated using derived magnetization current

*Magnetostatic simulation: short circuit condition*

Short circuit condition is simulated by setting the secondary winding currents to the nominal output current $I_2$ and the primary winding currents such that the core flux cancels. Simulation results obtained under these conditions are shown in Figure 9.24. As can be seen, the core flux has been reduced to close to zero and the majority of the stored energy is found in-between the windings. Integration of the magnetic energy density over the simulation volume allows calculation of the associated

leakage inductance referred to the secondary from $L_s'' = (2/I_2^2) \cdot \int \rho_m dV$. Here, the total leakage inductance was simulated to be 430 µH. Notably, the corresponding value estimated analytically through (5.102) is 428 µH, i.e., within 1%.

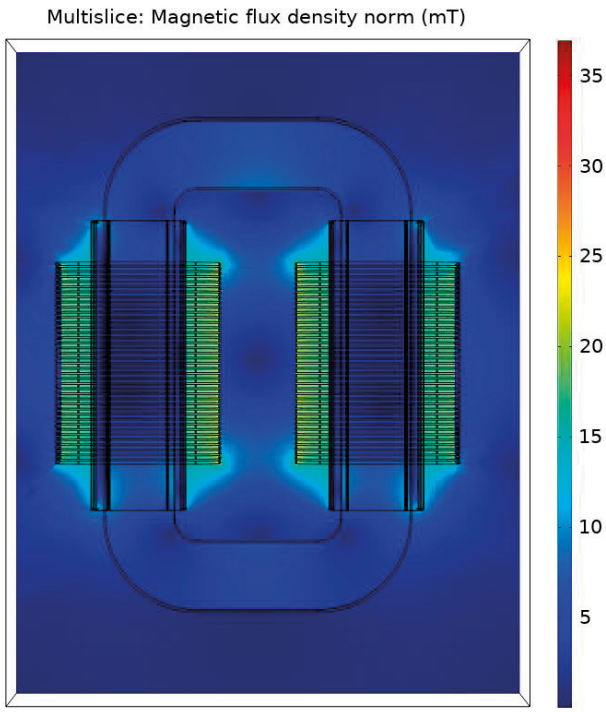



Figure 9.24: Transformer magnetic flux density distribution in short circuit condition applying nominal load currents

## 9.2.2 Common mode inductor

*Electrostatic simulation: model setup*

The common mode inductor is first simulated in electrostatic condition. The purpose of this simulation is to 1) ensure that proper isolation distance is maintained internally as well as with respect to surrounding components, and to 2) quantify the parasitic capacitive elements. Here, a surrounding enclosure representing surrounding high-voltage module components must be included. Importantly, two simulation cases derived from two switch states yielding unique electrostatic field distributions are required for a complete study. Again, these simulations are based on a complete 3D representation of the component. To reduce complexity and improve simulation time, the 3D model was simplified in accordance with Figure 9.25, in which, e.g., the two inductor windings have been replaced with sheets.

Model materials were then defined as indicated in Figure 9.26. Again, all ‘metallic parts’ have been defined as copper for simplicity. The meshed geometry is shown in Figure 9.27.

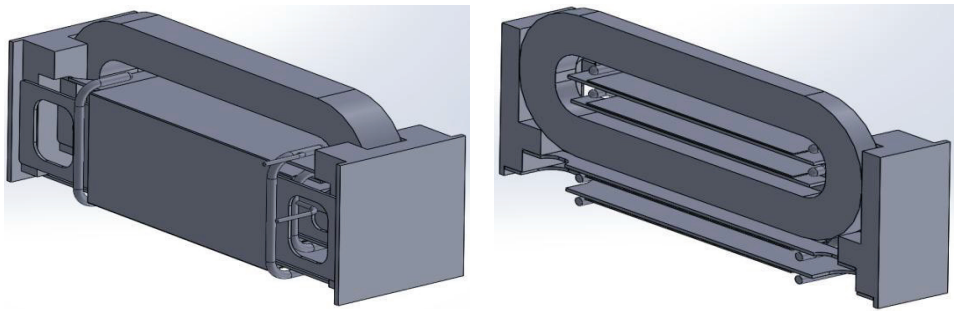


Figure 9.25: Simplification of common mode inductor geometry for finite element analysis in electrostatic condition

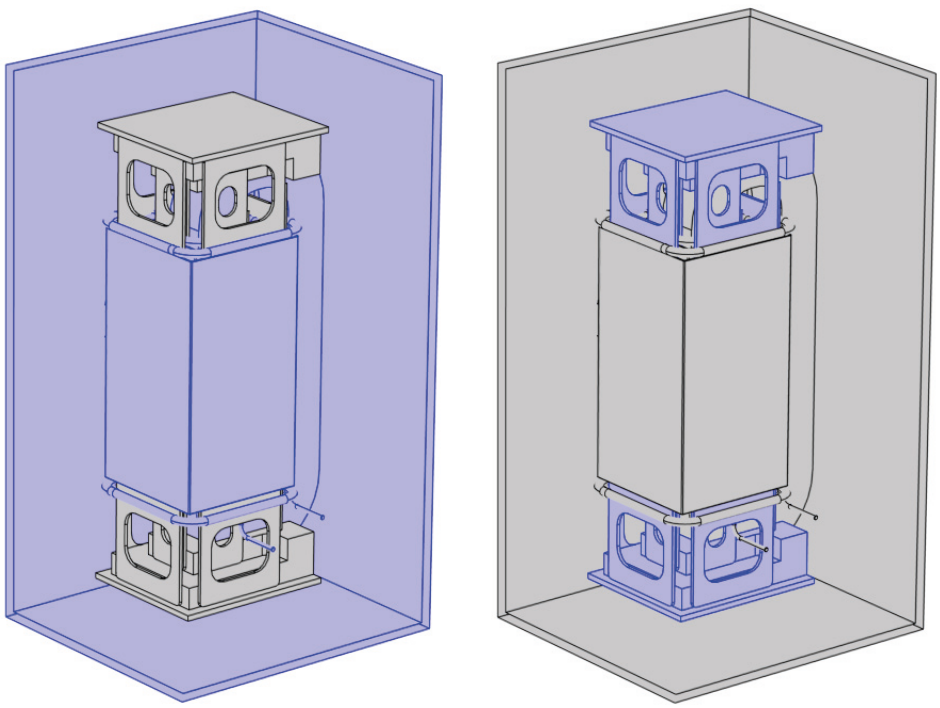


Figure 9.26: Material setup for common mode inductor for finite element analysis in electrostatic condition

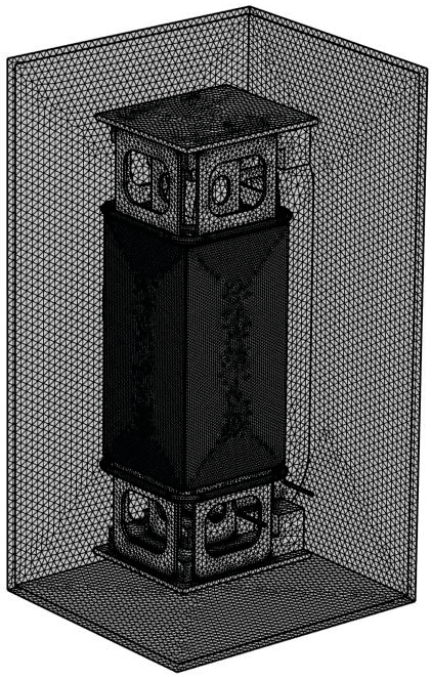


Figure 9.27: Meshed common mode inductor geometry for finite element analysis

*Electrostatic simulation: field distribution (case 1)*

The first case arises when the inductor input is driven by the source such that a potential difference exists between the internal and external windings. By design, this potential difference is limited to that of 26 kV. As described for the HVHF transformer, above, it is of interest to study the worst possible field distribution. In considering this case, the external winding as well as the associated anti-corona rings and connecting wires are set to a potential of 26 kV. Correspondingly, the internal winding, the associated anti-corona rings and connecting wires as well as the magnetic core and surrounding enclosure are set to ground potential. All insulators are left floating. This model set-up is depicted in Figure 9.28.

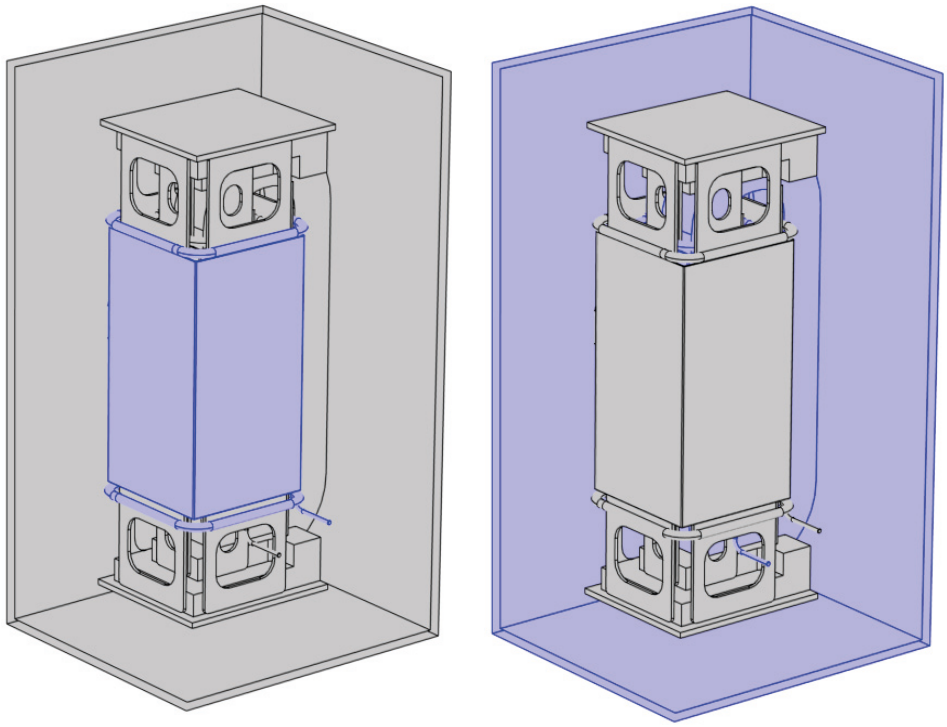


Figure 9.28: Electrostatic potential setup for common mode inductor in calculating electrostatic field distribution for ‘case 1’

Simulation of the above-described model yields results exemplified in Figure 9.29. Here, the simulated electrostatic field distribution in the plane defined by the upper anti-corona ring on the external winding in top-down view is shown. From this figure, it may be verified that the electrostatic field strength – in this part of the geometry – never exceeds that of 6 kV/mm. The corresponding electrostatic field distribution was visualized at multiple points of interest as indicated in Figure 9.30 and summarized in Table 9.3. It is verified that the electrostatic field strength never exceeds the limiting value of 10 kV/mm.

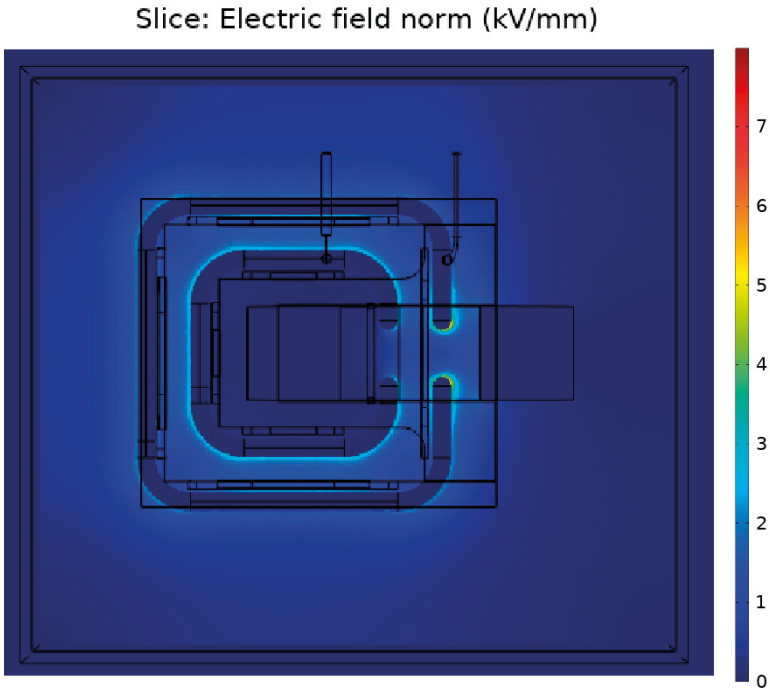



Figure 9.29: Example of field simulation

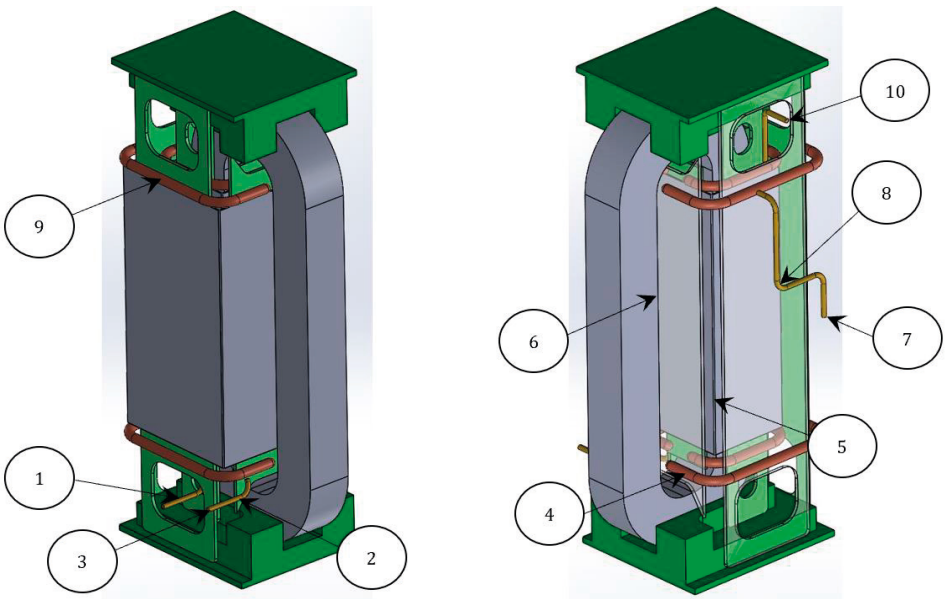



Figure 9.30: Points of interest (case 1)

Table 9.3: Electrostatic field strength at points of interest identified in Figure 9.30

| Point | Description | Field strength [kV/mm] |
|---|---|---|
| 1 | Small wire connected to internal winding | < 2 |
| 2 | Small wire connected to external winding, straight section | < 4 |
| 3 | Small wire connected to external winding, termination | ~6-8 |
| 4 | Lower external anti-corona rings, close to core | ~5 |
| 5 | Corners of internal winding | < 7 |
| 6 | Corners of magnetic core (part external to windings) | < 3 |
| 7 | Small wire connected to external winding, termination | < 8 |
| 8 | Small wire connected to external winding, straight section | < 4 |
| 9 | Upper anti-corona rings | < 6 |
| 10 | Small wire connected to internal winding, termination | ~2 |

*Electrostatic simulation: field distribution (case 2)*

The second case arises when the potential difference between the internal and external windings is zero, but – due to the use of a virtual ground – there still exists a potential between both windings and the virtual ground. This potential difference is again limited to that of 26 kV. The adjusted model is set-up according to that shown in Figure 9.31.

Simulation of the above-described model yields results exemplified in Figure 9.32. It is again verified that the electrostatic field strength – in this part of the geometry – never exceeds that of 6 kV/mm. The corresponding electrostatic field distribution was visualized at multiple points of interest as indicated in Figure 9.33 and summarized in Table 9.4. It is verified that the electrostatic field strength never exceeds the limiting value of 10 kV/mm.

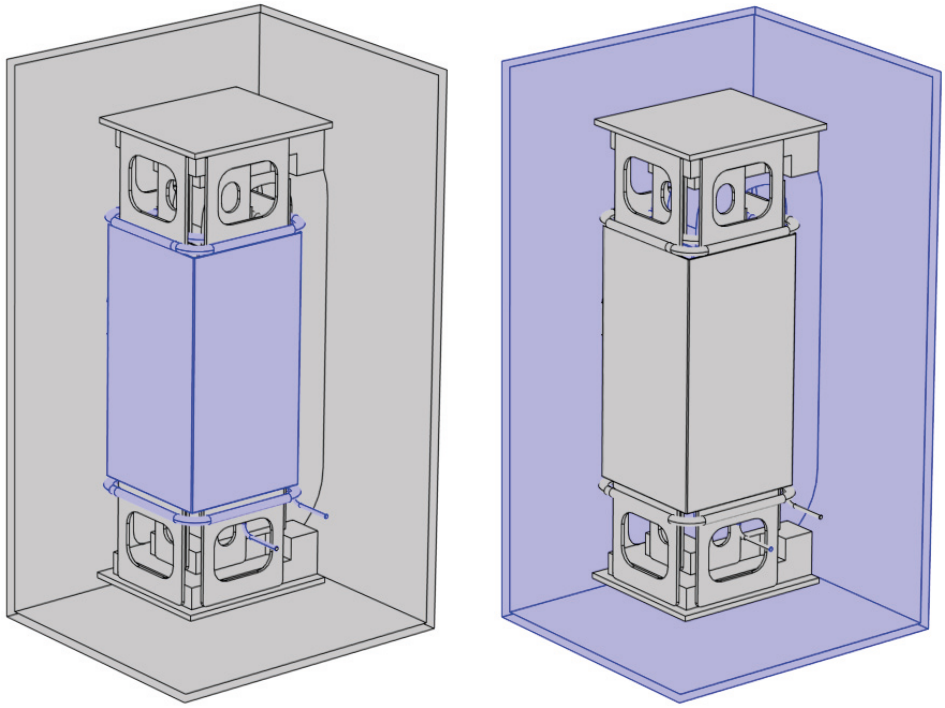


Figure 9.31: Electrostatic potential setup for common mode inductor in calculating electrostatic field distribution for ‘case 2’

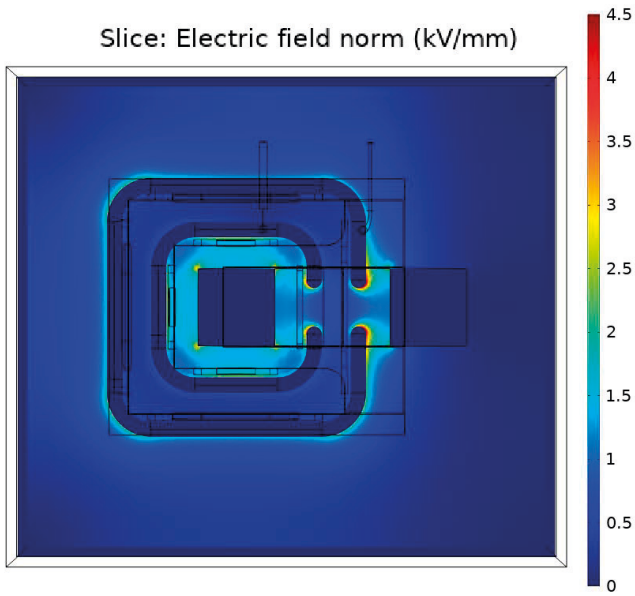



Figure 9.32: Example of field simulation

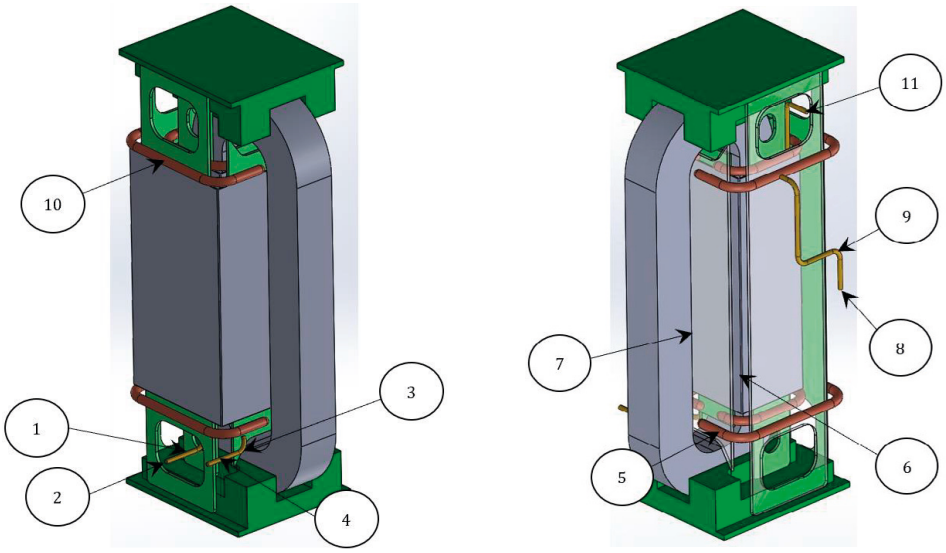



Figure 9.33: Points of interest (case 2)

**Table 9.4: Electrostatic field strength at points of interest identified in Figure 9.33**

| Point | Description | Field strength [kV/mm] |
|---|---|---|
| 1 | Small wire connected to internal winding, straight section | < 4 |
| 2 | Small wire connected to internal winding, termination | < 9 |
| 3 | Small wire connected to external winding, straight section | ~4 |
| 4 | Small wire connected to external winding, termination | < 9 |
| 5 | Lower external anti-corona rings, close to core | ~5 |
| 6 | Corners of magnetic core (part internal to windings) | ~3-4 |
| 7 | Corners of magnetic core (part external to windings) | < 3 |
| 8 | Small wire connected to external winding, termination | < 6 |
| 9 | Small wire connected to external winding, straight section | < 4 |
| 10 | Upper anti-corona rings | ~5 |
| 11 | Small wire connected to internal winding, termination | < 8 |

*Electrostatic simulation: calculation of parasitic capacitance*

The procedure to analytically calculate the stray capacitive elements of the high-voltage common mode inductor geometry was described in section 5.3.7 and the derived equivalent circuit model was shown in Figure 5.43. There, the stray capacitive elements were divided among those derived from the electrical field present between 1) the external inductor winding and the surroundings, 2) the external and internal inductor windings, and 3) the internal inductor winding and the (virtually grounded) magnetic core. To verify these calculations, the electrostatic potential setups shown in Figure 9.28 Figure 9.31 were modified such that, primarily, the potential varies along the inductor windings (as is the case in practice). Then, the electrostatic energy stored in the volumes associated with the identified capacitive elements was calculated by integration. The analytically calculated values are compared to those derived from finite element analysis in Table 9.5.

**Table 9.5: Comparison of high-voltage common mode inductor stray capacitance values derived from analytical equations and using finite element analysis**

| Capacitive element | Capacitance (analytic) [pF] | Capacitance (FEA) [pF] | Estimation error [%] |
|---|---|---|---|
| $\sum C_{CM-e-i}$ | 17.4 | 19.3 | -9.8% |
| $\sum C_{CM-e}$ | 12.7 | 13.1 | -3.1% |
| $\sum C_{CM-i}$ | 16.6 | 15.3 | 8.5% |

*Magnetostatic simulation: model setup*

The common mode inductor was then simulated in magnetostatic condition. The purpose of this simulation is to 1) ensure that the magnetic flux density never exceeds the limits of the core material, and to 2) quantify the common mode and differential mode inductance values. In this case, it is sufficient to model only the inductor. Again, as with the transformer, 1) all objects not constituting either a winding arrangement or magnetic material was removed, 2) the windings were modelled in full detail in ensuring maximally accurate field descriptions, and 3) part of the magnetic core was removed in accounting for magnetic fill factor. The resulting simplified inductor geometry is shown in Figure 9.34. Model materials were then defined as indicated in Figure 9.35, and the meshed geometry is shown in Figure 9.36.

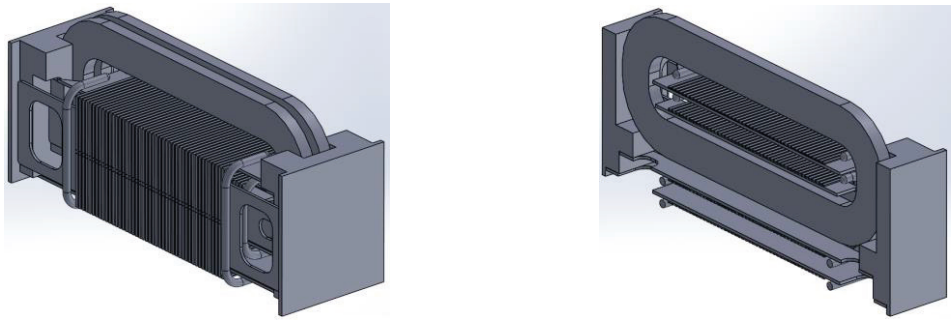


Figure 9.34: Simplification of common mode inductor geometry for finite element analysis in magnetostatic condition

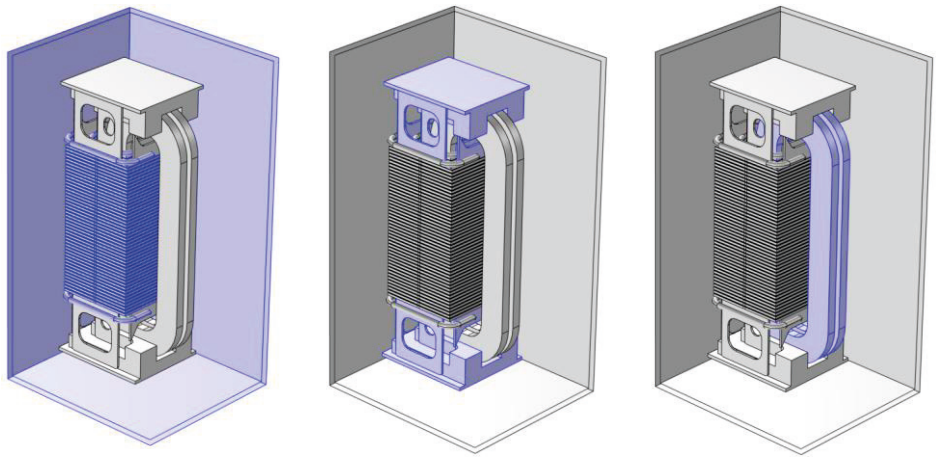


Figure 9.35: Material setup for common mode inductor for finite element analysis in magnetostatic condition

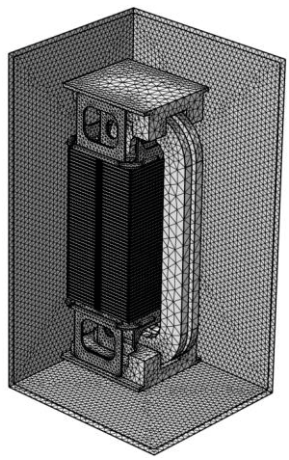


Figure 9.36: Meshed common mode inductor geometry for finite element analysis

*Magnetostatic simulation: common mode excitation*

In common mode excitation, the current in both windings is set such that they produce flux in the same (common) direction. In practice, it is difficult to know precisely what the common mode component of the load current waveform will be. Here, it is set to $\hat{\imath}_{cm}$ according to that described in section 5.3.7. The resulting magnetic flux density distribution is shown in Figure 9.37. As can be seen, the entirety of the flux is confined to the core. Hence, the common mode inductance may be calculated from $L_{cm} = \left(2/{\hat{\imath}_{cm}}^2\right) \cdot \int \rho_m dV$. In this case, $L_{cm} = 105\ mH$, matching that of the design value within 1%. Also note that the magnetic flux density is well within the limits of the VITROPERM 500F core material.

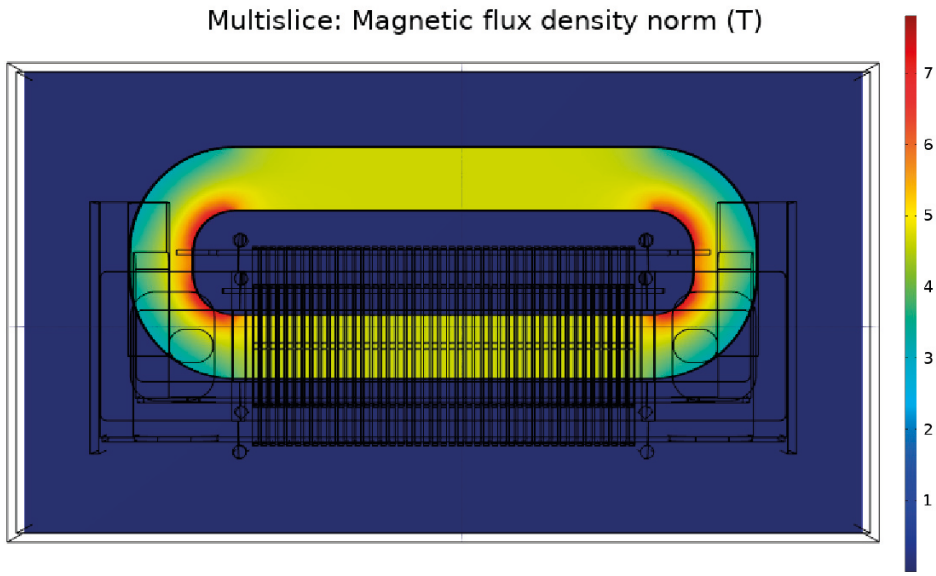



Figure 9.37: Common mode inductor magnetic flux density distribution under common mode current excitation

*Magnetostatic simulation: differential mode excitation*

In differential mode excitation, the current in the windings is set such that they produce flux in the opposite (differential) direction. Here, the current is set to equal the nominal load current. Of course, with the same number of turns on the external and internal windings and with the same amount of current in both windings, the generated magnetic flux should be zero. However, as indicated by the simulation results presented in Figure 9.38, this is strictly not true due to leakage effects. While the flux density distribution resembles that of the HVHF transformer, Figure 9.24, a fundamental difference is that the common mode inductor only has a single winding set. Consequently, the leakage flux may close by returning via the air or by

way of the magnetic material, giving rise to the flux density plot shown in Figure 9.38. Regardless, the peak magnetic flux density is well below the limits of the core material. Finally, the resulting differential mode inductance may be calculated from $L_{dm} = (2/I_2^2) \cdot \int \rho_m dV = 85.2\ \mu H$. Note that the residual $L_{dm}$ is less than 0.1% of the targeted design value $L_{cm}$.

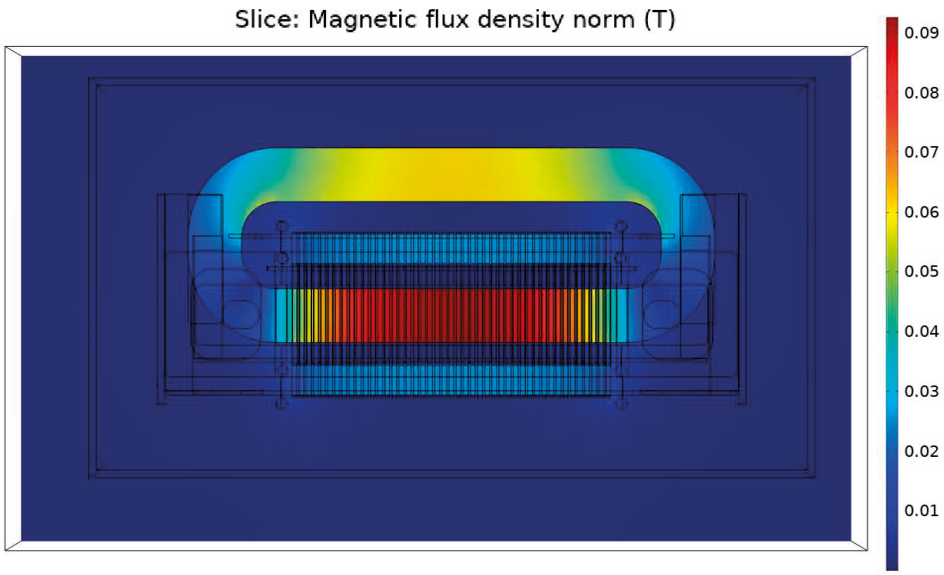



Figure 9.38: Common mode inductor magnetic flux density distribution under differential mode current excitation

### 9.2.3 High-voltage rectifier

*Electrostatic simulation: model setup*

The high-voltage rectifier is simulated in electrostatic condition. The purpose of this simulation is to 1) ensure that proper isolation distance is maintained internally as well as with respect to surrounding components, and to 2) quantify the parasitic capacitive elements. Here, a surrounding enclosure representing surrounding high-voltage module components must be included. Again, modeling is based on a complete 3D representation of the component. To reduce complexity and improve simulation time, the 3D model was simplified in accordance with Figure 9.39, in which, e.g., all rectifier components have been removed. Model materials were then defined as indicated in Figure 9.40, and the meshed geometry is shown in Figure 9.41.

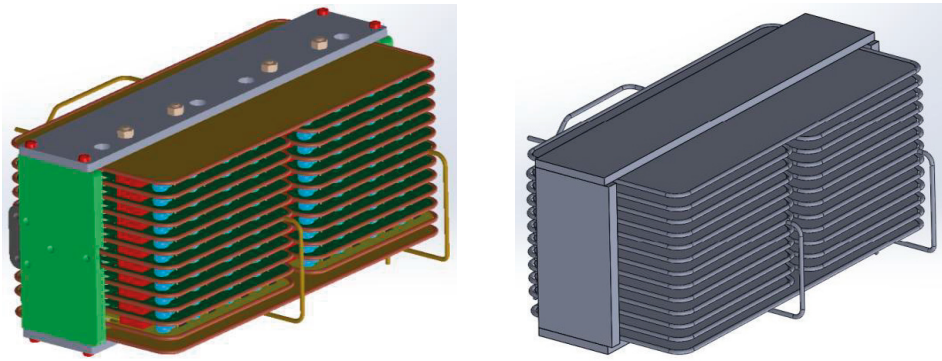


Figure 9.39: Simplification of high-voltage rectifier geometry for finite element analysis in electrostatic condition

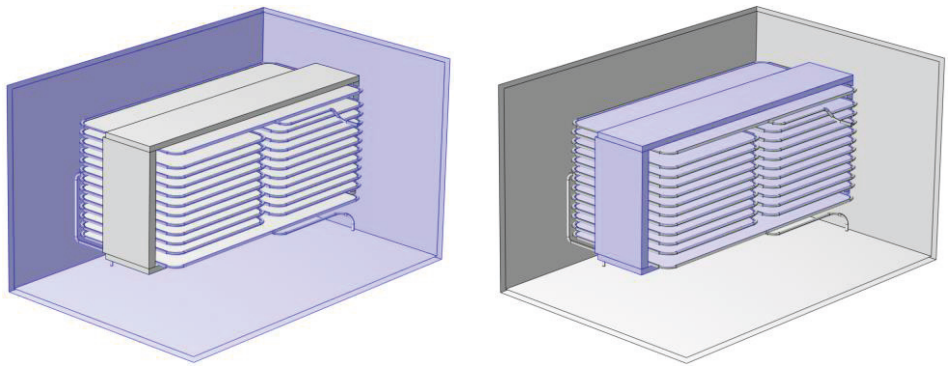


Figure 9.40: Material setup for high-voltage rectifier for finite element analysis in electrostatic condition

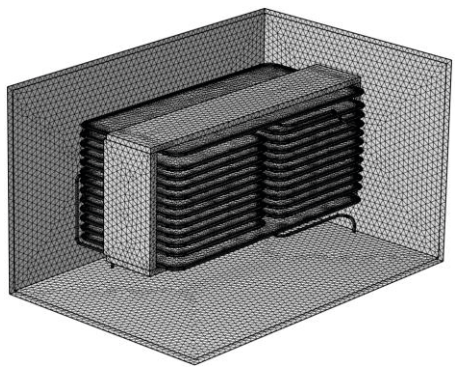


Figure 9.41: Meshed high-voltage rectifier geometry for finite element analysis

*Electrostatic simulation: worst-case field distribution*

The electrostatic potential of the individual rectifier boards (i.e., in this case essentially the anti-corona rings) is set-up according to the description given in section 5.3.5. The surrounding enclosure is set to ground potential. Simulation of the above-described model yields the results exemplified in Figure 9.42. Additionally, as in this type of simulation the high voltage rectifier geometry is essentially comprised by the set of anti-corona rings, it is possible to visualize the electrostatic field strength at all critical points simultaneously. It is verified that the electrostatic field strength never exceeds that of 5 kV/mm, and is well below the limit value of 10 kV/mm.

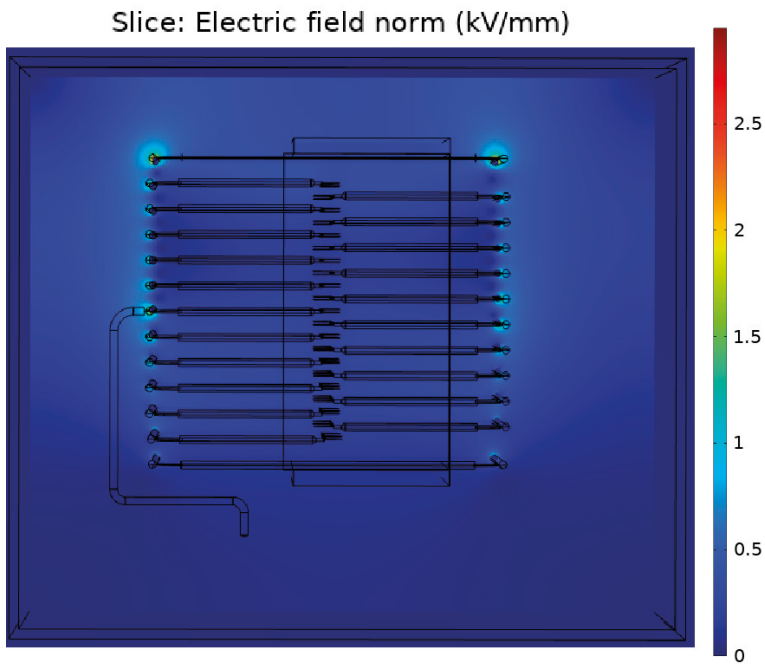



Figure 9.42: Example of field simulation

*Electrostatic simulation: calculation of parasitic capacitance*

The procedure to analytically calculate the stray capacitive elements of the high-voltage rectifier geometry was described in section 5.3.5 and the derived equivalent circuit model was shown in Figure 5.33. There, it was argued that the majority of stored electrostatic energy may be assigned to a single capacitive element $C_{HVR}$. Thus, this capacitance is straightforwardly estimated by integrating the electrostatic energy stored in the entire geometry. The analytically calculated value is compared to that derived from finite element analysis in Table 9.6.

Table 9.6: Comparison of high-voltage rectifier stray capacitance values derived from analytical equations and using finite element analysis

| Capacitive element | Capacitance (analytic) [pF] | Capacitance (FEA) [pF] | Estimation error [%] |
|---|---|---|---|
| $\sum C_{HVR}$ | 109.2 | 106.4 | 2.6 |

### 9.2.4 High-voltage inductor

*Electrostatic simulation: model setup*

The high-voltage inductor is first simulated in electrostatic condition. The purpose of this simulation is to 1) ensure that proper isolation distance is maintained internally as well as with respect to surrounding components, and to 2) quantify the parasitic capacitive elements. Here, a surrounding enclosure representing surrounding high-voltage module components must be included. Importantly, two simulation cases derived from two switch states yielding unique electrostatic field distributions are required for a complete study. Again, these simulations are based on a complete 3D representation of the component. To reduce complexity and improve simulation time, the 3D model was simplified in accordance with Figure 9.43, in which, e.g., the two inductor windings have been replaced with sheets. Model materials were then defined as indicated in Figure 9.43. Again, all 'metallic parts' have been defined as copper for simplicity. The meshed geometry is shown in Figure 9.44.

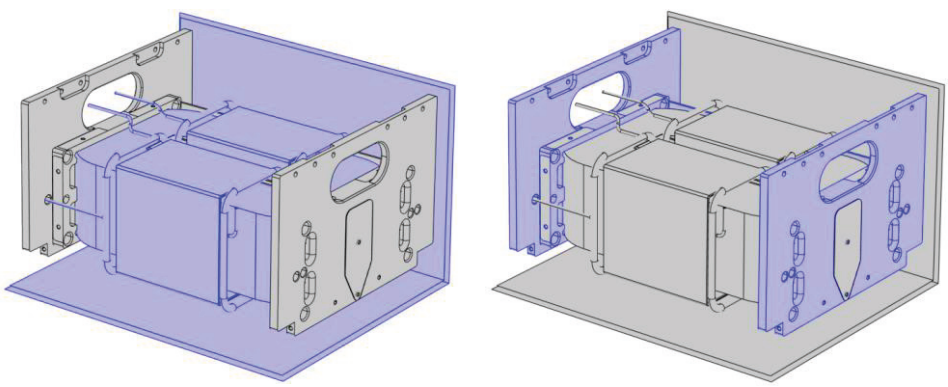


Figure 9.43: Material setup for high-voltage inductor for finite element analysis in electrostatic condition

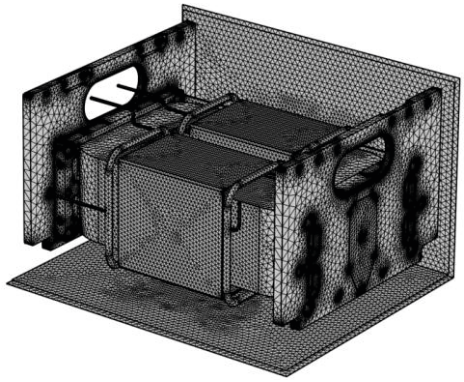


Figure 9.44: Meshed high-voltage inductor geometry for finite element analysis

*Electrostatic simulation: field distribution (case 1)*

As with the common mode inductor, the first case arises when the inductor input is driven by the source such that a potential difference exists between the two inductor windings. Again, this potential difference is limited to that of 26 kV. To study the worst possible field distribution associated with this case, the one of the two windings as well as the associated anti-corona rings and connecting wires are set to a potential of 26 kV. Correspondingly, the other winding, the associated anti-corona rings and connecting wires as well as the magnetic core and surrounding enclosure are set to ground potential. All insulators are left floating. This model set-up is depicted in Figure 9.45.

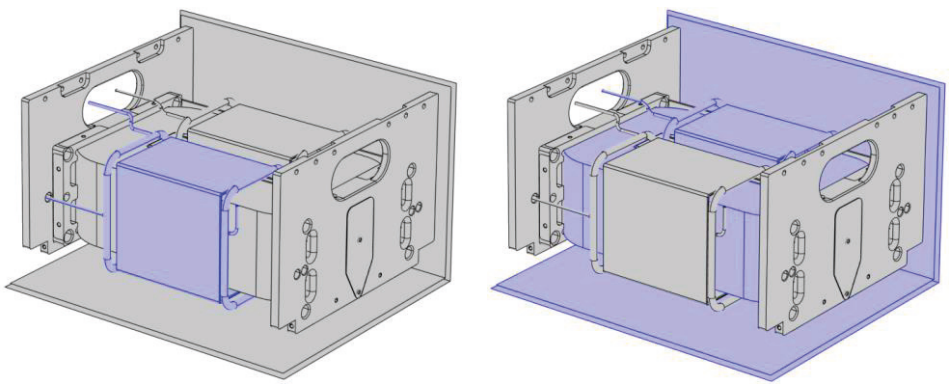


Figure 9.45: Electrostatic potential setup for common mode inductor in calculating electrostatic field distribution for 'case 1'

Simulation of above-described model yields results exemplified in Figure 9.46. Here, the simulated electrostatic field distribution in the plane defined by the upper anti-corona ring of the windings in top-down view is shown. From this figure, it

may be verified that the electrostatic field strength – in this part of the geometry – never exceeds that of 5 kV/mm. The corresponding electrostatic field distribution was visualized at multiple points of interest as indicated in Figure 9.47 and summarized in Table 9.7. It is verified that the electrostatic field strength never exceeds the limiting value of 10 kV/mm.

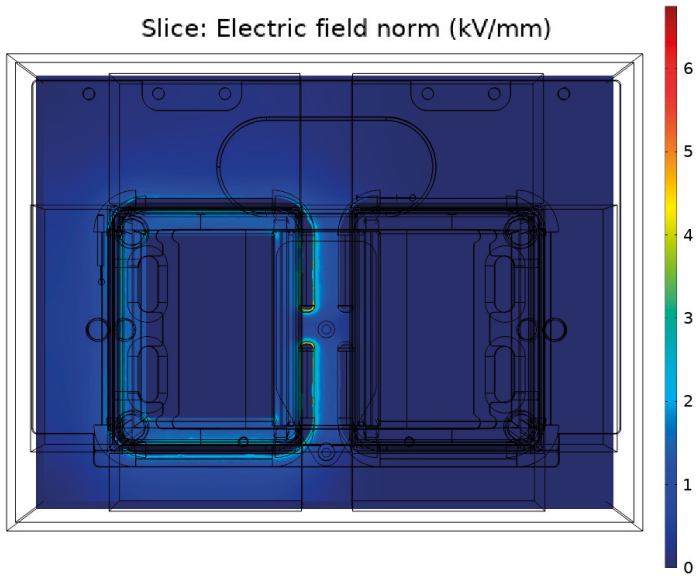



Figure 9.46: Example of field simulation

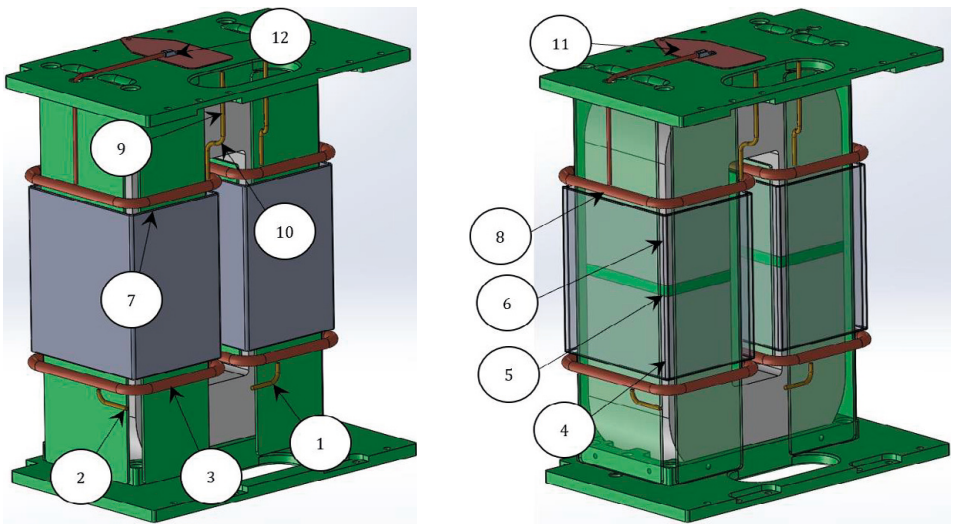



Figure 9.47: Points of interest for ‘case 1’

Table 9.7: Electrostatic field strength at points of interest identified in Figure 9.47

| Point | Description | Field strength [kV/mm] |
|---|---|---|
| 1 | Small wire, connected to lower anti-corona ring | < 1 |
| 2 | Small wire, connected to lower anti-corona ring, termination | < 8 |
| 3 | Lower anti-corona ring (at potential) | < 5 |
| 4 | Core corners, before air gap | ~5 |
| 5 | Core corners, at edge of air gap | < 7 |
| 6 | Core corners, after air gap | ~5 |
| 7 | Edge of winding (at potential) | ~5-6 |
| 8 | Upper anti-corona ring (at potential) | < 5 |
| 9 | Small wire, connected to upper anti-corona ring, straight | ~4 |
| 10 | Small wire, connected to upper anti-corona ring, bend | < 6 |
| 11 | Upper connection plate | < 8 |
| 12 | Lug connector and connecting wire | < 7 |

*Electrostatic simulation: field distribution (case 2)*

The second case arises when the potential difference between two windings is zero, but – due to the use of a virtual ground – there still exists a potential between both windings and the virtual ground. This potential difference is again limited to that of 26 kV. The adjusted model is set-up according to that shown in Figure 9.48.

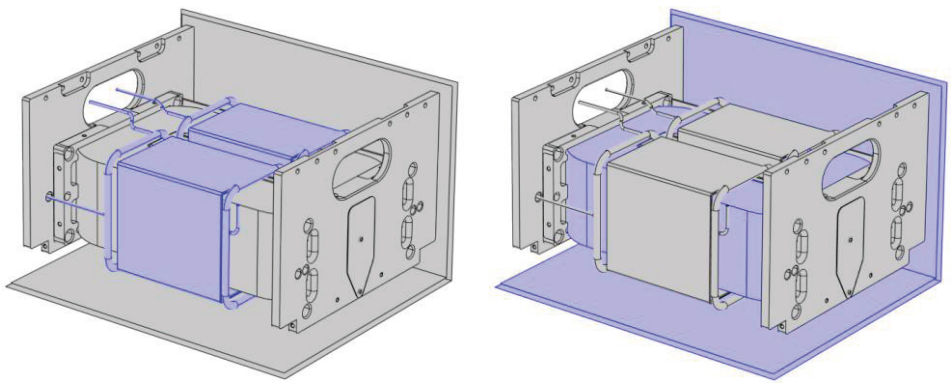


Figure 9.48: Electrostatic potential setup for common mode inductor in calculating electrostatic field distribution for 'case 2'

Simulation of the above-described model yields results exemplified in Figure 9.49. It is again verified that the electrostatic field strength – in this part of the geometry – never exceeds that of 5 kV/mm. The corresponding electrostatic field distribution was visualized at multiple points of interest as indicated in Figure 9.50 and summarized in Table 9.8. It is verified that the electrostatic field strength never exceeds the limiting value of 10 kV/mm.

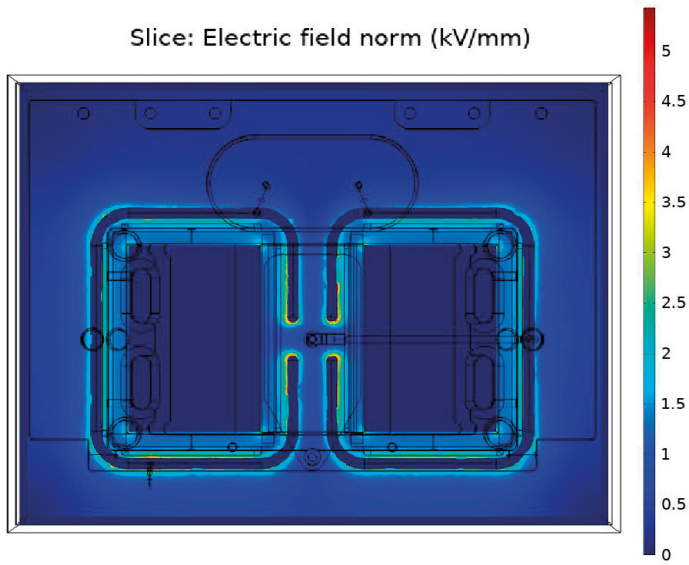



Figure 9.49: Example of field simulation

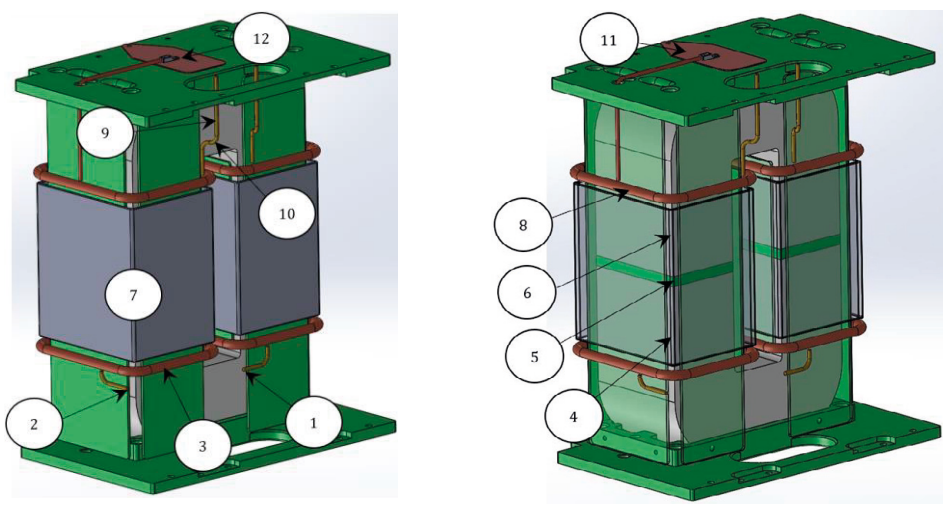



Figure 9.50: Points of interest for ‘case 2’

Table 9.8: Electrostatic field strength at points of interest identified in Figure 9.50

| Point | Description | Field strength [kV/mm] |
|---|---|---|
| 1 | Small wire, lower anti-corona ring, termination | < 9 |
| 2 | Small wire, lower anti-corona ring, termination | < 10 |
| 3 | Lower anti-corona rings | < 5 |
| 4 | Core corners, before air gap | ~5 |
| 5 | Core corners, at edge of air gap | < 7 |
| 6 | Core corners, after air gap | ~5 |
| 7 | Edge of windings | ~5-6 |
| 8 | Upper anti-corona rings | < 5 |
| 9 | Small wire, upper anti-corona ring, straight section | ~4 |
| 10 | Small wire, upper anti-corona ring, bend | ~4-5 |
| 11 | Upper connection plate | < 8 |
| 12 | Lug connector and connecting wire | < 7 |

*Electrostatic simulation: calculation of parasitic capacitance*

The procedure to analytically calculate the stray capacitive elements of the high-voltage filter inductor geometry was described in section 5.3.6 and the derived equivalent circuit model was shown in Figure 5.40. There, the stray capacitive elements were divided among those derived from the electrical field present between 1) the inductor windings and the surroundings, 2) the inductor windings and the (virtually grounded) magnetic core, and 3) between the two inductor windings. To verify these calculations, the electrostatic potential setups shown in Figure 9.45 and Figure 9.48 were modified such that, primarily, the potential varies along the inductor windings (as is the case in practice). Then, the electrostatic energy stored in the volumes associated with the identified capacitive elements was calculated by integration. The analytically calculated values are compared to those derived from finite element analysis in Table 9.9.

**Table 9.9: Comparison of high-voltage filter inductor stray capacitance values derived from analytical equations and using finite element analysis**

| Capacitive element | Capacitance (analytic) [pF] | Capacitance (FEA) [pF] | Estimation error [%] |
|---|---|---|---|
| $\sum C_{Lf-e-i}$ | 3.62 | 3.76 | -3.7% |
| $\sum C_{Lf-e}$ | 96.7 | 106 | -8.8% |
| $\sum C_{Lf-i}$ | 36.7 | 33.9 | 8.3% |

*Magnetostatic simulation: model setup*

The high-voltage inductor was then simulated in magnetostatic condition. The purpose of this simulation is to 1) ensure that the magnetic flux density never exceeds the limits of the core material, and to 2) quantify the resulting inductance value. Again, as with the transformer and the common mode inductor, 1) all objects not constituting either a winding arrangement or magnetic material was removed, 2) the windings were modelled in full detail in ensuring maximally accurate field descriptions, and 3) part of the magnetic core was removed in accounting for magnetic fill factor. Note that in this case, since an air gap is used, the removal of the core has to be done from the surface inwards in avoiding cutting the core in two pieces. The resulting simplified inductor geometry is shown in Figure 9.51. Model materials were then defined as indicated in Figure 9.51. Here, the relative permeability of the magnetic material is assumed to be on the order of 5000. Finally, the meshed geometry is shown in Figure 9.52.

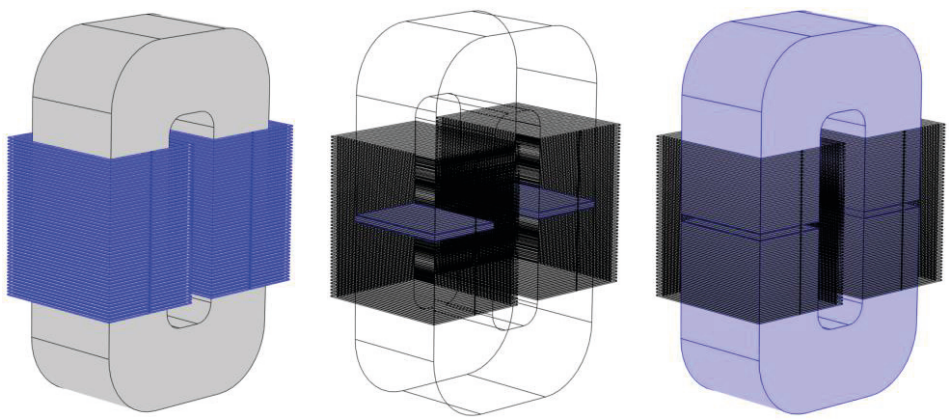


Figure 9.51: Material setup for high-voltage inductor for finite element analysis in magnetostatic condition

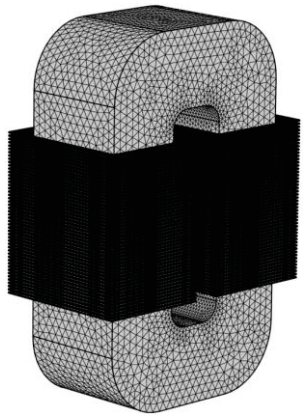


Figure 9.52: Meshed high-voltage inductor geometry for finite element analysis

*Magnetostatic simulation: calculation of inductance*

To evaluate the peak magnetic flux density in the inductor core geometry, the inductor windings are excited with the nominal load current. Here, the windings produce flux in the same direction. The resulting magnetic flux density distribution is shown in Figure 9.53. Importantly, the peak magnetic flux density in the straight section does not exceed that of 1.0 T, well within the limits of the core material. Again, the resulting inductance may be calculated from $L_f = (2/I_2^2) \cdot \int \rho_m dV = 8.19\ mH$, matching the design value within 5%.

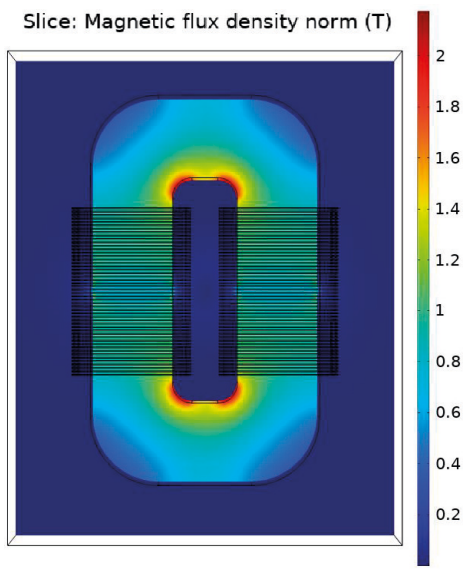



Figure 9.53: High-voltage inductor magnetic flux density distribution

### 9.2.5 Complete circuit simulation

The above-described component modeling was integrated with power electronic converter models in developing a complete system model for circuit simulation. Here, Figure 9.54 shows the simulated output pulse voltage waveform as well as the associated primary-side H-bridge voltage and currents. As shown, the simulated pulse rise time is on the order of 130 µs and the flat-top peak-to-peak ripple is on the order of 1 kV. As will be elaborated on in section 9.3.1, the pulse amplitude is limited to that of ~17.6 kV. The simulated pulse performance is validated through experiment in section 9.3.1. Then, Figure 9.55 shows the corresponding AC-side power quantities. Here, several pulsing periods are shown to include several charging cycles. In accordance with the work developed in chapter 7, the capacitor charger quickly reaches steady state in achieving constant power charging. With 1) the limited pulse amplitude and as 2) only one high-voltage module is used, the charging current is limited to that of ~100 A. The corresponding line current has an RMS value of ~127 A, corresponding to a system input power of ~89 kW and an efficiency of 87.5%. The simulated assessment is verified through experimentation in section 9.3.3.

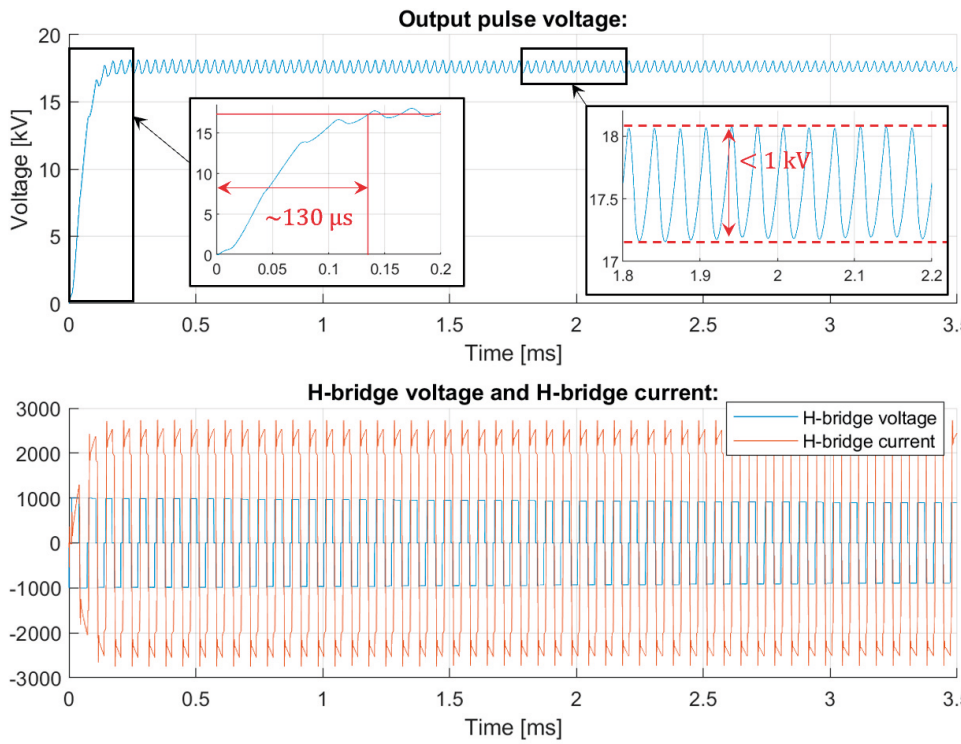



Figure 9.54: Simulated prototype converter chain output pulse waveform and associated primary-side H-bridge voltage and current waveforms

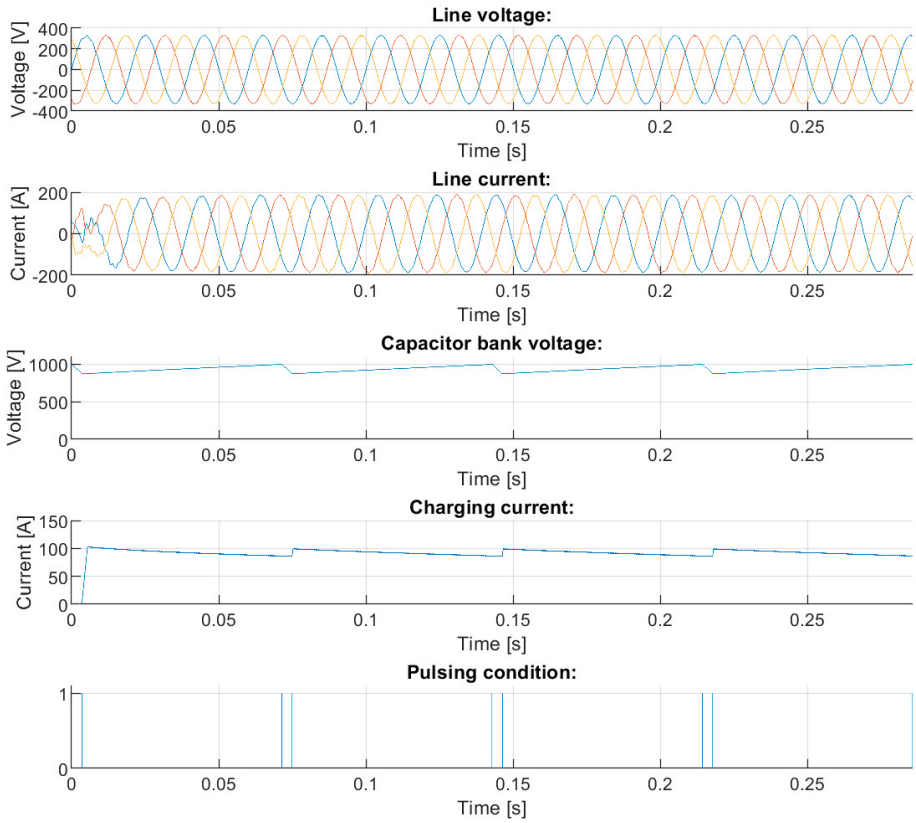



Figure 9.55: Simulated prototype converter chain line voltage and line current

## 9.3 Experimental validation of prototype converter chain

The prototype converter chain was experimentally validated by measurement using the Zimmer LMG670 precision power analyzer, [9.25]. This instrument permits measurement with a sample rate of 1.21 MS/s and 18-bit resolution. Here, low-voltage measurements (i.e., not exceeding that of ~1 kV) were carried out directly using the voltage measurement interface of the L60-CH-A1 power measurement channels, [9.26]. These channels feature accuracy on the order of 0.015%. High-voltage measurements were carried out interfacing with the HST12-1 precision wideband high-voltage divider, [9.27]. This sensor has a specified DC to 2.5 kHz accuracy of $\pm$0.1%, and an accuracy of $\pm$0.2% below that of 10 kHz. Importantly, this sensor has a specified absolute maximum periodic peak voltage limited to 20 kV. Hence, for safety reasons, a 10% safety margin was applied by always limiting

the pulse output voltage to that of ~18 kV. Finally, current measurements were carried out interfacing with the PCT600 precision current transducer, [9.28]. These sensors have a specified DC to 10 Hz accuracy of ±0.0015%, a 10 Hz to 2 kHz accuracy of ±0.01%, and an accuracy of ±0.2% below that of 10 kHz. The instruments and the probes were calibrated and certified by Zimmer prior to measurement.

### 9.3.1 High-voltage pulse quality

A measurement interval representing two pulse periods (i.e., 2/14 = ~0.14 s) is shown in Figure 9.56. As noted in the above, the peak pulse voltage is limited to that of 18 kV. Correspondingly, the peak pulse current is ~90 A. Then, Figure 9.57 shows a zoom across the pulse flat top in evaluating pulse performance. Importantly, the pulse rise time is limited to that of 130 μs, and the worst-case steady state pulse ripple is limited to that of ~1 kV. Importantly, assuming a worst-case ripple reduction ratio of 6, this is indicative of a worst-case normalized modulator ripple below that of 0.15%. Note also that flat-top ripple decreases over time and particularly towards the end of the pulse event in accordance with that described in section 5.3.6. Finally, the obtained pulse waveform is compared to the simulated waveform described in section 9.2.5 in Figure 9.58. As can be seen, the two waveforms are very similar with matching pulse rise time, peak-to-peak flat top ripple and flat-top droop.

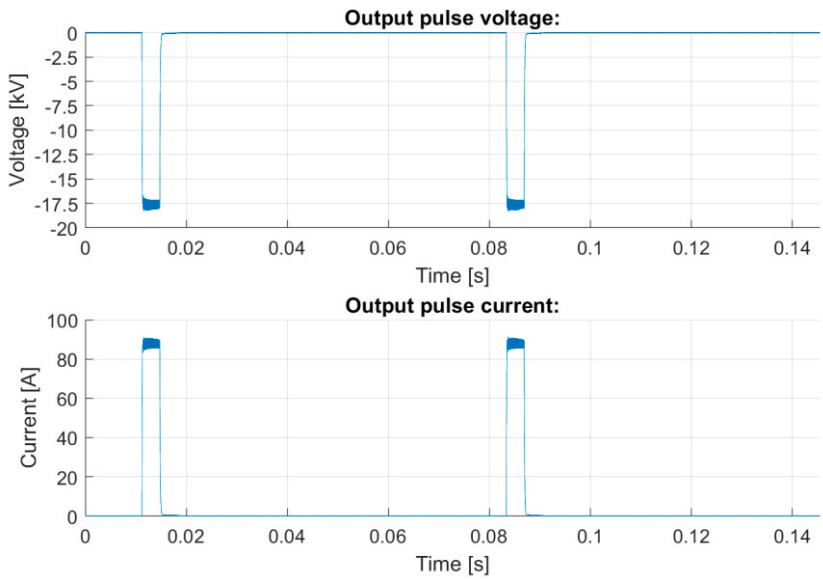



Figure 9.56: Measured prototype converter chain output pulse waveforms

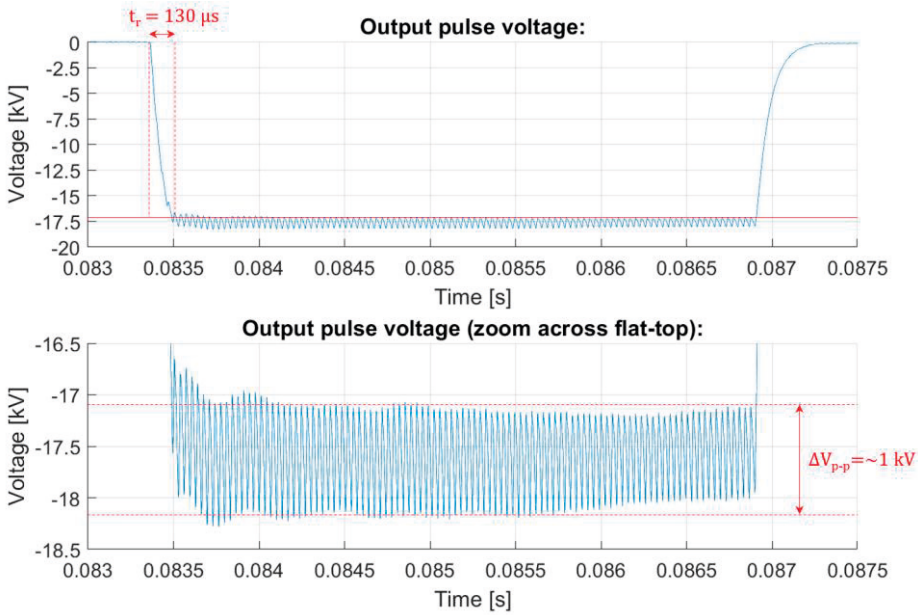



Figure 9.57: Zoom across pulse waveform flat-top

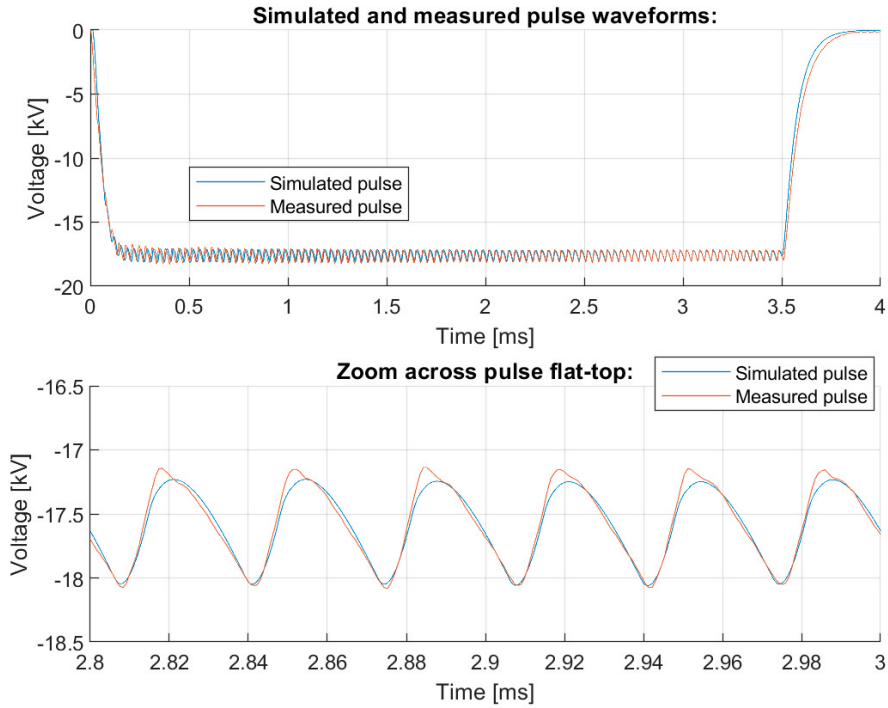



Figure 9.58: Comparison of simulated and measured output pulse waveforms

### 9.3.2 AC power quality

Figure 9.59 shows measured prototype converter chain line voltage and line current. This measurement was obtained simultaneously to those presented in Figure 9.56. First, the line current amplitude is approximately constant over time despite high-power pulsed operation due to the capacitor charging scheme for constant power charging described in section 7.2.2. Hence, flicker is effectively mitigated. Additionally, the line current waveforms are approximately sinusoidal and in phase with the corresponding line voltage waveforms. Here, the precision power analyzer measured an effective power factor of ~0.97. Note that this can be further improved by compensating for the capacitive currents drawn by the line-side filter. This functionality was not implemented in view of these experiments. Still, it is emphasized that the obtained power factor is well beyond the requirements. Finally, Figure 9.60 presents the harmonic spectrum of the line current waveforms shown in Figure 9.59. Here, the calculated line current THD is on the order of 3.5%. It is pointed out that the complete modulator system features three phase interleaved front-end circuits such that the effective line current THD should be significantly improved. Still, the achieved THD is well below that of applicable standards.

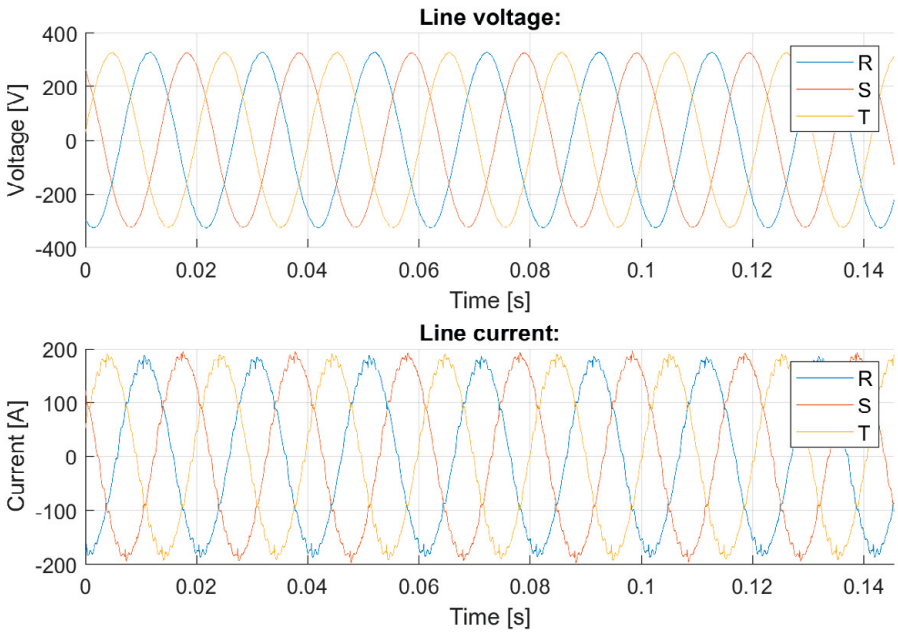



Figure 9.59: Measured prototype converter chain line voltage and line current

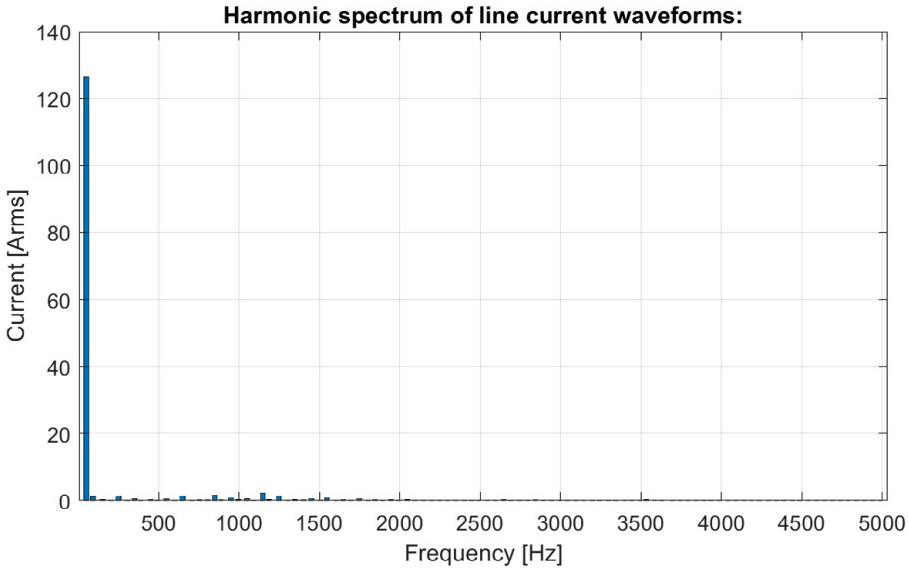



Figure 9.60: Harmonic spectrum of line current waveforms

### 9.3.3 Loss dissipation and efficiency

Loss dissipation associated with individual components was measured as follows. First, one full set of sensors was connected to the AC line input, e.g., as shown in Figure 9.61. Here, the line voltage is picked up on the input filter busbars, and the currents are measured at the system input (before the MCB). Then, a corresponding set of measurements were made at the other side of the AC filter capacitor branches, e.g., as shown in Figure 9.61.b. As the voltage is the same, the voltage measurements shown in Figure 9.61.a are routed to the second power measurement channel locally. On the other hand, as shown, the current sensors are placed after the power cables going to the filter capacitor branches. Here, it is assumed that the measured active power difference is dissipated in the filter branches, and particularly the filter damping resistors. Clearly, this is strictly not true. First, as shown in Figure 9.61, the auxiliary system is also fed from the same intersection and would be counted as filter resistor losses. Similarly, losses in the power cables as well as in the filter capacitors are also counted towards the filter resistor losses. Still, these losses are assessed to be minor in comparison to the filter resistor losses, i.e., the measurement should be accurate from a loss estimation perspective. Then, keeping the first set of sensors at the AC line input, the second set of sensors is moved to the other side of the line inductors, e.g., as shown in Figure 9.61.c. By progressively moving the second set of sensors through the power intersections of the system, the loss associated with each component may be estimated. However, it is pointed out that certain intersections are difficult or practically impossible to

access. For example, measuring the loss dissipation associated with the active rectifier and the dc/dc converter individually would require measuring the current on the dc-link busbars. As these are not accessible (especially in practically fitting the aperture of the precision current sensor around the busbar, without disassembling the power stack), the total loss dissipation of the entire power stack is considered. Similarly, connecting the high-voltage probe to different components inside the high-voltage module enclosure is practically impossible. Instead, the total loss dissipation of the complete module is considered.

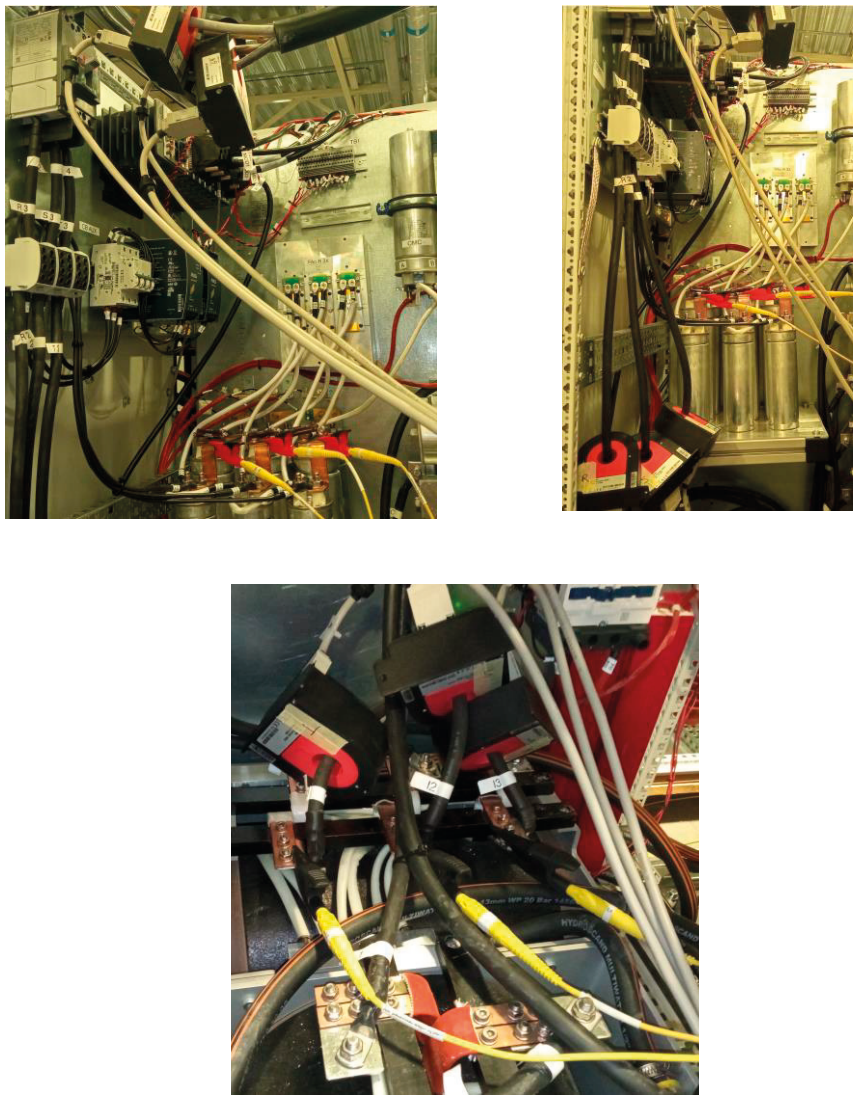


Figure 9.61: Technique used in measuring component power loss dissipation and system efficiency

The total system input power was measured to be 88.9 kW whereas the corresponding system output power was measured to be 77.8 kW. This matches well with the loss dissipation summarized in Table 9.10 as measured using the above-described technique, indicating that all major loss sources are included. Furthermore, the measured loss dissipation of the indicated component groups compares well (with the exception of the busbar, as discussed below) with the power dissipation estimated by the models developed in chapter 5. The corresponding efficiency is 87.5%. Here, it is pointed out that the front-end system operates at only half the rated power and at only 400 V (whereas it has been designed for 600 V). Correspondingly, the converter modulation index is reduced, further degrading efficiency. Very importantly, the power dissipated in the busbar was greater than expected, in part due to the skin and proximity effects. Additionally, the busbars had been made longer than necessary to facilitate interconnection, increasing total losses. Interestingly, extended heat run testing further revealed issues with the busbar design. This experience influenced busbar design in the final modulator configuration. Accounting for the above factors, as will be demonstrated in subsequent sections, reveals a modulator efficiency of 90% in accordance with that presented in chapter 5.

**Table 9.10: Loss dissipation measured for prototype converter chain**

| Component | Measured power dissipation | Estimated power dissipation |
|---|---|---|
| AC-line filter (resistors) | 250 W | 250 W |
| AC-line inductors | 250 W | 450 W* |
| Front-end power stack | 2750 W | 2690 W |
| DC-side inductor | 250 W | 414 W* |
| Charging diodes | 100 W | 90 W |
| H-bridge power stack | 4600 W** | 4670 W** |
| Busbar | 600 W | - |
| High-voltage module | 2300 W | 2300 W |

### 9.3.4 Notes on pulse control

The output pulse waveform is generated using the open loop controller described in section 7.3.3. Clearly, and especially in considering open loop control methods, model inaccuracies represent performance deviations, i.e., it is important to be able to intuitively tune the controller parameters in-situ. However, as an addition, a

function automatically varying the controller parameters around a proposed starting point and saving the associated resulting pulse waveforms was implemented as an aid in optimizing the controller. The process is summarized in the following. First, the method described in section 7.3.3 is used in generating a first set of PWL breakpoints. The generated breakpoints are fed into the local control system controlling the prototype converter chain. Pulse generation is started and the resulting pulse performance is noted. The controller parameters are then varied within a pre-defined range. The resulting waveforms are measured and saved to file by the local control system. Then, the stored pulse waveforms are characterized in terms of a number of performance indicators such as pulse rise time, pulse overshoot, pulse flatness, and so on. Eliminating controller parameters resulting in unfeasible pulse performance, a suitable set of controller parameters can be selected by studying the trade-off between the performance indicators. It is important to note that the quality of the results produced by this procedure is greatly influenced by 1) the chosen starting point, 2) the method of choosing parameter variations, and 3) the number of variations. This is pointed out because the number of variations is directly connected to the time required in evaluating the parameter sweep. Considering $N_b$ breakpoints, $N_v$ variations per breakpoint and $N_0$ repetitions per configuration, the total time of evaluating the parameter sweep is given by:

$$T = \frac{\left(N_p{}^{N_v}\right)N_0}{f_r} \tag{9.1}$$

As an example, considering a relatively limited set-up with six breakpoints, five variations per breakpoint, and repeating each configuration two times, the ESS pulse repetition rate of 14 Hz requires a runtime of almost 20 minutes. Clearly, it is of interest to implement an optimization procedure in cleverly selecting suitable variations. However, due to time restrictions in prototyping work, a straightforward brute force procedure was instead implemented. Here, though the theory developed in chapter 7 indicated that five unknown breakpoints would suitably match the ideal reference waveform, this would be excessive (with one time and one value per breakpoint) considering (9.1). Instead, it was considered that it should be possible to determine the first and last breakpoints with reasonable accuracy ahead of time, reducing the problem to that of three unknown breakpoints, i.e., six parameters, Figure 9.62.

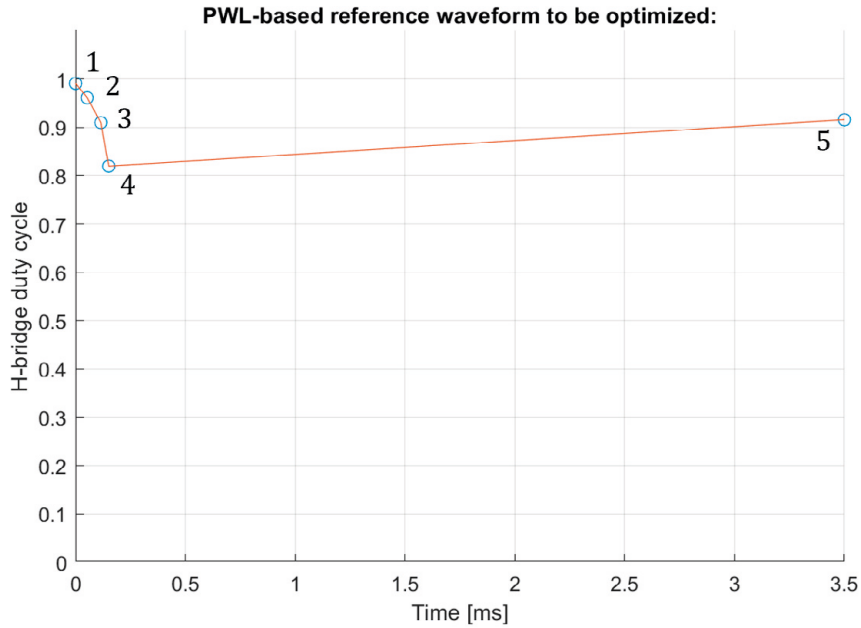



Figure 9.62: Reference waveform to be optimized

The procedure was set up in accordance with the above and with five unique values per parameter. Eliminating parameter configurations resulting in rise times exceeding that of 200 µs, yielded the results presented in Figure 9.63. Here, 'pulse flatness' is evaluated by curve fitting the pulse flat top to a first order polynomial and extracting the slope coefficient. Note that as the pulse voltage is negative, a negative pulse flatness value (slope coefficient) indicates an overcompensated pulse waveform. Especially interesting are the 'groups' of parameter configurations, indicating that certain breakpoints have greater impact (in some regards) than others. Expectedly, analysis indicated that the breakpoint labelled '2', Figure 9.63, most significantly contributed to pulse rise time (e.g., a short segment of relatively low value corresponds to longer pulse rise time). Hence, the discrete variations of this breakpoint give rise to the discrete groups separated on the axis representing pulse rise time. Correspondingly, variation of the other breakpoints mildly affects the pulse rise time, resulting in the variance seen within each group. Similarly, the breakpoint labelled '4', Figure 9.63, most significantly contributed to pulse flatness. Clearly, placing the third breakpoint too low or too late results in an overcompensated pulse flat top. Still, it is emphasized that this analysis is not general and depends heavily on the imposed parameter variation, influenced by the development described in chapter 7.

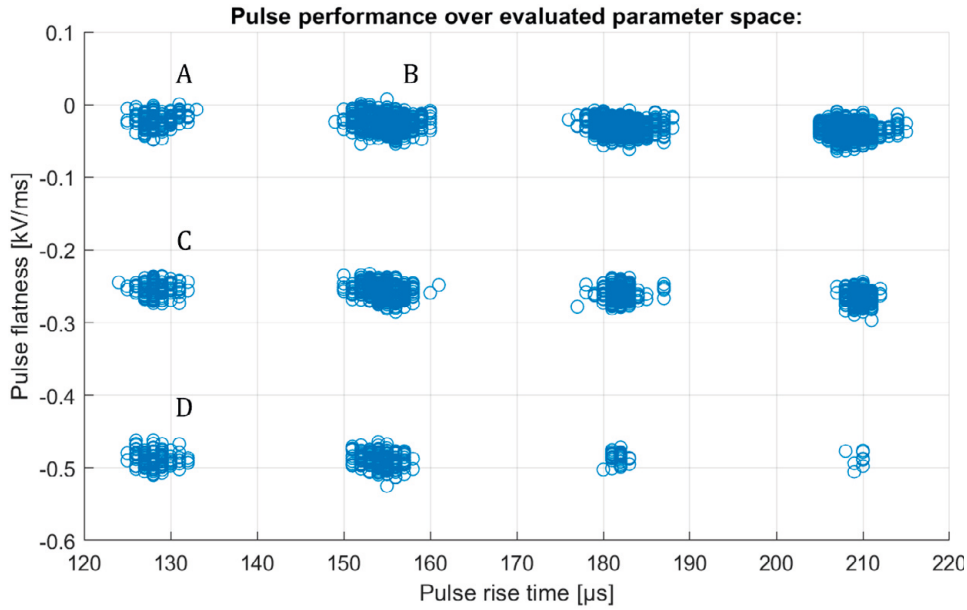



Figure 9.63: Pulse performance over evaluated parameter space

The above results and conclusions are exemplified in the following set of figures, where the resulting pulse waveforms for sample pulse reference waveforms chosen from the groups labelled 'A' to 'D' in Figure 9.63 are shown. Note the quality of the pulse measurements, especially in comparison to, e.g., Figure 9.57 and Figure 9.58. As described, the local control system measures and stores the pulse waveforms – use of the precision analyzer equipment is not practical in considering these experiments – in this case limiting the sampling rate of the signal to that of 100 kS/s. Additionally, the resolution and accuracy of the measurements are reduced. Still, the resulting measurements are highly indicative of pulse performance.

The reference waveform in Figure 9.64 is included in the other figures as reference. The difference between, e.g., Figure 9.64 and Figure 9.65, is the slight change in slope of the first segment. As described, this difference significantly degrades the pulse rise time, in this case by about ~25 µs. Still, the fourth breakpoint is correctly placed resulting in appropriate droop compensation. In Figure 9.66, the third and – especially – the fourth breakpoint are placed too low, resulting in an overcompensated pulse waveform. This trend is exaggerated in Figure 9.67.

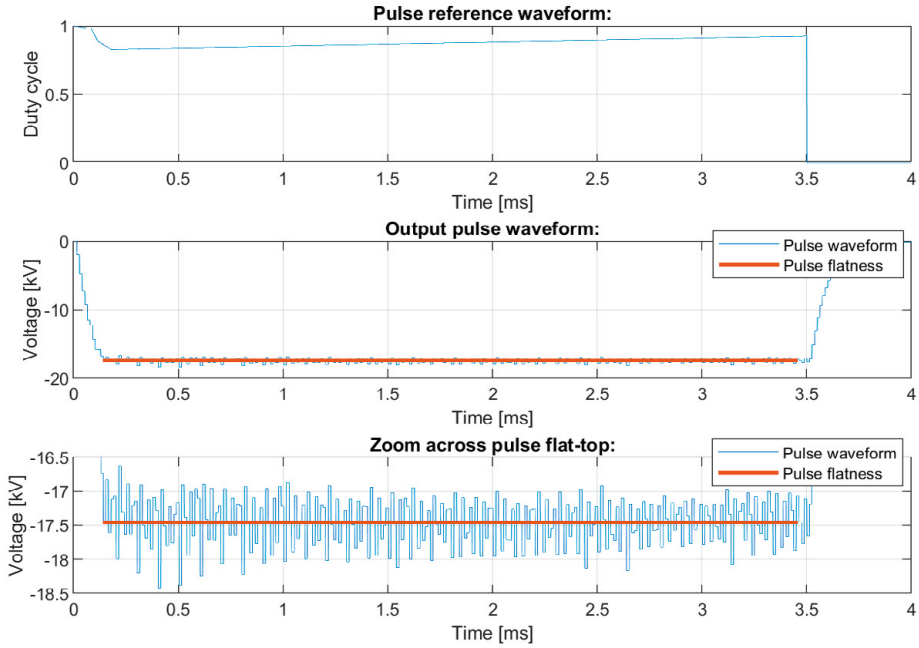



Figure 9.64: Pulse performance for sample parameter configuration from group ‘A’

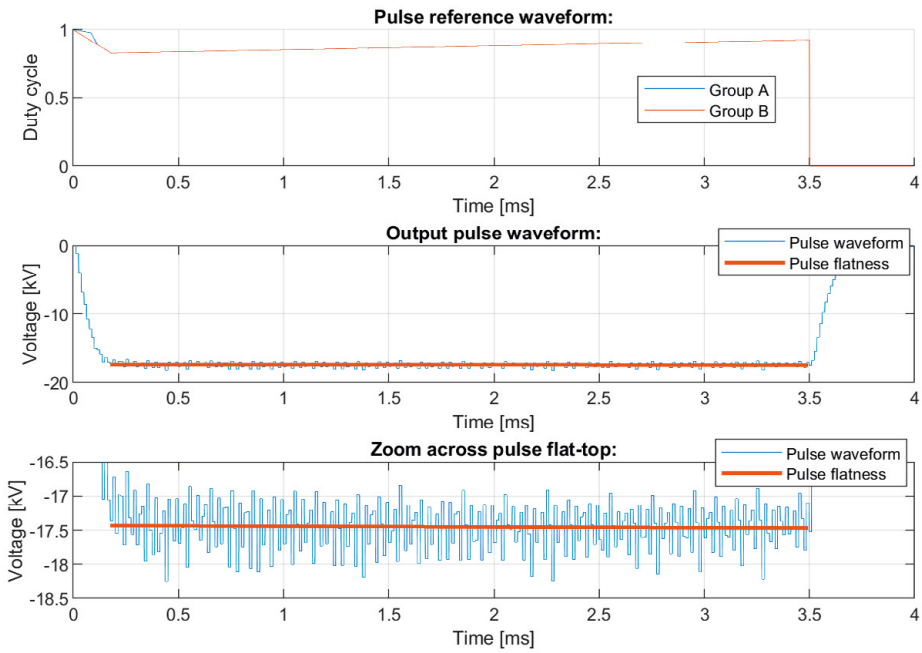



Figure 9.65: Pulse performance for sample parameter configuration from group ‘B’

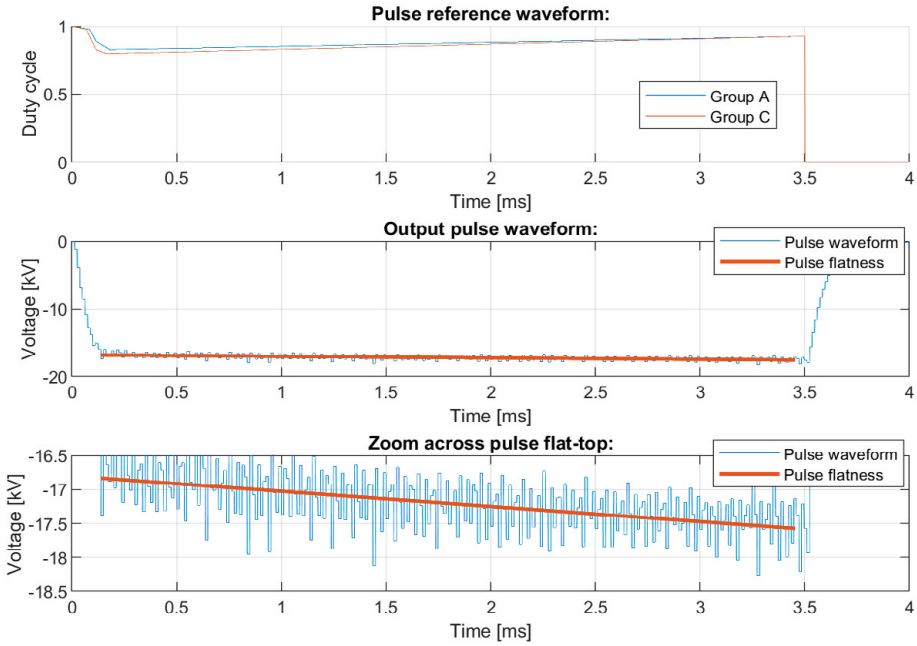



Figure 9.66: Pulse performance for sample parameter configuration from group 'C'

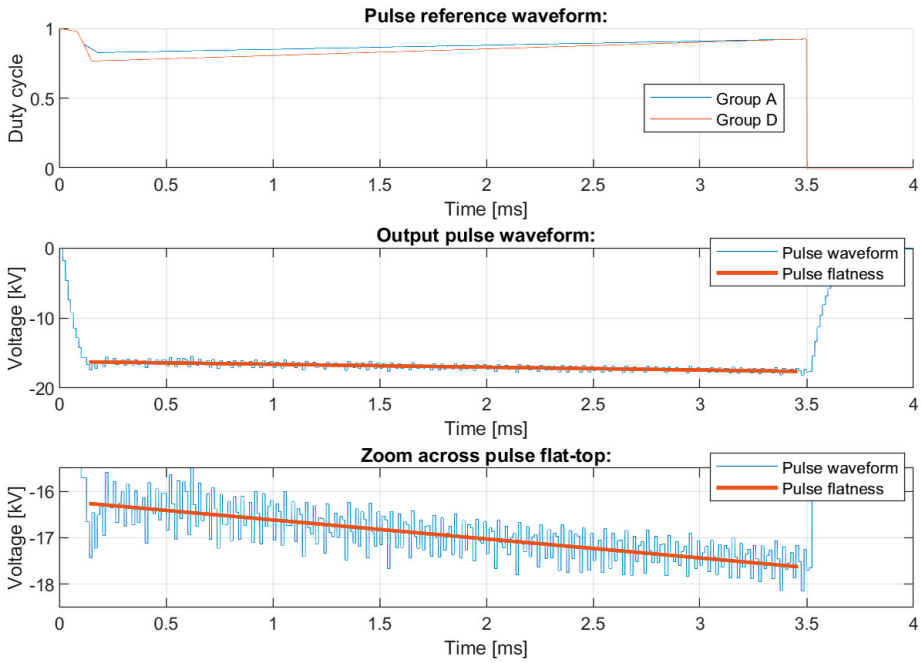



Figure 9.67: Pulse performance for sample parameter configuration from group 'D'

Clearly, a parameter configuration from group ‘A’ is considered desirable. Here, Figure 9.68 shows measured pulse performance for an optimized parameter selection obtained both locally as well as with the LMG670 precision analyzer. Note that this is the same waveform shown earlier in Figure 9.64. Though the waveform obtained with the precision analyzer is significantly more accurate, overall agreement between waveforms is good, indicating that the obtained results are reliable.

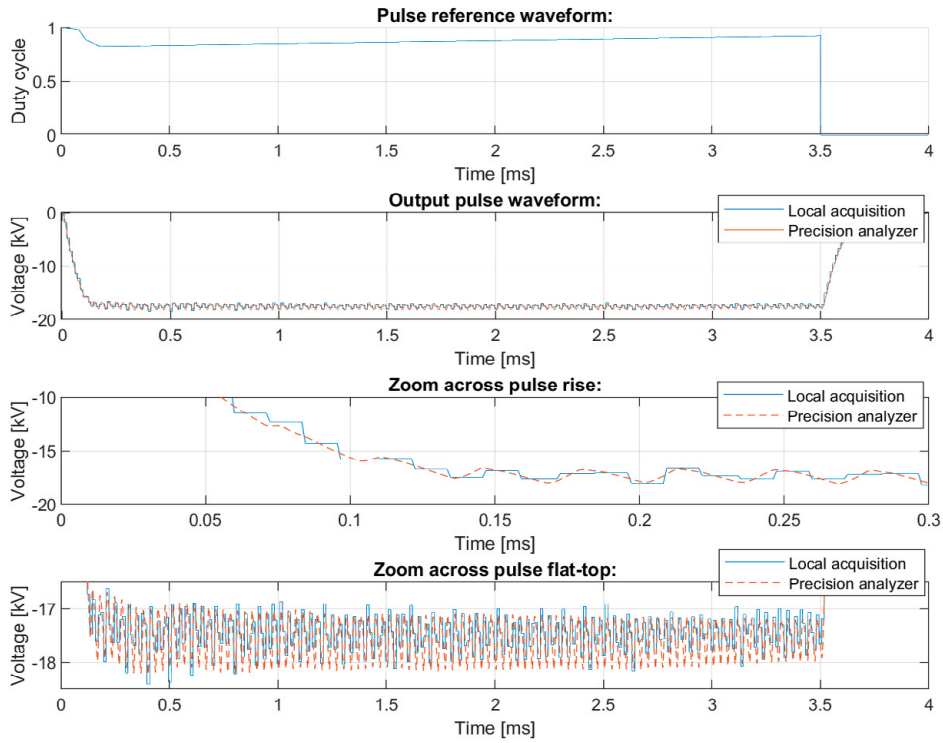



Figure 9.68: Comparison of acquired waveforms; local acquisition (cRIO) and precision analyzer (LMG670)

## 9.3.5 Conclusions

The preceding sections have demonstrated the technical feasibility of the designed components and developed modulator concept through experiment, and the obtained performance matches expected design targets. The measured pulse rise time is on the order of ~130 µs and the peak-to-peak flat top ripple is ~1 kV. Here, the pulse rise time and the flat top droop was explored and optimized by way parameter sweeping. Confirming the design and the developed technology, the obtained results enabled the launch of full-scale modulator development and eventual series production.

## 9.4 Development of full-scale modulator

An overview of the complete full-scale modulator was shown in Figure 9.1 and the associated electrical schematic was shown in Figure 9.2. As described, the complete modulator is based on the same main power components as that used and verified in the prototype converter chain. As such, this section is largely focused on describing the final integration of the modulator system.

### 9.4.1 Low-voltage part

The complete modulator shown in Figure 9.1 is again shown in Figure 9.69 in profile views with the low-voltage cabinet access doors open. Note the similarity of the final system to that of the modulator layout proposed in section 5.4. In particular, the row of capacitors comprising the main capacitor bank is seen throughout the length of the modulator. Three H-bridge power stacks are seen on both sides of the main capacitor bank row, suitably placed in facilitating interconnection with the high-voltage modules. The free space between H-bridge power stacks houses the measurement and interfacing boards as well as the three front-end power stacks. One section is reserved for the integrated control system, and one section is reserved for the modulator input power stage comprising, e.g., the main circuit breaker and the input EMC filter. The main capacitor bank is shown in top-down view in Figure 9.70. The capacitor bank is divided into three sections as indicated in Figure 9.2. As can be seen, the connection from the main capacitor bank to each H-bridge power stack is done by low-inductance busbar and through a fast fuse, protecting the components in case of short-circuit in either the busbars or the power stack. Finally, an overview of the integrated control system is shown in Figure 9.71. The control system is again based on the CompactRIO platform (described in further detail, below). Additionally, a safety PLC is used. The PLC runs in parallel to and independently of the CompactRIO control system, ensuring critical personnel safety functions.

In the following subsections, important low-voltage system components differing from that implemented in the prototype converter chain are identified and described. In the majority of cases, these differences stem from the fact that the prototype converter chain was 1) designed to validate the function and performance of, particularly, custom power components (which are identical in both cases) and 2) to be operated from a 400 V grid at comparatively low average power. It was assumed that the functionality and indicated performance of off-the-shelf performance may be relied on. Additionally, component availability played a major part in prototype component selection.

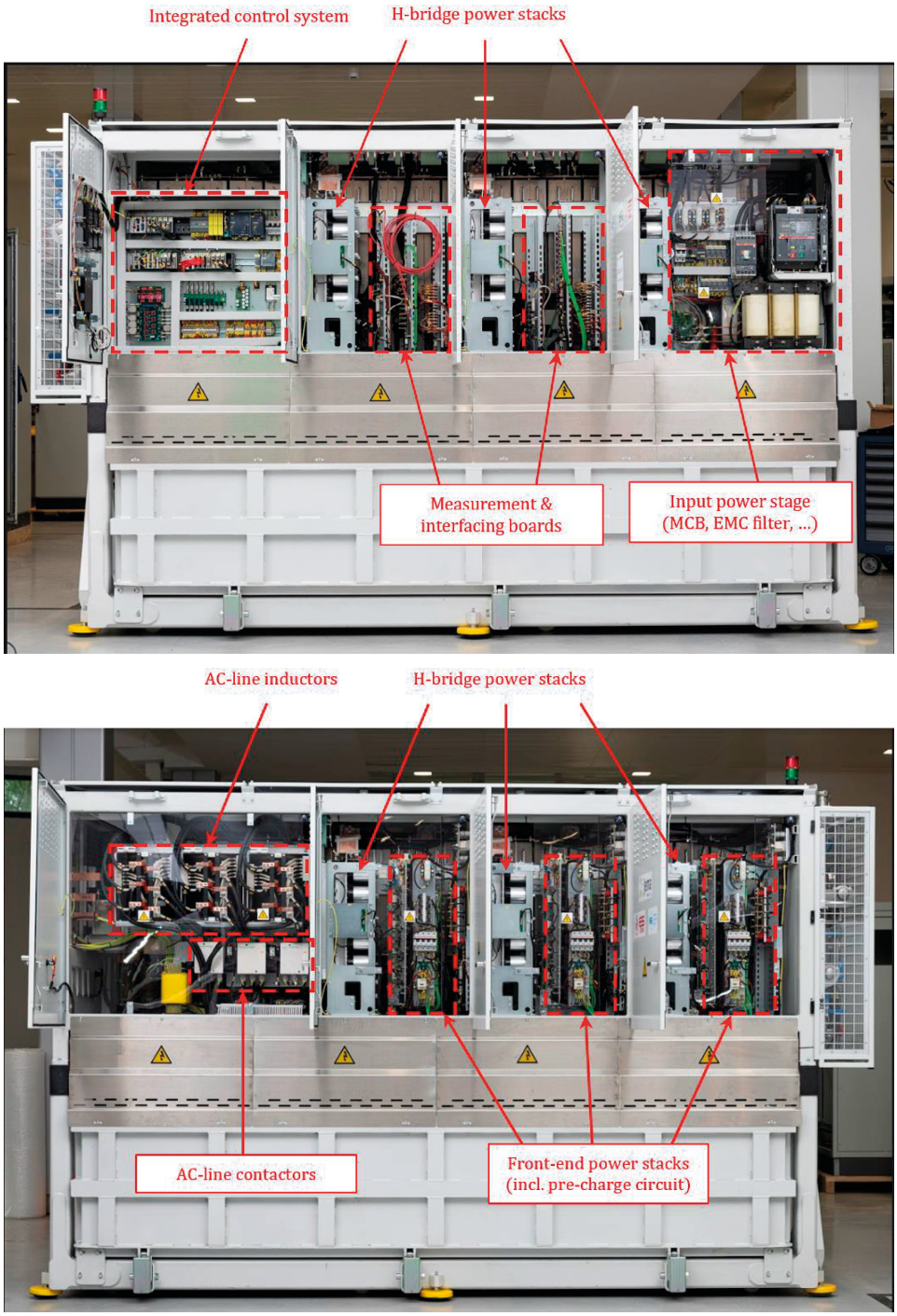



Figure 9.69: Side views of complete full-scale modulator.

Figure 9.70: Top-down view of complete full-scale modulator exposing row of capacitors comprising the main capacitor bank. The roof has been removed for clarity.

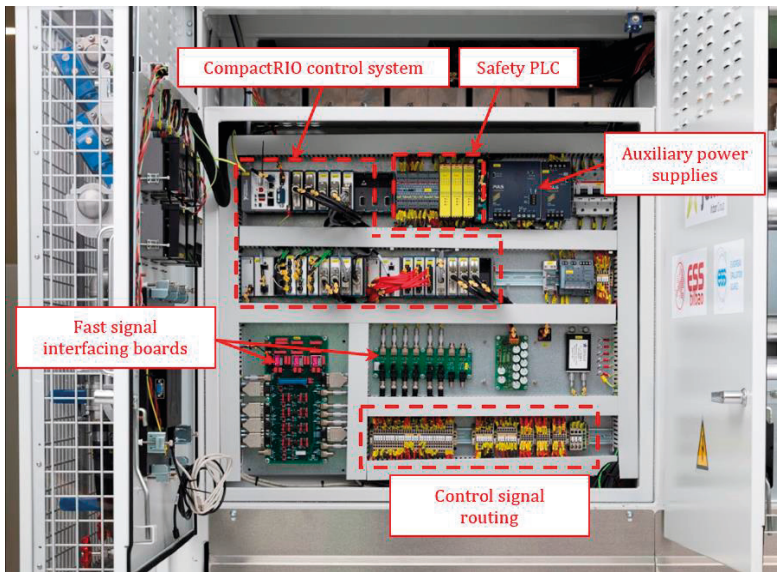



Figure 9.71: Overview of integrated control system of complete full-scale modulator.

*EMC filter*

Emission of EMC is in part mitigated through installation of an EMC filter at the input AC power port. Here, an off-the-shelf 3-phase EMC filter, 3F690-800.260, from FUSS-EMV was selected, [9.29]. The chosen filter is designed for use with industrial power converters connected to 690 V electrical grid with phase currents up to 800 A. Further details are omitted as this topic has not been discussed in detail in this dissertation.

*Main circuit breaker*

The main circuit breaker (MCB) connects/disconnects the entire modulator system to/from the electrical grid (with the notable exception of the control system and certain auxiliaries). The MCB is controllable and operated directly by the main control system. Here, the 1SDA062658R1 breaker from ABB was chosen, [9.30]. This breaker is rated for operation at 600 V, 800 A with short-circuit breaking capacity of up to 31.5 kA.

*Line filter capacitor branches*

An overview of the line filter capacitor branches is shown in Figure 9.72. The capacitor branches are based on the E62.N12-104C60 (100 µF, rated 450 V and 80 A) and E62.P17-204C60 (200 µF, rated 450 V and 80 A) from Electronicon, [9.31] and [9.32]. The damping resistors are the same as in the prototype converter chain (custom design, 50 mΩ), but are water-cooled due to the high steady-state temperature experienced in operating the prototype with only natural convection. The filter capacitor branches are connected to the rest of the circuit using busbars.

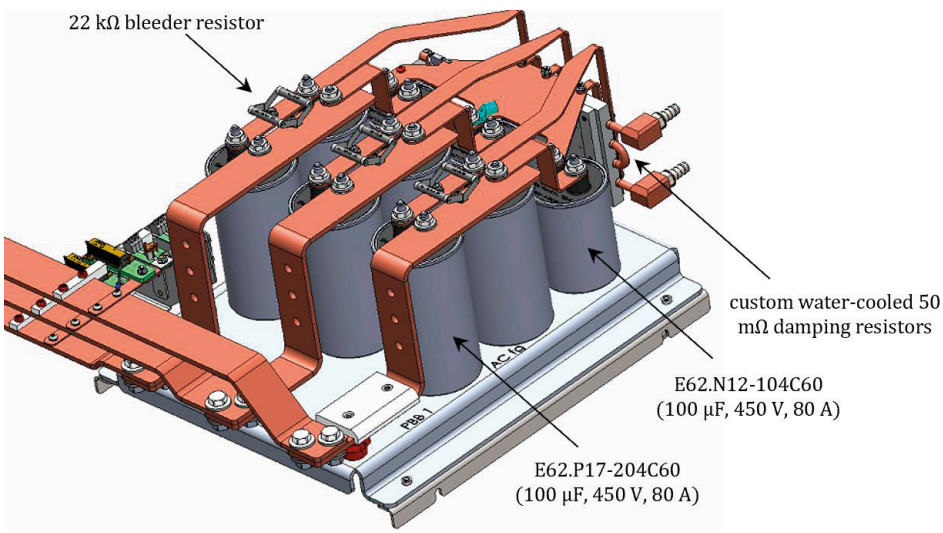



Figure 9.72: Overview of line filter capacitor branches

*Line contactors*

The capacitor charger circuits are connected and disconnected by separate AC-line contactors controlled by the main control system, providing redundancy and permitting reduced-power operation. Here, the LC1F330 contactor from Schneider Electric was chosen, [9.33]. This contactor is rated for 600 V and 330 A.

*Pre-charge system*

Each front-end capacitor charger system is equipped with an individual dc-link pre-charge system. The circuit comprises a contactor, a three-phase diode rectifier and a set of pre-charge resistors. Additionally, a circuit breaker is used for safety. Closing the contactor charges the dc-link through the resistors. The contactor is then opened and the system may be operated as usual through the main ac-line contactors. As in the prototype converter chain, the resistor RPS0500DH47R0JB (47 Ω, 500 W) from Vishay is used, [9.34]. The SKD53 (1600 V, 53 A) bridge rectifier from SEMIKRON was chosen, [9.35]. Finally, the contactor LC1D25BD from Schneider, [ref], and the circuit breaker 1SAM350000R1006 from ABB, [9.36] were selected.

*Main capacitor bank*

The main capacitor bank is based on the FFLC46MMC1698 (16900 μF, 1.0 kV) polypropylene capacitor from Kyocera AVX, [9.37]. The capacitors are placed in a single row as proposed in section 5.4. The capacitor bank comprises three sections of six capacitor units each for a capacitance of ~101.4 mF per section and 304.2 mF for the complete bank.

*Control system*

The main control system is based on the CompactRIO platform including an FPGA backplane for fast and deterministic control, a CPU handling remote control interfacing and modulator state machine functionality and a set of directly interfacing I/O modules, [ref]. In this case, the functionality of the central CompactRIO controller (cRIO-9039, [9.38]) was extended with two additional expansion chassis (NI-9149, [9.39]). The developed software and user interface may be operated by Ethernet or using the integrated TSM-1017 industrial grade LCD monitor with touch interface, [9.40]. The configuration is shown in overview in Figure 9.73. Here, in the main controller, modules 1 and 2 are 100 kHz, 16-bit analog voltage input modules connected to the interface boards collating all voltage and current measurements Then, modules 3 and 4 are 5 V, 100 ns, 8-channel digital input/output modules (configured to provide 8 independent output channels) sending the gating signals to the half-bridge modules comprising the active rectifiers and dc/dc converters, Figure 9.2. Note that these modules connect to intermediary interface boards generating the required complementary IGBT gating signals and providing the +/- 15 V required by the IGBT driver circuits. Finally, module 5

provides a fast bidirectional communication link to the two expansion chassis permitting exchange of critical information such as fault conditions. The remaining module slots are currently unused.

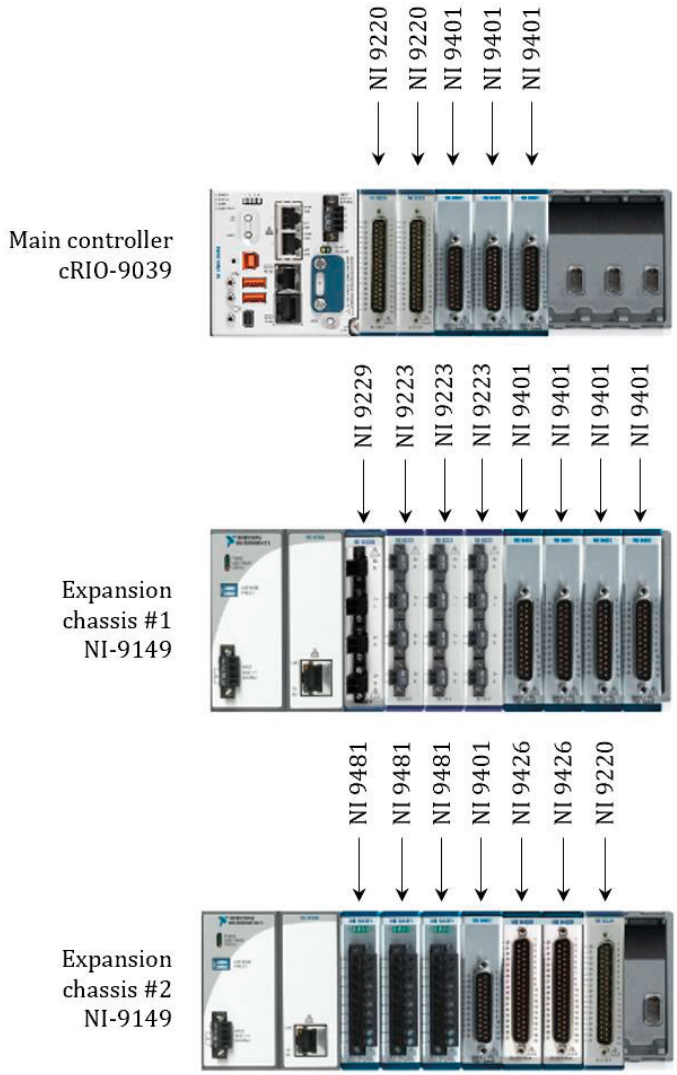



Figure 9.73: Overview of main control system for complete full-scale modulator

Then, for the first expansion chassis, modules 2, 3 and 4 are 1 MHz, 16-bit analog voltage input modules for fast and precise measurement of the six H-bridge currents as well as the pulse output signals, [9.41]. Module 1 is a 100 kHz, 16-bit analog

voltage input module carrying a copy of the pulse output voltage. Finally, modules 5, 6, 7 and 8 are 5 V, 100 ns, 8-channel digital input/output modules. The two first modules are used in sending the gating signals to the IGBT modules comprising the H-bridge converters, Figure 9.2. Again, note that these modules connect to intermediary interface boards generating the required complementary IGBT gating signals and providing the +/- 15 V required by the IGBT driver circuits. The third module is used for remote control and interlocking, and the final module provides a fast bidirectional communication link to the main controller and the second expansion chassis permitting exchange of critical information.

Finally, for the second expansion chassis, modules 1, 2 and 3 are relay control modules. The first two relay control modules used to (directly or indirectly) control the main circuit breaker, power contactors and discharge contactors. The third module is used to control the high-voltage output relays. Module 4 is a 5 V, 100 ns, 8-channel digital input/output module providing a fast bidirectional communication link to the main controller and the first expansion chassis permitting exchange of critical information. Modules 5 and 6 are 24 V, 32 channel digital input modules connected to the two interface boards collating all logic interlock signals. In essence, these interface boards contain digital readback (status signals) from, e.g., auxiliary contacts of relays/contactors and water flow-/thermoswitches to allow fault detection. Finally, module 7 is a 100 kHz, 16-bit analog voltage input module used to measure the H-bridge output currents as well as status signals from the arc protection circuit and the oil tank temperature and humidity sensors. The remaining module slot is currently unused.

### 9.4.2 High-voltage oil tank assembly

An overview of the developed high-voltage assembly is shown in Figure 9.74. The assembly again comprises six high-voltage modules. Note the similarity to that proposed in section 5.4. Additionally, a high-voltage output stage comprising the four high-voltage output sockets, high-voltage power relays, output current sensors, high-voltage divider and arc protection circuit is implemented. Several features were developed to facilitate maintenance. First, the components of the high-voltage assembly are mounted on a frame. As shown in Figure 9.76, this permits easy insertion/extraction of the high-voltage assembly into the oil tank. Additionally, the entire high-voltage stage is placed on sliding rails such that it can be inserted/extracted to/from under the low-voltage stage on top. This arrangement maximizes system power density while retaining maintainability.

Figure 9.74: Contents of developed high-voltage assembly mounted on a frame to facilitate maintenance.

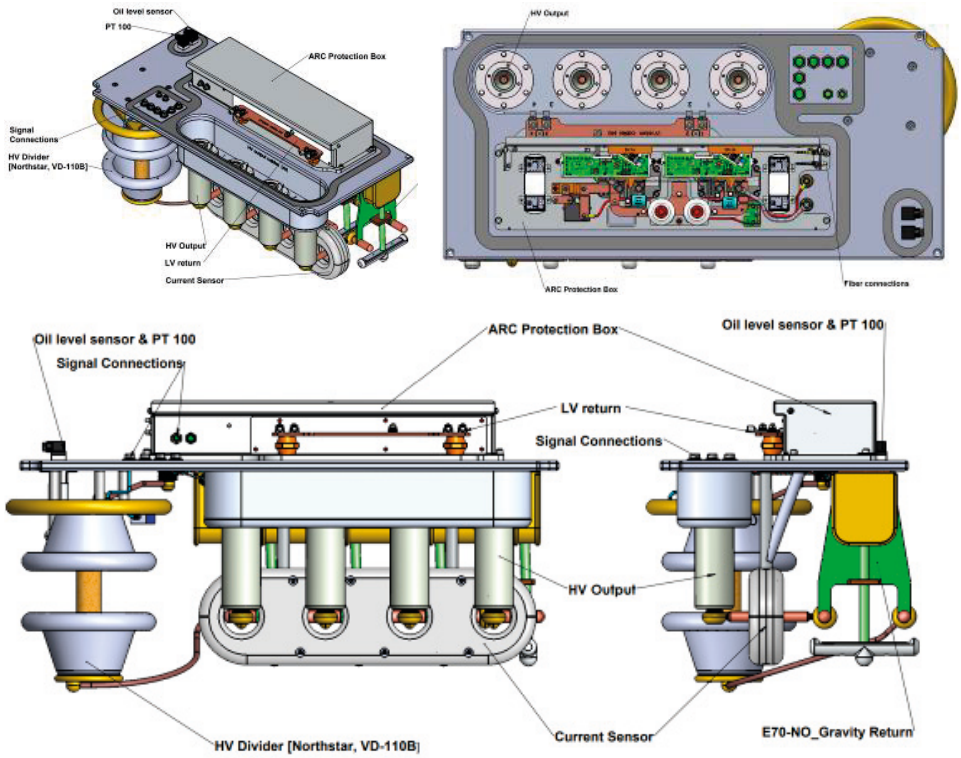



Figure 9.75: High-voltage output stage comprising four HV output sockets, high-voltage power relays, output current sensors, the high-votlage divider and the arc protection circuit.

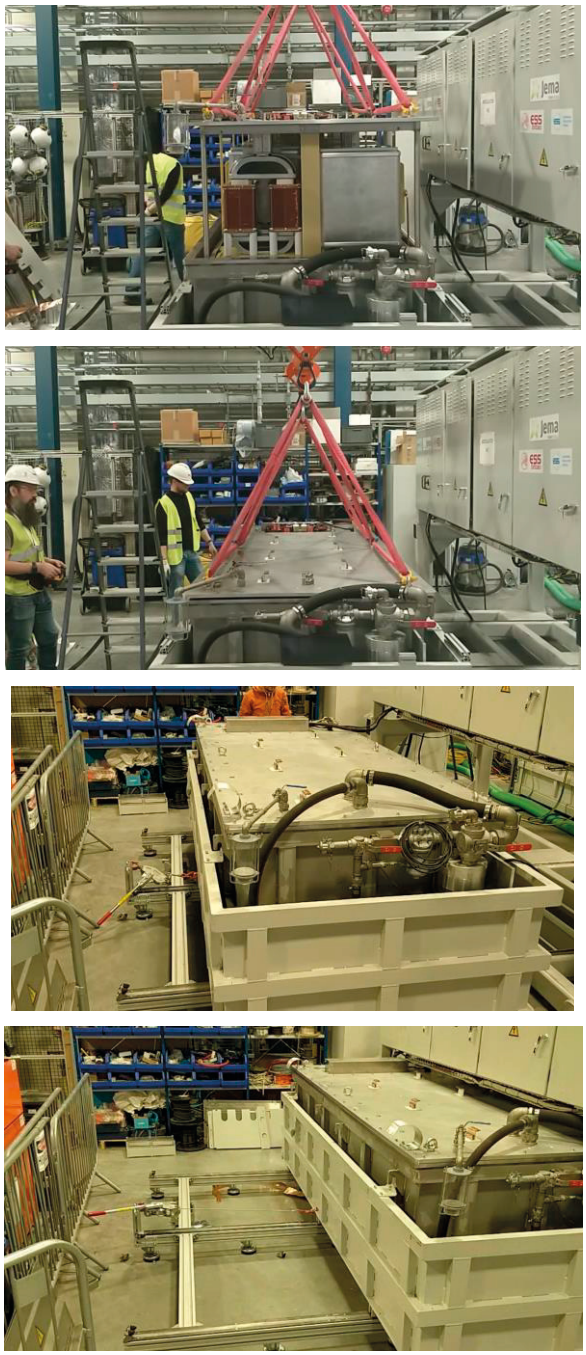


Figure 9.76: High-voltage stage insertion/extraction procedure

## 9.5 Simulation of full-scale modulator

A complete simulation model of the above-described modulator design was developed to verify the design and the expected modulator performance. Most importantly, Figure 9.77 shows the simulated high-voltage pulse waveform, indicating the main performance indicators. As shown, the flat-top varies less than 0.15% of the pulse amplitude, and features a high-frequency flat-top ripple on the order of 0.13% of the pulse amplitude. In this case, the 0-99% pulse rise time is on the order of 120 µs. The simulated assessment is verified through experimentation in the following section.

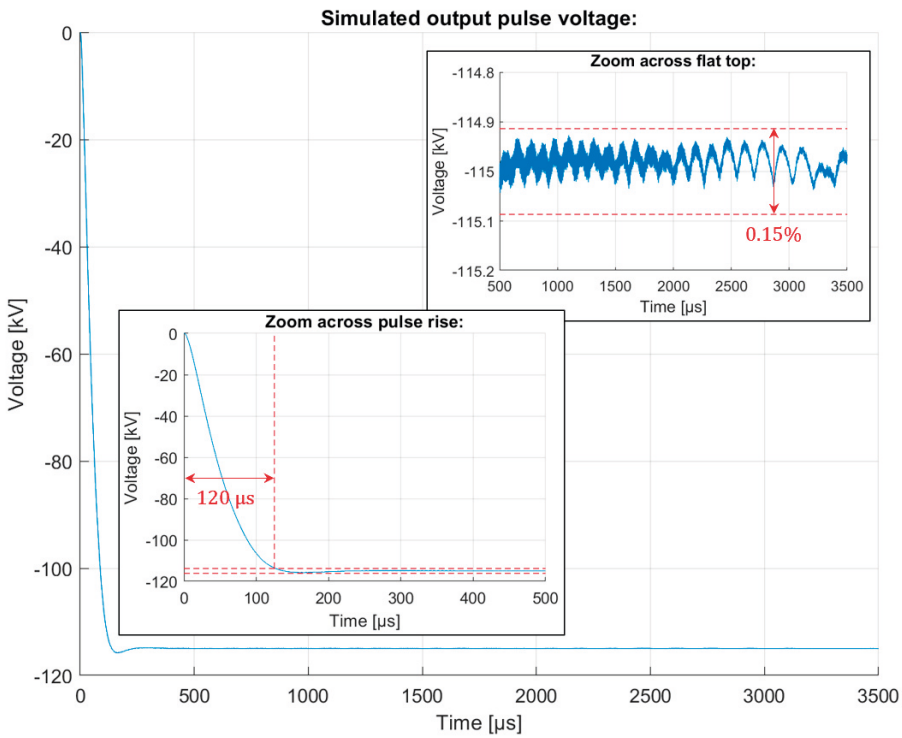



Figure 9.77: Simulated HV pulse waveform

## 9.6 Experimental validation of full-scale modulator

The modulator was experimentally validated by measurement, both using the local control system as well as with the Zimmer LMG670 precision power analyzer described in the preceding section.

### 9.6.1 High-voltage pulse quality

*Pulse rise time, droop and high-frequency ripple*

Figure 9.78 shows the obtained high-voltage pulse measurement, indicating the main performance indicators. As shown, the flat-top varies less than 0.15% of the pulse amplitude, and features a high-frequency flat-top ripple on the order of 0.13% of the pulse amplitude. In this case, the 0-99% pulse rise time is on the order of 120 µs.

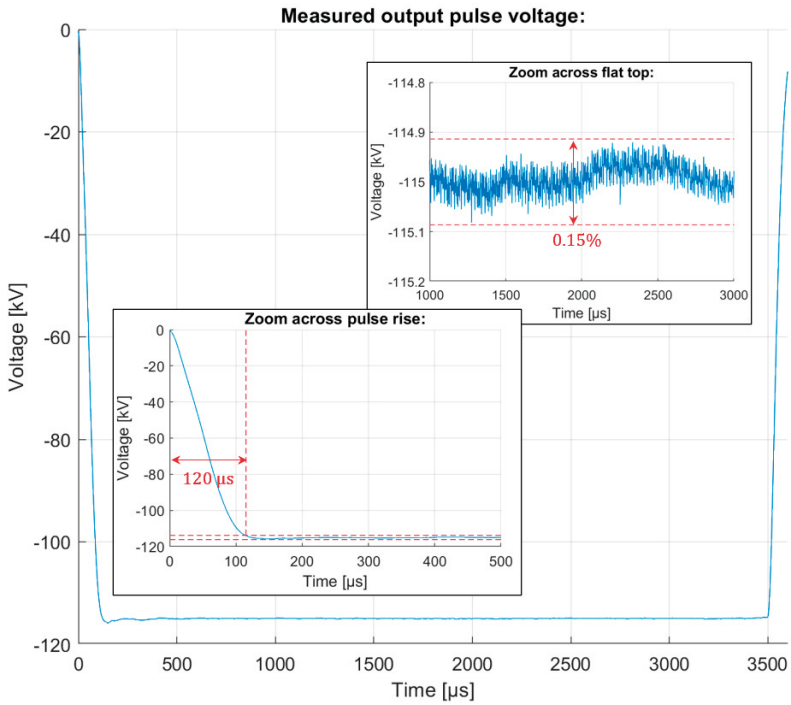



Figure 9.78: Measured HV pulse waveform

*Pulse-to-pulse reproducibility*

Figure 9.79 shows the HV pulse amplitude (sampled in the middle of the pulse flat-top) in modulator steady-state for a large number of consecutive pulses. Figure 9.79.b shows 400 long 3.5 ms pulses at 108 kV repeated at 14 Hz, corresponding to nominal operating conditions. Here, the variation of the pulse amplitude is less than 60 V, i.e., less than 0.05% of the amplitude set-point. Similarly, Figure 9.79.a shows 80 short 0.5 ms pulses at 20 kV repeated at 1 Hz. Note that this case corresponds to an average output power of only ~170 W. Still, pulse-to-pulse reproducibility remains excellent, again well below that of 0.05% of the amplitude set-point.

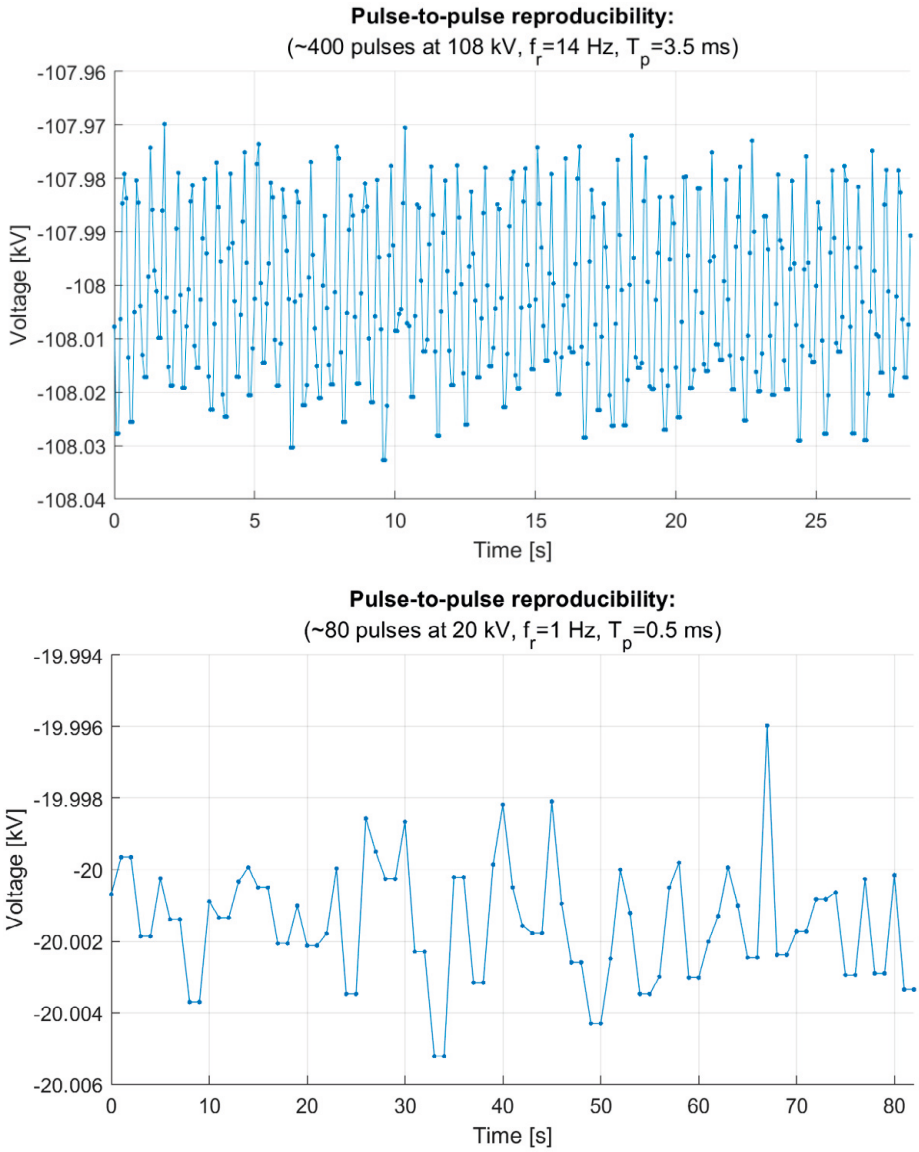



Figure 9.79: Pulse-to-pulse reproducibility. Measurement and comparison of- a) 80 pulses at 20 kV, 1 Hz, 0.5 ms; b) 400 pulses at 108 kV, 14 Hz, 3.5 ms.

*Transient performance: pulse amplitude ramping*

The preceding sections have characterized pulse quality in steady state. Additionally, as discussed, the local control system must be able to match and synchronize the power flow in the different power conversion stages for any change of user input, e.g., pulse amplitude, pulse width or pulse repetition rate. Particularly, and especially in considering open loop pulse control, it is important that the capacitor charger circuit provides the correct amount of charge to the main capacitor bank over the pulse period. Consequently, an additional pulse amplitude regulation loop was implemented to slowly adjust the pulse amplitude over several pulse periods in ensuring smooth transient operation. Here, Figure 9.80.a shows the measured pulse amplitude (again sample in the middle of the pulse flat-top) over time as the pulse amplitude set-point is changed from -20 kV to -108 kV at $t = 10\ s$. The pulse width is 3.5 ms and the pulse repetition rate is 14 Hz. Under these conditions, the nominal operating point is reached in less than 10 seconds. Later, at $t = 33\ s$, the set-point is again changed to -20 kV. Again, the new set-point is reached in less than 10 seconds. A similar situation is shown in Figure 9.80.b. Here, however, the pulse repetition rate is very low (1 Hz), requiring a significantly longer period to ramp up and ramp down the pulse amplitude in guaranteeing low pulse overshoot. Here, the response time is on the order of ~120 seconds.

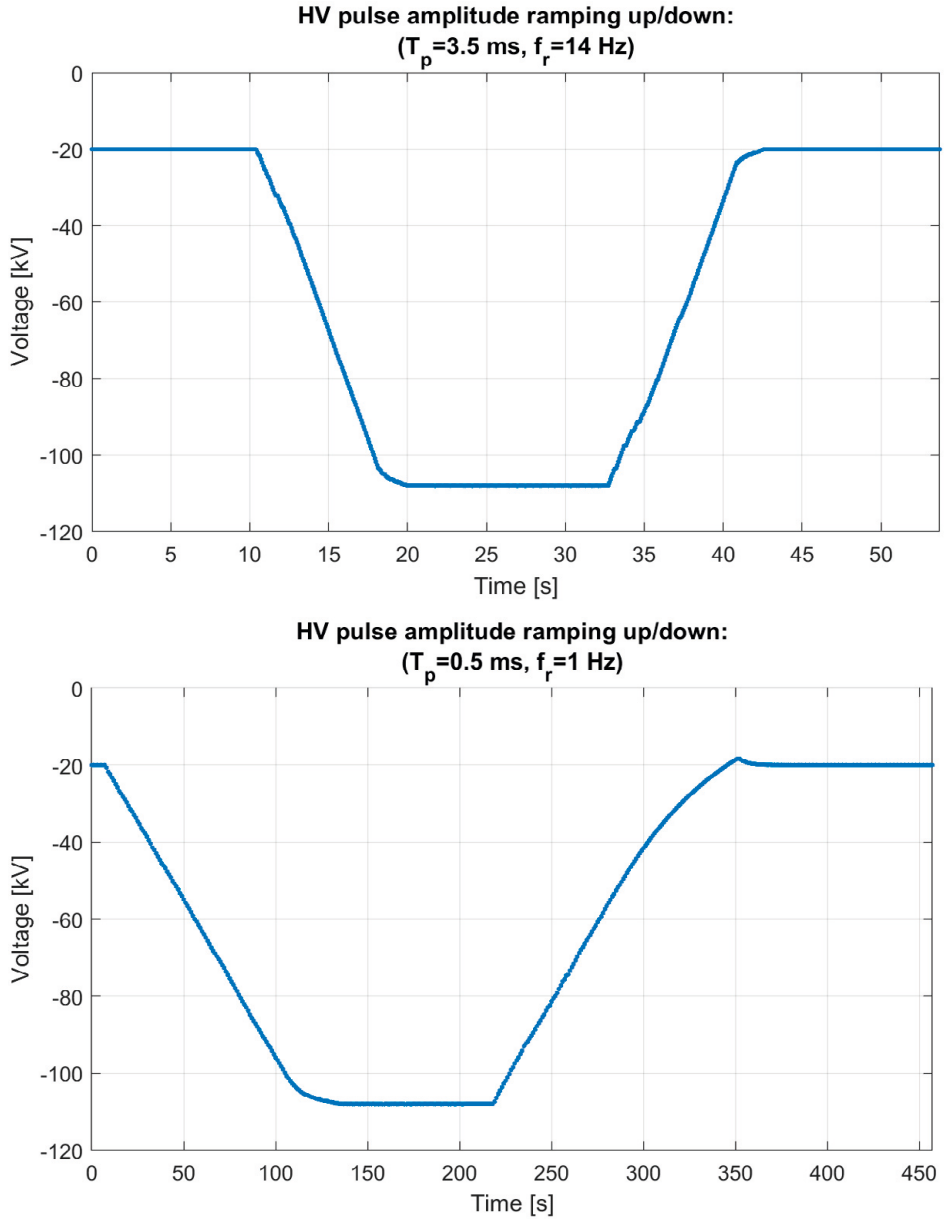



Figure 9.80: Ramping the pulse amplitude from -20 kV to -108 kV, and then back to -20 kV- a) 3.5 ms pulses repeated at 14 Hz; b) 0.5 ms pulses repeated at 1 Hz

*Transient performance: step change of pulse repetition rate*

Finally, Figure 9.81 shows the response in HV pulse amplitude to a step change in pulse repetition rate from 1 Hz to 14 Hz. As can be seen, despite the large transient incurred, the HV pulse amplitude deviates less than 8% of the nominal value with a recovery time of less than 2 seconds. Importantly, the main capacitor bank voltage and line currents are correctly adjusted during the transient without exceeding fault levels or activating modulator interlocks.

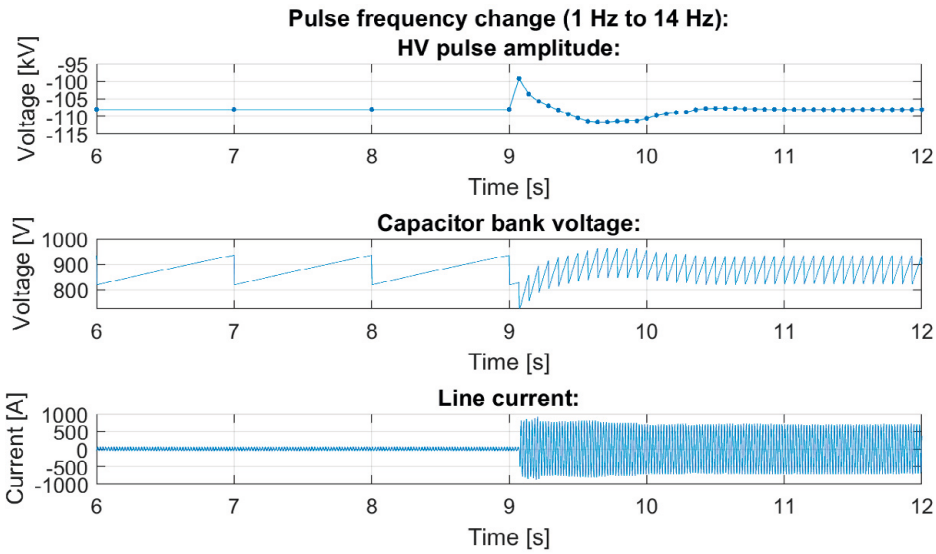



Figure 9.81: Modulator response to step change to pulse repetition rate from 1 Hz to 14 Hz (-108 kV, 96 A, 3.5 ms).

## 9.6.2 AC power quality

Figure 9.82 shows measured modulator line voltage and line current. This measurement was obtained simultaneously to those presented in Figure 9.78. As shown in Figure 9.82.b, the line current amplitude is approximately constant over time. Here, the amplitude fluctuation over two complete pulse periods is less than 2% across the three phases. The corresponding impact on line voltage flicker is negligible in accordance with that presented in chapter 7. Additionally, the line current waveforms are approximately sinusoidal and in phase with the corresponding line voltage waveforms. Here, the precision power analyzer measured an effective power factor of ~0.99. Finally, Figure 9.83 presents the harmonic spectrum of the line current waveforms shown in Figure 9.82. Here, the calculated line current THD is on the order of 1.5%, well below that of applicable standards.

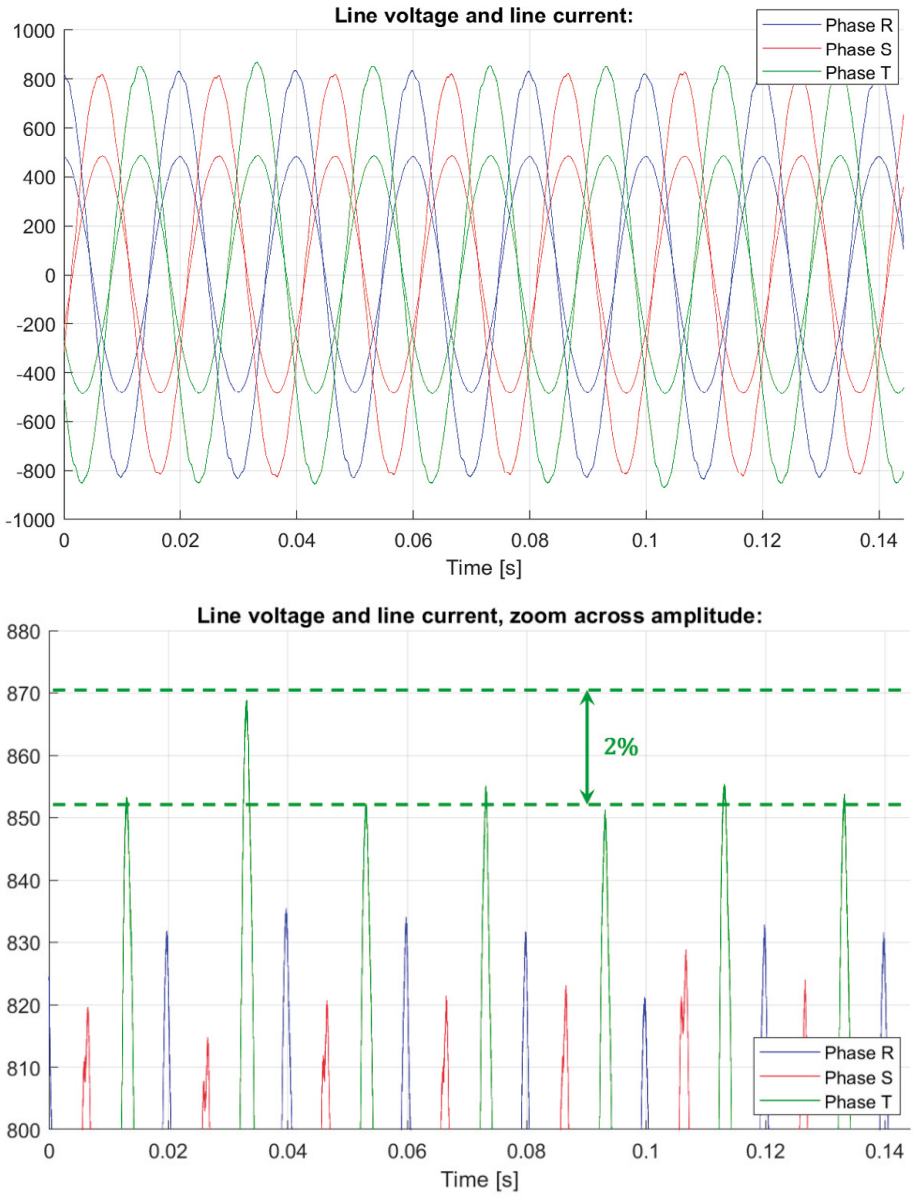



Figure 9.82: Measured line voltage and line current in nominal operation condition

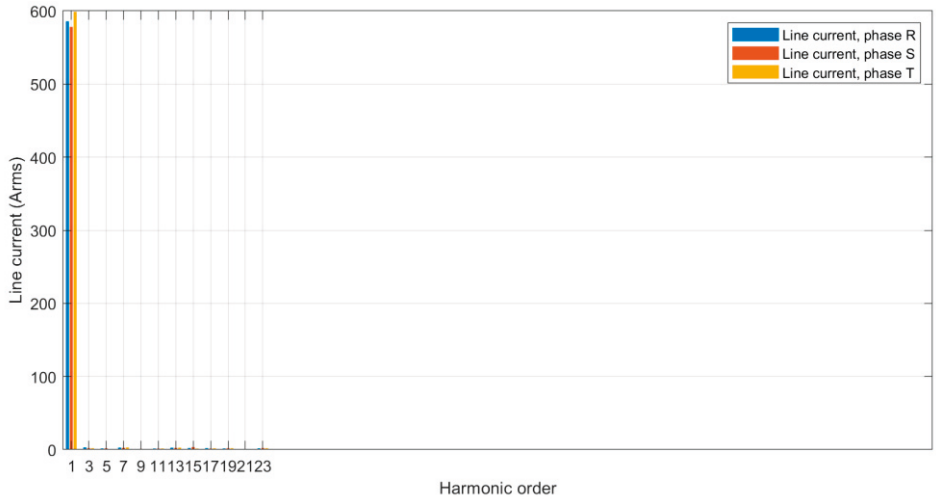



Figure 9.83: Harmonic spectrum of line currents shown in Figure 9.82

### 9.6.3 Modulator efficiency

Figure 9.84 shows the result of an efficiency measurement carried out on the developed full-scale modulator. Here, measurement group 1 represents the measurement on the modulator power input, i.e., before the EMC filter in Figure 9.2. The line voltages were measured directly using the voltage measurement interface of the L60-CH-A1 power measurement channels. The line currents were measured interfacing with the PCT600 precision current transducer. Measurement group 2 represents the measurement on the modulator output, i.e., the output pulse voltage and pulse current. Here, the output pulse voltage was measured with the VD-100 high-voltage probe from North Star, [9.42]. This probe has a DC accuracy better than 0.1%, and better than 1% considering frequencies up to 1 MHz, [9.42]. The output pulse current was measured by placing the four return cables through a single PCT600 precision current transducer, [9.43].

The measured modulator average input power is ~584.8 kW. Here, there is a ~5% active power imbalance between phases. Note that the corresponding apparent power is ~586.2 kVA, representing the measured power factor of 0.998. The measured modulator output power is ~526.7 kW. The total system losses amount to ~58.3 kW, with measured system efficiency of 90.0%.


Figure 9.84: Efficiency measurement on SML modulator

### 9.6.4 Assessment of long-term pulse stability

Figure 9.85 shows the long-term pulse stability of the SML modulator feeding the RFQ klystron over a time period of 4 days and of 5 months. The stability is assessed indirectly from the phase of the RFQ RF phase in open loop condition (i.e., without the LLRF control system), in reality comprising the stability of not only the modulator but also the klystron, the circulator, the RF generator, and so on. As can be seen, the phase evolution over time has the same shape in all cases, irrespective of pulse length. However, an offset of ~2.5 degrees is seen over the 5-month period. This is attributed to temperature drift between the summer and winter seasons, and will be straightforwardly compensated by the LLRF control system once activated.

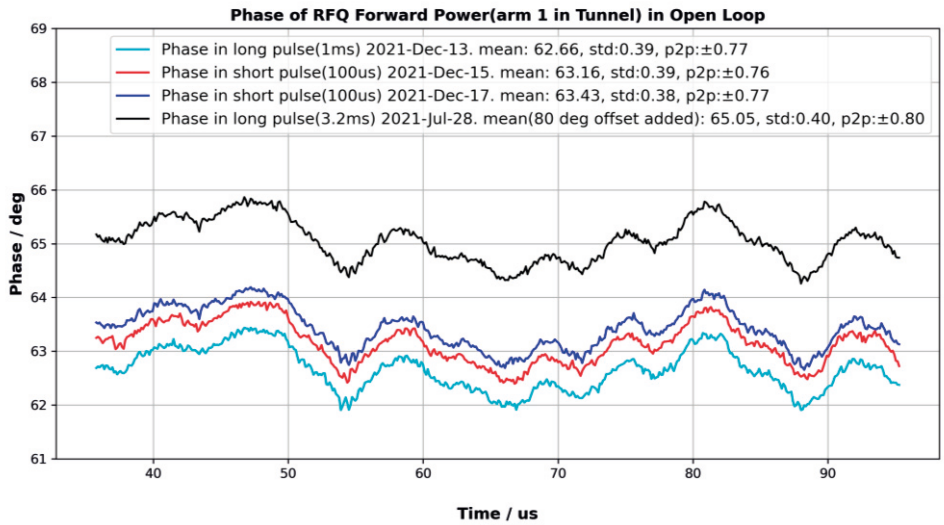



Figure 9.85: Long term pulse stability (108 kV/96 A/14 Hz) for different pulse lengths

### 9.6.5 Assessment of reliability from initial operations

As of today, ten SML modulators have successfully passed Site Acceptance Test, including at least 40 hours of full-power testing on high-voltage resistive load, and have been installed in the ESS Linac RF Gallery. One of these modulators has been driving klystron loads for over two years, cumulatively representing more than 2000 hours of operation. Additionally, three modulators have been used for klystron conditioning, with hundreds of hours of operation, and a final modulator has been used in the Superconducting RF test stand, with approximately 1000 hours of operation. No failures or malfunctions have been reported in any of these units.

## 9.7 References

[9.1] ABB 1SDA068208R1 XT1D. Accessed: June 24, 2023. [Online]. Available: https://new.abb.com/products/1SDA068208R1/xt1d-160-3p-f-f

[9.2] KEMET C44PKGR6100RBSJ. Accessed: June 24, 2023. [Online]. Available: https://www.kemet.com/en/us/capacitors/film/product/C44PKGR6100RBSJ.html

[9.3] KEMET C44PLGR6200RASJ. Accessed: June 24, 2023. [Online]. Available: https://www.kemet.com/en/us/capacitors/film/product/C44PLGR6200RASJ.html

[9.4] XTCE150G00TD

[9.5] MagComp. Accessed: June 24, 2023. [Online]. Available: https://www.magcomp.se/

[9.6] A. Reinap et al, "Evaluation of soft magnetic mouldable composite core motors," in Proc. of 2008 18th Int. Conf. on Elec. Machines, Vilamoura, Portugal, Sept. 2008, pp. 1-5.

[9.7] A. Reinap et al, "Prototype based study of different winding configurations with SM2C core," in Proc. of The XIX Int. Conf. on Elec. Machines (ICEM), Rome, Italy, Sept. 2010, pp. 1-6.

[9.8] SEMIKRON SKM400GB17E4 IGBT Module. Accessed: June 24, 2023. [Online]. Available: https://www.semikron-danfoss.com/products/product-classes/igbt-modules/detail/skm400gb17e4-22895010.html

[9.9] Electronicon E50 DC-Capacitors. Accessed: June 24, 2023. [Online]. Available: https://www.electronicon.com/en/products/dc-capacitors/pk16

[9.10] Vishay RPS0500DH47R0JB. Accessed: June 24, 2023. [Online]. Available: https://www.vishay.com/docs/50047/rps500.pdf

[9.11] IXYS VUO52-16NO1. Accessed: June 24, 2023. [Online]. Available: https://ixapps.ixys.com/datasheet/vuo52-16no1.pdf

[9.12] Siemens 3TG1001-0BB4. Accessed: June 24, 2023. [Online]. Available: https://mall.industry.siemens.com/mall/en/ww/Catalog/Product/3TG1001-0BB4

[9.13] Siemens 5SY4316-8. Accessed: June 24, 2023. [Online]. Available: https://mall.industry.siemens.com/mall/en/ww/Catalog/Product/5SY4316-8

[9.14] KEMET C20AKGR6100AASK. Accessed: June 24, 2023. [Online]. Available: https://www.kemet.com/en/us/capacitors/film/product/C20AKGR6100AASK.html

[9.15] Electronicon Kondensatoren GmbH. Accessed: June 24, 2023. [Online]. Available: https://www.electronicon.com/

[9.16] Mitsubishi Electric CM1800HC-34N IGBT Module. Accessed: June 24, 2023. [Online]. Available: https://www.mitsubishielectric.com/semiconductors/php/eTypeNoProfile.php?TYPENO=CM1800HC-34N&FOLDER=/product/powermodule/hvigbt_ipm/n_series

[9.17] Electronicon E50 DC-Capacitors. Accessed: June 24, 2023. [Online]. Available: https://www.electronicon.com/en/products/dc-capacitors/pk16

[9.18] TE Connectivity Resistors. Accessed: June 24, 2023. [Online]. Available: https://www.te.com/usa-en/plp/resistors/Y30xv.html

[9.19] Schneider Electric Industrial Contactors. Accessed: June 24, 2023. [Online]. Available: https://www.se.com/ww/en/product-subcategory/1510-industrial-contactors/?filter=business-4-low-voltage-products-and-systems

[9.20] Vacuumschmelze Amorphous and Nanocrystalline Cores. Accessed: June 24, 2023. [Online]. Available: https://vacuumschmelze.com/products/inductive-components-and-cores/amorphous-and-nanocrystalline-cores

[9.21] IXYS DSEP90-12AZ. Accessed: June 24, 2023. [Online]. Available: https://ixapps.ixys.com/DataSheet/DSEP90-12AZ.pdf

[9.22] TDK UHV-12A. Accessed: June 24, 2023. [Online]. Available: https://product.tdk.com/en/search/capacitor/ceramic/uhv/info?part_no=UHV-12A

[9.23] Metallux AG High-voltage Resistors. Accessed: June 24, 2023. [Online]. Available: https://www.metallux.ag/products/high-voltage-resistors/

[9.24] Ohmite Maxi-Mox Series. Accessed: June 24, 2023. [Online]. Available: https://www.ohmite.com/catalog/maxi-mox-series

[9.25] Zimmer LMG670 Power Analyzer. Accessed: June 24, 2023. [Online]. Available: https://www.zes.com/en/Products/Predecessor-Products/Energy-and-Power-Meters/LMG670

[9.26] Zimmer L60-CH-A1 Measurement Channel. Accessed: June 24, 2023. [Online]. Available: https://www.zes.com/en/Products/Predecessor-Products/Energy-and-Power-Meters/LMG670

[9.27] Zimmer HST Precision Wideband High Voltage Divider. Accessed: June 24, 2023. [Online]. Available: https://www.zes.com/en/Products/Sensors/HST

[9.28] Zimmer PCT (Precision current transducer). Accessed: June 24, 2023. [Online]. Available: https://www.zes.com/en/Products/Sensors/PCT

[9.29] FUSS 3F690-800.260. Accessed: June 24, 2023. [Online]. Available: https://www.fuss-emv.de/fileadmin/documents/produktdatenblaetter/emi-filter/emv-netzfilter/3F690-xxx.260_UL.pdf

[9.30] ABB 1SDA062658R1. Accessed: June 24, 2023. [Online]. Available: https://new.abb.com/products/1SDA062658R1/t7h-800-pr231-p-ls-i-in-800a-3p-f-f-m

[9.31] Electronic AC Power Capacitor E62.N12-104C60. Accessed: June 24, 2023. [Online]. Available: https://www.electronicon.com/en/products/ac-power-capacitors/e62

[9.32] Electronic AC Power Capacitor E62.P17-204C60. Accessed: June 24, 2023. [Online]. Available: https://www.electronicon.com/en/products/ac-power-capacitors/e62

[9.33] Schneider Electric LC1F330. Accessed: June 24, 2023. [Online]. Available: https://www.se.com/se/sv/product/LC1F330/kontaktor-3-polig-tesys-f-ac3-330a-160kw-utan-spole/

[9.34] Vishay RPS0500DH47R0JB. Accessed: June 24, 2023. [Online]. Available: https://www.vishay.com/docs/50047/rps500.pdf

[9.35] SEMIKRON SKD 53 Bridge Rectifier Module. Accessed: June 24, 2023. [Online]. Available: https://www.semikron-danfoss.com/products/product-classes/bridge-rectifier-modules/detail/skd-53-072328100723282007232830072328400723285007232860.html

[9.36] ABB 1SAM350000R1006. Accessed: June 24, 2023. [Online]. Available: https://new.abb.com/products/1SAM350000R1006/ms132-1-6

[9.37] Kyocera AVX DC Filtering Capacitors (FFLC). Accessed: June 24, 2023. [Online]. Available: https://www.kyocera-avx.com/products/film-capacitors/medium-power-film-caps/fflc/

[9.38] NI cRIO-9039 CompactRIO Controller. Accessed: June 24, 2023. [Online]. Available: https://www.ni.com/sv-se/support/model.crio-9039.html

[9.39] NI-9149 CompactRIO Chassis. Accessed: June 24, 2023. [Online]. Available: https://www.ni.com/sv-se/support/model.ni-9149.html

[9.40] NI TSM-1017 Industrial Touch Screen Monitor. Accessed: June 24, 2023. [Online]. Available: https://www.ni.com/sv-se/support/model.tsm-1017.html

[9.41] NI C Series Voltage Input Modules. Accessed: June 24, 2023. [Online]. Available: https://www.ni.com/sv-se/shop/hardware/products/c-series-voltage-input-module.html

[9.42] North Star High Voltage VD-100. Accessed: June 24, 2023. [Online]. Available: https://www.highvoltageprobes.com/product/vd-100/

[9.43] Zimmer PCT (Precision current transducer). Accessed: June 24, 2023. [Online]. Available: https://www.zes.com/en/Products/Sensors/PCT

# 10. Summary and conclusions

This doctoral dissertation treats topics related to power converters and electromagnetic components for pulse power generation in particle accelerator applications. Whereas the main focus is the development of a modulator topology suitable for long-pulse high-power applications - in particular considering the exceptional requirements presented by the ESS linac - other pulse power applications and aspects have also been treated. This chapter summarizes this doctoral dissertation work and presents the main conclusions:

- The review of state-of-the-art modulator technology reveals that there are appreciable challenges in increasing modulator power and attainable pulse length considering existing technology. Adoption of these technologies implies use of either a small number of very large components or a large number of very small components; corresponding to issues related to complexity as well as challenges in appropriate component design and system maintainability. Importantly, while these issues are already substantial in present-day applications, these issues are further magnified in scaling, especially as pulse flat top performance must be maintained or even improved over an extended pulse length period. Additionally, as the footprint of existing systems are demonstrably large, increased system average power levels are likely to result in prohibitive system designs.

- The Stacked Multi-Level (SML) topology is presented. The topology is based on hard-switched power converters, greatly benefiting from limited modularity (use of 4..10 generator modules is appropriate). Importantly, the topology promotes use of standardized, commercial off-the-shelf low voltage semiconductor components and furthermore avoids placement of active switches in the high-voltage oil tank assembly, greatly enhancing maintainability. The topology also incorporates a novel capacitor charger structure and control strategy eliminating flicker despite high-power pulsed operation. Finally, the topology features a great degree of freedom and potential for optimization in design as well as in output pulse waveform control.

- Design models and an integrated optimization framework for the conventional pulse transformer-based modulator topology are presented. Importantly, considering particularly the pulse transformer unit itself, analytical equations expressing the maximum attainable pulse length as a function of the application parameters and system constraints are developed. It is demonstrated that high-voltage pulse transformers intended for long-pulse high-power applications -

irrespective of winding technique - are very large and may weigh upwards of 10,000 kg and may be over 2 m tall. As presumed considering the review of the state-of-the-art, the often-beneficial simplicity of the pulse transformer-based topology here represents appreciable challenges, particularly with respect to component design, component size, system maintainability and, in extension, system scalability.

- Design models and an integrated optimization framework for the SML modulator topology are presented. Applying the optimization framework to the case of the ESS linac, a solution with a system footprint of ~4.8 $m^2$ and efficiency of ~90.7% was selected. This solution is implemented as described in chapter 9, where the final system footprint ~5.3 $m^2$ and measured efficiency >90% are attained.

- The developed optimization frameworks (i.e., considering the conventional pulse transformer-based modulator topology as well as the proposed SML modulator topology) are set to optimize designs considering a fixed output (115 kV and 100 A, representing a typical high-power klystron output) and with the pulse length varying from 1 to 5 ms and the pulse repetition rate varying from 1 to 50 Hz. Considering the ESS application (i.e., 3.5 ms and 14 Hz), adoption of the SML modulator topology permits a reduction in modulator footprint and absolute volume of up to 30% with respect to the conventional pulse transformer-based modulator topology. Considering applications with considerably longer pulse length or higher pulse repetition rate, even greater benefits are seen. As an example, considering applications with twice the pulse length or twice the pulse repetition rate, the SML modulator footprint and absolute volume approaches only half that of the corresponding pulse transformer-based modulator. Importantly, taking into account also the issues of manufacturability and maintainability, this comparison indicates an approximate delineation of the theoretical and practical limits of the pulse transformer-based modulator as well as the range of applications where the added complexity of the proposed SML modulator topology is justified.

- A novel capacitor charger structure and control strategy eliminating flicker despite high-power pulsed operation is developed and compared to conventional charging methods. Considering ESS application requirements, simulations indicate that conventional charging would result in flicker exceeding the levels prescribed in standards by more than 500%. At the same time, the proposed charging method features flicker levels an order of magnitude below that prescribed in standards (i.e., flicker reduction of ~50 times with respect to conventional charging methods). The proposed charging method is verified experimentally, including the verification of system dynamics in response to transient events. Here, it is verified that the proposed method is able to eliminate flicker within one pulse cycle following a step change in either pulse length, voltage setpoint, or pulse repetition rate.

- A detailed transfer function-based model of the modulator is derived for use in the analysis and design of the output pulse waveform controller. Here, the classical PI controller is used in benchmarking the selected open loop controller. A method for

automatic synthesis of the open loop reference waveform is developed, characterized and implemented. The proposed method is verified experimentally.

- The development of a reduced-scale technology demonstrator (115 kV, 20 A, 3.5 ms, 14 Hz) as well as the series full-scale modulators (115 kV, 100 A, 3.5 ms, 14 Hz) now in use at ESS is detailed, including a complete description of component selection and design, simulation results (circuit simulation as well as finite element analysis) and experimental results. Nominal load experiments (115 kV, 100 A, 3.5 ms, 14 Hz) carried out on the full-scale modulator system feature a pulse rise time of ~120 μs and a combined flat top ripple and droop below 0.15% of the pulse amplitude, well in accordance with design specifications. The pulse-to-pulse reproducibility is assessed through the statistical pulse amplitude variation, and is verified to be less than 0.05%. Finally, the corresponding line-side current THD is ~1.5%, the power factor exceeds 0.99, and the efficiency exceeds that of 90%.

# Appendix A – Capacitor design procedure

Klystron modulators contain several high-power capacitor elements that need to be dimensioned and appropriately selected. This appendix describes a general capacitor selection procedure based on a catalogue tabulating the key performance characteristics of commercially available capacitors, Figure. A.1. In the catalogue, each row $i$ represents a specific capacitor reference and is defined by the per-unit capacitance, the maximum capacitor voltage rating, the peak and RMS current ratings, the per-unit size, and the equivalent series parameters.

To design a capacitor configuration using this catalogue, the required capacitance value is translated into the required number of parallel capacitor units for each capacitor reference according to (A.1). This condition ensures that the required capacitance value is obtained without exceeding peak or rms current limits. Here, $C$ is the required capacitance, $I_c$ is the expected capacitor RMS current and $\hat{\imath}_C$ is the expected capacitor peak current. Capacitor reference $i$ is specified by its per-unit capacitance value $C(i)$, the maximum RMS current per capacitor unit $\hat{I}_C(i)$ and the maximum peak current per capacitor unit $\hat{\imath}_C(i)$.

$$N_C(i) = ceil\left[max\left[\left[\frac{C}{C(i)}\right], \left[\frac{I_c}{\hat{I}_C(i)}\right], \left[\frac{\hat{\imath}_C}{\hat{\imath}_C(i)}\right]\right]\right] \tag{A.1}$$

The conditions given by (A.2) and (A.3) are then applied to exclude references which 1) do not fulfil peak voltage requirements (avoiding series connection of capacitors) and which 2) yield a capacitance deviating too far from the expected value, respectively. Here, $\hat{V}_C$ is the expected peak capacitor voltage, $V_{C,max}(i)$ is the rated voltage of capacitor reference $i$, and $k_s$ represents the margin used in design.

$$\hat{V}_C \leq k_s V_{C,max}(i) \tag{A.2}$$

$$|C - N_C(i)C(i)| \leq \varepsilon_C \tag{A.3}$$

In most cases considered in this thesis, capacitor power losses may be neglected due to the large number of parallel connected capacitor units. Consequently, capacitor references which fulfil the above constraints may be evaluated and compared in terms of their total volume, (A.4), where $\emptyset(i)$ and $h(i)$ are the diameter and height of capacitor reference $i$.

$$V_C(i) = N_C(i)\emptyset^2(i)h(i) \tag{A.4}$$

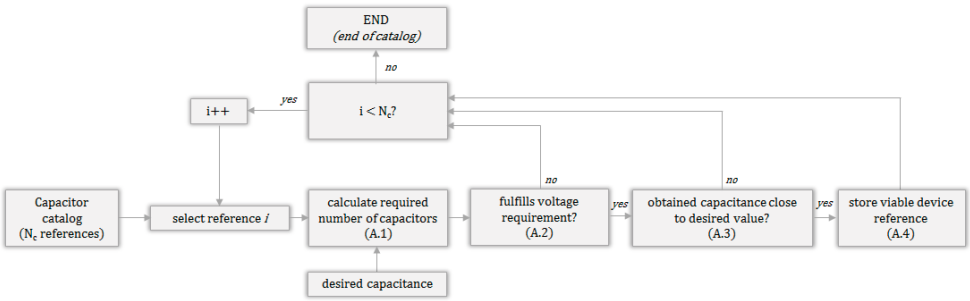



Figure A.1: Overview of capacitor selection procedure

# Appendix B – Selection of power modules in pulse power applications

Klystron modulators are high-power pulsed converters with expected system lifetime beyond ~25 years. With this expectation, modulator subsystems must be rugged and must be designed for continuous and reliable operation at their full ratings. For semiconductor devices, fulfilment of this requirement is usually ensured by selecting a device whose ratings comfortably surpass the requirements of specified application operating points. Most often, this means choosing a device 1) with an appropriate blocking voltage and 2) which generates acceptable power losses for the intended operating points, i.e., resulting in good converter efficiency without exceeding the maximum device junction temperature. However, in high-power pulsed applications, significant power is converted during - relatively speaking - very short periods of time resulting in considerable peak power losses and thereby a corresponding increase in the device junction temperature. Pulses are often repeated at tens of Hz, i.e., in thermal steady state it is clear that - considering typical thermal time constants of, e.g., the semiconductor module case or the converter heatsink - the surroundings will remain at an essentially fixed temperature whereas the semiconductor chip as well as the bond wires and solder will all cycle with some temperature difference $\Delta T$ at pulse frequency, Figure. B.1. This phenomenon is called power cycling and is the cause of multiple aging and failure mechanisms, e.g., bond wire lift-off due to thermal expansion. Power cycling and its effects on semiconductor lifetime have been studied and documented. Most often, results are summarized in a graph depicting the number of power cycles to device failure versus cycle temperature difference $\Delta T$ with the average junction temperature as parameter, Figure. B.2.

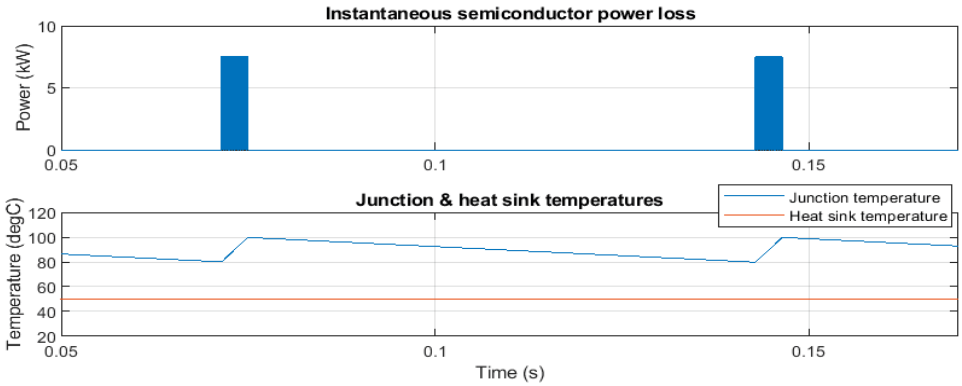



Figure B.1: Power cycling - significant losses are generated during the pulse event resulting in a considerable junction temperature increase. In this example, the pulse event is 3.5 ms long and is repeated at 14 Hz. The average device losses are only a few hundreds of Watts, and despite that the maximum junction temperature is only 100 DegC - well below the permissible temperatures of modern semiconductor devices - the expected lifetime of the device is only ~1 year according to reported data summarized in Figure. B.2.

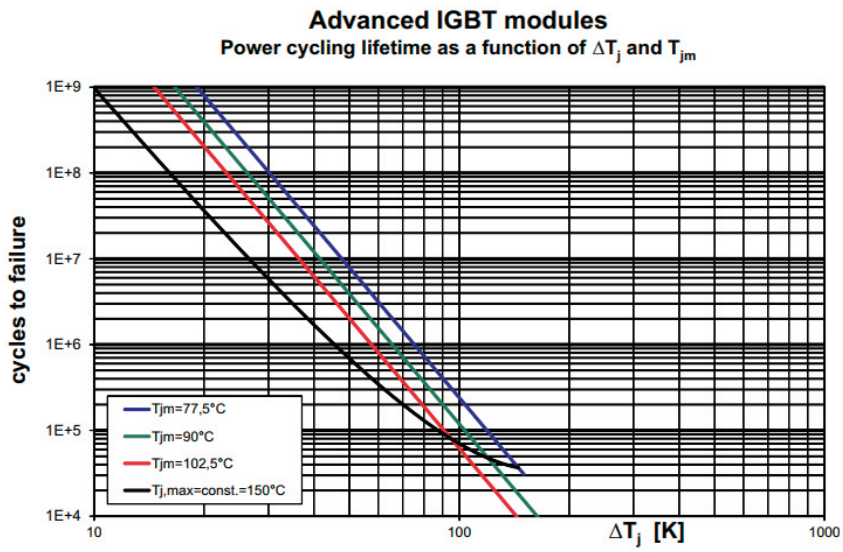



Figure B.2: Number of power cycles to failure as function of temperature swing $\Delta T$ with the average junction temperature as parameter. The figure has been reprinted from [3.3].

In the following, a semiconductor selection procedure suitable for pulse power applications is described, Figure B.3. The procedure is based on a catalog of commercially available semiconductor devices tabulating key performance characteristics obtained from datasheets. For IGBT modules, these performance characteristics include the maximum blocking voltage, the nominal chip current, the repetitive peak collector current, the collector-emitter threshold voltage, the on-state slope resistance, the switch on- and switch off energy dissipations, the junction-to-

case thermal resistance, the case-to-heatsink thermal resistance, and the transient thermal impedance parameters. The corresponding parameters for the module anti-parallel diode are also stored. Additionally, the assumed conditions for these performance characteristics are stored to permit scaling to different operating points.

To utilize the catalog for design purposes, expressions for the converter conduction and switching losses as a function of expected circuit waveforms as well as the application pulse length and pulse repetition rate must be supplied along with an equivalent thermal network matching the intended device layout. With this information at hand, the procedure entails estimating the average junction temperature as well as the junction temperature swing from the calculated power losses and the equivalent thermal network. If the peak junction temperature is too high, parallel modules may be added to split the current thereby reducing individual module losses. Once the peak junction temperature is within device limitations (or the system is too complex to be considered viable), the converter lifetime may be estimated using fits of the curves presented in Figure. B.2. Automatizing this process, one can quickly characterize the complete semiconductor catalog and be presented with viable choices in terms of, e.g., efficiency, power stack volume, complexity (e.g., by way of number of modules), estimated lifetime, or other interesting performance criteria.

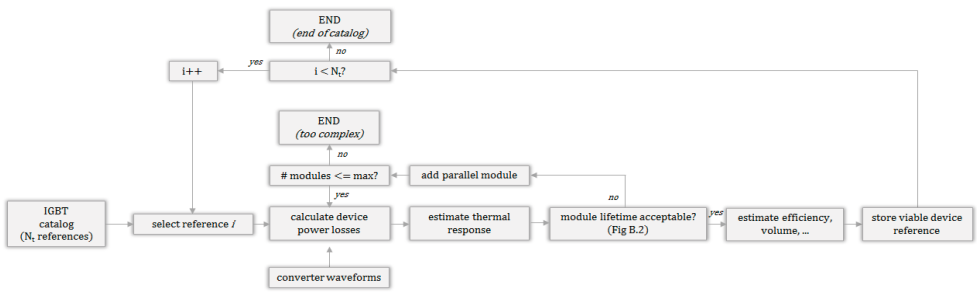



Figure B.3: Overview of semiconductor selection procedure for pulse power applications