III-V Devices for Emerging Electronic Applications

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III-V Devices for Emerging Electronic Applications

Doctoral Thesis

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Abstract

TODAY's digitalized society relies on the advancement of silicon (Si) Complementary Metal Oxide Semiconductor (CMOS) technology, but the limitations of down-scaling and the rapidly increasing demand for added functionality that is not easily achieved in Si, have pushed efforts to monolithically 3D-integrate III-V devices above the Si-CMOS technology. In addition, the demand for increased computational power and handling of vast amounts of data is rapidly increasing. This has led to an increased interest in quantum computing, offering the potential to solve specific complex problems more efficiently than conventional computers. Superconducting transmon Quantum Bits (qubits) are promising for the realization of quantum computers, which has led to an increased interest in cryogenic electronics. For these applications, III-Vs are suitable as their high carrier mobility enables low power consumption, low noise, and highly transparent superconductor-semiconductor interfaces. High-quality interfaces between superconductors and semiconductors are crucial for the implementation of gate-tunable hybrid superconductor-semiconductor qubits known as gatemon qubits.

This thesis explores the potential of utilizing indium arsenide (InAs) and indium gallium arsenide (InGaAs) nanowire and quantum well devices in these emerging electronic applications. Both as an add-on in Si-CMOS technology, as well as the channel material in electronic devices for cryogenic applications.

The electron transport in near-surface quantum wells is studied by DC-measurements in combination with applied magnetic fields, from room temperature down to cryogenic temperatures. Several different ways to extract

the carrier mobility are investigated, such as standard current-voltage sweeps, the Geometrical Magnetoresistance Effect (gMR), as well as the Hall effect. A deeper understanding of electron transport at cryogenic temperatures is obtained by the development of a model for the current characteristics of long-channel InGaAs quantum well Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), which includes the effects of band tail states, electron concentration-dependent mobility, and interface trap density. The model shows an increased effect of remote impurity scattering associated with mobility degradation in the subthreshold region.

A demultiplexer based on an InGaAs nanowire network was fabricated, to enable routing of DC-currents on-chip and reduce the number of connections to the cryostat. To facilitate system-level investigation of circuits containing Josephson Field-Effect Transistors (JoFETs), a compact model was developed which by circuit simulations accurately reproduced the measured data from our JoFET.

Finally, a process for the growth of InAs nanowires on tungsten was developed. This novel approach is based on Template-Assisted Selective Epitaxy (TASE) and allows for easy 3D-integration of III-V devices in Si-CMOS technology.

Populärvetenskaplig sammanfattning

I dagens digitala samhälle är man alltid tillgänglig, uppkopplad, och uppdaterad. Datorer, smarta mobiltelefoner och internet har revolutionerat våra liv. Den genomsnittliga användaren använder till exempel sin smarta telefon under totalt mer än tre timmar varje dag uppdelat på 58 tillfällen. Grunden för den här utvecklingen började 1947 på Bell laboratories i New Jersey, då de tre forskarna Shockley, Bardeen och Brattain hade tillverkat den första fungerande transistorn. Denna upptäckt gav dem senare Nobelpriset i fysik, och anses idag vara en av de viktigaste uppfinningarna någonsin.

I princip all dagens elektronik innehåller transistorer. En transistor har tre kontakter, source, drain och gate. Gaten används för att styra strömmen som går mellan source och drain, likt en ventil som styr flödet av vatten mellan två vattentankar. Storleken på strömmen mellan source och drain kan ändras med en faktor 100 000 genom att ändra potentialen på gaten några tiondels volt. Detta möjliggör för snabba beräkningar i det binära talsystemet där ”1:or” och ”0:or” motsvaras av hög respektive låg ström i dagens datorer. Ett annat viktigt användningsområde för transistorer är som förstärkare av elektriska signaler, vilket är essentiellt för att ta emot och skicka information över internet och telenätet.

Den extremt snabba prestandautvecklingen av dagens elektronik baseras främst på att transistorerna blir mindre och mindre. Idag finns det flera miljarder transistorer på en yta av några hundra kvadratmillimeter. Detta medför att beräkningar kan ske snabbare och till lägre effektförbrukning. Gränsen för hur små transistorerna kan bli börjar dock närma sig, då vissa strukturer

bara består av några atomlager. Ett problem som uppstår då transistorernas dimensioner blir mindre är att det blir svårare att kontrollera strömmen i kanalen mellan source och drain. För att mer effektivt kunna styra strömmen har nya kanal-geometrier utvecklats. Från att ha varit plana strukturer, där gaten bara påverkar kanalen mellan source och drain från en sida, har kanalstrukturer i form av fenor och trådar utvecklats. Det möjliggör kontroll av strömmen genom kanalen från flera sidor. Ett möjligt sätt att förbättra prestandan utan att minska storleken ytterligare, är att tillverka transistorer av andra material. Historiskt sett har halvledaren kisel använts som material i kanalen, men i andra halvledare kan elektronerna färdas snabbare vilket ökar prestandan. Till exempel har kombinationer av material från grupp 13 och 15 i det periodiska systemet visat sig ge elektronerna mycket högre mobilitet. Dessa kristaller, som brukar kallas III-V halvledare, utklassar kisel i vissa applikationer men är samtidigt dyrare och mer sällsynta. Att helt och hållet ersätta kisel med III-V halvledare är därför väldigt osannolikt, men att integrera III-V halvledare i kiselbaserad teknologi skulle medföra ökad prestanda och funktionalitet. Det är dock en komplex uppgift, eftersom kisel och III-V halvledarna har olika avstånd mellan atomerna i kristallerna så måste de växas på olika substrat och sedan flyttas över till samma substrat. I denna avhandling har vi undersökt ett annat alternativ. Vi har utvecklat en process för att växa kristaller av III-V halvledare direkt på en metall, och vilket substrat som används spelar därför ingen roll. Denna metod har därför potential att möjliggöra integrering av III-V halvledare på kiselsubstrat.

Ett annat intressant tillvägagångssätt för att öka beräkningskapaciteten är att byta ut de digitala bitarna ”1” och ”0” mot kvantbitar, som utöver ”1” eller ”0” även kan vara i en superposition av dessa två tillstånd. Det möjliggör att vissa typer av komplexa beräkningar som skulle ta orimligt lång tid att utföra på en konventionell dator, kan utföras parallellt. Viktiga användningsområden för kvantdatorer skulle vara inom områden där stora mängder data hanteras, till exempel inom medicinforskning, energioptimering, finansiell modellering, och kryptering. En av de mest lovande kvantbitarna baseras på att vissa metaller blir supraledande vid temperaturer nära absoluta nollpunkten (-273.15°C). Vid dessa låga temperaturer blir effektförbrukningen och inverkan av brus särskilt viktigt. Elektroner med hög mobilitet har visat sig minska både effektförbrukningen och bruset, vilket gör III-V halvledare intressanta även för dessa användningsområden. I denna avhandling fokuserar vi på att tillverka högpresterande transistorer av III-V material, och studera elektrontransporten vid temperaturer nära absoluta nollpunkten.

Acknowledgments

TIME has swiftly passed as I've enjoyed every moment of my Ph.D. studies! Working with numerous inspiring individuals has been a true delight and has played a pivotal role in bringing this thesis to fruition. First and foremost, I extend my gratitude to my supervisors, *Erik Lind* and *Mattias Borg*. Thank you for dedicating your time and effort to make this work possible. Your expertise and guidance have been indispensable throughout these years, and I am sincerely thankful for that. Special thanks to *Johannes Svensson* for always keeping your door open and for being ready to discuss cleanroom work, EBL-designs and so much more. *Lars-Erik Wernersson*, thank you for creating this fantastic research environment.

A great thank you to *Lasse* for the countless hours we spent together in the cleanroom and the stimulating discussions about sample designs and measurements. I also express my appreciation to *Louise*, not only my younger sister but also one of my closest friends. It has been a pleasure exploring the realm of superconductivity with you, and I am confident in your success during your Ph.D. and future career. To an old friend, *Robin*, who would have thought when we first met at 16 that we would spend the next 12 years studying together! Your presence as a colleague and friend has always been a source of security, and I am genuinely grateful for that.

I also want to thank all fantastic colleagues I have had the opportunity to work with, thank you *Sebastian*, *Olli-Pekka*, *Markus*, *Fredrik*, *Stefan*, *Adam*, *Johan*, *Anton*, *Heera*, *Abinaya*, *Saketh*, *Navya*, *Zhongyunshen*, *Gautham*, *Hannes*, *Marcus*, *Ben*, *Niklas*, *André*, *Alexandros*, *Paula*, *Karthik*, *Philipp*, *Anette*, *Ngoc-Duc*, *Lars*, *Mats*, *Daniel*, and *Karl-Magnus*.

Finally, I extend my deepest gratitude to my family for their unwavering support and encouragement. None of this would have been possible without you!

And to *Linn*, just as there are fundamental laws in nature stating that energy cannot be created nor destroyed, you've made me realize another law—I cannot live without you!

Lund, February 2024

Contents

Preface

This thesis is the culmination of five years of work in the *Electromagnetics and Nanoelectronics* division at the Department of Electrical and Information Technology, Lund University, and presents detailed studies of III-V devices at cryogenic temperatures, as well as their potential integration in Si-CMOS technology. The work was supervised by Professor *Erik Lind* and Associate Professor *Mattias Borg*.

STRUCTURE OF THE THESIS

The three main parts of this thesis are: Introduction, Appendices, and Papers. The introduction provides a summary of the research field, its development, and fundamental concepts. This part is intended to be comprehensible for aspiring researchers with a Master's degree in a related subject. The appendices contain detailed fabrication schemes, intended to work as a guide for future Ph.D. students, as well as a summary of R_C for different semiconductor/metal combinations, along with extracted values of μ_{EFF}. The papers appended in the back, form the main body of the thesis.

- **INTRODUCTION**
  The introduction aims to motivate the research performed in this thesis, provide a broader view of the research field, introduce its fundamental concepts, and make the appended publications understandable for readers with basic knowledge of semiconductor device physics.

- **APPENDICES**

  A Fabrication of Near-Surface Quantum Well Devices
  Appendix A provides a detailed process flow for the fabrication of near-surface quantum well devices.

B Fabrication of Lateral Nanowire Devices
Appendix B provides a detailed process flow for the fabrication of lateral nanowire devices.

C Fabrication of Vertical Nanowire Devices using TASE
Appendix C provides a detailed process flow for the fabrication of vertical nanowire devices using TASE.

D Summary of Extracted R_C and μ_{EFF}
Appendix D provides a summary of extracted R_C and μ_{EFF} for some different semiconductor/metal combinations.

- **PAPERS**
  The papers forming the main body of the thesis are reproduced in the back and listed in the following.

INCLUDED PAPERS

The following papers form the main body of this thesis and the respective published or draft versions are appended in the back.

Paper I: P. Olausson, L. Södergren, M. Borg, and E. Lind, "Optimization of Near-Surface Quantum Well Processing", *Physica Status Solidi (A) Applications and Materials Science*, vol. 218, no. 7, pp. 2000720, January 2021, doi: 10.1002/pssa.202000720.

► *I developed the process flow, fabricated the devices, carried out all electrical measurements and analyses, and wrote the paper.*

Paper II: P. Olausson, R. Yadav, R. Timm, and E. Lind, "Low temperature atomic hydrogen annealing of InGaAs MOSFETs", *Semiconductor Science and Technology*, vol. 38, no. 5, pp. 055001, March 2023, doi: 10.1088/1361-6641/acc08c.

► *I fabricated the devices, carried out all electrical measurements and analyses, and wrote the paper.*

Paper III: P. Olausson, and E. Lind, "Geometrical Magnetoresistance as a Tool for Carrier Mobility Extraction in InGaAs MOSFETs", *IEEE Transactions on Electron Devices*, vol. 70, no. 11, pp. 5614-5618, November 2023, doi: 10.1109/TED.2023.3318556.

► *I developed the process flow, fabricated the devices, carried out all electrical measurements and analyses, co-performed the simulations, and wrote the paper.*

Paper IV: L. Södergren, P. Olausson, and E. Lind, "Cryogenic Characteristics of InGaAs MOSFET", *IEEE Transactions on Electron Devices*, vol. 70, no. 3, pp. 1226-1230, March 2023, doi: 10.1109/TED.2023.3238382.

► *I fabricated the devices and carried out most of the electrical measurements and analyses.*

Paper V: L. Södergren, P. Olausson, and E. Lind, "Low-Temperature Characteristics of Nanowire Network Demultiplexer for Qubit Biasing", *Nano Letters*, vol. 22, no. 10, pp. 3884-3888, May 2022, doi: 10.1021/acs.nanolett.1c04971.

► *I co-fabricated the devices and assisted during electrical measurements and analyses.*

Paper VI: L. Olausson*, P. Olausson*, and E. Lind, "Gate-controlled near-surface Josephson junctions", *Applied Physics Letters*, vol. 124, no. 4, pp. 042601, January 2024, doi: 10.1063/5.0182485.

* *Contributed equally.*

► *I planned and performed the device fabrication, co-performed the measurements, performed most of the data analysis, and co-wrote the paper.*

Paper VII: J. Svensson*, P. Olausson*, H. Menon*, S. Lehmann, E. Lind, and M. Borg, "Three-Dimensional Integration of InAs Nanowires by Template-Assisted Selective Epitaxy on Tungsten", *Nano Letters*, vol. 23, no. 11, pp. 4756-4761, June 2023, doi: 10.1021/acs.nanolett.2c04908.

* *Contributed equally.*

► *I developed the process flow, fabricated the devices, and carried out all electrical measurements and analyses.*

RELATED WORK

The following publications are not included in the thesis, but summarize related work that I was involved in. The work is divided into peer-reviewed journal papers and conference contributions and is listed according to the thematic order of the thesis.

JOURNAL PAPERS

Paper viii: N.S. Garigapati, L. Södergren, P. Olausson, and E. Lind, "Strained $In_xGa_{(1-x)}As/InP$ near surface quantum wells and MOSFETs", *Applied Physics Letters*, vol. 120, no. 9, pp. 092105, March 2022, doi: 10.1063/5.0073918.

CONFERENCE CONTRIBUTIONS

Paper ix: J. Svensson, P. Olausson, H. Menon, E. Lind, and M. Borg, "Template-Assisted Selective Epitaxy of InAs on W", *Compound Semiconductor Week (CSW)*, Jun. 2022. doi: 10.1109/CSW55288.2022.9930423

Acronyms and Symbols

Here, important acronyms, abbreviations, and symbols are listed, which are recurring throughout the thesis. Some parameters, which only occur in a narrow context, are intentionally omitted; some parameters are used in more than one way, but the context is always explicitly clarified in the corresponding text. Some (compound) units are provided with prefixes to reflect the most commonly encountered notations in literature.

ACRONYMS AND ABBREVIATIONS

2DEG	2-Dimensional Electron Gas
AHA	Atomic Hydrogen Annealing
ALD	Atomic Layer Deposition
ART	Aspect Ratio Trapping
BEOL	Back-End-Of-Line
BOE	Buffered Oxide Etchant
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DIBL	Drain-Induced Barrier Lowering
DOS	Density Of States
EBL	Electron-Beam Lithography
EOT	Equivalent Oxide Thickness
FEOL	Front-End-Of-Line

FinFET	Fin Field-Effect Transistor
GAA	Gate-All-Around
gMR	Geometrical Magnetoresistance Effect
HSQ	Hydrogen Silsesquioxane
IC	Integrated Circuit
ICP	Inductively Coupled Plasma
IPA	Isopropanol
IRDS	International Roadmap For Devices and Systems
JJ	Josephson Junction
JoFET	Josephson Field-Effect Transistor
MBE	Molecular-Beam Epitaxy
MIBK	Methyl Isobutyl Ketone
MLA	Maskless Aligner
MOCVD	Metal-Organic Chemical Vapour Deposition
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PBTI	Positive-Bias Temperature Instability
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PMA	Post-Metal Annealing
pMR	Physical Magnetoresistance Effect
QCL	Quantum Capacitance Limit
qubit	Quantum Bit
RF	Radio-Frequency
RIE	Reactive Ion Etching
RTP	Rapid Thermal Process
SAE	Selective Area Epitaxy
SEM	Scanning Electron Microscope
S.I.	Semi-Insulating
SQUID	Superconducting Quantum Interference Device
SS	Subthreshold Swing
TASE	Template-Assisted Selective Epitaxy
TLM	Transfer Length Method
TMAH	Tetramethylammonium Hydroxide
TMAl	Trimethylaluminum

UVL	Ultraviolet Lithography

LATIN SYMBOLS

Al		Aluminum
Al_2O_3		Aluminum oxide
Ar		Argon
As		Arsenic
AsH_3		Arsine
Au		Gold
C_C	F m^{-2}	Centroid capacitance
C_G	F m^{-2}	Gate capacitance
CH_3COOH		Acetic acid
C_{IT}	F m^{-2}	Interface-trap capacitance
C_{OX}	F m^{-2}	Oxide capacitance
C_Q	F m^{-2}	Quantum capacitance
Cl		Chlorine
Cl_2		Chlorine gas
Cr		Chromium
d	m	Thickness of dielectric
D_{IT}	J^{-1} m^{-2}	Interface-trap density
D	m^2 s^{-1}	Diffusivity
E_U	J	Urbach energy
F		Fluorine
Fe		Iron
g_d	S	Output conductance
g_m	S	Transconductance
$Ga(CH_3)_3$		Trimethylgallium
Ge		Germanium
H_2		Hydrogen gas
H_2O		Water
H_2O_2		Hydrogen peroxide

$\mathbf{H_3PO_4}$		Phosphoric acid
$\mathbf{H_2SO_4}$		Sulfuric acid
HCl		Hydrochloric acid
HF		Hydrofluoric acid
$\mathbf{HfO_2}$		Hafnium dioxide
$\mathbf{HNO_3}$		Nitric acid
In		Indium
InAs		Indium arsenide
$\mathbf{In(CH_3)_3}$		Trimethylindium
InGaAs		Indium gallium arsenide
InP		Indium phosphide
$I_{\mathbf{DS}}$	A, mA µm^{-1}	Drain-Source current, often normalised by the gate width
$I_{\mathbf{OFF}}$	A, mA µm^{-1}	Off-current, often normalised by the gate width
$I_{\mathbf{ON}}$	A, mA µm^{-1}	On-current, often normalised by the gate width
$k_{\mathbf{B}}$		$\approx 1.381 \times 10^{-23}$ kg m^2 K^{-1} s^{-1}, Boltzmann's constant
$L_{\mathbf{G}}$	m	Gate length
$L_{\mathbf{G,EFF}}$	m	Effective gate length
$L_{\mathbf{T}}$	m	Transfer length
m_0	kg	$\approx 9.109 \times 10^{-31}$ kg, electron rest mass
m^*	m_0	Effective mass
Mo		Molybdenum
MoRe		Molybdenum rhenium alloy
n	m^{-3}	Carrier concentration
n_s	m^{-2}	Surface carrier concentration
$N_{\mathbf{2D}}$		2-dimensional effective density of states
$\mathbf{N_2}$		Nitrogen gas
$\mathbf{NH_4OH}$		Ammonium hydroxide
$\mathbf{(NH_4)_2S}$		Ammonium sulfide
Ni		Nickel
$\mathbf{O_2}$		Oxygen
Pd		Palladium

q		$\approx 1.602 \times 10^{-19}$ C, Elementary charge
Q_{CH}	C m^{-2}	Mobile channel charge density
R_{ACC}	Ω m	Access resistance
R_C	Ω m	Contact resistance
R_{CH}	Ω m	Channel resistance
R_{ON}	Ω	On-resistance
R_{SH}	Ω	Sheet resistance
SF_6		Sulfur hexafluoride
Si		Silicon
SiO_2		Silicon dioxide
Si_3N_4		Silicon nitride
Sn		Tin
Ti		Titanium
TiN		Titanium nitride
v_{SAT}	m s^{-1}	Saturation velocity
v_T	m s^{-1}	Thermal injection velocity
V_{DD}	V	Drive voltage
V_{DS}	V	Drain-Source voltage
V_{GS}	V	Gate-Source voltage
V_{HALL}	V	Hall voltage
V_{OV}	V	Overdrive voltage
V_T	V	Threshold voltage
W	m	Device width
W		Tungsten

GREEK SYMBOLS

χ	J	Electron affinity
Γ		Transmission coefficient
κ		Relative permittivity
λ	m	Mean free path

μ	$cm^2\ V^{-1}\ s^{-1}$	Mobility
μ_{FE}	$cm^2\ V^{-1}\ s^{-1}$	Field-effect mobility
μ_{EFF}	$cm^2\ V^{-1}\ s^{-1}$	Effective mobility
μ_{gMR}	$cm^2\ V^{-1}\ s^{-1}$	gMR mobility
μ_{HALL}	$cm^2\ V^{-1}\ s^{-1}$	Hall mobility
ϕ_M	J	Work function
ϕ_B	J	Schottky barrier
ρ	Ω m	Resistivity

INTRODUCTION

1

Background

CURIOSITY is one of the driving forces in our society, and research is the structured way to gain knowledge and drive innovation. From fundamental research, unraveling the mysteries of nature, to inventions such as smartphones and healthcare applications, research continues to form our society and the way we live our lives.

The cornerstone of the research performed in this thesis was developed already in 1947 when the first transistor was realized [1, 2]. From the inception of the initial transistor, transistor technology has undergone remarkable advancements, profoundly enhancing and transforming our daily existence. Today, the transistor is the most widely manufactured device in history, and in 1965 Gordon Moore presented his famous observation, that the number of transistors in an integrated circuit doubles every year (later revised to every second year) [3].

The transistor is the main building block of our digitalized society. But, what led to this development, and how long can it continue? In the following paragraphs, a brief overview will be provided of key milestones in the development of the transistor and the digitalization of the world.

The first transistor was fabricated from germanium (Ge), but in the late 1950s silicon (Si) replaced Ge as the dominant semiconductor material. Si has many advantages: it is the second most abundant material in earth's crust, withstands high temperatures, easy to purify, high density of states, good electron mobility, and forms a native oxide, silicon dioxide (SiO_2), which is suitable as an insulator between the gate electrode and channel in Metal-Oxide-Semiconductor Field-Effect Transistor (**MOSFET**) devices, see Fig. 1.1

for schematics of **MOSFET**s, and Chapter 2 for details on their working principles.

In 1958 another essential invention for today's digitalized society was realized: the Integrated Circuit (**IC**) [4]. The **IC** made it possible to easily fabricate smaller circuits and allowed for an increased number of components. The development has since then, relied on scaling of the transistor dimensions in order to improve the device performance, in terms of speed and energy efficiency, and increase the number of components on a chip. Today, some dimensions of the transistors are only a few atomic layers, and the limit for how small the device can be is thus approaching.

In 1960, the first **MOSFET** was fabricated [5]. The **MOSFET** is by far the most common transistor in today's digital circuits, and almost all calculations and logic functions are realized by Complementary Metal Oxide Semiconductor (**CMOS**) technology, i.e. combining p- and n-type **MOSFET**s. The **CMOS** is ideal for digital applications, since no current flows except when switching from on- to off-state.

A lot of research has been performed on new materials and device structures. For instance, III-V semiconductors outperform Si in certain applications, due to their direct band gap and higher carrier mobility. The direct band gap is beneficial in optoelectronic applications while the high mobility is utilized in high-frequency applications [6, 7]. Initially, III-Vs were intended to replace Si, but today they are instead viewed as a way to add new functionalities to Si digital technology [8–11]. One challenge with III-Vs is that their native oxide is of poor quality, and not suitable as a gate dielectric [12]. In 2003 an Atomic Layer Deposition (**ALD**) process was for the first time used to deposit a high-quality aluminum oxide (Al_2O_3) on top of a III-V semiconductor [13]. In addition to enabling high-performance III-V **MOSFET**s, the **ALD** process also allows for scaling of the oxide thickness and the possibility to deposit oxides with higher dielectric constant, κ. Scaling of the oxide is essential for maintaining good electrostatic control of the channel potential as the gate length is scaled down, while the high-κ value allows for a thicker oxide and less gate leakage current, for equivalent capacitive coupling to the channel. This is described by the Equivalent Oxide Thickness (**EOT**), which relates the high-κ thickness to the standard SiO_2 gate oxide,

$$\mathbf{EOT} = d\frac{\kappa_{SiO_2}}{\kappa}, \tag{1.1}$$

where d is the thickness of the dielectric.

For short gate lengths, the source and the drain potential will influence the channel potential and minimize the region of the channel controlled by the gate potential. In order to mitigate this problem, transistors with 3-dimensional channel structures have been realized, enabling gate control

from multiple sides. The 3-dimensional channel structure also enables denser packaging of the devices. In Fig. 1.1, **MOSFET**s with different channel geometries are presented. The Fin Field-Effect Transistor (**FinFET**), see Fig. 1.1 (b), has a channel in the shape of a fin, which enables gate control from three sides, making it possible to decrease the gate length further and still have good electrostatic control of the channel potential with the gate potential [14]. The **FinFET** became commercialized in the 2010s and is today the dominant channel design for logic devices [15]. However, according to International Roadmap For Devices and Systems (**IRDS**) a transition from **FinFET**s to Gate-All-Around (**GAA**) devices will take place to further increase the number of devices on a single chip. In 2022, Samsung introduced a **GAA** device structure in the form of stacked nanosheets, see Fig. 1.1 (c) [16]. Another variant of a **GAA** structure is the vertical nanowire device shown in Fig. 1.1 (d).

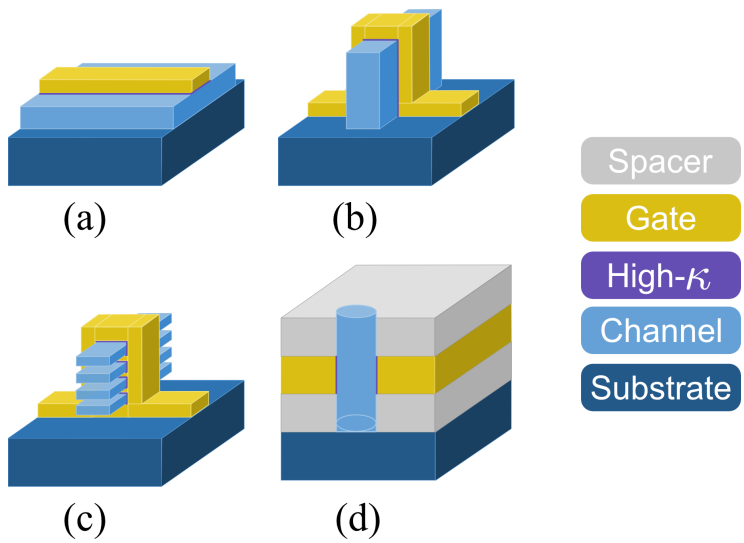


Figure 1.1: Schematic representation of different channel geometries. For a planar device, the channel is only controlled from one side (a). The electrostatic control of the channel is increased for fin-shaped channel geometries, where the channel is electrostatically controlled from three sides (b). A **GAA** device structure gives optimal electrostatic control of the channel and can be realized by horizontal nanosheets (c). A cross-section of another **GAA** device geometry is shown in (d). In this case, the channel takes the form of a vertical nanowire.

1.1 MOTIVATION TO THIS THESIS

III-V devices excel Si in high-frequency and optoelectronic applications because of their superior carrier mobility and direct band gap [6, 7]. The high carrier mobility of III-V devices also makes them interesting for emerging cryogenic electronics, where there is a need for extremely low-power electronics, to enable scaling of the number of devices and at the same time maintain the low-temperature [17]. The high mobility of III-Vs could enable low power consumption [18] and low noise [19]. The growing interest in cryogenic electronics is closely tied to advancements in the realization of superconducting Quantum Bit (**qubit**)s. The dominating superconducting **qubit** is the transmon **qubit**, which major companies like Google [20] and IBM [21] are working on. The transmon **qubit** relies on the Josephson Junction (**JJ**), which consists of a superconductor/weak-link/superconductor and acts as a non-linear element, making it possible to address the two lowest quantum levels individually. Usually, two **JJ**s are connected in a superconducting loop, known as a Superconducting Quantum Interference Device (**SQUID**), allowing for tuning of the **qubit** frequency with a magnetic flux [22]. However, this requires the introduction of dissipative currents to generate the magnetic flux, and scaling of the number of **qubit**s, while keeping a cryogenic temperature, is thus very challenging. A possible way to mitigate this problem is to construct a hybrid **JJ** with a semiconductor as the weak-link between the superconductors. This variant of superconducting **qubit** is called a gatemon **qubit**, and allows for tuning of the **qubit** frequency with a low dissipative gate bias [23, 24]. For hybrid superconductor-semiconductor devices, high mobility has shown to be critical for the formation of highly transparent interfaces [25]. III-V devices thus seem to be essential in emerging cryogenic electronics as well as in high-frequency and optoelectronic applications. However, Si-**CMOS** technology is dominating today's digital integrated circuits and will most probably not be replaced by III-Vs. One of the main reasons is that III-V devices are more expensive to fabricate and not sufficiently much better than Si in digital applications. To get the best of both technologies, III-Vs need to be monolithically integrated with Si-**CMOS** technology, which will add functionality, enable operation at higher frequencies, and reduce latency. The objective of this thesis was to investigate:

I. *The potential of III-V devices for cryogenic electronics*, see Section 1.2

II. *The integration of III-V devices in Si-**CMOS** technology*, see Section 1.3.

1.2 III-V DEVICES FOR CRYOGENIC ELECTRONICS

In this work, the focus has been on the development of high mobility indium gallium arsenide (InGaAs) **MOSFET**s, which could be used in emerging cryogenic electronics. In Paper I, we developed an optimized fabrication process for InGaAs near-surface quantum well devices, and in Paper IV we did an extensive investigation of the electron transport at cryogenic temperatures. We have also investigated different annealing processes to further improve the mobility, see Paper II, and shown that the Geometrical Magnetoresistance Effect (**gMR**) is a powerful tool for mobility extraction, see Paper III. We fabricated Josephson Field-Effect Transistor (**JoFET**)s based on our InGaAs system, by replacing our normal source and drain contacts with aluminum (Al), which turns superconducting at $T \approx 1.2$ K. The **JoFET** is the main building block of gate-tunable gatemon **qubit**s. Our devices exhibit effective gate control over the supercurrent flowing through the semiconductor. We also developed a Verilog-A-based compact model to facilitate circuit simulations and the possibility to investigate the potential of our devices in **qubit** systems, see Paper VI. In Paper V, we fabricated a demultiplexer based on a network of lateral InGaAs nanowires. Our device demonstrates on-chip routing of DC-currents, which could be used for **qubit** biasing, and this type of device thus has the potential to address the challenge of an increasing number of cables entering the cryostat associated with the scaling of the number of **qubit**s.

1.3 INTEGRATION OF III-V DEVICES IN Si-CMOS TECHNOLOGY

3D-heterointegration of high-frequency systems is considered essential for next-generation wireless communication (6G) [26]. It is however very challenging to monolithically integrate III-Vs on Si-**CMOS** due to lattice mismatch and different thermal expansion coefficients. So far, the main approaches to integrate III-Vs in Si technology have been: epitaxial growth of III-Vs on top of Si using thick buffer layers to accommodate the strain from the lattice mismatch [27], different types of selective area growth techniques on Si using dielectrics as growth masks [28–30], or transfer of III-V layers by direct wafer bonding [9, 31, 32]. Direct wafer bonding has been used to successfully 3D-integrate III-V Radio-Frequency (**RF**) devices on Si-**CMOS** circuits [9]. However, the main challenge of direct wafer bonding is that the process requires very low surface roughness, and any remaining particles at the interface between the transferred layers result in extended bonding defects and degraded device performance [33].

In Paper VII, we apply the Template-Assisted Selective Epitaxy (**TASE**) technique with silicon nitride (Si_3N_4) as a growth template, but instead of

growing III-Vs on Si, we grow single crystalline indium arsenide (InAs) nanowires directly on tungsten (W). W is usually used at the interface between Front-End-Of-Line (**FEOL**) and Back-End-Of-Line (**BEOL**) in Si-**CMOS** technology, and our process is thus enabling integration of III-V devices in Si-**CMOS** stacks. **FEOL** is the part of the **CMOS** stack containing the devices, while **BEOL** is the part containing dielectrics and metallization layers, interconnecting the devices in **FEOL**.

2

MOSFET Theory

The Metal-Oxide-Semiconductor Field-Effect Transistor (**MOSFET**), on which our digital society relies, is a three-terminal device with a source, a drain, and a gate. The basic principle of a **MOSFET** is to control the current in the channel between the source and the drain, using the gate. The size of the current can be changed by several orders of magnitude by changing the bias on the gate only by tenths of a volt. The possibility to quickly switch the current from high to low enables fast calculations in computers using a binary numerical system, represented by high and low currents. The gate is separated from the channel by a thin oxide with a high relative permittivity (high-κ), and capacitively controls the current in the channel. In Fig. 2.1 a schematic of an n-type near-surface quantum well device with raised highly doped n+ contacts is shown.

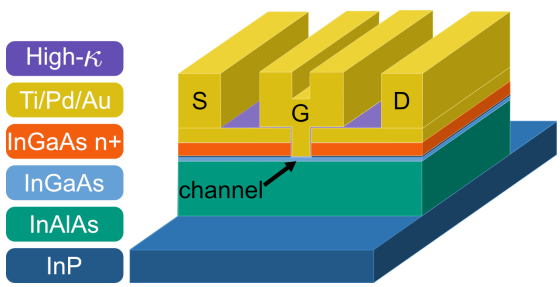


Figure 2.1: Schematic illustration of a near-surface quantum well **MOSFET** with raised n+ contacts. The electron transport between the source (S) and the drain (D) is capacitively controlled by the gate (G).

The highly doped n+ contacts will make the energy barrier between metal and semiconductor thinner, allowing for quantum tunneling and Ohmic behavior,

see Section 4.1 for details. Silicon (Si) **MOSFET**s usually have the opposite doping, in this case p-doping, in the channel where the electron transport occurs. The **MOSFET** is operated by forming an inversion layer under the gate oxide using the gate electrode. For III-V **MOSFET**s the channel layer is usually undoped and the **MOSFET** is operated by accumulation of electrons in the channel. In any case, a potential barrier for the electrons is formed between the source and the drain, see Fig. 2.5. The height of the barrier can be electrostatically controlled by the gate electrode, and hence the conductivity in the channel. If the barrier is lowered by a positive bias on the gate, the conductivity is increased, and if instead a negative bias is applied on the gate, the conductivity is decreased.

Depending on the gate bias, V_{GS}, relative to the threshold voltage, V_T, the **MOSFET** can be operated in three different modes. If $V_{GS} < V_T$, the device is in the subthreshold regime, and the current increases exponentially with V_{GS}. When instead $V_{GS} > V_T$ the device is in the on-state, which can be divided into two modes of operation, namely the linear region and the saturation region. These two modes of operations are highlighted in Fig. 2.2 (a), showing the output characteristics of a near-surface quantum well **MOSFET**. Another way to visualize the **MOSFET** performance is by its transfer characteristics, where the drain current, I_{DS}, is measured as a function of V_{GS}, for a fixed value of the drain bias, V_{DS}, see Fig. 2.2 (b), where the subthreshold region also is indicated. At high V_{GS} the channel resistance is negligible and the current is limited by contact resistances.

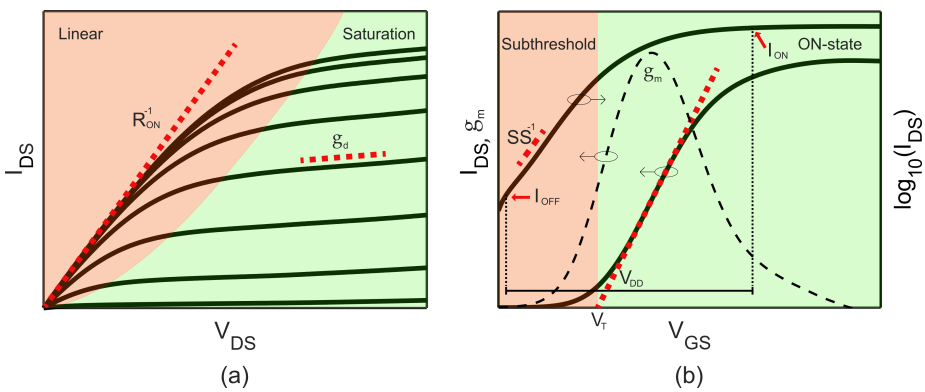


Figure 2.2: Typical I-V characteristics of near-surface quantum well **MOSFET**s fabricated in this thesis work. The different modes of operation, as well as important metrics, are indicated in the figures. The output characteristics are presented in (a), while (b) shows the transfer characteristics.

2.1 PERFORMANCE METRICS

In this section, standard figures of merit for transistors for digital applications are introduced and discussed. Specifically their definition, influence on device performance, and possible ways to improve them. All metrics discussed in this section are indicated in Fig. 2.2. While the focus of this thesis is not on transistors for digital applications, the purpose of this section is to familiarize the reader with fundamental **MOSFET** operation. This knowledge is crucial for comprehending the following chapters and the accompanying papers, with particular emphasis on parameters such as Subthreshold Swing (**SS**), on-resistance (R_{ON}), and threshold voltage (V_T), which all play a significant role throughout the rest of this thesis.

In industry, the off-current, I_{OFF}, is typically defined as I_{DS} at $V_{GS} = 0$ and $V_{DS} = V_{DD}$, where V_{DD} is the drive voltage. The on-current, I_{ON}, is defined as I_{DS} for the bias point, $V_{DS} = V_{DD}$ and $V_{GS} = V_{DD}$. In digital circuits $V_{GS} = V_{DD}$ and $V_{GS} = 0$ represent "1" and "0" in the binary number system used to perform all calculations. This means that every time a binary condition changes, the voltage is switched from V_{DD} to 0 or vice versa. The time to perform a switching event is limited by charging and discharging of capacitances and depends thus strongly on I_{ON}. I_{ON} is determined by the product of injection velocity and carrier concentration [34]. One way to increase I_{ON}, while keeping the drive voltage constant, is thus to use a channel material facilitating higher injection velocity or higher Density Of States (**DOS**). III-V devices can reach several times higher injection velocities compared to silicon-based devices, but is limited by its lower **DOS** [35].

It is of course also important to keep a small I_{OFF} to minimize the power consumption. For short gate lengths I_{OFF} can be limited by direct tunneling from source to drain, other limitations could be gate leakage current or band to band tunneling.

Another important metric in the off-state is **SS**, which is a measure of the current modulation by the gate. **SS** is defined as the inverse of the slope in the subthreshold region, $(\frac{\partial \log I_{DS}}{\partial V_{GS}})^{-1}$. To improve **SS**, a Gate-All-Around (**GAA**) approach can be used, where the channel is capacitively coupled to the gate from several sides. High-κ materials as gate dielectric, and annealing processes to minimize defects in the oxide can further improve **SS**. For transistors where the drain current is limited by thermionic emission over a barrier between source and drain, the theoretical limit is set by the thermal voltage, $\frac{k_B T}{q}$, which gives **SS** ≈ 60 mV/decade at room temperature.

The metric that defines the border between on- and off-state is the threshold voltage, V_T. V_T can be extracted from a linear extrapolation of I_{DS}, at the point of maximum transconductance $g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$. The point where the linear

extrapolation intersects the V_{GS}-axis, corresponds to V_T. However, this is only one of several different ways to extract V_T, which is not uniquely defined. n-type **MOSFET**s, which have a $V_T < 0$ is called to be depletion-mode or normally-on **MOSFET**s, while a $V_T > 0$ is characteristic for enhancement-mode or normally-off **MOSFET**s. The position of V_T is thus very important because it will determine the off-state power consumption. **SS** together with V_T determines the ratio, $\frac{I_{ON}}{I_{OFF}}$, for a specific V_{DD}.

The transconductance is **SS**'s counterpart in the on-state. **SS** describes how efficiently the gate controls the drain current in the subthreshold region, while g_m is a measure of how much the drain current changes with gate bias in the on-state. The transconductance is especially important for high-frequency applications, since it is related to the transistor's gain and thus its amplifying capabilities. Other important metrics in the on-state are the on-resistance, R_{ON}, and the output conductance g_d. The on-resistance is extracted from the linear region, where it is the sum of channel resistance, access resistance, and contact resistance, $R_{ON} = 2R_C + 2R_{ACC} + R_{CH}$, and should be as small as possible in order to give high I_{ON}. The output conductance should also be as small as possible in order for the **MOSFET** to act as a gate-controlled current source. A high g_d means that the current will depend on V_{DS} even in the saturation region. This is a common issue for short-channel devices and is referred to as Drain-Induced Barrier Lowering (**DIBL**). The **DIBL** effect arises because the drain bias will affect the height of the barrier in the channel region, meaning that when V_{DS} is increased the barrier between source and drain is lowered and the current is increased. The **DIBL** effect will also shift V_T in the negative direction when V_{DS} is increased.

2.2 GATE CAPACITANCE AND OXIDE DEFECTS

In order to understand the transport mechanism in **MOSFET**s, the electrostatics of the system need to be considered. The height of the barrier between the source and the drain is what determines the current through the device, and is set by the capacitive coupling between the three electrodes and the channel, and by the carrier concentration in the channel. In a well-behaving **MOSFET** the gate capacitance is however much larger than the source and drain capacitances, meaning that the height of the barrier only is set by the gate to channel coupling. The gate capacitance can be modeled as three capacitances in series, see Fig. 2.3.

The total gate capacitance is the series combination of these three capacitances,

$$C_G = \left(\frac{1}{C_{OX}} + \frac{1}{C_C} + \frac{1}{C_Q} \right)^{-1}. \tag{2.1}$$

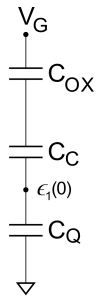


Figure 2.3: Circuit diagram used to model the gate capacitance C_G. C_G is the series combination of C_{OX}, C_C, and C_Q. $\epsilon_1(0)$ represents the potential at the minimum of the first subband at the top of the barrier between the source and the drain.

The oxide capacitance, C_{OX}, is the geometrical contribution, which can be seen as a parallel plate capacitor between the gate electrode and the channel, separated by the thickness of the oxide,

$$C_{OX} = \frac{\kappa\epsilon_0}{t_{OX}}, \tag{2.2}$$

where κ is the relative permittivity of the gate oxide, ϵ_0 is the vacuum permittivity, and t_{OX} is the thickness of the oxide. A high κ thus means that C_{OX} is large, and the gate-to-channel coupling is good. If a positive bias is applied on the gate electrode and an accumulation of electrons occurs in the channel, the repulsive interactions between the electrons will lead to an upward shift of the energy bands [36,37]. This effect is described by the charge centroid capacitance,

$$C_C = \frac{\epsilon_S\epsilon_0}{0.36t_W}, \tag{2.3}$$

where ϵ_S is the relative permittivity of the semiconductor channel and t_W is the thickness of the channel layer. The quantum capacitance, C_Q, for a fully degenerate quantum well with only the first subband occupied can be expressed as

$$C_Q = q^2 D_{2D}, \tag{2.4}$$

where q is the elementary charge and D_{2D} is the 2D density of states [38]. From Eq. (2.4), it is evident that C_Q increases with **DOS**, which means that for a material with high **DOS** and thick oxide, $C_Q >> C_{OX}$, the third term in Eq. (2.1), i.e. $\frac{1}{C_Q}$, can be neglected. In this case, the device is said to be in the MOS limit, and the electrostatic control of the channel by the gate is mainly determined by C_{OX}. The coupling between the gate and the channel

can thus be improved by scaling the gate dielectric. This is often the case for Si **MOSFET**s but rarely for III-V **MOSFET**s due to their much lower **DOS**. In the other limit where $C_Q << C_{OX}$, the device is operating in the Quantum Capacitance Limit (**QCL**), and the first term in Eq. (2.1), i.e. $\frac{1}{C_{OX}}$, can be neglected. In this regime, the gate is directly controlling the potential at the top of the barrier according to Eq. (2.4). Further scaling of the oxide thickness will thus not increase the charge in the channel for a device operating in **QCL**. However, it has been shown that further scaling of the gate oxide will improve the power delay product, that is, the energy dissipated in a Complementary Metal Oxide Semiconductor (**CMOS**) circuit per switching operation [39].

The **MOSFET** performance depends strongly on the gate-to-channel coupling, which will be influenced by defects in the oxide, and at the high-κ/III-V interface. Since an interface between an amorphous dielectric and a crystalline semiconductor is formed, it is not surprising that a lot of defects arise at the interface [40]. These defects will be detrimental, since the charging and discharging of defect-induced trap states will reduce the movement of the Fermi level, resulting in increased **SS** [41]. The trap energies related to the increased **SS** are primarily situated in the band gap, while trap energies situated in the conduction band will influence the on-state performance. Charging and discharging of defect-induced trap states can be modeled as an interface-trap capacitance, C_{IT}, parallel to the semiconductor capacitance, i.e. the series combination of C_Q and C_C, see Fig. 2.4.

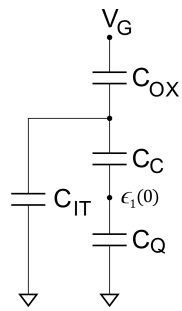


Figure 2.4: Circuit to model C_G, including the effect from interface traps modeled by the parallel capacitance C_{IT}.

The interface-trap capacitance will depend on the interface-trap density according to

$$C_{IT} = q^2 D_{IT}. \tag{2.5}$$

It is worth noting that the interface-trap density, D_{IT}, will in general be energy dependent, and different parts of the D_{IT} distribution will participate at different gate biases.

In addition to the degradation of the device performance by introducing the capacitance, C_{IT}, the defects will also increase the scattering of electrons in the channel, degrading the device performance in terms of carrier mobility.

2.3 ELECTRON TRANSPORT AND MOBILITY

The main focus of this thesis has been the study of electron transport in InGaAs **MOSFET**s at cryogenic temperatures, to explore its potential in future cryogenic electronics. The following sections will introduce the basic concepts of electron transport in **MOSFET**s, which is the fundament upon which this thesis is built.

2.3.1 DRIFT AND DIFFUSION

The electrons in a nondegenerate semiconductor material, with no applied electric field, will move in a random pattern. The random nature of the motion will eventually even out any concentration gradients. Thus, there will be a net flow of electrons from high to low concentration, called the diffusion current. The diffusion current density is given by

$$J_{\text{diff}} = qD\frac{\partial n}{\partial x}, \tag{2.6}$$

where $D = \mu k_B T/q$ is the diffusivity, q is the elementary charge, n is the electron carrier concentration, μ is the mobility, k_B is Boltzmann's constant, T is the temperature, and x is the dimension in which current flows.

If an applied electric field is introduced the electrons will move against the field lines. The current density is described as

$$J_{\text{drift}} = qn\mu E_x, \tag{2.7}$$

where E_x is the magnitude of the electric field in the x-direction. The mobility is a measure of how easily the electrons move in the electric field and depends on the effective mass in the material and the concentration of scattering centers. The total current density is the sum of J_{diff} and J_{drift}, which can be described in terms of the gradient of the quasi-Fermi level [42],

$$J = J_{\text{diff}} + J_{\text{drift}} = n\mu\frac{\partial E_F}{\partial x}. \tag{2.8}$$

For short-channel devices, the potential difference, ΔV, between the source and the drain gives rise to very high electric fields even at low applied voltages, $E_x = \frac{-\Delta V}{L_G}$. The electron velocity, $v = \mu E_x$, is proportional to the electric field, but will due to scattering saturate at a certain velocity, v_{SAT}, called the saturation velocity [43].

2.3.2 BALLISTIC TRANSPORT

In this section, the discussion on electron transport in 2-dimensional short-channel devices with high electron mobility will closely follow Mark Lundstrom's textbook [38]. Under such circumstances, electrons can travel from the source to the drain without scattering, and this is called ballistic transport. The mean distance a charge carrier travels between scattering events is called the mean-free path, λ, and if $L_G < \lambda$, ballistic transport could occur.

The current between the source and the drain is controlled by the gate bias, which varies the height of the barrier between the source and the drain, see Fig. 2.5.

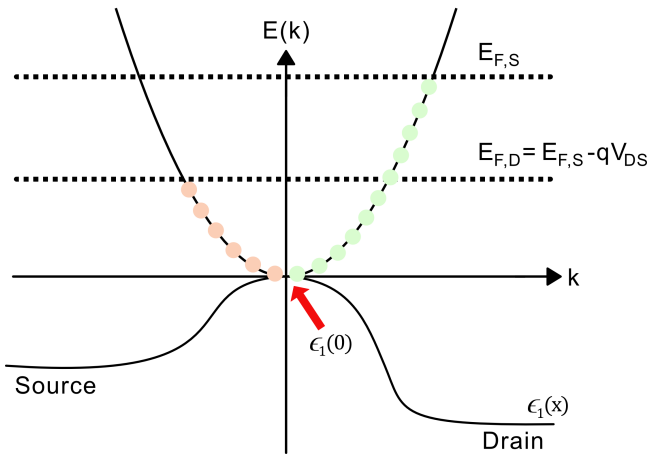


Figure 2.5: Schematic of the lowest conduction subband in a fully ballistic 2-dimensional **MOSFET** device, as a function of position, $\epsilon_1(x)$. The minimum of the first subband at the top of the barrier between the source and the drain is located at $x = 0$. The height of this barrier can be electrostatically controlled by the gate. An inset of energy versus momentum for parabolic bands is also included. The positive k-states are occupied to the source Fermi level, while the negative k-states are occupied to the drain Fermi level.

Fig. 2.5, shows the lowest conduction subband energy versus position, $\epsilon_1(x)$, and in the following, it is assumed that only the lowest subband is occupied. An inset of energy versus momentum, k, for parabolic bands is also included. The positive k-states are populated by injection from the source, and occupy all states up to the source Fermi level, $E_{F,S}$. In the same way, the negative k-states are populated by injection from the drain, and occupy all states up to the drain Fermi level, $E_{F,D} = E_{F,S} - qV_{DS}$. When V_{DS} is increased, the population of negative k-states is decreased, while the population of

positive k-states is increased, leading to a net flow of electrons from the source to the drain.

The concentration of electrons injected from the source and the drain can be calculated from the density of states and the probability that a state is occupied,

$$n_s{}^{+}\left(E_{\mathrm{F,S}}\right) = \frac{1}{2}\int_0^{\infty} f_0\left(E, E_{\mathrm{F,S}}\right) D(E)\, dE, \tag{2.9}$$

$$n_s{}^{-}\left(E_{\mathrm{F,D}}\right) = \frac{1}{2}\int_0^{\infty} f_0\left(E, E_{\mathrm{F,D}}\right) D(E)\, dE, \tag{2.10}$$

where n_s is the surface carrier concentration, f_0 is the Fermi function and D is the density of states. The factor $\frac{1}{2}$, comes from the fact that only one half of the k-states have positive velocity and the other half has negative velocity. For 2-dimensional transport, Eq. (2.9) and Eq. (2.10) can be written in terms of the 2-dimensional effective density of states, N_{2D}, and the Fermi-Dirac integral of order 0, F_0,

$$n_s{}^{+} = \frac{N_{\mathrm{2D}}}{2} F_0\left(\eta_F\right), \tag{2.11}$$

$$n_s{}^{-} = \frac{N_{\mathrm{2D}}}{2} F_0\left(\eta_F - U_D\right). \tag{2.12}$$

Here, $\eta_F = \frac{E_{F,S} - \epsilon_1(0)}{k_{\mathrm{B}}T}$, $\epsilon_1(0)$ is the minimum of the first subband at the top of the barrier, k_{B} is Boltzmann's constant, T is the temperature, and $U_D = \frac{qV_{\mathrm{DS}}}{k_{\mathrm{B}}T}$. The effective density of states for 2-dimensional transport is

$$N_{\mathrm{2D}} = \frac{m^* k_{\mathrm{B}} T}{\pi \hbar^2}, \tag{2.13}$$

where m^* is the effective mass, and $\hbar$ is the reduced Planck's constant. The Fermi-Dirac integral of order j is defined as

$$F_j\left(\eta_F\right) \equiv \frac{1}{\Gamma\left(j+1\right)} \int_0^{\infty} \frac{\xi^j}{1 + e^{(\xi - \eta_F)}}\, d\xi, \tag{2.14}$$

where $\xi = \frac{E - \epsilon_1(0)}{k_{\mathrm{B}}T}$ and the Γ-function is defined as

$$\Gamma\left(z\right) \equiv \int_0^{\infty} t^{(z-1)} e^{-t}\, dt. \tag{2.15}$$

The total carrier density at the top of the barrier is the sum of $n_s{}^{+}$ and $n_s{}^{-}$, which is determined by the gate bias and gate capacitance,

$$n_s{}^{+} + n_s{}^{-} = \frac{C_{\mathrm{G}} V_{\mathrm{OV}}}{-q}, \tag{2.16}$$

where $V_{OV} = V_{GS} - V_T$ is the overdrive voltage. The capacitive effects from the source and the drain are neglected, since these are much smaller than C_G for a well-behaving **MOSFET**.

Expressions for the drain current of ballistic 2-dimensional **MOSFET**s, will be derived by investigating two different operating conditions. First, we assume that the electron gas is nondegenerate, which means that the carrier concentration is low. This could for instance be the case when the III-V **MOSFET** is operated close to V_T. At these conditions $F_j(\eta_F) \rightarrow e^{\eta_F}$, for any order, j, of the Fermi-Dirac integral. Eq. (2.11) and Eq. (2.12), can then be written as

$$n_s{}^+ = \frac{N_{2D}}{2} e^{\eta_F}, \tag{2.17}$$

$$n_s{}^- = \frac{N_{2D}}{2} e^{(\eta_F - U_D)}. \tag{2.18}$$

The current density is calculated by multiplying the charge density by the elementary charge, q, and the thermal injection velocity, v_T. The current is subsequently obtained by multiplying with the width of the device, W, resulting in

$$I^+ = Wq \frac{N_{2D}}{2} e^{\eta_F} v_T, \tag{2.19}$$

$$I^- = Wq \frac{N_{2D}}{2} e^{(\eta_F - U_D)} v_T, \tag{2.20}$$

where the thermal injection velocity is defined as

$$v_T = \sqrt{\frac{2k_B T}{\pi m^*}}. \tag{2.21}$$

The total current is then the difference between the positive and negative currents, which can be expressed as

$$I_{DS} = WC_G v_T V_{OV} \frac{1 - e^{-qV_{DS}/k_B T}}{1 + e^{-qV_{DS}/k_B T}}. \tag{2.22}$$

This expression for I_{DS} is only valid under nondegenerate conditions and therefore a poor assumption above V_T for III-V **MOSFET**s. At cryogenic temperatures and degenerate conditions, $\eta_F \gg 1$, and $n_s{}^+$ and $n_s{}^-$ will be described by step functions, Θ,

$$n_s{}^+ = \frac{m^*}{2\pi\hbar^2} \left[E_{F,S} - \epsilon_1(0) \right] \Theta \left(E_{F,S} - \epsilon_1(0) \right), \tag{2.23}$$

$$n_s{}^- = \frac{m^*}{2\pi\hbar^2} \left[E_{F,S} - qV_{DS} - \epsilon_1(0) \right] \Theta \left(E_{F,S} - qV_{DS} - \epsilon_1(0) \right). \tag{2.24}$$

If $E_{F,S} < \epsilon_1(0)$ no positive k-states will be populated, and in order for negative k-states to be populated $E_{F,D} = E_{F,S} - qV_{\mathrm{DS}} > \epsilon_1(0)$. Similar to the nondegenerate case, expressions for I^+ and I^- can be derived by multiplying the charge density with the elementary charge, the velocity of the charge carriers, and the width of the device. The velocity is described as

$$v^+ = \frac{4}{3\pi}\sqrt{\frac{2\left[E_{F,S} - \epsilon_1(0)\right]\Theta\left(E_{F,S} - \epsilon_1(0)\right)}{m^*}}, \tag{2.25}$$

$$v^- = \frac{4}{3\pi}\sqrt{\frac{2\left[E_{F,S} - qV_{\mathrm{DS}} - \epsilon_1(0)\right]\Theta\left(E_{F,S} - qV_{\mathrm{DS}} - \epsilon_1(0)\right)}{m^*}}, \tag{2.26}$$

and the currents become

$$I^+ = qW\frac{\left[2m^*\left[E_{F,S} - \epsilon_1(0)\right]\Theta\left(E_{F,S} - \epsilon_1(0)\right)\right]^{\frac{3}{2}}}{3m^*\pi^2\hbar^2}, \tag{2.27}$$

$$I^- = qW\frac{\left[2m^*\left[E_{F,S} - qV_{\mathrm{DS}} - \epsilon_1(0)\right]\Theta\left(E_{F,S} - qV_{\mathrm{DS}} - \epsilon_1(0)\right)\right]^{\frac{3}{2}}}{3m^*\pi^2\hbar^2}. \tag{2.28}$$

At low V_{DS}, the following relationship between I^+ and I^- is valid,

$$I^- = I^+ - \left(\frac{\partial I^+}{\partial E_{F,S}}\right)qV_{\mathrm{DS}}, \tag{2.29}$$

and I_{DS} becomes

$$I_{\mathrm{DS}} = I^+ - I^- = \left(\frac{\partial I^+}{\partial E_{F,S}}\right)qV_{\mathrm{DS}}. \tag{2.30}$$

By evaluating the derivative in Eq. (2.30) using Eq. (2.27) we obtain

$$I_{\mathrm{DS}} = M\frac{2q^2}{h}V_{\mathrm{DS}}, \tag{2.31}$$

where h is Planck's constant. The factor $M = \frac{Wk_{F,S}}{\pi}$ corresponds to the number of occupied transverse k-states, where $k_{F,S}$ is the source Fermi wave vector. A 2-dimensional ballistic **MOSFET** at cryogenic temperatures therefore should show a quantized conductance above V_{T},

$$G = M\frac{2q^2}{h}, \tag{2.32}$$

where each transverse mode contributes with $\frac{2q^2}{h}$ S. In practice, it is impossible to distinguish individual steps in the conductance due to the closely spaced energy modes. However, by reducing the device width, W, the energy gaps

between the modes increase, and in the case of a nanowire, it is possible to measure distinct steps in the conductance [44].

Now we have expressions for I_{DS} under both nondegenerate and degenerate operating conditions. This will mark the upper performance limit for high mobility short-channel quantum well **MOSFET**s. In the next section, the effect of scattering will be considered, in order to describe I_{DS} for more realistic devices.

2.3.3 QUASI-BALLISTIC TRANSPORT

In real devices, scattering events will occur, resulting in a performance below the ballistic limit [45]. In the ballistic case, all electrons with positive k-sates are populated by the source contact and in equilibrium with the source Fermi level. This simple picture does however not hold anymore when scattering is introduced. Now electrons injected from the source can scatter and get negative momentum. If the scattering event occurs close to the source, there is a high probability that the electron never reaches the drain. To explain this we assume that an electron is injected from the source, and after traveling only a short distance it scatters and travels back towards the source contact. If the distance to the source contact is much smaller than the mean free path, the probability is low that the electron will scatter again before reaching the source contact. The electron injected from the source will therefore not contribute to the positive current from source to drain, but instead contribute to the negative current from drain to source. Similarly, an electron injected from the source which scatters close to the drain, will travel back towards the source, but if the distance is longer than the mean free path it is probable that it will scatter again and travel towards the drain again. I_{DS} is thus mostly influenced by scattering close to the source contact, which has been confirmed by simulations [46].

One very interesting and quite contradicting observation is that a long-channel device fabricated already in 1987 [47], showed performance close to the ballistic limit [48]. However, the expected improved ballisticity for devices with L_G less than the mean free path has been absent. A possible explanation for this is provided by Kenji Natori [49]. In the paper, they show that the ballistic limit should be reached for short-channel devices if the drain electrode is assumed to accept all incoming electrons, but in a real device with a highly doped drain contact, elastic scattering will occur inside the drain. A significant amount of the electrons reaching the drain will thus be scattered back into the channel, without losing any energy. For a short-channel device, the backscattered electrons will with high probability reach the source contact without any scattering event. On the contrary, for a long-channel device, electrons that have been backscattered at the drain will with a

high probability scatter again in the channel, turning back towards the drain. In addition, if inelastic scattering is dominant in the channel, the probability that the backscattered electrons will reach the energy level of the source is very small. In order for the drain to accept the electrons, the size needs to be large enough for frequent scattering inside the drain, and inelastic scattering needs to be predominant over elastic scattering for energy relaxation to occur. Even for a highly doped drain contact, long-channel devices can reach the ballistic limit, if inelastic scattering is predominant over elastic scattering in the channel.

The transport mechanism calculations become quite complex when introducing scattering, but a simple way to overcome this is to introduce the transmission coefficient, Γ. The transmission coefficient represents the probability that an electron injected from one of the contacts will reach the other contact, and if scattering occurs $\Gamma < 1$. The mean free path, λ, and the effective gate length, $L_{\mathrm{G,EFF}}$, are used to determine Γ [50],

$$\Gamma = \frac{\lambda}{\lambda + L_{\mathrm{G,EFF}}}. \tag{2.33}$$

The effective gate length corresponds to the low-field part of the channel, close to the source. At low V_{DS}, $L_{\mathrm{G,EFF}} = L_{\mathrm{G}}$, but at high V_{DS}, $L_{\mathrm{G,EFF}} < L_{\mathrm{G}}$. Electrons scattering in the high-field region of the channel, close to the drain, will be very unlikely to return to the source [51].

The ballistic currents for nondegenerate and degenerate carrier statistics derived in the previous section, see Eq. (2.19)-(2.20), and Eq. (2.27)-(2.28), will hereafter be denoted I_B^+ and I_B^-. The total drain current, I_{DS}, in the quasi-ballistic case can be expressed in terms of these ballistic currents. The drain current will be the sum of the electrons flowing into the drain contact. This sum has three contributions, the electrons injected from the source that reach the drain (ΓI_B^+), plus the electrons injected from the drain that are scattered back to the drain ($(1-\Gamma)I_B^-$), minus the electrons injected from the drain (I_B^-),

$$I_{\mathrm{DS}} = \Gamma I_B^+ + (1-\Gamma)I_B^- - I_B^-. \tag{2.34}$$

Eq. (2.34) can be simplified as

$$I_{\mathrm{DS}} = \Gamma I_B^+ + I_B^- - \Gamma I_B^- - I_B^- = \Gamma\left(I_B^+ - I_B^-\right) = \Gamma I_B, \tag{2.35}$$

where I_B is the ballistic drain current. This means that the ballistic current simply is reduced by the transmission coefficient.

2.3.4 TRANSPORT AT CRYOGENIC TEMPERATURES

During this thesis work, **MOSFET** characterization at cryogenic temperatures has been one of the main investigations. In this section, some effects on

electron transport which are clearly visible at cryogenic temperatures but may be hidden at room temperature due to thermal broadening, will be discussed. These effects are important to consider when studying **MOSFET**s at cryogenic temperatures.

Band tails are localized electronic states close to the valence band edge and the conduction band edge, but inside the band gap [52]. They arise due to different types of disorders in the crystal structure and show an exponential distribution defined by the Urbach energy, E_U [53]. The exponential decrease in density of band tail states below the conduction band can be expressed as

$$D_T(E) \propto e^{(E-E_C)/E_U}, \tag{2.36}$$

where E_C is the conduction band energy. The band tail states will broaden the band edge, see Fig. 2.6, where the 2D density of states is plotted with and without including the effect from band tail states. At low temperatures, and with a Fermi level close to the conduction band edge, these band tail states will have a detrimental effect on the subthreshold swing. This is explained by the fact that electrons will transfer through these states, increasing the drain current and thus increasing **SS**.

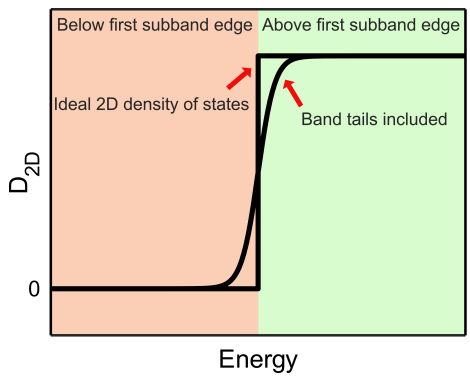


Figure 2.6: The 2D density of states for parabolic bands as a function of energy. Ideally, there are no states below the band edge of the first subband, but if the effect from band tails is included, the band edge is broadened, giving states even below the band edge.

The subthreshold swing for a **MOSFET** can be expressed as

$$\mathbf{SS} = \ln(10)\frac{k_B T}{q}\left(1 + \frac{C_Q + C_{IT}}{C_{OX}}\right), \tag{2.37}$$

where k_B is Boltzmann's constant, T is the temperature, C_Q is the quantum capacitance, C_{IT} is the interface-trap capacitance, and C_{OX} is the oxide capacitance. According to Eq. (2.37), the subthreshold swing will approach zero,

when the temperature goes to zero. Measurements at cryogenic temperatures show however consequently higher values than expected from Eq. (2.37) [54–57]. This can be explained by the band tail states, and is easily included by introducing a critical temperature, $T_0 = E_U/k_B$, at which **SS** saturates,

$$\mathbf{SS}_{SAT} = \ln(10)\frac{k_B T_0}{q}\left(1 + \frac{C_Q + C_{IT}}{C_{OX}}\right). \tag{2.38}$$

In Fig. 2.7, a comparison between **SS** with and without including the effect of band tail states is shown.

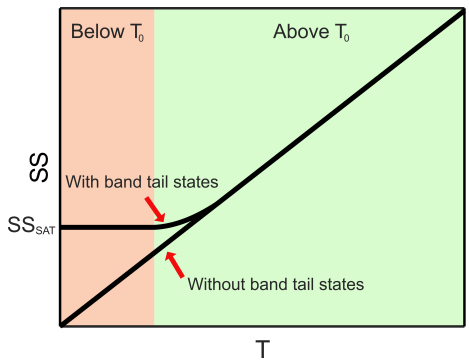


Figure 2.7: Ideally **SS** will approach zero when the temperature is approaching $T = 0$, but due to the band tail states, **SS** will saturate at $\mathbf{SS}_{SAT}$ for temperatures below a critical temperature T_0.

In addition to broadening, the fact that the band edges will be rough due to charged defects at the semiconductor/high-κ interface [58], will affect the electron transport at cryogenic temperatures. For 1D devices, the rough band edge can be seen as multiple quantum dots and will give rise to sequential tunneling and resonances. This will show up as resonance current peaks in **MOSFET** measurements at low drain biases, when the electron transport is close to the band edge.

An interesting feature which is more prominent at cryogenic temperatures, is the fact that the carrier mobility is dependent on the carrier density, see Paper III and Paper IV. At low gate bias and low carrier densities, the mobility is limited by remote impurity scattering, but also by the roughness of the conduction band edge. When the gate bias is increased, both these scattering mechanisms are reduced. The increased carrier concentration leads to more efficient screening by the charge carriers, and the higher kinetic energy of the charge carriers results in less impact from the roughness of the conduction band edge. At an even higher gate bias, the electrons will be confined too close to the high-κ/III-V interface, and scattering from defects at the interface

as well as the influence from interface roughness will increase, decreasing the mobility. The peak mobility is higher at low temperatures compared to room temperature, due to reduced phonon scattering. At low carrier concentration, on the other hand, the mobility is higher at room temperature, which is explained by the fact that electrons with higher kinetic energy will be less affected by Coulomb scattering. The carrier concentration dependence is thus less visible at higher temperatures, see Fig. 2.8, where the carrier density dependence of the mobility is compared by measurements on the same device at room temperature and 9.4 K.

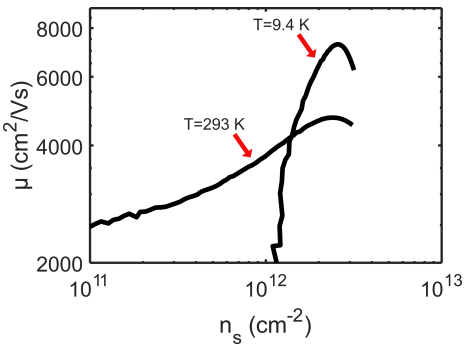


Figure 2.8: Carrier mobility extracted from a near-surface quantum well device at $T = 9.4$ K and $T = 293$ K, respectively. The carrier density dependence is less visible at $T = 293$ K, due to less impact from Coulomb scattering and increased impact from phonon scattering.

At cryogenic temperatures, the mobility depends strongly on the carrier concentration and hence varies along the channel between source and drain. If $V_{DS} > 0$ the Fermi level is decreasing towards the drain side, meaning that the carrier concentration is decreasing and thus also the mobility. The mobility reduction along the channel leads to a reduced current and hence a lower **SS**. When the effect of carrier-dependent mobility is prominent, it is potentially possible to get **SS** lower than what is set by the thermal voltage, $\mathbf{SS} = \ln(10)\frac{k_B T}{q}$ [59]. This can be explained by the fact that the current is proportional to the carrier concentration times the mobility. The carrier concentration decreases exponentially with V_{GS} at a maximum rate of $\ln(10)\frac{k_B T}{q}$, which for constant mobility gives 60 mV/decade at room temperature. But if the mobility is decreasing with the carrier concentration, the product of carrier concentration times mobility will decrease with a rate faster than $\ln(10)\frac{k_B T}{q}$, meaning that $\mathbf{SS} < \ln(10)\frac{k_B T}{q}$.

2.4 SUMMARY

Achieving high-performance **MOSFET**s necessitates excellent material quality. The semiconductor quality within the channel must be exceptional to minimize scattering and facilitate high mobility of the charge carriers. The interfaces between different materials play a crucial role in determining the device's overall performance. A high quality of the semiconductor/high-κ interface is required to obtain good electrostatic control of the channel and minimize scattering of the charge carriers. Moreover, optimizing the interface between the semiconductor and metal contact is crucial for minimizing the contact resistance. At cryogenic temperatures, the material quality becomes even more important. Defects in the semiconductor's crystal structure introduce band tail states, which are detrimental for **SS**, and a rough conduction band edge, due to charged defects at the semiconductor/high-κ interface will decrease the mobility. In cryogenic applications, it is particularly crucial to utilize a low operating bias and, consequently, achieve low power consumption and low power dissipation, otherwise, the low temperature can not be maintained. In addition to high-quality materials and interfaces, a channel geometry that improves the electrostatic control of the channel is important in order to improve **SS** and minimize short-channel effects such as **DIBL**. The material choice is of course essential, where a high mobility channel material and a high-κ gate oxide are beneficial for the device performance.

3

Fabrication

Fabrication of devices on the nm-scale is complex and requires high material quality. In this regime, the surface-to-volume ratio is large, meaning that the surface quality is essential. Interfaces, crystal growth, and the potential to integrate different materials are thus of high interest. A rough semiconductor surface, or poor interface between the gate oxide (high-κ) and the semiconductor channel, has detrimental effects on the device's performance. In addition, different parts of the devices are defined in separate steps, hence requiring extremely high spatial precision. In order to fabricate these types of devices in a research lab, process modules are developed and new process flows are realized by integrating these process modules in a carefully considered manner. For small features or high alignment accuracy Electron-Beam Lithography (**EBL**) is the choice of use, while process steps with lower requirements can be performed using less-time consuming Ultraviolet Lithography (**UVL**).

In the work presented in this thesis, mainly three different process flows have been used, and in the next sections, the purpose of the main process steps will be described. More detailed step-by-step procedures can be found in Appendix A, Appendix B, and Appendix C.

3.1 NEAR-SURFACE QUANTUM WELL DEVICES

Variations of this type of device are used in Paper I, Paper II, Paper III, Paper IV, and Paper VI. A schematic of the process flow is shown in Fig. 3.1.

3.1.1 GATE LENGTH DEFINITION

The starting wafer consists of epitaxial layers of III-Vs on top of a Semi-Insulating (**S.I.**) indium phosphide (InP) substrate, see Fig. 3.1. In order to be able to electrostatically control the conductivity of the undoped indium gallium arsenide (InGaAs) channel layer, the highly doped n+ InGaAs and InP above the channel need to be removed, or in other words, the gate length needs to be defined. The structure of certain polymers changes upon electron-beam exposure, which alters their solubility in certain solvents. This is utilized by spin-coating the sample with an electron-beam sensitive polymer and then writing the desired pattern in the polymer using an electron beam. This way of patterning is called lithography. The patterned polymer is then used as an etch mask for pattern transfer into the wafer, see Fig. 3.1. The width of the line defines the gate length.

3.1.2 MESA DEFINITION

During the mesa definition, the devices undergo electrical isolation from each other through wet etching down to the **S.I.** InP substrate. The etch mask is established using **UVL** with a Maskless Aligner (**MLA**) rather than **EBL** due to the lower resolution demands.

3.1.3 SOURCE-DRAIN METALLIZATION

To achieve low contact resistance, the metal should be deposited directly onto the n+ InGaAs, and any native oxide on the semiconductor needs to be removed in hydrochloric acid (HCl) just before deposition. Precise alignment of the source-drain contacts with respect to the highly doped n+ InGaAs is essential for minimizing the access resistance. The contacts should be placed as close to the n+ edge as possible, to minimize the distance of electron transport in the n+ layer. Therefore **EBL** is used to define the contacts. The metal is then deposited using e-beam evaporation. After evaporation, a process called lift-off is performed. The sample is put in acetone and the polymer used during **EBL** is dissolved, which makes the metal deposited on the polymer to be lifted off the sample, while the metal deposited in the polymer openings stays on the sample. In a subsequent lithography step, the measurement pads are defined. The measurement pads are designed to be large to accommodate wire bonding, and **EBL** is considerably more time-consuming than **UVL**. Therefore the measurement pads are defined by **UVL** using a **MLA**, followed by evaporation and lift-off.

3.1.4 PASSIVATION AND GATE OXIDE DEPOSITION

One of the most important device characteristics of Metal-Oxide-Semiconductor Field-Effect Transistor (**MOSFET**)s for digital applications is the Subthreshold Swing (**SS**), which determines how fast the transistor can switch from on- to off-state. The quality of the high-κ/III-V interface is crucial for fast switching, and defects in the oxide and interface states will have detrimental effects, see Section 2.2. In order to get as pristine a surface as possible before the gate oxide is deposited, the sample is cleaned and oxidized in an ozone atmosphere. Subsequently, the sample is immersed in an ammonium sulfide solution ($(NH_4)_2S$:H_2O), wherein the oxide is eliminated, and the surface undergoes passivation with sulfur to prevent re-oxidation [60]. The sample is then put into the Atomic Layer Deposition (**ALD**) chamber, where pre-pulsing of Trimethylaluminum (**TMAl**) is performed in order to restore surface arsenic (As) atoms to bulk-like bonding and reduce the interface-trap density (D_{IT}) [61]. This is followed by the deposition of a bilayer of aluminum oxide (Al_2O_3) and hafnium dioxide (HfO_2), which gives a high-quality interface in combination with a low Equivalent Oxide Thickness (**EOT**).

3.1.5 GATE METALLIZATION

The gate electrode is defined by **UVL** followed by e-beam evaporation, and lift-off in acetone.

3.1.6 ANNEALING

To improve the device performance in terms of **SS** and carrier mobility, the sample is annealed in forming gas. Forming gas is a mixture of hydrogen (H_2) and nitrogen (N_2), in our case the composition is 95% N_2 and 5% H_2. During the annealing process, H_2 is passivating defects in the oxide and interface states [62, 63], leading to improved electrostatic control of the channel by the gate electrode and improved mobility due to decreased scattering rates. The purely thermal effects of annealing will contribute to minimizing the number of fixed charges [63].

3.2 LATERAL NANOWIRE DEVICES

The greatest difference between the lateral nanowire devices described here and the quantum well devices described in Section 3.1, is that these devices are 1-dimensional instead of 2-dimensional. These kinds of devices are more complex to fabricate, and the channel will be gated from three sides allowing for better electrostatic control of the channel. For certain exotic applications,

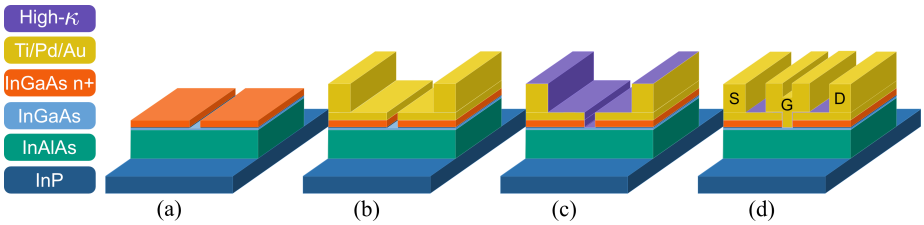


Figure 3.1: Schematic of the process flow of near-surface quantum well devices. First InGaAs n+ and InP is etched in the active region, followed by mesa etching down to the InP substrate (a). Next, source/drain electrodes are deposited followed by deposition of the thicker source/drain measurement pads (b). Passivation in $(NH_4)_2S$:H_2O is performed just before deposition of high-κ (c). Finally, the gate pad is deposited, and high-κ is etched on top of source/drain measurement pads (d).

for instance realization of Majorana fermions, a 1-dimensional semiconductor is required [64].

In this thesis work, we fabricated a demultiplexer device in the form of a lateral nanowire network, see Paper V. Our device is a so-called 1-to-4 demultiplexer, which takes one input signal and delivers it to one of four outputs, using four control signals, see Fig 3.2. The device allows for on-chip routing of DC-currents and could be used for Quantum Bit (**qubit**) biasing. For each layer added to the demultiplexer, the number of outputs is doubled, while the number of control signals only is increased by two. Our device is a proof-of-concept device, but a larger network could potentially address the challenge posed by the escalating number of cables entering the cryostat, a challenge that intensifies with the growing number of **qubit**s. A schematic of the process flow is shown in Fig. 3.3, in this case for a single lateral nanowire **MOSFET**, but the principle is the same as for a lateral nanowire network.

3.2.1 NANOWIRE GROWTH

The starting wafer is a **S.I.** InP substrate. On top of this substrate, we use Selective Area Epitaxy (**SAE**) to define our InGaAs nanowire, which acts as the channel of the device. **SAE** is an epitaxial method where a growth mask is used to define areas where the growth is blocked. In this way, arbitrary 2-dimensional growth geometries can be realized. However, care has to be taken regarding the resulting facets of the grown crystal. Compared to an etching scheme similar to what is described in 3.1.1 and 3.1.2, this method allows for smaller feature sizes, since the features are defined by the growth mask, and not broadened by isotropic etching.

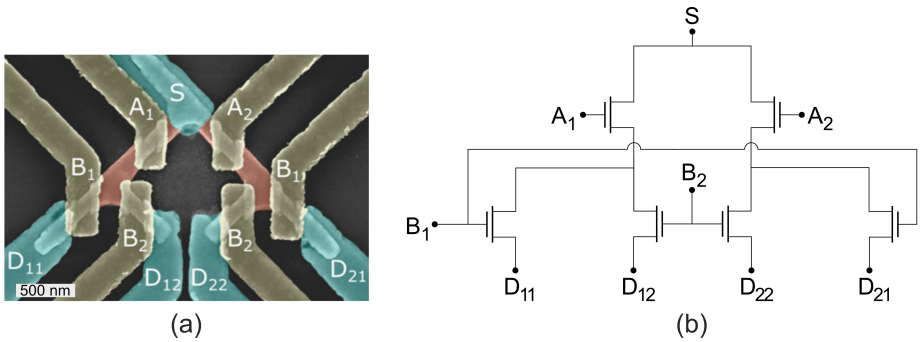


Figure 3.2: A false-colored Scanning Electron Microscope (**SEM**) image of a 1-to-4 demultiplexer is shown in (a), while a circuit representation is presented in (b). The device has one input (S), four gates (A_1, A_2, B_1, B_2), and four outputs (D_{11}, D_{12}, D_{22}, B_{21}). The gated parts of the InGaAs network are undoped, while the rest of the network is highly doped n+ InGaAs.

The growth mask needs to be electron-beam sensitive in order to facilitate the definition of small features using **EBL**, it also needs to withstand high temperature, since the temperature in the growth chamber is 600°C, and the nucleation of growth precursors on the resist needs to be much smaller than on the InP. Hydrogen Silsesquioxane (**HSQ**) is an excellent choice for this, and the one used in this thesis work. After spin-coating of **HSQ** and patterning using **EBL**, a pre-growth cleaning in hydrofluoric acid (HF) 1:1000 is performed, just before loading the sample into the growth chamber. The interface between the substrate and epitaxial layer is essential and needs to be as clean as possible to avoid donor-like defects at the interface, which counteracts the gate effect, see Paper I.

The growth is performed using Metal-Organic Chemical Vapour Deposition (**MOCVD**), and the dynamics of the **SAE** can be described as follows: when the growth precursor gases, in this case, trimethylgallium ($Ga(CH_3)_3$), trimethylindium ($In(CH_3)_3$) and arsine (AsH_3), are approaching the semiconductor surface, pyrolysis occurs. The subspecies will then diffuse from the growth mask into the openings, where surface reactions and epitaxial growth occur. The growth rate will be different in different crystal directions, where the growth rate perpendicular to the surface of the highest surface energy will be the fastest. This surface will thus be small or even disappear. The relative surface energy of the different surfaces will determine the facet structure of the nanowire. The growth is stopped when a desired thickness is reached, then the sample is unloaded and the growth mask removed.

3.2.2 CONTACT REGROWTH

In order to minimize contact resistance, the next step is to grow highly doped InGaAs where the source-drain contacts will be placed. To do this, we use a similar scheme as we did when defining the nanowire, see Section 3.2.1. **HSQ** is patterned using **EBL**, followed by **SAE** of highly doped InGaAs, and removal of the growth mask.

3.2.3 MESA DEFINITION

The device area is defined and the devices are electrically isolated, by the definition of a mesa. The mesa is defined using **HSQ** and **EBL**, followed by wet etching into the InP substrate. In this step, the **HSQ** mask acts as an etch mask instead of a growth mask.

3.2.4 SOURCE-DRAIN METALLIZATION

The source-drain electrodes need to be closely spaced and placed close to the n+ InGaAs edge, which requires high alignment accuracy. This is important in order to minimize access resistance. On the other hand, the measurement pads are large in order to facilitate wire bonding. **EBL** is much more time-consuming than **UVL** and not suitable for large area exposure. Therefore, this step is performed as two separate lithography steps. First, the small features are defined by **EBL**, evaporation and lift-off, and in a subsequent lithography step, the measurement pads are defined, by **UVL** using a **MLA**, followed by evaporation and lift-off. Just before evaporation, the native oxide on InGaAs is removed by HCl in order to avoid an oxide barrier at the semiconductor-metal interface.

3.2.5 PASSIVATION AND GATE OXIDE DEPOSITION

This step is performed in the same way as described for the devices under Section 3.1. The sample is cleaned and oxidized in an ozone atmosphere. Subsequently, the sample is immersed in $(NH_4)_2S$:H_2O, wherein the oxide is eliminated, and the surface undergoes passivation with sulfur to prevent re-oxidation [60]. The sample is then put into the **ALD** chamber, where pre-pulsing of **TMAl** is performed in order to restore surface As atoms to bulk-like bonding and reduce D_{IT} [61]. This is followed by the deposition of a bilayer of Al_2O_3 and HfO_2, which gives a high-quality interface in combination with a low **EOT**.

3.2.6 GATE METALLIZATION

The gate electrode metallization is performed in two separate steps. First, the gate arm is defined using **EBL** followed by evaporation and lift-off. In this step, the alignment is crucial in order to minimize the overlap between the gate and the source-drain contacts, and thus minimize parasitic capacitances. The gate pad is then defined by **UVL** using a **MLA**, followed by evaporation and lift-off.

3.2.7 ANNEALING

The annealing process is performed in the same way as for the near-surface quantum well devices, see Section 3.1.6. To improve the device performance in terms of **SS** and carrier mobility, the sample is annealed in forming gas (95% N_2/ 5% H_2). Throughout the annealing process, H_2 acts to passivate defects in the oxide and interface states [62, 63], resulting in improved electrostatic control of the channel by the gate electrode and enhanced mobility through reduced scattering rates. The purely thermal effects of annealing will contribute to minimizing the number of fixed charges [63].

3.3 VERTICAL NANOWIRE DEVICES USING TASE

The process outlined in this section is designed to facilitate a potentially straightforward heterogeneous 3D-integration of III-V devices in silicon (Si) Complementary Metal Oxide Semiconductor (**CMOS**) technology.

A major difference for these devices compared to the devices described in Section 3.1 and 3.2 is that we do not use III-V material as the substrate, instead we use standard Si wafers coated with silicon dioxide (SiO_2). In principle, we can use any substrate as long as it can be coated with tungsten (W). The nanowires are defined by Template-Assisted Selective Epitaxy (**TASE**) using **MOCVD**. **TASE** is sort of a derivative from Aspect Ratio Trapping (**ART**). In **ART** high aspect ratio trenches are formed in a dielectric, which acts as a growth mask for **SAE**. The idea is that threading dislocations originating from the Si/III-V interface will terminate on the vertical sidewalls of the trenches leaving a defect-free top part of III-V material [65]. In **TASE** the trenches are replaced by tubular openings in which defect-free III-V nanowires can be grown. In our process, we are growing vertical indium arsenide (InAs) nanowires directly on W. The approach is to tune the growth parameters in order to only get one nucleation event per opening. If the openings are much smaller than the growth precursors' diffusion length, it means that once a nucleation event has occurred, all new material arriving to the opening will be able to reach the nucleation site and continue the growth, instead of initiating

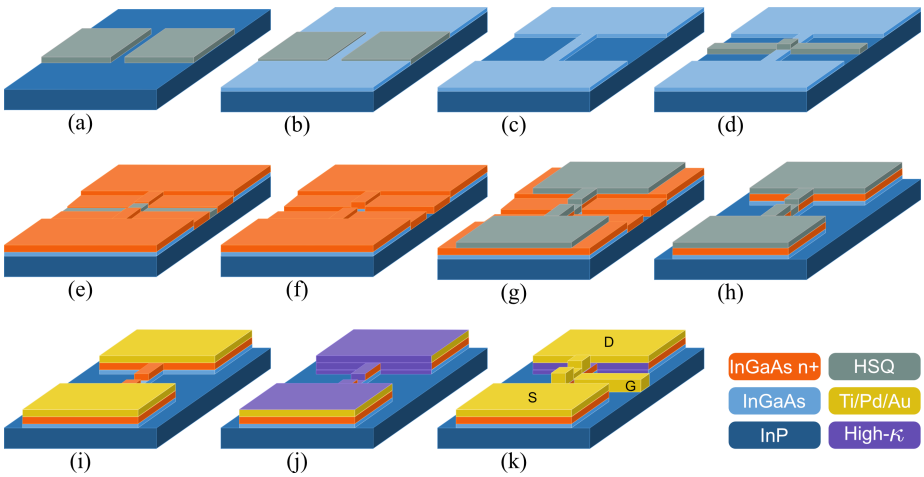


Figure 3.3: Schematic of the process flow of lateral nanowire devices. **HSQ** is patterned using **EBL** (a). **HSQ** acts as a growth mask for the **MOCVD** of InGaAs (b). The patterned **HSQ** used for the definition of the nanowire growth is removed (c) followed by patterning of a new layer of **HSQ** acting as a growth mask for the growth of highly doped n+ InGaAs (d). **MOCVD** of n+ InGaAs is performed (e) followed by removal of the **HSQ** growth mask (f). Next, a new layer of **HSQ** is patterned (g), followed by a mesa etch into the InP substrate (h). The **HSQ** etch mask is removed followed by deposition of source/drain contacts (i). Passivation in $(NH_4)_2S{:}H_2O$ is then performed just before deposition of high-κ (j). Finally, the gate pad is deposited, and high-κ is etched on top of source/drain measurement pads (k).

a second nucleation event. On the other hand, if the openings are much larger than the diffusion length of the precursors, they will not be able to reach the first nucleation site before they nucleate somewhere else. In this way, there is a critical size of the openings, which determines if the growth will be single- or polycrystalline, when growing on polycrystalline substrates. The diffusion length depends on the probability for a precursor to nucleate on the W surface and can be altered by the growth conditions. Different diameters of the tubular openings will thus require different growth conditions in order to get single crystalline growth from the bottom of the openings. In addition, to ensure nucleation on the W and not on the silicon nitride (Si_3N_4) template, the probability of nucleation on W must be sufficiently higher than the probability of nucleation on the Si_3N_4. Another important aspect is that the crystal extends and fills out the tubular hole in the template, otherwise, the crystal shape will not be defined by the template.

In order to facilitate easy integration of III-Vs in Si-**CMOS** technology, we performed **TASE** directly on W, see Paper VII. W is a commonly used metal at the interface between Front-End-Of-Line (**FEOL**) and Back-End-Of-Line (**BEOL**) in Si-**CMOS** stacks, and our approach is thus believed to enable easy integration of III-Vs in Si-**CMOS** technology. Furthermore, given that we are growing directly on W, our approach is highly flexible, allowing us, in principle, to utilize any substrate wafer. We are thus not relying on expensive III-V substrates. A schematic of the process flow is shown in Fig. 3.4.

3.3.1 LAYER STACK DEFINITION

On top of the starting Si/SiO_2 wafer, W is deposited by sputtering. The epitaxial growth of InAs will commence from this W-layer, which will also serve as the bottom contact of the device. Next, an etch-stop layer of Al_2O_3 is deposited using **ALD**, followed by deposition of the Si_3N_4 growth template using Plasma-Enhanced Chemical Vapor Deposition (**PECVD**). The Al_2O_3 etch-stop layer is intended to protect the W during the etching of Si_3N_4 in a subsequent step, while the thickness of the Si_3N_4 layer defines the final length of the nanowires.

3.3.2 ETCH MASK DEFINITION

It is very challenging to form high-aspect ratio openings in Si_3N_4, required for growth template formation. In order to create nanometer-sized tubular openings within the growth template of Si_3N_4, which is several hundred nanometers thick, an anisotropic dry etch is required. Wet etches are usually isotropic, while dry etches under certain conditions can be anisotropic [66]. In this case, we use fluorine (F) based Inductively Coupled Plasma (**ICP**) Reactive Ion Etching (**RIE**) at low pressure to define the tubular openings in the Si_3N_4 template. However, one critical issue is that the polymer resist used to transfer the pattern defined by **EBL** into the Si_3N_4 template, also is etched in the dry etch. The polymer will be thinned down, and the openings widened, therefore a more robust etch mask is needed. The pattern transfer into the Si_3N_4 is therefore performed in two steps, using a chromium (Cr) mask as the final etch mask for the pattern transfer. The Cr-mask is deposited on top of Si_3N_4 by evaporation, and patterned using **EBL** followed by chlorine (Cl) based **ICP-RIE**.

3.3.3 GROWTH TEMPLATE DEFINITION

The patterned Cr-mask is used as an etch mask in a F-based **ICP-RIE** dry etch into the Si_3N_4 template. The etch rate of Al_2O_3 is very slow, therefore the etch

stops at the Al_2O_3 etch-stop layer. After the definition of the tubular openings in the Si_3N_4, the Cr-mask is removed in a wet etch process.

3.3.4 NANOWIRE GROWTH

Just before growth, the etch stop is removed followed by the removal of the W-oxide. The growth is performed at a low **CMOS**-compatible temperature of 450°C. In order to get single crystalline growth and complete template filling, the growth is performed in two steps. In the nucleation step, we use a low precursor flow and low V/III ratio to avoid multiple nucleation events and polycrystalline nanowires. Then in the second growth step, the precursor flows and V/III ratio are increased in order to ensure complete filling of the tubular openings. A high V/III ratio will give similar growth rates in all crystal directions [67] and thus uniform nanowire lengths, even though the crystal orientation of the nanowires will vary.

3.3.5 VIA DEFINITION TO BOTTOM CONTACT

Since the nanowires are grown directly on the W-layer, we only need to contact this layer in order to get a bottom contact to the wires. **UVL** followed by F-based **ICP-RIE** of Si_3N_4 is used to form vias to the W-layer.

3.3.6 METALLIZATION

It is crucial that the top of the nanowires are properly connected, which could be challenging since the wires may not protrude much from the template. However, sputtering offers sufficiently good step coverage to solve this. Sputtering of nickel (Ni) and gold (Au) is followed by the definition of an etch mask using **UVL**. Next, wet etching of Au is followed by removal of the etch mask. Finally, Ni is etched using Au as an etch mask, and contacts to the top of the nanowires as well as the W-layer are created. Just before sputtering, the native oxide on the nanowires is removed in a wet etch in order to minimize R_C.

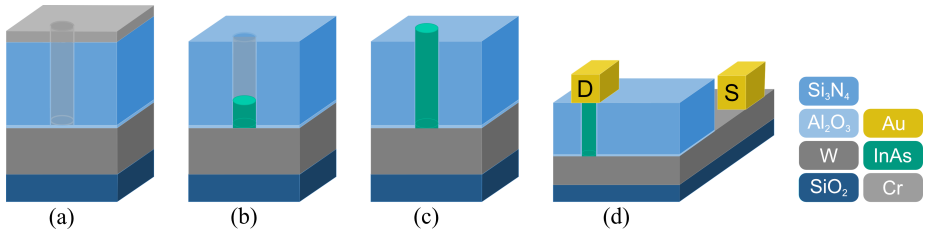


Figure 3.4: Schematic of the process flow. After preparation of the layer stack, **EBL** followed by Cl-based **ICP-RIE** is used to pattern the Cr hard mask. F-based **ICP-RIE** is then used in order to form vertical tubular openings in the Si_3N_4 growth template, using the Cr layer as etch mask (a). After removal of the Cr mask and the etch stop layer, **MOCVD** of InGaAs is performed (b) and (c). Next, **UVL** is performed followed by F-based **ICP-RIE** to form vias to the bottom W electrode, and finally measurement pads are deposited (d).

4

Device Characterization

LECTRICAL characterization of the III-V devices fabricated during this thesis work has been concentrated to Direct Current (**DC**) measurements at room temperature and cryogenic temperatures. In Paper I and Paper II, the focus has been to optimize the device performance in terms of Subthreshold Swing (**SS**) and carrier mobility, by pre-growth cleaning and Post-Metal Annealing (**PMA**). In Paper II, Positive-Bias Temperature Instability (**PBTI**) measurements were performed to evaluate the defect density in the gate oxide (high-κ) and high-κ/III-V interface.

The performance at cryogenic temperatures has been extensively evaluated in Paper III, Paper IV, Paper V, and Paper VI in order to explore the potential of these devices in low-temperature stages in scaled quantum computers, or as superconducting gatemon Quantum Bit (**qubit**)s. In combination with simulations, these results have gained a deeper understanding of Metal-Oxide-Semiconductor Field-Effect Transistor (**MOSFET**) operation at cryogenic temperatures, specifically the electron transport and mobility behavior.

Different methods to extract the carrier mobility have been studied in order to facilitate easy and proper device evaluation. In Paper III, the Geometrical Magnetoresistance Effect (**gMR**) method was used for the first time on indium gallium arsenide (InGaAs) **MOSFET**s, and it turns out to be a powerful tool for carrier mobility extraction in diffusive devices.

We have also characterized indium arsenide (InAs) nanowires grown on polycrystalline tungsten (W) to evaluate the potential of Template-Assisted Selective Epitaxy (**TASE**) on W as a way to facilitate easy 3D-integration of III-V devices in silicon (Si) Complementary Metal Oxide Semiconductor (**CMOS**) technology, see Paper VII. These devices were evaluated in terms of resistivity and field-effect mobility.

4.1 CONTACT RESISTANCE

The standard way to extract the contact resistance, R_C, is by measuring the resistance between two contacts as a function of the distance between the contacts. By applying a linear fit to the measured data, the resistance at zero distance between the contacts corresponds to $2R_C$. This method is called the Transfer Length Method (**TLM**), and can be applied on transistors. From measurements of the transfer characteristics in the linear mode of operation, the on-resistance, R_{ON}, can be extracted as $R_{ON} = \frac{V_{DS}}{I_{DS}}$ at a certain overdrive voltage, V_{OV}. If R_{ON} is extracted for devices of different gate lengths, L_G, and a least squares linear fit of R_{ON} versus L_G is performed, the contact resistance can be extracted. The intercept at $L_G = 0$ corresponds to $2R_C$, see Fig. 4.1. The transfer length, L_T, can also be extracted from the linear fit, corresponding to the intercept at $R_{ON} = 0$. The transfer length is the distance under the contacts in which a voltage drop occurs. The inverse of the slope of the linear fit is proportional to the effective mobility, μ_{EFF}, see Section 4.2.1 for details.

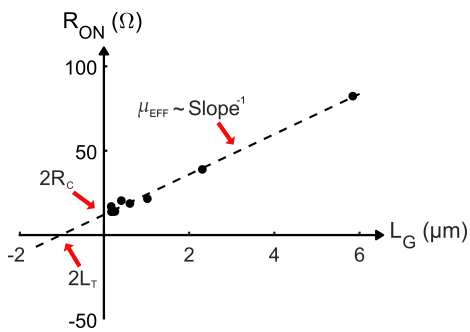


Figure 4.1: Typical plot of R_{ON} versus L_G for a near-surface quantum well device fabricated during this thesis work. A least squares linear fit is used to extract R_C, L_T, and μ_{EFF}.

The contact resistance depends on the interface quality between the metal electrode and the underlying semiconductor. It is crucial to remove any native oxide on the semiconductor before metal deposition; otherwise, the oxide will act as an insulating barrier between the semiconductor and the metal. The contact resistance also depends weakly on the difference between the work function of the metal, ϕ_M, and the electron affinity of the semiconductor, χ. In a simplified picture the barrier height, ϕ_B, called the Schottky barrier is set by, $\phi_B = \phi_M - \chi$, see Fig. 4.2. In reality, the primary factor influencing the barrier height at the interface, however, is associated with charges present at the interface.

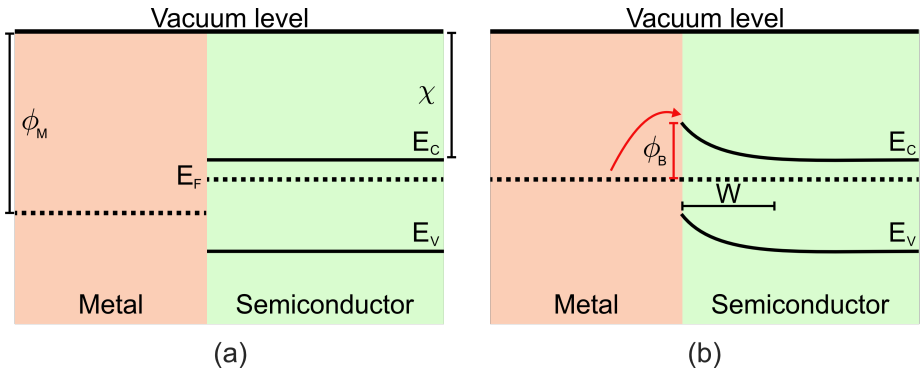


Figure 4.2: Schematic band diagram of the combination of a metal and an n-type semiconductor, neglecting the effect from charges at the interface. Before thermal equilibrium the work function of the metal, ϕ_M, and the electron affinity of the semiconductor, χ, are indicated (a). After thermal equilibrium has been established, a Schottky barrier, ϕ_B, is formed at the metal-semiconductor interface. The charge carriers have to overcome this energy barrier, and the transport is limited by thermionic emission. The width of the depletion region within the semiconductor is indicated by W (b).

For electrons to transfer between the metal contact and the semiconductor, they need to overcome the potential barrier at the interface. The current is thus limited by thermionic emission, and the net current density is given by

$$J_{Schottky} = A^* T^2 e^{\frac{-\phi_B}{k_B T}} \left(e^{\frac{qV}{k_B T}} - 1 \right), \tag{4.1}$$

where $A^* = 4\pi m^* q {k_B}^2 / h^3$ is the Richardson's constant, T is the temperature, k_B is Boltzmann's constant, V is the applied voltage, q is the elementary charge, m^* is the effective mass of the electrons, and h is Planck's constant [68]. The height of the Schottky barrier, ϕ_B, can thus be extracted from I-V measurements at different temperatures. The Schottky-barrier will give rise to a diode-like or rectifying behavior [69], but an Ohmic behavior can be obtained by increasing the concentration of dopants in the semiconductor. This will decrease the width of the barrier, which corresponds to the depletion region within the semiconductor. When the barrier width is sufficiently narrow, quantum mechanical tunneling can occur, see Fig. 4.3. The current density is then no longer limited by thermionic emission, but will instead depend on the tunneling probability.

Regardless of which metal is used, some semiconductors are more prone to form Ohmic contacts than others. This is related to charge accumulation at the metal-semiconductor interface. InAs, for instance, is known to form

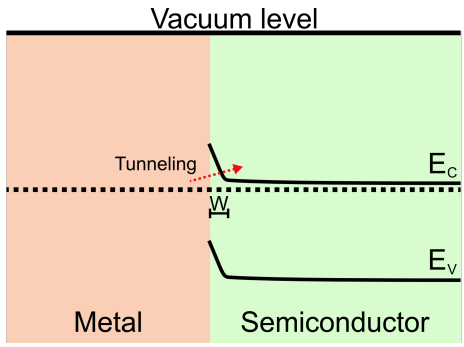


Figure 4.3: Schematic band diagram of the combination of a metal and a heavily doped n-type semiconductor. The width of the depletion region, W, is small due to the high dopant concentration, allowing for the tunneling of charge carriers between the metal and the semiconductor. The current is no longer limited by thermionic emission, but rather by the tunneling probability.

an Ohmic contact with most metals, which is explained by the fact that on both arsenic (As) and indium (In) terminated InAs, donor-like intrinsic surface states are formed, giving rise to electron accumulation layers [70, 71]. For InGaAs on the other hand, the Fermi level is usually pinned inside the band gap due to the formation of metal-induced gap states and interface states at the InGaAs surface [72]. The position at which the Fermi level is pinned depends however on the In-composition. For In-compositions above ~ 0.8, the Fermi level is pinned above the surface conduction band minima, while a lower In-composition gives a Fermi level pinned inside the band gap [73]. In Appendix D, a summary of R_C extracted from **TLM**-measurements for different semiconductor/metal combinations is presented along with the effective mobility, μ_{EFF}, extracted from R_{ON} versus L_G. For details about extraction and interpretation of μ_{EFF}, see Section 4.2.1.

4.2 CARRIER MOBILITY

The mobility of charge carriers in the semiconductor material is crucial for the device's performance. A higher mobility means lower R_{ON} and thus lower power consumption in the on-state. The high-frequency response is also set by the mobility of the charge carriers in the semiconductor channel, meaning that devices with higher carrier mobility can operate at higher frequencies. At low electric fields, the carrier velocity is proportional to the mobility, which means that the carriers travel faster through the device leading to a higher frequency response. Moreover, high-mobility materials exhibit

higher currents, facilitating quicker charging of capacitances. In more exotic applications, for instance, hybrid superconductor-semiconductor devices for quantum computation, the mobility is closely related to the ability to induce superconductivity in the semiconductor material [74].

There are different ways to extract the carrier mobility, and these different mobilities are not equivalent. In the next few sections, different mobility extraction methods used in this thesis work will be discussed, and their differences in interpretation and measurement procedures will be highlighted.

4.2.1 EFFECTIVE MOBILITY

In Paper I, and Paper II, the effective mobility is extensively used as an evaluation of the device performance. The effective mobility is closely related to the average mobility of the charge carriers in the channel of the **MOSFET**, and in the linear mode of operation the effective mobility is usually defined as

$$\mu_{\mathrm{EFF}} = \frac{L_{\mathrm{G}} I_{\mathrm{DS}}}{W Q_{\mathrm{CH}} V_{\mathrm{DS}}}, \tag{4.2}$$

where L_{G} is the gate length, W is the gate width, I_{DS} is the drain current, V_{DS} is the drain voltage, and Q_{CH} is the concentration of free charge carriers in the channel. It is important to note that Eq. (4.2) only is valid if compensated for series resistance. An accurate way to do this is by replacing $\frac{L_{\mathrm{G}} I_{\mathrm{DS}}}{V_{\mathrm{DS}}}$ with the inverse of the slope of a least squares linear fit to R_{ON} versus L_{G}, see Fig. 4.1. In this way, the effect from series resistance is eliminated and Eq. (4.2) becomes

$$\mu_{\mathrm{EFF}} = \frac{1}{W Q_{\mathrm{CH}} k}, \tag{4.3}$$

where k is the slope of the linear fit to R_{ON} versus L_{G}. Usually, we extract R_{ON} from the transfer characteristics at the bias point, $V_{\mathrm{OV}} = 0.3$ V and $V_{\mathrm{DS}} = 50$ mV, to ensure that we are in the linear mode of operation. The charge, Q_{CH}, is related to the gate bias, and how effectively the channel is controlled by the gate electrode, or in other words the gate capacitance, C_{G},

$$Q_{\mathrm{CH}} = C_{\mathrm{G}} V_{\mathrm{OV}}, \tag{4.4}$$

where V_{OV} is the overdrive voltage. Eq. (4.3) can then be written as

$$\mu_{\mathrm{EFF}} = \frac{1}{W C_{\mathrm{G}} V_{\mathrm{OV}} k}. \tag{4.5}$$

The effective mobility can also be extracted when the **MOSFET** is in saturation. Then, the current is described as

$$I_{\mathrm{DS}} = \frac{W}{2L_{\mathrm{G}}} \mu_{\mathrm{EFF}} C_{\mathrm{G}} (V_{\mathrm{GS}} - V_1 - V_{\mathrm{T}})^2, \tag{4.6}$$

where V_1 is defined according to Fig. 4.4.

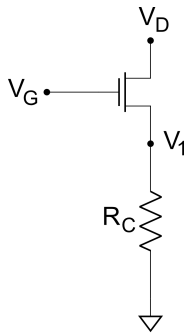


Figure 4.4: Circuit schematic of a n-**MOSFET**, showing the definition of V_1.

After noting that V_1 can be expressed in terms of I_{DS} and R_C, Eq. (4.6) can be rewritten as

$$I_{DS} = \frac{W}{2L_G}\mu_{EFF}C_G(V_{GS} - R_C I_{DS} - V_T)^2, \tag{4.7}$$

and by solving this equation for I_{DS} we obtain

$$I_{DS} = \frac{\mu_{EFF}C_G W(V_{GS} - V_T)^2}{2L_G(1 + \mu_{EFF}C_G\frac{W}{L_G}R_C(V_{GS} - V_T))}. \tag{4.8}$$

The effective mobility can then be extracted by fitting Eq. (4.8) to the measured transfer characteristics, using μ_{EFF} and R_C as fitting parameters.

4.2.2 FIELD-EFFECT MOBILITY

The field-effect mobility, μ_{FE}, is a lower estimation of the effective mobility, μ_{EFF}. Here the mobility is extracted from the transconductance, g_m, rather than from the drain conductance as in the case of μ_{EFF}. I_{DS} is related to V_{DS} according to

$$I_{DS} = \frac{W}{L_G}\mu_{EFF}C_G\left(V_{GS} - V_T\right)V_{DS} = \frac{W}{L_G}\mu_{EFF}Q_{CH}V_{DS}, \tag{4.9}$$

which gives

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{W}{L_G}\left(\frac{\partial \mu_{EFF}}{\partial V_{GS}}Q_{CH} + \mu_{EFF}\frac{\partial Q_{CH}}{\partial V_{GS}}\right)V_{DS}. \tag{4.10}$$

Usually, the approximation that the mobility does not depend on the gate bias is assumed, and (4.10) is simplified to

$$g_{\mathrm{m}} = \frac{W}{L_{\mathrm{G}}}\left(\mu_{\mathrm{FE}}\frac{\partial Q_{\mathrm{CH}}}{\partial V_{\mathrm{GS}}}\right)V_{\mathrm{DS}} = \frac{W}{L_{\mathrm{G}}}\mu_{\mathrm{FE}}C_{\mathrm{G}}V_{\mathrm{DS}}, \tag{4.11}$$

and when solved for the mobility,

$$\mu_{\mathrm{FE}} = \frac{g_{\mathrm{m}}L_{\mathrm{G}}}{WC_{\mathrm{G}}V_{\mathrm{DS}}}. \tag{4.12}$$

Due to the approximation that the mobility does not depend on the gate bias, see Eq. (4.10) and Eq. (4.11), μ_{FE} will be smaller than μ_{EFF}. In Paper VII, we used this approach to get a rough estimation of the lower bound of the carrier mobility of the device.

4.2.3 HALL MOBILITY

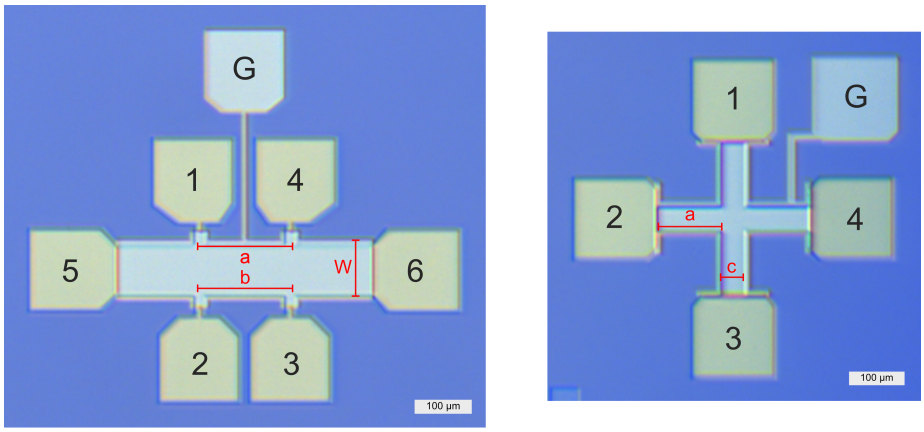
The Hall effect was discovered in 1879 by Edwin Hall [75], and today Hall effect measurements have become one of the most common methods for accurate characterization of electron transport in semiconductor material. Hall effect measurements combined with van der Pauw resistivity measurements, are used to extract the carrier concentration and resistivity of the semiconductor material. Using the carrier concentration and resistivity, the carrier mobility can be calculated. To get an accurate extraction of these properties, a test structure of certain geometry is required. Through this thesis work, we have mainly used two different test structures, namely Hall bars and Greek crosses, see Fig. 4.5. In the next few paragraphs, the procedure to extract the carrier concentration, the resistivity, and the carrier mobility from simple electrical **DC**-measurements in combination with applied magnetic fields will be explained.

When a charged particle is moving in an electric field, $\vec{E}$, and a magnetic field, $\vec{B}$, it will experience the Lorentz force,

$$\vec{F} = q\vec{E} + q\vec{v} \times \vec{B}, \tag{4.13}$$

where q is the charge of the carrier, and $\vec{v}$ is its velocity. In Fig. 4.6, a schematic of the electron transport in a 2-dimensional material is shown, under the influence of electric and magnetic fields.

If no $\vec{B}$ is applied, $\vec{v}$ will be parallel to $\vec{E}$, but the last term in Eq. (4.13) gives rise to a force which is perpendicular to both $\vec{v}$ and $\vec{B}$. Thus, if the electrons are traveling in the x-direction and a magnetic field is applied in the z-direction, the electrons traveling direction will bend towards the negative y-direction. If the device is long compared to its width, this will give rise to



(a) (b)

Figure 4.5: Optical images of a Hall bar (a) and a Greek cross (b). Important dimensions used when extracting the Hall mobility are indicated. All contacts are labeled by numbers except the gate which is labeled G.

accumulation of electrons on one side and depletion of electrons on the other side, and thus build up a so-called Hall voltage, V_{HALL}. When the steady state has been established the force on the electron due to V_{HALL} will be equal but opposite to the force from the magnetic field,

$$\frac{qV_{\mathrm{HALL}}}{W} = qv_x B_z, \tag{4.14}$$

where W is the width of the semiconductor, see Fig. 4.6.

The surface carrier concentration, n_s, can then be solved by using the fact that the charge carrier velocity, $v_x = \frac{I}{qn_sWt}$, where I is the current and t is the thickness of the semiconductor, see Fig. 4.6. This, combined with Eq. (4.14), gives

$$n_s = \frac{IB_z}{qV_{\mathrm{HALL}}t}. \tag{4.15}$$

Hall bars and Greek crosses are commonly used test structures for accurate determination of the carrier concentration. To get as accurate values as possible, the magnetic field is applied in both positive and negative directions, and the current is usually also sourced in both directions to eliminate the effect of thermoelectric voltages. Eq. (4.16) to Eq. (4.19) describe the set of measurements on the Hall bar in Fig. 4.5 (a), required to determine V_{HALL},

$$V^{B+}_{56,21} = \frac{V^{B+}_{21}(I^{+}_{56}) - V^{B+}_{21}(I^{-}_{56})}{2}, \tag{4.16}$$

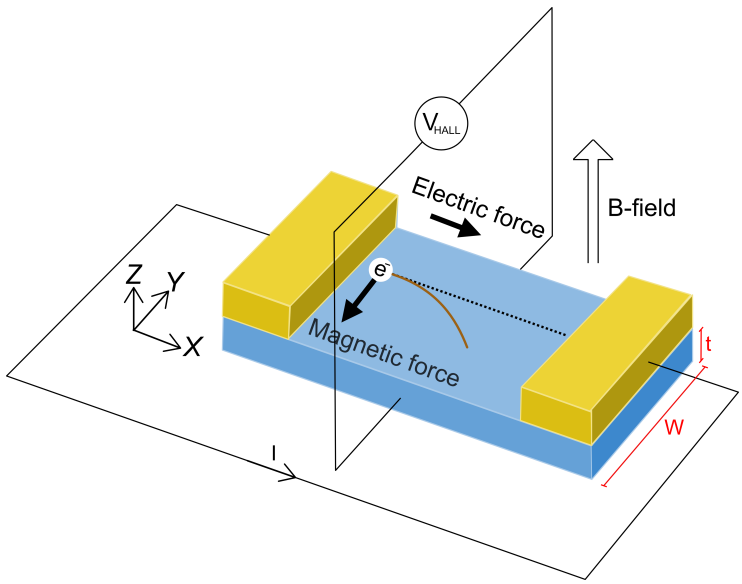


Figure 4.6: Schematic of an electron traveling in a 2-Dimensional Electron Gas (**2DEG**) under influence of electric and magnetic fields. The electric and magnetic forces are perpendicular, which gives rise to a centripetal force on the electron. Accumulation of electrons on one side of the **2DEG**, and depletion of electrons on the other side of the **2DEG**, gives rise to a Hall voltage, V_{HALL}.

$$V_{56,21}^{B-} = \frac{V_{21}^{B-}(I_{56}^{+}) - V_{21}^{B-}(I_{56}^{-})}{2}, \tag{4.17}$$

$$V_{\mathrm{HALL},1} = \frac{V_{56,21}^{B+} - V_{56,21}^{B-}}{2}. \tag{4.18}$$

$V_{\mathrm{HALL},2}$ is determined by performing the same set of measurements, but by measuring the voltage between 3 and 4 instead of between 2 and 1, see Fig. 4.5 (a). Ideally, $V_{\mathrm{HALL},1}$ and $V_{\mathrm{HALL},2}$ should be equal, and by calculating the average of these two Hall voltages, the impact of geometrical errors is reduced,

$$V_{\mathrm{HALL}} = \frac{V_{\mathrm{HALL},1} + V_{\mathrm{HALL},2}}{2}. \tag{4.19}$$

V_{HALL} is then used to calculate the carrier concentration according to Eq. (4.15). The same methodology as described in Eq. (4.16) to Eq. (4.19) applies to the Greek cross, see Fig. 4.5 (b), but $V_{\mathrm{HALL},2}$ is not required.

The resistivity can easily be extracted from a Hall bar using standard 4-terminal measurements. A current is sourced between 5 and 6, while the

voltage is measured between 1 and 4, or 2 and 3, see Fig. 4.5 (a). The resistivity is calculated according to (4.20) and (4.21),

$$\rho_a = \frac{V_{14}(I_{56}^+) - V_{14}(I_{56}^-)}{I_{56}^+ - I_{56}^-}\frac{W}{a}, \tag{4.20}$$

$$\rho_b = \frac{V_{23}(I_{56}^+) - V_{23}(I_{56}^-)}{I_{56}^+ - I_{56}^-}\frac{W}{b}, \tag{4.21}$$

where a, b, and W are defined in Fig. 4.5 (a). Note, that the current is measured in both directions to eliminate thermoelectric voltages. The resistivity in (4.20) and (4.21) should ideally be equal, but an average will reduce errors caused by geometric deviations,

$$\rho_{avg} = \frac{\rho_a + \rho_b}{2}. \tag{4.22}$$

One problem with this approach is that 1-dimensional transport is assumed. In fact, this is a 2-dimensional geometry, and Poisson's equation needs to be solved to determine the electrical potential throughout the sample and convert the resistance measurements to resistivity. But in 1958 van der Pauw described a method to extract the resistivity from a square sample with point contacts on the four corners of the sample. However, the van der Pauw method can be applied on Greek crosses, see Fig. 4.5 (b), giving an error less than 1% if $\frac{a}{c} > 1.5$ [76]. The method is as follows: first a current is sourced from 1 to 2, and the voltage between 4 and 3 is measured, this is performed in both directions to eliminate thermoelectric voltages. Then the reciprocal of this measurement is performed, namely, the current is sourced from 4 to 3 and the voltage between 1 and 2 is measured. These measurements give rise to two resistances which ideally should be equal,

$$R_{12,43} = \frac{V_{43}(I_{12}^+) - V_{43}(I_{12}^-)}{I_{12}^+ - I_{12}^-}, \tag{4.23}$$

$$R_{43,12} = \frac{V_{12}(I_{43}^+) - V_{12}(I_{43}^-)}{I_{43}^+ - I_{43}^-}. \tag{4.24}$$

The average of these two resistances gives a more accurate value of the resistance, reducing the influence of geometric deviations,

$$R_1 = \frac{R_{12,43} + R_{43,12}}{2}. \tag{4.25}$$

Next, the same set of measurements is performed between 1, 4 and 2, 3,

$$R_{14,23} = \frac{V_{23}(I_{14}^+) - V_{23}(I_{14}^-)}{I_{14}^+ - I_{14}^-}, \tag{4.26}$$

$$R_{23,14} = \frac{V_{14}(I_{23}^{+}) - V_{14}(I_{23}^{-})}{I_{23}^{+} - I_{23}^{-}}, \tag{4.27}$$

$$R_2 = \frac{R_{14,23} + R_{23,14}}{2}. \tag{4.28}$$

The sheet resistance, R_{SH}, is obtained by numerically solving the van der Pauw equation,

$$1 = e^{\frac{-\pi R_1}{R_{\mathrm{SH}}}} + e^{\frac{-\pi R_2}{R_{\mathrm{SH}}}}, \tag{4.29}$$

from which the sample resistivity is obtained $\rho = R_{\mathrm{SH}} t$, where t is the thickness of the conducting layer.

Now the Hall mobility, μ_{HALL}, can finally be calculated using the extracted surface carrier concentration from Hall effect measurements, and the extracted resistivity from van der Pauw measurements,

$$\mu_{\mathrm{HALL}} = \frac{1}{\rho n_s q}. \tag{4.30}$$

The advantage of Hall bars compared to Greek crosses is that the resistivity measurements are quicker. For Hall bars only four measurements are required, see Eq. (4.20) and (4.21), compared to Greek crosses where eight measurements are required, see Eq. (4.23), (4.24), (4.26), and (4.27). The extracted resistivity may, however, be more accurate when extracted from Greek crosses, since the van der Pauw method is applied. In addition, the Hall effect measurements are quicker for Greek crosses, where $V_{\mathrm{HALL},2}$ is not required and only four measurements are performed, compared to eight measurements for Hall bars, see Eq. (4.16), (4.17), and (4.18). Another benefit of Greek crosses is that they are possible to make smaller and only four contacts are needed for non-gated measurements, facilitating more devices per area and in addition simplifying the wire bonding of the devices.

4.2.4 gMR MOBILITY

For Hall effect measurements the device geometry should be long compared to its width, otherwise V_{HALL} will be shorted by the long contacts. **MOSFET**s usually have $L_{\mathrm{G}} << W$ making them bad devices for Hall effect measurements. On the other hand, even though V_{HALL} will be negligible, the Lorentz force, see Eq. (4.13), will make the charge carriers deviate from a straight traveling direction, increasing the traveling distance and effectively increasing the resistance between source and drain, see Fig. 4.6. This effect is called the Geometrical Magnetoresistance Effect (**gMR**). In general, also the resistivity of a semiconductor is increased when placed in a magnetic field, which is related to anisotropic conduction, or energy-dependent scattering [77]. This effect is

called the Physical Magnetoresistance Effect (**pMR**). The ratio between the resistance with and without applied magnetic field becomes

$$\frac{R_B}{R_0} = \frac{\rho_B}{\rho_0}\left[1 + (\mu_{gMR}B)^2\left(1 - 0.54\frac{L_G}{W}\right)\right], \tag{4.31}$$

where ρ_B is the resistivity in a magnetic field of magnitude B [78,79]. For a **MOSFET** the $\frac{L_G}{W}$ ratio is generally small, and the **pMR** effect is usually much smaller than the **gMR** effect, making the assumption $\frac{\rho_B}{\rho_0} \approx 1$ valid [77]. Eq. (4.31) can then be rewritten as

$$\frac{R_B}{R_0} \approx 1 + (\mu_{gMR}B)^2. \tag{4.32}$$

The μ_{gMR} can easily be obtained, by measuring transfer characteristics at different applied magnetic fields, calculating R_B and R_0, and fitting to Eq. (4.32), using μ_{gMR} as fitting parameter. An example of measured transfer characteristics and fitting of Eq. (4.32) to the extracted resistance, is shown in Fig. 4.7.

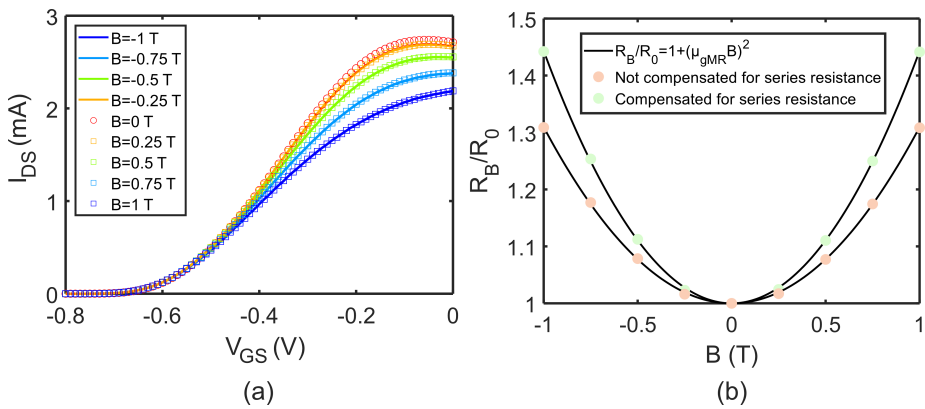


Figure 4.7: Transfer characteristics for different applied magnetic fields at $V_{\mathrm{DS}} = 50$ mV. The current decreases with increased magnetic field, and opposite field directions give the same current (a). The extracted resistance at $V_{\mathrm{GS}} = -0.25$ V as a function of the applied magnetic field, together with fits using Eq. (4.32). The importance of accurately extracted series resistance is clearly visible (b).

As seen in Fig. 4.7, the extracted μ_{gMR} is very sensitive to the effect of series resistance, and an accurate way to extract the series resistance of the devices is required to get reliable **gMR** mobilities. Another drawback of the **gMR** method, which we showed in Paper III, is that the **gMR** technique only works

for diffusive devices. Measurements on quasi-ballistic devices will give rise to considerably lower mobilities than the diffusive mobility of interest, which is related to the fact that the relaxation approximation used to obtain Eq. (4.32), only is valid for diffusive transport. There are however great advantages of the **gMR** method over the commonly used Hall method. For instance, the **gMR** method can be performed directly on **MOSFET**s, as long as they are diffusive and have $L_G << W$. Therefore, no extra test structures are required, giving more space on the chip, and only three contacts are needed, simplifying the wire bonding. The **gMR** measurements are in addition very quick, since only transfer characteristics are required, and the gate dependence of the mobility is directly obtained. In comparison μ_{FE} assumes no gate dependence, and Hall measurements need to be performed at all gate voltages of interest, in order to obtain the gate dependence. It has also been shown that the **gMR** approach works well even at low carrier densities [80], where the Hall approach becomes problematic.

4.2.5 SUMMARY OF MOBILITY EXTRACTION METHODS

The effective mobility, μ_{EFF}, can be extracted directly from the **MOSFET**s of interest, and is closely related to the average mobility of the charge carriers. However, if the extraction is performed in the linear region, several devices of different gate lengths are required. In saturation, it is possible to extract μ_{EFF} from single devices, and comparing this mobility to the one extracted in the linear region is a good sanity check, but keep in mind that the mobility depends on the carrier concentration and μ_{EFF} extracted in saturation should be higher than μ_{EFF} extracted in the linear region. In addition, the effective mobility is the mobility used in all theoretical models of **MOSFET**s, which makes μ_{EFF} interesting for device characterization. If several devices with different gate lengths are not available, the field-effect mobility, μ_{FE}, is a good estimation of the lower bound of μ_{EFF}. Hall mobility measurements require special test structures, and can not be performed on the **MOSFET**s. The Hall mobility, μ_{HALL}, is however a well-established technique, and the availability of Hall mobilities from different material systems, makes μ_{HALL} a good tool for performance comparisons. The **gMR** method is on the other hand a very sparsely used mobility extraction method. However, it has several strengths compared to other methods. It is quick and can be performed directly on the **MOSFET**s of interest, as long as they are diffusive and have $L_G << W$. In addition, the **gMR** method works well even at low carrier concentrations and inherently gives the gate dependence of the mobility. The main drawback is however that R_C influences the extracted mobility a lot, and an accurate method to extract R_C is thus required.

4.3 POSITIVE-BIAS TEMPERATURE INSTABILITY MEASUREMENTS

In today's **MOSFET** technology, the gate oxide is usually deposited by Atomic Layer Deposition (**ALD**). **ALD** enables scaling of the gate oxide and the possibility to deposit oxides with high relative permittivity (high-κ), improving the capacitive coupling of the gate electrode to the semiconductor channel. In Si technology, a so-called *reliability anneal* is usually performed to improve the quality of the dielectric layer. The annealing is often performed at as high a temperature as 900°C and decreases the number of defects in the oxide [81]. Annealing at this high temperature can however not be performed for III-V devices due to their lower thermodynamic stability. In Paper II, we investigated Atomic Hydrogen Annealing (**AHA**) as a low-temperature annealing process to mitigate this problem. In the paper, we performed **PBTI** measurements to characterize the defect concentration and defect distribution in the gate oxide.

When a positive gate bias is applied to the gate electrode, electrons from the semiconductor channel will move towards the gate, and may be trapped at defect sites inside the gate oxide, or at the high-κ/III-V interface. When the gate bias then is set to zero again, these trapped electrons will act as a negative bias on the gate electrode. This means that in order to turn the device on, a more positive bias is required compared to before any electrons were trapped. In other words, the trapped electrons will give rise to a positive V_T-shift.

To investigate this effect, **PBTI** measurements could be performed as follows: first one transfer curve is measured on a device in order to extract V_T. Then a certain V_{OV} is held for a certain time, after which the gate bias is set to zero and the drain current is measured. The measured drain current at zero gate bias is then compared to the original transfer curve, in order to extract the V_T-shift, see Fig. 4.8 (a). Next, the same procedure is performed on a second device, but for a different V_{OV}. If this procedure is performed on several devices at different V_{OV}, the defect density and defect distribution can be characterized. In Fig. 4.8 (b), a power law expression is fitted to the measured V_T-shift as a function of V_{OV}. The coefficient is proportional to the defect density, while the exponent is related to the defect distribution.

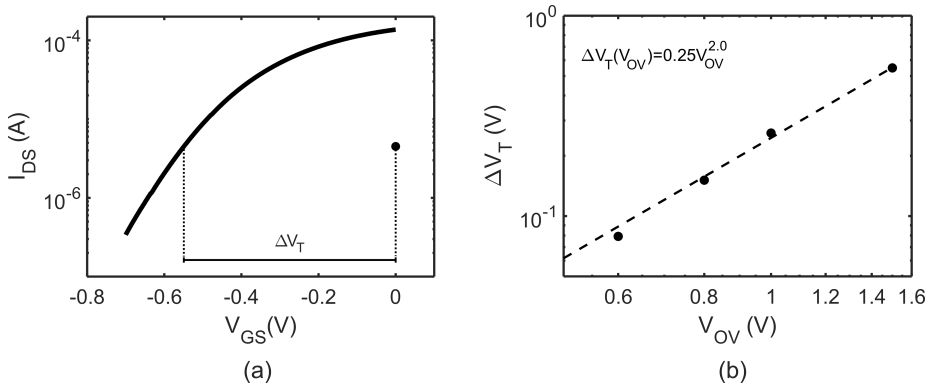


Figure 4.8: Transfer characteristics at $V_{DS} = 50$ mV, and measurement of I_{DS} at $V_{GS} = 0$ after holding $V_{OV} = 1.5$ V for 300 s. A positive V_T-shift of 0.55 V is observed (a). The V_T-shift after holding V_{OV} for 300 s is plotted versus V_{OV}, together with a power law fit to the measured data (b).

5

Conclusion and Outlook

This thesis has explored the potential of III-V devices in emerging electronic applications. III-Vs have properties that make them outperform silicon (Si) in certain applications, but they will probably never replace Si in digital electronics, due to their many drawbacks. III-Vs are a combination of two elements, which makes them more complex and difficult to work with compared to Si. In addition, they are not abundant in nature, which may be their greatest drawback. In order to utilize their outstanding mobility and direct band gap, but not be limited by their cost and rareness, they need to be integrated with Si-based technology.

The main contributions from this thesis work to the research community, are enhanced insights into III-V processing, increased knowledge about electron transport at cryogenic temperatures, and a demonstration of a possible way to facilitate easy 3D-integration of III-V devices in Si-Complementary Metal Oxide Semiconductor (**CMOS**) technology, without reliance on expensive III-V substrates.

In the first part of this chapter, a summary of our contributions to the research field, paper by paper, will be presented. The chapter's second part will discuss a completely new way to fabricate vertical nanowire Metal-Oxide-Semiconductor Field-Effect Transistor (**MOSFET**)s using a semiconductor-last approach based on Template-Assisted Selective Epitaxy (**TASE**). The chapter ends with an outlook toward an intriguing fusion of the semiconductor-last approach and superconducting electrodes, offering the potential realization of highly transparent interfaces between superconductors and semiconductors.

5.1 SUMMARY OF PAPERS

- Paper I "Optimization of Near-Surface Quantum Well Processing", doi: 10.1002/pssa.202000720.

  Emerging applications in cryogenic electronics require devices with extremely low power consumption and power dissipation in order to sustain low temperatures while accommodating an increasing number of devices. Furthermore, superconducting quantum computing based on hybrid superconductor-semiconductor devices, such as Majorana-based topological Quantum Bit (**qubit**)s and gatemon **qubit**s, rely on a gate-tunable semiconductor weak link with high mobility. In this paper, we optimized the process flow of near-surface indium gallium arsenide (InGaAs) **MOSFET**s and improved the device performance in terms of Subthreshold Swing (**SS**) and carrier mobility.

- Paper II "Low temperature atomic hydrogen annealing of InGaAs MOSFETs", doi: 10.1088/1361-6641/acc08c.

  III-V semiconductors are temperature sensitive, which makes it impossible to do a so-called *reliability anneal* at 900°C, usually performed in Si technology. Due to the inability to perform a high-temperature anneal, a high-quality gate dielectric and high-quality III-V/high-κ interface can not be realized. III-V devices therefore suffer from bad reliability and device variability. In this paper, we investigated the potential of Atomic Hydrogen Annealing (**AHA**) as a low-temperature annealing process for InGaAs **MOSFET**s. We conclude that the device performance in terms of **SS**, mobility, and reliability is improved by **AHA**, and comparable to improvements from Rapid Thermal Process (**RTP**) annealing in forming gas. **AHA** allows for a lower temperature compared to **RTP** annealing but instead a longer annealing time is required, and the thermal budget is thus not decreased. **AHA** seems to be comparable to annealing in forming gas, but not a superior annealing alternative.

- Paper III "Geometrical Magnetoresistance as a Tool for Carrier Mobility Extraction in InGaAs MOSFETs", doi: 10.1109/TED.2023.3318556.

  The carrier mobility is one of the most important properties of the semiconductor material used in **MOSFET**s and hybrid superconductor-semiconductor devices. In this paper, we explored the potential of

the Geometrical Magnetoresistance Effect (**gMR**) as a tool for mobility extraction in InGaAs **MOSFET**s. The **gMR** method shows excellent agreement with the mobility obtained from the well-established Hall effect method. In addition, the **gMR** method inherently gives the gate dependence and allows for measurements directly on the **MOSFET** of interest. However, we also showed the limitations of this method when it comes to ballistic or quasi-ballistic devices, where the extracted μ_{gMR} underestimates the diffusive mobility.

- Paper IV "Cryogenic Characteristics of InGaAs MOSFET", doi: 10.1109/TED.2023.3238382.

  Cryogenic electronics become more and more interesting as the interest in superconducting **qubit**s is increasing. To enable scaling of the number of **qubit**s, the control electronics must be integrated with the **qubit**s inside the cryostat. This will decrease the number of cables into the cryostat as well as the thermal noise. In this paper, we studied the current characteristics of near-surface InGaAs **MOSFET**s at cryogenic temperatures, in order to increase the understanding of electron transport in this regime. We developed a model, which takes into account band tail states, electron concentration dependent mobility, and density of interface traps. Our model accurately describes the device behavior down to cryogenic temperatures, and is important for understanding **MOSFET** operation in this temperature regime.

- Paper V "Low-Temperature Characteristics of Nanowire Network Demultiplexer for Qubit Biasing", doi: 10.1021/acs.nanolett.1c04971.

  To enable scaling of the number of **qubit**s, the number of cables from room temperature into the cryostat needs to be decreased. In this paper, we investigated the potential of on-chip routing of currents used for **qubit**-biasing, by fabrication of a demultiplexer based on an InGaAs nanowire network grown by Selective Area Epitaxy (**SAE**). Our 1-to-4 demultiplexer device worked as intended, and is a proof-of-concept device. However, in order to decrease the number of cables into the cryostat a larger network is required. For our device, four inputs are needed for the four outputs. Each new layer in the network will however double the number of outputs, while the number of inputs only is increased by two, or in other words a 1-to-2^n demultiplexer requires $2n$ inputs and has 2^n outputs.

- Paper VI "Gate-controlled near-surface Josephson junctions", doi: 10.1063/5.0182485.

  Hybrid superconductor-semiconductor Josephson Junction (**JJ**)s are an interesting platform for studying the superconducting proximity effect since they provide the possibility to tune the junction properties by a gate voltage. The Josephson Field-Effect Transistor (**JoFET**) is the central part in the realization of gate-controlled superconducting **qubit**s. In literature, there are several works on implementations of compact models for **JJ**s [82–84], but there are very few works that investigate the gate-tunable superconductor-semiconductor-superconductor junction. In this paper, we developed a model that can be used for actual non-ideal **JoFET**s. Our compact model considers the gate tunability of the semiconductor, the carrier density dependent mobility, non-ideal interfaces, and nonlinear excess resistances, allowing for circuit modeling with more realistic **JoFET**s. Our model enables system-level investigation of circuits containing **JoFET**s, which is essential for the development of gate-tunable **qubit**s. The validity of our model was confirmed by the successful reproduction of our measured data by circuit simulations.

- Paper VII "Three-Dimensional Integration of InAs Nanowires by Template- Assisted Selective Epitaxy on Tungsten", doi: 10.1021/acs.nanolett.2c04908.

  Today's digital electronics rely on Si-**CMOS** technology, while III-Vs are dominating high-frequency analog electronics, as well as optoelectronic applications. The possibility to integrate III-V devices in Si-**CMOS** technology is thus very interesting and considered essential for emerging 6G wireless networks [26]. In this paper, we developed a process for Metal-Organic Chemical Vapour Deposition (**MOCVD**) growth of vertical single crystalline indium arsenide (InAs) nanowires directly on tungsten (W), which is a commonly used metal between the Front-End-Of-Line (**FEOL**) and Back-End-Of-Line (**BEOL**) in the Si-**CMOS** stack. Our process is based on **TASE** performed at a **CMOS** compatible temperature of 450°C, showing potential for easy 3D-integration of III-V devices in Si-**CMOS** technology.

5.2 SEMICONDUCTOR-LAST APPROACH BASED ON TASE

The process scheme presented here is a further development of the process developed in Paper VII. The major difference is that the gate metal is formed inside the growth template, and the gate dielectric is deposited before the growth of the III-V nanowires. A schematic of the process is shown in Fig. 5.1.

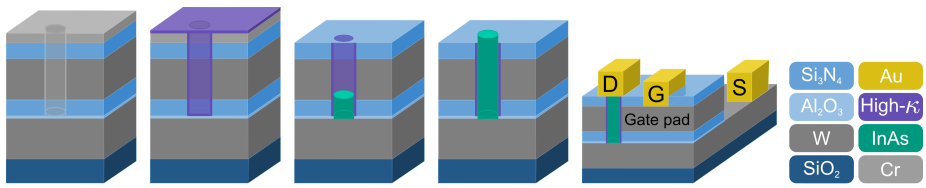


Figure 5.1: First the nanowire pattern is transferred into the chromium (Cr) hard mask using Electron-Beam Lithography (**EBL**) followed by chlorine (Cl) based Inductively Coupled Plasma (**ICP**) Reactive Ion Etching (**RIE**). The Cr-mask is subsequently used as an etch mask for anisotropic fluorine (F) based **ICP-RIE** down to the aluminum oxide (Al_2O_3) etch stop layer (a). Next, a high-κ oxide is deposited by Atomic Layer Deposition (**ALD**) (b). Anisotropic F-based **ICP-RIE** is then performed to remove high-κ from all planar surfaces (c). After removal of Al_2O_3 in Buffered Oxide Etchant (**BOE**), **MOCVD** of InAs is performed (c) and (d). Next, vias to the gate and bottom contact are formed by Ultraviolet Lithography (**UVL**) using a Maskless Aligner (**MLA**), followed by F-based **ICP-RIE**. Finally, the measurement pads are defined by sputtering, **UVL**, and wet etching (e).

This process scheme allows for high-temperature annealing of the gate dielectric before the growth of the temperature-sensitive III-V material, and will potentially also lead to a completely native oxide-free III-V/high-κ interface. There is thus potential to achieve very high quality of the III-V/high-κ interface, which could greatly improve the reliability of the III-V **MOSFET**s. The process also facilitates easy scaling of the gate length, which is defined only by the thickness of the intermediate W-layer, as well as vertical stacking of multiple devices by deposition of a second growth template on top of the first one. Since the nanowires are grown directly on W, this process could facilitate easy 3D-integration of III-V devices in Si-**CMOS** technology, but then high-temperature annealing can not be performed since it is not compatible with the Si-**CMOS BEOL**. However, another benefit of this process scheme is that we do not rely on expensive III-V substrates, but can deposit W and grow the nanowires on, in principle, any substrate.

5.3 HYBRID SUPERCONDUCTOR-SEMICONDUCTOR DEVICES USING TASE

One of the key challenges when fabricating hybrid superconductor-semiconductor devices is to get a high-quality superconductor-semiconductor interface and transparent contacts. It has been shown that a nearly perfect interface can be formed if the superconductor is grown in-situ on the semiconductor [64]. By growing the superconductor in-situ no native oxide is formed on the semiconductor. In the process described in Paper VII, we use a similar but somewhat inverted approach, where we grow the semiconductor on top of the metal. Even in this approach, the formation of native oxide on the semiconductor should be inhibited. It would thus be very interesting to replace our W bottom contact, see Fig. 5.1, with for instance a molybdenum rhenium alloy (MoRe), which is an exciting superconductor for hybrid device applications [85].

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APPENDICES

A

Fabrication of Near-Surface Quantum Well Devices

In this appendix, a detailed step-by-step process flow for fabrication of near-surface quantum well devices is presented. The intention is to provide researchers with the details required to reproduce the devices investigated in this thesis, but also facilitate the transfer of knowledge to future Ph.D. students in order to avoid the "reinvention of the wheel".

STARTING WAFER

A wafer with layer stack according to Table A.1 is used. The wafers are ordered from *Intelligent Epitaxy Technology, Inc.*, and the layers are grown by Molecular-Beam Epitaxy (**MBE**). The wafer stack is designed to maximize the carrier concentration in the high In part of the composite channel, resulting in high electron carrier mobility [86]. The purpose of the highly doped n+ InGaAs is to reduce the contact resistance.

GATE LENGTH DEFINITION

1. **Organic cleaning**
   - 3 min in acetone using ultra-sonic bath
   - 3 min in Isopropanol (**IPA**) using ultra-sonic bath
2. **Resist application**
   - Prebake on a hot plate at 200°C for 5 min
   - Spin coat adhesion promoter SurPass 4000 at 3000 rpm (1500 rpm/s) for 30 s
   - Rinse in H_2O for 1 min

Table A.1: Layer stack of starting wafer.

Layer	Material	x	Thickness (Å)	Dopant	Level $\left(\mathbf{cm}^{-3}\right)$	Type
10	$In_xGa_{1-x}As$	0.63	250	Si	4.0×10^{19}	n+
9	$In_xGa_{1-x}As$	0.53	200	Si	4.0×10^{19}	n+
8	InP		60	Si	1.0×10^{19}	n+
7	InP		10			i
6	$In_xGa_{1-x}As$	0.53	30			i
5	$In_xGa_{1-x}As$	0.80	50			i
4	$In_xGa_{1-x}As$	0.53	40			i
3	$In_xAl_{1-x}As$	0.52	30			i
2	$In_xAl_{1-x}As$	0.52	30	Si	1.0×10^{19}	n+
1	$In_xAl_{1-x}As$	0.52	1900			i
Substrate	S.I. InP					

- Prebake on a hot plate at 180°C for 5 min
- Spin coat resist PMMA 950 A4 at 4500 rpm (1500 rpm/s) for 60 s
- Postbake on a hot plate at 180°C for 2 min and 15 s

3. **Electron-Beam Lithography (EBL) exposure**
   - Acceleration voltage: 50 kV
   - Aperture: 30 µm
   - Writefield size: 500 µm
   - Area step size: 5 nm
   - Area base dose: 720 µC/cm^2
   - Line step size: 2 nm
   - Line base dose: 1200 pC/cm
4. **Resist development**
   - 90 s in Methyl Isobutyl Ketone (**MIBK**):**IPA** (1:3)
   - 30 s in **IPA**
5. **Oxygen plasma ashing and post baking**
   - 30 s O_2 plasma at 5 mbar, with cage
   - Postbake on a hot plate at 115°C for 10 min
6. **Recess etch**
   - 45 s in H_3PO_4:H_2O_2:H_2O (1:1:25)

- 1 min in H_2O
- 7 s in HCl:H_2O (1:1)
- 1 min in H_2O

7. **Strip etch mask**
   - 15 min in acetone on a hot plate at 60°C
   - 1 min in **IPA**
   - 30 s O_2 plasma at 5 mbar, with cage

MESA DEFINITION

1. **Resist application**
   - Prebake on a hot plate at 115°C for 5 min
   - Spin coat S1813 at 5000 rpm (1500 rpm/s) for 60 s
   - Postbake on a hot plate at 115°C for 90 s
2. **Maskless Aligner (MLA) exposure**
   - Dose: 200 mJ/cm^2
   - Defocus: 0
   - Laser wavelength: 405 nm
3. **Resist development and post baking**
   - 50 s in MF319
   - 1 min in H_2O
   - Postbake on a hot plate at 120°C for 15 min
4. **Oxygen plasma ashing**
   - 1 min O_2 plasma at 5 mbar, with cage
5. **Mesa etching**
   - 45 s in H_3PO_4:H_2O_2:H_2O (1:1:25)
   - 1 min in H_2O
   - 7 s in HCl:H_2O (1:1)
   - 1 min in H_2O
   - 200 s in H_3PO_4:H_2O_2:H_2O (1:1:25)
   - 1 min in H_2O
6. **Strip etch mask**
   - 30 min in Remover 1165 on a hot plate at 90°C
   - 2 min in H_2O
   - 1 min in **IPA**
   - 30 s O_2 plasma at 5 mbar, with cage

DEFINITION OF SOURCE AND DRAIN CONTACTS

1. **Resist application**
   - Prebake on a hot plate at 180°C for 5 min
   - Spin coat resist PMMA 950 A4 at 4500 rpm (1500 rpm/s) for 60 s
   - Postbake on a hot plate at 180°C for 2 min and 15 s
2. **EBL exposure**
   - Acceleration voltage: 50 kV
   - Aperture: 30 µm
   - Writefield size: 300 µm
   - Area step size: 5 nm
   - Area base dose: 720 $\mu C/cm^2$
3. **Resist development**
   - 90 s in **MIBK**:**IPA** (1:3)
   - 30 s in **IPA**
4. **Oxygen plasma ashing**
   - 30 s O_2 plasma at 5 mbar, with cage
5. **Removal of native oxide**
   - 20 s in HCl:H_2O (1:20)
   - 30 s in H_2O
6. **Evaporation**
   - Ti/Pd/Au (5/5/40 nm)
7. **Lift-off**
   - 15 min in acetone on a hot plate at 60°C
   - 3 min in acetone using ultra-sonic bath
   - 3 min in **IPA** using ultra-sonic bath
8. **Oxygen plasma ashing**
   - 30 s O_2 plasma at 5 mbar, with cage

DEFINITION OF SOURCE AND DRAIN MEASUREMENT PADS

1. **Resist application**
   - Prebake on a hot plate at 110°C for 5 min
   - Spin coat resist ma-N 440 at 6000 rpm (1500 rpm/s) for 45 s
   - Postbake on a hot plate at 95°C for 3 min
2. **MLA exposure**
   - Dose: 2000 mJ/cm^2
   - Defocus: 0
   - Laser wavelength: 375 nm

3. **Development**
   - 105 s in developer ma-D 532/s
   - 1 min in H_2O
4. **Oxygen plasma ashing**
   - 30 s O_2 plasma at 5 mbar, with cage
5. **Removal of native oxide**
   - 20 s in HCl:H_2O (1:20)
   - 30 s in H_2O
6. **Evaporation**
   - Ti/Pd/Au (5/5/300 nm)
7. **Lift-off**
   - 15 min in acetone on a hot plate at 60°C
   - 3 min in acetone using ultra-sonic bath
   - 3 min in **IPA** using ultra-sonic bath
8. **Oxygen plasma ashing**
   - 30 s O_2 plasma at 5 mbar, with cage

GATE OXIDE DEPOSITION

1. **Organic cleaning**
   - 2 min in acetone
   - 2 min in **IPA**
2. **Ozone cleaning**
   - 8 min ozone cleaning at 500 sccm O_2 flow
3. **Sulfur passivation**
   - 20 min in $(NH_4)_2S$:H_2O (1:1)
   - 7 s in H_2O
4. **Atomic Layer Deposition (ALD)**
   - 5 cycles of Trimethylaluminum (**TMAl**) at 300°C
   - 7 cycles of Al_2O_3 at 300°C
   - 100 cycles of HfO_2 at 120°C

DEFINITION OF GATE MEASUREMENT PAD

1. **Resist application**
   - Prebake on a hot plate at 110°C for 5 min
   - Spin coat resist ma-N 440 at 6000 rpm (1500 rpm/s) for 45 s
   - Postbake on a hot plate at 95°C for 3 min

2. **MLA exposure**
    - Dose: 2000 mJ/cm^2
    - Defocus: 0
    - Laser wavelength: 375 nm
3. **Development**
    - 105 s in developer ma-D 532/s
    - 1 min in H_2O
4. **Oxygen plasma ashing**
    - 30 s O_2 plasma at 5 mbar, with cage
5. **Evaporation**
    - Ti/Pd/Au (5/5/300 nm)
6. **Lift-off**
    - 15 min in acetone on a hot plate at 60°C
    - 3 min in acetone using ultra-sonic bath
    - 3 min in **IPA** using ultra-sonic bath
7. **Oxygen plasma ashing**
    - 30 s O_2 plasma at 5 mbar, with cage

DEFINITION OF HIGH-κ ETCH MASK

1. **Resist application**
    - Prebake on a hot plate at 115°C for 5 min
    - Spin coat resist S1813 at 5000 rpm (1500 rpm/s) for 60 s
    - Postbake on a hot plate at 115°C for 90 s
2. **MLA exposure**
    - Dose: 200 mJ/cm^2
    - Defocus: 0
    - Laser wavelength: 405 nm
3. **Development and post baking**
    - 50 s in developer MF319
    - 1 min in H_2O
    - Postbake on a hot plate at 120°C for 15 min
4. **Oxygen plasma ashing**
    - 1 min O_2 plasma at 5 mbar, with cage
5. **High-κ etch**
    - 8 min in Buffered Oxide Etchant (**BOE**) 10:1
    - 1 min in H_2O
6. **Strip etch mask**

- 30 min in Remover 1165 on a hot plate at 90°C
- 2 min in H_2O
- 1 min in **IPA**
- 30 s O_2 plasma at 5 mbar, with cage

ANNEALING

1. **Rapid Thermal Process (RTP) annealing**
   - 5 min in forming gas (N_2/H_2, 95/5%) at 350°C

B

Fabrication of Lateral Nanowire Devices

In this appendix, a detailed step-by-step process flow for fabrication of lateral nanowire devices is presented. The intention is to provide researchers with the details required to reproduce the devices investigated in this thesis, but also facilitate the transfer of knowledge to future Ph.D. students in order to avoid the "reinvention of the wheel".

STARTING WAFER

The wafer used for the fabrication of lateral nanowire device, is a (100) InP:Fe wafer ordered from *InPACT*. The epitaxial growth is performed in-house, using an Aixtron 200/4 MOCVD system.

NANOWIRE DEFINITION

1. **Organic cleaning**
   - 3 min in acetone using ultra-sonic bath
   - 3 min in Isopropanol (**IPA**) using ultra-sonic bath
2. **Ozone cleaning**
   - 10 min ozone cleaning at 500 sccm O_2 flow
3. **Resist application**
   - Prebake on a hot plate at 200°C for 5 min
   - Spin coat resist 2% Hydrogen Silsesquioxane (**HSQ**) at 6000 rpm (2000 rpm/s) for 60 s
   - Postbake on a hot plate at 200°C for 2 min
4. **Electron-Beam Lithography (EBL) exposure**

- Acceleration voltage: 50 kV
- Aperture: 30 µm
- Writefield size: 300 µm
- Area step size: 2 nm
- Area base dose: 1500 µC/cm^2

5. **Resist development**
   - 90 s in Tetramethylammonium Hydroxide (**TMAH**) (25%) on hot plate at 40°C
   - 1 min in H_2O
   - 30 s in **IPA**
6. **Baking and surface cleaning**
   - 60 min in O_2 at 350°C
   - 20 s in HF:H_2O (1:1000)
   - 30 s in H_2O
7. **Nanowire growth**
   - Selective Area Epitaxy (**SAE**) of 4 nm InP at 600°C
   - **SAE** of 13 nm InGaAs at 600°C
8. **Strip HSQ and contrast enhancement**
   - 4 min in Buffered Oxide Etchant (**BOE**) 10:1
   - 1 min in H_2O
   - 1 min in **IPA**
   - 4 s in HCl:H_2O (1:1)
   - 1 min in H_2O
   - 1 min in **IPA**

DEFINITION OF RAISED n+ CONTACTS

1. **Resist application**
   - Prebake on a hot plate at 200°C for 5 min
   - Spin coat resist 2% **HSQ** at 6000 rpm (2000 rpm/s) for 60 s
   - Postbake on a hot plate at 200°C for 2 min
2. **EBL exposure**
   - Acceleration voltage: 50 kV
   - Aperture: 30 µm
   - Writefield size: 300 µm
   - Area step size: 8 nm
   - Area base dose: 1500 µC/cm^2
3. **Resist development**

- 90 s in **TMAH** (25%) on hot plate at 40°C
- 1 min in H_2O
- 30 s in **IPA**

4. **Contact regrowth**
   - **SAE** of 25 nm Sn-doped InGaAs n+ at 600°C
5. **Strip HSQ**
   - 4 min in **BOE** 10:1
   - 1 min in H_2O
   - 1 min in **IPA**

DEFINITION OF MESA

1. **Resist application**
   - Prebake on a hot plate at 200°C for 5 min
   - Spin coat resist FOx-15 at 6000 rpm (2000 rpm/s) for 60 s
   - Postbake on a hot plate at 200°C for 2 min
2. **EBL exposure**
   - Acceleration voltage: 50 kV
   - Aperture: 40 µm
   - Writefield size: 300 µm
   - Area step size: 8 nm
   - Area base dose: 1500 $\mu C/cm^2$
3. **Resist development and post baking**
   - 2 min in **TMAH** (25%) at room temperature
   - 1 min in H_2O
   - 30 s in **IPA**
   - Postbake on a hot plate at 200°C for 5 min
4. **Mesa etch**
   - 35 s in H_3PO_4:H_2O_2:H_2O (1:1:25)
   - 1 min in H_2O
   - 4 s in HCl:H_2O (1:1)
   - 1 min in H_2O
   - 30 s in **IPA**
5. **Deposition of Si_3N_4**
   - Plasma-Enhanced Chemical Vapor Deposition (**PECVD**) of 14 nm Si_3N_4 at 200°C
6. **Strip HSQ and "lift-off" of Si_3N_4**
   - 100 s in **BOE** 10:1

- 1 min in H_2O
- 30 s in **IPA**

7. **Digital etch**
   - 8 min ozone cleaning at 500 sccm O_2 flow
   - 15 s in HCl:H_2O (1:10)
   - 30 s in H_2O
   - 30 s in **IPA**

DEFINITION OF SOURCE AND DRAIN CONTACTS

1. **Resist application**
   - Prebake on a hot plate at 180°C for 5 min
   - Spin coat resist PMMA 950 A4 at 4500 rpm (1500 rpm/s) for 60 s
   - Postbake on a hot plate at 180°C for 2 min and 15 s
2. **EBL exposure**
   - Acceleration voltage: 50 kV
   - Aperture: 30 µm
   - Writefield size: 300 µm
   - Area step size: 5 nm
   - Area base dose: 720 µC/cm^2
3. **Resist development**
   - 90 s in Methyl Isobutyl Ketone (**MIBK**):**IPA** (1:3)
   - 30 s in **IPA**
4. **Oxygen plasma ashing**
   - 30 s O_2 plasma at 5 mbar, with cage
5. **Removal of native oxide**
   - 20 s in HCl:H_2O (1:20)
   - 30 s in H_2O
6. **Evaporation**
   - Ti/Pd/Au (5/5/40 nm)
7. **Lift-off**
   - 15 min in acetone on a hot plate at 60°C
   - 3 min in acetone using ultra-sonic bath
   - 3 min in **IPA** using ultra-sonic bath
8. **Oxygen plasma ashing**
   - 30 s O_2 plasma at 5 mbar, with cage

DEFINITION OF SOURCE AND DRAIN MEASUREMENT PADS

1. **Resist application**
   - Prebake on a hot plate at 110°C for 5 min
   - Spin coat resist ma-N 440 at 6000 rpm (1500 rpm/s) for 45 s
   - Postbake on a hot plate at 95°C for 3 min
2. **Maskless Aligner (MLA) exposure**
   - Dose: 2000 mJ/cm^2
   - Defocus: 0
   - Laser wavelength: 375 nm
3. **Development**
   - 105 s in developer ma-D 532/s
   - 1 min in H_2O
4. **Oxygen plasma ashing**
   - 30 s O_2 plasma at 5 mbar, with cage
5. **Removal of native oxide**
   - 20 s in HCl:H_2O (1:20)
   - 30 s in H_2O
6. **Evaporation**
   - Ti/Pd/Au (5/5/300 nm)
7. **Lift-off**
   - 15 min in acetone on a hot plate at 60°C
   - 3 min in acetone using ultra-sonic bath
   - 3 min in **IPA** using ultra-sonic bath
8. **Oxygen plasma ashing**
   - 30 s O_2 plasma at 5 mbar, with cage

GATE OXIDE DEPOSITION

1. **Organic cleaning**
   - 2 min in acetone
   - 2 min in **IPA**
2. **Ozone cleaning**
   - 8 min ozone cleaning at 500 sccm O_2 flow
3. **Sulfur passivation**
   - 20 min in $(NH_4)_2S$:H_2O (1:1)
   - 7 s in H_2O
4. **Atomic Layer Deposition (ALD)**
   - 5 cycles of Trimethylaluminum (**TMAl**) at 300°C

- 7 cycles of Al_2O_3 at 300°C
- 100 cycles of HfO_2 at 120°C

DEFINITION OF GATE CONTACT

1. **Resist application**
   - Prebake on a hot plate at 180°C for 5 min
   - Spin coat resist PMMA 950 A4 at 4500 rpm (1500 rpm/s) for 60 s
   - Postbake on a hot plate at 180°C for 2 min and 15 s
2. **EBL exposure**
   - Acceleration voltage: 50 kV
   - Aperture: 30 µm
   - Writefield size: 300 µm
   - Area step size: 5 nm
   - Area base dose: 720 $\mu C/cm^2$
3. **Resist development**
   - 90 s in **MIBK**:**IPA** (1:3)
   - 30 s in **IPA**
4. **Oxygen plasma ashing**
   - 30 s O_2 plasma at 5 mbar, with cage
5. **Evaporation**
   - Ti/Pd/Au (5/5/40 nm)
6. **Lift-off**
   - 15 min in acetone on a hot plate at 60°C
   - 3 min in acetone using ultra-sonic bath
   - 3 min in **IPA** using ultra-sonic bath
7. **Oxygen plasma ashing**
   - 30 s O_2 plasma at 5 mbar, with cage

DEFINITION OF GATE MEASUREMENT PADS

1. **Resist application**
   - Prebake on a hot plate at 110°C for 5 min
   - Spin coat resist ma-N 440 at 6000 rpm (1500 rpm/s) for 45 s
   - Postbake on a hot plate at 95°C for 3 min
2. **MLA exposure**
   - Dose: 2000 mJ/cm^2
   - Defocus: 0

- Laser wavelength: 375 nm

3. **Development**
   - 105 s in developer ma-D 532/s
   - 1 min in H_2O
4. **Oxygen plasma ashing**
   - 30 s O_2 plasma at 5 mbar, with cage
5. **Evaporation**
   - Ti/Pd/Au (5/5/300 nm)
6. **Lift-off**
   - 15 min in acetone on a hot plate at 60°C
   - 3 min in acetone using ultra-sonic bath
   - 3 min in **IPA** using ultra-sonic bath
7. **Oxygen plasma ashing**
   - 30 s O_2 plasma at 5 mbar, with cage

DEFINITION OF HIGH-κ ETCH MASK

1. **Resist application**
   - Prebake on a hot plate at 115°C for 5 min
   - Spin coat resist S1813 at 5000 rpm (1500 rpm/s) for 60 s
   - Postbake on a hot plate at 115°C for 90 s
2. **MLA exposure**
   - Dose: 200 mJ/cm^2
   - Defocus: 0
   - Laser wavelength: 405 nm
3. **Development and post baking**
   - 50 s in developer MF319
   - 1 min in H_2O
   - Postbake on hot plate 120°C for 15 min
4. **Oxygen plasma ashing**
   - 1 min O_2 plasma at 5 mbar, with cage
5. **High-κ etch**
   - 8 min in **BOE** 10:1
   - 1 min in H_2O
6. **Strip etch mask**
   - 30 min in Remover 1165 on a hot plate at 90°C
   - 2 min in H_2O
   - 1 min in **IPA**

- 30 s O_2 plasma at 5 mbar, with cage

ANNEALING

1. **Rapid Thermal Process (RTP) annealing**
   - 5 min in forming gas (N_2/H_2, 95/5%) at 350°C

C

Fabrication of Vertical Nanowire Devices using TASE

In this appendix, a detailed step-by-step process flow for fabrication of vertical nanowire devices using TASE is presented. The intention is to provide researchers with the details required to reproduce the devices investigated in this thesis, but also facilitate the transfer of knowledge to future Ph.D. students in order to avoid the "reinvention of the wheel".

STARTING WAFER

In this process, we are flexible with the starting wafer, and in principle, any substrate can be used. Usually, we start with a standard SiO_2 coated Si wafer. The epitaxial growth is performed in-house, using an Aixtron CCS MOCVD system.

LAYER STACK DEFINITION

1. **Deposition of bottom contact**
   - Sputter 50 nm W at 100 W DC-power and 16 sccm Ar flow
2. **Deposition of etch stop**
   - 60 cycles Al_2O_3 at 250°C
3. **Deposition of Si_3N_4**
   - Plasma-Enhanced Chemical Vapor Deposition (**PECVD**) of 400 nm Si_3N_4 at 200°C
4. **Deposition of Cr hard mask**
   - Evaporation of 12 nm Cr

DEFINITION OF GROWTH TEMPLATE

1. **Resist application and Electron-Beam Lithography (EBL) exposure**
   - Spin coat with 230 nm AR-P resist (Performed at Chalmers)
   - **EBL** exposure and resist development (Performed at Chalmers)
2. **Oxygen plasma ashing**
   - 30 s O_2 plasma at 5 mbar, with cage
3. **Pattern transfer into Cr mask**
   - Inductively Coupled Plasma (**ICP**) Reactive Ion Etching (**RIE**) of Cr
   - Flows: Cl_2/O_2 (20/2 sccm)
   - **ICP** power: 800 W
   - Radio-Frequency (**RF**) power: 10 W
   - Pressure: 10 mTorr
4. **Strip resist**
   - 1 min O_2 plasma at 5 mbar, without cage
   - 5 min in Remover AR600-71
   - 1 min in H_2O
   - 30 s in Isopropanol (**IPA**)
   - 1 min O_2 plasma at 5 mbar, without cage
5. **Pattern transfer into Si_3N_4**
   - **ICP-RIE** of Si_3N_4
   - Flows: SF_6/N_2 (25/25 sccm)
   - **ICP** power: 400 W
   - **RF** power: 25 W
   - Pressure: 5 mTorr
6. **Remove Cr hard mask**
   - 15 min O_2 plasma in TEPLA using 800 W power
   - 3 min in Cr etchant
   - 3 min in H_2O
7. **Remove etch stop**
   - 30 s in Buffered Oxide Etchant (**BOE**) 10:1
   - 1 min in H_2O
8. **Remove W oxide**
   - 30 s in NH_4OH:H_2O (1:5) at 80°C

NANOWIRE GROWTH

1. **Nucleation step**

- Template-Assisted Selective Epitaxy (**TASE**) at 450°C using a low precursor flow and V/III ratio

2. **Template filling**
   - **TASE** at 450°C using a high precursor flow and V/III ratio

VIA FORMATION TO BOTTOM CONTACT

1. **Resist application**
   - Prebake on a hot plate at 115°C for 5 min
   - Spin coat resist S1813 at 5000 rpm (1500 rpm/s) for 60 s
   - Postbake on a hot plate at 115°C for 90 s
2. **Maskless Aligner (MLA) exposure**
   - Dose: 200 mJ/cm^2
   - Defocus: 0
   - Laser wavelength: 405 nm
3. **Development and post baking**
   - 50 s in developer MF319
   - 1 min in H_2O
   - Postbake on hot plate 120°C for 15 min
4. **Oxygen plasma ashing**
   - 1 min O_2 plasma at 5 mbar, with cage
5. **Si_3N_4 etch**
   - **ICP-RIE** of Si_3N_4
   - Flows: SF_6/N_2 (25/25 sccm)
   - **ICP** power: 400 W
   - **RF** power: 25 W
   - Pressure: 5 mTorr
6. **Remove etch stop**
   - 30 s in **BOE** 10:1
   - 1 min in H_2O
7. **Strip resist**
   - 30 min in Remover 1165 on a hot plate at 90°C
   - 2 min in H_2O
   - 1 min in **IPA**
   - 30 s O_2 plasma at 5 mbar, with cage

DEFINITION OF CONTACTS

1. **Removal of native oxide**
   - 20 s in HCl:H_2O (1:20)
   - 30 s in H_2O
2. **Deposition of metal**
   - Sputter 10/150 nm Ni/Au at 100 W DC-power and 9 sccm Ar flow
3. **Resist application**
   - Prebake on a hot plate at 115°C for 5 min
   - Spin coat resist S1813 at 5000 rpm (1500 rpm/s) for 60 s
   - Postbake on a hot plate at 115°C for 90 s
4. **MLA exposure**
   - Dose: 200 mJ/cm^2
   - Defocus: 0
   - Laser wavelength: 405 nm
5. **Development and post baking**
   - 50 s in developer MF319
   - 1 min in H_2O
   - Postbake on hot plate 120°C for 15 min
6. **Oxygen plasma ashing**
   - 1 min O_2 plasma at 5 mbar, with cage
7. **Etch Au**
   - 30 s in Au etchant
   - 1 min in H_2O
8. **Strip resist**
   - 30 min in Remover 1165 on a hot plate at 90°C
   - 2 min in H_2O
   - 1 min in **IPA**
   - 30 s O_2 plasma at 5 mbar, with cage
9. **Etch Ni using Au as etch mask**
   - 100 s in H_2O:H_2SO_4:HNO_3:CH_3COOH (15:1:2.5:2.5)
   - 1 min in H_2O

D

Summary of Extracted R_C and μ_{EFF}

In this appendix, a summary of the extracted contact resistance (R_C) for different semiconductor/metal combinations is presented, along with extracted values of the effective mobility (μ_{EFF}), see Table D.1. For the samples in this summary, the semiconductor stack is grown in-house, using an Aixtron 200/4 MOCVD system. The growth is performed at 600°C, and the substrate used is a (100) InP:Fe wafer from *InPACT*. The intention is to provide a transfer of knowledge to future Ph.D. students.

Table D.1: Summary of R_C extracted from Transfer Length Method (**TLM**) measurements, together with μ_{EFF} extracted from R_{ON} versus L_G.

Semiconductor	**Metal stack**	**Precleaning**	$\mathbf{R_C(\Omega\mu m)}$	μ_{EFF}**(cm²/Vs)**
Undoped InGaAs	Ti/Pd/Au	HCl:H_2O (1:20)	800	2100
Undoped InGaAs	Ti/Al/Ti/Pd/Au	HCl:H_2O (1:20)	15000	1700
Undoped InGaAs	Ti/Al/Ti/Pd/Au	$(NH_4)_2S$:H_2O (1:1)	9000	1900
n+ InGaAs	Ti/Pd/Au	HCl:H_2O (1:20)	20	
n+ InGaAs	Ti/Al/Ti/Pd/Au	$(NH_4)_2S$:H_2O (1:1)	5	
n+ InGaAs	Mo	HCl:H_2O (1:20)	200	

PAPERS

Paper I

Paper I

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ORIGINAL PAPER

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Optimization of Near-Surface Quantum Well Processing

*Patrik Olausson, Lasse Södergren, Mattias Borg, and Erik Lind**

Herein, an optimized process flow of near-surface quantum well metal–oxide–semiconductor field-effect transistors (MOSFETs) based on planar layers of metalorganic vapor-phase epitaxy (MOVPE) grown $In_xGa_{1-x}As$ is presented. It is found that by an optimized pre-growth cleaning and post-metal anneal, the quality of the MOS structure can be greatly enhanced. This optimization is a first step toward realization of a scalable platform for topological qubits based on a well-defined network of lateral $In_xGa_{1-x}As$ nanowires grown by selective area growth.

1. Introduction

The processing of near-surface quantum wells is of great interest for high-frequency III–V field-effect transistors (FETs), where near-surface quantum well metal–oxide–semiconductor field-effect transistors (MOSFETs) have potential to replace high electron mobility transistors (HEMTs). For short-channel FETs, the cutoff frequency is inversely proportional to the gate capacitance, C_g, which consists of the sum of an intrinsic gate–source capacitance, approximated as a plate capacitor, and parasitic capacitances.[1]

$$C_g = C_{g,intrinsic} + C_{g,parasitic} \approx \frac{\varepsilon_{barrier} L_G}{t_{barrier}} + C_{g,parasitic} \quad (1)$$

Here, $\varepsilon_{barrier}$ is the dielectric constant of the barrier between channel and gate contact, L_G is the gate length, and $t_{barrier}$ is the thickness of the barrier. A large $\varepsilon_{barrier}/t_{barrier}$ ratio is, therefore, preferred to reduce the influence of parasitic capacitances. The inherent structure of a MOSFET, where the channel is separated from the gate only by a thin gate oxide, is, thus, beneficial compared with a buried channel in HEMTs.

Another interesting application of near-surface quantum wells is in topological quantum devices. An exciting solid-state approach using near-surface quantum wells is Majorana-based qubits in which the quantum information is encoded in delocalized fermionic states. This way of encoding the qubits has a great advantage compared with other suggested platforms, which often suffer from short coherence times. As the quantum information is encoded in delocalized states, it will be protected against local perturbations and, thus, has a potential of very long coherence times.[2] However, even though the state is protected against local perturbations, it is possible to manipulate the state by physical exchange (braiding) of Majoranas, which is due to their non-abelian statistics.[3] It has been shown theoretically that Majorana quasiparticles will arise if a Josephson junction consisting of a 1D semiconductor sandwiched between two superconductors is placed in a magnetic field perpendicular to the spin–orbit interaction.[4,5] One requirement for reaching the topological phase is the closing and reopening of the superconducting gap. The superconducting gap is closed by the magnetic field, which breaks the Cooper pairs by aligning the electron spins, and the reopening then requires strong spin–orbit interaction to prevent the alignment of electron spins.[6]

Processing of near-surface quantum wells based on semiconductors with high mobility and strong spin–orbit coupling, such as InGaAs or pure InAs, is, thus, very interesting for high-frequency applications and Majorana-based quantum devices.

A well-defined network of lateral InGaAs nanowires has potential as an easily scalable system for topological qubits. One method of forming a branched nanowire network is through selective area growth, where a hard mask is used to pattern the growth.[7] This requires epitaxial growth utilizing only an ultrathin buffer layer. Residual oxides and impurity atoms at the substrate surface can then lead to poor material quality, as well as strong unintentional doping at the interface.

Optimization of near-surface quantum well processing compatible to selective area growth of lateral $In_xGa_{1-x}As$ nanowires is, therefore, a prerequisite to investigate the potential of this system as a platform for topological qubits. Here, the quality of near-surface $In_xGa_{1-x}As$ quantum wells grown on InP substrates is investigated, by varying the pre-growth treatment and post-metal anneal. The samples are evaluated by electrical characterization of MOSFET devices and evaluated in terms of subthreshold slope (*SS*) and mobility. The interface defect density on the top surface is particularly important to control, for minimal scattering and excellent electrostatic control of the quantum well potential.

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2. Results

Figure 1 shows the minimum *SS* for different pre-growth cleaning procedures prior to post-metal annealing (PMA). The samples are named by indium content (InXX) and InGaAs thickness ($t = $ YY nm). The mean value and 95% confidence interval are shown for each sample. It is clear that cleaning before growth will give rise to a decreased *SS* as compared to performing no cleaning at all. An insufficient clean of the InP prior to growth can lead to a high background electron concentration resulting in poor *SS* due to the induced second channel at the InP/InGaAs interface. A defect-rich InP surface can also give poor growth quality, leading to a large amount of interface defects (D_{it}) at the upper quantum well surface. In general, all the etchants improve the performance of the devices, resulting in a lower average *SS* and smaller device-to-device variation. Sulphur passivation ($(NH_4)_2S$:H_2O (1:1) for 20 min) is the cleaning procedure, which stands out here, with the lowest mean $SS = 135$ mVdecade^{-1}. This cleaning procedure, however, leads to a very low $I_{on} \approx 5 \times 10^{-7}$ A μm^{-1}, approximately a factor of 10 lower than the other samples, possibly indicating a defect-rich material. From atomic force microscopy (AFM) investigation, see **Figure 2**, step-flow growth is confirmed regardless if no cleaning, diluted hydrofluoric acid (HF 1:100), or $(NH_4)_2S$:H_2O (1:1) are used prior growth. The root mean squared (RMS) roughness is 126, 118, and 136 pm, respectively, for these three cases. However, if the substrate is cleaned using $(NH_4)_2S$:H_2O (1:1), evenly distributed dots appear on the surface; see Figure 2d. The source of these dots is not further investigated in this study, but it could be related to a precipitation process, in which solid material is formed in the solution ($(NH_4)_2S$:H_2O (1:1)) and then transferred to the sample surface. Due to these effects, this cleaning procedure was rejected. Another important aspect is that the cleaning procedure should not significantly etch hydrogen silsesquioxane (HSQ) resist, which has been successfully used as growth mask for selective area growth of lateral nanowires.[8] A significant drawback of HCl cleaning is that it etches InP (etch rate for HCl 1:1 is ≈4 nm s^{-1}), which could compromise the adhesion of HSQ. The etch rate, however, quickly decreases with decreasing HCl concentration.[9] HF etching before growth seems to give a better slope than if NH_4OH is used. In addition, it has been shown that the diluted HF can improve HSQ processing by removing residues caused by proximity effect and improve the contrast on the edges of HSQ lines.[10] Therefore, cleaning the substrate using HF gives the added benefit of removing HSQ residues caused by proximity effect and possibly also decreases the line edge roughness of HSQ patterns. Thus, HF etching (HF 1:1000) is chosen as the most promising cleaning procedure of the ones investigated here.

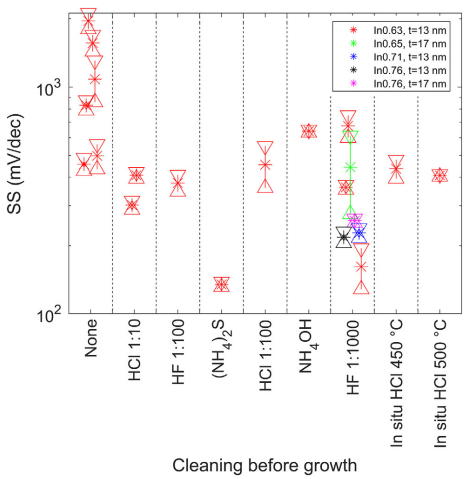

Figure 1. *SS* for different pre-growth cleaning procedures. The mean *SS* and 95% confidence interval are shown for each sample. For all samples, five to ten devices were measured, except for the In0.63, $t = 13$ nm sample with lowest *SS* cleaned using HF 1:1000 for which 96 devices were measured. It is clear that cleaning before growth improves *SS*, which could indicate a reduction of donor-like defects at the substrate–buffer layer interface.

In **Figure 3**a, the effect of PMA temperature on *SS* is shown for four different samples, which all had pre-growth clean using HF 1:1000. Evidently, the PMA process improves *SS* dramatically. Several studies have shown that annealing of InGaAs/HfO_2, InGaAs/Al_2O_3, or InGaAs/(Al_2O_3/ HfO_2) stacks in gas mixtures containing hydrogen leads to a significant reduction of D_{it},[11–15] which is explained by hydrogen passivation of defects in the oxide and interface states.[12] Increasing the annealing temperature tends to further improve *SS*. In addition, the spread between devices on the same sample also decreases, at least up to 350 °C annealing temperature. However, as shown in Figure 3b, above 350 °C some devices degrade, which could be related to diffusion at the semiconductor-high-k interface and crystallization of the relatively thick HfO_2 layer. At this high annealing temperature, the number of fixed charges close to the InGaAs channel could be increased due to the formation of Ga–O and decomposition of As–O and In–O, leading to more Coulomb scattering and lower mobility.[16] As the PMA is performed at the end of the device processing, the contacts are also annealed. At the annealing temperatures above ≈400 °C, degradation of the contacts is observed, probably due to Ti diffusion into the semiconductor leading to the formation of TiAs, whereas As and In are diffusing out from the bulk semiconductor leading to the formation of Ga-rich $In_xGa_{1-x}As$ and metallic In.[17] The optimal PMA temperature if Pd is included in the metal stack seems to be somewhere between 350 °C and 400 °C.

The concentration of interface defects (D_{it}) can be estimated from

$$SS = \frac{kT}{q}\ln(10)(C_{ox} + qD_{it})/C_{ox} \quad (2)$$

using the minimum *SS*. Using Equation (2), sample In0.76, $t = 17$ nm (see Figure 3), with $SS_{min} \approx 76$ mV decade^{-1}, gives $D_{it} \approx 3 \times 10^{12}$eV^{-1} cm^{-2}, which is consistent with D_{it} obtained from *C–V* (2×10^{12} to 4×10^{12}eV^{-1}cm^{-2}). According to the literature,[18]

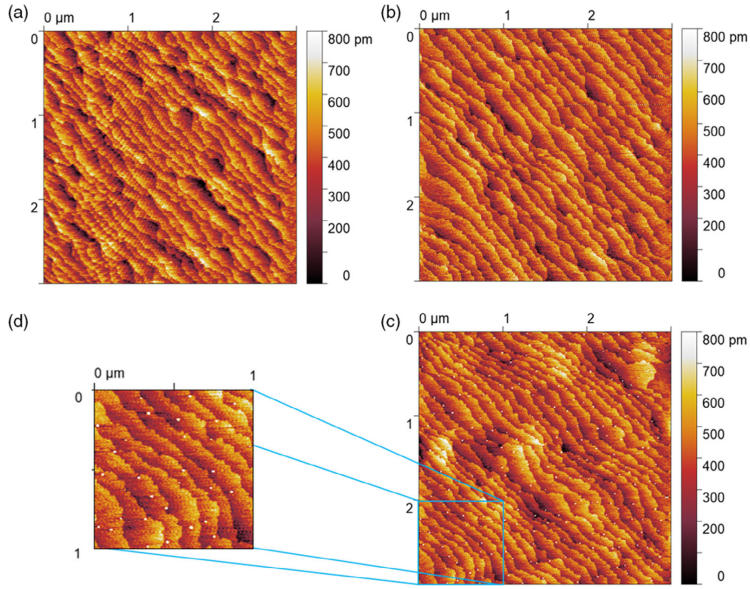

Figure 2. AFM images taken after growth of 4 nm InP followed by 13 nm InGaAs at 600 °C. a) No cleaning was performed before growth. b,c) Cleaning was performed using HF 1:100 and $(NH_4)_2S$:H_2O (1:1), respectively. In all three cases, step-flow growth occurs, and the degree of step bunching is similar in all cases. The main difference is the occurrence of evenly distributed dots on sample (c), which is clearly visible in (d). These dots could be the reason to the poor electrical performance of this sample.

the concentration of interface defects at the InGaAs–Al_2O_3 interface varies between $4 \times 10^{11} eV^{-1}cm^{-2}$ and $3 \times 10^{13} eV^{-1}cm^{-2}$, which also is in line with the value obtained in this work.

Figure 3c,d displays the extracted field-effect mobility and contact resistance obtained by fitting Equation (3) (see the Experimental Section) to the transfer characteristics. The mean value and 95% confidence interval are shown for each sample, and the mobility obtained from Hall measurements is indicated by a red star for the sample with 13 nm thick $In_{0.71}Ga_{0.29}As$ annealed at 350 °C. Both thickness and In content were determined by X-ray diffraction assuming a fully strained InGaAs layer. The Hall factor is defined as the ratio between Hall mobility and field-effect mobility and is between 1.2 and 1.25 for InGaAs at room temperature.[19] Using the highest and lowest field-effect mobility in the confidence interval (sample In0.71, $t = 13$ nm, see Figure 3c), we get a Hall factor between 0.91 and 3.24. The quite large spread of the Hall factor indicates some uncertainty in obtaining the field-effect mobility. The main factors influencing the field-effect mobility when extracting it from Equation (3) are D_{it} and contact resistance. D_{it} is accounted for in C_{it}, and the contact resistance is the second fitting parameter when extracting the field-effect mobility. The Hall mobility obtained here is consistent with previous works.[20] It is, however, interesting to note that the mobility is higher for samples with higher In content, which is in line with the fact that InAs has higher electron mobility than GaAs. In Figure 3d, the mean value of the fitted contact resistance, which is positive for all samples, is plotted together with a 95% confidence interval. Due to the uncertainty in extracting the resistance, some error bars reach negative values.

Further analysis of mobility and PMA temperature dependence is performed by one-way analysis of variance (ANOVA). The ANOVA analysis shows for all samples a 95% significant improvement of the mobility after PMA at 400 °C. For sample In0.76, $t = 17$ nm, a 95% significant improvement is achieved already at 300 °C PMA, whereas 400 °C is needed for the other samples. A comparison of the mean value of the field-effect mobility before and after PMA at 400 °C is shown in **Figure 4** for samples of varying In content and InGaAs thickness. As already evident in Figure 3c, a higher In content gives a higher mobility. Samples with equal In content (In0.76, $t = 17$ nm and In0.76, $t = 13$ nm) have almost the same mobility before PMA, but the sample with thinner $In_{0.76}Ga_{0.24}As$ shows a greater enhancement. This is not surprising, because a thinner $In_{0.76}Ga_{0.24}As$ layer means more electron transport close to the surface, and therefore, the improved surface quality achieved by the PMA process will have a greater impact on the mobility.

Figure 5 shows the transfer characteristics of a sample, which was cleaned before growth using HF 1:1000 and has a 13 nm thick $In_{0.71}Ga_{0.29}As$ layer. After annealing at 350 °C, the gate modulation is greatly improved, with a mean *SS* improving from

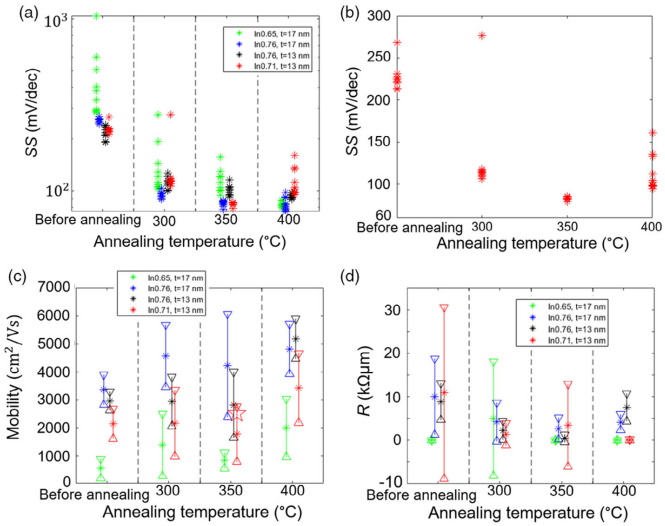

Figure 3. a) *SS* as a function of annealing temperature. Annealing leads to lower *SS*, and higher annealing temperature tends to further improve *SS*. b) One of the samples (In0.71, $t = 13$ nm) is plotted in linear scale indicating a minimum *SS* at 350 °C. c,d) The extracted mobility and contact resistance are shown as a function of PMA temperature. The mean value and 95% confidence interval are shown for each sample, and the mobility obtained from Hall measurements is included by a red star in (c) for the sample with 13 nm thick $In_{0.71}Ga_{0.29}As$ layer annealed at 350 °C. For all samples, five devices were measured to get the mean value.

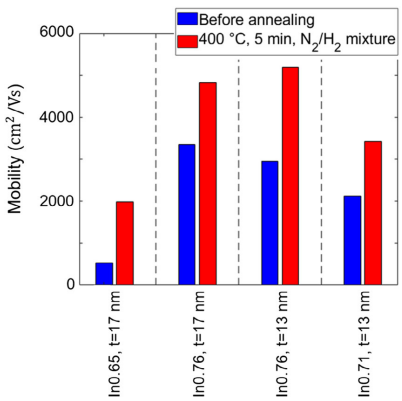

Figure 4. Comparison of mobility for samples with different In contents and channel thicknesses before and after PMA at 400 °C. The height of the bars corresponds to the mean value of the mobility. For all samples, five devices were measured to get the mean value. Higher In content gives rise to a higher mobility both before and after PMA. The annealing process has a greater impact on samples with thinner InGaAs layers, which is because more of the electron transport is close to the surface, and the improvement of the surface quality, thus, has a larger impact.

227 mV decade^{-1} to 84 mV decade^{-1}. A V_T shift also occurs, shifting the mean V_T from −0.23 to 0.17 V, and the V_T spread is decreased. Before annealing, a 95% confidence interval of V_T is between −0.28 and −0.18 V, and after annealing, this interval is between 0.15 and 0.19 V, reducing the spread by a factor of 2.5. Both improved gate modulation and increased V_T are consistent with the effect of PMA on buried InGaAs channels.[21] The minimum off-state current decreases with device width, indicating that surface leakage in the surrounding InP can be limiting for $W = 6$ μm. In **Figure 6**, transfer characteristics at 13 K are shown. The slope naturally becomes steeper compared with at room temperature because of the lower thermal energy of the electrons, and $SS = 17$ mV decade^{-1} as the best. The off-state leakage current is at the measurement noise floor, which indicates a suppressed surface leakage in the InP.

3. Conclusion

We have optimized the processing of near-surface quantum well devices as well as characterized the material quality of metalorganic vapor-phase epitaxy (MOVPE) grown $In_xGa_{1-x}As$ on InP (100). Pre-growth cleaning is vital avoiding donor defects at the interface between substrate and epitaxial layers and, thus, counteracts the gate effect. Pre-growth cleaning also reduces the number of defects at the $InGaAs/Al_2O_3$ interface and, therefore, improves the gate modulation and *SS*. HF 1:1000 is a

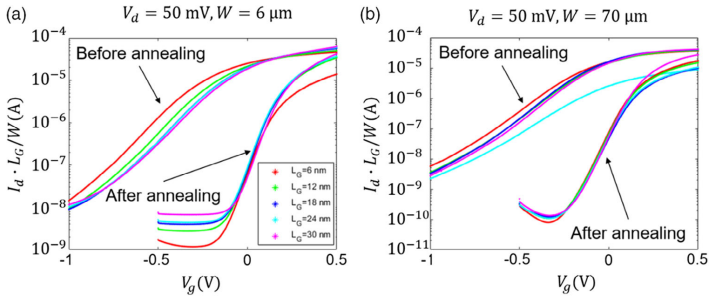

Figure 5. Transfer characteristics (normalized by L_G/W) before and after annealing (5 min in forming gas N_2/H_2, 95/5%) at 350 °C. The different curves correspond to devices with different gate lengths (L_G), ranging from L_G = 6 to 30 µm. The gate width is a) 6 µm and b) 70 µm.

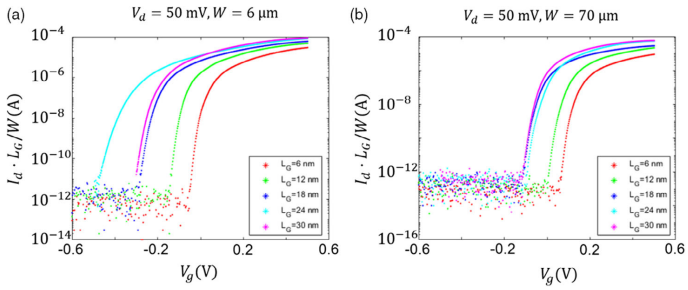

Figure 6. Transfer characteristics at T = 13 K (normalized by L_G/W) after annealing (5 min in forming gas N_2/H_2, 95/5%) at 350 °C. The different curves correspond to devices with different gate lengths (L_G), ranging from L_G = 6 to 30 µm. The gate width is a) 6 µm and b) 70 µm.

suitable choice for the pre-growth cleaning, because it is compatible with HSQ to be used as mask for selective growth and may even improve the quality of the HSQ patterns. In all cases, it is important to perform PMA to improve both *SS* and mobility further. PMA may reduce the number of defects in the gate oxide, but too high (>400 °C) annealing temperature will lead to worse *SS* possibly related to interdiffusion across the InGaAs/Al_2O_3 interface. In the current device process, PMA will also degrade the contacts if performed at temperatures above ≈400 °C, due to interdiffusion between metal and semiconductor.

This optimization is a first step toward realization of a scalable platform for topological qubits based on a well-defined network of lateral $In_xGa_{1-x}As$ nanowires grown by selective area growth.

Table 1. Pre-growth etch procedures used to reduce the effect of impurities at the substrate.

Etchants	Etch time
HCl 1:10	1 min
HCl 1:100	1 min
In situ HCl 450 °C	30 s
In situ HCl 500 °C	30 s
HF 1:100	3 min
HF 1:1000	20 s
$(NH_4)_2S$	20 min
NH_4OH	1 min

4. Experimental Section

InGaAs quantum wells were formed on InP:Fe (100) substrates by MOVPE. Prior to growth, the substrates were cleaned by ozone for 10 min at room temperature after which various pre-growth etching procedures, as tabulated in **Table 1**, were explored to obtain as clean and pristine surface as possible. Both HCl- and HF-based etchants have been shown to effectively remove epi-ready oxide on InP:Fe (100) substrates.[22] The wet etches are performed ex situ, and the samples are then transferred to an Aixtron 200/4 MOVPE within 2 min. The in situ HCl etchants are performed inside the MOVPE by flowing 2 sccm HCl at 100 mbar for 30 s. After the pre-growth etch step, a thin (4 nm) InP buffer layer is grown by MOVPE followed by growth of an $In_xGa_{1-x}As$ layer, where in different samples, the In content and thickness are varied between x = 0.63 and x = 0.76 and the thicknesses between 13 and 17 nm. The growth of both InP and InGaAs is performed at 600 °C and 100 mbar using trimethylgallium ($Ga(CH_3)_3$), trimethylindium ($In(CH_3)_3$), arsine (AsH_3), and phosphine (PH_3) as precursors, with H_2 as carrier gas. A schematic of the sample structure after growth is shown in **Figure 7**a. After growth, devices

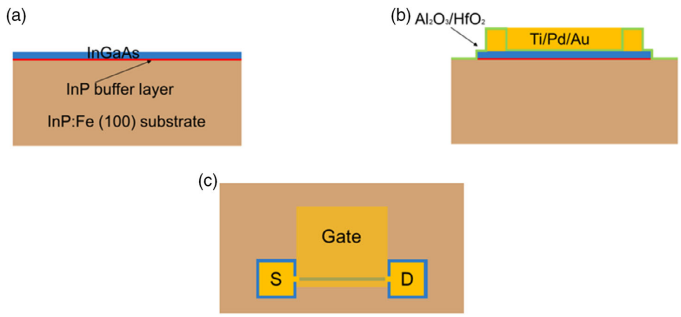

Figure 7. Schematics showing the sample structure after a) growth and b,c) processing. a) Material stack after growth. b) Cross section of finished device. c) Finished device, where source (S), drain (D), and gate contacts are labeled.

are fabricated into MOSFETs, with the gate lengths varying between 6 and 30 μm and the gate widths of 6–70 μm. Devices are electrically isolated by forming a mesa by UV lithography and wet etching (H_3PO_4:H_2O_2:H_2O (1:1:25) followed by HCl:H_2O (1:1)). Source and drain electrodes are defined by UV lithography, electron beam evaporation (Ti/Pd/Au or Ti/Au), and liftoff in acetone. For simplicity, the first devices were fabricated using Ti/Au contacts, but due to degradation of the contacts during annealing, Pd was later added to the metal stack acting as a diffusion barrier. The total contact resistance of source and drain can be estimated to ≈10 kΩ μm before annealing but is reduced after annealing; see Figure 3d. The large contact resistance originates from that the contacts are formed directly on the undoped thin quantum well. Cleaning and passivation of the InGaAs surface are performed by 8 min ozone cleaning at room temperature followed by immersion in $(NH_4)_2S$:H_2O (1:1) for 20 min just prior deposition of the gate oxide, consisting of Al_2O_3/HfO_2 (1/10 nm) deposited by thermal ALD at 300 and 100 °C, respectively. The thin interfacial layer of Al_2O_3 provides a high-quality interface to the semiconductor and reduced D_{it}, which also should improve *SS*.[23] A bilayer of Al_2O_3 and a high-k dielectric such as HfO_2 will, thus, provide low D_{it} in combination with a low equivalent oxide thickness (EOT).[24] The deposited oxide gives an oxide capacitance of $C_{ox} \approx 1.45$ μF cm^{-2}, which were determined by *C*–*V* measurements. A metal gate (Ti/Pd/Au or Ti/Au) is then fabricated by UV lithography and electron beam evaporation, and PMA is finally performed in forming gas (N_2/H_2, 95/5%) for 5 min. A schematic of a finished device is shown in Figure 7b,c.

As a first metric, the devices are evaluated on terms of their *SS*. Further characterization of selected samples is performed by AFM and low-temperature electrical characterization at 13 K. Field-effect mobility and contact resistance are also extracted by fitting the drain current of a long channel FET with source resistance, as given in the following equation

$$I_d = \frac{\mu_n C_g W (V_{gs} - V_T)^2}{2L_G\left(1 + \mu_n C_g \frac{W}{L_G} R_S (V_{gs} - V_T)\right)} \quad (3)$$

to the transfer characteristics. Here, μ_n is the electron mobility, C_g is the gate capacitance (calculated using C_{ox} obtained from *C*–*V* measurements and considering the channel quantum capacitance (C_q), the centroid capacitance (C_c), and the capacitance due to interface states (C_{it})), W is the gate width, V_{gs} is the gate–source voltage, V_T is the threshold voltage, L_G is the gate length, and R_S is the contact resistance. Equation (3) assumes a constant mobility, so it is an estimate of the field effect. A comparison with the more accurate measurement of Hall mobility is also made for one sample.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

InGaAs, metal–oxide–semiconductor field-effect transistors, metalorganic vapor-phase epitaxy, mobility, quantum wells

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Paper II

Paper II

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Low temperature atomic hydrogen annealing of InGaAs MOSFETs

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Abstract

Recent work showing a strong quality improvement of the Si/SiO_2 material system by low temperature atomic hydrogen annealing (AHA), and the fact that III–V semiconductors outperform Si in many applications makes the investigation of AHA on III–V/high-k interfaces to a very interesting topic. In this work, the potential of AHA as a low temperature annealing treatment of InGaAs metal–oxide–semiconductor field-effect transistors is presented and compared to conventional annealing in a rapid thermal process (RTP) system using forming gas. It is found that post metal annealing in atomic hydrogen greatly enhances the quality of the metal–oxide–semiconductor structure in terms of effective mobility, minimum subthreshold swing, and reliability. The device performance is comparable to RTP annealing but can be performed at a lower temperature, which opens up for integration of more temperature-sensitive materials in the device stack.

Keywords: InGaAs, MOSFETs, atomic hydrogen annealing, subthreshold swing, effective mobility, reliability

(Some figures may appear in colour only in the online journal)

1. Introduction

Today's digitalized society relies on the advancement of silicon complementary metal oxide semiconductor (CMOS) technology, but the limitations of down-scaling in combination with the rapidly increasing demand for added functionality not easily achieved in Si has pushed efforts to development of III–V semiconductor technology. The direct bandgap and higher carrier mobility of III–Vs would enable for high-performance optoelectronic and high frequency applications [1, 2]. Further, the ability to form highly-transparent interfaces to superconducting electrodes, as well as large spin–orbit interaction, make narrow bandgap III–Vs interesting for emerging quantum technologies [3, 4].

In III–V metal–oxide–semiconductor field-effect transistor (MOSFET) technology, the gate oxide is usually deposited using atomic layer deposition (ALD). ALD provides the possibility to deposit a gate oxide with high dielectric constant and thus a low equivalent oxide thickness (EOT). A bilayer of Al_2O_3/HfO_2 provides a high-quality interface to the semiconductor combined with a low EOT [5]. However, one of the key issues with III–V/high-k interfaces is to reduce the amount of interface traps, oxide traps and charged defects leading to degraded device performance. This is in general more difficult as compared with Si technology, due to complex oxides formed by the presence of several atomic species, as well as lower thermodynamic stability of III–Vs as compared with Si.

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The density of interface traps (D_{it}) is one limiting factor of the device performance in terms of the subthreshold swing (*SS*), see equation (1)

$$SS = \frac{kT}{q}\ln(10)\left(C_{ox} + qD_{it}\right)/C_{ox} \quad (1)$$

where, k is the Boltzmann constant, T is the temperature, q is the elementary charge, C_{ox} is the oxide capacitance and D_{it} is the density of traps which mainly originates from traps at the interface, as well as border traps. Also, a charged interface and border defects act as scattering centers, leading to increased channel scattering and reduced mobilities [6]. Reducing the effects of such defects are of importance to obtain high quality device operation, with high mobility and low subthreshold swings.

However, several studies have shown that annealing of InGaAs/HfO_2, InGaAs/Al_2O_3 or InGaAs/(Al_2O_3/HfO_2) stacks in gas mixtures containing hydrogen leads to a significant reduction of D_{it} [7–12] and increased mobility which can be explained by hydrogen passivating electrically-active border- and interface traps that inhibit Fermi level movement [8]. It has also been shown that hydrogen can passivate both O and Al dangling bonds, thus neutralizing fixed charges [9]. Even though annealing in gas mixtures containing hydrogen generally improves the device performance, III–Vs still suffer in device variability. This is due to the inability to realize high quality high-k and high-k/III–V interface at low annealing temperatures. In Si technology a high temperature reliability anneal at 900 °C is performed to yield high quality oxide and reliability. This can unfortunately not be performed in III–V technology due to their temperature sensitivity. It has however been shown that atomic hydrogen annealing (AHA), i.e. annealing a sample in a low pressure flow of hydrogen radicals, can greatly improve the oxide quality and reliability in Si/SiO_2 material systems [13, 14]. AHA at as low temperature as 100 °C gives even higher oxide quality than annealing at 900 °C in molecular hydrogen [14]. AHA has also shown great impact on Ge/GeO_2 interfaces [15]. So far the investigation of AHA in combination with III–Vs is lacking. Here, we investigate the potential of AHA as a low-temperature annealing process that possibly could give improved device performance and less device variability of III–V MOSFETs.

One application of III–V technology is as an add-on to silicon CMOS in the back-end-of-line (BEOL) for 3D heterogeneous integration. The BEOL technology has stringent demands on the temperature budget, which could fit well with the lower temperature used for III–V technologies. Thus, also a low-temperature annealing process is required. The investigation in this paper is focused on the InGaAs material system but should be applicable to other III–Vs, for instance GaN, which is very interesting for high-power applications.

Here, we postulate and systematically investigate the use of AHA to lower the temperature needed during the annealing process of InGaAs MOSFETs. This is performed by fabrication and annealing of InGaAs MOSFETs. The device performance is evaluated in terms of *SS* and effective mobility, μ_n. The mobility is related to the conductivity, σ, according to (2), where n and p corresponds to the electron and hole carrier concentrations, and μ_n and μ_p corresponds to the mobility of electrons and holes respectively. Since our device is unipolar, (2), can be rewritten as (3), which shows that the conductivity is directly proportional to the extracted mobility:

$$\sigma = q\left(n\mu_n + p\mu_p\right) \quad (2)$$

$$\sigma = qn\mu_n. \quad (3)$$

Investigation of threshold voltage (V_T) shifts and reliability measurements have also been performed as well as the gate current dependence on annealing temperature. The device performance is greatly enhanced with a peak performance when AHA is performed at 250 °C for 30 min. The effective mobility and *SS* are comparable to if rapid thermal process (RTP) annealing in forming gas is performed at 350 °C. The lower annealing temperature makes it possible for integration of more temperature-sensitive materials in the device stack.

2. Method

The devices used for this study are junction-less InGaAs MOSFETs fabricated on InP substrates. A schematic of the process flow is shown in figure 1.

Prior epitaxial growth, the substrate, InP:Fe (100), was cleaned using an optimized pre-growth cleaning procedure [16]. The substrates were cleaned by oxidation in ozone for 10 min followed by removal of the formed oxide by HF 1:1000 in order to get an as clean and pristine surface as possible. The epitaxial layers were then grown by metal organic vapor-phase epitaxy (MOVPE) in an Aixtron 200/4 reactor. After the pre-growth etch step, a thin (4 nm) InP buffer layer was grown followed by growth of an $In_{0.71}Ga_{0.29}As$ layer (13 nm). The growth was performed at 600 °C and 100 mbar using trimethylgallium ($Ga(CH_3)_3$), trimethylindium ($In(CH_3)_3$), arsine (AsH_3) and phosphine (PH_3) as precursors, with H_2 as carrier gas. MOSFETs were then fabricated, with varying gate lengths between 6 and 30 μm and gate widths of 6 and 70 μm. The devices were electrically isolated from each other by a mesa etch defined by UV lithography and wet etching (H_3PO_4:H_2O_2:H_2O (1:1:25) followed by HCl:H_2O (1:1)). Source and drain electrodes were defined by UV-lithography, electron beam evaporation (Ti/Pd/Au) and lift-off in acetone. Before deposition of the gate oxide the samples were cleaned and the InGaAs surface passivated by 8 min ozone cleaning at room temperature followed by immersion in (NH_4)$_2$S:H_2O (1:1) for 20 min. The deposited gate oxide consisted of a bilayer of Al_2O_3/HfO_2 (1/10 nm) deposited by thermal ALD at 300 °C and 120 °C, respectively. Then the gate metal was defined by UV lithography, electron beam evaporation (Ti/Pd/Au) and lift-off in acetone.

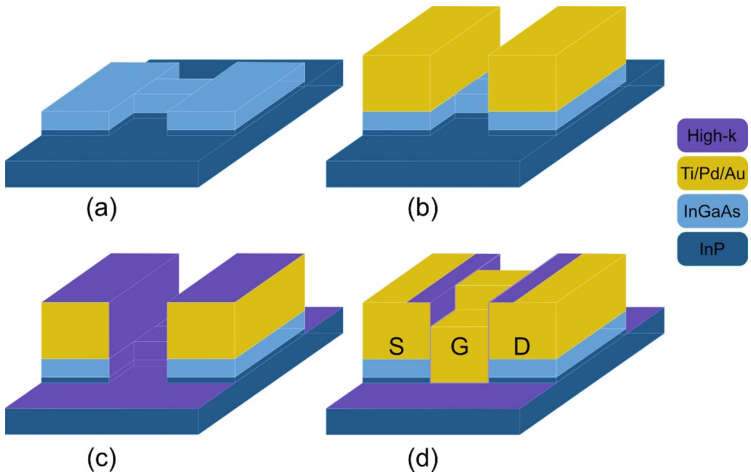

Figure 1. Schematic of the process flow of junction-less InGaAs MOSFETs. First a thin MOVPE grown layer of InP was grown on top of the InP substrate, followed by growth of the InGaAs channel. Next, a mesa etch was performed to electrically isolate the devices from each other (a). Then source and drain contacts were deposited by e-beam evaporation and lift-off (b). After passivation in $(NH_4)_2S{:}H_2O$ (1:1) the gate oxide was deposited by thermal ALD (c). Finally the gate contact was deposited followed by etching of high-k on top of source and drain contacts (d). Annealing was either performed after this step or before deposition of the gate oxide.

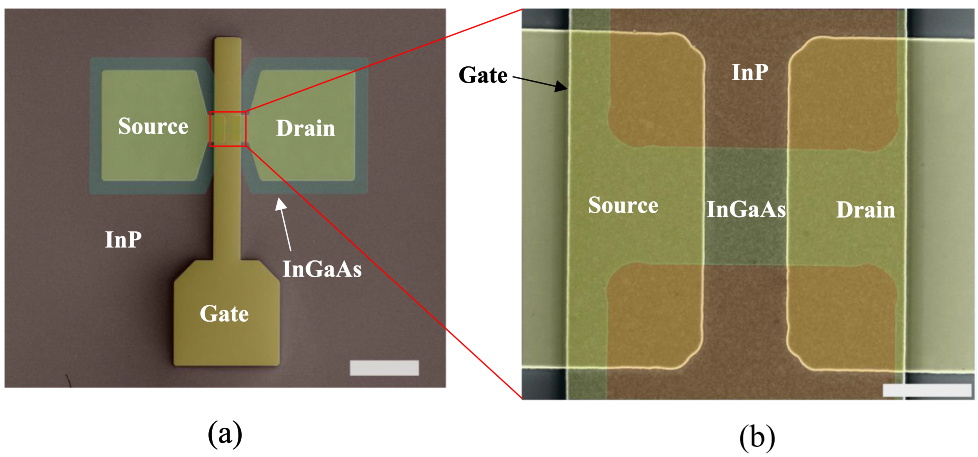

Figure 2. False colored SEM-images showing a finished device. The three terminals as well as the InGaAs channel and semi-insulating (SI) InP are indicated in the figures. The scale bar is 50 μm in (a) and 5 μm in (b).

For post deposition annealing (PDA) samples, AHA was performed before deposition of the gate electrode and for post metallization annealing (PMA) samples, AHA was performed after deposition of the gate electrode. A false colored SEM image of a finished device is shown in figure 2.

Fabricated devices were indium glued on a stainless-steel sample plate and then transferred into a UHV chamber ($p < 10^{-9}$ mbar) for AHA. A beam of hydrogen radicals (H·) was created using a commercial thermal cracker (from MBE Komponenten GmbH), operating at a cracking temperature of 1700 °C–1730 °C with a H_2 base pressure of 2×10^{-6} mbar and mounted 15–20 cm above the sample. Devices were annealed at temperatures between 100 °C and 350 °C for time intervals between 20 and 60 min. Sample temperatures above

250 °C were measured directly using a pyrometer and temperatures below the pyrometer limit ($T < 250$ °C) were measured using a thermocouple connected to the sample plate, which was calibrated using the pyrometer at higher temperatures. For comparison, devices were also annealed in H_2 (without thermal cracker) and Ar gas environment.

The devices were electrically evaluated by extraction of *SS* and effective mobility. The effective mobility is obtained from the slope of a least squares linear fit to the on-resistance (R_{on}) versus gate length (L_g), fitted for devices with L_g between 6 and 30 μm, see equation (4)

$$R_{on} = \frac{C_g \mu_n}{L_g V_{ov}} \tag{4}$$

where, $C_g \sim 0.6$ μF cm^{-2} is the gate capacitance and V_{ov} is the overdrive voltage (0.3 V). The devices were further investigated by reliability measurements, where the devices were stressed at a specific V_{ov} for 300 s and then the threshold voltage, V_T, shift was measured. A fresh device was used for each stress voltage.

3. Results and discussion

The electrical characterization showed a great improvement of the device performance by AHA, with a peak $\mu_n \sim 4500$ cm^2 Vs^{-1} and *SS* $\sim$ 100 to $\sim$110 mV/decade for AHA performed at 250 °C for 30 min. This is 100 °C lower temperature than RTP annealing but gives comparable device performance. The thermionic limit of *SS* at room temperature is 60 mV/decade, and the higher extracted value here can be explained by the relatively thick gate oxide of $\sim$10 nm. However, similar devices fabricated previously have measured *SS* below 80 mV/decade [16]. Please, note that in all figures (except figure 10) data from devices fabricated during different process runs are included. The devices are fabricated according to the same process scheme and should be very similar. The only parameter extracted that clearly depends on the specific process run is V_T, which is very sensitive to the conditions in the ALD chamber during deposition of the high-k, which may vary slightly from run to run. The spread between devices from the same process run is however small. In figures 7 and figure 9 the different process runs are indicated to make this clear. Figure 3 shows the minimum *SS* (a) and effective mobility (b) for samples annealed in atomic hydrogen for 30 min at different temperatures. Both *SS* and μ_n are compared to samples annealed in a RTP system at 350 °C for 5 min in forming gas. A comparison between PMA and PDA is also included. Before annealing a 95% confidence interval gives *SS* from $\sim$190 to $\sim$200 mV/decade and μ_n from $\sim$1200 to $\sim$2300 cm^2 Vs^{-1}. It is clear that PMA gives better result than PDA both in terms of *SS* and effective mobility. The highest performance for PMA samples is at an annealing temperature of 250 °C, showing a strong improvement in mobility to $\mu_n \sim 4500$ cm^2 V^{-1} s^{-1} as well as a reduction in *SS* down to $\sim$100 to $\sim$110 mV/decade. The performance then decreases with higher temperature, which could be related to diffusion at the semiconductor/high-k interface and/or crystallization of the relatively thick HfO_2. Especially for the PDA anneals both the mobility and *SS* degrades quickly for higher temperatures, and above 250 °C the PDA data shows very scattered R_{on} versus L_g which makes it impossible to reliably extract an effective mobility. At 250 °C the PMA AHA sample has comparable *SS* to the RTP annealed sample but even higher effective mobility. In the case of the mobility we only have one data point and no strong conclusion can be drawn, but this indicates that AHA could be a feasible route for passivation of interface defects at reduced temperatures.

To explore lower temperature budgets, in figure 4 even lower temperatures are investigated and the annealing time is kept constant at 20 min. The effective mobility and *SS* are shown as a function of annealing temperature. The device performance of the AHA samples are increasing with increasing annealing temperature up to 250 °C, giving *SS* down to $\sim$100 mV/decade and $\mu_n \sim 2900$ cm^2 V^{-1} s^{-1}. But even at much lower temperature, $T = 150$ °C, there is a great improvement compared to before annealing which reduces *SS* $\sim$120 to $\sim$125 mV/decade and μ_n to $\sim$2600 cm^2 V^{-1} s^{-1}. The best values for *SS* at $T = 250$ °C is comparable to the RTP annealed samples while the maximum effective mobility is lower, but as we can see in figure 5 the maximum effective mobility for the AHA samples is after 30 min annealing. In figure 5 *SS* and effective mobility is plotted against annealing time for samples annealed at 250 °C. For AHA samples the performance improves until 30 min annealing and then starts to degrade, which again could be explained by diffusion at the semiconductor/high-k interface. After 30 min the performance is comparable to the RTP annealed sample but with higher effective mobility.

Figure 6 shows annealing in different atmospheres. Blue data points correspond to annealing at 250 °C for 20 min, while red data points correspond to RTP annealing for 5 min in forming gas, and black data points are measured before any annealing. It is clear that the performance is not improved as much if the annealing is performed in Ar compared to H_2 or H·. This can be explained by the lack of hydrogen passivation of defects in the oxide and interface, and thus giving a smaller improvement of D_{it}, most likely originating from reduction of disorder in the oxide. Annealing in H_2 or H· gives comparable *SS* but the effective mobility is slightly higher if the annealing is performed in H_2. The hydrogen radicals are extremely reactive and are expected to react with the first atom they hit. Even though there is a directed flux of H· towards the sample surface most of the H· will probably not reach the contact area as H· but rather as H_2, which could explain the similar device performance. On the other hand the gate metal may act as a catalyst for splitting of H_2 molecules into H· [12, 17]. Therefore regardless if it is H· or H_2 reaching the contact area H· will be formed and effectively passivate defects close to the semiconductor/high-k interface. This explanation is in line with the worse performance of the PDA samples, where the lack of a gate metal leads to less H· at the semiconductor/high-k interface.

In figure 7 V_T for samples annealed in atomic hydrogen for 30 min at different temperatures is plotted and compared to samples annealed in RTP at 350 °C for 5 min in forming

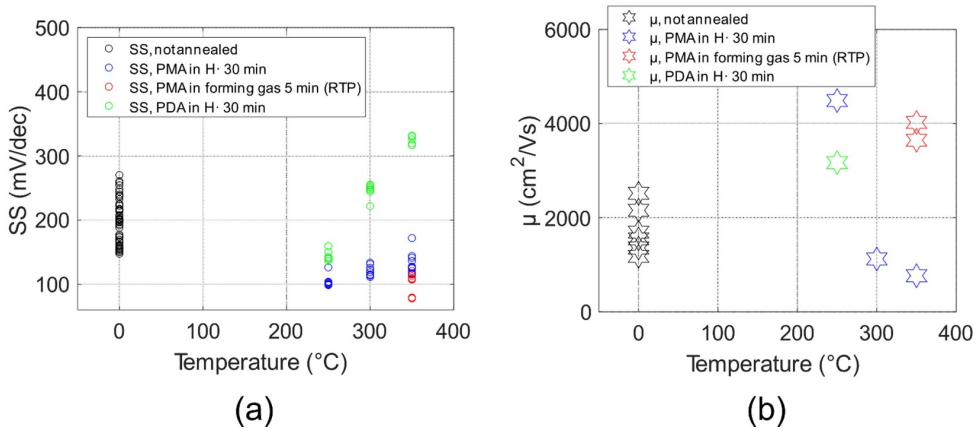

Figure 3. Minimum *SS* (a) and effective mobility (b) for samples annealed in atomic hydrogen for 30 min. A comparison to samples annealed in RTP for 5 min in forming gas as well as a comparison between PMA and PDA is also included. It is clear that PMA gives better results than PDA both in terms of *SS* and effective mobility. Above 250 °C R_{on} versus L_g is just scattered data for PDA samples which makes it impossible to extract any effective mobility. PMA for 30 min at 250 °C in atomic hydrogen gives comparable performance to RTP annealing in forming gas at 350 °C for 5 min. Above 250 °C the performance decreases with increasing annealing temperature, which could be related to diffusion at the semiconductor/high-k interface and/or crystallization of the relatively thick HfO_2.

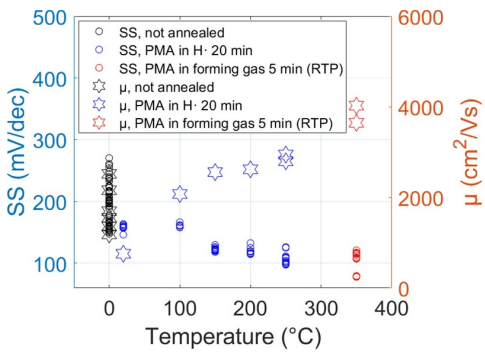

Figure 4. *SS* (circles) and effective mobility (stars) versus annealing temperature. The device performance of the AHA samples are increasing with increasing annealing temperature, and at 250 °C *SS* is comparable to *SS* of the RTP annealed samples. The effective mobility is however lower, but is comparable (even higher) if the annealing time is increased to 30 min, see figure 5.

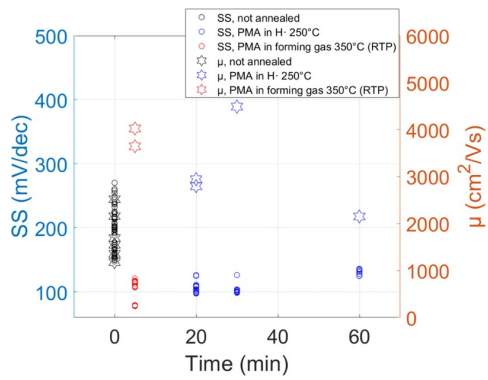

Figure 5. *SS* (circles) and effective mobility (stars) versus annealing time for samples annealed at 250 °C. For AHA samples the performance improves until 30 min annealing and then starts to degrade, which could be explained by diffusion at the semiconductor/high-k interface. After 30 min AHA the performance is comparable to RTP annealing but with even higher effective mobility.

gas. Note that the RTP samples correspond to three separate process runs clearly showing different V_T, where the encircled data corresponds to the same process run as the AHA samples. A comparison between PMA and PDA is also included. For PMA samples annealed in H·, V_T seems to decrease with decreasing annealing temperature, and in figure 8 even lower temperatures are investigated, showing a further decrease in V_T until ∼100 °C for AHA devices. Before annealing there is a big spread between devices which is reduced after annealing in H·. From figure 7 it is also evident that V_T does not increase as much for the RTP samples which could be because of the short annealing time and insufficient time for diffusion, which is in line with our investigation of different annealing times, see figure 9. Also in figure 9 the RTP samples correspond to

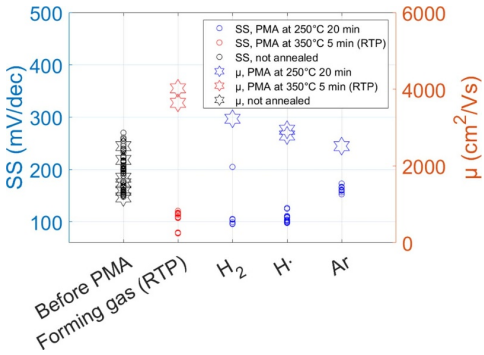

Figure 6. *SS* (circles) and effective mobility (stars) for different annealing atmospheres. It is clear that the performance is not improved as much if the annealing is performed in Ar compared to H_2 or H·. Which is because Ar is inert and will not passivate defects in the oxide and semiconductor/high-k interface. Annealing in H_2 or H· gives comparable *SS* but the effective mobility is higher if the annealing is performed in H_2.

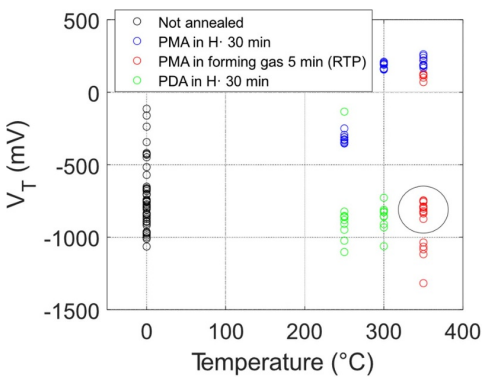

Figure 7. V_T for samples annealed in atomic hydrogen for 30 min at different temperatures is plotted and compared to samples annealed in RTP at 350 °C for 5 min in forming gas. For PMA samples annealed in H·, V_T seems to decrease with decreasing annealing temperature, which is in line with figure 8. V_T does not increase as much for the RTP samples which could be because of the short annealing time and insufficient time for diffusion. The RTP samples correspond to three separate process runs, where the encircled data corresponds to the same run as the AHA samples.

three different process runs, where the encircled data is from the same process run as the AHA samples annealed for 30 and 60 min.

In figure 10 the reliability as obtained from positive bias temperature instability measurements before and after annealing is compared. The obtained V_T shifts can be well fitted with a standard power law expression. The reliability

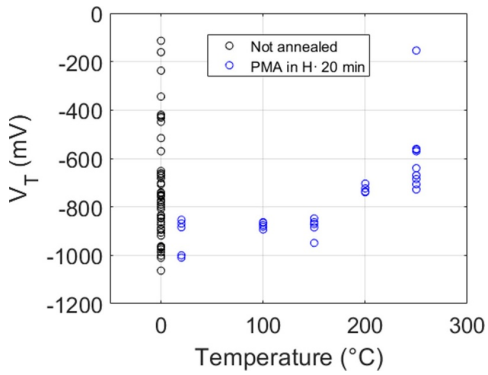

Figure 8. V_T versus temperatures is investigated, showing a decrease in V_T for decreasing annealing temperature until ∼100 °C. Before annealing there is a big spread between devices which is reduced after annealing.

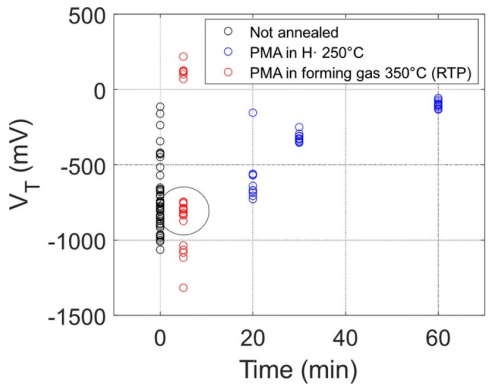

Figure 9. V_T versus annealing time for PMA samples, showing an increased V_T with increasing annealing time. The RTP data corresponds to samples from three separate process runs, where the encircled data is from the same process run as the AHA samples annealed for 30 and 60 min.

measurement is performed by holding a specific V_{ov} for 300 s and then measure the V_T shift. From the power law fits, we obtain a reduction in traps by a factor 2 after AHA at 250 °C for 20 min. Both RTP and H_2 annealing gives worse reliability, whereas the exponent is close to 2 for all anneals, indicating no major change in the defect distribution. The slightly higher exponent for the AHA sample can indicate a more peaked defect distribution.

Another indication of the quality of the oxide is the gate current, which is plotted as a function of annealing temperature in figure 11. Here the gate current is plotted as a function of annealing temperature. As long as the AHA

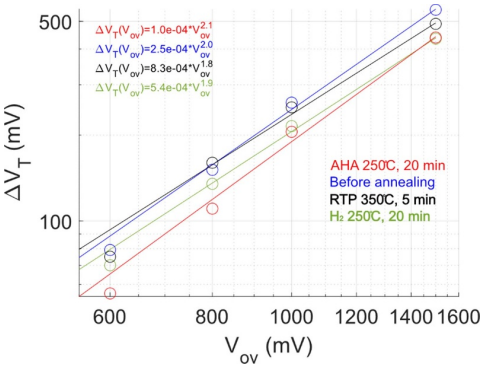

Figure 10. Reliability before and after annealing. The solid lines correspond to power law fits to the data points. The V_T shift is measured after stressing at a specific V_{ov} for 300 s. The smaller V_T shift of the AHA annealed sample indicates a 50% reduction in the defect density at the oxide and semiconductor/high-k interface. The other two annealing procedures gives slightly higher V_T shifts after annealing.

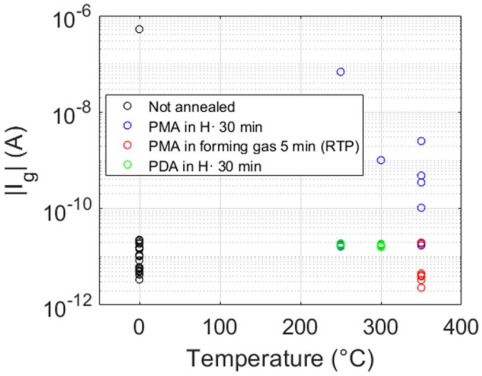

Figure 11. Gate current versus annealing temperature. The gate current is low for AHA samples annealed at 250 °C but then increases, which could be due to crystallization of the gate oxide. However, the RTP annealed samples do not show any increased gate current, which could be due to the short annealing time and the oxide will thus not have time to crystalize.

temperature is below 250 °C the gate current overlaps with the gate current measured before annealing, but above 250 °C the gate current starts to increase. This can be explained by crystallization of the gate oxide and current leakage between the crystals. The RTP annealed samples on the other hand do not show any increased gate current even though the annealing temperature is 350 °C, which could be due to the short annealing time and the oxide will thus not have time to crystalize.

4. Conclusion

We have investigated the potential of AHA as a low temperature annealing process for InGaAs MOSFETs. The device performance is greatly improved by AHA and comparable to the performance obtained after RTP annealing in forming gas. We have also confirmed that the reliability is improved and the gate current is kept low if the AHA is performed at 250 °C for 20–30 min. The performance is highest when AHA is performed at 250 °C for 30 min. If the annealing time is shortened or the annealing temperature lowered there is not sufficient time and energy for fully hydrogen passivation of defects in the oxide and semiconductor/high-k interface leading to less improvement of effective mobility and *SS*. If the temperature is above 250 °C or annealing time longer than 30 min it instead leads to a degraded interface, probably originating from diffusion at the semiconductor/high-k interface and/or crystallization of the HfO_2 leading to degraded device performance. The peak performance is obtained after AHA at 250 °C, which is 100 °C lower than if RTP annealing is performed. Thus, the use of AHA indeed results in a significant reduction of the annealing temperature while maintaining comparable device performance. This in addition to the improved reliability makes AHA an interesting treatment for future III–V integration in Si CMOS BEOL.

Data availability statement

The data that support the findings of this study are openly available at the following URL/DOI: https://doi.org/10.5281/zenodo.7590357 [18].

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Conflict of interest

The authors declare no conflict of interest.

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Paper III

Paper III

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Geometrical Magnetoresistance as a Tool for Carrier Mobility Extraction in InGaAs MOSFETs

Patrik Olausson and Erik Lind, *Member, IEEE*

***Abstract*— In this work, we for the first time show that the geometrical magnetoresistance (gMR) effect is a powerful tool for extracting the carrier mobility in diffusive InGaAs near-surface quantum well MOSFETs. The technique shows excellent agreement to Hall effect measurements, confirming its validity. In addition, the gMR approach is less time-consuming, is suitable for measurements directly on the FETs of interest, and works well even at low carrier concentrations. We investigate the temperature and gate dependence of the carrier mobility, from room temperature down to cryogenic temperatures. The peak gMR mobility for long-channel diffusive devices increases from ∼4700 cm^2/Vs at room temperature up to ∼7300 cm^2/Vs at 9.4 K. On the other hand, short-channel quasi-ballistic devices show a low gMR mobility of ∼2700 and ∼3900 cm^2/Vs at room temperature and 9.4 K, respectively. By comparing the extracted mobility from devices with different gate lengths and using quantum transport simulations, we address this drop in extracted gMR mobility to an increased degree of ballistic transport and display the limitations of the gMR method for quasi-ballistic transport.**

***Index Terms*— Ballistic, carrier concentration, cryogenic, diffusive, Hall effect, InGaAs, magnetoresistance effect, mobility, MOSFET, quantum well, threshold voltage.**

I. Introduction

THE carrier mobility is one of the most important properties of semiconductor material in field-effect transistors (FETs). Device performances, such as the high-frequency response and ON-resistance, are set by the mobility. The mobility is also important in more exotic applications, such as Majorana Fermion-based hybrid superconductor–semiconductor devices for quantum computation [1], [2].

In this article, we are investigating the geometrical magnetoresistance (gMR) effect as a tool for carrier mobility extraction. This technique has mainly been used for silicon on insulator (SOI)-MOSFETs [3], [4], [5], [6], [7], but also Si MOSFETs [8], InGaAs high-electron-mobility transistors (HEMTs) [9], graphene-based HEMTs [10], and GaN/AlGaN MOSFETs [7]. Here, we apply the gMR method for the first time on InGaAs MOSFETs.

The gMR approach has several advantages over the commonly used Hall effect measurements. For instance, it can be performed directly on the real FETs of interest, and in addition, the gMR measurements are very quick, since only one transfer measurement (I_d versus V_g) at each magnetic field is required. Another benefit of the gMR approach is that it gives reliable mobilities even at low carrier densities [3]. However, one drawback of the gMR technique is that the contact resistance is very important since it adds to the measured resistance, as well as that the standard analysis is assumed for purely diffusive transport.

II. Diffusive gMR

When a semiconductor is placed in a magnetic field, $\vec{B}$, the resistance is increased, due to the fact that the charge carriers experience the Lorentz force. The carriers will thus deviate from a straight traveling direction, giving a longer traveling distance and thus higher resistance. This effect is called the gMR effect. Due to scattering of the charge carriers, a third term within the relaxation approximation is added to the Lorentz force, which becomes

$$\vec{F} = q\vec{E} + q\vec{v} \times \vec{B} + \frac{m\vec{v}}{\tau} \tag{1}$$

where q is the charge of the charge carrier, $\vec{E}$ is the electric field, $\vec{v}$ is the velocity, m is the effective mass, and τ is the scattering time. If the device is long, a Hall voltage will build up between the edges along the traveling direction, due to the accumulation of charge carriers, but if the device is short compared to its width, the Hall voltage will be small and the ratio between the resistance without, R_0, and with, R_B, applied magnetic field becomes in the following equation [11], [12]:

$$\frac{R_B}{R_0} = \frac{\rho_B}{\rho_0}\left[1 + \left(\mu_{\mathrm{gMR}} B\right)^2 \left(1 - 0.54 L/W\right)\right] \tag{2}$$

where ρ_0 is the resistivity at zero magnetic field, ρ_B is the resistivty at magnetic field with magnitude B, μ_{gMR} is the gMR mobility, L is the length of the device, and W is the width of the device. MOSFETs have a small L/W ratio, and since the physical magnetoresistance (pMR) effect is typically

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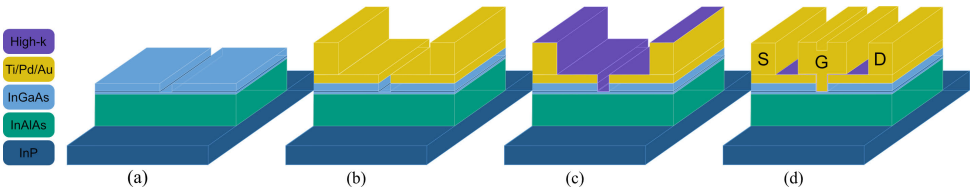

Fig. 1. Schematic of the process flow. (a) First InGaAs n+ and InP is etched in the active region, followed by mesa etching down to the InP substrate. (b) Next, source/drain electrodes are deposited followed by the deposition of the thicker source/drain measurement pads. (c) Passivation in $(NH_4)_2S{:}H_2O$ is then performed before deposition of high-k. (d) Finally, the gate pad is deposited, and high-k is etched on top of source/drain measurement pads.

small [13], the assumption $\rho_B/\rho_0 \approx 1$ is valid. Equation (2) can then be rewritten as

$$\frac{R_B}{R_0} \approx 1 + \left(\mu_{\mathrm{gMR}} B\right)^2 \tag{3}$$

from which μ_{gMR} is easily obtained by extracting the resistance from transfer characteristics at different applied magnetic fields, and fitting to (3), after removal of possible access and contact resistance.

For high mobility and short gate length devices, the near equilibrium electron transport is better described as ballistic or quasi-ballistic. In a transversal magnetic field, the cyclotron motions of the electrons will add to the formation of magnetic subbands, which will lead to a reduction in the amount of conducting modes $M(B)$, increasing the effective device resistance. For devices suitable for diffusive gMR ($W \gg L$), the complex interplay between the cyclotron radius and the source/drain reservoirs makes it complicated to derive approximative $M(B)$.

III. Method

InGaAs MOSFETs with raised n+ source and drain were fabricated. The channel consists of a composite InGaAs quantum well 3/5/4-nm-thick layers with an In composition 0.53/0.80/0.53. From eight band strain-dependent k·p modeling, the effective electron mass for the first and second subbands is $m_1^* = 0.0288m_e$ and $m_2^* = 0.0506m_e$, where m_e is the electron rest mass, and the energy separation between the first two subbands is $E_2 - E_1 = 0.1783$ eV. The nonparabolicity factor for the first subband is $\alpha = 2.2\ \mathrm{eV}^{-1}$ [14].

First, the gated area was created by electron beam lithography (EBL), followed by wet etching of InGaAs n+ and InP. Then, a mesa etch to the substrate, followed by the deposition of source/drain electrodes, was performed. Next, passivation in $(NH_4)_2S{:}H_2O$ followed by gate oxide Al_2O_3/HfO_2 (1/10 nm, 300 °C/120 °C) deposition by atomic layer deposition (ALD) was performed. The gate electrode was then deposited, followed by annealing (H_2/N_2, 5%/95%) at 350 °C for 5 min. A schematic of the process steps is shown in Fig. 1.

Devices with gate lengths, L_g, from 177 nm to 5.8 μm, and device width, $W = 63$ μm, were fabricated and characterized. The devices show good electrostatic control, with a minimum SS of 123 mV/decade at room temperature and 23 mV/decade at 14 K.

Electrical characterization of the devices was performed in a closed cycle helium refrigerator. Transfer characteristics at drain voltage, $V_{\mathrm{ds}} = 50$ mV, were measured at temperatures from 9.4 to 293 K, and magnetic fields from -1 to 1 T, applied perpendicular to the sample surface [see Fig. 2(a)]. For short-channel devices, the contact resistance, R_c, was estimated from the resistance between source and drain at high overdrive voltage, when the channel resistance, R_{ch}, is negligible. On the other hand, for long-channel devices where the channel resistance is larger, R_c was estimated from a linear fit to ON-resistance versus gate length, at an overdrive voltage, $V_{\mathrm{ov}} = 0.3$ V [see Fig. 2(b)]. The intercept at $L_g = 0$ corresponds to $2R_c + R_{\mathrm{Ballistic}}$

$$R_{\mathrm{Ballistic}} = \frac{12\,900}{W\sqrt{2\frac{n_s}{\pi}}} \tag{4}$$

where the numerator corresponds to the resistance per mode and the denominator corresponds to the number of modes as a function of carrier concentration, n_s. Fig. 2(c) shows the fitting of (3) to measured data for a device with $L_g = 2.31$ μm at 9.4 K. The effect of removing $2R_c - R_{\mathrm{Ballistic}}$ from the total resistance is clearly shown. For the long-channel device ($L_g = 2.31$) at 9.4 K and room temperature, a total resistance of 440 and 620 $\Omega\mu$m was removed from the measured resistance, respectively. The increased contact resistance at higher temperature can be explained by a decreased mobility and hence an increased sheet resistance under the ohmic metal.

For short L_g devices, we have modeled ballistic and quasi-ballistic magnetotransport using the quantum transport tight-binding-based Kwant package at $T = 0$ K [15]. Two-dimensional devices with widths of $W = 2$ μm and 10 nm $< L_g <$ 200 nm have been modeled, with magnetic fields perpendicular to the channel between 0 and 1 T. In order to model quasi-ballistic transport, random potential fluctuations have been introduced using randomly placed charges modeled by a screened Yukagawa potential along the area of the device. After calculating the increase in resistance with an applied magnetic field, we use (3) as a definition of a ballistic, $\mu_{\mathrm{gMR},b}$, and quasi-ballistic, $\mu_{\mathrm{gMR},qb}$, gMR mobility. The extracted gMR mobility will depend on the applied magnetic field at which the mobility is extracted. For 200-nm-long devices, $(d\mu/dB) = -1900$ cm^2/Vs/T and -800 cm^2/Vs/T, for ballistic and quasi-ballistic devices, respectively. We calculate the modeled ballistic and quasi-ballistic gMR mobility at an applied field of 1 T using (3).

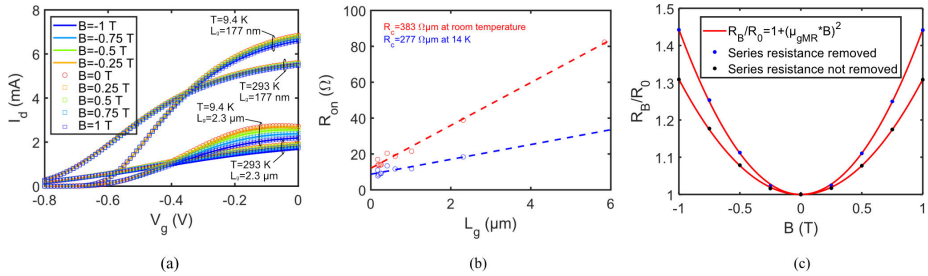

Fig. 2. (a) Transfer characteristics at $V_{ds} = 50$ mV, and applied magnetic fields from $B = -1$ T to $B = 1$ T. (b) Linear fits used to extract contact resistance for long-channel devices. Here only shown for temperatures $T = 14$ K and room temperature. (c) Fitting of (3) for a device with $L_g = 2.31$ μm at $V_g = -0.25$ V. The effect of removing the contact resistance is clearly shown.

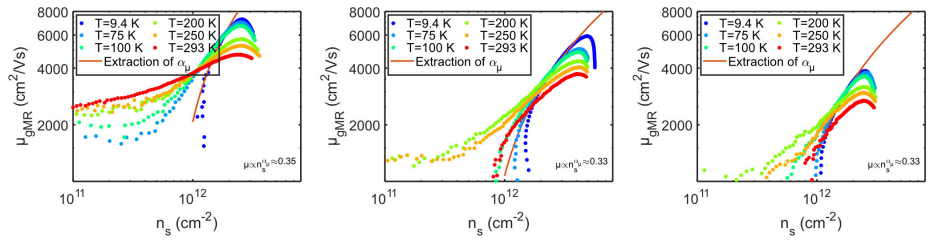

Fig. 3. Extracted μ_{gMR} as a function of n_s at different temperatures. The fit used to extract the mobility exponent, α_μ, is shown for $T = 9.4$ K. (a)–(c) correspond to $L_g = 2.31$ μm, $L_g = 408$ nm, and $L_g = 177$ nm, respectively.

IV. Result

Fig. 3 shows measured μ_{gMR} for three different gate lengths ($L_g = 2.31$ μm, $L_g = 408$ nm, and $L_g = 177$ nm) all with $W = 63$ μm, as a function of surface carrier concentration, n_s, where n_s is extracted from μ_{gMR} using

$$n_s = \frac{L_g}{Wq(R_0 - R_c)\mu_{gMR}} \tag{5}$$

where q is the elementary charge, and R_c is the contact resistance estimated from transfer characteristics, taking corrections from the ballistic resistance, $R_{Ballistic}$, into account.

μ_{gMR} follows the expected trend, increases with gate voltage at low carrier concentration, then reaches a maximum, and starts to decrease at even higher carrier concentration. This shape can be explained by the fact that the low-field mobility is primarily limited by scattering from remote impurities at low carrier concentrations [16]. This scattering mechanism will decrease when the carrier concentration increases due to screening and hence an increase in mobility, but at even higher carrier concentration, the charge carriers will come closer to the high-k/III-V interface, increasing the scattering rates. Further surface scattering and additional subband and intervalley scattering will further limit the mobility at high carrier concentration.

The peak $\mu_{gMR} \approx 4700$ cm^2/Vs at $T = 293$ K for the long-channel device [see Fig. 3(a)] and increases to $\mu_{gMR} \approx 7300$ cm^2/Vs at 9.4 K due to reduced phonon scattering. This is similar effect as for Si MOSFETs but shows a smaller increase due to the stronger scattering from charged impurities at the high-k/III-V interface. For low T, a strong decrease with carrier concentration is observed for the mobility. This effect is smaller for $T = 293$ K, due to the nondegenerate carrier statistics and phonon scattering. The nature of the dominant scattering process can be obtained from the mobility exponent, α_μ (see Fig. 3). The extracted $\alpha_\mu \approx 0.35$ to $\alpha_\mu \approx 0.33$ at 9.4 K, which indicates that Coulomb scattering from impurities close to the high-k/III-V interface is dominating for all three devices [17].

The cryogenic mobility is an order of magnitude lower as compared with InGaAs HEMT results [9], [18], [19], indicating the effect of the remote Coulomb scattering for the III–V MOSFETs.

In order to verify the long-channel gMR results, Hall measurements were performed in order to obtain the Hall mobility, μ_{Hall}. There is an excellent agreement between μ_{gMR} and μ_{Hall} (see Fig. 4) obtained at $T = 293$ K, especially at degenerate conditions, which is in line with theory [4], [20]. The discrepancy at nondegenerate conditions is expected [20] but could also be explained by the fact that gMR has the added advantage of being easily performed at low carrier densities, where Hall measurements typically become problematic. Since gMR mobility is very sensitive to the effect of contact resistance [see Fig. 2(c)], the agreement in Fig. 4 further indicates that the removal of the extrinsic contact resistance is accurate.

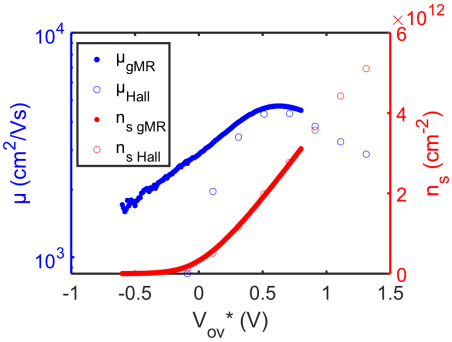

Fig. 4. Extracted mobility from gMR and Hall, showing an excellent agreement at degenerate conditions. V_{ov}^* is the overdrive from the intercept of the tangent from n_s with the gate voltage axis.

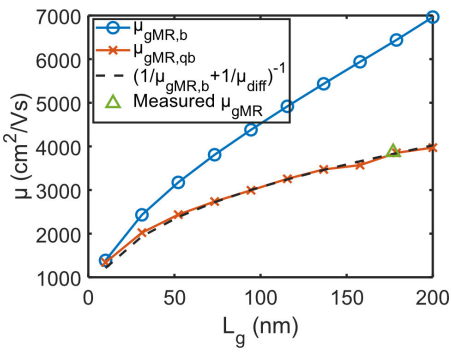

Fig. 5. Simulated $\mu_{\mathrm{gMR,b}}$ and $\mu_{\mathrm{gMR,qb}}$ as a function of L_g. The measured μ_{gMR} agrees well with the simulated $\mu_{\mathrm{gMR,qb}}$. The dashed line corresponds to the combination of simulated $\mu_{\mathrm{diff}} = 9500$ cm^2/Vs and $\mu_{\mathrm{gMR,b}}$ using Matthiessen's rule.

For short L_g devices, we observe a drop in the gMR mobility as obtained from (3) (see Fig. 3). The extracted peak mobility seems to decrease with decreasing L_g. The gMR method assumes diffusive transport, and the relaxation approximation used to obtain (3) is not entirely correct for quasi-ballistic transport. Quasi-ballistic transport may thus explain the discrepancy from the Hall mobility for the short-channel devices. In order to show this, we performed quantum transport simulations (see Fig. 5). Here, we have reproduced the measured data for the short-channel (L_g = 177 nm) device by introducing random potential fluctuations along the area of the device. By comparing the simulated quasi-ballistic magnetoresistance mobility, $\mu_{\mathrm{gMR},qb}$, to the measured peak μ_{gMR} as obtained from (3) at $T = 9.4$ K for the short-channel device (indicated by a triangle in Fig. 5), an excellent agreement is obtained. This indicates that the measured μ_{gMR} is underestimating μ_{diff} due to a crossover from diffusive to quasi-ballistic transport. The simulated ballistic magnetoresistance mobility, $\mu_{\mathrm{gMR},b}$, and

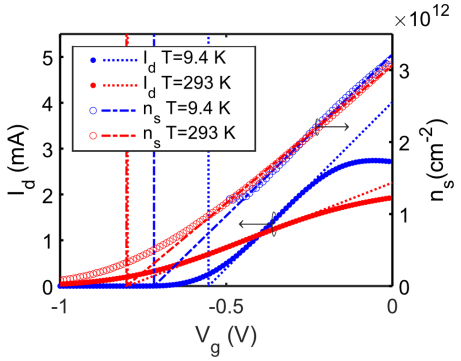

Fig. 6. Positive V_T shift occurs when the temperature is decreased. At $T = 293$ K, the intercept of the linear fit from the carrier concentration, V_T, almost coincides with, V_T^*, extracted using the linear extrapolation method, as expected for devices with constant mobility. The discrepancy at $T = 9.4$ K could be explained by a rapid mobility reduction at small V_g, and hence a larger extracted V_T^*, from the linear extrapolation method. We find that the electrostatic V_T due to the Fermi level shift and trap occupancy increases 0.083 V, and the mobility effects further increases the effective V_T^* by another 0.16 V.

the simulated, $\mu_{\mathrm{gMR},qb}$, is plotted versus L_g, for a Fermi level, $E_f = 0.2$ eV corresponding to a carrier concentration $n_s \approx 2.5 \cdot 10^{12}$ cm^{-2}, close to the long-channel peak mobility. The simulated quasi-ballistic device has a mean free path of ~360 nm (as obtained from the transmission), corresponding to a long-channel diffusive mobility $\mu_{\mathrm{diff}} = 9500$ cm^2/Vs, which is in the same range as the measured $\mu_{\mathrm{gMR}} = 7300$ cm^2/Vs for the $L_g = 2.31$-μm device. This further indicates that the measured gMR mobility for the short-channel devices underestimates μ_{diff} due to the quasi-ballistic transport of these devices. The deviation between μ_{diff} from the simulation and the measured mobility for the long-channel device can be explained by an uncertainty in the position of E_f and the fact that the simulated $\mu_{\mathrm{gMR},qb}$ depends on the applied magnetic field at which $\mu_{\mathrm{gMR},qb}$ is extracted.

One should also note that similar reduction in μ_{gMR} has been observed for short L_g Si MOSFETs [21] and is attributed to an increased effect from scattering from neutral defects. Both effects might also be present here, but the quasi-ballistic effects might be more pronounces for the high mobility channel materials. The gMR approach thus has to be used with care for quasi-ballistic transport, where the gMR method is not valid, but is a powerful tool for mobility extraction in diffusive devices. Interestingly, we empirically find that the simulated, $\mu_{\mathrm{gMR},qb}$, can be reproduced using Matthiessen's rule, combining the simulated $\mu_{\mathrm{gMR},b}$ with μ_{diff}.

As seen in Fig. 6, a positive threshold voltage, V_T, shift, as extrapolated from the sheet carrier concentration, of around 0.083 V occurs when the temperature is decreased from $T = 293$ K to $T = 9.4$ K. This could be explained by a shift of the temperature-dependent Fermi level. An interesting feature of the remote Coulomb scattering limited mobility is that it will lead to a discrepancy between the electrostatically defined threshold voltage, V_T, obtained from the intercept of the linear

fit from the carrier concentration, and the apparent threshold voltage, V_T^*, obtained from conductance measurements using the linear extrapolation method. This is shown in Fig. 6 for the device measured in Fig. 3(a). At room temperature, V_T^* obtained from conductance measurements using the linear extrapolation method is almost the same as V_T obtained from the intercept of the linear fit from the carrier concentration, as expected for constant mobility devices. It only differs 0.0036 V. On the other hand, at $T = 9.4$ K, V_T^* is 0.16 V larger than V_T. This difference is induced by the reduced mobility with decreasing carrier concentration, which is much more prominent at low temperatures (see Fig. 3). The lower mobility at small gate bias and low temperature will in turn give a reduced current and an apparent larger threshold voltage, V_T^*.

From the slope of the linear fit to the carrier concentration, the extracted gate capacitance, $C_{\rm gg}$, is $C_{\rm gg} = 0.61$ μF/cm^2 and $C_{\rm gg} = 0.72$ μF/cm^2 for 293 and 9.4 K, respectively. These values agree well with a calculated room temperature $C_{\rm gg} = 0.66$ μF/cm^2 obtained from reference C–V measurements [22], including the effect from channel quantum capacitance (using the effective mass obtained from k·p modeling [14]) and the centroid capacitance.

V. Conclusion

In this article, we for the first time show that the gMR effect is a powerful tool for extracting the carrier mobility in diffusive InGaAs MOSFETs. We extract the gMR mobility from a diffusive device at several temperatures and confirm its validity by comparing it to the mobility extracted from Hall effect measurements. We also extract the gMR mobility from short-channel quasi-ballistic devices, which show considerably lower $\mu_{\rm gMR}$ compared to the diffusive device. This apparent drop in the mobility seems to increase with decreased L_g, and we address this to an increased degree of ballistic transport. By simulations of ballistic and quasi-ballistic magnetotransport using the quantum transport tight-binding-based Kwant package, we show the limitations of the gMR method when applied on nondiffusive devices. The gMR mobility obtained from quasi-ballistic devices is lower than the diffusive mobility. The diffusive mobility can, however, be estimated from simulated $\mu_{{\rm gMR},b}$ and measured $\mu_{\rm gMR}$

$$\mu_{\rm diff} = \left(\frac{1}{\mu_{\rm gMR}} - \frac{1}{\mu_{{\rm gMR},b}}\right)^{-1}. \tag{6}$$

Care must be taken when using (6) since the estimated diffusive mobility depends strongly on the Fermi-level position used in the simulations.

We have also shown and explained the origin of an apparent larger V_T^* at low temperatures when obtained using extrapolation from conductance measurements, compared to V_T obtained from the carrier concentration. The larger V_T^* is related to the rapid mobility reduction with decreased carrier concentration and in turn reduced current at small gate bias.

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Paper IV

Paper IV

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Cryogenic Characteristics of InGaAs MOSFET

L. Södergren, P. Olausson, and E. Lind, *Member, IEEE*

***Abstract*— We present an investigation of the temperature dependence of the current characteristic of a long-channel InGaAs quantum well MOSFET. A model is developed, which includes the effects of band tail states, electron concentration-dependent mobility, and interface trap density to accurately explain the measured data over all modes of operation. The increased effect of remote impurity scattering is associated with mobility degradation in the subthreshold region. The device has been characterized down to 13 K, with a minimum inverse subthreshold slope of 8 mV/dec and a maximum ON-state mobility of 6700 $cm^2/V{\cdot}s$ and with values of 75 mV/dec and 3000 $cm^2/V{\cdot}s$ at room temperature.**

***Index Terms*— Band tail, charge carrier mobility, cryogenic electronics, InGaAs, MOSFETs.**

I. Introduction

CRYOGENIC electronics are of interest in applications, such as control circuits in quantum computing and space applications. In a typical modern quantum computer, the bias and control electronics are separated from the qubits since they operate at room temperature. In order to scale up a quantum computer to a higher number of qubits, there is a need to integrate the classical devices and the qubits to both be inside the cryostat. This is useful to reduce the number of connections needed into the cryostat; the benefits also include the reduction of thermal noise and signal distortion. In order to improve the understanding of MOSFETs operating at cryogenic temperatures, we have in this article characterized long-channel InGaAs MOSFETs, which exhibits high electron mobility. We have characterized the device down to 13 K, where we see a saturation of the subthreshold swing, which deviates from Boltzmann statistics. We present a model that utilizes a band tail parameter in the form of an effective lattice temperature, interface trap density, and an electron concentration-dependent mobility to accurately capture the current characteristics in both depletion and accumulation over a wide temperature range.

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II. Device Fabrication

The device fabrication starts with MOVPE growth of a thin film of 13-nm $In_{0.69}Ga_{0.31}$ As on a (100) InP:Fe substrate. The substrate is cleaned in 0.05% HF just before growth. After growth, the devices are isolated by a wet etch in H_3PO_4:H_2O_2:H_2O (1:1:25) followed by a short dip in HCl:H_2O (1:1) to etch 16 nm in to the InP substrate. Source and drain contacts consisting of Ti/Pd/Au (5/5/200 nm) are then placed using a UV lithography liftoff process and electron-beam evaporation. Just prior to evaporation, the native oxide removal is performed by a short dip in HCl:H_2O (1:20). This facilitates a good interface with the metal, creating low resistive ohmic contacts. A bilayer gate oxide consisting of Al_2O_3/HfO_2 (7/100 cycles) is then deposited using atomic layer deposition (ALD) at 300 °C and 120 °C. The subsequent step is the gate metal deposition of Ti/Pd/Au (5/5/200 nm) using UV lithography liftoff and electron-beam evaporation. The device is finalized by a post metal anneal at 350 °C in a H_2/N_2 (5%/95%) mixture for 5 min. Fig. 1 shows a schematic of the finished device and a top-view scanning electron microscope (SEM) image.

III. Device Modeling and Measurements

To compute the current characteristics, a 2-D transport model, including band tail states, defect interface trap density, and electron density-dependent mobility, was used. In order to calculate the current for degenerate systems at low temperatures, we utilize that the isothermal diffusive current is given by the gradient of the quasi-fermi level E_{Fn} as

$$J_D = n_s \mu_n \frac{dE_{\mathrm{Fn}}}{dx} \tag{1}$$

where n_s is the sheet electron concentration and μ_n is the electron mobility, which is valid for arbitrary temperatures and band structures [1], [2], [3]. The electron transport is along the x-direction and the total channel length is L. Using the gradual channel approximation and integrating over the length of the channel give

$$J_D = \frac{1}{L}\int_0^{qV_{\mathrm{DS}}} n_s(E_F)\mu(n_s(E_{\mathrm{Fn}}))dE_{\mathrm{Fn}} \tag{2}$$

where the mobility is approximated, as shown in Fig. 2. For these surface channel devices, the low-field mobility is mainly limited by scattering from remote impurities and the InGaAs high-k interface, as such we model the mobility as

$$\mu^{-1} = k_1 n_s^{-\gamma_1} + k_2 n_s^{\gamma_2} + \mu_0^{-1}. \tag{3}$$

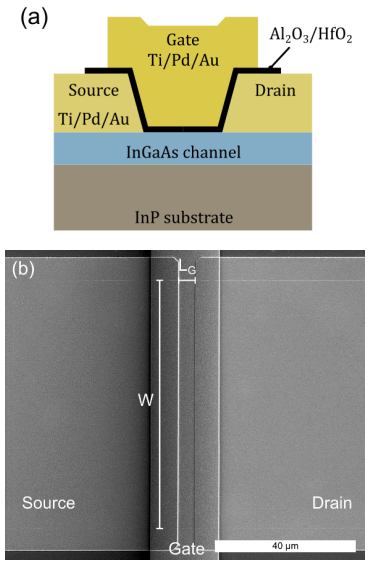

Fig. 1. (a) Schematic of the MOSFET. (b) Scanning tunneling microscopy image of the finished device.

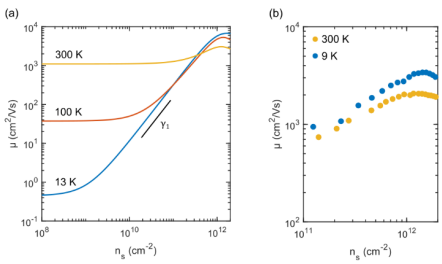

Fig. 2. (a) Simulated electron mobility as a function of sheet carrier concentration. The curves are fit to match the experimental data. (b) Measured Hall mobility obtained at 9 and 300 K.

With $\gamma_1 \approx 1.5$ for remote Coulomb scattering [4], γ_2 term takes the effect of the vertical field of mobility into account. For nondegenerate carriers, the scattering becomes essentially independent of the carrier concentration [3], [5], which is modeled by the μ_0 term. For low temperatures, the k_1/γ_1 term is dominating, and we expect to see a large increase in mobility with increasing n_s, which is also observed for high-purity 2-DEGs. This behavior has also been observed by Hall measurements on InGaAs MOSFETs [6].

As seen in Fig. 2(a), the fit peak mobility is 6700, 5300, and 3000 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ for 13, 100, and 300 K, respectively, with $\gamma_1 \approx 1.45$, 1.36, and 1.17. To verify the fit mobility model, gated Hall measurements on large area Hall bars have been performed, and the measured Hall mobility is shown in Fig. 2(b). Reasonable agreement is obtained, with peak $\mu_H = 3100\ \mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ and $\mu_H = 2100\ \mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ for $T_L = 9$ and 300 K, respectively.

Band tails or Urbach tails are localized states inside the bandgap induced by disorder in the crystal. These states play an important role in the subthreshold transport, especially at cryogenic temperatures, and will limit the lowest achievable inverse subthreshold slope. We use an empirical extension of the density of states to account for 2-D band tail states exponentially decaying into the bandgap [7]

$$D_{2\text{-D},E0}(E) = \frac{m^*}{\pi\hbar^2}\mathcal{F}_{-1}\left(\frac{E-E_c}{E_0}\right). \tag{4}$$

The sheet carrier concentration is then calculated using

$$\begin{aligned} n_s(E_F) &= \int D_{2\text{-D},E_0}(E)\, f_0(E, E_{\mathrm{Fn}}, T_L)\, dE \\ &\approx \frac{m^* k_B T_{\mathrm{eff}}}{\pi\hbar^2}\mathcal{F}_0\left(\frac{E_F - E_c}{k_B T_{\mathrm{eff}}}\right). \end{aligned} \tag{5}$$

The generalized Fermi–Dirac integrals of order -1 and 0 are approximated by $\mathcal{F}_0(\eta_F) = \ln(1+e^{\eta_F})$ and $\mathcal{F}_{-1}(\eta_F) = 1/(1+e^{-\eta_F})$, respectively, m^* is the effective mass, f_0 is the Fermi–Dirac distribution, T_L is the lattice temperature, and E_c is the subband edge. In the second step in (5), in order to avoid having to integrate numerically, we replace the lattice temperature with an effective temperature, taking both the effect of the band tails (E_0) and the lattice temperature. The effective temperature, defined as a simple average, $T_{\mathrm{eff}} = \left(T_0^\alpha + T_L^\alpha\right)^{1/\alpha}$. For the best fit, we find $\alpha = 5$. The critical temperature $T_0 = E_0/k_B$, where E_0 is the band tail parameter.

T_{eff} is equal to the actual lattice temperature at high temperatures and will saturate at T_0 at cryogenic temperatures. This is because, at high T_L, the nondegenerate statistics is set by thermal broadening, leading to statistics set by the lattice temperature. At low T_L, the Fermi–Dirac distribution becomes a step function, so the subthreshold statistics is set by the effect of the band tails. At degenerate conditions, (5) becomes independent of temperature.

The electron concentration calculated by numerically solving the integral and by using the approximative expression in (5) is plotted in Fig. 3(a). The approximation works well at high electron concentrations, due to the temperature-independent degenerate statistics. However, at lower electron concentrations, there is a small error (<10%) when T is far from T_0 and a maximum error of roughly a factor of 2 when $T = T_0$, as highlighted in Fig. 3(b). Equation (5) with T_{eff} gives a simple physical explanation of the effect of tails on the carrier statistics and can be used with reasonable accuracy for calculations. Using standard 1-D MOS electrostatics suitable for long-channel devices, the surface potential ψ_s is related to the gate voltage by

$$V_{gs} = \psi_s + \frac{q n_s(E_{\mathrm{F_n}})}{C_{\mathrm{ox}}} + \frac{q}{C_{\mathrm{ox}}}\int_{E_{F_n}}^{+\infty} D_{\mathrm{it}}(E)\, dE. \tag{6}$$

Here, the interface trap density is included as an additional capacitance $C_{\mathrm{it}} = q^2 D_{\mathrm{it}}(E)$. The sheet electron concentration

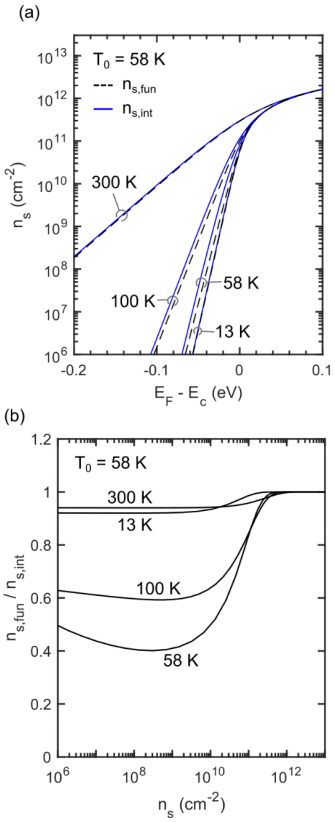

Fig. 3. (a) Electron concentration calculated from the approximative function in (5) and from numerically solving the complete integral. (b) Ratio $n_{s,\mathrm{fun}}/n_{s,\mathrm{int}}$ as a function of electron concentration.

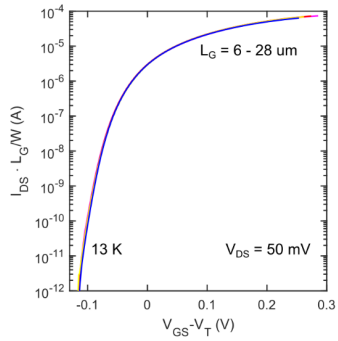

Fig. 4. Measured normalized transfer characteristics at 13 K for $L_G = 6$–28 μm and $V_{DS} = 50$ mV.

in relation to the gate bias is then found by self-consistently solving (5) and (6).

Measurements were performed on long-channel InGaAs MOSFETs with $L_G = 6$–28 μm, $W = 70$ μm, and a channel thickness of 13 nm. Devices with different L_G values show very similar behavior at all temperatures when normalizing with L_G for the same gate voltage overdrive, indicating reproducible data and negligible effect from parasitic resistances, as shown in Fig. 4. The long-channel devices give a well-defined mobility, small effect from contact resistances and can be well modeled using 1-D statistics. For short-channel devices, the modified statistics (5) should still apply, but (2) should for high mobility channels instead be solved using a quasi-ballistic model.

Fig. 5 shows the transfer characteristics for a $L_G = 28$ μm device at three different temperatures, 13, 100, and 300 K. The model can greatly reproduce the data. The model is fit by first considering the capacitance obtained at 13 K, as shown in Fig. 6. The slope of the onset of the capacitance is used to find the threshold voltage and band tail parameter, $E_0 = 5$ meV, which is assumed to be temperature independent. At these low temperatures and when the Fermi energy is close to the conduction band edge, the interface traps are assumed to only have a very small impact on the capacitance.

However, the capacitance does not fit very well in the ON-state due to parasitic overlap capacitances included in the measurement, as well as omission of nonparabolicity and charge centroid variation with n_s in the model [7]. The ON-state current level and the transition to the OFF-state measured at $V_{\mathrm{DS}} = 50$ mV are fit by the electron concentration-dependent mobility. In order to obtain the amount of interface traps, the $T_L = 300$ K subthreshold regions are fit assuming and an exponentially increasing D_{it} toward the valence band is introduced as $D_{\mathrm{it}} = 8.7 \times 10^{11} e^{-7.8(E-E_C)}$ cm^{-2}·eV^{-1}, which is used to correctly fit the data. The same D_{it} is then found to also reproduce the $T_L = 100$ K and $T_L = 13$ K data. As shown in Fig. 5(b), the model can also reproduce the data obtained in the saturation region at $V_{\mathrm{DS}} = 500$ mV without changing any fitting parameters. The drain bias dependence is captured by the integral limits in (2).

In subthreshold, there are several effects impacting the current. First, the band tail states, which the electrons can transfer through, will increase the current at a given voltage. Second, oxide defects such as interface traps or border traps, in this article, modeled as D_{it}, will reduce the current in two ways. First, charging/discharging the traps will act as a capacitor in parallel with the quantum capacitance and lower the gate effectiveness. Second, the traps are charged defects situated close to the channel and will act as scattering centers for the conducting electrons, and this reduces the electrons' effective mobility. The defects will also impact the energy profile along the channel, creating fluctuations in the conduction band edge [8]. This will reduce the transmission of the channel, especially close to (and below) V_T when the Fermi energy is close to the band edge. These effects introduce a carrier concentration dependence on electron mobility. At low

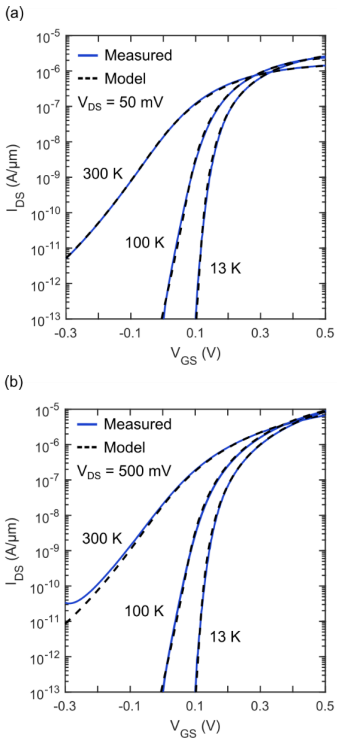

Fig. 5. Measured transfer characteristics at 13, 100, and 300 K together with the fit model with (a) $V_{DS} = 50$ mV and (b) $V_{DS} = 500$ mV.

gate bias, when the carrier concentration is low, the remote impurity scattering will be strong due to the reduced screening effect. The conducting electrons will also be close (in energy) to the conduction band edge fluctuations further reducing the effective mobility. Increase the gate bias, as the electron concentration is increased and so is the mobility. At high gate bias, the electron wave function will be shifted toward the semiconductor/oxide interface and the interaction with the remote scattering centers will increase, reducing the mobility. Similar mobility behavior can also be due to the population of higher effective mass valleys or scattering with the second subband [9], [10]. This behavior is captured in (3).

Note that, in the current calculated from (2), the mobility is dependent on $n_s(E_{Fn})$. Since E_{Fn} is decreasing toward the drain when $V_{DS} > 0$, a dependence of the position x along the channel is introduced. With large applied V_{DS}, the mobility at the drain side of the channel will be reduced due to the decreased electron concentration. An alternative way to compute the current is to let

$$J_D = \frac{\mu_n(n_s)}{L} \int_0^{qV_{DS}} n_s(E_{Fn}) dE_{Fn} \tag{7}$$

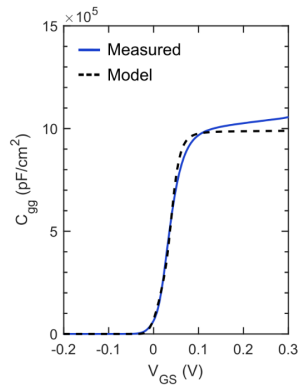

Fig. 6. Measured and simulated capacitance–voltage characteristics at 13 K.

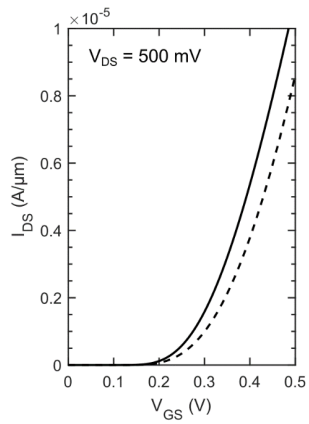

Fig. 7. Calculated drain current using (5) (dashed line) and (7) (solid line) with $V_{DS} = 500$ mV.

where the mobility is the source side mobility independent of the channel position. This is the mobility, which is usually extracted from ON-resistance measurements at low V_{DS}. In Fig. 7, the current at $V_{DS} = 500$ mV calculated using the two methods is shown. We see that using the source side or low-field mobility will overestimate the current in saturation. This is because, in a more realistic picture, the mobility will degrade at the high field/low electron concentration region close to the drain.

For room temperature operation, the inverse subthreshold slope for the device will behave close to a standard MOSFET since the effect of band tails is insignificant, and the nondegenerate mobility is essentially constant along the channel. However, the small drop in μ_n with n_s can potentially lead to a subthreshold swing, which potentially can go below

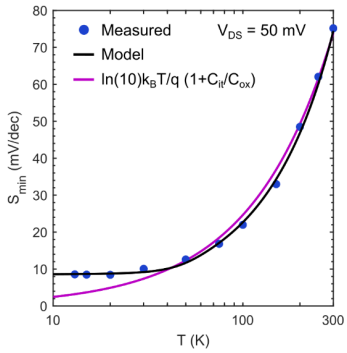

Fig. 8. Measured and simulated temperature dependence of the minimum subthreshold swing.

60 mV/decade, as also recently pointed out in [11]. At low temperatures, deviations will be observed due to the effect from the band tails and mobility degradation. Also, for the typical example of increasing D_{it} toward the valence band, we expect to see a decrease in the slope since the subthreshold regime occurs close to the conduction band edge for lower temperatures.

The measured minimum subthreshold swing from room temperature down to 13 K is shown in Fig. 8 together with fit simple models. A low minimum swing of 8 mV/decade is found. The standard expression for a quantum well thermionic device gives that exponential gate voltage dependence of the drain current is described by

$$S = \frac{k_B T_L}{q} \ln(10)\left(1 + \frac{C_{\text{it}} + C_q}{C_{\text{ox}}}\right) \tag{8}$$

where $C_{\text{it}} = q^2 D_{\text{it}}$ describes the capacitance due to the interface traps and C_q is the quantum capacitance. In subthreshold, C_q is exponentially suppressed and can be approximated as 0. To obtain the correct inverse subthreshold slope at room temperature, $D_{\text{it}} = 2 \times 10^{12}$ cm^{-2}·eV^{-1} was used. We observe that the measured swing deviates from (8) at both high and low T_L.

Below the critical temperature ($T_0 = E_0/k_B = 58$ K), the subthreshold swing starts to deviate from the value predicted by the Boltzmann statistics. This is because the localized band tail states allow the electrons to be transported through the channel, increasing the current, which is captured by the use of T_{eff} instead of T_L. Using only $T_0 = 58$ K would give a minimum swing of 11.5 mV/decade assuming no D_{it}, which is higher than the measured swing of 8 mV/decade. However, the carrier-dependent mobility for low T_L will lead to a reduction in the current with n_s, leading to a lower subthreshold swing. The subthreshold swing will saturate at a value depending on the band tail parameter E_0, D_{it}, and the OFF-state mobility. To include these effects in a simple way, (8) is modified to

$$S = \frac{k_B T_{\text{eff}}}{q(1 + \gamma_1(T))} \ln(10)\left(1 + \frac{C_{\text{it}}(T)}{C_{\text{ox}}}\right). \tag{9}$$

The factor γ_1 [from (3)] describes the electron concentration dependence of the mobility at the bias point of minimum subthreshold swing. For high T ($T > 100$ K), we observe a faster reduction on the measured slope as compared with the standard expression, which mainly can be attributed to a reduction in the effective D_{it}, whereas the mobility degradation factor stays fairly small. For low T (< 50 K), the slope is essentially set by the band tail limiting T_{eff} to around 60 K, as well as the mobility degradation, which helps in decreasing the minimum slope. For low T, the effective D_{it} also stays approximately constant. The effect of improvement in the slope due to mobility degradation was also pointed out recently in [11].

IV. Conclusion

In summary, we have fabricated long-channel InGaAs quantum well MOSFETs and characterized them down to 13 K. A 2-D transport model is presented, which can describe the behavior over a wide temperature range and all modes of operation. The model includes the effects of band tails, interface traps, and electron concentration-dependent mobility. We show how the band tails can be incorporated as an effective temperature for calculating the sheet charge. Understanding the interplay between the band tails, interface traps, and the mobility is important to accurately model MOSFETs operating at cryogenic temperatures.

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Paper V

Paper V

L. Södergren, P. Olausson, and E. Lind, "Low-Temperature Characteristics of Nanowire Network Demultiplexer for Qubit Biasing," *Nano Letters*, vol. 22, no. 10, pp. 3884-3888, May 2022, doi: 10.1021/acs.nanolett.1c04971.

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Letter

Low-Temperature Characteristics of Nanowire Network Demultiplexer for Qubit Biasing

Lasse Södergren,* Patrik Olausson, and Erik Lind

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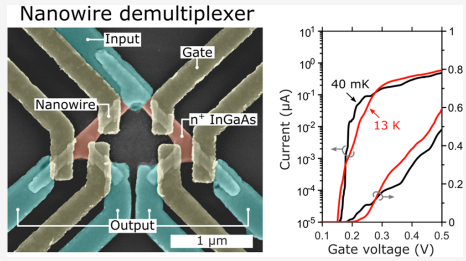
ABSTRACT: In current quantum computers, most qubit control electronics are connected to the qubit chip inside the cryostat by cables at room temperature. This poses a challenge when scaling the quantum chip to an increasing number of qubits. We present a lateral nanowire network 1-to-4 demultiplexer design fabricated by selective area grown InGaAs on InP, suitable for on chip routing of DC current for qubit biasing. We have characterized the device at cryogenic temperatures, and at 40 mK the device exhibits a minimum inverse subthreshold slope of 2 mV/dec, which is encouraging for low power operation. At low drain bias, the transmission breaks up into several resonance peaks due to a rough conduction band edge; this is qualitatively explained by a simple model based on a 1D real space tight-binding nonequilibrium Green's functions model.

KEYWORDS: *nanowire, multiplexer, InGaAs, cryogenic*



In current quantum computers, most low frequency bias, high frequency readout, and control electronics are generated at room temperature and connected with cables to the qubit chip at low temperatures. However, as quantum computers are scaled to a large number of qubits, the number of input/output (I/O) connections of the cryostat becomes unmanageable.[1−4] By moving some of these circuits into the cryostat and operating them at cryogenic temperatures the amount of I/O needed can be reduced significantly. Therefore, there is a need for an increased effort in characterization of low-temperature electronics which are designed to operate at the low-temperature stages in scaled quantum computers. One circuit element of interest is the demultiplexing device for individually biasing many qubits with few input signals. Different kind of qubits such as transmons, spin qubits, or Majorana-based qubits all need current/voltage for biasing or control.[5−9] For example, transmons need a biasing magnetic field provided by a current in close proximity on the qubit chip. Apart from the standard CMOS-implementation, multiplexing structures have also been demonstrated before in both III−V modulation doped quantum well devices[1] and Si nanowires.[10] In this paper, we have built a 1-to-4 demultiplexer (demux) proof of concept device based on a selective area grown lateral InGaAs nanowire network on InP with current control through gates coupled to the channel using high-κ oxide. Such a device can allow for highly scaled routing of bias currents/voltages, while operating under low power constraints due to a high on/off ratio and low on-resistance. The higher electron mobility and lower effective mass of the InGaAs nanowires compared to Si enables operation with lower drive voltage, which reduces the power dissipation, which is important for mK cryogenic operation where the cooling power is limited.[3] On-chip (de)multiplexing devices can also be used to obtain statistics for wire-bonded devices operated in dilution fridges, where the device pin count can be limited.[11] The device characteristics have been measured down to 40 mK. At cryogenic temperature the low inverse subthreshold slope allows the device to be efficiently turned off, minimizing the leakage currents. Operation of the fabricated devices at frequencies relevant for qubit control (∼1−5 GHz) requires some further considerations. The individual InGaAs nanowire transistors can be operated at high frequencies by utilizing a T-gate design which reduces parasitic capacitances and small gate lengths enabling a high transconductance.[12] Considerations regarding the (de)multiplexer gate design also must be done to limit the capacitive leakage through the gates at the operating frequency.

A demultiplexer is a simple circuit which is able to deliver an input signal to one of many outputs. Figure 1a shows a

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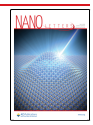

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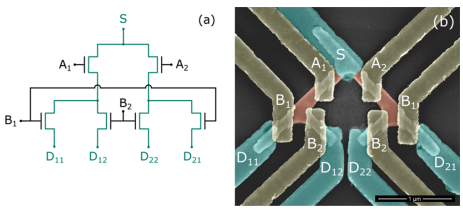

Figure 1. (a) A 1-to-4 demultiplexer circuit schematic with one input (S), four outputs (D) and four control gates (A, B). (b) False-colored scanning electron microscope (SEM) image of a demultiplexer. Source/drain contacts in blue, doped InGaAs in red, and gate contacts in yellow. The device has in total four different gates, A_1, A_2, B_1, and B_2, since the respective B gates are shorted (not shown). The unintentionally doped InGaAs channel, which can be seen under the gates have dimensions of W = 80 nm and L_G = 120 nm.

schematic of a 1-to-4 demultiplexer; this network has one input at the source contact and four outputs at the drains. The gates (A, B) are used for controlling which drain the signal reaches. This type of network is very scalable, each added layer doubles the number of outputs while only requiring two more control signals, a 1:2^n multiplexer requires 2n control gates. Thus, the fabricated nanowire demultiplexing network shown in Figure 1b has four control gates (A_1, A_2, B_1, B_2) and four outputs drains (D_{11}, D_{12}, D_{21}, D_{22}). The proposed technology can be used to implement multiplexers with bigger fan-out (n > 2); this however requires a back-end-of-line technology for routing some of the gate wires as they need to cross some internal electrodes.[1]

The lateral InGaAs nanowire network was fabricated on a semi-insulating InP:Fe (100) substrate by selective area epitaxy (SAE) using a metal organic vapor phase epitaxy (MOVPE) system. Figure 2 illustrates the fabrication process. Hydrogen

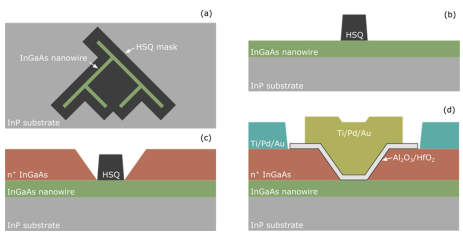

Figure 2. Simplified schematics of the fabrication steps for one gated region. (a) The InGaAs nanowire network is grown using selective area epitaxy with HSQ as a growth mask on an InP substrate. (b) An EBL defined HSQ dummy gate patterned across the nanowire. (c) Highly doped n$^+$ InGaAs contacts are grown. (d) Final device structure after dummy gate removal, gate oxide deposition, and metallization steps.

silesquioxane (HSQ) patterned by an electron beam lithography (EBL) system was used as a growth mask. The mask openings were 80 nm wide and aligned to ⟨001⟩. This leads to nanowires defined by {110} facet sidewalls and (100) top surface, which limits the overgrowth of the mask.[13] The sample was cleaned in 0.05% HF solution just prior to the first growth step consisting of 4 nm InP followed by 13 nm $In_{0.65}Ga_{0.35}As$ grown at 600 °C. The increased indium content relative to the lattice matched (53% indium) gives a crystal with increased electron mobility, simultaneously the thickness of 13 nm InGaAs is not sufficient for relaxation to occur. Buffered oxide etch (BOE) was used to remove the HSQ mask before dummy gate HSQ lines were patterned along the (110) direction, defining the gate length of 120 nm. In the second growth step, 25 nm of doped $In_{0.65}Ga_{0.35}As$ ($N_D \approx 5 \times 10^{19}$ cm^{-3}) contact layer was grown, which is sufficient to create a good contact with source/drain metal. After the HSQ was removed by BOE, a HSQ etch mask was patterned, outlining the mesa. Mesa isolation was done by wet etching the grown InGaAs using $H_3PO_4/H_2O_2/H_2O$ followed by a short HCl/H_2O dip, etching 16 nm into the substrate. Plasma-enhanced chemical vapor deposition (PECVD) was used to deposit 14 nm of SiN_x before removing the HSQ with BOE, leaving SiN_x everywhere on the sample surface except the active device area. This ensures proper isolation between measurement pads. The surface of the sample is etched by ozone oxidation followed by diluted HCl. An EBL lift-off process and electron beam evaporation of Ti/Pd/Au was used to fabricate the source and drain contacts. Next, the surface was passivated by ozone cleaning and 20 min in $(NH4)_2S$ (10% solution in water) before deposition of Al_2O_3/HfO_2 gate oxide (7/100 cycles) at 300/120 °C. The device is completed by gate definition by evaporation of Ti/Pd/Au using a lift-off process followed by a forming gas (H_2/N_2, 5/95%) annealed at 300 °C. The implemented structure thus allows routing of a current between input and output and avoids losses due to ohmic contacts within the structure. Other circuit elements, such as MOSFETs, varactors, and MIM-capacitors, can also be implemented within this material platform.

The typical transfer characteristics at V_{DS} = 50 mV and 500 mV of a W = 80 nm and L_G = 120 nm demux device are presented in Figure 3. The measurements were done at 13 K by first simultaneously applying a constant drain bias to all of the drains; then, the current was sequentially routed to the respective drain. This was done by setting the respective gate A at a constant high voltage (~800 mV), making sure the

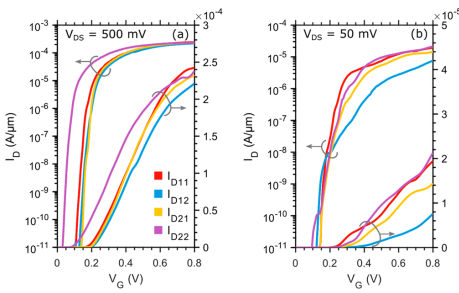

Figure 3. Low-temperature transfer characteristics normalized to the nanowire width at (a) V_{DS} = 500 mV and (b) V_{DS} = 50 mV measured at 13 K. The different colored lines refer to the drain current in each respective drain, as indicated in Figure 1. During the measurements, the drain bias was applied to all drains simultaneously, and the gates were then used to only set one source-drain path in a low resistive state at any given time. The current in the high resistive paths were below the noise floor of the measurement setup (<1 pA).

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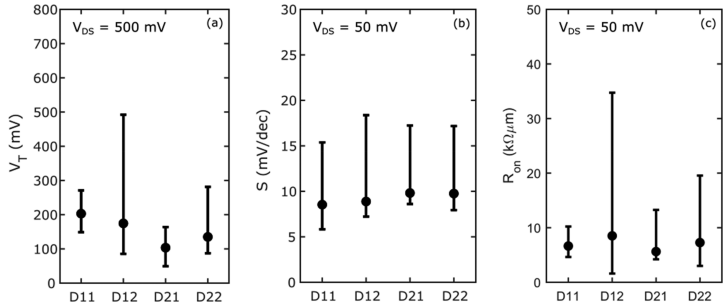

Figure 4. Extracted (a) threshold voltage, (b) minimum inverse subthreshold slope, and (c) on-resistance for different drain connections, measured on eight multiplexers at 13 K. The filled circles are the median value of each drain, and the bars show the 95% confidence interval.

channel is in the on-state, then sweeping the voltage of the respective gate B. The two other gates are set in the off state. Doing the reverse, sweeping gate A while gate B is at a high voltage, yields similar characteristics. For example, to route the current between S and D_{11}, gate A_1 and B_1 are turned on while gate A_2 and B_2 are turned off. All gate currents and the drain currents in the turned off paths are measured simultaneously to be below the noise floor of the measurement setup (<1 pA), demonstrating demultiplexing functionality. This demonstrates a well-behaved device with a very small gate leakage and good isolation between all gates and drains. The small signal transconductance of the devices with respect to a single gate is $g_m \approx 0.6$ mS/μm.

Statistics of device threshold voltages, minimum inverse subthreshold slopes, and on-resistances from several different devices are shown in Figure 4. The data is extracted from 8 demux devices, which essentially is equivalent to 32 available current paths, since there should be no difference between the 4 drains. The difference in the median threshold voltage is within 100 mV between the four drains. The total median minimum inverse subthreshold slope of all current paths is below 10 mV/dec, showing a good control of the channel electrostatics. The on-resistance is extracted at 300 mV above V_T with a total median of 6800 Ωμm. Measurements on similar samples show that the metal/semiconductor contact resistance R_C = 20 Ωμm, and the access resistance through the doped n+ InGaAs layer R_A = 30 Ωμm are both reasonably low. This suggests there is some additional series resistance in the structure, most likely originating from the interface between the undoped InGaAs channel and the doped n+ InGaAs layer. Although the statistics are limited, this data indicates a high process yield with all demultiplexers operational. Only one source-drain current path exhibits high V_T and R_{on}, resulting in an effective yield of over 95%.

Figure 5a compares the transfer characteristics at 13 K and 40 mK of the D_{11} current. For this specific drain, the minimum inverse subthreshold slope is 130, 6, and 2 mV/dec at 300 K, 13 K, and 40 mK, respectively. At cryogenic temperatures, the source/drain thermal energy is extremely sharp (kT = 3 μeV at 40 mK), potential fluctuations leading to 1D resonant tunneling type of behavior will lead to transmission resonances, which can enhance the subthreshold slope even for very low temperatures. This is in contrast to 2D type of devices, where averaging will lead to current limited by exponential band tails.[14−16] At cryogenic temperatures the inverse subthreshold

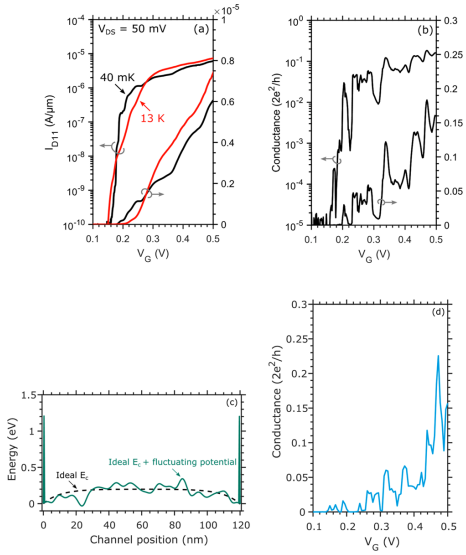

Figure 5. (a) Transfer characteristics normalized to the nanowire width of D_{11} with V_{DS} = 50 mV at 13 K and 40 mK. (b) Normalized conductance of D_{11} measured with V_{DS} = 5 mV at 40 mK. (c) Electrostatic potential along the channel used for calculations. A fluctuating potential with σ = 100 meV and L = 5 nm is superimposed on the ideal conduction band edge profile. (d) Simulated conductance characteristics at 40 mK using a 1D real space tight-binding nonequilibrium Green's functions model.

slope is probably limited by a combination of tunneling through potential fluctuations and interface trap states, while at room temperature limit is set by the Fermi−Dirac distribution and interface trap states. The very small inverse subthreshold slope is encouraging for low voltage operation in order to minimize the power dissipation for cryogenic operation, where cooling power often is very limited.

Figure 5b shows the normalized conductance of D_{11} measured at 40 mK and a low V_{DS} = 5 mV, when sweeping

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gate B_1. This is the minimum limit of the conductance since there is some voltage drop over the channel under gate A_1 as well. At this relatively small bias window, several clear peaks and valleys appear in the conductance. We attribute this to charged defects in the oxide, changing the energy landscape and roughening the conduction band edge. This can be seen as quantum dots connected in series along the channel, which leads to resonance peaks in the transmission at certain energy levels. The resulting electron mobility degradation can be alleviated by moving the conducting channel away from the oxide interface by inserting a thin layer of InP.[17] The drawback of this approach is the reduction of electrostatic control of the channel due to a lower gate-channel capacitance.

Presented in Figure 5c is such a fluctuating potential along the channel. A varying conduction band edge potential (mean standard deviation σ = 100 meV with a correlation length L = 5 nm) is superimposed on a smoothly varying background, obtained from an analytical solution of Poisson's equation and 1D electrostatics. To calculate the transmission and hence the conduction through such a potential, a simple model based on a 1D real space tight-binding nonequilibrium Green's functions (NEGF) model has been used.[18] Each subband is added by an energy separation given by a two-band **k·p** model.[19] The current and transmission through the fluctuating potential are then calculated using NEGF, the resulting conductance is presented in Figure 5d. This model can qualitatively explain the data, since the transmission and resonance peaks highly depend on the exact potential variation along the channel. In order to agree with the experimental data, high potential barriers (1.2 eV) are also needed to be added at the source-drain region. This indicates a need to optimize the regrown contact interface to enable a more transparent contact. This can potentially be achieved by additional cleaning prior to growth or further optimization of the growth parameters. The potential fluctuations within the channel can be minimized by reducing the charged defect concentration at the semiconductor/oxide interface.

In conclusion, we have designed and fabricated a 1-to-4 demultiplexer proof of concept device with good yield based on a selective area grown nanowire network. The design has been characterized at both 13 K and 40 mK and shows good isolation between gates and drains with very small gate leakage. The device exhibits a low minimum inverse subthreshold slope of 6 and 2 mV/dec at 13 K and 40 mK, respectively. At very low temperatures and low bias voltages, the transmission breaks up into resonance peaks due to a rough conduction band edge, highlighting the importance of oxide trap minimization especially when designing electronics for low-temperature operation.

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Notes

The authors declare no competing financial interest.

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Paper VI

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Gate-controlled near-surface Josephson junctions

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ABSTRACT

Gate-tunable Josephson junctions are interesting for quantum technology applications, such as gatemon qubits and topological Majorana-based qubits. Furthermore, high-frequency compatible geometries can be utilized for implementing electrically pumped parametric amplifiers. In this paper, we combine processing, measurements, and modeling of near-surface InGaAs Josephson field-effect transistors in order to facilitate circuit simulations of actual non-ideal devices. We developed a compact model using Verilog-A and confirmed the validity of our model by accurately reproducing our measured data by circuit simulations in Advanced Design System. From the circuit simulations, an effective gate-dependent transmission coefficient, with a peak value of ∼ 3.5%, was extracted, mainly limited by contact transparency.

The increasing interest in quantum computation has put efforts toward the realization of hybrid superconductor–semiconductor devices with highly transparent interfaces.[1–4] The potential application in emerging quantum technologies spans from superconducting quantum computation[5,6] to electrically tuned parametric amplifiers.[7,8] To fully understand and optimize advanced circuits containing hybrid devices, a compact device model is required, that is, a mathematical description of the system using parametric equations. In the literature, there are several works on implementations of compact models for superconductor/insulator/superconductor-based Josephson junctions (JJs)[9–11] and gate-tunable superconductor/semiconductor/superconductor junctions.[12–14] However, there is lack of work that combines processing, measurements, and modeling to facilitate circuit simulations of actual quasi-ballistic non-ideal hybrid devices, which is essential for system-level integration.

We investigate the superconducting properties of a near-surface Al–InGaAs–Al Josephson field-effect transistor (JoFET). The channel is located directly at the surface, allowing for fabrication of short-gate length devices with high gate control. In addition, we use a thinner gate oxide compared to similar works,[15,16] which increases the electrostatic control even further. Such geometry is needed for very short gate length scaling, similar to that of high-performance field-effect transistors.

To facilitate circuit simulations of our device, we developed a compact model, which considers the gate tunability of the semiconductor, the carrier density-dependent mobility and transmission coefficient, semiconductor band tails, non-ideal interfaces, and nonlinear excess resistances, allowing for circuit modeling with more realistic JoFETs.

InGaAs JoFETs were fabricated on a wafer with a layer stack according to Table I, where the 2DEG consists of layers 4, 5, and 6. The epitaxial layer stack is designed for maximum electron carrier concentration in the high indium part of the composite channel, layer 5.

The devices were electrically isolated by resist masking using direct laser writing (DLW), followed by a mesa wet etch into layer 1 using H_3PO_4:H_2O_2:H_2O (1:1:25). Next, source and drain contacts (Ti/Al, 5/40 nm) were defined by electron beam lithography (EBL) followed by e-beam evaporation and liftoff. Titanium is known for its rapid reaction with oxygen and its oxygen-scavenging effects.[17,18] The thin Ti layer in our device serves the purpose of decreasing the amount of free oxygen in the air in the evaporator chamber. This is achieved by formation of titanium oxides, thereby minimizing the formation of insulating low-k Al_2O_3 at the semiconductor–superconductor interface. Just before evaporation, the native oxide on InGaAs was removed in HCl:H_2O (1:20). Next, the gate oxide was deposited by ALD (Al_2O_3/HfO_2, 1/10 nm, 300 °C/120 °C), followed by deposition of the gate contact (Ti/Pd/Au, 5/5/200 nm) by e-beam evaporation and liftoff. The ALD process involves pre-pulsing of trimethylaluminum to restore surface As atoms to a bulk-like bonding configuration and reduce the density of interface traps.[19] Subsequently, the bilayer of Al_2O_3 and HfO_2 is deposited, resulting in a high-quality interface with a low equivalent oxide thickness. The device characterized in this work

TABLE I. Sample layer stack.

Layer	Material	X	T (Å)	Si (cm^{-3})	Function
6	$In_{(x)}Ga_{(1-x)}As$	0.53	30		Channel
5	$In_{(x)}Ga_{(1-x)}As$	0.80	50		Channel
4	$In_{(x)}Ga_{(1-x)}As$	0.53	40		Channel
3	$In_{(x)}Al_{(1-x)}As$	0.52	30		Spacer
2	$In_{(x)}Al_{(1-x)}As$	0.52	30	1.0×10^{19}	Delta doping
1	$In_{(x)}Al_{(1-x)}As$	0.52	1900		Buffer
0	S.I. InP				Substrate

has a device width of $W = 4\,\mu$m and a gate length of $L_g = 210$ nm. A schematic of the device and fabrication steps are shown in Fig. 1.

The devices were characterized at cryogenic temperatures in a Triton dilution refrigerator from Oxford Instruments, with a base chamber temperature at 15 mK. Current-driven measurements were performed as four-point measurements, where the voltage drop was measured over the inner contacts. An alternative device geometry, featuring a T-gate to minimize parasitic capacitances or a junction involving superconductor, semiconductor, and normal conductor, would have facilitated a more in-depth exploration of RF-performance and the induced superconducting gap. A magnetic field evaluation of the induced supercurrent is presented in the supplementary material. However, the primary aim of our device was to validate our DC circuit simulations. Therefore, the simpler device design was adopted. The carrier mobility was extracted by Hall measurements in a closed cycle helium refrigerator at 9 K, with an applied magnetic field from −1 T to 1 T perpendicular to the sample surface.

We implemented a Verilog-A code to model the behavior of our device in Advanced Design System (ADS). A circuit schematic of the system used is shown in Fig. 2(a). A voltage source, V_{drive}, in series with a 20 MΩ resistor is used to simulate current-driven measurement similar to the real experiments. R_g and V_g represents the gate finger resistance and the applied gate voltage, respectively. Two parasitic capacitances, $\frac{C_p}{2}$, are included due to an overlap between the gate contact and the source–drain contacts. The part of the circuit within the dashed line in Fig. 2(a) is implemented in a Verilog-A code, where JJ represents the Josephson junction. The full device is characterized by contact resistance, R_c, normal channel resistance, R_{ch}, a nonlinear excess resistance, R_{ex}, and total intrinsic gate capacitance, C_{gg}. C_{gg} is obtained from reference C–V measurements,[20] including the influences of centroid capacitance and quantum capacitance based on the effective mass obtained through k·p modeling.[21] C_p is determined from the overlap area between the gate electrode and source–drain electrodes, using the relative permittivity of the gate oxide,[20] and assuming a parallel plate capacitor. Their corresponding values are $C_{gg} = 5.58$ fF and $C_p = 160$ fF, and thus $C_{gg} \ll C_p$.

We assume that the total current, I, has one contribution from the normal quasi-particle current, I_N, which obeys Ohm's law, and one contribution from the supercurrent, I_S, which satisfy the Josephson equation,[22]

$$I_S = I_c \sin(\Delta\varphi), \tag{1}$$

where $\Delta\varphi$ is the gauge invariant phase difference between the superconductors, and the critical current, I_c, is the maximum supercurrent of the junction. The phase difference is implemented in the circuit model by connecting our device to a voltage-controlled current source parallel to a capacitor, see Fig. 2(b). The voltage and gauge invariant phase over the JJ is given by

$$V_{JJ} = \frac{\hbar}{2q}\frac{d\Delta\varphi}{dt}, \tag{2}$$

where $\hbar$ is the reduced Planck's constant, and q is the elemental charge. In the circuit simulator, the gauge invariant phase difference is represented by voltage V_φ over a capacitor C_φ in the subcircuit in Fig. 2(b). The voltage-controlled current source is controlled by V_{JJ}, and with a gain of unity, the current becomes

$$I_\varphi = V_{JJ} = C_\varphi \frac{dV_\varphi}{dt} = \frac{\hbar}{2q}\frac{d\Delta\varphi}{dt}, \tag{3}$$

where we have used the definition of the current through a capacitor. If the capacitance is set to $\frac{\hbar}{2q}$, $\Delta\varphi$ and V_φ are interchangeable, and the supercurrent current through the JJ, see Eq. (1), can be expressed as

$$I_S = I_c \sin(V_\varphi). \tag{4}$$

It is important to note that $\Delta\varphi$ and V_φ do not have the same dimension, and the substitution is solely performed to facilitate the implementation of a phase difference in ADS. The method used to get Eq. (4) is based on the work in Ref. 23. The expression of the critical current, I_c, is based on the works in Refs. 24 and 25, see the supplementary material for details,

$$I_c = N\frac{D_n}{4\pi}\frac{q}{\tau}, \tag{5}$$

where D_n can be seen as an effective transmission coefficient and τ is related to the time it takes for a Cooper pair to travel from one

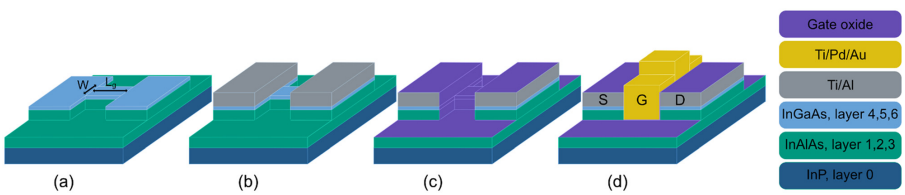

FIG. 1. A mesa was defined by resist masking and wet etching into InAlAs (a). Ti/Al contacts were deposited by e-beam evaporation (b), followed by deposition of the gate oxide (c). Finally, the gate contact was deposited (d). The gate length L_g and device width W are indicated in the figure, and the layer numbers are given in Table I.

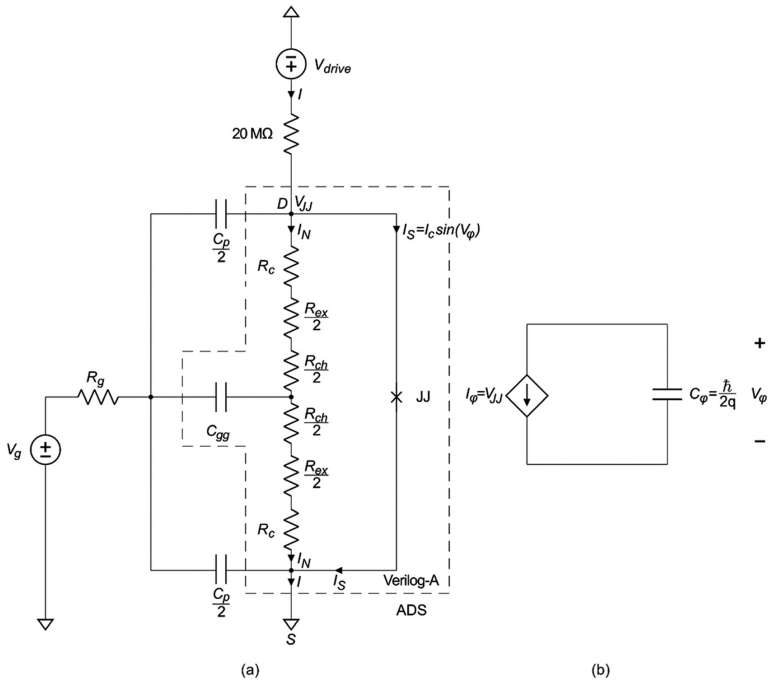

FIG. 2. Circuit schematic of the system used in Verilog-A and ADS (a). Circuit used to implement the phase difference, $\Delta\varphi$ (b).

superconductor to the other. D_n is used as a fitting parameter and is assumed to be equal for all conducting modes. The number of modes can be found from

$$N = \frac{W}{\left(\frac{\pi}{k_F}\right)} = W\sqrt{\frac{2n_s}{\pi}}, \tag{6}$$

where k_F is the Fermi wave vector and n_s is the electron carrier concentration. Following the work in Ref. 26, an approximate expression for n_s is

$$n_s = \frac{C_{gg} n \phi_t}{q} \ln\left(1 + e^{\frac{V_{gs}-V_T}{n\phi_t}}\right), \tag{7}$$

where V_T is the threshold voltage and $n = \frac{SS}{\phi_t \ln(10)}$ is the subthreshold coefficient, described by the subthreshold swing, SS, and the thermal voltage $\phi_t = \frac{k_B T}{q}$, where k_B is the Boltzmann constant and T is the temperature. Eq. (7) is suitable to use for circuit simulations due to the expression being continuous and valid for both $V_{gs} \gg V_T$ and $V_{gs} \sim V_T$. At lower temperatures, the influence of band tails becomes significant, and this effect is captured by the subthreshold coefficient. The channel resistance, R_{ch}, used to calculate the contribution from the normal current, can then be expressed using the transport transmission probability per conducting mode τ_{ch},

$$R_{ch} = \frac{1}{NW}\frac{h}{2q^2}\frac{1}{\tau_{ch}}, \tag{8}$$

where $\tau_{ch} = \frac{\lambda}{\lambda + L_g}$[27] and $\lambda = n_s q \mu_n \frac{h}{2q^2}\frac{W}{N}$[27] is the mean free path. Here, μ_n is the gate-dependent channel mobility. The gate dependence of the mobility is implemented in the model by measurements of the Hall mobility at 9 K and $V_{gs} = 0$ V.[28]

The total resistance of the device is modeled by $R_{tot} = 2R_c + R_{ch} + R_{ex}$, where R_{ex} describes how the nonlinear resistance of the junction varies with V_{JJ} and can give rise to a positive or negative excess current. We use the Octavio–Tinkham–Blonder–Klapwijk (OTBK) theory,[29] assuming ballistic transport and fully incoherent junctions, which for nontransparent contacts predicts a positive

nonlinear resistance that goes to zero for large enough V_{JJ}. Using the work by Niebler *et al.*[30] and assuming $I_{ex} < 0$, the nonlinear resistance can be modeled as

$$R_{ex} = \begin{cases} 0 & \text{if } |V_{JJ}| \geq \eta 2\Delta, \\ -\frac{R_0}{2\Delta\eta}|V_{JJ}| + R_0 & \text{if } |V_{JJ}| < \eta 2\Delta, \end{cases} \quad (9)$$

where $\Delta = 1.764 k_B T_c$ is the superconducting gap at $T = 0$ K, T_c is the critical temperature, and R_0 and η are fitting parameters for better fit to the real quasi-ballistic transport. Numerical solution of the OTBK model shows that the nonlinear resistance, for $I_{ex} < 0$, behaves approximately as we describe with the simpler fit that R_{ex} decreases linearly from R_0 and goes to zero when V_{JJ} becomes sufficiently large. The normal current is $I_N = \frac{V_{JJ}}{R_{ex}}$, and the total measured current is $I = I_S + I_N$. In the compact model, the fitting parameters are $D_n(V_{gs})$, $R_0(V_{gs})$, η, and V_T, where D_n and R_0 are described by analytic functions of V_{gs}.

The device shows good electrostatic control, with a normal current subthreshold swing of $SS \sim 130$ mV/decade at 15 mK and $V_{ds} = 50$ mV. Even lower swings can be achieved by sulfur passivation,[20,21,31] which however is not directly compatible with the gate-last process utilized here. From Hall effect measurements, $\mu_n \sim 7700$ cm^2/V s and $n_s \sim 4 \times 10^{12}$ cm^{-2} were extracted at 9 K and $V_{gs} = 0$ V, which correspond to a mean free path $\lambda \sim 400$ nm $> L_g$, indicating that the device is operating close to the ballistic limit for $V_{gs} \gg V_T$. For lower carrier concentrations, we expect the mobility to decrease due to remote coulomb scattering,[32] and we have observed from reference samples that $\mu_n \propto n_s^{2.1}$ for low n_s. The crossover from diffusive to ballistic regime is important to consider for devices operating close to V_T, which will influence both the normal resistance and the critical current. Relating λ to the coherence length, ξ_0, using Eq. (S1) in the supplementary material, gives $\lambda \ll \xi_0 \sim 4000$ nm, and the device is thus in the ballistic dirty limit.[15] This gives a dirty coherence length, $\xi_{0,d} = \sqrt{\xi_0 \lambda} \sim > 1300$ nm, close to the coherence length of Al.[33]

In Fig. 3(a), the gate and temperature dependence of I_c is presented, showing a good electrostatic control of I_c, and a decrease in I_c with increasing temperature, related to a decreased induced superconducting gap. At 700 mK, the V–I plateaus have disappeared, and I_c is not possible to extract anymore. We, therefore, conclude that $T_c \approx 700$ mK. The noise in Fig. 3(a) at 700 mK is only related to uncertainty in the low current I_c extraction.

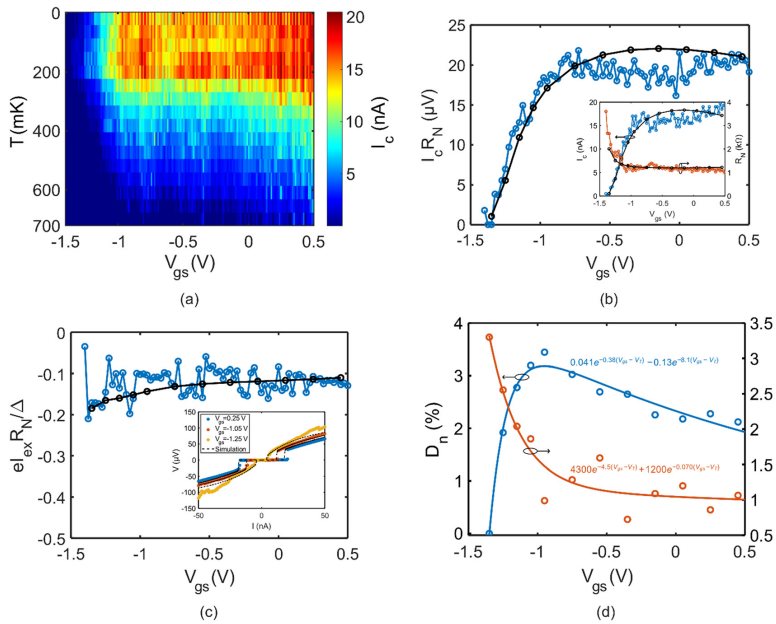

FIG. 3. Temperature and gate dependence of I_c, showing $T_c \approx 700$ mK (a). I_cR_N is plotted vs V_{gs}, together with simulated data in black (b). The inset shows measured I_c and R_N together with simulations in black, plotted vs V_{gs}. The normalized $I_{ex}R_N$ product is plotted vs V_{gs}, together with simulations in black. (c). The inset shows V–I curves for three different V_{gs}. The gate-dependent fitting parameters used in the compact model of the JoFET (d). The effective transmission coefficient, D_n, increases to a peak value of 3.5% and then decreases due to the high R_c.

In Fig. 3(b), the standard figure of merit for hybrid JJs, R_N times I_c, is plotted vs V_{gs}. The measured and simulated data from circuit simulations shows excellent agreement. The inset shows I_c and R_N plotted vs V_{gs}, showing a strong initial increase in I_c above V_T and then a more gradual increase, deviating somewhat from the ideal $I_c \propto \sqrt{V_{gs} - V_T}$ behavior, see Eqs. (5)–(7). The strong increase close to V_T is related to an increase in the mean free path due to the increased mobility, with a gentler increase for larger gate overdrives as the mobility is more constant. At large positive V_{gs}, when R_{ch} is negligible, R_N is approximately equal to $2R_c \sim 1100\,\Omega$. In the compact modeling, $R_c = 550\,\Omega$ was used. In Fig. 3(c), the normalized product of I_{ex} times R_N is plotted vs V_{gs}. The Andreev reflection across the junction gives rise to an excess current, $I_{ex} = I - \frac{V_{JJ}}{R_N}$, which can be found from the V–I curves, three of which are shown in the inset, by extrapolation back to the $V_{JJ} = 0$ axis.[34] The product $I_{ex}R_N$ shows no clear gate voltage dependence, which indicates that $I_{ex}R_N$ is not affected by the change in carrier concentration in the 2DEG, but rather depends on the interface transparency Z of the superconductor–semiconductor interface.[15] It is clear that $I_{ex} < 0$, which indicates that the current gain due to the Andreev reflection is smaller than the current loss due to the normal reflection process. Therefore, the excess current observed in this device is rather a deficit current,[35] suggesting a $Z > 1.2$.[30] The presence of the interface barriers implies a small Andreev reflection coefficient, meaning few carriers that penetrate from the 2DEG into the superconductor, effectively producing a deficit current.[36] This is in line with transmission line measurements on reference samples, showing a specific contact resistance between Al and the InGaAs stack, $R_c \approx 10^4\,\Omega\,\mu$m, as compared with optimized ohmic contact technology yielding $R_c < 10^3\,\Omega\,\mu$m.

In Figs. 3(b) and 3(c), the data obtained from circuit simulations using our compact model of the JoFET are indicated in black and show excellent agreement with the measured data. The gate-dependent fitting parameters used in the compact model of the JoFET are presented in Fig. 3(d) as a function of V_{gs}. The data points correspond to exact fittings to the measured data, while the gate dependence used in the final model is obtained by fitting exponentials to these data points. R_0 resembles R_N but does not increase as quickly at low V_{gs}. The effective transparency, D_n, follows approximately the mobility. First, a strong increase is shown close to V_T, with a maximum transmission of 3.5%, then a decrease due to the limited transparency of the Al-InGaAs contacts is observed. There is an uncertainty in D_n, which is related to the fitting value used for V_T. If V_T is overestimated, less modes will be conducting and D_n will need to be larger in order to give the same current. In the compact model, V_T is set to -1.5 V, and η is set to 0.46.

We have fabricated and characterized a near-surface JoFET at cryogenic temperatures. Our device shows good tunability of the supercurrent and a high channel mobility of 7700 $\mathrm{cm^2/V\,s}$ at 9 K. To investigate the potential of JoFETs in future gate-tunable qubit systems, we developed a Verilog-A-based compact model of the near-surface JoFET. Circuit simulations in ADS using our compact model show excellent agreement with the measured data at cryogenic temperatures. Especially, when operating close to V_T, we find that the device shows a crossover from diffusive to ballistic regime, which must be considered for device concepts operating close to V_T. Our model enables system-level investigation of circuits containing realistic, non-ideal JoFETs, which is essential for the development of gate-tunable qubits.

See the supplementary material for magnetic field evaluation of the induced supercurrent as well as an explanation of the expression for the critical current.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

L. Olausson and P. Olausson contributed equally to this work.

L. Olausson: Conceptualization (equal); Investigation (equal); Methodology (equal); Writing – original draft (equal); Writing – review & editing (equal). **P. Olausson:** Conceptualization (equal); Investigation (equal); Methodology (equal); Writing – original draft (equal); Writing – review & editing (equal). **E. Lind:** Conceptualization (equal); Funding acquisition (lead); Methodology (equal); Supervision (lead); Writing – review & editing (supporting).

DATA AVAILABILITY

The data that support the findings of this study are openly available in Zenodo at https://doi.org/10.5281/zenodo.10401032, Ref. 37.

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Paper VII

Paper VII

J. Svensson, P. Olausson, H. Menon, S. Lehmann, E. Lind and M. Borg, "Three-Dimensional Integration of InAs Nanowires by Template-Assisted Selective Epitaxy on Tungsten," *Nano Letters*, vol. 23, no. 11, pp. 4756-4761, June 2023, doi: 10.1021/acs.nanolett.2c04908.

NANO LETTERS

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Three-Dimensional Integration of InAs Nanowires by Template-Assisted Selective Epitaxy on Tungsten

Johannes Svensson,* Patrik Olausson, Heera Menon, Sebastian Lehmann, Erik Lind, and Mattias Borg

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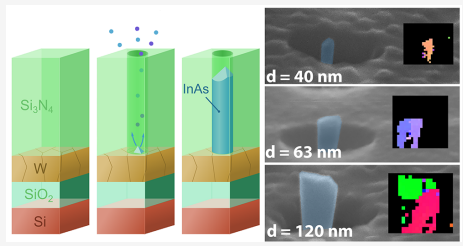
ABSTRACT: 3D integration of III-V semiconductors with Si CMOS is highly attractive since it allows combining new functions such as photonic and analog devices with digital signal processing circuitry. Thus far, most 3D integration approaches have used epitaxial growth on Si, layer transfer by wafer bonding, or die-to-die packaging. Here we present low-temperature integration of InAs on W using Si_3N_4 template assisted selective area metal–organic vapor-phase epitaxy (MOVPE). Despite growth nucleation on polycrystalline W, we can obtain a high yield of single-crystalline InAs nanowires, as observed by transmission electron microscopy (TEM) and electron backscatter diffraction (EBSD). The nanowires exhibit a mobility of 690 $cm^2/(V\,s)$, a low-resistive, Ohmic electrical contact to the W film, and a resistivity which increases with diameter attributed to increased grain boundary scattering. These results demonstrate the feasibility for single-crystalline III-V back-end-of-line integration with a low thermal budget compatible with Si CMOS.



KEYWORDS: *InAs, III-V semiconductors, nanowires, metal–organic vapor-phase epitaxy, selective area epitaxy, Si CMOS integration*

III-V semiconductor devices are dominating applications in optoelectronics and high-speed analog electronics such as signal amplification and processing due to their high carrier mobilities and injection velocities. For emerging 6G wireless networks, 3D heterointegrated high-frequency systems are considered essential,[1] and it is thus highly attractive to monolithically integrate high-performing III-V devices such as high electron mobility transistors (HEMTs) or high-speed photodetectors on top of Si CMOS circuitry, since this enables new functionalities, minimizes latency, and allows optimal heat dissipation. However, any viable III-V integration method needs to (i) be cost-efficient i.e. enable integration on Si substrates without the use of expensive bulk III-V substrates, (ii) be scalable to the 200–300 mm wafer diameters used in industry, (iii) use low-temperature processes to not exceed the temperature budget of Si CMOS, and (iv) achieve a sufficiently high material quality.

Until now, the most promising routes have been direct wafer bonding[2] and variations of selective area epitaxial growth techniques using dielectric masks. Direct wafer bonding has been used to demonstrate integration of III-V layers on Si wafers with diameters up to 200 mm[3] and integration of high electron mobility transistors and Si CMOS;[4] however, the process requires ultraclean surfaces with very low roughness, as any particles result in extended bonding defects and a degraded quality of the transferred film.[5] In addition, for direct wafer bonding to be economically viable requires that the donor III-V wafer can be reused.[3] The most successful direct epitaxial techniques are conformal lateral overgrowth,[6] aspect ratio trapping,[7] and template-assisted selective epitaxy (TASE).[8] These selective area growth techniques[9] are closely related and rely on crystal nucleation inside openings in dielectric masks which stop threading dislocations, that originate from the III-V/Si interface, from extending far into the material. In TASE, a circular dielectric mask opening with a small diameter is used, since such confinement in two dimensions promotes crystal formation from a single nucleation event and thus antiphase boundaries can be avoided.[10]

The TASE technique has enabled various innovations such as sequential and dense cointegration of different III-V semiconductors (InAs and GaSb),[11] lateral heterojunctions[12] as well as III-V MOSFETs,[13] tunnel field effect transistors,[14] and photodetectors,[15] all integrated to be coplanar with Si. Thus, TASE allows for integration of III-V devices close to the active layer in a CMOS stack, which is known as the front-end-of-line (FEOL). In this paper, we extend the use of the TASE method to allow also for III-V device integration further up in the metal layer stack, in what is known as the back-end-of-line

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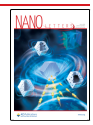

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(BEOL) consisting of metal interconnects and dielectric layers. This enables true heterogeneous and monolithic 3D systems to be realized, combining for instance high-speed low-noise amplifiers, photodetectors, and sensors on top of Si CMOS circuitry used for readout and digital processing, without requiring significant changes to the CMOS active layer or increasing the total chip area.

Here we present a technique for InAs metal organic vapor phase epitaxy (MOVPE) directly on W using TASE. The confinement induced by a Si_3N_4 template allows the creation of single-crystalline InAs on polycrystalline W, in contrast to unmasked growth, which has been shown to result in a poor-quality semiconductor.[16] In addition, our method does not require expensive substrates, since the W can be deposited on various surfaces, it is also scalable to large-diameter wafers and the growth temperature of 450 °C is sufficiently low to not degrade any underlying CMOS circuits,[17] thus fulfilling the requirements (i)−(iii) discussed above. W is suitable since it has a high melting point, a low thermal expansion coefficient, and a low resistivity and has been demonstrated to form a low-resistivity contact to InGaAs.[18] Also, since W is used at the interface between the FEOL and BEOL of a Si CMOS stack, our III-V integration method can be deemed to be CMOS compatible.

The samples consist of a layer stack of 50 nm W/6 nm Al_2O_3/380 nm Si_3N_4/12 nm Cr (bottom to top) deposited on Si with a 100 nm thick SiO_2 layer (Figure 1). Circular holes with 40−300 nm diameter and 500−2000 nm pitch were etched in the Si_3N_4 using the Cr as a hard mask which had been patterned by electron beam lithography (see the Supporting Information for details). InAs was grown for ∼15 min at 450 °C using MOVPE with TMIn and AsH_3 without any preceding annealing step, which is below the maximum allowed temperature budget for Si CMOS.

The grown samples were cleaved to enable cross sectional imaging using scanning electron microscopy (SEM). The orientation and the crystallinity of InAs nanowires were inspected using electron backscatter diffraction (EBSD) at an accelerating voltage of 10 kV and a 20−50 nm step size to maximize the number of pixels per nanowire. To inspect the nanowires in more detail, they were mechanically transferred onto a lacey-carbon-supported Cu grid using a micromanipulator to enable transmission electron microscope (TEM) imaging.

To enable electrical characterization, 10 nm Ni/150 nm Au contacts were patterned on top of individual InAs nanowires of different diameters by optical lithography, sputtering, and lift-off, while utilizing the Si_3N_4 template as an isolating planar spacer. To access the W layer and contact the bottom of the nanowires, vias were etched using SF_6-based ICPRIE prior to metal deposition and electrical characteristics were measured at room and cryogenic temperatures.

With the optimized growth conditions, as will be discussed below, we achieve InAs nanowire growth in all template openings. The nanowires in an array have uniform lengths and an inversely tapered geometry which follows that of the Si_3N_4 template (Figure 2a).

To achieve single-crystalline InAs growth, it is imperative that there is only a single nucleation event on the exposed W at the bottom of each template tube and that this nucleus grows to fill up the full template cross-sectional area before another nucleation event occurs. This requires the nucleation probability on the W surface to be sufficiently high compared

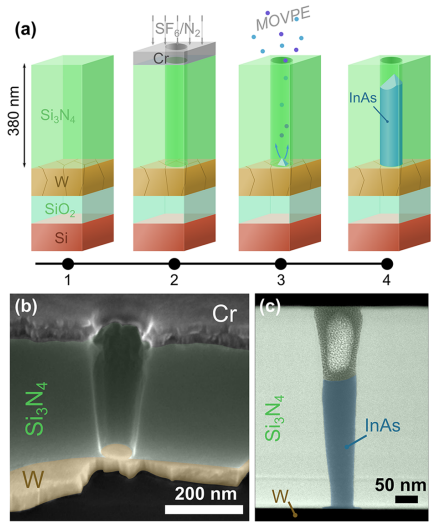

Figure 1. (a) Schematic illustration of the process to (1) form the material stack on a Si substrate, (2) etch template openings in Si_3N_4 using ICPRIE with an EBL patterned Cr mask, and (3) remove the Cr mask followed by MOVPE where a single nucleus is formed on the exposed W, resulting in (4) a single-crystalline InAs nanowire inside the Si_3N_4 template. (b) SEM cross section of a template before the Cr mask etch. (c) Scanning TEM of an as-grown InAs nanowire inside the template which has been filled with Pt for lamella preparation. Coloring of the SEM and STEM images are only for visualization purposes.

to the surrounding Si_3N_4 surfaces. However, the nucleation probability on the W cannot be too high, as this would inevitably lead to nucleation of multiple distinct crystallites that would converge into a polycrystal. To optimize the conditions for selective InAs growth initiated from a single nucleus on the W, we study the effect of flow and V/III ratio on InAs nucleation. For a growth process with only a short (6 min) nucleation step, it is possible to observe the number of nuclei by SEM. For low precursor molar fractions of X_{TMIn} = 3.8×10^{-7} and X_{AsH_3} = 7.6×10^{-6}, i.e. V/III = 20, template openings with 120 nm diameter (Figure 2b) and larger mostly exhibit multiple nuclei, which upon further growth could lead to a polycrystalline nanowire. On the other hand, template openings with a diameter of 40 nm predominately have a single nucleus (Figure 2c).

In contrast, if the growth is initiated using a high precursor molar fraction and high V/III ratio (X_{TMIn} = 3.8×10^{-6}, X_{AsH_3} = 3.8×10^{-4}, V/III = 100), InAs nucleates on the top edge or the inner sidewalls of the template openings instead of on the W surface at the bottom (Figure S1 in the Supporting Information). Under these conditions, the supersaturation is high enough that the precursors do not reach the bottom of the templates before nucleation occurs on the Si_3N_4 surface. However, high V/III ratios are necessary during the main part of the growth process to avoid incomplete filling of the template openings (Figure S2 in the Supporting Information),

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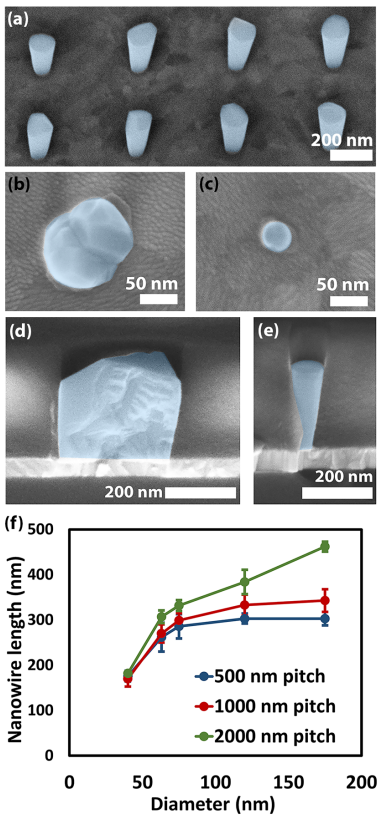

Figure 2. (a) False-color SEM image of InAs crystals grown in 75 nm diameter templates after the Si_3N_4 template has been removed. (b, c) Crystals after the 6 min nucleation step with low V/III ratio with 120 nm (b) and 40 nm (c) template diameter. (d, e) InAs crystals grown in 315 nm and 63 nm diameter templates. (f) Length vs template diameter for three different pitches. Note that the longest nanowires for 2000 nm pitch protrude above the 380 nm thick Si_3N_4 template.

since a low V/III ratio is known to give anisotropic growth, mainly on the (111)B facet, an effect which is more pronounced at low growth temperatures.[19] Also, since we do not at this point control the orientation of the InAs crystals, the upward-facing facet types will vary between different template openings. Having similar growth rates on all facets thus ensures uniform nanowire dimensions across the sample. Therefore, by combining a nucleation step using a low flow and V/III ratio with a subsequent growth step using a considerably higher flow and V/III ratio, we achieve a complete filling of the template openings (see Figure 2a,d,e) and uniform InAs nanowire lengths.

Having established suitable nucleation conditions, we investigate the growth dynamics due to the tubular templates. For the larger template openings (>120 nm) (Figure 2d), the crystals exhibit multiple, uncorrelated facets, which is a sign of polycrystallinity. In contrast, only one flat top facet or a few inclined facets can be observed for InAs grown in the smaller openings (Figure 2e), indicating that these may be single crystalline. We also observe that the growth rate is significantly reduced with decreasing template diameter (Figure 2f) in agreement with Borg et al.,[8] who concluded that growth in TASE is limited by Knudsen diffusion for which the molecular flow per area is linearly dependent on the template diameter. The growth rate follows a linear increase with template diameter up to 75 nm, with little or no impact of the pitch between template openings, thus indicative of Knudsen diffusion. For larger diameters, the aspect ratio of our 380 nm deep templates is small and Knudsen diffusion may no longer limit the growth rate. Indeed, we observe an almost diameter-independent growth rate for the largest openings. In addition, for these diameters the growth rate increases with increased template opening pitch, indicating that the growth rate is limited by the collection of material from the neighboring area at the top of the Si_3N_4. For a smaller pitch, the collection areas overlap and thus there is competition for material, resulting in a decreased growth rate. Note that the arrays with the largest diameter and pitch have InAs nanowires that protrude above the template, which gives a high growth rate at the end of the process. For extended growth times using the conditions for optimal template filling, also the InAs nanowires from small-diameter openings protrude above the mask, extending laterally to form a larger crystal at the top.

High-resolution TEM was used to image InAs nanowires grown in 40 and 120 nm template openings (Figure 3). The nanowires have a single-crystalline zincblende crystal structure and exhibit a wider base due to underetching of Al_2O_3 underneath the Si_3N_4 template. The 40 nm diameter nanowire has a high density of stacking faults with a large inclination angle with respect to the Si_3N_4 template orientation that results in streaks in the diffraction pattern (Figure 3c). In contrast, apart from the nucleation region, the 120 nm diameter InAs nanowire has a very low density of stacking defects but has a few twinned segments along different ⟨111⟩ directions, in line with previous observations of twin formation predominantly occurring on the (111)B growth plane.[19] It has previously been shown that such stacking faults and twins do not significantly affect the resistivity of InAs nanowires and they are therefore not expected to be detrimental to device characteristics.[13,20] It was not possible to obtain high-quality images of the bottom of the 120 nm diameter nanowire, and thus we cannot exclude that the growth is polycrystalline at the nucleation stage. Due to the diameter dependence of precursor transport, it is likely that growth conditions at the bottom of the templates are different for the two diameters, which may impact nucleation and thus defect formation as the nucleus expands.

EBSD was used to probe the crystal structure of 17−30 nanowires for each diameter to obtain statistics not possible with HRTEM. To do this, the Si_3N_4 film was partially wet etched (BOE 1:10) so that the InAs nanowires protruded. In Figure 4 (and Figure S3 in the Supporting Information), SEM images of arrays of nanowires with 40, 63 and 120 nm diameters are presented together with the crystal orientation of the nanowires parallel to the normal direction of the sample as obtained by EBSD. It is clear that almost all of the 40 and 63 nm diameter nanowires are single crystalline and have different orientations. In contrast, more than half of the 120 nm diameter nanowires (Figure 4c) exhibit EBSD patterns with

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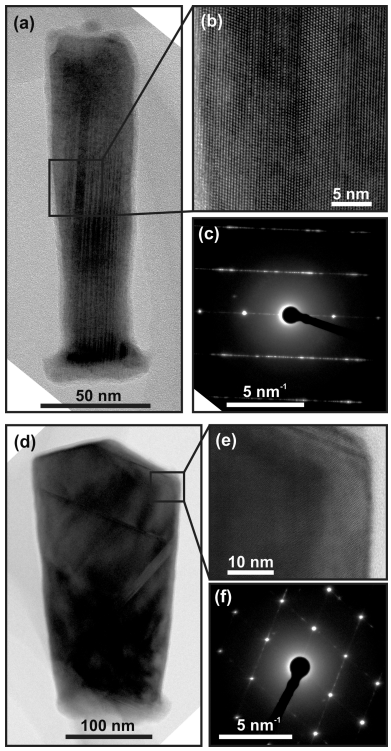

Figure 3. TEM overview and high-resolution (HRTEM) images and selected area diffraction patterns (SADPs) from InAs nanowires with 40 nm (a–c) and 120 nm (d–f) diameters obtained at 300 kV using a JEOL 3000F instrument. The 40 nm diameter nanowire has a high density of stacking faults, as can be observed from the HRTEM image and the streaks in the SADP, while the 120 nm diameter nanowire is almost free of stacking defects apart from three twinned segments.

multiple uncorrelated orientations in each template, clearly being the result of polycrystalline growth. Note that the EBSD map of one of the nanowires with 63 nm diameter has two stripes. By correlating the relative orientation of these areas to the rest of the nanowire, it is concluded that these are twin plane defects are not the result of polycrystalline growth. We observe a 95% single-crystalline yield for template diameters of 63 nm and below (Figure 4d), with a reduction in yield for larger diameters. Note that we do not observe any preferred crystal orientation from EBSD measurement on 120 nm nanowires (color map in Figure 4). This result gives us confidence that this method can achieve high-crystal-quality InAs nanowires suitable for device integration in the Si BEOL.

Since large-diameter template openings give polycrystalline InAs and even the single-crystalline nanowires have uncontrolled orientations, it is of interest to study the W film in more detail. Sputtered W forms two major phases depending on sputtering parameters, and the low-resistivity α-W phase, with a bcc structure and a lattice constant of 0.316 nm, is typically

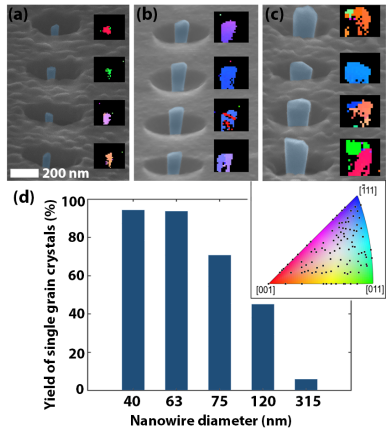

Figure 4. (a–c) EBSD analysis of InAs crystals grown in Si_3N_4 template openings of different diameters. The template has been partially wet etched so that the InAs protrudes. SEM images at 70° tilt and corresponding EBSD color map (IPZ orientation) of InAs nanowires with 40 nm (a), 63 nm (b) and 120 nm (c) diameters. The orientation of all 120 nanowires analyzed is displayed in the color map. (d) Yield of single-grain InAs as a function of template opening diameter as determined from EBSD analysis.

predominant.[21] Indeed, X-ray diffraction analysis of 50 nm W gives three peaks ({110}, {200}, {211}) corresponding to the α-W phase (Figure S4 in the Supporting Information), and an EBSD analysis of 20 nm W shows that 87% of the grains have the α-W phase and no evident texture (Figure S5 in the Supporting Information). The majority of grains are much larger than the smallest template opening (0.001 μm^2), indicating that in most cases a single grain should be present at the bottom of the templates.

To be able to control the crystal orientation of the InAs nanowires by e.g. tuning the texturing of the W film,[22] there needs to be an epitaxial relationship between them. However, due to the geometry used in the EBSD setup, it is not possible to correlate the crystal orientation of entire nanowires to the orientation of the W grains on which they nucleated. Therefore, EBSD was performed on InAs grown using only the short nucleation step (Figures S6 and S7 in the Supporting Information). Distinctive Kikuchi patterns for two InAs crystals and W grains showed that for one of the InAs crystals, its orientation was close to that of one of the W grains in its vicinity. However, no orientation relation was deduced from a second InAs crystal; therefore, we cannot draw general conclusions of a possible epitaxial relationship at this point.

A major and unique benefit of our integration approach is that we directly grow the InAs nanowires on a metal that without further processing could potentially be used as a contact in an electronic device. It is therefore vital to evaluate the electrical characteristics of the W/InAs contact as well as the InAs nanowires themselves (Figure 5). The current–voltage (I–V) characteristics of representative InAs nanowires are Ohmic, with no indication of Schottky-like behavior at either of the electrodes. Indeed, we confirm the absence of a significant energy barrier by measuring the I–V characteristics

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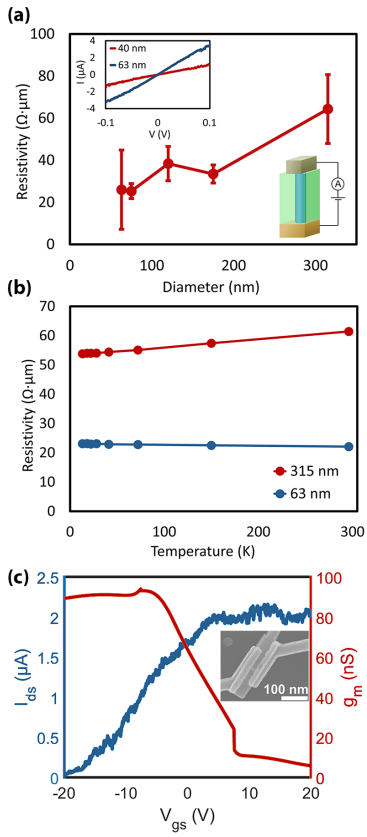

Figure 5. (a) Resistivity as a function of nanowire bottom diameter at room temperature obtained using a Keysight B1500A parameter analyzer. 4−6 nanowires were measured for each diameter. The *I*−*V* characteristics for 40 and 63 nm diameter nanowires and a schematic device are displayed in the insets. (b) Resistivity as a function of temperature for nanowires with 63 nm and 315 nm diameters. (c) Transfer characteristics and transconductance of a single 70 nm diameter back-gated nanowire at V_{ds} = 10 mV with a SEM image of the device being given in the inset.

at various temperatures down to 13 K, which in all cases result in similar Ohmic characteristics.

The resistivities of the InAs nanowires were extracted from the inverse slope of the *I*−*V* characteristics, taking into account the tapered geometry of the nanowires (Figure S8 in the Supporting Information) and evaluated as a function of diameter and temperature. Again we see the impact of polycrystallinity for nanowires with larger diameters. The resistivity increases significantly from 26 Ω μm for the 63 nm template opening to 64 Ω μm for the 315 nm opening. This is attributed to an increasing number of grain boundaries in polycrystalline InAs grown in the larger openings which results in more electron trapping and scattering.[23,24] We see little change in resistivity with temperature, indicating that the mobility is limited by charged impurity scattering as opposed to phonons.[25]

A crude estimation of the carrier concentration can be obtained by $n = \frac{1}{q \times \mu \times \rho}$, where ρ is the resistivity, μ the mobility, and q the elementary charge. To estimate the mobility, the Si_3N_4 was wet etched, nanowires were transferred to a Si substrate with a 200 nm thick SiO_2 layer, and Ni/Au source-drain contacts were patterned using EBL and lift-off. Transfer characteristics were measured at V_{DS} = 10 mV using the Si substrate as a back gate (Figure 5c). The field effect mobility is then obtained from $\mu_{FE} = g_m L^2/CV_{DS}$, where $g_m = dI_D/dV_{GS}$ = 94 nS is the transconductance, L = 140 nm the distance between the contacts, C = 2.68 aF the capacitance to the back gate calculated using the finite element method (Figure S9 in the Supporting Information), and V_{DS} = 10 mV the source-drain bias.[26] This calculation gives a lower bound estimate of the mobility of μ_{FE} = 690 $cm^2/(V\,s)$, assuming that contact and series resistances and interface states are negligible. Combining the lower mobility estimate with the resistivity of 25 Ω μm obtained from vertical nanowires gives an upper bound carrier concentration of $n = 3.6 \times 10^{18}$ cm^{-3}.

This result indicates a moderate unintentional doping in our nanowires that could originate from background carbon incorporation due to the low growth temperature[27] but more likely is due to Si incorporation from a nonstochiometric Si_3N_4 film. This background doping could be reduced by the use of an ethyl-type In precursor (triethylindium), Si_3N_4 of higher quality, or a SiO_2 template.[13] Nevertheless, the measurements demonstrate electrically well-behaving InAs nanowires with Ohmic connection to the bottom W electrode without the need for further processing.

In summary, we have demonstrated that single-crystalline InAs nanowires can be grown on polycrystalline W films by confining the growth in two dimensions in a dielectric template, resulting in nanowires with uniform dimensions determined by the shape of the template, but at this point with uncontrolled crystal orientation. The W/InAs interface provides a stable and Ohmic contact to the InAs nanowires which have unintentional doping estimated to be at most 3.6×10^{18} cm^{-3}. In conclusion, our low-temperature TASE on W process enables growth on noncrystalline substrates and paves the way toward low-cost, scalable heterogeneous integration of III-V devices in the Si CMOS BEOL.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.2c04908.

Growth template fabrication process, SEM images of InAs grown with high total flow and high V/III and low flow and low V/III, additional EBSD orientation maps, GIXRD scan of bare W film, EBSD phase map and grain area analysis of W, EBSD analysis of InAs and the surrounding W grains after the nucleation step, EBSD of band contrast of a single InAs grain, and FEM simulation of potential distribution in InAs for resistivity calculations (PDF)

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Author Contributions

J.S., P.O., and H.M. contributed equally to this work.

Notes

The authors declare no competing financial interest.

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