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Ferroelectric Memristors - Materials, Interfaces and Applications

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2024

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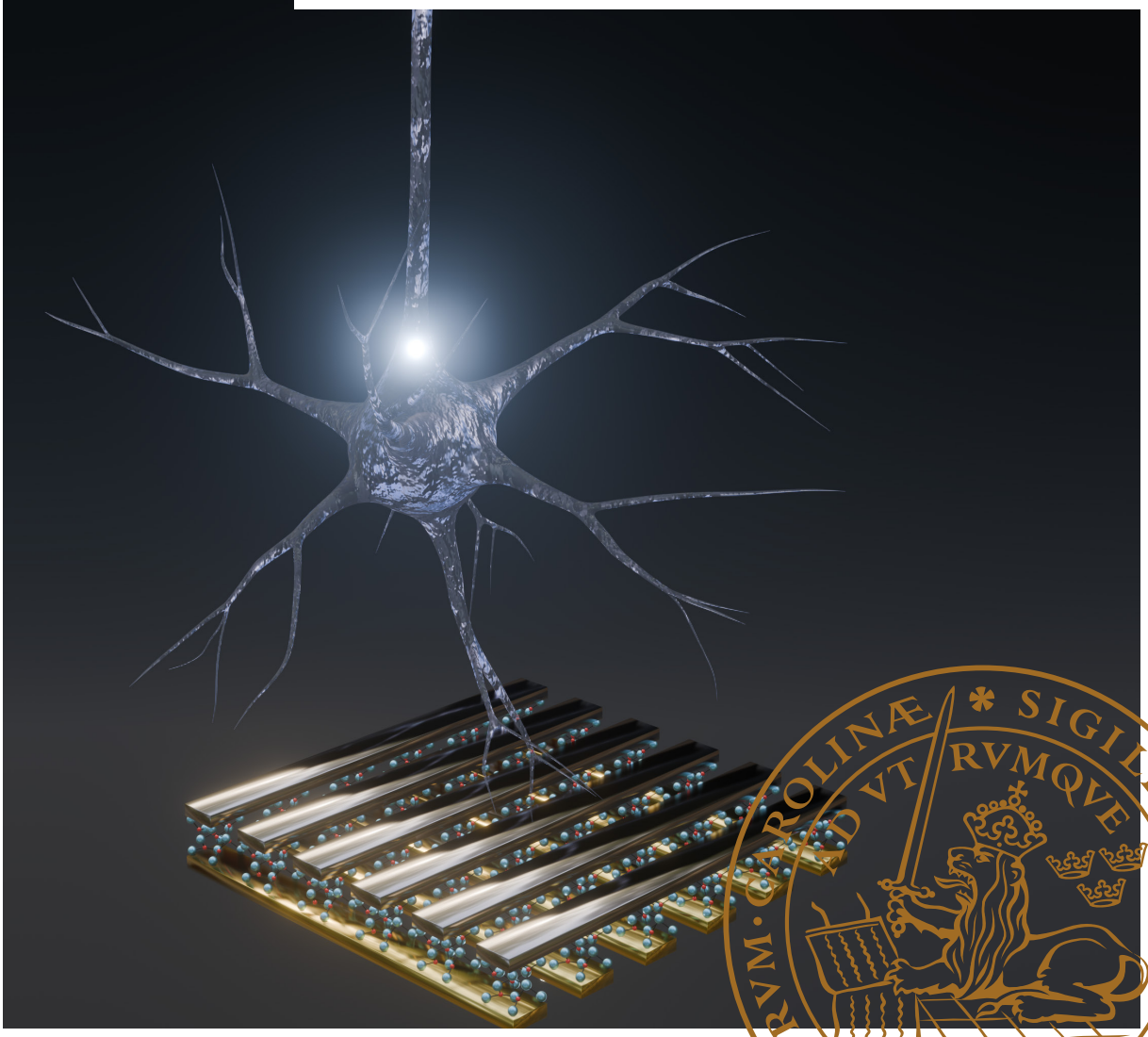

Ferroelectric Memristors - Materials, Interfaces and Applications

Doctoral Thesis

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Lund, March 2024

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Series of Licentiate and Doctoral Theses
ISSN 1654-790X, No. 168
ISBN 978-91-8039-978-4 (printed)
ISBN 978-91-8039-979-1 (digital)

This thesis is typeset using LaTeX 2_ε.

Frontispiece: A biological neuron utilizing a crossbar array of $Hf_xZr_{1-x}O_2$ ferroelectric tunnel junction memristors as its synapse to transmit electrical signals.

Printed by Tryckeriet i E-huset, Lund University, Lund, Sweden.

With gratitude and devotion to those whose influence has defined my character.

Abstract

The backbone of modern computing systems rely on two key things: logic and memory, and while computing power has seen tremendous advancements through scaling of the fundamental building block – the transistor, memory access hasn't evolved as rapidly, leading to significant memory-bound systems. Additionally, the rapid evolution of machine learning and deep neural network (DNN) applications, has exposed the fundamental limitations of the traditional von Neumann computing architecture, due to its heavy reliance on memory access. The physical separation between the computing unit and the memory in von Neumann architectures is limiting performance and energy efficiency. A promising solution to address these challenges is the development of emerging non-volatile memory technologies that provide significant scaling and integration possibilities, fast switching speeds, and highly energy-efficient operations. Additionally, by integrating "memory resistors" (memristors) in large crossbar arrays, the computation can take place in-memory which can resolve the bottleneck in traditional von Neumann architectures.

This thesis investigates the implementation of ferroelectric HfO_2 in ferroelectric tunnel junctions (FTJs) and ferroelectric field effect transistors (FeFETs) as potential candidates for emerging non-volatile memories and memristors.

Initially, the thesis focuses on the integration of ferroelectric HfO_2 onto the high mobility III-V semiconductor InAs for the fabrication of metal-oxide-semiconductor (MOS) capacitors. Moreover, optimization of the processing conditions on the critical interface between the semiconductor and high-k oxide is extensively studied using both electrical characterization and syn-

chrotron radiation techniques. After optimization of the annealing treatment and top electrode texturing, the fabrication of vertical InAs nanowire FeFETs is successfully implemented. The FeFET shows encouraging initial results with limitations solvable by further process engineering.

The fabrication of metal-insulator-metal (MIM) capacitors with a tungsten (W) top electrode enables ferroelectricity in $Hf_xZr_{1-x}O_2$ films down to 3.2 nm thickness. However, achieving ferroelectric properties in ultra-thin films requires an annealing temperature above the thermal budget for back-end-of-line (BEOL) integration. To combat this, nanosecond laser annealing (NLA) is introduced, where an ultrafast laser pulse confines the annealing both spatially and depth-wise. Using NLA, we crystallize 3.6 nm-thick $Hf_xZr_{1-x}O_2$ films while still being BEOL compatible.

The ability to fabricate thin ferroelectric HfO_2 films opens up for the fabrication of FTJs, however, being constrained to a W top electrode is severely limiting the device design. By introducing the concept of a crystallization electrode (CE) and a metal replacement process, tuning of the FTJ device characteristics is achieved. We also highlight the impact of the post-metallization annealing (PMA) temperature on the tunneling electroresistance ratio (TER) of the FTJ. Despite giving similar ferroelectric properties, the PMA temperature strongly affects the interface quality which is key for FTJ performance.

Partial polarization switching is utilized to achieve multi-state conductance levels in the FTJs, demonstrating its memristive capabilities. The stable state retention and low variability are promising for the realization of in-memory computing using crossbar arrays. Finally, the impact of random telegraph noise (RTN) in ultra-scaled FTJs and the scalability of FTJ crossbar arrays is assessed. The low conductance of FTJ memristors reduces the IR drop, while the self-rectifying current-voltage property relaxes the need for an external selector, results that encourage the realization of FTJ-based in-memory computing accelerators.

Popular Science Summary

Området artificiell intelligens eller AI, har sett en explosionsartad utveckling de senaste åren med digitala verktyg som Chat GPT och Gemini som skapat debatter om betydelsen av intelligens. Dessa verktyg besitter så kallad generativ AI, vilket innebär att dem kan skapa text, skriva kod eller rita bilder utifrån kommando. De snabba framgångarna inom AI har till stor del åstadkommits genom utvecklingen av större och kraftfullare modeller. I takt med att AI modeller blivit mer och mer komplexa har den konventionella "von Neumann"-kretsarkitekturen, som särskiljer minne och beräkningsenhet, medfört betydande begränsningar. "Von Neumann"-arkitekturen bygger på en kontinuerlig utväxling av data mellan minne och beräkningsenhet vilket för stora AI modeller med många parametrar (kallade vikter) som kontinuerligt behöver användas skapar en flaskhals. Chat GPTs senaste modell GPT-4 har 1.8 *Biljoner* vikter och optimerades under 100 dagar på Microsofts superdator med 25 000 Nvidia A100 grafikkort och konsumerade uppskattningsvis 52 GWh (!). Detta motsvarar ca 5000 svenskars årliga elförbrukning eller 10 000 varv runt jorden i en Tesla model 3. Den enorma beräkningskraft och energi som krävs för att optimera AI modeller har blivit en stor utmaning både ur ekonomiska och miljömässiga perspektiv, samtidigt som tillgången till dessa verktyg ökar de socioekonomiska klyftorna i samhället. För att lösa dessa utmaningar krävs ett paradigmskifte med nya innovativa lösningar.

Till skillnad från våra elektroniska komponenter är den biologiska hjärnan fenomenal på att hantera och lagra stora mängder intryck (data) på ett extremt energieffektivt sätt. Med en uppskattad energiförbrukning på ca 20 W är den

i en klass för sig själv. Hjärnan består av ett enormt nätverk av neuroner som är kopplade till varandra med en viss styrka via så kallade synapser, där både minne och beräkning sker på samma ställe. Den på senare tid ökade förståelsen om hur hjärnan fungerar har skapat ett stort intresse och en förhoppning att kretsarkitekturer inspirerade av hjärnan kan lösa "von Neumann"-flaskhalsen och drastiskt minska AI's energikonsumtion.

Denna avhandling fokuserar på utvecklingen av ferroelektriska material för att skapa nya typer av energieffektiva minnen som kan användas för att efterlikna hjärnans funktion i hårdvara, där minne och beräkning är sammankopplat. Ett ferroelektriskt material fungerar som en "elektrisk magnet" med en negativ och en positiv laddning på var sin sida av materialet. Genom att applicera ett elektriskt fält kan dessa laddningar byta plats, en förändring som är bestående även när det elektriska fältet tas bort. Laddningen från det ferroelektriska materialet kan användas för att attrahera eller repellera laddningar i intilliggande material. Beroende på om laddning attraheras eller repelleras kan mängden ström i de omkringliggande materialen gradvis styras. Strömmen beror på hur det elektriska fältet över det ferroelektriska materialet har varierat tidigare vilket skapar en ändringsbar resistor med minne, en så kallad ”memristor”. Minnet i en memristor skapas alltså av skillnaden i dess elektriska motstånd, även kallat resistans, vilket skiljer sig från lagringen av elektrisk laddning i traditionella minnen. Denna skillnad möjliggör mer energieffektiva och snabbare minnen samtidigt som de kan göras ännu mindre vilket ökar mängden data som kan lagras. Dessutom möjliggör styrningen av memristorns resistans att den kan imitera funktionen av en biologisk neuronkoppling i hjärnan där styrkan av kopplingen mellan olika neuroner på motsvarande sätt regleras genom storleken på kopplingens motstånd. Genom att integrera memristorer i stora artificiella neuronnätverk kan strömmen ut ur nätverket styras genom resistansen hos memristorerna i samma nätverk. Detta kan utnyttjas för att ultrasnabbt göra de två viktigaste matematiska operationerna inom AI, vilket kan både drastiskt öka hastigheten och energieffektiviteten för AI-tillämpningar. Denna avhandling bidrar specifikt med att utveckla och implementera ferroelektriska tunnelövergångar och ferroelektriska transistorer som nya minneselement och för nya memristorbaserade kretsarkitekturer. Memristorerna integreras med nya material och geometrier för att möjliggöra så kallade neuromorfa kretsar, inspirerade av hjärnan, med målet om att skapa nästa generations elektronik.

Acknowledgments

"If you want to walk fast, walk alone.
But if you want to walk far, walk together."

Ratan Tata

The journey to earning a PhD is a challenging path marked by numerous highs and lows, encompassing memorable moments, accomplishments, and setbacks. I consider myself fortunate, as my journey has been enriched by remarkable individuals who have supported, inspired, and pushed me. Therefore, expressing my gratitude to those who have stood beside me is an integral part of completing this meaningful endeavor. Firstly, I would like to express my deepest appreciation to my main supervisor **Mattias Borg** for providing (and convincing) me with the opportunity to embark on this journey. Your endless enthusiasm, attention to detail and unprecedented ambition is truly inspiring. Your guidance, support and encouragement over these years have shaped me both as a researcher and a person. For this, I am forever grateful. I would have never thought I would end up here when asking you about a masters thesis on something called "ferroelectrics" at a table in K-space in 2018. Would you?

I would also like to warmly thank my co-supervisor **Lars-Erik Wernersson** for always providing a second opinion and being my most frequent visitor at the probe station. I admire your leadership skills and am grateful for the valuable advice you have given me over the years.

A special thank you to **Anton Persson** who embarked with me on this journey of ferroelectrics. Your constant stream of ideas has been a great inspiration to me, and I always had fun working together. **Hannes Dahlberg** and **André Andersen**, I am grateful for all the laughs and discussions we have had, it has been a pleasure sharing office with you. I have no doubt that the research on ferroelectrics in Lund will make great progress with the two of you steering the ship. **Patrik Olausson** we have followed suit for many years now but here our companionship ends. Thank you for your assistance in developing the process flow for crossbar FTJs. You are the best

nanofabrication engineer I know. **Johannes Svensson** thank you for your undying enthusiasm regarding anything and everything, you are like the oracle one visits for answers. **Heera Menon**, thank you for always listening, your ability to see the positive in things have cheered me up when research was rough.

I also would like to thank Andrea, Lars, Sebastian, Olli-Pekka, Fredrik, Karl-Magnus, Markus, Adam, Stefan, Lasse, Saketh, Zhongyunshen, Marcus, Ben, Philipp, Anette, Louise, Paula, Gautham, Abinaya, Navya, Karthik, Ufuk, Duc, Niklas, Alexandros, Johan, Daniel, Mats and Erik. You have made these years a pleasure and I wish you all the best in your future endeavors. Beyond EIT I would like to thank Yen-po, Zephyr, Megan, Zhihua, Rainer, Anders, Elias, and Jesper from the Physics department for excellent collaborations. I want to express my gratitude towards all the engineers and technicians in the Lund Nano Lab for providing the infrastructure to conduct my research. A special mention to Anders Kvennefors, Alex Den Ouden, Peter Blomqvist, and George Rydemalm for always assisting me when needed. George, are those speakers still for sale?

While it may not always be evident, there exists a life outside of work even for a PhD student, and I am blessed to have great friends who help me disconnect from work in various ways. **Fredrik** thank you for always wanting to play discgolf when I ask, our mulligan rounds at St Hans are some of my most cherished memories. **Mikael** thank you for being a great gym bro and fellow tech nerd. **Fredrik**, **Julia**, **Linus** and **Alfred** thank you for all our board game nights and barbecues. I would be remiss if I did not acknowledge my furry non-human friend who has helped me through this PhD: **Koda**, you are the goodest boy ever. Thanks also to Monster Ultra white which has powered my early mornings and late nights during these years, a sponsorship would be highly appreciated!

Lastly, I want to convey my sincere gratitude to my family whose support, love, and belief have been invaluable during these years. My deepest appreciation to the love of my life whose unwavering support and understanding have been the cornerstone of my journey throughout the completion of this thesis. **Elin** thank you for being my anchor, my muse, and my biggest supporter. I am blessed to have you by my side.

Lund, March 2024

Contents

Preface

This thesis is the culmination of more than five years of work in the division of *Electromagnetics & Nanoelectronics* at the Department of Electrical and Information Technology, Lund University, and investigates the development and integration of ferroelectric hafnium oxide for emerging memory and memristive device implementations. The work was supervised by Associate Professor *Mattias Borg* as the main supervisor and Professor *Lars-Erik Wernersson* as co-supervisor.

STRUCTURE OF THE THESIS

This is a compilation thesis, meaning that it is a collection of research papers with an introductory section providing a summary of the research field comprehensible for aspiring researchers with an M.Sc. degree interested in pursuing similar research. The appended publications in the back, form the main body of the thesis.

- **INTRODUCTION**
  The purpose of the introduction is to offer a wide-ranging and inclusive overview of the published and related research within the field of study. This thesis aims to establish a strong groundwork for individuals with a general background in physics and electronics who wish to delve deeply into the realm of ferroelectric devices. It is assumed that the reader possesses a fundamental understanding of semiconductors, electronics, and material characterization.

- **APPENDICES**

A Fabrication Process
Appendix A provides insight into the fabrication details used within this work.

B Measurement Setups
Appendix B describes the scripting measurement setup using C++.

C Creative Commons
Appendix C holds information regarding copyright licenses for some material used in the thesis.

- **PAPERS**
  The papers forming the main body of the thesis are reproduced in the back and listed in the following section.

INCLUDED PAPERS

The following papers form the main body of this thesis and the respective published or draft versions are appended in the back.

Paper I: A. E. O. Persson, R. Athle, P. Littow, K.-M. Persson, J. Svensson, M. Borg, and L.-E. Wernersson, "Reduced annealing temperature for ferroelectric HZO on InAs with enhanced polarization", *Applied Physics Letters*, vol. 116, pp. 062902, Feb 2020, doi: 10.1063/1.5141403.
► *I co-developed the process flow, co-fabricated the structures, and helped with the measurements and the writing of the paper.*

Paper II: R. Athle, T. Blom, A. Irish, A.E.O. Persson, L.-E. Wernersson, R. Timm and M. Borg, "Improved Endurance of Ferroelectric $Hf_xZr_{1-x}O_2$ Integrated on InAs Using Millisecond Annealing", *Adv. Mater. Interfaces*, vol. 9, no. 27, Sep. 2022, doi: 10.1002/admi.202201038
► *I developed the process and supervised the fabrication, did the electrical measurements, did the analysis,and wrote the paper.*

Paper III: R. Athle, A. E. O. Persson, A. Irish, H. Menon, R. Timm, and M. Borg, "Effects of TiN Top Electrode Texturing on Ferroelectricity in $Hf_{1-x}Zr_xO_2$", *Applied materials & interfaces*, vol. 13, pp. 11089-11095, Feb 2021, doi: 10.1021/acsami.1c01734.
► *I planned the project, fabricated the samples, carried out the electrical and GIXRD measurements and analysis, and wrote the paper.*

Paper IV: R. Athle ,A. E. O. Persson, A. Troian, and M. Borg, "Top Electrode Engineering for Freedom in Design and Implementation of Ferroelectric

Tunnel Junctions Based on $Hf_xZr_{1-x}O_2$", *ACS Applied Electronic Materials*, vol. 4, pp. 1002-1009, Feb 2022, doi: 10.1021/acsaelm.1c01181.

► *I planned the project, developed the process flow, fabricated the samples, did the electrical characterization, the analysis, and wrote the paper.*

Paper V: R. Athle and M. Borg, "Impact of Temperature-Induced Oxide Defects on $Hf_{1-x}Zr_xO_2$ Ferroelectric Tunnel Junction Memristor Performance", *IEEE Transactions on Electron Devices*, vol. 70, no. 3, pp. 1412-1416, March. 2023, doi: 10.1109/TED.2023.3240399.

► *I planned the project, fabricated the samples, carried out the measurements and the analysis, and wrote the paper.*

Paper VI: A. E. O. Persson, Z. Zhu, R. Athle, and L.-E. Wernersson, "Integration of ferroelectric $Hf_xZr_{1-x}O_2$ on Vertical III-V Nanowire Gate-all-around MOSFETs on Silicon", *IEEE Electron Device Letters*, vol. 43, pp. 854-857, May 2022, doi: 10.1109/LED.2022.3171597.

► *I developed the measurement setup and did the endurance measurements, helped with the analysis and the styling and writing of the paper.*

Paper VII: R. Athle, and M. Borg, "Ferroelectric Tunnel Junction for In-Memory Computing Accelerators", *Wiley Advanced Intelligent Systems*, pp. 2300554, Dec 2023, doi: 10.1002/aisy.202300554.

► *I planned the project, fabricated the samples, performed the electrical measurements, the simulations, the analysis, and wrote the paper.*

Paper VIII: R. Athle, M. O. Hill, A. Irish, H. Chen, R. Timm, E. Kristensson, J. Wallentin, and M. Borg, "Ferroelectricity in Ultra-thin HfO_2-based Films by Nanosecond Laser Annealing", *Manuscript Submitted*

► *I planned the project, developed the process flow, did the fabrication, performed the electrical measurements and the analysis, and wrote the paper.*

RELATED WORK

The following publications are not included in the thesis, but summarise related work in which I was involved.

Paper ix: A. E. O. Persson, R. Athle, J. Svensson, M. Borg, and L.-E. Wernersson, "A method for estimating defects in ferroelectric thin film MOSCAPs", *Applied Physics Letters*, vol. 117, pp. 242902, Dec 2020, doi: 10.1063/5.0029210.

► *I co-developed the process flow, helped with the analysis and the writing of the paper.*

Paper x: H. Dahlberg, A. E. O. Persson, R. Athle, and L.-E. Wernersson, "Ferroelectric-Antiferroelectric Transition of $Hf_{1-x}Zr_xO_2$ on Indium Arsenide with Enhanced Ferroelectric Characteristics for $Hf_{0.2}Zr_{0.8}O_2$", *ACS Applied Electronic Materials*, vol. 4, pp. 6357-6363, Dec 2022, doi: 10.1021/acsaelm.2c01483.

► *I co-developed the process flow, and helped with the measurements, the analysis, and the writing of the paper.*

Paper xi: H. Menon, L. Södergren, R. Athle, J .Johansson, M. Steer, I. Thayne and M. Borg, "Improved quality of InSb-on-insulator microstructures by flash annealing into melt", *Nanotechnology*, vol. 32, pp. 165602, Jan 2021, doi: 10.1088/1361-6528/abd656.

► *I did the FIB-lamella for TEM, and helped with the FLA experiments and the writing of the paper.*

Paper xii: H. Menon, N. P. Morgan, C. Hetherington, R. Athle, M. Steer, I. Thayne, A. Fontcuberta i Morral and M. Borg, "Fabrication of Single-Crystalline InSb-on-Insulator by Rapid Melt Growth", *physica status solidi (a)*, vol. 219, pp. 2100467, Feb 2022, doi: 10.1002/pssa.202100467.

► *I did the FIB-lamella for TEM, and helped with the writing of the paper.*

Acronyms and Symbols

Here, important acronyms, abbreviations, and symbols are listed, which are recurring throughout the thesis. Some parameters, which only occur in a narrow context, are intentionally omitted; some parameters are used in more than one way, but the context is always explicitly clarified in the corresponding text. Some (compound) units are provided with prefixes to reflect the most commonly encountered notations in the literature.

ACRONYMS AND ABBREVIATIONS

1T1C	One-transistor, One-capacitor
AC	Alternating current
AFM	Atomic force microscopy
AI	Artifical intelligence
ALD	Atomic layer deposition
ANN	Artifical neural network
BE	Bottom electrode
BEOL	Back end of line
BOE	Buffered oxide etch, a mixture of NH_4F, HF, and H_2O
CMOS	Complementary metal–oxide–semiconductor
CPU	Central processing unit
CV	Capacitance-voltage
DC	Direct current
DNN	Deep neural network

DR	Dynamic range
DRAM	Dynamic random-access memory
eNVM	Emerging non-volatile memory
FeFET	Ferroelectric field-effect transistor
FEOL	Front end of line
FeRAM	Ferroelectric random-access memory
FIB	Focused ion beam
FLA	Flash lamp annealing
FTJ	Ferroelectric tunnel junction
GAA	Gate all around
GIXRD	Grazing incidence X-ray diffraction
HRSMU	High resolution source measure unit
HSQ	Hydrogen silsesquioxane
HZO	Zr-doped HfO_2, $Hf_xZr_{1-x}O_2$
IC	Integrated circuit
IMC	In-memory computing
IMPF	Inelastic mean free path
IR	Interconnect resistance(s)
KAI	Kolmogorov-Avrami-Ishibashi model
MAC	Multiply and accumulate
MIM	Metal insulator metal
MIMCAP	Metal insulator metal capacitor
MLA	Maskless aligner
MOS	Metal oxide semiconductor
MOSCAP	Metal oxide semiconductor capacitor
MOSFET	Metal oxide semiconductor field effect transistor
MOVPE	Metalorganic vapor phase epitaxy
MW	Memory window
NEXAFS	Near edge X-ray absorption fine structure
nid	Non-intentionally doped
NLA	Nanosecond laser annealing
NLS	Nucleation limited switching
PCM	Phase change memory
PFM	Piezoresponse force microscopy

PLD	Pulsed laser deposition
PUND	Positive-Up-Negative-Down
PV	Polarization-voltage
RF	Radio frequency
RRAM	Resistive random-access memory
RT	Room temperature
RTA	Rapid thermal anneal, synonymous with RTP
RTN	Random telegraph noise
RTP	Rapid thermal processing, synonymous with RTA
SEM	Scanning electron microscope
SMU	Source measure unit
SPM	Scanning probe microscopy
SRAM	Static random-access memory
SRAM	Scanning transmission electron microscope
TE	Top electrode
TEM	Transmission electron microscope
TER	Tunnel electroresistance
UV	Ultraviolet
VMM	Vector-matrix-multiplication
WGFMU	Waveform generator module
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction

LATIN SYMBOLS

$\boldsymbol{A}$	m^2	Area
$\mathbf{Al_2O_3}$		Aluminum Oxide
$\boldsymbol{D}$	$\mathrm{C\,m^{-2}}$	Displacement field
$\boldsymbol{E}$	$\mathrm{V\,m^{-1}}$	Electric field
$\boldsymbol{E_c}$	$\mathrm{MV\,cm^{-1}}$	Coercive field
$\boldsymbol{E_F}$	eV	Fermi Level Energy
$\boldsymbol{E_g}$	eV	Band Gap

f	Hz	Frequency
G	S	Conductance
I	A, A	Current
InAs		Indium Arsenide
I_S	A, mA µm^{-1}	Source Current, often normalized by the gate width
k_B		$\approx 1.381 \times 10^{-23}$ kg m^2 K^{-1} s^{-1}, Boltzmann Constant
L_G	m	Gate Length
m_0		$\approx 9.109 \times 10^{-31}$ kg, Electron Rest Mass
P	µC cm^{-2}	Polarization
P_r	µC cm^{-2}	Remanent polarization
Q	C	Charge
q		$\approx 1.602 \times 10^{-19}$ C, Elemental Charge
TDMAHf		Tetrakis(dimethylamido)hafnium
TEMAZr		Tetrakis(ethylmethylamido)zirconium
V_T	V	Threshold Voltage

GREEK SYMBOLS

ε_0	$\approx 8.854 \times 10^{12}$ F m^{-1}, Vacuum permittivity
ε_r	Relative permittivity
κ	Relative Permittivity
λ	Thomas-Fermi sceening length
ϕ	Screening potential
σ	Screening charge surface density
θ	Angle

INTRODUCTION

1

Background

"From the end spring new beginnings"

Pliny the Elder

1.1 MOORE'S LAW IS STALLING

In the realm of semiconductor devices, logic, and memory play pivotal roles, forming the backbone of modern computing systems. The evolution of these devices has traditionally been driven by Moore's Law, a principle that has propelled the industry forward through the downscaling of transistors, supply voltage, and an increase in clock frequency (Figure 1.1). Moore's Law, formulated by Gordon Moore in 1965 [1], postulates that the number of transistors on a microchip would double approximately every two years, leading to increased computing power and performance. However, the relentless pursuit of Moore's Law faces a formidable challenge as the downsizing of transistors approaches its scaling limits. In particular, the gate insulator thickness and operating voltage could no longer be reduced alongside other device dimensions. Increasing issues with quantum mechanical tunneling and an unacceptable trade-off between higher off current or lower switching speed proved difficult to solve. Meanwhile, the continuously improved integration density but modest operation voltage reductions have resulted in escalating power consumption, which, in conjunction with diminishing sizes, presents substantial hurdles in dissipating the generated heat. To combat this, the clock frequency has been limited, and segments of the CPU need to be temporarily deactivated (referred to as "dark silicon") to avert harmful overheating of the

circuit. A challenge partially circumvented by the integration of multiple parallel cores on a single chip.

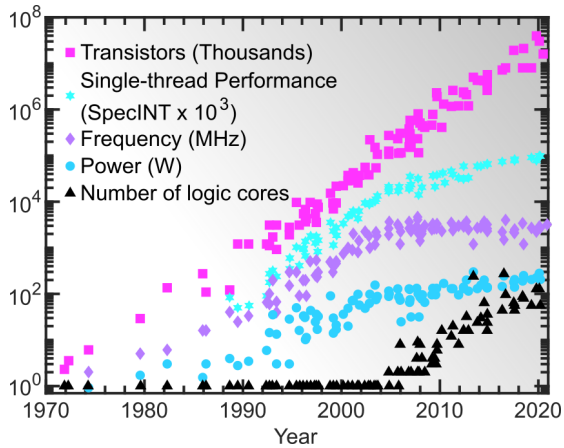

Figure 1.1: Microprocessor trend data, showing the evolution of transistors (squares), single-thread performance (hexagrams), frequency (diamonds), power (circles), and number of logic cores (triangle). Details about the data are found in Appendix C.

The semiconductor industry is confronted with a critical juncture where sustaining Moore's Law in terms of integration density and device switching speed demands innovative solutions. The inability of further voltage scaling has led to a power-constrained scenario, where higher clock frequencies and increased on-chip processor cores are no longer viable options due to unacceptable levels of power consumption and heat generation. Consequently, today's systems find themselves at the crossroads of performance enhancement and power constraints, compromising factors such as battery life in consumer electronics and escalating cooling costs in large data centers.

Traditionally, Flash, SRAM, and DRAM, all based on transistor technology, have been the cornerstone of memory hierarchies in computing systems. However, the limitations of these existing memory technologies, especially SRAM's area-intensive nature and DRAM's non-volatility and scaling challenges, necessitate a reevaluation of the current landscape.

The majority of die real estate in contemporary semiconductor devices is allocated to SRAM memory, a structure consisting of six transistors per bit. To alleviate the spatial constraints, Complementary Field Effect Transistor (CFET) technology allows for stacking P and N type transistors, decreasing the chip's footprint. Despite advancements, SRAM will always be limited to the fabrication limits of the transistor technology. Flash memory, on the

other hand, has been forced to turn to 3D stacking to enhance density, an approach that faces extremely high process complexity, escalating costs and diminishing returns. DRAM, despite being a vital memory component, faces significant hurdles in scaling as the diminishing footprint increases both the access resistance and the process complexity.

The ability of a chip to execute a program is limited to the interaction between the processor and the memory - a problem not solved by scaling. The limitations of traditional memory technologies have led to an overreliance on cache memory (SRAM), occupying a substantial portion of the chip. A trend which eventually will lead to diminishing information throughput. The volatility and poor density of SRAM makes systems dependent on non-volatile storage media which is slow to access and limited by the bandwidth of the data bus.

In addition to the aforementioned challenges faced by traditional memory devices, today's computer architecture, known as the "von Neumann" architecture, further contributes to the limitations of contemporary computing. This architecture, originally designed to facilitate a straightforward sequential programming model, features a physical separation between the processing unit and memory on the chip. Therefore, the existing memory hierarchy, tailored for applications emphasizing data locality, encounters a significant limitation in today's more loosely structured datasets, necessitating frequent off-chip memory access. This data movement introduces latency and energy consumption, particularly when data must travel through a data bus with limited bandwidth to reach the processor. Consequently, integrating every larger amount of memory on chip with the processor will therefore be an ongoing priority to address these challenges. Progress in this regard could be accelerated and sustained by the integration of non-charge based emerging memory devices such as memristors, which will be introduced in the following section.

1.2 THE MEMRISTOR - A NON-CHARGE BASED MEMORY

Memristors are resistive-switching devices endowed with a memory ("memory-resistors"), storing a distinct and stable conductance state depending on the atomic arrangements of a material. Memristors being non-charge based, come with attractive characteristics such as low operating voltage and random access. In this section, the memristor concept will be introduced, followed by an introduction of the currently most promising memristor types.

1.2.1 DEFINITION

The memristor concept was initially introduced by L. Chua in 1971 [2], arising from considerations of symmetry in theoretical electronics, see Fig 1.2. Functioning as a resistor with memory, this theoretical element establishes a complete framework for the four fundamental electronic variables: voltage V, current I, magnetic flux ϕ, and electric charge q. The variables are connected by ideal circuit elements such as resistor, capacitor, and inductor. With the addition of the memristor, the symmetry was completed as the relation between magnetic flux ϕ and electric charge q could be resolved.

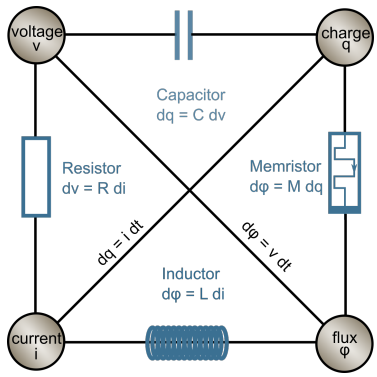

Figure 1.2: Relations between the four fundamental electrical variables: voltage v, electrical current i, magnetic flux ϕ, and electric charge q. The variables are connected by the four circuit elements: resistor, capacitor, memristor, and inductor.

Originally, the equations for a memristor described a non-linear resistor whose resistance was influenced by the input signal history and potentially time-dependent. However, in 1976 Chua et al. extended the work to "memristive systems" with less strict theoretical restrictions [3]. In their general form, these are defined by the following equations:

$$\dot{x} = f(x, u, t), \tag{1.1}$$

$$y = g(x, u, t)u, \tag{1.2}$$

where u and y represent the input and output, respectively, in terms of voltage or current, while x characterizes the internal state of the system. The function g determines the system's resistance R or its conductance G, and the function f, the evolution of the internal system state x. In essence, these equations define a nonlinear resistor, wherein the resistance or conductance

depends on the historical input signals (memory) and may explicitly vary with time t.

It is noteworthy that today's usage of the terms "memristor" or "memristive device" pertains to devices whose resistance (or conductance) can be set and sustained at multiple distinct values. In 2011 L. Chua again broadened the definition to encompass all resistive switching memory devices as well [4].

For this thesis, the term "memristor" is employed to describe all non-volatile resistive switching device implementations, disregarding the precise definition and constraints.

1.2.2 EMERGING MEMRISTOR TYPES

Memristive characteristics have been identified in a diverse range of systems employing various technologies. This section intends to offer a brief survey of several promising, emerging memristor technologies, emphasizing their advantages and current challenges. In this thesis, particular emphasis is placed on ferroelectric devices for memories and memristors that achieve modulation by manipulating the orientation of ferroelectric polarization and will be addressed separately in Chapter 2.

1.2.2.1 Phase-Change Memory - PCM

PCM is a highly mature technology with products already on the market and a clear roadmap for scaling. This, in combination with its CMOS compatibility, makes it highly attractive for memory and neuromorphic computing applications. PCM leverages specific materials that can reversibly switch between amorphous and crystalline phases, which exhibit different electrical resistivity. A PCM device comprises a nanometric volume of this phase-change material between two electrodes as can be seen in Figure 1.3a. To transition from the amorphous to the crystalline state, the PCM must be heated precisely just below its melting point. To reverse the induced crystallization, quenching is performed by heating it above the melting point and rapidly cooling it down. The heat is induced by running an electrical current through the device. The required current is directly proportional to the volume of the switched material.

PCM is increasingly explored for neuromorphic computing, where it can be operated both as a binary non-volatile memory or as a memristor with a continuum of resistance values. [5–8] This enables the implementation of vector-matrix multiplication (VMM) operations, heavily used in both training and inference of deep neural networks (DNNs). PCMs change state at a time scale of tens of nanoseconds, coupled with a great endurance of 10^6-10^9 programming cycles. However, there still persist some fundamental

challenges with the technology [9]. A key challenge associated with logic implementations of PCMs is the large spread in the SET conductance, making evaluation of the programmed state challenging.

For in-memory VMM operations, the limited precision is caused by $1/f$ noise and conductance drift. [9] Drift arises from the structural relaxation in the amorphous phase. Another challenge involves maintaining stoichiometric stability during cycling, as ion migration typically occurs. Additionally, the accumulative behavior in PCM is nonlinear and stochastic, which can be advantageous for stochastic computing but is detrimental for tasks like precise DNN training. It should be noted that some of these challenges can be mitigated through multi-PCM synaptic architectures, however, this comes at the cost of higher integration complexity and reduced density.

Recently, an in-memory compute core, named *HERMES* with arrays of 256 x 256 PCM memristors was integrated into the 14 nm CMOS process node [10]. HERMES achieved a classification accuracy of 98.6% and 88.4% on the Modified National Institute of Standards and Technology (MNIST) [11] and Canadian Institute For Advanced Research (CIFAR-10) databases respectively, showcasing the potential of this technology as a in-memory hardware accelerator.

1.2.2.2 Resistive Random Access Memory - RRAM

Regarding resistive random access memories (RRAMs), there are various categories including filamentary, interfacial, and redox transistor-based devices. For the sake of simplicity, this thesis will exclusively focus on the most established approach within this technology, which is the filamentary-based RRAM, particularly the oxide-based variant that operates based on the migration of oxygen vacancies.

RRAMs are two-terminal devices where a thin oxide layer is sandwiched between the two electrodes, as depicted in Figure 1.3b. Through the use of electric stimuli, the resistance state of the device can be altered by creating or rupturing a conductive filament. The ability to control the filament diameter and rupturing can lead to two or multiple conductance states in the device. The key benefits of RRAMs are the high on/off ratio (>1000), excellent retention (> 10 years), fast reads and writes (< 10 ns), low operation voltage (sub 1 V), and the ability to have both cumulative switching and stochastic intermediate switching. [9]

Although it is easy to understand why there is a large interest in these devices based on the metrics stated above, there are still many issues pending with the technology. The main limitations of RRAM, according to the IRDS2022, are the high switching currents of tens of µA, for devices based on the most mature materials (HfO_x and TaO_x) [12], limiting the integration

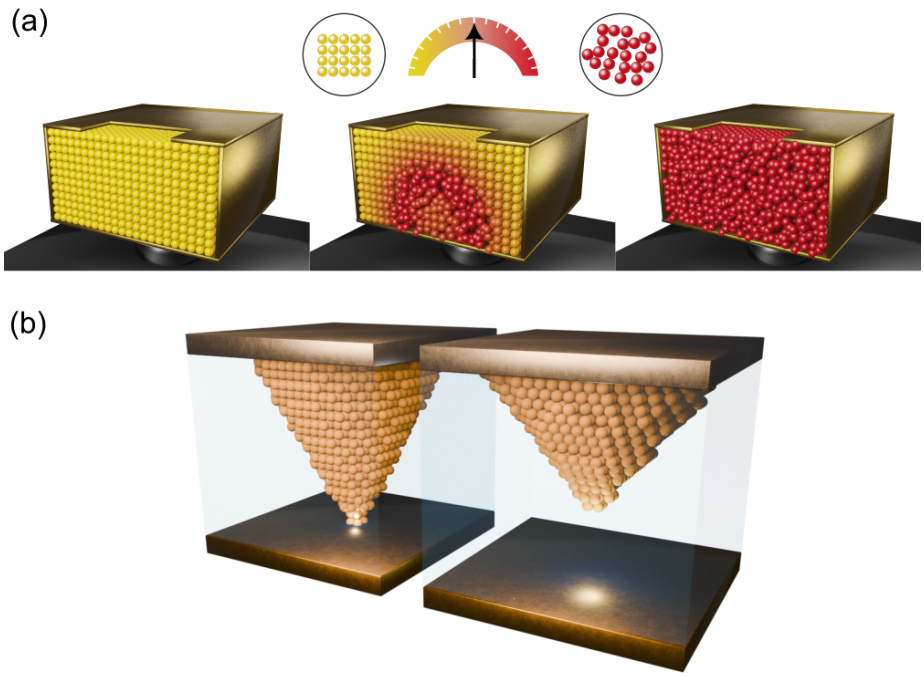

Figure 1.3: Schematic of PCM and RRAM memristor devices. In (a) the crystal structure of the PCM is altered by local heating. (b) RRAM with a complete (left) and ruptured (right) filament.

in large arrays. Additionally, the formation and rupture of the filament is a stochastic process in nature which results in large variations in the switching parameters.

For in-memory computing (IMC) applications, the low device resistance also poses a significant problem for larger arrays due to the voltage drop along the word and bit lines. Moreover, the device and switching variability caused by the stochastic nature of both the forming and operation processes have to be considered [9]. Furthermore, the inherent Joule heating in the device makes the transition time for conductance change very short, making it difficult to control. This typically results in a very abrupt set operation and a low symmetry, which has been demonstrated to be detrimental to the classification performance [13].

Finally, from a system-level integration point of view, the selector or access device required ultimately determines the scalability of the integration which due to the high on-state currents, typically needs to be rather large. Moreover,

the need to "form" the filament for each device, an operation that requires a high voltage ($\sim$5 V) adds additional complexity to the integration.

With that said, there is a lot of effort and resources put into developing this technology and advancing the fundamental understanding of the processes at play in these devices. Recent demonstrations of RRAM-based 1T1R crossbar arrays for inference show a promising future for the technology. [14–17]

1.2.2.3 Ferroelectrics

When it comes to the class of ferroelectric memristors, two device concepts are usually presented: the ferroelectric tunnel junction (FTJ) and the ferroelectric field effect transistor (FeFET). Both of these rely on the spontaneous and reversible polarization of a ferroelectric (FE) material. The polarization can be reversed in the presence of an external electric field, thus ferroelectric memristors are voltage-driven, differentiating them from both PCM and RRAM which are current-driven memristors. This provides a unique potential for low-power non-volatile electronic devices and relaxes the requirements on a potential selector device required for integration. Additionally, ferroelectric switching is a well-behaved switching mechanism, contrary to the stochastic nature of RRAM and PCM. The ferroelectric effect and its use in electronics is described in greater detail in Chapter 2.

1.3 NEUROMORPHIC COMPUTING AND AI

Since the inception of microcircuit development, computer architectures have been fine-tuned to process information in a prearranged and predictable manner. Consequently, the handling of natural data, which often appears in a disorganized and noisy format, proves to be a formidable challenge for these conventional systems. In contrast, the human brain excels at tasks like spotting a familiar face in a crowd or focusing on a speaker's words amidst a conversation. This has spurred many researchers to seek insights into the functioning of the brain with the goal of applying its principles to artificial circuits. This pursuit constitutes the field of neuromorphic computing. This section introduces the basic operation of artificial neural networks and how memristors can be used to mimick the working principle of the brain in hardware.

1.3.1 ARTIFICIAL NEURAL NETWORKS

Artificial neural networks are a branch of machine learning models based on the fundamental principles of biological neural networks found in the brain. In a very simple model, the brain can be described as a large network com-

posed of neurons that are interconnected by synapses. When learning occurs new connections between neurons are created and old related connections are strengthened. In this section, the software implementation of a classical artificial neural network (ANN) used for processing data is described. Note that there are many more types of neural networks implemented for specific tasks that will not be covered here, but the interested reader is referred to the work by Silva et al. [18].

Figure 1.4 displays a basic structure of a simple neural network (NN). It contains various layers that consist of a specific number of nodes. Generally, a neural network is comprised of three types of layers: input layer, hidden layer(s), and output layer. The nodes within one layer can transfer information to the nodes in the next layer, but the transmission strength is determined by the *weight* (w) of each connection. For complex applications, the neural network structure becomes larger with the implementation of multiple hidden layers between the input and output layers. A neural network with several hidden layers is known as a *deep neural network* (DNN).

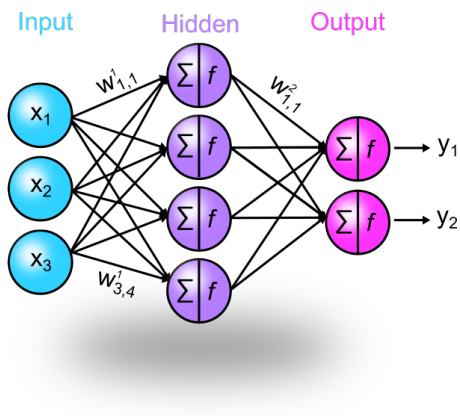

Figure 1.4: Schematic of a simple fully connected neural network with one hidden layer. The neurons between adjacent layers are connected by a certain strength, represented as the weight $w^k_{i,j}$. Each neuron performs a non-linear transformation (f) of its weighted input.

In Figure 1.4 the input layer receives the initial signal $\vec{x}$ for processing, while the output layer carries out the designated task, such as prediction or classification. The true computational core of the network lies in its arbitrary number of hidden layers positioned between the input and output layers. The neurons within the network undergo training using the backpropagation learning algorithm to find a local optima in the weight distribution. These kinds of networks are engineered to approximate any continuous function

and can address problems that aren't linearly separable. They have proved to be highly efficient in tasks like pattern classification, recognition, prediction, and approximation.

1.3.2 NEUROMORPHIC COMPUTING

The rapid growth of machine learning has exposed the limitations of the traditional von Neumann architecture. Complex applications such as simultaneous localization and mapping (SLAM), natural language processing (NLP), chatbots, and virtual assistants rely heavily on DNNs which have grown in size to encompass trillions of trainable parameters. As larger networks (more weights) improve performance, the already significant bottleneck caused by the physical separation of computation and memory hampers progress within this field.

In contrast to the von Neumann architecture, neuromorphic computing seeks to physically merge memory and logic functions into the same device (in-memory computing, IMC), emulating the architecture and function of the human brain and has emerged as a potential solution to this bottleneck. Figure 1.5a illustrates one type of IMC implementation, specifically the memristor crossbar array, in which the memristor devices provide programmable conductance states. This particular configuration holds promise for accelerating fundamental and abundant operations in neural network training and inference, such as vector-matrix multiplication (VMM) and multiply and accumulate (MAC) tasks. In such a crossbar arrangement, the process of "accumulation" is accomplished by applying Kirchhoff's law, wherein the currents originating from different word lines are combined at each bit-line. On the other hand, the process of "multiplication" is typically achieved using Ohm's law ($I = G \cdot V$), with I being the current, G being conductance, and V the voltage amplitude. However, this implementation requires that G is a constant with respect to voltage, i.e. an ohmic current-voltage (I-V) relationship, which is uncommon among memristors, typically only occurring in the high conductance range, resulting in undesirably high current levels.

As an alternative for non-linear memristors, a commonly employed implementation, seen in Figure 1.5b, encodes the input x_i in the voltage pulse length t_n using a constant amplitude V_0. The resulting added charge, Q, on the bitline is then measured by current integration and used as the result of the MAC operation. By maintaining a constant amplitude, a linear relationship between Q and t_n can be established as $Q = V_0 G(V_0) \cdot t_n$, despite a voltage-dependent conductance. In this way, the memristor crossbar array offers extreme parallelism which can lead to substantial energy savings and improved performance for VMM and MAC tasks.

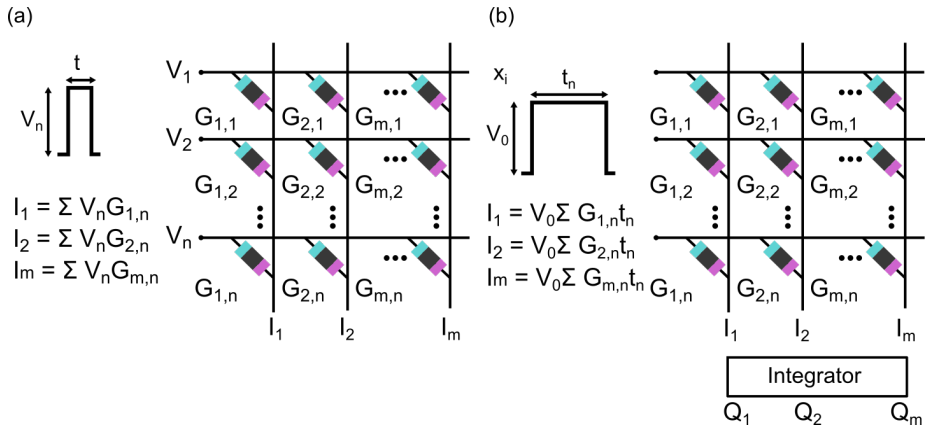

Figure 1.5: Memristor crossbar array implementation, where each bit line and word line is connected through a memristor. (a) Input encoding in amplitude V_n and (b) input encoding in the pulse width t_n.

1.3.2.1 Memristor Requirements for Implementation

Within this segment, we will discuss the essential attributes of memristors crucial for effective integration into hardware accelerators for IMC. The requisites for IMC and applications involving multilevel storage share numerous similarities, and these criteria draw heavily from the insights presented by Shimeng Yu in reference [19]. Nevertheless, it is imperative to recognize that a significant portion of these metrics depends on the specific requirements of particular applications, which can vary based on factors such as online versus offline training and the scale of the considered dataset.

Device size: The large-scale integration of neural networks requires a compact synaptic device with a small device footprint. Therefore, resistive synaptic devices with scalability down to a sub-10-nm regime are preferred. Ultimately, a two-terminal eNVM device that is compatible with the crossbar array architecture and can be integrated in 3-D, should be the target for future research.

Multilevel States: In general, more multilevel states could be translated into a better learning capability, denser storage capability, and improved neural network robustness. However, this requirement is strongly application-dependent, as not all models require the same precision. In general, 100 different conductance states in the memristor is desirable as this would allow a weight change as small as 1%. Additionally, recent studies indicate that binary synaptic devices, when coupled with stochastic weight updates,

may offer comparable performance to analog synapses for some simpler implementations [19, 20].

Dynamic Range: Dynamic range is defined as the on/off ratio between the maximum conductance and minimum conductance. The larger the dynamic range is, the better the mapping capability of the weights in the algorithms to the conductance in the devices, because the weights in the algorithms are typically normalized within a range (e.g., between 0 and 1). A large dynamic range yields a large separation between the states which makes the system more resistant to noise. Considering the power consumption for parallel reading of large-scale systems (e.g. 512 x 512 or larger), the desired conductance range of a single device could be between 1 nS - 1 µS, as the maximum column current would be limited to several hundreds of µA to allow for practical circuit design [19].

Asymmetry and Linearity in Weight update: Ideally, there should be a linear and symmetric relationship between device conductance and the number of programming pulses to accurately map weights to conductance. Asymmetry/nonlinearity is undesired as the change in the weight Δw depends on the current weight w, meaning that there is a history dependence on the weight update. This becomes highly impractical as the weight update must be mapped according to the nonlinear and asymmetric conductance function of the memristor. However, real-world synaptic devices do usually exhibit nonlinearity in weight updates, resulting in asymmetry. This nonlinearity and asymmetry can lead to a loss of learning accuracy. Various strategies, such as using pulse pairs or nonidentical pulses, can be employed to improve linearity, but these approaches may be impractical for on-chip implementations due to calibration challenges. It's worth noting that weight update nonlinearity/asymmetry primarily impacts online training, as opposed to offline training where iterative programming with write-verify techniques can mitigate this issue [19].

Programming Energy Consumption: The estimated energy consumption per synaptic event is around $\sim$1-10 fJ in biological synapses. Whereas most memristors today exhibit programming energy around 100 fJ - 100 pJ. Therefore, further effort is required to lower the energy consumption. One promising approach to achieve this is to improve the programming speed down to the $\sim$ns regime, as the programming energy E is directly proportional to the pulse length ($E = V \cdot I \cdot t$).

Retention and Endurance: During online training, synaptic weights undergo frequent updates, and the retention of data becomes less critical. However, once training is completed, resistive synaptic devices should act as long-term memory, retaining data for up to ten years at the maximum chip operating temperature (e.g., 85 $^{\circ}$C).

The cycling endurance required for online training depends on the complexity of the task and the number of weight updates required for a specific application. For simpler datasets like the MNIST, an endurance of $\tilde{1}0^4$ would be sufficient whereas for a more challenging dataset such as ImageNet or CIFAR-10, a higher endurance is most likely necessary. However, it's worth noting that endurance is typically evaluated on the device level by fully setting and resetting the device whereas a weight update typically only involves a small incremental change in the conductance. Thus, the application-based endurance is therefore probably significantly higher. Thus, cycling endurance beyond 10^9 is probably not required.

Variability: Evaluating the influence of device-to-device (DtD) and cycle-to-cycle (CtC) variability in conductance updates can be challenging due to their reliance on nonlinearity. In broad strokes, for nonlinear memristors, maintaining low levels of DtD and CtC variation proves advantageous in addressing nonlinearity and enhancing classification performance. However, if this variability becomes too pronounced, it can have an adverse effect. Interestingly, the network appears to exhibit greater resilience and can mitigate the impact of substantial DtD variability. In contrast, even a linear memristor demonstrates heightened sensitivity to CtC variability. The CtC variability also determines the minimum separation required between states to avoid overlapping conductances, ultimately limiting the number of states available within the dynamic range. Therefore, it is crucial to focus on minimizing CtC variability, as this would yield the most substantial performance improvements. [19]

1.3.2.2 State of the Art

In recent years the development of memristor-based hardware accelerators has picked up pace. This section aims to provide a short description of the state of the art for analog in-memory computing systems, at the time of writing.

In 2016 Shafiee et.al. demonstrated ISAAC - A convolutional neural network accelerator with in-situ analog arithmetic in crossbars. This work was one of the first to design and characterize a complete analog accelerator based on crossbar arrays. ISAAC is based on the 28 nm technology node with 2-bit RRAM storage units integrated into crossbar arrays. The demonstration of ISAAC marked a great leap forward in terms of throughput, energy, and computational density compared to the previous state-of-the-art DaDianNao architecture which was based on near-memory computing. [21] This was later in 2017 followed up by the work of Song et.al where PipeLayer was introduced [22], a processing-in-memory (PIM) accelerator specifically for convolutional neural networks (CNNs) that supported both training and test-

ing. PipeLayer, like ISAAC, is based on RRAM in the 28 nm node, however, it uses a precision of 4-bit per cell instead of 2. The suggested architecture in PipeLayer allowed a further improvement in computational efficiency to 1485 GOPS/s/mm^2, a 3.1x improvement over ISAAC. However, this was at the expense of power efficiency which at 142.9 GOPS/s/W is $\sim$0.38x that of ISAAC, which was attributed to the use of only RRAM arrays for data storage instead of using eDRAMs as buffers. Additionally, an interesting comparison with the NVIDIA GTX 1080 was made where a speedup and energy saving of about 42x and 7x respectively were achieved using PipeLayer.

The aforementioned architectures enable the training and inference of high-precision networks, albeit at the expense of power and area consumption. In the case of ISAAC, a substantial portion (58%) of power usage and area (31%) is allocated to the 8-bit analog-to-digital converter (ADC). To address this, several studies have explored lower precision, including binary weight representations [23], although these architectures tend to excel only in specific scenarios and lack general applicability. Nevertheless, the concept of precision reduction through bit-decomposition techniques has shown great promise in significantly enhancing energy efficiency. FELIX [24], a neural network accelerator employing single-bit FeFETs as storage units in the 22 nm technology node, has achieved a notable 12x improvement in energy performance using this approach. However, the use of single-bit FeFETs as memory cells comes with a trade-off, leading to lower area-efficiency performance of FELIX when compared to both ISAAC and PipeLayer.

Numerous intriguing strides have been made in the realm of neuromorphic hardware accelerators, with FELIX standing as a pioneering example based on ferroelectric devices, a technology exhibiting significant potential. Consequently, a key objective of this thesis is to make a meaningful contribution towards the development of neuromorphic accelerators utilizing ferroelectric tunnel junction memristors.

1.4 III-V MATERIALS

With silicon MOSFET scaling approaching its physical limits, the quest for other materials to enable computing system advancements is being explored. According to the IRDS 2022 roadmap [25], III-V materials are mentioned as one of the leading semiconductor materials to complement Si. III-Vs are compound semiconductors consisting of elements from groups III and V in the periodic table of elements. The main benefit of III-Vs is the high electron mobility [26], which determines the speed at which electrons can travel through the material. Compared to Si, III-Vs have several times higher electron mobility, which makes them suitable for high-frequency electronics,

as higher mobility allows for a more rapid response when varying the gate potential of the transistor.

In this thesis, the development and characterization of ferroelectric HfO_2 onto the highly attractive high-mobility III-V material InAs is explored. In the initial phase, the integration of ferroelectric $Hf_xZr_{1-x}O_2$ on 2D planar InAs was pursued as a crucial step towards the realization of a III-V nanowire ferroelectric field effect transistor. III-V nanowire devices exhibit compelling features, including outstanding carrier transport, effective electrostatic control facilitated by the gate-all-around (GAA) geometry, and vertical implementation that separates the footprint from the channel and contact length, allowing for dense integration.

2

Ferroelectric Materials and Memories

"I haven't failed. I have just found 10,000 ways that won't work."

Thomas Edison

FERROELECTRIC materials belong to the class of dielectric materials and is characterized by its spontaneous electric polarization that can be reversed by the application of an external electric field. The spontaneous polarization present in these materials stems from the breaking of symmetry in the crystal structure along a unique axis, specifically, a non-centrosymmetric lattice. The name "ferroelectric" is inspired by the magnetic counterpart, the ferromagnetic, due to their similar hysteric behavior. The first reported demonstration of ferroelectricity was in Rochelle salt by Joseph Valasek in 1920, who could experimentally demonstrate a polarization hysteresis. However, it was the discovery of ferroelectricity in perovskites that captured the interest of researchers due to their superior stability. Although perovskites in many ways provide excellent ferroelectric properties, their poor compatibility with CMOS has stood in the way of integration into electronic applications [27]. The limited switching endurance, sensitivity toward reducing gases like H_2 [28], low polarization in 3D structures [29], extended 600-800°C anneals, and the need for an oxygen barrier halted the integration at the 130 nm technology node [27]. Even so, the work on perovskite ferroelectrics provides fundamental insights and theoretical models, vital for understanding the characteristics of ferroelectric materials.

2.1 FUNDAMENTAL DESCRIPTION OF FERROELECTRICITY

The Ginzburg-Landau-Devonshire (GLD) model is a great place to start describing phase transitions in ferroelectrics as it provides a simple yet powerful model [30]. The model assumes a uni-axial ferroelectric material, where the Gibbs free energy G can be described by a Taylor expansion of G around polarization $P = 0$ as shown in equation 2.1.

$$G = -EP + \frac{\alpha}{2}P^2 + \frac{\beta}{4}P^4 + \frac{\gamma}{6}P^6 + ... \tag{2.1}$$

where E is an external electric field, and α, β and γ are Taylor coefficients. For certain values of the coefficients this equation leads to a G function with local minima away from $P = 0$, which gives rise to bistable states with nonzero polarization, even with $E = 0$, as seen in Figure 2.1. Through the application of an external electric field E the symmetry is broken and one of the states becomes more energetically favorable compared to the other. As the applied external electric field becomes large enough to lower the transition barrier between the states the high-energy state becomes unstable and a transition to the low-energy state will occur. The impact of both temperature and electric field based on this model is depicted in Figure 2.1. It should be noted that all parameters do depend on temperature T, however, for simplicity the temperature dependence is usually reduced only to the α parameter as $\alpha = \alpha_0(T - T_C)$ where T_C is the Curie temperature defined as the thermal limit below which the ferroelectric phase is stable. Above this temperature $G(P)$ will only have a minimum at $P = 0$.

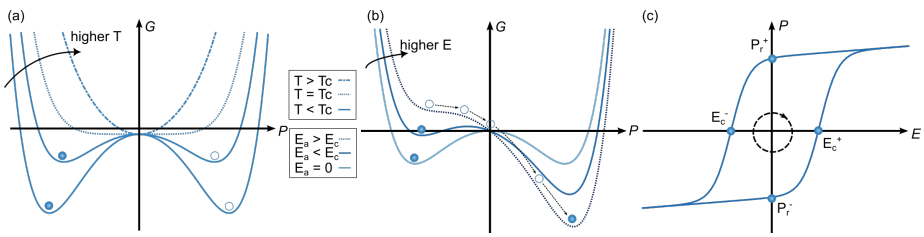

Figure 2.1: Energy potential landscapes based on Landau theory. Impact of temperature (a) and electric field (b) on the free energy of a ferroelectric as a function of the electric polarization. (c) characteristic polarization vs electric field hysteresis curve of a ferroelectric.

From an atomistic point of view, this energy landscape can be visualized as two equally thermodynamically stable configurations of the unit cell. Atoms within this unit cell are then physically moved between two positions provided that the applied electric field is strong enough. This movement of

charged atoms changes the polarization dipole direction of the unit cell. By reversing the electric field polarity the process can be reversed. This movement of atoms (or effectively charge) can be characterized and explains the previously alluded to hysteresis behavior in Figure 2.1c. From the hysteresis curve, key metrics are derived - the remanent polarization P_r and the coercive field E_c. Where P_r represents the macroscopic polarization of the material without the presence of an external electric field, and E_c is the strength of the external electric field required to bring the polarization to zero [31].

While there have been some demonstrations of epitaxial HfO_2-based ferroelectrics [32, 33], the focus of this thesis is on the study of polycrystalline films exhibiting a population of single crystalline grains each with a distinct crystal orientation and one of several crystal phases. Consequently, it is necessary to extend this basic model to include the effect of polycrystallinity. Therefore, a domain is a defined volume within the ferroelectric material displaying a uniform spontaneous polarization. Within this simplified model, domains are presumed to maintain a consistent spontaneous polarization, with abrupt transitions occurring at their boundaries. A commonly employed model for such materials is one resembling the Ising model, as depicted in Figure 2.2a. This model is predicated on two critical assumptions: firstly, that the polarization's magnitude is inherently linked to the material's crystal structure; and secondly, that the crystal orientations, specifically the direction of the polarization axis, are statistically distributed across the population of crystallites. While all crystallites are assumed to share the same value for E_c, only the electric field component parallel to the polarization axis contributes to the switching of remanent the polarization. Consequently, there is a dispersion of effective coercive fields within the material, as depicted in Figure 2.2b, influencing its overall impact on polarization in its surroundings. A switching process that occurs more in-plane necessitates a higher coercive field and makes a lesser contribution to the macroscopic polarization.

While the presented model provides a valuable representation of the conceptualization of the ferroelectric switching phenomena, it is a simplification that does not provide the complete picture in real-world samples. In practical scenarios, factors like the presence of defects, the effects of finite temperatures, and other variables contribute to the non-uniformity of ferroelectric polarization switching [34]. However, for most of this thesis, the simple Ising-based view is sufficient, and additional refinements will be made when it is necessary to understand the results.

2.1.1 ANTIFERROELECTRICITY

Antiferroelectricity, mirroring the analogy between ferroelectricity and ferromagnetism, is the electrical counterpart of antiferromagnetism. In this

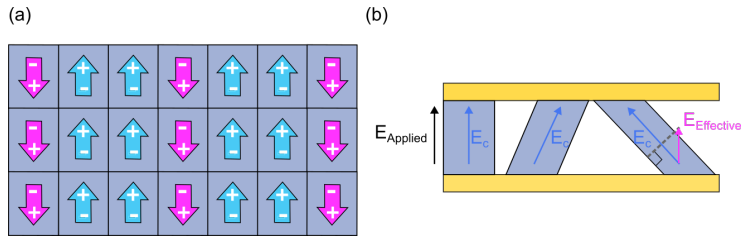

Figure 2.2: An Ising-like model for polycrystalline multidomain thin film ferroelectrics. (a) Electric dipoles inside of the material. The orientation of the crystal impacts the effective electric field across the dipole $E_{Effective}$, changing the magnitude of the applied electric field $E_{Applied}$ required for polarization reversal.

scenario, the electrical dipoles within the material are considered to be oriented in opposite directions when no voltage is applied. This means that adjacent dipoles point in opposing directions, resulting in a net remanent polarization that cancels out to zero. However, at a certain voltage, an energy barrier emerges, leading to a new stable state at high electric fields. Consequently, applying a sufficiently large electric field causes the dipoles to align similarly as in a ferroelectric material. However, once the voltage is removed, the dipoles revert to their antiparallel ground state [35]. Due to the symmetry of the free energy landscape depicted in Fig. 2.3a), these phenomena occur for both negative and positive voltages. Consequently, when plotted on a polarization-voltage graph, this results in the emergence of a double hysteresis loop, as shown in Fig. 2.3b).

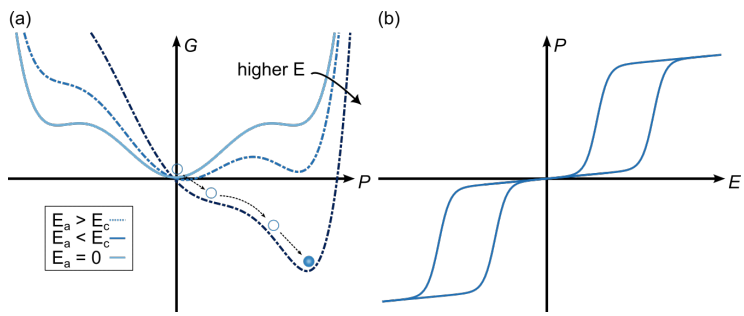

Figure 2.3: Energy potential landscape based on Landau theory for an antiferroelectric material.(a) Impact on the energy landscape for an applied field E_a, (b) characteristic polarization vs electric field hysteresis loop of an antiferroelectric material.

While this chapter separates ferroelectricity and antiferroelectricity into distinct sections, the polycrystalline composition of the materials investigated in this thesis allows for the coexistence of both characteristics within the same material. This phenomenon is commonly termed mixed-phase ferroelectrics [36]. The resultant polarization properties, whether they exhibit ferroelectric (FE), antiferroelectric (AFE), or a combination of both behaviors, are contingent on various factors including doping concentration, electrode selection, thickness, and more. An excellent example of this is $Hf_xZr_{1-x}O_2$ where the Zr doping concentration can determine the either ferroelectric or antiferroelectric(-like) behavior of the material. Consequently, it is crucial to understand the electrical characteristics of both FE and AFE materials [37].

2.2 FERROELECTRIC ELECTRONICS

Since its initial discovery, scientists have been captivated by the potential electronic applications of ferroelectric properties. Of particular interest is their utilization as binary memory in computers. As early as 1952, Dudley Allen Buck, a graduate of MIT, introduced the concept of ferroelectric RAM (FeRAM) [38]. However, it wasn't until the 1990s that FeRAM saw widespread adoption as a memory technology [39]. SEGA, for instance, employed FeRAM to store gameplay data in Sonic the Hedgehog 3. However, the most noteworthy consumer-level application of FeRAM was in the form of the 8 MB memory card for the best-selling video game console of all time, the Sony PlayStation 2 [40].

Although FeRAM saw extensive adoption and success in the early 2000s, its usage declined due to the inadequate CMOS compatibility of perovskite-based ferroelectrics. Issues such as degradation under forming gas annealing [41], uneven deposition, and difficulties in scalability posed significant barriers to the integration [42]. As semiconductor devices underwent rapid and aggressive scaling in accordance with Moore's Law, the limited scalability of perovskite ferroelectrics hindered their continued use in electronics.

Recently, the spotlight has shifted to HfO_2-based fluorite-type ferroelectrics, which have piqued industrial interest. HfO_2 is a well-established oxide material in the semiconductor industry and is fully compatible with CMOS technology. The use of HfO_2 as gate dielectric in silicon CMOS was introduced in 2007 in Intel's 45 nm node to increase the gate capacitance and decrease the leakage current. [43]. Thus, it is no coincidence that the discovery of ferroelectricity in HfO_2 in 2011 [44], a scalable and CMOS-compatible material [45] has generated great interest in this research field. At the time of writing, ferroelectric HfO_2-based materials have been demonstrated down to 1 nm [46, 47]. However, it should be noted that due to the relatively recent

finding of ferroelectricity in HfO_2, the progress in this field is lagging a few years behind other emerging non-volatile memory (eNVM) concepts.

2.2.1 MEMORIES

Despite many potential applications of ferroelectricity in electronics such as steep slope devices [48], reconfigurable electronics [49], the most mature application closest to commercialization, is its use for memories. This section will introduce the working principle of the three most promising technologies.

2.2.1.1 FeRAM

The main application of Ferroelectric random-access memory (FeRAM) is to replace dynamic random-access memory (DRAM) that constitutes the *main memory* (colloquially called the "RAM") of today's devices. FeRAM is structurally very similar to DRAM, therefore, we will introduce the basic working principle of DRAM followed by a discussion regarding the benefits of FeRAM. DRAM is based on a 1T1C architecture - a capacitor as the storage element and an access transistor to control the charge on it. To read or write data, a voltage opens the transistor gate, and data is sensed on the bit line connected to the source of the transistor. If the bit line bias increases or decreases a "1" or "0" was stored on the capacitor. Although DRAM is affordable, fast, and durable, it has a few significant drawbacks. A major limitation of DRAM is the capacitor size as it must be able to store a large enough charge to be sensed, which has lead to vertical integration of the capacitor on top or below the drain contact of the transistor. However, scaling of this process becomes extremely challenging at advanced nodes, which limits the memory capacity as the on-chip footprint cannot be further scaled down. Additionally, the access transistor used to control the charge of the capacitor leaks current. To combat this, periodic refreshing is required to avoid data loss, making it a volatile memory. This refreshing might not seem like a dealbreaker but for the newest DDR5 standard, the specified refresh rate is once per 32 ms which for memories with billions of memory cells, causes significant power draws, above 35% of the total chip power [50, 51].

The FeRAM architecture, depicted in Figure 2.4a, resembles DRAM, but with one key difference, that the insulator in the capacitor is now a ferroelectric film, allowing for non-volatile charge storage. The read and write procedures are similar to DRAM and as the access transistor is opened, a voltage is applied across the ferroelectric capacitor. Then, if polarization reversal occurs, the sensed current will be significantly larger than a non-switched one. The non-volatile nature of FeRAM removes the need for refresh which makes it incredibly power efficient. However, the read operation is still

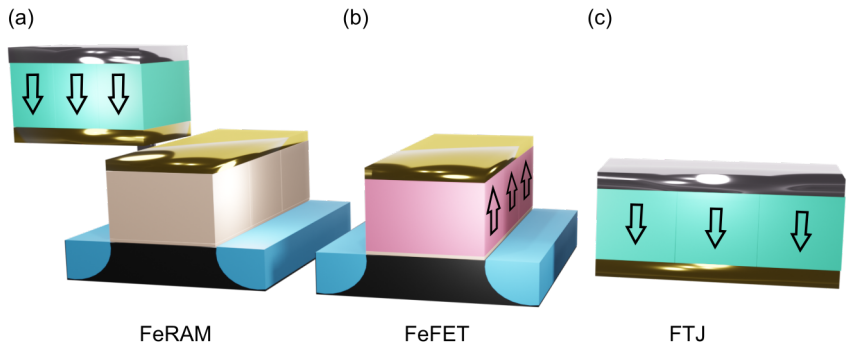

Figure 2.4: Overview figure of the three promising ferroelectric device concepts. (a) FeRAM consisting of 1T-1C where the storage capacitor is a non-volatile ferroelectric. (b) FeFET, where the ferroelectric material is integrated as the gate oxide and the polarization direction can promote either accumulation or depletion in the semiconducting channel, changing the threshold voltage V_t. (c) FTJ, where the ferroelectric is sandwiched between two metal electrodes, and the transmission probability of charge carriers is dependent on the polarization direction of the ferroelectric.

destructive, although very recently a non-destructive read process for FeRAM was demonstrated, focusing on the difference in capacitance between the two polarization states, allowing for read endurance beyond 10^{11} cycles [52]. Moreover, the charge density offered by ferroelectrics enables the integration of smaller capacitors. Despite these glaring advantages, challenges such as limited cycling endurance, and high write voltage still require further improvements before consumer products can be realized [53, 54].

2.2.1.2 FeFETs

As discussed above, FeRAM aims to replace DRAM, and regarding non-volatile storage, similar arguments can be made regarding FeFETs as a replacement for Flash memory. Flash memory is a non-volatile semiconductor storage technology widely used in electronic devices such as USB drives, solid-state drives (SSDs), and memory cards. Its operation is based on a threshold voltage shift to realize two different memory states. It achieves this through the principle of storing charge on a floating gate buried between the

gate electrode and transistor channel. As charges are trapped in the floating gate, the electric field of the gate electrode is screened. This increases the threshold voltage of the transistor. Although flash memory is well established, it suffers from limited endurance (typically < 10^5) and very high write energy consumption ($\sim$1 nJ/bit) [55].

The ferroelectric field effect transistor (FeFET), shown in Figure 2.4b, offers improved endurance and significantly improved energy efficiency and has the potential to replace flash memory in non-volatile applications. Despite its novelty, multiple emerging structures of ferroelectric transistors such as planar FeFET, Fe-FinFET, and gate-all-around FeFETs, have been demonstrated [56,57], even at the foundry level. Despite differences in structure, the fundamental working principle of all is the same: utilizing the ferroelectric polarization surface charge to modulate the electrostatics of the MOSFET. Thus, depending on the polarization state of the ferroelectric, a low-V_T and a high-V_T state can be achieved. The difference in threshold voltage between the two configurations is denoted the "memory window" and is a common benchmark metric of these devices. Recent works demonstrate FeFETs with endurance up to 10^{12} [58], a memory window of 1.5 V, and write energy of 1 fJ/bit.

Finally, another concept has been introduced where instead of integrating the ferroelectric directly in the gate stack of the transistor, a ferroelectric capacitor which shares one of its electrodes with the transistor gate, is connected in series with a traditional non-ferroelectric transistor. This device approach is called a ferroelectric-metal-field-effect-transistor (FeMFET) and allows for reduced programming voltages and generally better reliability when compared to the standard FeFETs [59].

2.2.1.3 FTJs

In addition to the more mature memory technologies just discussed, the ferroelectric tunnel junction (FTJ) seen in Figure 2.4c, is a newer concept holding great promise. FTJs are two-terminal voltage-controlled devices comprised of a thin enough ferroelectric layer (to allow a current to flow through it), sandwiched between two metal electrodes. The basic concept of FTJs was introduced in 1971 by Esaki et al. who named it a "polar switch" [60]. However, due to challenges with realizing thin enough ferroelectric layers to allow sufficient tunneling currents, it took until the early 2000s before the first experimental demonstrations were published [61,62].

This section contains the basic concepts of the electrical characteristics of FTJs. Initially, the main electrical transport mechanisms found in FTJs will be introduced, followed by different phenomena that may cause resistance changes in these structures.

2.2.1.3.1 Electrical transport

The memory state in an FTJ stems from the different transmission probabilities for charge carriers through the ferroelectric barrier, depending on the polarization direction of the ferroelectric, altering the "resistance" through the ferroelectric barrier. Therefore, understanding the electron transport mechanisms present in the FTJ is essential. Luckily, due to the similar materials and geometry, we can draw from the vast knowledge based on the leakage through high-k gate oxides, as well as HfO_x-based RRAMs. The conduction mechanisms present in fluorite-based oxide films can be divided into two categories: interface-limited and bulk-limited mechanisms. Figure 2.5 shows four commonly observed conduction mechanisms: direct tunneling (DT), Fowler-Nordheim tunneling (FNT), thermionic emission (TE), and trap-assisted tunneling (TAT). The first three mechanisms are interface-limited conduction mechanisms while TAT is bulk-limited. Despite FTJs having a very thin ferroelectric, the TAT contribution arises from the significant defect density present in these polycrystalline films. In the study by Hwang et. al [63] it was shown that FNT manifests at high voltage, while DT and TE prevail at low voltage. Thicker films shift the primary transport from DT to TE, with this transition occurring at higher thickness for fluorite-structured FTJs compared to perovskite-based [64], owing to the relatively large band offset (1.5-2.5 eV), between the electrode conduction band and the oxide barrier [63]. Moreover, other bulk-limited current mechanisms such as Ohmic conduction (OC), Poole-Frenkel emission (PF), and space-charge-limited-conduction (SCLC) also exist, however, they rarely dominate the current response in FTJs.

2.2.1.3.2 Resistance Switching in FTJs

According to the model proposed by Zhuravlev, the fundamental working principle of the FTJ depends on the asymmetric screening of the polarization charge at the interfaces of the metal electrodes which leads to a modification of the effective barrier height [65], as schematically depicted in Figure 2.6. As a result, the probability of charge carrier transmission across the barrier is influenced by the polarization direction. This ultimately changes the resistance of the device and depending on the polarization direction of the ferroelectric a high (on) or low (off) conductance G state can be achieved. The corresponding "memory window" of the FTJ is called the tunneling electroresistance ratio (TER) and is defined as $TER = \frac{(G_{on} - G_{off})}{G_{off}}$. In addition, the notation I_{on}/I_{off} or "dynamic range" (DR) is also used to quantify the conductance ratio between the two states.

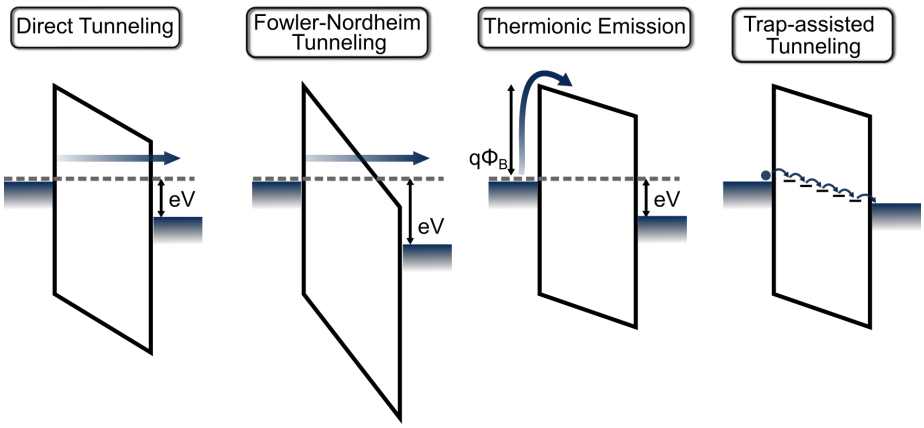

Figure 2.5: Commonly observed conduction mechanisms in thin flourite-based FTJs. Direct tunneling (DT), Fowler-Nordheim tunneling (FNT) and thermionic emission (TE) are interface-limited mechanisms, while trap-assisted tunneling (TAT) is a bulk-limited.

According to the Thomas-Fermi model of screening [66], the screening potential in the metal electrodes as a function of the distance x from the ferroelectric interface is given by

$$\phi_{1,2}(x) = \begin{cases} \frac{\pm\sigma_S\lambda_1}{\epsilon_0\varepsilon_1} e^{\frac{x}{\lambda_1}}, & x \leq 0 \\ \frac{\pm\sigma_S\lambda_2}{\epsilon_0\varepsilon_2} e^{\frac{(d-x)}{\lambda_2}}, & x \geq d, \end{cases} \tag{2.2}$$

where $\lambda_{1,2}$ and $\varepsilon_{1,2}$ are the Thomas-Fermi screening lengths and the ionic permittivities of the electrodes respectively, and $\pm\sigma_S$ is the screening charge surface density. With the assumption of $\phi_1(\infty) = \phi_2(\infty)$, and a condition of potential continuity at the interfaces [64], σ_S can be expressed as

$$\sigma_S = \frac{Pd}{\varepsilon_{stat}(\frac{\lambda_1}{\varepsilon_1} + \frac{\lambda_2}{\varepsilon_2}) + d}, \tag{2.3}$$

where ε_{stat} is the static relative permittivity of the potential barrier. Moreover, the depolarization field inside the ferroelectric is then given by

$$E_d(x) = \frac{P - \sigma_S}{\epsilon_0\varepsilon_{stat}}. \tag{2.4}$$

To determine the transport across the barrier, the energy barrier profiles $E_B(x)$ need to be calculated. Exploiting a trapezoidal barrier, the profile is determined by the interfacial barrier heights, composed of the initial barriers

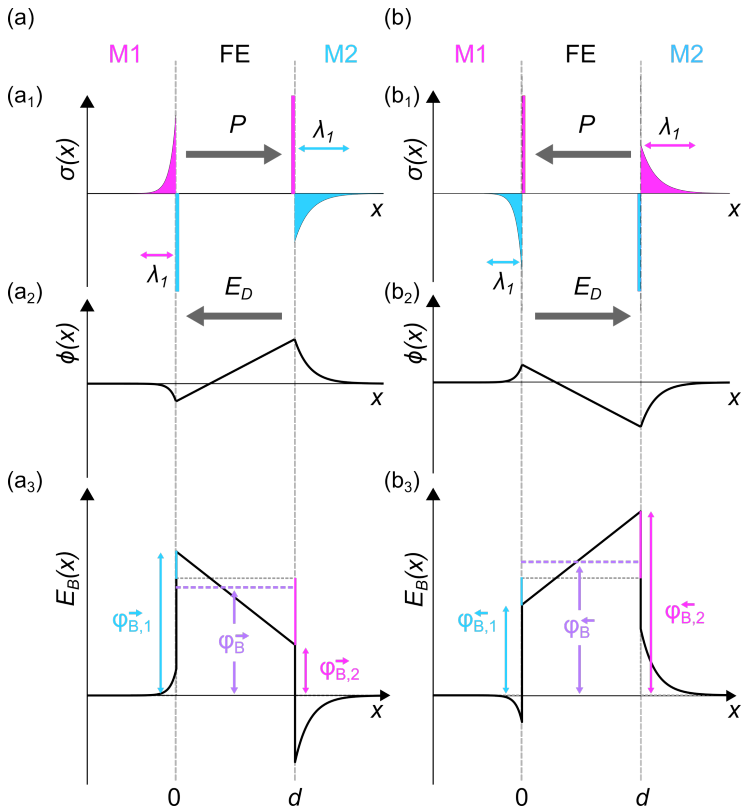

Figure 2.6: Resistance change in FTJs with asymmetric electrodes, ($\lambda_1 < \lambda_2$). (a) Low resistance state (on) and high resistance state (off) in (b), depending on the polarization direction in the ferroelectric. In (a_1,b_1) the charge distribution σ in the layer stack, in (a_2,b_2) the electrostatic potential profiles caused by the incomplete screening of the polarization charges, resulting in a finite depolarization field E_D. Finally, in (a_3,b_3), the resulting energy barrier profiles where the effective barrier height φ_B is modulated, which alters the transmission probability of charge carriers, and thus the tunneling resistance.

$\varphi_{B,1}$ and $\varphi_{B,2}$ and the changes induced by the screening charges $\pm e\phi_{1,2}$ in the metallic electrodes depending on the polarization direction of the ferroelectric:

$$\begin{aligned} \varphi^{\rightarrow}_{B,i} &= \varphi_{B,i} \pm e\phi_i \\ \varphi^{\leftarrow}_{B,i} &= \varphi_{B,i} \mp e\phi_i \end{aligned} \tag{2.5}$$

In general, the effect of asymmetric metal screening lengths on the electroresistance modulation is quite limited (TER = ∼10), a result that can

be combated by replacing one metal electrode with a semiconducting one with much lower carrier density, and fermi level close to the conduction or valence band edge [67]. This allows for utilizing the band bending in the semiconducting electrode to also modulated the width of the tunnel barrier, thus improving the TER dramatically. This has been successfully demonstrated in perovskite FTJs where TER up to 10^9 has been achieved [68].

As discussed above, the major contribution to the resistance change in FTJs is believed to stem from altering the height of the tunneling barrier by screening effects in the electrodes. However, mechanisms such as interface effects, strain effects due to the material's piezoelectric nature, and oxygen vacancy movement have also been suggested to impact the observed resistance change [69–72]. Ultimately, an FTJ device exhibits several of these in addition to ferroelectric effects, which complicates the analysis of the device behavior.

Additionally, there are also demonstrations of double-layer FTJs where a thicker ferroelectric layer (∼7-12 nm) is used together with a higher band gap dielectric material, placed at one of the electrode-ferroelectric interfaces. The idea behind this approach is to decouple the ferroelectric switching from the tunneling layer to allow for independent optimization of the two. [73] Although this approach has been rather successful in yielding a high TER [74–76], it comes at the cost of very low on-current levels, high voltage requirements, and reliability issues caused by the increased depolarization field [77].

Finally, the implementation of anti-ferroelectric tunnel junctions (AFTJ) has been demonstrated [78–80]. The AFTJ requires lower switching voltages to alter the state, which is beneficial for write endurance and power consumption. However, for successful operation, a reproducible work function (WF) offset creating a built-in bias field to shift the hysteresis and pure AFE properties are required.

To summarize, the FTJ is a promising device for non-volatile memory applications offering a small cell size down to $4F^2$ being a two-terminal device. Moreover, fast switching speeds (< 600 ps) [81], high energy-efficiency (1 fJ/bit), and non-destructive read make it an excellent contender to replace DRAM. Yet, the technology's early stage of development leaves several unanswered questions and challenges regarding its scalability, reliability, and read speed, all of which still need evaluation [75].

2.2.2 MEMRISTORS

While the adoption of ferroelectrics in memory applications is nearing commercialization, there has been a substantial surge in interest in memristors for neuromorphic computing in recent years. Additionally, as discussed in

Chapter 1, the criteria for ferroelectric memristors are slightly different from memory applications as well as significantly more applications specific. For instance, in ANN inference applications, the preservation of conductance values is crucial to prevent data loss. Conversely, for online training, the emphasis shifts to endurance, given the frequent updates to weights, allowing for a more relaxed retention requirement. Consequently, this section will present the principles of FeFET and FTJ memristors while outlining their advantages and challenges for use in neuromorphic computing.

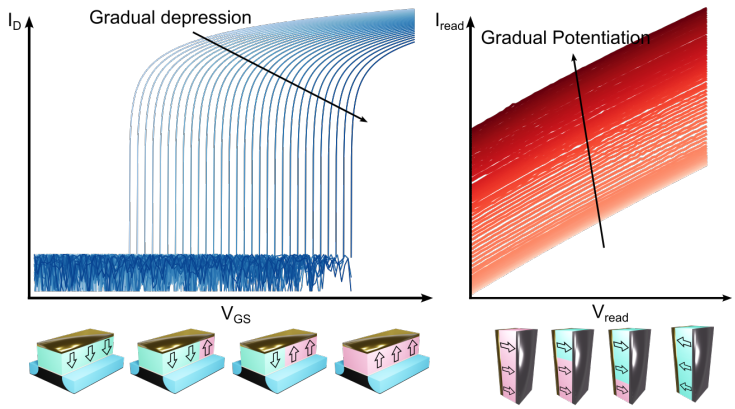

Figure 2.7: Conductance change in FeFET (left) and FTJ (right). The partial polarization switching allows for a gradual change of the V_t or tunneling current in the FeFET and FTJ respectively.

2.2.2.1 FeFET

The FeFET can be used to mimic synaptic behavior, where the strength of the synapse is modulated through the FeFETs conductance. Contrary to the binary memory application, where all the polarization is switched, a partial polarization reversal is utilized. This can be accomplished due to the coercive field distribution present in these devices. By correctly tuning the gate input signal to the FeFET, the ability to gradually change the threshold voltage V_t within the memory window as seen in Figure 2.7, can be achieved. In the ideal case, the V_t can be linearly tuned with a high resolution, and as the programming is field-driven the write operation is highly energy efficient (< fJ). Additionally, FeFET memristors offer a high on/off ratio (typically 10-1000) with demonstrations of more than 128 states [72, 82], fast read (< 10 ns), and write speed ($\sim$ 300 ps) [83] and endurance demonstrated up to 10^{10} write cycles [84]. Despite these excellent characteristics the FeFET memristor also exhibits some challenges, primarily a high device-to-device variability,

large write voltage requirements (∼5 V), and a large footprint owing to its three terminal device structure. Finally, despite the high on-state conductance allowing a fast readout, it does make integration in large crossbar arrays difficult due to the parasitic voltage drop along the bit and word lines.

2.2.2.2 FTJ

In FTJs, the conductance can be tuned as the effective barrier height is gradually altered depending on the fraction of the polarization pointing toward one or the other electrode. Again utilizing the spread in the coercive field of the ferroelectric domains. In prior work by Boyn et al., a combination of PFM and electrical measurements was used to extract the following relation between the conductance of their bismuth ferrite (BFO) FTJs and the fraction of down domains [71].

$$\frac{1}{R} = \frac{1-S}{R_{\uparrow}} + \frac{S}{R_{\downarrow}} \tag{2.6}$$

where R is the resistance of the FTJ, S is the fractional device area of domains with a polarization pointing down, and $R_{\downarrow}$ and $R_{\uparrow}$ are the off and on resistances of the fully switched junction respectively. This simple parallel resistance model could accurately describe the measured junction conductance, suggesting that the observed behavior stems from the nucleation and propagation of the ferroelectric domains [85]. However, it should be noted that this was done on a $Ca_{0.96}Ce_{0.04}MnO_3$ (CCMO) n-type semiconducting bottom electrode where the polarization modulates the carrier concentration of the CCMO, effectively widening the tunneling barrier while simultaneously lowering the effective barrier height.

In general, the FTJ memristor offers great potential due to its small cell size down to $4F^2$ by being a two-terminal device. In addition, the nonlinear current-voltage (I-V) behavior of the FTJ, relaxes the requirement of an external selector device, opening for integration in very large crossbar arrays [86]. In fact, true FTJ crossbar arrays can potentially be fabricated instead of using pseudo-crossbars containing access transistors which significantly increases the processing complexity and on-chip footprint. In recent years, multiple demonstrations of working FTJ memristors have been presented [73, 87–94]. However, the low on-current density of FTJs is considered to be the key challenge for large-scale integration as it causes a slow read-out (> 10us) [54]. An issue that is further worsened as the device area is scaled down. To overcome the low on-current density and allow for device scaling, the switching-layer thickness needs to be thinned down further, while keeping good memristive properties.

2.2.2.3 The size dilemma

The ability to achieve multi-level conductance states in the memristors discussed above requires as mentioned a spread in the coercive field of the ferroelectric domains. Therefore, one can easily understand that depending on the device size, a rich variety of switching dynamics can be observed. Dynamics range from digital switching (as in the memory application), single domain and accumulative switching for a small area device, or gradual switching with many intermediate conductance states for a large area device. Figure 2.8 highlights these different switching dynamics that can be observed in ferroelectric memristors depending on their size.

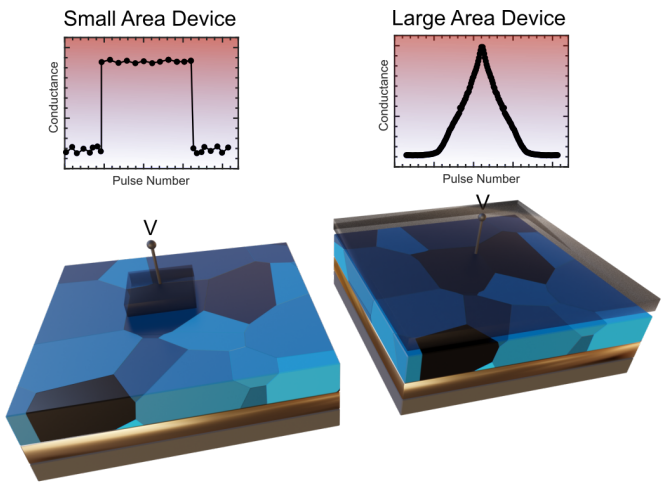

Figure 2.8: The correlation between the switching kinetics and area in ferroelectric devices. Gradual switching can only be achieved in a large-scale device where multiple domains with a stochastic distribution of coercive fields exist. Accumulative stochastic switching dynamics require small-scale devices with few switchable ferroelectric domains.

The ability to alter the switching dynamics offers both flexibility and limitations as it enables the integration of different types of device characteristics for the same material stack, simply by varying the device area. However, it also raises questions about the limits of down-scaling primarily the multi-level devices but also the yield in ultra-scaled single-domain implementations, as the polycrystalline nature of the films inherently induces variations.

2.3 FERROELECTRICITY IN HAFNIA COMPOUNDS

The first published work of both anti- and ferroelectricity in HfO_2 dates back to 2011 and was published by Böscke et al. Ferroelectricity in HfO_2 was initially achieved by doping it with 3.8 mol% of Si, which greatly improved the permittivity of the material [44]. Through rigorous characterization, the presence of the now highly desired $Pca2_1$ orthorhombic crystal phase could be demonstrated. Following this work, several additional papers were published analyzing the material characteristics as well as the first demonstrations of a HfO_2-based FeFET, produced in the 65-nm technology node. One year later, in 2012, integration in the 28 nm node was demonstrated as well as the first demonstration of Zr-doped ferroelectric HfO_2, which since then has become the most popular material choice to study due to its large doping window and varying characteristics [95]. The pioneering studies by Böscke et al. have laid the foundation for extensive research within this field, subsequently gaining large momentum. Notably, Böscke's original work has at the time of writing garnered over 2000 citations, highlighting the vast interest in the discovery of ferroelectricity in HfO_2.

The main focus of this thesis has been devoted to evaluating and understanding the material properties of Zr-doped ferroelectric HfO_2 ($Hf_xZr_{1-x}O_2$, HZO), and thus from this point any mention of ferroelectric HfO_2 will assume HZO, unless specified otherwise.

2.3.1 CRYSTAL STRUCTURE OF HAFNIA COMPOUNDS

Despite the incorporation of HfO_2 as a gate dielectric in CMOS as early as 2007, it is evident that, during this period, the intricate structure and diverse properties of the material were not thoroughly understood. Both bulk crystalline HfO_2 and ZrO_2 have been demonstrated to exist in various polymorphs, including monoclinic (space group: $P2_1/c$), tetragonal (space group: $P4_2/nmc$), and cubic (space group: $Fm\bar{3}m$), all of which are centrosymmetric and incapable of exhibiting ferroelectricity. However, as the film thickness was reduced below 20 nm, for which surface and interface energies dominate, additional crystal phases emerged. In 2014, Huan et al. computed the equilibrium phase diagram of Hafnia to identify low-energy phases at various temperatures and pressures (Figure 2.9a). Two space groups, specifically $Pca2_1$ and $Pmn2_1$, were found to exhibit ferroelectric properties with a slight free energy distinction in comparison to the equilibrium phases (Figure 2.9b). However, ferroelectricity has only been experimentally observed in orthorhombic-III (space group: $Pca2_1$), except for a recent demonstration of ferroelectricity in a polar rhombohedral phase (space group: R3m); however, this phase appears to be exclusive to epitaxially grown HZO [96]. Adhering

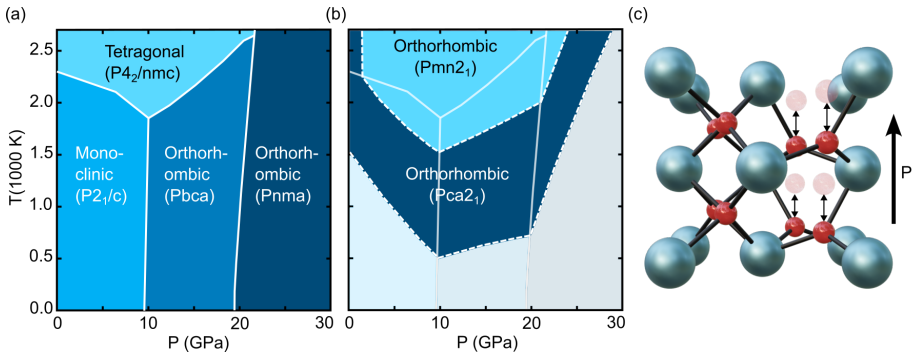

Figure 2.9: (a) Computed equilibrium phase diagram of hafnia, (b) regimes in which the free energy difference between $Pca2_1$ and $Pmn2_1$, and the equilibrium phases are small ($<k_BT/5$). Redrawn from [97]. (c) Crystal structure of the $Pca2_1$ phase with up polarization, lattice parameters from [98].

to the established practices in the research field, this thesis will employ the following nomenclature for the phases: monoclinic (m), tetragonal (t), cubic (c), and orthorhombic (o), with the latter assumed to represent the ferroelectric oIII-phase ($Pca2_1$) unless noted otherwise.

The crystal structure of HfO_2-based ferroelectrics is very different when compared to the traditional perovskite-based ferroelectrics, and a more sophisticated model than what was introduced in section 2 is required to understand the working principle of these fluorite-structured materials. A key difference between perovskite-based and HfO_2-based ferroelectrics is the magnitude of the respective coercive fields, which for the latter is about one order of magnitude larger [99]. This large increase stems from the different crystal structures between the two material groups. For HfO_2-based ferroelectrics, which have a fluorite-structured crystal lattice (Figure 2.9c), the remanent polarization stems from the off-centering of half of the eight oxygen atoms inside the unit cell, instead of a single off-center atom as in the case of perovskites [98]. Additionally, the stronger atomic bonding in the fluorite-structured materials requires a stronger force to break, resulting in an increased coercive field required for polarization reversal, crucial to allow for sufficient memory characteristics even at scaled thicknesses.

2.3.2 INDUCING FERROELECTRICITY IN HFO_2

The complex nature of the crystal structure in combination with the ferroelectric o-phase only being thermodynamically metastable at room temperature and atmospheric pressure, necessitates deliberate efforts in the fabrication process to achieve the desired phase successfully. In addition to this com-

plexity, the as-deposited state of the material using atomic layer deposition, is amorphous, meaning that a separate crystallization process is required. In the following sections, the most commonly implemented approaches to achieve the o-phase in ferroelectric HfO_2 will be discussed.

Annealing

The amorphous as-deposited doped HfO_2 requires crystallization to become ferroelectric. This is typically done using an annealing approach where the sample is heated above its crystallization temperature. Ostwald's law states that thermodynamically metastable phases should nucleate first [100], meaning that crystallization starts with the formation of small regions called nucleation sites of the metastable phases. For HfO_2-based materials, this primarily tends to be the t-phase as it has the lowest surface and interface energy of the different phases. These nucleation sites grow at elevated temperatures and at a certain size and favorable conditions, a transition from t- to o-phase can occur. However, additionally a transition from t- to m-phase is also possible. With the m-phase being the most stable phase in bulk, there is a risk associated with continuous grain growth that the t- to m-phase and even o- to m-phase transitions might occur. The critical nucleation size is heavily dependent on multiple factors but one of the most important comes from the increased impact of strain and interface energy in thin films compared to their bulk counterpart, which reduces the energy barrier for the t- to o-phase transition below that of the t-to-m [101].

As both thermodynamic and kinetic factors are involved, the phase composition of the resulting polycrystalline film depends on both the temperature and the duration that the film is held at that temperature. Most commonly, the time scale that is used is in seconds to tens of seconds, using a traditional rapid thermal annealing system. However, there is an increasing research trend towards both shorter and longer time scales. Flash lamp annealing (FLA) and nanosecond laser annealing (NLA) are two increasingly popular approaches where annealing takes place in the ms [87,102,103] or ns [104,105] time regimes. Both these methods are used in this thesis work and will be covered in Chapter 3. Contrary to these rapid approaches which limit the extent of diffusive processes, furnace anneals on the time scale of tens of minutes to hours, are also reported [106] and have been shown to minimize the wake-up effect otherwise typically present in these materials [107]. Even the cooling rate has an impact on the resulting crystal phases, as it can impact the probability of certain phase transitions. However, when it comes to cooling rates there is still controversy on the best approach where both quick (quenching) and slow cooling have been claimed to be superior [106,108–110].

Doping

While achieving dopant-free ferroelectricity is possible, the general consensus is that doping HfO_2 films represents a crucial method for tuning ferroelectricity. The reason being, that the addition of a dopant reduces the free energy difference between the o-phase and t-phase, relative to the m-phase [111]. The primary role of the dopant is to stabilize the t-phase at the annealing temperature, facilitating its transition into the o-phase during the cooling process [101]. Numerous dopants such as Al, Y, Si, Zr, La, have demonstrated success in inducing ferroelectricity in HfO_2 [112, 113]. However, over time, Zr-doped HfO_2 has emerged as the standard doping choice for back-end-of-line (BEOL) applications due to its wide dopant concentration window and a relatively low annealing temperature required to attain ferroelectricity. For front-end-of-line (FEOL), Si-doped HfO_2 has become the go-to choice as it performs better with the higher annealing temperature used for dopant activation in CMOS logic. The doping concentration window signifies that there exists an optimal doping level at which the maximum remanent polarization is achieved. Deviating from this optimal concentration, either higher or lower, results in a diminished remanent polarization or an antiferroelectric-like behavior [31, 37, 111].

Stress

The electrode both below and on top of the HfO_2 has been demonstrated to mechanically confine the film, influencing its ferroelectricity based on the stress induced by the electrodes. Already in the first paper published by Böscke et al., it was demonstrated that using a capping TiN top electrode to mechanically encapsulate the HfO_2 suppressed the resulting m-phase and instead led to the formation of the o-phase. [44]. Since then, several studies have evaluated the impact of induced strain on the remanent polarization of the ferroelectric. Thickness, texture, and the thermal expansion coefficient of the electrodes have all been suggested to impact the ferroelectric properties, highlighting the crucial role of selecting a proper top electrode [76, 91, 114–116]. Additionally, it has been established that elevated tensile strain in the HfO_2 correlates with increased remanent polarization [117], as it increases the activation energy for the t- to m-phase transition making the t- to o-phase transition a more probable pathway [118].

Oxygen Vacancies

The existence of oxygen vacancies in ferroelectric HfO_2 presents an apparent paradox, acting as a double-edged sword by promoting a robust ferroelectric response in the film while simultaneously giving rise to reliability concerns

[119, 120]. In doped HfO_2 films, these vacancies are generally undesirable as they contribute to the formation of leakage current paths and can pin domains, preventing them from reversing their polarization. Nevertheless, the presence of oxygen vacancies appears indispensable for achieving the orthorhombic phase in undoped HfO_2 [121]. The concentration of oxygen vacancies significantly influences effects like imprint, wake-up, and switching dynamics, which will be elaborated upon in the subsequent section.

Thickness

As previously discussed, the thickness scaling of the HfO_2 played a critical role in achieving ferroelectric properties as the o-phase is not stable in bulk. From a memory and memristor application point of view, a thin film is generally desired. Reduced gate oxide thickness yields improved control due to better coupling between the gate and the channel of a transistor. Additionally, following the trend of semiconductor evolution, scalability is an absolutely fundamental property to gather any commercial interest. Currently, two seperate works by Cheema et al. [47] and Jo et al. [46], respectively indicate ferroelectricity in HfO_2 films down to 1 nm thickness. However, as one can imagine, electrically characterizing these ultra-thin films is quite a challenge, and traditional methods cannot be applied due to the high leakage current present. Instead, the mentioned works apply mostly structural characterization in the form of synchrotron XRD-based measurements such as in-plane GIXRD and 2D grazing incidence wide-angle X-ray scattering (GI-WAXS), TEM precession electron diffraction (PED) and piezoresponse force microscopy (PFM) to support their findings. Additionally, the fabrication of FTJs and negative differential capacitance MOSCAPs and FeFETs in these works show promising, yet rather ambiguous results where oxygen vacancy migration or other ion movement is difficult to rule out. Although the results are promising, a big challenge with scaling the film thickness below ~ 5 nm is the drastically increased annealing temperature required (> 700 °C) for crystallization, making BEOL integration difficult.

Finally, the use of ferroelectric films in power electronics has the opposite challenge. To withstand biases of hundreds of volts in these high-bias applications, the ferroelectric would need to become significantly thicker. However, the increased thickness makes the bulk energy dominate which promotes the non-ferroelectric phases making the o-phase unachievable. However, the use of thin interlayers of Al_2O_3 or similar seems to be a promising approach that enables ferroelectric properties in films up to at least 50 nm [122].

Structure

The prevalent method for depositing ferroelectric HfO_2-based films using Atomic Layer Deposition (ALD) involves an alternating layer strategy. In this approach, the Hf and Zr precursors are alternated in a 1:1 fashion during each cycle until the desired film thickness is achieved. This method results in what is commonly referred to as a "solid-solution" film, as the alternating materials tend to intermix directly during deposition or upon post-deposition annealing to form a uniform layer. However, in recent years, there has been a growing trend in adopting superlattices and nanolaminate structures. In superlattice configurations, a periodic arrangement of two materials is stacked, such as 5:5 or 10:10 Hf:Zr cycles and this stacking is repeated until the desired film thickness is attained. On the other hand, nanolaminates involve combinations like 4:12:4 or 6:12:6 Hf:Zr:Hf as the repeating unit. Although there may be inconsistencies in the nomenclature used in the literature, the terminology described here will be employed in this thesis. Implementations of these advanced growth strategies have demonstrated promising outcomes, showcasing enhancements in ferroelectric properties [47], tunability of coercive fields [123], reduced leakage currents, lower annealing temperatures, and in some instances, the deposition of crystallized films that eliminate the need for subsequent thermal treatments [124, 125]. The use of superlattices and nanolaminate structures in these materials represents a promising avenue to improve the ferroelectric properties beyond the solid-solution approach.

2.3.3 PRESENT CHALLENGES OF FERROELECTRIC HFO_2 INTEGRATION

Despite great progress since its discovery in 2011, there are still certain key non-ideal properties associated with the implementation of ferroelectric HfO_2 that impact the observed behavior. In this section, some of the most commonly discussed challenges will be addressed.

2.3.3.1 Depolarization Field

Due to the polar nature of ferroelectrics, the generation of a depolarization field is inevitable, strongly influencing the characteristics of thin films. The depolarization field arises from uncompensated charges at the interfaces. From device fabrication, the presence of a dielectric layer at the ferroelectric/metal interface, often referred to as a dead layer, is commonly present [99]. This dielectric layer inhibits the screening of the surface charge, because the counter charges in the metal electrode and the surface charge are spatially separate. The remaining unscreened charge cause a depolarization field across the ferroelectric, which reduces the effective polarization and limits the thickness scaling of the ferroelectric as its impact increases for a

thinner film [126–128]. Even in the case of having no dielectric interface layer, a depolarization field will still be present as even metal electrodes will have a non-zero screening length. However, the larger coercive field in HfO_2-based ferroelectrics compared to the traditional perovskite ferroelectrics should enable HfO_2 to withstand higher depolarization fields [77, 99]. The depolarization field is a necessary feature for the barrier height modulation in FTJs, while for FeFETs it is the cause of reduced memory state retention. The understanding and control of depolarization fields in ferroelectrics is therefore key for technological applications.

2.3.3.2 Retention

Retention in ferroelectric devices refers to the ability of a ferroelectric material to maintain its polarization over time, in the absence of an applied electric field. Retention is a crucial characteristic because it determines how long the ferroelectric state can be maintained once the external electric field is removed. Retention performance is influenced by various factors, including material properties, device architecture, and operating conditions [129]. Designing ferroelectric devices with high retention is important for ensuring the reliability and long-term stability of their functionality, particularly in applications where stored information needs to be preserved for extended periods.

2.3.3.3 Wake-up

It is common in HfO_2-based ferroelectrics to observe what is called a "wake-up" effect, which is a gradual increase of the P_r, during voltage cycling. The wake-up effect is typically especially strong during the first 1000 cycles or so. Initially, it was believed that the wake-up effect only stemmed from the redistribution of oxygen vacancies [119,130–132], causing domains in the film to de-pin which results in an elevated P_r. However, recent evidence suggests that the main contribution is a phase transition from the t- to the o-phase or even m-phase to o-phase during voltage cycling, offering an alternative explanation for the observed increase in P_r [133,134]. This explanation is especially attractive as it is congruent with the explanation for antiferroelectricity in Zr-rich $Hf_xZr_{1-x}O_2$. Currently, substantial efforts are underway to mitigate the presence of the wake-up effect in HfO_2-based ferroelectrics by engineering the thermal treatment [107], introducing La dopants [135], and optimizing the deposition conditions.

2.3.3.4 Endurance

The endurance of a ferroelectric material refers to its ability to undergo repeated cycles of polarization switching without significant degradation.

However, it is not uncommon for HfO_2-based ferroelectrics to experience a hard breakdown before any significant degradation of the polarization occurs. Thus the cycles until breakdown is typically what is reported. Reported endurance values for HfO_2 ferroelectrics span a range from 10^4 to 10^{11} cycles. It should however be emphasized that comparison of reported endurance values should be done with care, as the measured endurance is highly frequency and field magnitude dependent. A better metric may in fact be the time until break down which, as demonstrated in the excellent work by Toprasertpong et al., is constant independently of the cycling frequency used [136]. Additionally, as the coercive field is thickness-independent while the breakdown field decreases with thickness, thinner films are expected to have improved endurance compared to thicker films [136].

2.3.3.5 Fatigue

When a ferroelectric material undergoes repeated switching of its polarization under the influence of an external electric field, it can experience a reduction in its ability to maintain a stable and well-defined polarization state. This degradation in performance is known as fatigue. Several mechanisms contribute to fatigue in ferroelectrics. One common factor is the accumulation of defects, such as oxygen vacancies, in the material during the polarization-switching process. Over time, these defects can impede the movement of domain walls (pinning) and hinder the ability of the material to maintain a stable polarization state. As a result, fatigue can lead to a gradual decrease in the remanent polarization and, consequently, affect the reliability and performance of the ferroelectric device.

3

Fabrication of Ferroelectric Thin Films and Memory Devices

This chapter is dedicated to the fabrication process and will cover the methods used in the thesis to realize ferroelectric devices. The intention is to provide an overview but only process steps specifically related to achieving and tuning the ferroelectric properties will be treated in greater depth.

3.1 ATOMIC LAYER DEPOSITION

Ferroelectric HfO_2 can be deposited through various methods, including sputtering, chemical solution deposition (CSD), pulsed laser deposition (PLD), and atomic layer deposition (ALD). Among these, ALD stands out as the most widely adopted approach due to its numerous advantages. The self-limiting nature of ALD and its ability to achieve monolayer-by-monolayer growth provide excellent control over the thickness, roughness, and allow for conformal deposition, particularly crucial for intricate 3D structures with high aspect ratios [137] Given these attributes and the prevalent use of ALD in CMOS processes, it emerges as one of the most important deposition methods for ferroelectric HfO_2-based materials.

In this thesis, the primary focus has been on the development and implementation of HZO deposited through thermal ALD in a Picosun Sunale system, depicted in Figure 3.1a. Figure 3.1b illustrates the fundamental working principle of this method. ALD operates in two "half-cycles" to grow a single atomic layer of the desired material [138]. Each half-cycle involves pulsing and purging steps. During pulsing, the surface chemistry changes either by adsorbing a metal precursor or by oxidizing it. With proper settings to ensure growth within the "ALD window", these steps are self-limiting.

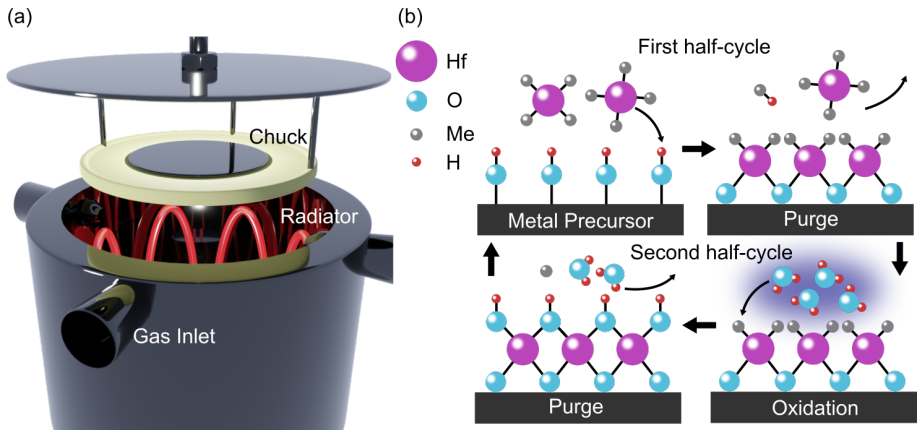

Figure 3.1: Schematic illustration of (a) the Picosun ALD chamber setup, (b) surface reactions during a full ALD cycle of HfO_2, broken up into two half cycles.

Subsequently, a purging step removes excess precursor molecules and/or reaction by-products. Repeating these half-cycles achieves precise monolayer thickness control.

While the fundamental working principle of ALD is straightforward, optimizing the deposition process is a complex endeavor. It necessitates careful consideration of numerous parameters, such as precursor selection, deposition temperature, pulse duration, and reactor conditions, to achieve the desired film properties and uniformity. Furthermore, as layer thicknesses are further reduced to sub 2-3 nm, a more in-depth understanding of the initial growth cycles becomes imperative. Facilities such as MAX IV, offering the capability to monitor surface chemistry in-situ during ALD growth using ambient pressure XPS (APXPS), will play a pivotal role in advancing this understanding [139,140].

3.2 THERMAL PROCESSING

As mentioned earlier in section 2.3.2, the initially deposited HfO_2 film is typically amorphous and necessitates a thermal processing step for crystallization to attain ferroelectric properties. The choice of thermal treatment depends on the intended implementation (BEOL/FEOL) and the substrate, which impose specific limitations on the thermal budget. For instance, certain III-V semiconductors are sensitive to elevated temperatures due to out-diffusion of the group V species. Additionally, the interface between the III-V material

and the HfO_2 experiences oxidation and deterioration, as a result of this diffusion. Furthermore, the concerns are exacerbated when dealing with oxide thicknesses less than 5 nm, as the annealing temperature required for crystallization significantly rises. Given these challenges, considerable efforts have been dedicated to evaluating the thermal processes depicted in Figure 3.2, which cover various time regimes.

3.2.1 FURNACE ANNEALING

Furnace annealing (FA) is one of the simplest approaches to crystallize the as-deposited amorphous HfO_2. Using FA, a slow ramp up to the target temperature ($< 400\ ^\circ C$) is used together with long-duration annealing of multiple hours. Even the cooling step is typically a slow ramp down in temperature.

3.2.2 RAPID THERMAL PROCESSING

Rapid thermal processing/annealing (RTP/RTA) is the most commonly used thermal treatment to induce ferroelectricity in amorphous HfO_2 films, and was the primary choice of annealing in Papers I, III-VII. The process involves a rapid (10-100 $^\circ C/s$) and precisely controlled high-temperature (400-1000 $^\circ C$) treatment for a typical duration of seconds to minutes. Following the annealing step, a rapid cooling approach is implemented to aid the formation of the o-phase by quenching.

The impact of the annealing temperature on the resulting ferroelectric, interfacial, and memristive properties has been evaluated in Papers I, II, and V, and the results are presented in Chapter 5.

3.2.3 MILLISECOND FLASH LAMP ANNEALING

Millisecond flash lamp annealing (FLA) is a thermal processing method that involves subjecting a material to an intense pulsed and broadspectrum light source, typically lasting in the millisecond range, to achieve rapid and surface-confined heating. A preheating temperature significantly below the crystallization temperature is applied coupled with a bright flash from a xenon lamp, which elevates the surface temperature above the crystallization temperature for a brief duration. The brief annealing time of FLA is particularly crucial for III–V materials due to their sensitivity to thermal decomposition. At millisecond time scales, diffusive and dissociative processes are significantly reduced compared to traditional RTP, making FLA a promising approach to combine ferroelectric properties with the advantages of III–V semiconductors. FLA is used in Paper II to improve the endurance of ferroelectric HZO on InAs. However, temperature measurements in an FLA system pose a

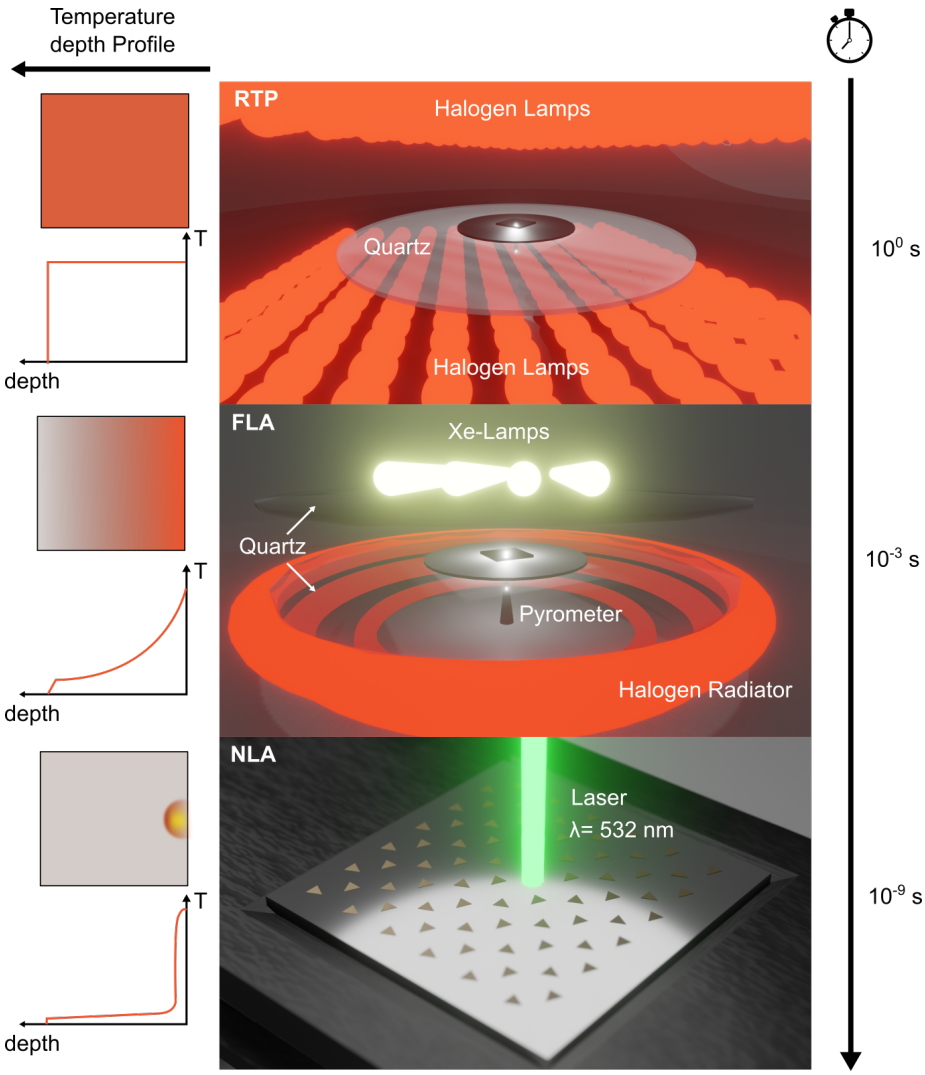

Figure 3.2: Thermal processing methods used to crystallize HfO_2. The treated approaches operate at vastly different time scales, with RTP being the slowest with an anneal duration of tens of seconds. FLA and NLA are pulse-based techniques where the annealing is much more rapid. In FLA a Xenon flash with a pulse length in the millisecond regime is used and in NLA a laser pulse of only a few nanoseconds heats the specimen.

challenge, as the flash pulse primarily heats the surface (approximately 100 µm) of the sample. To estimate the surface temperature, it is necessary to

model the temperature profile through the depth of the sample. Pyrometer measurements of the substrate backside temperature were conducted in this thesis work to validate the model and the assumptions regarding material parameters.

3.2.4 NANOSECOND LASER ANNEALING

Nanosecond laser annealing is a thermal processing technique that utilizes short pulses of laser light, typically lasting in the nanosecond range (10^{-9} seconds), to achieve rapid and controlled heating of a material. It is a technique that has only rarely been employed for the crystallization of ferroelectric HfO_2 [141]. The spatial selectivity of nanosecond laser annealing is advantageous for several reasons. First, it enables precise control over the heat distribution, minimizing the impact on the surrounding materials. Second, the short duration of the laser pulses prevents excessive heat from spreading, reducing the risk of damage to the substrate or adjacent layers.

Similarly to FLA, temperature measurements on this time scale are extremely challenging and one instead has to rely on simulations to estimate the actual surface temperature. Due to the very short pulse length in NLA, the heat is dissipated in approximately the top 50-100 nm of the sample allowing high-temperature annealing even in BEOL without damaging the logic placed in FEOL. Although diffusive processes can be minimized using this approach, the throughput takes a significant hit using NLA. FA, RTP, and FLA all provide similar throughput as the entire sample is annealed simultaneously, however, for NLA a raster scan approach is necessary to anneal wafer-size samples [141]. On the other hand, for research, the localized annealing allows for a large annealing parameter space to be explored on a single sample, for example varying laser pulse energy or the number of pulse repetitions. With similar local characterization methods, a complete process study can be made while keeping the starting material identical. This was done in Paper VIII.

3.3 CRYSTALLIZATION ELECTRODE AND WORK FUNCTION ENGINEERING

As discussed in section 2.3.2, the top electrode plays a crucial role in confining the film during crystallization to induce ferroelectricity. However, a top electrode material that is the most beneficial for crystallization might not necessarily be the most desirable for optimal device operation. To counter this, the concept of top electrode replacement is introduced.

3.3.1 CRYSTALLIZATION ELECTRODE

A tungsten (W) top electrode has proven a suitable choice for crystallizing thin (<5 nm) ferroelectric HfO_2 films due to the large tensile strain it induces. Nevertheless, being confined to a W top electrode would be challenging in the design of devices with high performance. Instead, we advocate for the utilization of a W electrode specifically during the crystallization phase (referred to as the crystallization electrode or CE). Following crystallization, the CE is removed and substituted with a top electrode metal of choice through a metal replacement process. This methodology, used in Papers IV-V, and VII, and also employed by Kobayashi et al. in the development of HfO2-based FTJs [142], allows for the evaluation of device stacks possessing comparable ferroelectric properties. Moreover, it provides superior freedom and control in the device design, enabling the independent optimization of ferroelectricity in HfO_2 and the electronic properties of the top electrode. This separation of optimization parameters facilitates the creation of high-performance devices.

3.3.2 WORK FUNCTION ENGINEERING

A critical consideration when selecting a suitable top electrode in ferroelectric device design is the work function (WF). A work function is defined as the minimum thermodynamic work (energy) required to remove an electron from a solid to a point in the vacuum immediately outside the solid surface. The WF depends on the surface properties of a material and not on its bulk characteristics. Figure 3.3 shows the band diagram of a metal-vacuum-metal system in which the vacuum electrostatic potential ϕ is non-constant due the the difference in work function between the two metals.

The difference in WF between the top and bottom electrodes in a device changes the oxide electrostatic potential, and induces what is known as a built-in field. This built-in field shifts the hysteresis of the ferroelectric, making one polarization state more favorable. This allows for some tuning of the coercive field and has also been successfully implemented to stabilize the sub-loop hysteresis in AFE ZrO_2 enabling non-volatile data storage [143]. The inherent bias field produced by employing electrodes with distinct work functions can be expressed through the following equation:

$$E_{\text{built-in}} = \frac{1}{d \cdot q} \cdot (WF_{\text{TE}} - WF_{\text{BE}}), \tag{3.1}$$

where d represents the thickness of the ferroelectric, q is the elementary charge, and $WF_{\text{TE}}/WF_{\text{BE}}$ are the work function values of the top and bottom electrodes respectively.

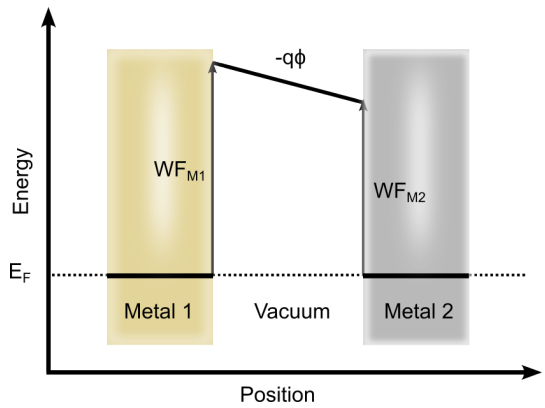

Figure 3.3: Band diagram of a metal-vacuum-metal system where metal 1 (M1, left) has a higher WF than metal 2 (M2, right), which causes a non-constant vacuum electrostatic potential ϕ.

3.4 CAPACITOR STRUCTURES

Capacitor structures offer a quick and simple approach to evaluating ferroelectric properties. Electrical characterization offers systematic and dependable means to swiftly evaluate key parameters such as coercive fields, remanent polarization, switching dynamics, leakage and transient currents, endurance, imprint, and retention for a specific film. The prompt and cost-effective fabrication process allows for a quick assessment of film behavior, offering insights into performance before integration into more sophisticated devices. In principle, all initial testing is done on capacitor structures before integration onto more sophisticated structures for practical application takes place.

3.4.1 MIMCAP

The simplest structures investigated are the metal-insulator-metal capacitors (MIMCAPs) where processing is rather straightforward. It can in the simplest case be completed using just three steps, sputtering of a bottom electrode, ALD growth of the oxide, and finally sputtering of the top electrode through a shadow mask. This process does however in some cases yield rather large uncertainty in the capacitor size. Instead, the implementation of a UV-lithography step and a lift-off process provides a significantly higher consistency of the process. Generally, the MIMCAP processing is carried out using the following six steps:

1. Bottom electrode deposition using sputtering or ALD.

2. ALD of doped HfO_2 film.
3. Top electrode deposition using sputtering or ALD.
4. Thermal treatment to crystallize the HfO_2.
5. Deposition of probing electrodes using e-beam evaporation or sputtering.
6. Capacitor definition by etching away the top electrode material in between devices.

A detailed process flow can be found in the thesis by Persson [144].

3.4.2 MOSCAP

The metal-oxide-semiconductor capacitor (MOSCAP) structure is very similar to the MIMCAP except the bottom metal electrode is exchanged for a semiconductor. The MOSCAPs fabricated in Papers I-III of the thesis, utilize a global bottom electrode of a InAs(100) III-V semiconducting substrate. Furthermore, as the semiconductor-oxide interface plays a significant role in device performance the MOSCAPs have (similar to MIMCAPs) been used for evaluating important properties associated with different process variations. The fundamental understanding achieved through the fabrication of these simple MOSCAP structures has paved the way for the successful integration of ferroelectric HZO in more sophisticated device structures, such as the vertical nanowire FeFET in Paper VI.

3.5 VERTICAL FEFET

Fabrication of the FeFET in Paper VI is a significant step up in complexity from the MIM- and MOSCAPs, and the detailed process flow can be found in appendix Appendix A. The process starts by growing an n^{++}-InAs buffer layer using MOVPE on a silicon substrate. Using EBL, gold seed particles are patterned for the VLS growth of the vertical nanowires (NW) in MOVPE. The first $\sim$200 nm of the NW forms the channel and is non-intentionally doped, the remaining $\sim$300 nm of the NW constitutes a highly doped n^{++} drain segment. During the growth of the drain segment, a thin highly doped shell overgrows the channel region which is removed by cyclic oxidation and etching using ozone and HCL. Then, a Zr-doped HfO_2 film is deposited by thermal ALD at 200 °C followed by DC magnetron sputtering of a 50 nm W gate metal. The gate pad is patterned using UV-lithography and reactive ion etching (RIE), and the gate length is defined by a resist etch-back process using an oxygen plasma followed by RIE. Vias to the source and drain are etched through the HZO using UV-lithography and BOE. At this stage, the HZO is crystallized by annealing with RTP to induce the ferroelectric o-phase.

Finally, a 30 nm Al_2O_3 top spacer is deposited by ALD, and vias to the source, gate, and drain are patterned by UV-lithography and BOE etching. Lastly, the device is contacted by depositing and patterning 10/200 nm Ni/Au.

3.6 FERROELECTRIC TUNNEL JUNCTIONS

The FTJ structures fabricated during this thesis can be classified into two classes based on their size: large-scale and small-scale devices. The large-scale structures have been implemented to facilitate the fundamental working principle of these devices and provide a quick and simple fabrication approach allowing for the development of appropriate electrical characterization methods. The work on large-scale devices, from here on denoted *micro FTJs* have been used towards the end of the thesis to develop the fabrication of small-scale devices, referred to as *nano FTJs*.

3.6.1 MICRO FTJS

The fabrication of micro FTJs is similar to that of MIMCAPs, however with some key exceptions. As the working principle of FTJs depends on the screening length, the interface quality is of utmost importance for device performance. Therefore, additional measures are considered during processing to ensure a high-quality interface between the ferroelectric and the top electrode.

A schematic illustration of the fabrication process is presented in Figure 3.4 and complemented by a detailed process flow in Appendix A. A TiN bottom electrode is deposited by RF magnetron sputtering on a highly doped silicon wafer. Next, a thin sub-5 nm HZO is deposited using ALD. The ALD is followed by the deposition of a 50 nm W crystallization electrode (CE) which induces a tensile strain on the oxide. Then, annealing is performed to crystallize the amorphous as-deposited oxide into the ferroelectric o-phase. As mentioned above, the interface between the oxide and the top electrode determines the screening of polarization charge, and thus the behavior of the FTJ. Therefore, a meticulous removal of the CE is paramount. The removal includes two steps: wet etching by heated H_2O_2, followed by wet etching by heated NH_4OH. Finally, devices were defined by patterning the top electrodes using UV lithography and electron-beam evaporation or DC magnetron sputtering, followed by a lift-off process.

Additionally, for micro FTJs annealed using NLA, a slightly different approach was adopted as annealing using this method is localized to the spot size of the laser (in our case $\sim$30-50 um). This necessitates the alignment of the annealed region and the top electrode position. Thus, for samples exposed to

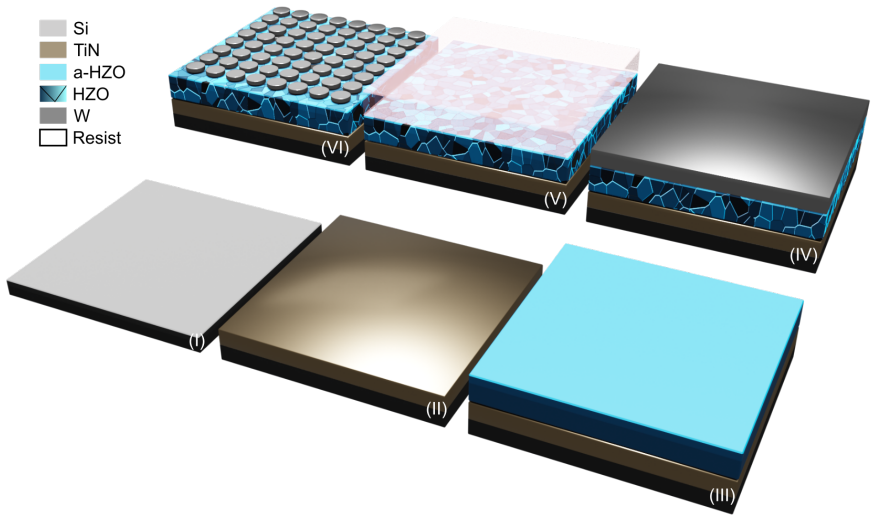

Figure 3.4: Process flow showing some of the key steps for the fabrication of micro FTJs, utilizing a CE and metal replacement process. On the Si substrate (I) a TiN bottom electrode is deposited by sputtering (II), followed by ALD of HZO (III) using alternating cycles of Hf:Zr in a 1:1 ratio. (IV) deposition of the W CE and thermal treatment, which crystallizes the HZO. (V)-(VI) stripping of the CE electrode, followed by UV lithography patterning, sputtering, and a lift-off process to define the fresh W top electrodes.

NLA, an additional patterned metal deposition step was introduced, between the CE deposition and annealing. In this step, a reference coordinate system shown in Figure 3.5 was deposited to position the laser spot with the desired annealing regions on the sample. Post annealing similar steps described above were implemented.

3.6.2 NANO FTJS

To assess the scaling limits of the FTJ, we devised a process flow for fabricating nano FTJs that surpass the constraints of UV lithography systems. This process incorporates a dedicated bottom electrode, a change from the previously used global electrode, which becomes pivotal when expanding device structures from individual units to large crossbar arrays (CBA) essential for hardware-accelerated in-memory computing applications.

Figure 3.6 highlights key steps in the process flow, while a comprehensive description of all fabrication steps can be found in Appendix A. To mitigate parasitic capacitances, fabrication was conducted on a silicon wafer with a 200 nm-thick SiO_2 layer. Additionally, a 300 nm SiN_x layer was deposited

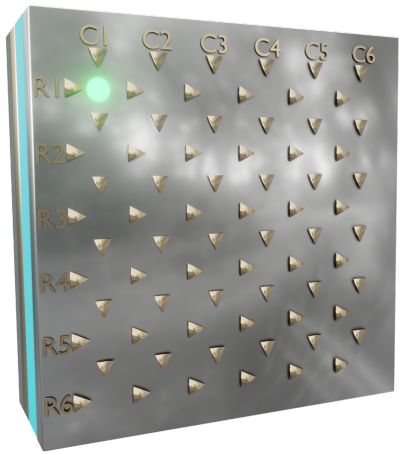

Figure 3.5: Coordinate system used in the NLA samples to align the laser spot (green) with the placement of the top electrode.

using PECVD. Subsequently, 50 nm Pd bottom electrode pads and alignment markers were deposited through a combination of UV lithography, e-beam evaporation, and a lift-off process. Next, a TiN deposition via RF sputtering covered the entire sample surface, which then was capped with a thin (5 nm) SiO_2 layer grown by ALD. To enhance marker visibility in subsequent steps, a UV lithography step was performed to dry etch the SiO_2 and TiN atop the alignment markers.

With markers visible, the definition of bottom electrode arms was executed by exposing AR-N resist in EBL and subsequently dry etching SiO_2 and TiN. Following this, 45 cycles of HZO were deposited using thermal ALD at 200°C, and a 50 nm W crystallization electrode was added through sputtering. As etching crystallized HZO is challenging, removal of HZO deposited on Pd bottom pads was achieved by patterning an etch mask of S1813 using UV lithography and dry etching the W atop the Pd pads, exposing the HZO. The exposed SiO_2/HZO was then etched using BOE. Subsequently, crystallization of the HZO via RTP annealing in a nitrogen environment to achieve the ferroelectric o-phase commenced.

Post annealing, a metal replacement etch, using heated H_2O_2 and NH_4OH, removed the crystallization electrode (CE) and the WO_x at the interface. For top electrode definition, a 50 nm-thick W layer was deposited through sputtering, capped by a 5 nm SiO_2 layer grown by ALD. Again, a similar approach using UV lithography and dry etching was applied to display the alignment markers for the EBL exposure. Using EBL for patterning followed

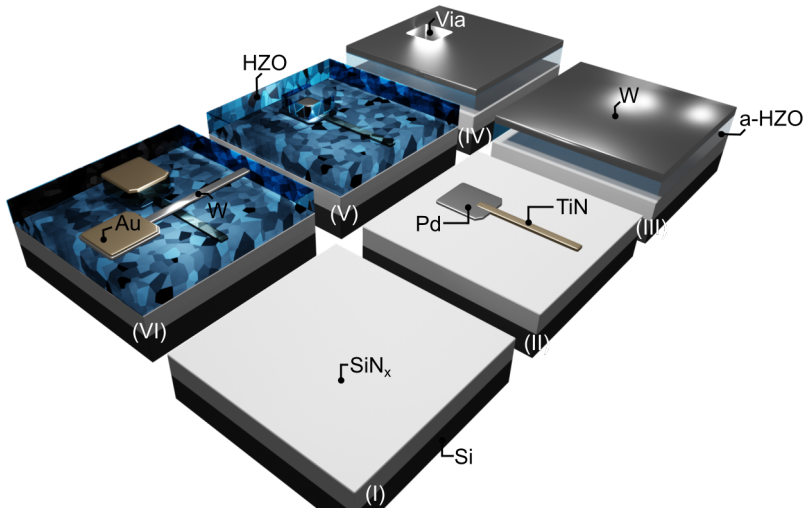

Figure 3.6: Schematic of the process flow to fabricate nano FTJs. (I) SiN_x deposition on a Si substrate, (II) deposition of bottom electrode pad (Pd) and arm, (III) high-k deposition of a-HZO and W as a crystallization electrode (CE), (IV) bottom electrode via definition followed by RTP for crystallization of the a-HZO, (V) stripping of the CE, and (VI) deposition of top electrode arm and pad (W) followed by a probing metal (Au).

by dry etching of SiO_2 and W, the top electrode arms and pads were defined. Finally, Ti/Pd/Au (5/5/200 nm) was patterned and deposited on the top and bottom electrodes using UV lithography, e-beam evaporation, and lift-off, ensuring good probing contact.

3.6.3 FUTURE OUTLOOK

It is crucial to highlight that the process flow outlined above for nano FTJ devices remains compatible with micro FTJs with a simple substitution of EBL steps for UV lithography steps. In the case of micro FTJ devices, the process can be further streamlined by eliminating the two UV lithography steps needed to enhance alignment marker visibility. The step height difference provides sufficient contrast in an optical system, making these additional UV lithography steps unnecessary. Furthermore, the proposed fabrication process opens the possibility for realizing large crossbar array (CBA) structures. Additionally, the design and fabrication of chips for system-level integration become feasible by bonding for use with an external controller, such as a field-programmable array (FPGA), enabling off-chip programming and verification.

4

Characterization of Ferroelectric HfO_2 Thin films and Devices

In this chapter, we will describe essential characterization methods employed throughout the thesis to comprehend the ferroelectric behavior exhibited by the devices. A thorough understanding of material and device properties necessitates the integration of both structural and electrical characterization. Consequently, the chapter will be segmented into these two primary sections, each addressing the most frequently utilized techniques.

4.1 STRUCTURAL CHARACTERIZATION

Assessing and measuring material properties in nanoscale devices can pose a considerable challenge. This section introduces structural characterization methods utilized to acquire a foundational comprehension of surface chemistry and arrangement in ferroelectric devices. It is crucial to highlight that results from a singular method are often ambiguous, underscoring the importance of employing multiple methods to complement the findings.

4.1.1 SCANNING PROBE MICROSCOPY

Scanning probe microscopy (SPM) represents a family of high-resolution imaging techniques that revolutionized the field of nanoscale characterization. Unlike traditional microscopy methods, SPM operates by raster-scanning a sharp probe over the sample surface and sensing various interactions to create detailed images.

4.1.1.1 Atomic Force Microscopy

One of the most prominent SPM techniques is atomic force microscopy (AFM), which is a high-resolution imaging technique used to study the surface morphology and properties of materials at the nanoscale. AFM operates based on the principle of measuring forces between a sharp tip and the surface of a sample. The AFM instrument consists of a cantilever with a sharp tip at its end. The tip is brought into proximity with the sample, and as the tip scans across the surface, interactions between the tip and the sample surface cause the cantilever to deflect. This deflection is measured, and the data is used to create detailed images of the sample's topography [145]. Figure 4.1 shows the topography data of PVD-deposited TiN post-annealing, allowing for quantification of the surface roughness.

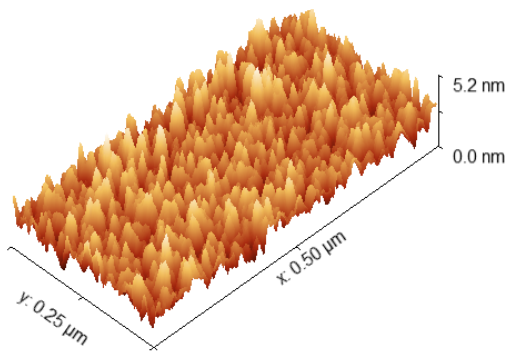

Figure 4.1: AFM topography data of PVD deposited TiN post-annealing.

Unlike other imaging techniques, such as optical microscopy, AFM does not rely on light. Instead, it works by sensing the forces between the tip and the atoms or molecules on the sample surface. This makes AFM particularly powerful for studying materials at atomic and molecular levels.

One of the key advantages of AFM is its exceptional spatial resolution, allowing researchers to visualize features on the order of nanometers. Additionally, AFM can be used under various environmental conditions, including in air, liquid, and even vacuum, making it a versatile tool for studying a wide range of samples, including biological specimens, polymers, and nanomaterials.

4.1.1.2 Piezoresponse Force Microscopy

In addition to traditional imaging, AFM can be used in other modes of operation, for example studying mechanical and electrical material properties. As ferroelectric films are scaled down to just a couple of nanometers, the high leakage current through the film poses a significant challenge for traditional electrical characterization methods. Instead, piezoresponse force microscopy (PFM) provides a promising approach to studying polarization reversal and domain wall motion in ultra-thin ferroelectric films [146–148].

PFM takes advantage of the inverse piezoelectric effect, in which a piezoelectric material will contract or expand in the presence of an external electric field. The working principle of PFM is illustrated in Figure 4.2, where a sharp conductive tip is used to scan the surface of the ferroelectric material. The application of an AC bias to the tip during scanning yields contraction or expansion of the ferroelectric domains which impacts the cantilever deflection and displaces the laser reflection on the detector [148]. The contraction and expansion of domains of a specific polarization orientation will be in phase with the applied electric field whereas domains with the opposite orientation will be 180° out of phase.

PFM allows researchers to visualize and map the distribution of ferroelectric domains, domain walls, and other related properties with nanoscale resolution [146]. This technique is particularly useful for understanding the behavior of ferroelectric materials in electronic devices, sensors, actuators, and other applications where their unique properties are leveraged. However, it must be emphasized that quantitative analysis of the measured PFM signal can be extremely difficult due to the impact of non-piezoelectric contributions and artifacts arising during the measurement [149]. This has led to many non-ferroelectric materials showing "ferroelectric characteristics" in PFM [150]. Thus, the typical process of domain writing to "prove" ferroelectricity using PFM is not sufficient, and correctly looking phase and amplitude curves can be measured in non-ferroelectric samples as well. Electrochemical effects such as charge injection and field-effect charging in combination with physical effects probed by PFM, makes it hard to discern the true nature of the measured signal. Moreover, the presence of electrostatic forces on the cantilever further complicates the interpretation of the data [151]. Due to this very difficult nature of PFM analysis, the method is still not considered a stand-alone proof of ferroelectricity, however, it acts as a complementary technique allowing for spatially resolving electromechanical effects at the nanoscale.

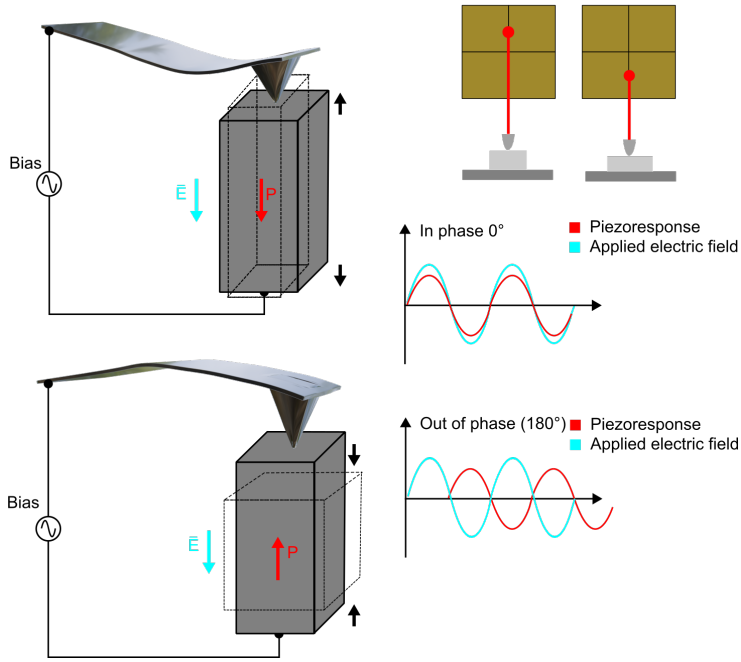

Figure 4.2: Illustration of the operational concept of PFM, leveraging the inverse piezoelectric effect. When an AC bias is administered to the cantilever tip, the ferroelectric material undergoes expansion or contraction, contingent on its polarization orientation. The inverse piezoelectric effect induces a modification in the cantilever deflection, detectable through the displacement of the laser reflection on the detector. The cantilever deflection synchronizes with the applied electric field in domains possessing a specific polarization orientation, while it is 180° out of phase with domains exhibiting the opposite orientation.

4.1.2 X-RAY SPECTROSCOPY METHODS

X-ray photoelectron spectroscopy (XPS), is a powerful analytical technique used to investigate the elemental composition and chemical state of a material's surface. XPS is based on the photoelectric effect, where X-rays are used to eject electrons from the atomic core shells of a material. The kinetic energy of the ejected electrons reflect the binding energy of the core level, which is sensitive to the chemical binding of the atom. The number of ejected electrons with a certain kinetic energy thus provides detailed information about the chemical environment of the elements present in the sample surface, such as the elemental composition, chemical states, and electronic structure of a

material's surface [152]. It is a highly surface-sensitive technique, making it ideal for studying thin films, coatings, and surfaces [152]. In this thesis we have specifically utilized the shifts of core level energies related to the oxidation state in TiN, InAs and HZO. The probing depth is determined by the inelastic mean free path (IMFP) of photoelectrons, which is energy dependent. Traditionally, soft X-rays with energies of 100 eV to 1.5 keV are used which gives an IMFP of 0.4 - 2nm [153]. However, the use of hard X-rays (HAXPES) which uses photon energies of multiple keV, increases the IMFP up to $\sim$10 nm [153], allowing one to probe deeper into the materials. In the analysis of data obtained at such depths, it is important to keep in mind that the signal one obtains carries information from all depths up to the IMFP, not just at the IMFP, which complicates the analysis.

Another X-ray-based technique used during this thesis work is the near-edge X-ray absorption fine structure (NEXAFS). In NEXAFS one studies the X-ray absorption by a material as a function of photon energy. When X-rays are directed at a sample, electrons from inner shells are excited to higher energy levels, causing the absorption of X-ray photons. The absorption spectrum, particularly in the near-edge region, contains fine structure related to transitions to unoccupied states just above the absorption edge [154]. NEXAFS provides insights into the elemental composition, chemical bonding, and electronic structure of a material's surface. It is particularly powerful in characterizing the local coordination and chemical state of specific elements. In Paper III we use NEXAFS to prove the incorporation of interstitial nitrogen (N_2) in the TiN top electrode which appears to improve the endurance of our MOSCAPs.

The use of XPS and NEXAFS during this project has been performed at synchrotron facilities such as MAX IV and Diamond in collaboration with the group of Rainer Timm at the Division of synchrotron radiation research at the Department of Physics at Lund University.

4.1.3 X-RAY DIFFRACTION

One of the most powerful techniques to characterize crystal structures is X-ray diffraction (XRD). X-rays can be generated by the heating of a cathode filament to produce electrons, which are accelerated towards a target material (commonly Cu or Mo) by an electric field. Electrons with sufficient energy to dislodge inner shell electrons of the target material generate characteristic X-ray spectra with a specific wavelength determined by the target material. Filtering and collimation of the X-ray spectra is utilized to produce monochromatic X-rays which are required for diffraction. The Bruker D8 Discovery tool mostly used in this thesis has a Cu target with CuKα radiation = 1.5418 Å, and has been used to study the crystallography of HZO in Papers I-III.

In crystals, a highly ordered atomic structure exists, meaning that X-rays which satisfy the Bragg condition:

$$n\lambda = 2d \sin\theta, \tag{4.1}$$

where λ is the wavelength, θ the incidence (and reflection) angle, d the lattice spacing, and n the diffraction order, will generate constructive interference, producing a peak in the signal intensity [155]. In all other cases, there will be destructive interference and, as a result, a low intensity will be measured. A common measurement procedure for single crystals utilizes the Bragg condition and sweeps the incidence angle at an angle θ and the detector collects the diffracted signal at a swept angle of 2θ, thus keeping the diffraction vector equal to the normal of the sample meaning that crystal planes parallel to the sample surface are probed. This is called the Bragg-Brentano geometry.

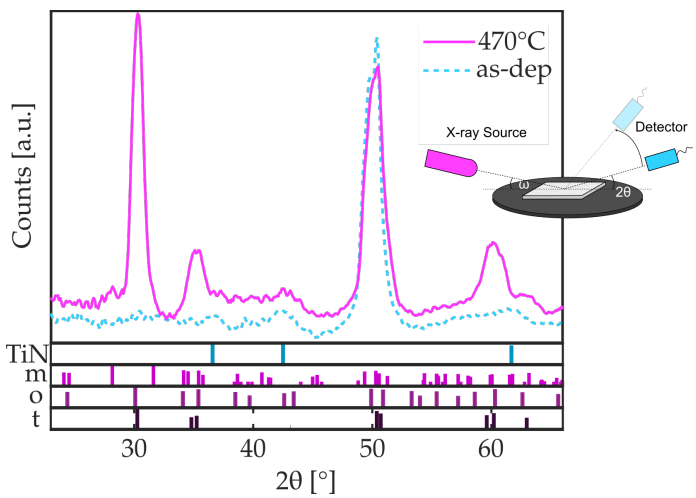

Figure 4.3: Gracing Incidence X-ray diffraction of amorphous and crystallized $Hf_xZr_{1-x}O_2$, measured with an incidence angle ω = 0.5°. The inset shows a schematic of the measurement geometry as well as calculated powder diffratograms of cubic TiN, monoclinic HfO_2, orthorhombic $Hf_{0.5}Zr_{0.5}O_2$, and tetragonal HfO_2.

4.1.3.1 GIXRD

For thin polycrystalline materials studied in this thesis, the deep penetration depth of X-rays in the traditional Bragg-Brentano geometry provides a significant challenge due to its limited surface sensitivity. Instead, by

using a small incidence angle (typically below 1°) the penetration depth can be reduced to a few nanometers making it a surface-sensitive technique by limiting interactions from the substrate [156,157]. This approach is referred to as gracing incidence X-ray diffraction (GIXRD) and has been used extensively throughout this thesis. In GIXRD the incidence angle is kept constant while the detector angle is swept through the desired range. GIXRD is commonly used to characterize the different crystal phases present in ferroelectric HZO but can also provide information on the residual stress in a material [158]. Figure 4.3 shows the GIXRD data of a crystallized (magenta) and an as-deposited HZO film, published in Paper I.

4.1.3.2 NanoMAX

With the other mentioned techniques, the measured result is an average of the sample surface investigated. However, in some applications, for instance when using NLA to crystallize $Hf_xZr_{1-x}O_2$, spatially resolved XRD is a crucial tool to investigate the impact of the localized annealing. The NanoMAX beamline at MAX IV is capable of delivering a high flux of coherent photons, focused down to a spot size of ∼50 nm [159], a capability that allows for unprecedented opportunities to study individual nanoscale crystals and grains in polycrystalline thin films, as evidenced in Figure 4.4 where the ferroelectric o-phase reflection is spatially resolved within the annealed area.

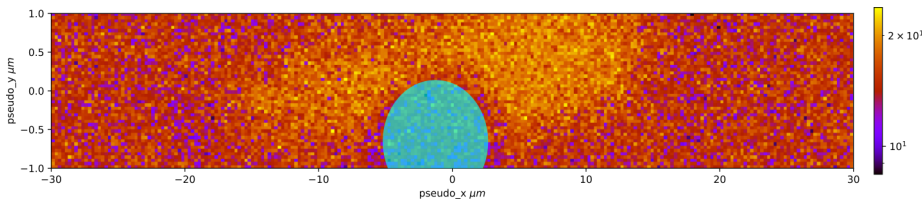

Figure 4.4: 2D intensity map of the ferroelectric o-phase (111) reflection using scanning X-ray diffraction on an NLA area. The blue circle illustrates the position of the W top electrode.

4.2 ELECTRICAL CHARACTERIZATION

To complement the structural characterization techniques, electrical characterization provides additional information of the highest importance for device integration. This section will cover the main electrical characterization methods used in this thesis for ferroelectric thin films and devices.

4.2.1 ELECTRICAL CHARACTERIZATION OF FERROELECTRIC THIN FILMS

Characterizing ferroelectric thin films is the first step toward ferroelectric device integration. In this thesis, the thin film characterization has been performed on MIM or MOS capacitor structures, fabricated according to the process described in section 3.4.

4.2.1.1 Polarization Measurements

The most commonly applied approach to derive the characteristic hysteresis curve of a ferroelectric material is by measuring the displacement current of a capacitor as a function of the applied voltage or electric field. The extraction of the hysteresis loop can be done according to the following equations:

$$D = \varepsilon_0 E + P = \varepsilon_0 \varepsilon_r E = \frac{Q}{A}, \tag{4.2}$$

where D is the displacement, E the electric field, P the polarization, ε_r and ε_0 are relative and vacuum permittivity respectively, Q is the electric charge and A the area. For ferroelectric materials with high permittivity (high-κ), the contribution of $\varepsilon_0 E$ is very small, and a simplification assuming $D = P$ is implemented. For HfO_2 with $\varepsilon_0 \sim 25$ specifically, the approximation yields a negligible error of only $\sim$1% [160]. Furthermore, as the current I and charge Q are related according to:

$$I(t) = \frac{\mathrm{d}Q(t)}{\mathrm{d}t}, \tag{4.3}$$

one can rewrite equation 4.2 as

$$P = \frac{Q}{A} = \frac{\int I(t)\mathrm{d}t}{A}. \tag{4.4}$$

However, it must be emphasized that this approach measures the change of charge and it can thus only provide information of the relative polarization and not the absolute. Thus, a second assumption where $|P_{\max}| = |P_{\min}|$ is usually made.

With this in mind, there are commonly two measurement techniques seen in literature to derive the polarization-voltage hysteresis, the PV and the positive-up-negative-down (PUND), both of which are depicted in Figure 4.5.

In the PV approach, a triangular voltage shape is employed, and the current passing through the capacitor is recorded. The polarization-voltage hysteresis can then be determined using equation 4.4, resulting in a hysteresis curve akin to Figure 4.5. However, it is important to note that since all measured current is integrated, the resultant charge encompasses various contributions. Alongside the polarization current, both dielectric and leakage

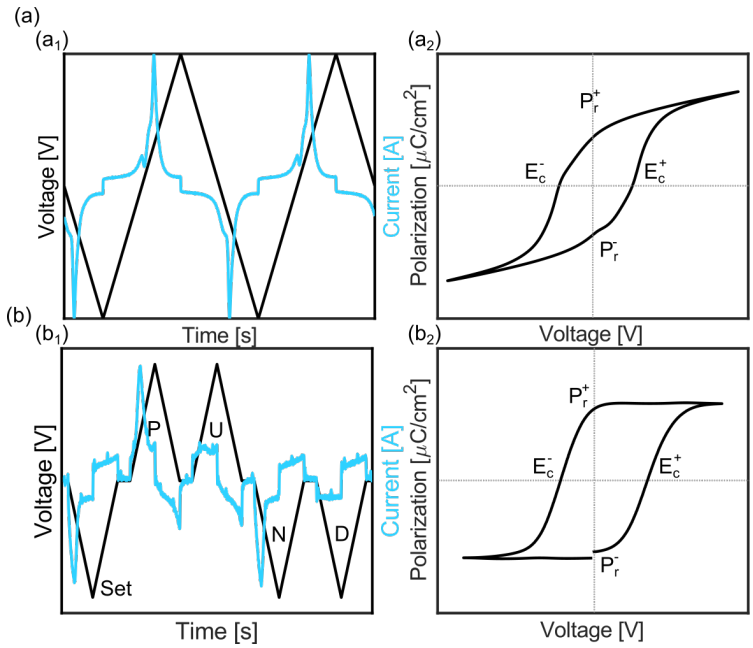

Figure 4.5: The predominant methods for electrically characterizing ferroelectrics are PV (a) and PUND (b). In (a_1,b_1), the current and voltage are depicted over time, while (a_2,b_2) illustrates the extracted polarization-voltage hysteresis curve derived from the data in (a_1,b_1), corresponding to PV and PUND method respectively.

current responses are integrated using this method. While the contribution of leakage current is not a significant concern for relatively thick films (> 5 nm), it becomes problematic for thin films below 5 nm.

To address this issue, the PUND method (Figure 4.5b) has been devised with the primary aim of subtracting the measured leakage and dielectric current, ideally isolating the contribution of the ferroelectric switching current [161]. Consequently, for thin films or films exhibiting high leakage, the PUND approach is widely favored. The PUND technique is elegantly simple, involving four pulses. The initial two pulses (P and U) share a positive polarity, while pulses three and four (N and D) share a negative polarity. During the initial pulse of each polarity (P and N), all three current contributions are present. In contrast, during the second pulse (U and D), only the dielectric and leakage contributions contribute to the measured current (assuming no depolarization of the ferroelectric polarization between pulses). Therefore, subtracting the measured current of the U and D pulses from the P and N

pulses, respectively, has the effect of isolating the pure ferroelectric response. This enables the derivation of a PV hysteresis with the characteristic observed in Figure 4.5b$_2$, from which important figures of merit such as P_r and E_c can be extracted.

4.2.1.2 Endurance

In an ideal situation, the ferroelectric HfO_2-based film would exhibit a consistent and strong polarization throughout its lifespan. However, this is not typically the case, as these ferroelectric films commonly undergo three distinct phases: wake-up, saturation, and fatigue. During the initial cycling of the ferroelectric material, there is usually an observed increase in polarization, referred to as the wake-up phenomenon. The cause of wake-up is often attributed to either a redistribution of oxygen vacancies in the film or a field-induced transition from the t- to the ferroelectric o-phase.

As the cycling progresses, the polarization eventually saturates after a certain number of cycles. With continuous cycling, the film enters the fatigue phase, during which the polarization starts to decrease. Fatigue is commonly linked to the generation of additional defects resulting from the cycling treatment. These defects can lead to domain pinning or hinder the nucleation of the opposite state. Moreover, as the defect concentration increases, a conductive filament may form, ultimately causing a hard breakdown of the film.

Given these effects, it is crucial to assess the evolution of ferroelectric properties with cycling, a parameter often referred to as ferroelectric endurance characteristics.

4.2.1.3 Switching Dynamics

Studying the switching dynamics of the ferroelectric film is pivotal for assessing its integration possibilities, and involves a comprehensive examination of the temporal evolution of polarization in response to external stimuli, in this case, the applied electric fields. This exploration not only unveils the fundamental mechanisms governing ferroelectric switching but also holds the key to optimizing material performance for diverse applications, ranging from non-volatile memory devices to sensors and actuators. For example, it has been shown that the type of dopant and the stochiometry in ferroelectric HfO_2 films alter the switching speed of the film [162].

To describe the reversal process in ferroelectric films the Kolmogorov-Avrami-Ishibashi (KAI) or the nucleation limited switching (NLS) model is typically used. The KAI model is more suitable for bulk ferroelectrics as the nucleation of reversed domains is faster than domain wall propagation.

However, in ferroelectric HfO_2 films, the domain well movement is limited due to the polycrystalline nature of the material and thus the KAI model has been shown to poorly describe the reversal dynamics [163]. Instead, both PFM measurements and stochastic switching in ultra-scaled FeFETs confirm the applicability of the NLS model in ferroelectric HfO_2 polycrystalline materials [83, 101, 163]. According to the NLS model, the time-voltage relation can be described as

$$t_{\mathrm{sw}} = t_0 \exp\left(\frac{\alpha}{k_{\mathrm{B}} T} \frac{1}{V_{\mathrm{pulse}}^2}\right), \tag{4.5}$$

where t_0 is the minimal nucleation/switching time, α a domain wall energy dependent parameter, k_{B} the Boltzmann constant, T the temperature, and V_{pulse} the applied voltage across the ferroelectric film [164].

To evaluate the switching dynamics of ferroelectric HfO_2 films a pulse scheme similar to Figure 4.6a is typically implemented. Here, the amplitude V_a and pulse width t_{width} are independently varied and the resulting polarization reversal is measured for each iteration. The switched polarization caused by the program pulse is read by a read pulse with opposite bias polarity. By plotting the measured change in polarization for each variation of the program pulse, a polarization switching map like the one in Figure 4.6b can be extracted. From the data in Figure 4.6b, the impact of t_{width} and V_a can be visualized by plotting the corresponding rows or columns of the switching map. Figure 4.6c-d demonstrates the relative polarization reversal as a function of t_{width} and V_a respectively. From this, it is possible to fit the measured data to the NLS model to verify its applicability [165].

4.2.1.4 Capacitance-Voltage

Capacitance-voltage (CV) measurements are one of the commonly implemented techniques to characterize ferroelectrics as they exhibit a non-linear dielectric permittivity that varies with the applied electric field. In the CV technique, a differential capacitance is measured by superimposing a small oscillating voltage (AC) onto a swept DC bias. By measuring the generated displacement current and the phase shift compared to the applied AC bias the complex admittance is derived. The complex admittance can then be converted to capacitance and conductance using an appropriate equivalent circuit model. The CV of a ferroelectric material is associated with a beautiful "butterfly" curve, with peaking capacitance around the coercive voltages, a phenomenon usually attributed to the non-linear domain-wall capacitance [166].

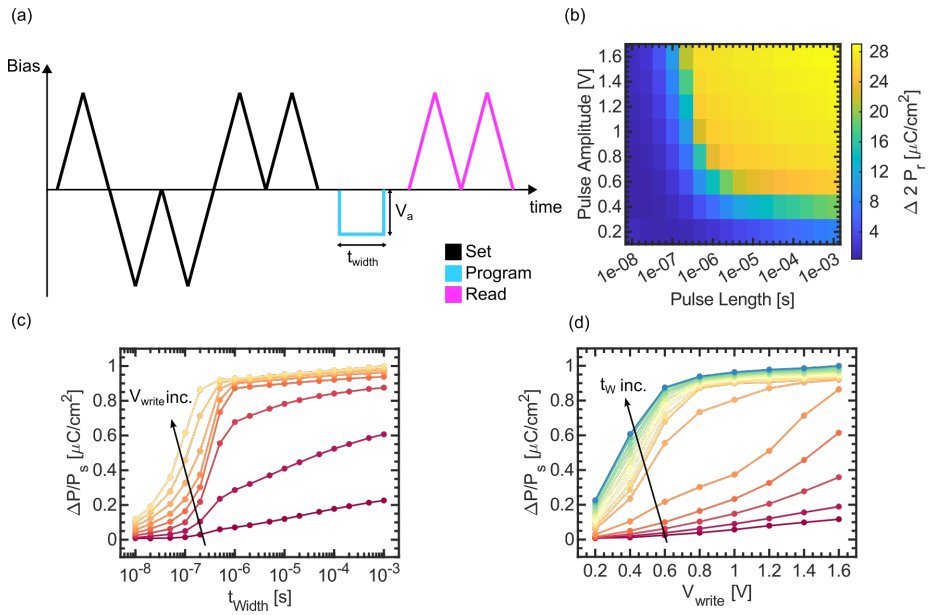

Figure 4.6: Characterization of the ferroelectric switching dynamics. (a) the implemented measurement scheme consisting of a set (black), program (teal), and read pulse (magenta). The width t_{pw} and amplitude V_a of the program pulse are varied to evaluate the switching dynamics of the ferroelectric. (b) A switching map of the polarization changes $\Delta 2P_r$ using a positive bias polarity of the program pulse. (c,d) Time and voltage dependence of the switched polarization ΔP normalized to the saturated polarization P_s, extracted from (b)

The implementation of CV measurements where the oscillation frequency is varied between the sweeps can provide valuable insights into defect contributions related to both the bulk and the interface. Analysis of the frequency dispersion of the capacitance or the hysteresis between samples provides a powerful approach to understanding the impact of both border traps and interface traps [167]. The interested reader is referred to the theses of Babadi [168], Wu [169], and Persson [144] for additional insights into CV measurements.

4.2.2 FERROELECTRIC DEVICE CHARACTERIZATION

In this section, some commonly used characterization techniques for benchmarking FeFET and FTJ devices will be presented. It should be noted that

there are additional characterization methods available in the literature and the ones presented in this section are the ones frequently used in this thesis.

4.2.2.1 Current-Voltage characteristics

Classic current-voltage (I-V) measurements are a quick and simple way to quantify the memory window in a FeFET or the TER ratio in an FTJ. Here, the leakage current through the ferroelectric film is measured as a function of applied voltage across the film. The leakage current is of great importance to FeFETs as there usually is a correlation between increasing leakage current and hard breakdown of the dielectric. For the FTJ the leakage current directly relates to the resistive memory state of the device. Moreover, for applications such as FeRAM, minimizing the leakage current is crucial to achieve long retention. Figure 4.7 shows the I-V characteristics of an FTJ being set and reset.

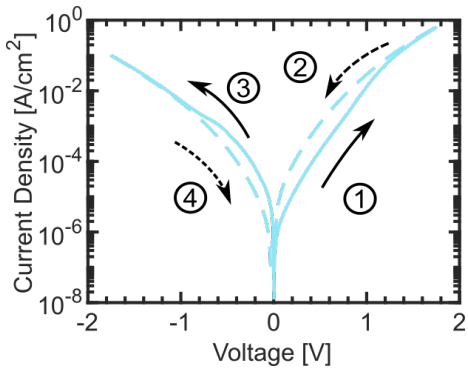

Figure 4.7: Typical current-voltage characteristics of an FTJ device. In the first sweep, the bias is swept above E_c which switches the polarization direction towards the bottom electrode, as the bias is reduced a higher current is achieved. Similarly, in sweep 3 a negative bias polarity below the negative coercive field is applied, switching the polarization direction back towards the top electrode. As a result, a lower tunneling current is measured during the forth and final sweep. The I-V measurements were acquired using an Agilent b1500 semiconductor parameter analyzer equipped with high-resolution source measure units (HRSMU) equipped with attosense units (ASU).

4.2.2.2 Programmability

Both FeFETs and FTJs share a fundamental functionality, which involves the capacity to alter device characteristics by manipulating the remanent

polarization in the ferroelectric material. An examination of the device's programmability provides insights into characteristics such as switching speed and voltage dependence. Moreover, key parameters for analog memory, including the number of accessible conductance states, dynamic range, and variability, are determined based on the device's programmable nature. In the case of the FTJ, the programmability is investigated by applying a voltage pulse of amplitude V_{write} and duration t_{pulse} to the top electrode while grounding the bottom electrode. Then the FTJ conductance is assessed using HRSMUs and a small I-V sweep from e.g. 0 - 300 mV, significantly below the coercive field, so as not to disturb the programmed state. Figure 4.8 shows the typically implemented approaches for modulating the conductance: amplitude (Figure 4.8a), pulse width (Figure 4.8b), or pulse repetition (Figure 4.8c) modulation. Similarly, the depression of the conductance is evaluated by applying a negative bias polarity to the top electrode. In addition to potentiation and depression characteristics, the resistance-voltage (R-V) curve is another common FTJ device characterization method for evaluating programmability. The R-V measurement scheme is shown in Figure 4.8d, illustrates a process where a positive-polarity programming voltage is gradually increased to a specific V_{max} and then decreased back to the initial value. Following each programming pulse, the device's conductance is read. Subsequently, the same sequence is repeated with a negative voltage polarity. This procedure generates a conductance hysteresis loop, offering insights into the stability of the programmed conductance state. During the ramp-down of the programming voltage, the ferroelectric domains are expected to remain unaffected, having already switched in the direction of the externally applied electric field. Consequently, a consistent conductance level should be observed until programming voltages of the opposite polarity which are large enough to alter the direction of the ferroelectric domains are applied.

For the FeFET the programmability is evaluated in a similar way, however the implementation is a bit different due to the three terminals of the device. During programming, the gate terminal is pulsed while the source and drain terminals are grounded, then during the read operation, the transfer characteristics are measured by applying a small transfer sweep below E_c to determine the threshold voltage.

4.2.2.3 Variability

For both memories and memristors, the variability of each individual device, as well as between devices is of significant importance for the viability of the technology in an integrated system. Thus, two common metrics are derived to quantify the variability: the device-to-device (DtD) and cycle-to-cycle (CtC) variation. Although there are many ways in which these figures-

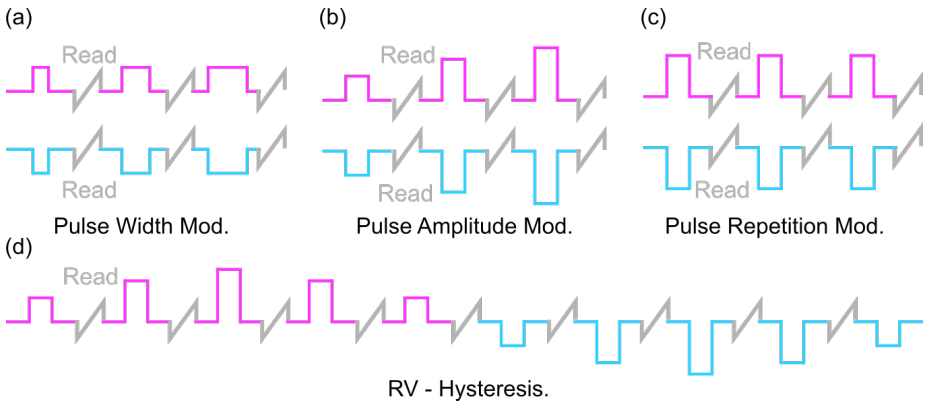

Figure 4.8: Commonly implemented pulse schemes to alter the conductance of a memristive device. The potentiating (magenta) or depressive (teal) write pulse is followed by a read sweep (grey). (a) Pulse width t_{pulse} modulation, (b) pulse amplitude V_{write} modulation, (c) pulse repetition modulation. In (d), the pulse scheme for RV hysteresis characterization.

of-merit could be evaluated, the commonly used methods for their use as analog memristive memories are as follows: by repeatedly going through cycles of potentiation and depression of the device conductance the CtCV can be quantified by comparing the programmed conductance value for a certain input pulse across the cycles. Doing this for all pulse numbers an average CtCV can be extracted. A similar approach can be adopted for the DtDV as well, where the same stimulus is applied to different devices and then the conductance variation for each pulse number can be evaluated. Typically the standard variation is used as the quantitative measure of both CtC and DtD variation.

4.2.2.4 Retention

A big benefit of using ferroelectricity in electronic devices is its intrinsic non-volatility. Thus, a programmed state should ideally be kept when the external electric field is removed. However, due to effects such as depolarization fields, and charge trapping this is not always the case. The ability for a device to hold its programmed state over time is known as retention and is for both the FeFET and FTJ characterized by measuring the conductance of the device continuously, as seen in Figure 4.9a. This is achieved by first programming the device using a write pulse and subsequently conducting read sweeps with progressively longer intervals between them. It is crucial that the read sweep is kept sufficiently small to avoid disrupting the programmed state.

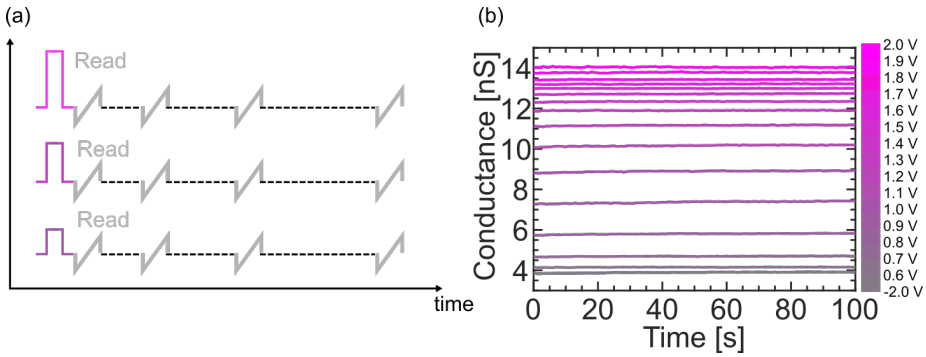

Figure 4.9: Memristor state stability. (a) Measurement scheme for retention characterization of the memristor multistate properties. (b) Example of measured retention of 16 distinct conductance states in a W/HZO/TiN micro FTJ.

As discussed previously, the retention requirements are application-dependent, and for non-volatile memories, a 10-year retention is a requirement. However, for practical reasons, retention is usually measured for a shorter time and then based on that data extrapolation to 10 years is done. A more rigorous method is to measure the time until loss of memory at several elevated temperatures and extrapolate to lower temperatures. In this way, one may obtain values also at the practically interesting value of 85 C, the maximum operation temperature of most electronic systems. These characterization methods become rather impractical for multi-state memristors where one would ideally present retention for all conductance states, which when the number of states becomes large is not feasible. Figure 4.9b shows the retention of 16 different in an FTJ measured during 100s, presented in Paper V.

4.2.2.5 Random Telegraph Noise

In strongly scaled devices, the absolute count of defects may be very low, making the effects of individual traps discernible in certain measurements. This becomes apparent when these traps exhibit capture and emission time constants that align closely with the integration time of each measurement point [170]. Figure 4.10a shows the recorded current during the readout of a nano-FTJ which displays a distinct step caused by defects.

If the read current, denoted as I_{read}, is continuously measured with sufficient time resolution at a fixed bias point near a noticeable capture/emission step, a phenomenon known as Random Telegraph Noise (RTN) can be witnessed. In RTN, the current fluctuates between two distinct levels due to the

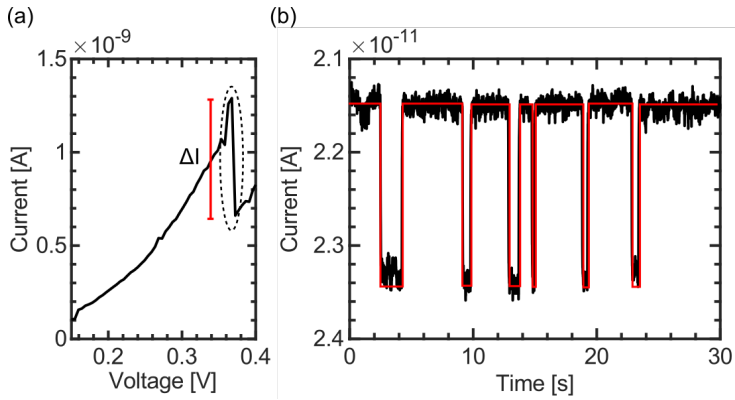

Figure 4.10: (a) Demonstration of how individual oxide traps can impact the read current in a nanoscaled FTJ. (b) Example of RTN (different device), at a fixed bias point close to a distinct step in the measured read current. The capture and emission event of an electron yields a current fluctuation between two distinct levels.

trapping and de-trapping of electrons in a specific defect, as exemplified in Figure 4.10b.

Given that the trapping and de-trapping follow a Poisson point process, the distribution of times in the high and low current states can be described by an exponential distribution, denoted as $f(t) = \tau^{(-1)} \exp(t/\tau)$, where t is the time, and τ is the characteristic time constant of the process. Thus, the characteristic capture and emission time constants of an individual trap can be deduced from the measured distributions.

5

Ferroelectric HfO_2 in Next Generation Electronics

"Science is like a cork-screw, you feel like you are walking in circles but the circles are actually leading you somewhere."

Inspired by Simone Giertz

This section will cover the main contributions made to the research field during this thesis project. It is divided into sections covering the integration of HZO onto the III-V semiconductor InAs, realizing ferroelectricity in ultra-thin HfO_2 films using nanosecond laser annealing, the impact of fabrication conditions on the FTJ properties, and finally an evaluation of FTJ memristors for brain-inspired computing.

5.1 FERROELECTRIC HFO_2 ON INAS

III-V semiconductors have significantly greater electron mobility compared to Si, which makes these materials highly attractive for high-frequency electronics applications. Additionally, the ability to grow vertical III-V nanowire structures allows for a vertical GAA geometry that provides superior electrostatics while decoupling the channel length from the footprint of the device. Thus, the ability to integrate ferroelectric properties onto a III-V material platform is highly desirable. A large part of this thesis work has been to implement and investigate the integration of ferroelectric HfO_2 on the III-V semiconductor InAs. InAs has an excellent electron mobility of $\sim$13 000 $cm^2V^{-1}s^{-1}$ [26] making it attractive for high-frequency electronics. However, its highly defective native oxides present at the surface makes it challenging to obtain reliable MOS stacks with reliable and stable threshold

voltages and small hysteresis. This has been well studied previously in the works by Babadi [168], Hellenbrand [170], and Persson [144]. The interface between InAs and HfO_2-based dielectrics is not improved by the annealing treatment required to crystallize the ferroelectric as InAs is a thermally sensitive material prone to decomposition at elevated temperatures. Thus, in Paper I we evaluate and optimize the integration of ferroelectric HfO_2 on planar InAs. We study the impact of the annealing temperature in traditional RTP, highlighting that the semiconducting properties of the InAs are kept post-annealing. Additionally, the use of InAs as a bottom electrode reduces the required annealing temperature to form ferroelectric HZO as compared to a TiN/HZO/TiN MIM capacitor (see Figure 5.1a). A strong polarization of P_r > 20 μC/cm^2 is achieved for the InAs MOSCAP at an annealing temperature of 370°C, a reduction of 50°C compared to the MIM structure. A significant reduction where integration below the 400°C "golden mark" allows BEOL integration of the technology, assuming that InAs itself could be integrated into the BEOL at these temperatures.

Despite the results in Paper I, the CV analysis presented in our related work by Persson et al. [167], showed similar defect densities for all crystallized HZO films, independently of the RTP peak temperature. Thus, to further improve the interface quality between InAs and HZO, Paper II evaluates ms-FLA to crystallize the HZO which significantly limits any diffusive processes. Comparing FLA to RTP, we find improved switching endurance in the FLA-treated samples. These results are supported by the observation of a reduced defect density at the InAs/HZO interface, extracted using C-V measurements, as shown in Figure 5.1b. This is further strengthened by XPS measurements where a distinct decrease in the metallic As component is observed for the FLA samples when compared to RTP. Metallic As is known to be a major source of interface defects at InAs/high-κ oxide interfaces and to be especially detrimental to device performance [103, 171]. The results in Paper II present an alternative approach to lowering the thermal budget for the integration of ferroelectric HZO on thermally sensitive substrates such as InAs.

The very intriguing result presented in Paper I where the integration of HZO on an InAs bottom electrode improved the P_r from ∼16 μC/cm^2 to ∼21 μC/cm^2, spurred the interest of further improving the P_r. Despite the improved P_r, the switching endurance was significantly reduced from 10^8 in our TiN/HZO/TiN MIM structures, to ∼10^4 on InAs. With this in mind, in Paper III we turned the focus towards optimization of the TiN top electrode, as Ti is a known oxygen scavenger that can detrimentally impact the switching endurance of the ferroelectric. By tuning the deposition pressure and introducing a nitrogen flow during the TiN top electrode deposition, we manage to increase the P_r to 30 μC/cm^2 and improve the endurance to 10^5

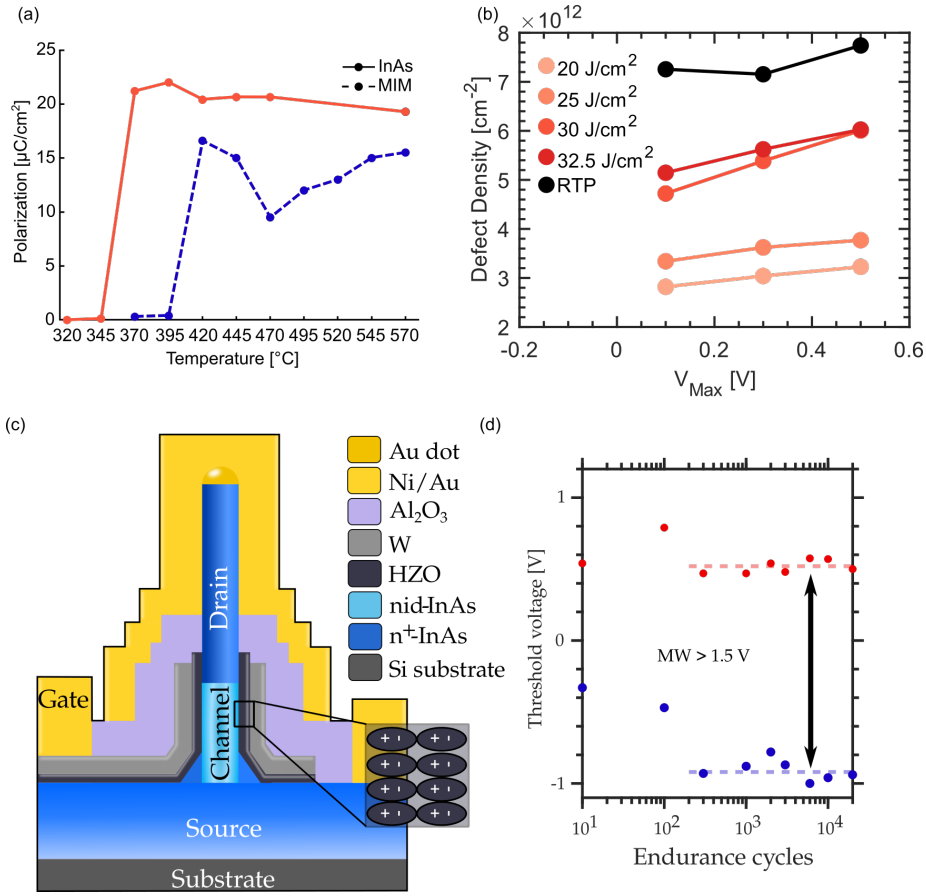

Figure 5.1: Integration of HZO on InAs. (a) The impact of annealing temperature on P_r for InAs MOS caps and TiN/HZO/TiN MIM caps. (b) Defect density, extracted from C-V measurements comparing traditional RTP annealing with ms-FLA for crystallization of the HZO. (c) Schematic of the vertical nanowire FeFET structure showing a memory window of 1.5 V, stable during cycling (d).

switching cycles. From GIXRD measurements, a correlation between the TiN (111) texturing and the relative o-phase fraction and thus P_r was found. The TiN (111) texture could also be demonstrated to induce an increased in-plane tensile stress in the HZO, beneficial in promoting the o-phase.

The results of Paper **??** provided the fundamental understanding required to eventually achieve the integration of the first vertical III-V nanowire FeFET schematically depicted in Figure 5.1c, published in paper Paper VI. The fabri-

cated FeFET demonstrates a sizeable memory window of 1.5 V which is stable with cycling as shown in Figure 5.1d, as well as a distinct separation between the two states after, but not limited to, 2000 seconds. The performance of this vertical nanowire FeFET is primarily limited by top-contact resistance and the amount of defects in the high-κ oxide after polarization switching. Limitations that may be improved by further process refinements.

5.2 REALIZING ULTRA-THIN FERROELECTRIC HFO_2

As discussed in Chapter 2, the current level in FTJs is proportional to the transmission probability of charge carriers through the barrier. This probability is exponentially dependent on the thickness of the barrier. Thus, the current levels in these devices are typically rather low. To combat this, the implementation of thinner ferroelectric layers is needed. However, scaling down the thickness of the ferroelectric layer is not a trivial task as it in general requires significantly higher annealing temperatures for crystallization. Additionally, the tensile strain induced by the top electrode also plays a key role. As we struggled to achieve ferroelectric properties in sub 5 nm-thick HZO films due to high leakage currents, a switch from a TiN to W top electrode was made. In Figure 5.2a, the necessary annealing temperatures to achieve ferroelectricity in HZO as a function of thickness is presented. Switching from a TiN to W top electrode allowed for the observation of ferroelectric properties down to $\sim$3.2 nm, while also reducing the leakage current levels. However, as is evident from Figure 5.2a, to crystallize ultra-thin films, a temperature of 700 °C was required which hinders BEOL integration, as well as being detrimental to the metal/oxide interface, as shown in Paper V. To circumvent this we implemented an NLA approach in Paper VIII, where highly localized annealing both spatially and depth-wise can be performed (see 5.2b). A laser pulse of 6 ns and spot size of 50 µm, allows for very high surface temperatures without damaging any logic placed in the FEOL. Figure 5.2c shows the resulting P_r achieved in a 3.6 nm-thick HZO film using NLA. A maximum $P_r \approx 6$ µC/cm^2 highlights the potential of using ultra rapid annealing approaches to induce ferroelectricity in HZO. Furthermore, the rapid annealing significantly suppresses any diffusion which improves the interface quality at the ferroelectric/bottom electrode, beneficial for device performance.

The localized annealing provided by the NLA approach opens up for studying spatial changes in the crystal phases within a sample. The included scanning XRD measurements in Paper VIII, performed at the NanoMAX beamline at MAX IV, verify the presence of the o-phase in the annealed area. By focusing the spot size of the X-ray beam down to 200 nm and

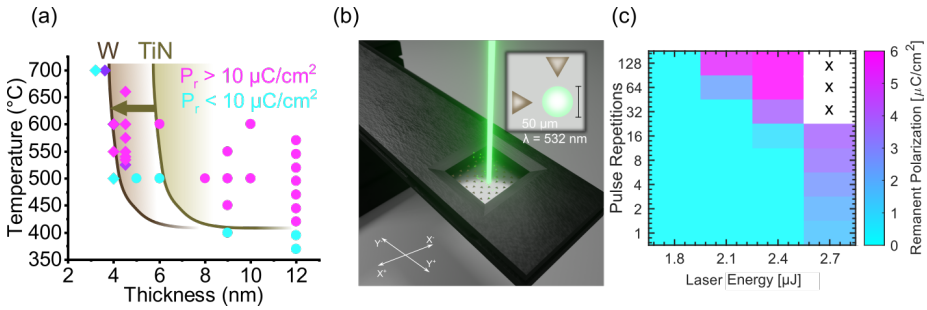

Figure 5.2: Realizing ultra-thin HZO. (a) Necessary annealing temperature to achieve ferroelectricity in HZO as a function of its thickness. A W top electrode (squares) allows for thinner ferroelectric films than TiN (circles). (b) NLA setup, which allows for localized heating due to a small spot size of 50 µm diameter. (c) map of the resulting P_r during NLA for varying laser energies and repetitions, X marks a shorted device.

scanning the annealed area, a 2D map of the ferroelectric o(111) reflection is spatially mapped. The ability to measure the diffraction of these very thin films without any special sample preparation is an encouraging result as the structural characterization methods otherwise available which can indicate the presence of ferroelectricity in really thin films, are limited.

5.3 FERROELECTRIC TUNNEL JUNCTIONS - FABRICATION CONSIDERATIONS

Although a W top electrode has proved to be a great choice to induce the ferroelectric properties in thin HZO films, being restricted to a single electrode material is a serious limitation when it comes to device design and tuning of device properties. Thus, the approach of using a sacrificial crystallization electrode (CE) in the FTJ processing, was introduced in Paper IV. The CE allows for the decoupling of the ferroelectric film properties and the device design, enabling tuning of the device properties. In Paper IV we demonstrate the benefit of having a high free electron density n_e by using Ni as a top electrode to achieve a high TER (see Figure 5.3a). However, due to the significantly higher WF of Ni compared to the TiN bottom electrode, we obtain a high built-in electric field. This built-in field negatively affects the reliability of the FTJ and limits retention and endurance. However, by implementing WF engineering and a bi-layer top electrode material, in this case, Cr/Ni (1/200 nm), a high n_e is combined with a low built-in bias field. Using this approach a high TER = 8 and good reliability were demonstrated.

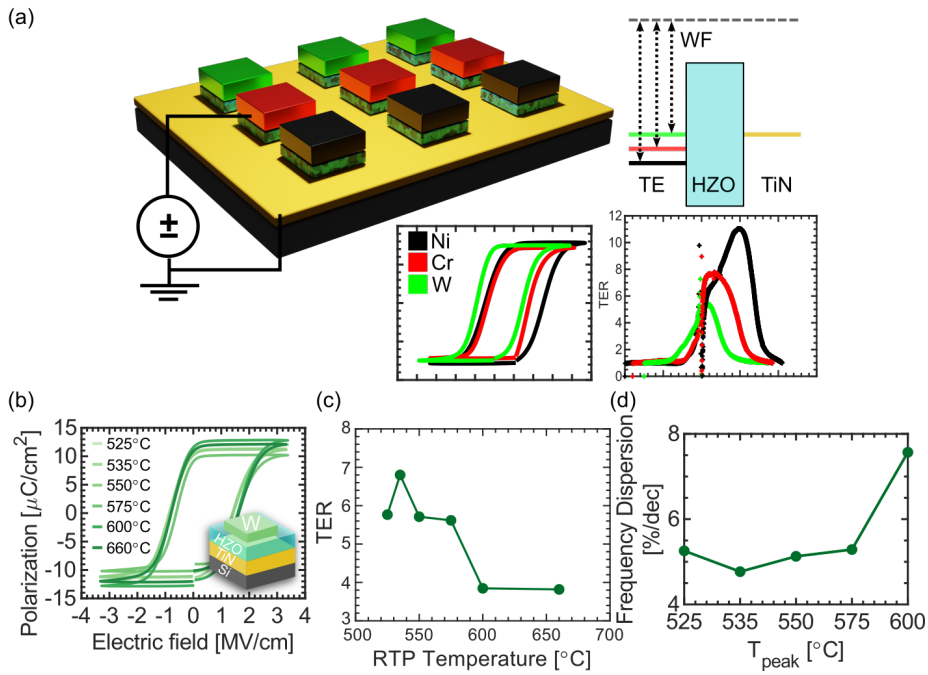

Figure 5.3: Impact of processing on FTJ characteristics. (a) The choice of top electrode alters both the built-in field which shifts the PE hysteresis as well as the screening of the polarization charge depending on the free electron density of the electrode, which then impacts the resulting TER of the FTJ. (b) P-E hysteresis curves of W/HZO/TiN FTJs annealed at different peak temperatures. (c) The impact on the TER for different PMA peak temperatures. A clear decrease in TER can be observed for excessive PMA temperatures despite almost identical P_r. (d) Frequency dispersion from C-V measurements indicating increase amount of defect with higher PMA temperatures.

This highlights the possibilities and benefits of using a CE and replacement process in FTJ fabrication.

As previously discussed, the interface chemistry is of great importance for ferroelectric devices and especially the FTJ as the screening length will directly depend on this surface chemistry. Ideally one would like to achieve a large asymmetry between the screening lengths of the top and bottom electrodes to enhance the TER. It is also well known that the TiN bottom electrode is prone to scavenge oxygen from the HZO generating defects which degrade the device performance. With this in mind, Figure 5.3b-d summarizes the impact

of the RTP annealing temperature on the device performance of W/HZO/TiN FTJs, which was evaluated in paper Paper V. A strong correlation between the PMA temperature used for crystallization and oxide/interface defect formation is observed. Despite very similar ferroelectric properties (Figure 5.3b) in the films, a clear reduction in endurance, TER (Figure 5.3c) and I-V nonlinearity is observed when an excessive PMA temperature is applied. CV measurements show a significantly increased frequency dispersion, as shown in Figure 5.3d, with increasing PMA temperature, highlighting the importance of carefully selecting an appropriate PMA temperature to optimize the FTJ performance, or alternatively, as I show in Papers Paper **??**, use ultra-short thermal processing to limit the diffusive processes responsible for interface degradation.

5.4 FERROELECTRIC TUNNEL JUNCTIONS FOR BRAIN-INSPIRED COMPUTING

In this section, the memristive properties of the fabricated FTJs will be discussed as well as considerations required to enable large-scale integration of FTJ crossbar arrays for hardware accelerators. The discussion is based on the results presented in papers Paper V and Paper VII.

5.4.1 ANALOG PROPERTIES

As mentioned earlier in the thesis, utilizing partial polarization switching of the ferroelectric film allows for programming a device into multi-level conductance states. This is achieved through primarily three different stimuli: amplitude, pulse width, or pulse repetition modulation. Furthermore, the resulting potentiation and depression response of the FTJ conductance using each approach can be seen in Figure 5.4a-c. For the FTJs presented in this thesis, the use of an amplitude modulation stimulus provides a significantly increased dynamic range (G_{on}/G_{off}) of DR = $\sim$10, when compared to the other modulation schemes. Additionally, it also provides a more linear and symmetric conductance change in both potentiation and depression, a characteristic beneficial to achieve a high classification accuracy in ANN applications. However, to avoid that the various memory states overlap over time it is critical that there is sufficient retention, and thus Figure 5.4d shows a histogram of the current levels of 16 different conductance states measured during 100 s. The conductance states are distinctly defined without overlap, and with low drift during the measurement window. Extending the measurement to 10^4 s does add additional spread to the state but again no conductance drift is observed, as evident from the black bars in Figure 5.4d.

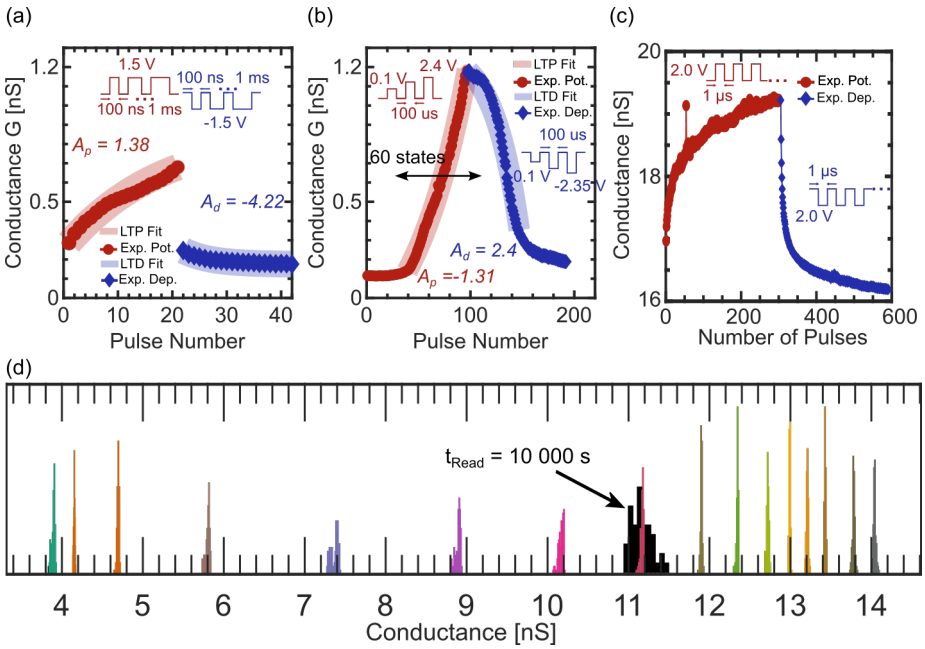

Figure 5.4: Conductance characteristics of micro-FTJ. (a)-(c) the potentiation and depression of the FTJ conductance using pulse width, pulse amplitude and pulse repetition modulation respectively. Note that the conductance in (c) is larger than in (a)-(b), explained by the ∼x16 larger device area. (d) histogram of the measured multistate retention of 16 individual conductance states during 100s. The black bars in (d) show the retention measurement of a single state during the extended period of 10^4s.

5.4.2 CLASSIFICATION OF HANDWRITTEN DIGITS USING FTJ CROSSBARS

The performance of our FTJs as artificial synapses in a crossbar array was investigated in Paper VII by using the *MLP+NeuroSim V3.0* framework [172]. The online learning accuracy of a true crossbar array was simulated, representing an ANN with 400 inputs, 100 hidden, and 10 output neurons (corresponding network structure shown in Figure 5.5a), trained on the modified National Institute of Standards and Technology (MNIST) [11] database. The non-linearity parameters A_p and A_d were fit to the FTJ potentiation/depression data presented in Figure 5.4b according to [172]. Figure 5.5b shows the learning accuracy of the MNIST database for ideal (blue) and non-ideal FTJ device characteristics. In the ideal case where potentiation and depression are linear and symmetric, the learning accuracy reaches 94%. Accounting for only the nonlinearity (NL) drops the accuracy to 84%,

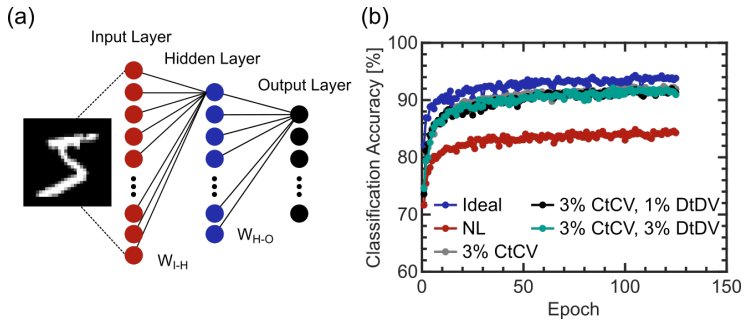

Figure 5.5: Online learning performance. (a) The neural network structure used in the *MLP+NeuroSim V3.0*, to train the MNIST database. (b) Online classification accuracy as a function of the number of ephocs for ideal (blue), and non-ideal device characteristics.

however, if a small CtC variation of 3% is introduced, the accuracy improves to an excellent 92%. Additionally, by adding a DtD variation up to 3%, which is the maximum observed for our FTJs (shown in [86]) the classification accuracy remains unchanged. Thereby we concluded that FTJ-based neuromorphic systems would be robust against DtD variability, and that some degree of CtC variability helps to counter the NL in potentiation/depression.

5.4.3 SCALABILITY OF FTJ CROSSBAR ARRAYS

In large crossbar arrays operated as random-access memory, undesirable sneak currents arising from half-selected cells diminish the read margin and limit the size for which the crossbar arrays remain functional. To combat this issue, an external selector device with highly non-linear I-V characteristics, such as a transistor or diode can be used in series with the memristor. A key benefit of the FTJ concept is the built-in highly non-linear I-V characteristics, as seen in Figure 4.7, due to the tunneling transport mechanism. In Paper VII we determine the maximum functional FTJ array size without external selectors, by evaluating the read margin $\Delta V/V_{pu}$ of the array. Figure 5.6a shows the read margin as a function of the number of word/bit lines for two different voltage schemes, namely the "V/2" and "V/3" [173]. The built-in I-V nonlinearity of these FTJs could potentially allow the integration of arrays up to 54 kbit and 1.2 Mbit using the V/2 and V/3 voltage schemes respectively.

In crossbar integrations, the voltage drop across the line resistance (IR drop) is a severe limitation in the upscaling of the array size. The IR drop arises from the non-negligible wire resistance along the row/column wires which increases quadratically with the number of rows and columns in the array.

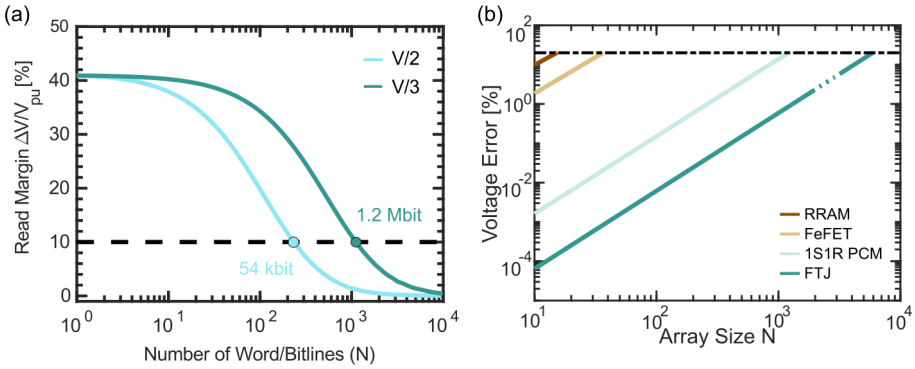

Figure 5.6: Scalability of FTJ crossbar arrays. (a) evaluation of the sneak currents through half-selected cells on the read margin $\Delta V/V_{pu}$ for V/2 and V/3 biasing schemes. (b) impact of the IR drop due to parasitic wire resistance on the voltage error in the $I = G \cdot V$ operation as a function of the array size N for device concepts with varying conductance. The dotted section indicates the start of extrapolation.

The low conductance of FTJs is beneficial in suppressing the IR drop as it is much larger than the parasitic wire resistance. This enables the scaling of the crossbar array size to larger arrays than for other technologies instead of using several smaller crossbars for the same amount of storage. This is beneficial because it dramatically saves on the overhead in terms of the required peripheral circuitry. Apart from regular storage, large crossbars are also key to achieving high energy and area efficiency in vector matrix multiplication accelerators for artificial neural network applications. Figure 5.6b shows the calculated relative error introduced in the $I = G \cdot V$ operation due to the IR drop for various memory technologies such as 1T1R RRAM [174], FeFET [175], 1S1R PCM [176] and the FTJs in this work. The voltage drop caused by interconnect resistances was calculated using the open-source Python framework *badcrossbar* [177], assuming a worst-case scenario where all memristors are programmed to their low resistive state.

These findings highlight the promising application of FTJ memristors for accelerating VMM and MAC operations, both being pivotal operations in ANNs. The inherent rectifying I-V characteristics and low conductance of these memristors not only facilitate the achievement of high density but also enable the development of energy-efficient, large-scale in-memory accelerators, addressing the inherent bottleneck associated with von Neumann-based architectures.

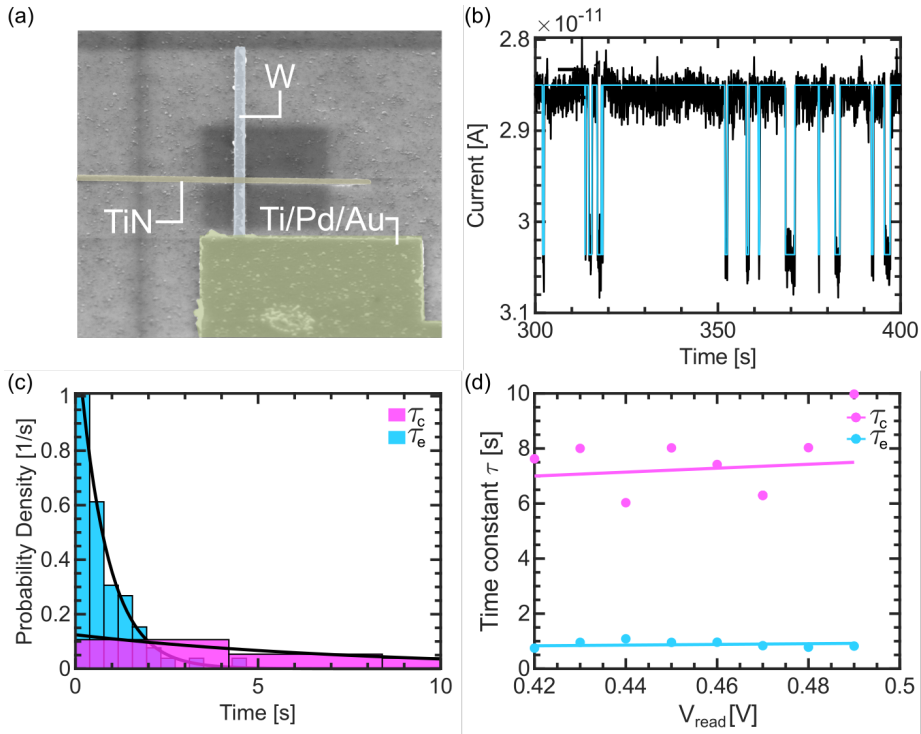

Figure 5.7: (a) Colored SEM image of nanoFTJ. (b) read current measured at a fixed bias point of V_{read}= 420 mV. (c) Histogram of measured RTN with fitted exponential distributions. (d) measured characteristic time constants τ_c and τ_e as a function of the applied V_{read}.

5.5 INDIVIDUAL TRAPS IN SCALED FTJS

For any eNVM technology, the ability to scale down the device dimensions is paramount as an improved integration density over current memory technologies are required to achieve notable benefits of integrating a new technology and to address the current challenges. However, as previously discussed in Chapter 4, in strongly scaled devices individual defects can measurably impact the device characteristics. Thus, by fabricating scaled nanoFTJs shown in Figure 5.7a, with dimensions down to 100 x 100 nm, we study the presence of RTN on the read current. Figure 5.7b shows the measured current over time for V_{read}= 420 mV where the current level fluctuates between two states due to the trapping and de-trapping of electrons in a specific defect. Figure 5.7c shows the histogram of the measured RTN with fitted exponential distributions. From the fitting τ_c = 7.6 s and τ_e = 0.74 s. The observation

that τ_c is more than one order of magnitude greater than τ_e suggests that the defect might be situated deep within the oxide, with this occurrence being the limiting factor. Furthermore, Figure 5.7d illustrates the relationship between $\tau_{c/e}$ and V_{read}. The derived time constants seem relatively unaffected by the applied V_{read}, implying that the trap captures electrons from both the bottom and top electrodes and releases them through thermionic emission, as suggested by Shi et al. [178]. However, the complete nature of this behavior remains unclear, necessitating additional measurements to fully comprehend the underlying processes. Conducting further measurements with variations in both bias range and measurement temperature would offer more insights into the ongoing processes, potentially validating the theory of thermionic injection/emission and providing an estimate of the energy level associated with the probed trap, as proposed by Chang et al. [179].

6

Outlook & Final Words

"People who think they know everything are a great annoyance to those of us who do."

Isaac Asimov

This thesis has investigated a wide range of approaches to integrate ferroelectric materials in electronic devices as an approach to push electronics technology beyond Moore's law. The work covers the fabrication of ferroelectric HfO_2-based films in both planar and vertical geometry on traditional CMOS materials and thermally sensitive III-V semiconductors. During the thesis work, the combined use of both advanced electrical and structural characterization techniques has provided unique insight into the fundamental working principle of ferroelectric materials and devices. Additionally, the fabrication of FeFETs and FTJs was successfully demonstrated, with a focus on FTJs, where stable multistate memristive properties were achieved. Finally, the results evaluating the large-scale integration of FTJs in crossbar arrays for in-memory computing accelerators show great promise to accelerate VMM and MAC operations. The appended papers in the back of the thesis can be divided into three primary categories: ferroelectric integration of HfO_2 on InAs (Papers I-III and VI), ferroelectricity in ultra-thin films (Paper VIII), and the fabrication of ferroelectric tunnel junctions for memory and memristor applications (Papers IV-V and VII). The results presented in the papers highlight the benefits and challenges of the applied approaches regarding the developed technology platform. A summary of the results within the three categories is presented below.

Ferroelectric HfO_2 on InAs

Paper I and Paper II focus on lowering the thermal budget for integration of ferroelectric HZO on InAs using RTP and FLA. Interestingly we demonstrate a reduction of the required annealing temperature by 50°C on InAs compared to TiN as well as an improved cycling endurance when using FLA to crystallize the HZO. A result of limited diffusion due to the short time scale of the FLA, which is supported by the lower defect densities confirmed in CV and XPS measurements.

To improve the endurance of our InAs MOSCAPs, Paper III studies the tuning of the TiN top electrode deposition conditions. By optimizing the pressure and introducing nitrogen during the deposition process, the texturing and stochiometry of the TiN are optimized, which increases the P_r to 30 $\mu C/cm^2$ and the endurance to 10^5. The use of XPS and EDX confirms the increased nitrogen incorporation whereas GIXRD and wafer bow measurements correlate the presence of TiN (111) and the formation of the ferroelectric o-phase.

With the studies on planar InAs paving the way for more advanced geometry, Paper VI presents the implementation of the first vertical nanowire FeFET. As a proof of concept device, the performance is relatively good with transistors showing a stable memory window of $\sim$1.5 V with continuous cycling. However, additional optimization of the fabrication process is required as the thermal treatment (RTP) currently degrades the quality of the top contact, creating a large series resistance.

Ferroelectricity in Ultra-thin films

Having established a technology platform for fabrication and characterization of ferroelectric HfO_2 the pursuit of FTJs required scaling down the thickness of the ferroelectric to allow for measurable tunneling current levels. The switch from a TiN top electrode to W with engineered strain resulted in the successful fabrication of ferroelectric HZO down to 3.2 nm. However, the high annealing temperature required to crystallize these films hinders BEOL integration. Therefore, Paper VIII uses NLA, which allows for spatial selective crystallization due to the ultra-fast time scale. Using this approach we crystallize a 3.6 nm ferroelectric HZO film while keeping BEOL compatibility.

Ferroelectric Tunnel Junctions

In Paper IV we demonstrate our first working FTJ and the use of a crystallization electrode and metal replacement process that allows us to decouple the ferroelectric film properties from the device design. This approach enables the optimization of both the TER ratio and the reliability of the FTJ by implementing a Cr/Ni bi-layer top electrode. Using the optimized stack,

switching endurance of at least 10^8 and 10-year retention (extrapolated) is demonstrated.

In Paper V the impact of temperature-induced oxide defects on the FTJ memristor performance is evaluated. From this study, the impact of carefully selecting the PMA temperature is highlighted as devices with very similar ferroelectric properties, still show vastly different memristive performance. CV measurements confirm that the use of an excessive PMA temperature increases the formation of oxide/interface defects that degrade the performance of the FTJ. By optimizing the PMA temperature we demonstrate an FTJ memristor with 16 distinctly separate conductance states and a low CtCV of 1.2% (average).

Finally, in Paper VII we evaluate the suitability of using FTJ memristors for in-memory computing hardware accelerators. By programming with an amplitude modulation scheme, a high I_{on}/I_{Off}, low inter- and intra-device variability, and excellent I-V nonlinearity are demonstrated. Based on the measured device characteristics, the classification performance of a true FTJ crossbar array is simulated. An excellent classification accuracy of 92% for the MNIST data set is achieved in a true crossbar array. Furthermore, the evaluation of sneak path currents and IR drop in large crossbar arrays shows promising results owing to the built-in rectifying I-V property and overall low conductance of the FTJs.

Outlook

The results presented in this thesis demonstrate important aspects to consider for the fabrication of ferroelectric HZO, as well as the advantages of ferroelectric devices as emerging memory and memristive devices. Throughout this thesis, many different aspects of ferroelectric integration have been investigated but there are still areas that require further attention. As a proposal for future research, examples of some of these areas are given below. To improve the poor top contact in the FeFETs it would be highly interesting to evaluate crystallization using FLA or NLA in the vertical NW geometry. The short time scale of these methods has shown promising results in the planar geometry and has the potential to significantly improve the performance of these devices.

Currently, the thickness limit on the ferroelectric properties using the NLA approach is still unknown, and the 3.6 nm achieved in this thesis should not be viewed as a lower limit. As the ferroelectric thickness is crucial to reducing the switching voltage and thereby the energy consumption, pushing the limits of NLA is time well invested. Additionally, with recent reports of ferroelectricity down to 1 nm using traditional methods I firmly believe that it can also be achieved using a localized annealing method. Nonetheless, the NLA films

exhibit a significant wake-up behavior that is non-ideal from a device point of view. The reason is not yet clear, but it could be that the ultrashort annealing time is insufficient for the t- to o-phase transition to occur, thus requiring the use of an external electric field to initiate this phase transition. The use of a longer low-temperature furnace anneal after the NLA treatment could perhaps help mitigate this effect. Another less obvious potential benefit of NLA has to do with the finite domain size of ferroelectric films, which limits the number of analog states a nanoscale ferroelectric memristor will exhibit. NLA could potentially offer a path to control grain and domain size to very small dimensions, allowing analog behavior down to extremely small device sizes, and although theoretical investigations support this idea [180] it has still to be demonstrated experimentally.

I do believe that the HZO-based FTJ is a highly promising device concept that could play a big role in advancing computation to the next level. As always there are technological challenges to be addressed, and at the time of writing, I currently envision the following primary future developments beyond the scope of this thesis: Firstly, the robustness of the material stack should be further improved, as even minute degradation of the interfaces will impact the energy landscape of the tunnel barrier which directly translates to a change in resistance. This especially affects the TER endurance which currently presents a major challenge as it rapidly decreases with cycling. The use of exciting materials such as RuO_2 which tends to reduce rather than oxidize could be an interesting approach to capture oxygen vacancies as they are formed and stabilize the device characteristics. Goh et al. demonstrated in their research that the utilization of a RuO_2 electrode showed promise in enhancing polarization, reducing the interfacial dead layer, and lowering oxygen vacancy concentration compared to a TiN electrode [181]. Furthermore, the electrical properties of RuO_2 undergo significant changes based on its structure; the common rutile structure renders it metallic, while first-principle calculations suggest that the fluorite structure transforms it into a semiconducting material [182]. This semiconducting property holds potential significance for device applications as it would allow for semiconductor last processing and barrier modulation in FTJs. Therefore, exploring this material further and assessing its impact on device characteristics represents an intriguing avenue for future research.

Secondly, and probably the most natural progression is to integrate the devices into large two-terminal crossbar arrays to enable external programming and sensing using e.g. an FPGA to demonstrate learning on a real array instead of just simulations. Although this may seem like a straightforward task, the geometry of crosspoint nano-FTJs as we have made them in this thesis has the drawback of having a junction not only on the top surface,

but also on the sides of the bottom electrode. As the devices are sensitive to the exact interface properties, it may be beneficial to conjure a more involved process scheme that allows the formation of the FTJ only on the top side of the bottom electrode. Finally, the footprint of devices should be reduced to enable stochastic switching characteristics which would enable the integration of low-power Spiking Neural Networks (SNN). A challenge in achieving this objective is that the absolute current level in individual nanoscale FTJs is typically extremely low, measured in femtoamperes (fA). To enable the desired scaling, there is a requirement to increase the current density by up to four orders of magnitude, necessitating further thinning down of the ferroelectric thickness. However, this approach introduces a concern related to the TER in a MIM FTJ, as it is expected to experience a significant reduction when direct tunneling becomes the predominant current mechanism [63, 64]. Consequently, there may be a need to modulate both the height and width of the barrier by incorporating a semiconducting electrode. Additionally, the low current levels in scaled FTJs could make them sensitive to noise, thus the impact of e.g. random telegraph noise (RTN) in ultra-scaled FTJ devices is another aspect that we have initiated to study in this thesis but that needs more detailed work.

As the final words of this thesis, I would like to express a sense of joy and honor to have played a small role in expanding humanity's collective knowledge. I aspire that the progress made in the field of ferroelectric materials and devices through this thesis can contribute to addressing the ever-so-pressing, significant societal and environmental challenges that lie ahead.

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APPENDICES

A

Fabrication Details

This appendix contains a detailed outline of the FTJ and vertical FeFET process flows used for the work presented in this thesis.

A.1 MICRO FTJS

The samples are fabricated on highly doped 2-inch silicon wafers (100) diced into 1 cm^2 pieces.

- 40 nm TiN sputtering using AJA Orion 5 with an RPM of 40 (RF power 150 W, 9 sccm Ar flow, ~0.9 nm/min).
- 1:1 alternation of tetrakis(dimethylamino)hafnium (TDMAHf) and Tetrakis(dimethylamino)zirconium (TDMAZr) for X cycles (2X cycles in total) at 200°C in Picosun ALD. Precursor source temperatures at 80°C, pulse times 1.6 s, purge times 5 s, and carrier gas 150 sccm. Water source at RT (normally 25°C), pulse time 0.1 s, purge time 10 s, and carrier gas 150 sccm. Chamber gas flow at 300 sccm, intermediate space 350 sccm, boost 600 sccm with pre-empty 0.5 s, master fill 1.2 s, and post-empty 0 s. Flush reaction space three times. MFC100 and MFC 200 set as master. Put in test sample at 200°C. Add a piece of silicon wafer without TiN for thickness measurement in step 3.
- Measure thickness on Si piece using Woollam RC2 variable angle spectroscopic ellipsometer using incident angles 60°, 65°, and 70° and model Si_JAW/NTVE_JAW (2.1 nm)/Savannah HfO2 Tauc-Lorentz by fitting in wavelength range 400-900 nm.
- 50 nm W CE sputtering using AJA Orion 5 with an RPM of 40 (RF power 100 W, 9 sccm Ar flow, ~6 nm/min).
- Anneal in RTP/FLA/NLA with suitable settings.

- Metal replacement etch with heated H_2O_2 at 60 °C for 60 s followed by NH_4OH at 60 °C for 60 s
- Sample dehydration at 105°C for 5 min on hotplate
- Spin Ma-N 440, 6 krpm 45 s, 1500 rpm/s, recipe: (PO6000)
- Soft bake the resist on a hotplate (95°C, 3 min)
- Top electrode patterning using Mask-less Aligner Heidelberg MLA150
- Develop the resist in ma-D 532/S with continuous stirring (90 + 15 s)
- Rinse in deionized water with continuous stirring (60 s) and blow dry with N_2 gun
- Clean the sample using O_2-plasma ashing in Plasma Preen with cage (30 s, 5 mbar)
- 50 nm W TE sputtering using AJA Orion 5 with an RPM of 40 (RF power 100 W, 9 sccm Ar flow, ~6 nm/min).
- Heated acetone lift-off, larger beaker as a lid, USB if necessary
- Rinse in IPA (30 s) and blow dry with N_2 gun

A.2 NANO FTJS

- **Definition of bottom electrode pads and alignment markers.**
  1. 30 cycles of SiN_x deposition at 200°C (∼300 nm)
  2. Spin Ma-N 440, 6 krpm 45 s, 1500 rpm/s, recipe: (PO6000)
  3. Bake resist at 95 °C, 3 min
  4. Exposure using MLA 150, Laser = 375 nm, dose = 2000 mJ/cm^2
  5. Development 90+15 s in Ma-D 532/s + millipore water 60 s
  6. Optical inspection in microscope
  7. Plasma preen, 30 s 5 mbar O_2 with cage
  8. E-beam evaporation, 50 nm Pd, Temescal
  9. Lift-off hot acetone 15 min + 1 min IPA, USB if required
  10. Plasma preen 60 s 5 mbar O_2, without cage
- **Definition of bottom electrode arms**
  1. RF sputtering of 20 nm TiN at 150 W, 9 sccm Ar-flow, rotation = 4, AJA ORION.
  2. ALD of 5 nm SiO_2 (50 cycles) at 100 °C, Fiji
  3. Spin S1813, 5000 rpm 60 s, recipe: PO5000
  4. Bake resist 115 °C 90 s
  5. Exposure using MLA 150, Laser = 405 nm, dose = 200 mJ/cm^2
  6. Development in MF319 50 s, millipore water 60 s
  7. Hard bake resist at 120 °C, 15 min (improve adhesion)
  8. Plasma preen 60 s 5 mbar O_2, with cage

9. Dry etching TiN and SiO_2, SF_6
10. Remover 1165 90 °C, 30 min, DIW 2 min, IPA 1 min
11. Tepla, 15 min, 800 W O_2 plasma
12. Spin coat AR-N 7520.07, 2000 rpm 60 s
13. Bake at 85 °C 1 min
14. EBL exposure bottom electrode arms
15. Development in MF319 4:1 60 s, rinse in DIW 30 s twice
16. Plasma preen 30 s 5 mbar O_2, with cage
17. Dry-etching of TiN and SiO_2
18. Tepla 15 min, 800 W O_2 plasma
19. Etch SiO_2 in BOE 1:10 15s (just before HZO deposition), DIW 60 s

- **High-k deposition**
  1. HZO deposition by alternating 1:1 tetrakis(dimethylamino)hafnium (TDMAHf) and Tetrakis(ethylmethylamino)zirconium (TEMAZr) with H_2O as oxidizer for 45 cycles at 200°C using Picosun ALD
- **Deposition of crystallization electrode**
  1. Deposition of 50 nm W by DC sputtering, 100 W, 9 sccm Ar-flow, AJA Orion
- **Definition of bottom electrode via**
  1. Spin S1813, 5000 rpm 60 s, recipe: PO5000
  2. Soft bake on a hotplate 115°C, 90 s
  3. Exposure using MLA 150, Laser: 405 nm, dose = 200 mJ/cm^2
  4. Development in MF319 50 s, DIW 60 s
  5. Hard bake resist at 120 °C, 15 min (improve adhesion)
  6. Plasma preen 60 s 5 mbar O_2, with cage
  7. Dry-etching of W SF_6
  8. Remover 1165 90 °C, 30 min, DIW 2 min, IPA 1 min
  9. Tepla 15 min, 800 W O_2 plasma
  10. HZO etch, BOE 1:10, 5 min
- **Annealing and CE removal**
  1. RTP annealing at 550 °C, 30 s, N_2 environment
  2. Metal replacement etch with heated H_2O_2 at 60 °C for 60 s followed by NH_4OH at 60 °C for 60 s
- **Marker Visibility**
  1. Deposition of 50 nm W by DC sputtering, 100 W, 9 sccm Ar-flow, rotation 40, AJA Orion,
  2. ALD of 5 nm SiO_2 (50 cycles) at 100 °C, Fiji
  3. Spin S1813, 5000 rpm 60 s, recipe: PO5000
  4. Soft bake on a hotplate 115°C, 90 s

5. Exposure using MLA 150, Laser: 405 nm, dose = 200 mJ/cm^2
6. Development in MF319 50 s, DIW 60 s
7. Hard bake resist at 120 °C, 15 min (improve adhesion)
8. Plasma preen 60 s 5 mbar O_2, with cage
9. Dry-etching of W and SiO_2 with SF_6
10. Remover 1165 90 °C, 30 min, DIW 2 min, IPA 1 min
11. Tepla 15 min, 800 W O_2 plasma

- **Top electrode definition arms & pads**
  1. Spin coat AR-N 7520.07, 2000 rpm 60 s
  2. Bake at 85 °C 1 min
  3. EBL exposure top electrode arms and pads
  4. Development in MF319 4:1 60 s, rinse in DIW 30 s twice
  5. Plasma preen 30 s 5 mbar O_2, with cage
  6. Dry-etching of SiO_2 and W
  7. Tepla 15 min, 800 W O_2 plasma
  8. Etch SiO_2 in BOE 1:10 15s, DIW 60 s
- **Deposition of probing metal**
  1. Spin Ma-N 440, 6 krpm 45 s, 1500 rpm/s, recipe: (PO6000)
  2. Bake resist at 95 °C, 3 min
  3. Exposure using MLA 150, Laser: 375 nm, dose = 2000 mJ/cm^2
  4. Development 90+15 s in Ma-D 532/s + millipore water 60 s
  5. Optical inspection in microscope
  6. Plasma preen, 30 s 5 mbar O_2 with cage
  7. E-beam evaporation, Ti/Pd/Au (5/5/200 nm), Temescal
  8. Lift-off hot acetone 15 min + 1 min IPA, USB if required
  9. Plasma preen 60 s 5 mbar O_2, without cage

A.3 VERTICAL NW FEFET

The samples are fabricated on lightly p-doped 4-inch silicon wafers (111). A low-resistive 300 nm-thick Sn-doped InAs buffer layer is grown by MOVPE (n^{++}, ~5×10^{19} cm^{-3}). EBL patterning, evaporation, and lift-off are used to deposit 15 nm thick gold seeds. Varying the gold seed size across the sample allows for variation in both the diameter and length of the grown core. The 4-inch wafer is diced into 1×1 cm^2 pieces where InAs nanowires are grown by Vapor-Liquid-Solid (VLS) growth using MOVPE with trimethylindium (TMIn) and arsine (AsH_3) as the In and As precursor, respectively. The wires are designed 500 nm long with the bottom 200 nm non-intentionally doped (nid) while the upper 300 nm drain being n^{++}-doped using triethyltin

(TESn) as precursor. During the growth of the highly doped top segment, an approximately 3-nm-thick highly doped shell overgrows the channel region. The nanowire growth has been performed by Dr. Johannes Svensson or Zhongyunshen Zhu.

- **Removal of the highly doped shell** (etches 1-2 nm per cycle and is repeated until the shell is etched away at the channel).
  1. Oxidize the InAs surface by ozone using UV-Ozone Cleaning system UVOH 150 at an elevated temperature (50°C, 10 min, O_2 flow of 500 sccm)
  2. Etch the InAs-oxide with HCl:IPA 1:10 (30 s)
  3. Rinse in IPA (30 s) and blow dry with N_2 gun
- **Gate stack deposition**
  1. HZO deposition by alternating 1:1 tetrakis(dimethylamino)hafnium (TDMAHf) and Tetrakis(ethylmethylamino)zirconium (TEMAZr) with H_2O as oxidizer for 75 cycles (150 cycles in total) at 200°C using Picosun ALD
  2. 60 nm W sputtered using AJA Orion 5 with rotation (DC power 100 W, 16 sccm Ar flow, ~0.09 nm/s)
- **Gate length definition**
  1. Spin on S1813 resist (60 s, 4000 rpm, 1000 rpm/s)
  2. Hard bake the S1813 on a hotplate (120°C, 15 min)
  3. Thin down S1813 using O-plasma in Trion Sirius T2 Plus RIE using Intellevation LEP400 laser interferometric etch depth monitor for thickness control (~0.66 nm/s, 300 mTorr). Use edge pieces to avoid uneven etching.
  4. Remove the exposed tungsten on top of the nanowire by SF_6/Ar plasma in Trion Sirius T2 Plus RIE (45 s, 45/10 sccm, 140 W, 185 mTorr)
  5. Etch residual Teflon from the SF_6 etch using O-plasma ashing in Plasma Preen without cage (60 s, 5 mbar)
  6. Remove the S1813 with acetone (10 min)
  7. Rinse in IPA (30 s)
- **Gate pad definition**
  1. Spin on S1813 resist (60 s, 4000 rpm, 1000 rpm/s)
  2. Soft bake on a hotplate (115°C, 90 s)
  3. Pattern the resist using Mask aligner MJB4 (6 s, 20 mW/cm^2)
  4. Develop the S1813 in MF319 (80 s)
  5. Rinse in H_2O (80 s)
  6. Hard bake on a hotplate (120°C, 15 min)

7. Clean the sample using O_2-plasma ashing in Plasma Preen without cage (30 s, 5 mbar)
8. Remove the exposed tungsten by SF_6/Ar plasma in Trion Sirius T2 Plus RIE (45 s, 45/10 sccm, 140 W, 185 mTorr)
9. Etch residual Teflon from the SF_6 etch using O-plasma ashing in Plasma Preen without cage (60 s, 5 mbar)
10. Remove the S1813 with acetone (10 min)
11. Rinse in IPA (30 s)

- **Source via etch**
  1. Spin on S1813 resist (60 s, 4000 rpm, 1000 rpm/s)
  2. Soft bake on a hotplate (115°C, 90 s)
  3. Pattern the resist using Mask aligner MJB4 (6 s, 20 mW/cm^2)
  4. Develop the resist in MF319 (80 s)
  5. Rinse in H_2O (80 s)
  6. Hard bake on a hotplate (120°C, 15 min)
  7. Clean the sample using O_2-plasma ashing in Plasma Preen without cage (30 s, 5 mbar)
  8. Etch the HZO by BOE 1:30 (~0.6 nm/min)
  9. Rinse in deionized water (30 s)
  10. Remove the S1813 with acetone (10 min)
  11. Rinse in IPA (30 s)
- **Etch HZO on top of nanowire**
  1. Spin on S1813 resist (60 s, 4000 rpm, 1000 rpm/s)
  2. Hard bake the resist on a hotplate (120°C, 15 min)
  3. Thin down S1813 using O-plasma in Trion Sirius T2 Plus RIE using Intellevation LEP400 laser interferometric etch depth monitor for thickness control (~0.66 nm/s, 300 mTorr). Use edge pieces to avoid uneven etching.
  4. Etch the HZO by BOE 1:30 (~0.6 nm/min)
  5. Rinse in H_2O (30 s)
  6. Clean the sample in acetone to remove the resist (10 min)
  7. Rinse in IPA (30 s)
- **Annealing in RTP (550°C, 30 s)**
- **Top spacer deposition**
  1. 300 cycles Al_2O_3 using trimethylaluminium (TMA) as precursor and H_2O oxidizer at 200°C in Picosun ALD
- **Top spacer source and gate vias**
  1. Spin on S1813 resist (60 s, 4000 rpm, 1000 rpm/s)
  2. Soft bake on a hotplate (115°C, 90 s)

3. Pattern the resist using Mask aligner MJB4 (6 s, 20 mW/cm^2)
4. Develop the resist in MF319 (80 s)
5. Rinse in H_2O (80 s)
6. Hard bake on a hotplate (120°C, 15 min)
7. Clean the sample using O_2-plasma ashing in Plasma Preen without cage (30 s, 5 mbar)
8. Etch the Al_2O_3 by BOE 1:30 (~0.3 nm/s)
9. Rinse in deionized water (30 s)
10. Remove the S1813 with acetone (10 min)
11. Rinse in IPA (30 s)

- **Top spacer top etch** (to expose drain contact)
  1. Spin on S1813 resist (60 s, 4000 rpm, 1000 rpm/s)
  2. Hard bake on a hotplate (120°C, 15 min)
  3. Thin down S1813 using O-plasma in Trion Sirius T2 Plus RIE using Intellevation LEP400 laser interferometric etch depth monitor for thickness control (~0.66 nm/s, 300 mTorr). Use edge pieces to avoid uneven etching.
  4. Etch the Al_2O_3 by BOE 1:30 (~0.3 nm/s)
  5. Rinse in deionized water (30 s)
  6. Clean the sample in acetone to remove the resist (10 min)
  7. Rinse in IPA (30 s)
- **Top metal definition**
  1. Etch with HCl:IPA 1:10 (30 s) to remove InAs oxide on top of the nanowire to improve the metal-semiconductor contact
  2. Metal sputtering of Ni/Au, thickness 10/200 nm using AJA Orion 5 with rotation
  3. Spin on S1813 resist (60 s, 4000 rpm, 1000 rpm/s)
  4. Soft bake on a hotplate (115°C, 90 s)
  5. Pattern the S1813 using Mask aligner MJB4 (6 s, 20 mW/cm^2)
  6. Develop the S1813 in MF319 (80 s)
  7. Rinse in deionized water (80 s)
  8. Hard bake on a hotplate (120°C, 15 min)
  9. Clean the sample using O_2-plasma ashing in Plasma Preen without cage (30 s, 5 mbar)
  10. Etch Au using 1:2:17 KI:I_2:H_2O (35 s)
  11. Rinse in deionized water (30 s)
  12. Clean the sample in acetone to remove the resist (10 min)
  13. Rinse in IPA (30 s)
  14. Etch Ni using 2.5:2.5:1:15 CH_3COOH:HNO_3:H_2SO_4:H_2O (100 s)

15. Rinse in deionized water (30 s)

B

Measurement Setups

In this appendix, the measurement setups for important measurement are explained, so that future researchers may reassemble the setups.

SCRIPTING

For all electrical measurements described in section 4.2 (except C-V and cryogenic) an Agilent B1500A semiconductor analyser coupled with an MPI TS2000-SE semi automatic probe station was used. The B1500A is equipped with HRSMUs, ASU and WGFMU with RSU. The built-in GUI EasyExpert is great for simple measurements and provides a good place to start. However, for more extensive measurements it is much more efficient to connect remotely through GPIB and script the measurement protocols instead. The C++ libraries provided by the manufacturer allow control of the B1500 system and its containing modules. To enable access to this approach and to improve usability for new users, I developed the measurement setup *Athle's Advanced Automatic Ferroelectric Measurments (AAA-FEM)* in Visual Studios, with the goal of providing vast applicability and a great starting point that enables users to develop their own tailored measurements. The developed functionalities of the repository are as follows:

- **Stage control**
- set contact height, skate, and hover
- load in sub-site coordinate list from file
- sub-site move

Before this feature can be used the home position of the stage must be defined in the Sentio software of the MPI.

- **Measurements**

- Polarization measurements
- Endurance
- Polarization switching dynamics
- WGFMU control
- Wake-up pulsing
- Potentiation and depression by amplitude, pulse width, or repetition modulation.
- Resistance-voltage hysteresis measurements
- I-V sweeps
- I/V-t sampling measurements

The scripted measurements enable more advanced measurement protocols than what can be done directly with EasyExpert as well as automatic gathering of data for many devices which enable statistics to be made with a reasonable effort. In principle any combination of measurements can be scripted, and this was used to combine the pulsing capabilities of the WGFMU for programming with high-precision readout of low current levels using HRSMU for the FTJ devices.

CV AND CRYOGENICS

For CV measurements an Agilent 4294A Impedance Analyzer controlled via a labview interface was used. It should be noted that CV measurements can also be carried out using the B1500 setup, however, for consistency and comparability with previous results, the Agilent 4294A was used for all CV measurements. The cryogenic measurements were carried out in a Lake Shore CRX-6.5 probe station.

C

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MOORE'S LAW PLOT

The data plotted in Figure 1.1 up to the year 2010 was collected and plotted by M. Horowiz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten. The data between 2010-2021 was collected by K. Rupp.

The data was fetched from the github repository: https://github.com/karlrupp/microprocessor-trend-data/tree/master, with the creative commons license agreement avaliable at https://github.com/karlrupp/microprocessor-trend-data/blob/master/LICENSE.txt

PROXIMITY EFFECTS BLENDER 3D

The geometry node setup for the proximity effect used in 1.3(a) was developed and provided by Dr. Joseph G. Manion at CG Figures. under the CC0 1.0 license.

C.1 FIGURES FROM MANUSCRIPTS

Figure 5.3a is directly taken from Paper IV and Figure 5.3b,d and Figure 5.4d are directly taken from Paper V. Figure 5.5 is directly taken from Paper VII.

C.2 FRONT COVER

The neuron on the front cover was remodeled based on the "Multipolar neuron" by Alain Sorazu, licensed under Creative Commons Attribution-ShareAlike. The updated model is available from me under the same license by reasonable request.