Low-frequency noise in ferroelectric III-V vertical gate-all-around FETs

Zhu, Zhongyunshen; Mamidala, Karthik Ram; Persson, Anton E. O.; Wernersson, Lars-Erik

Published in:
IEEE Electron Device Letters

DOI:
10.1109/LED.2025.3546165

2025

Document Version:
Peer reviewed version (aka post-print)

Low-Frequency Noise in Ferroelectric III-V Vertical Gate-All-Around FETs

Zhongyunshen Zhu, Mamidala Karthik Ram, Anton E. O. Persson and Lars-Erik Wernersson

***Abstract*—In this letter, we demonstrate low-frequency noise (LFN) characterization of an InAs vertical gate-all-around hafnium-zirconium oxide (HZO) ferroelectric field-effect transistor (FeFET). The LFN characteristics are investigated before and after ferroelectric switching for up to 1000 cycles in the FeFET. The evolution of such cycling reveals distinct differences in the LFN for the two polarization states. The LFN is found to change more during cycling in the high-V_T state than in the low-V_T state, where the latter has an increased LFN already at various current levels during the first switching cycle. Our findings indicate that the mobility fluctuation and carrier number fluctuation are the dominant source of the LFN for low currents in the off-state and near-V_T current levels, respectively, verified by fitting the experimental data to the different models.**

***Index Terms*—Low-frequency noise, III-V, Gate-all-around, FeFETs**

I. Introduction

HAFNIUM-based ferroelectric field-effect transistors (FeFETs) have garnered extensive interest as they are promising candidates for non-volatile memory, in-memory computing, and neuromorphic applications owing to their fast switching speeds, low energy consumption, and CMOS compatibility [1], [2], [3]. As high-mobility channel materials, III-Vs such as In(Ga)As have been widely used for radio frequency switches and low-noise amplifiers, and their applications have recently expanded into the cryogenic regime with exceptional potential for quantum computing [4], [5]. Integrating ferroelectric hafnium-zirconium oxide (HZO) with III-Vs can introduce reconfigurable functionality to III-V-based devices, enabling high-speed and low-power operations. This device integration has been intensively investigated through both III-V metal-oxide-semiconductor (MOS) capacitance [6], [7], [8] and FeFETs [9], [10], [11]. To reduce device footprint for high-density integration while improving gate control, vertical III-V nanowire gate-all-around (GAA) FeFETs have also been demonstrated with extensive device characterization [11], [12] and application implementations [13], [14]. Recently, the low frequency noise (LFN) or 1/*f* noise, commonly used as a quality metric to assess defect dynamics in the gate oxide and transistor reliability [15], [16], has been actively explored in HZO-based ferroelectric diodes and FeFETs due to the growing need to better understand how trapping effects influence endurance performance [17], [18], [19], [20]. However, to the best of our knowledge, the LFN has not been studied for III-V-based ferroelectric transistors, especially those with a scaled vertical architecture, where such insights are urgently needed.

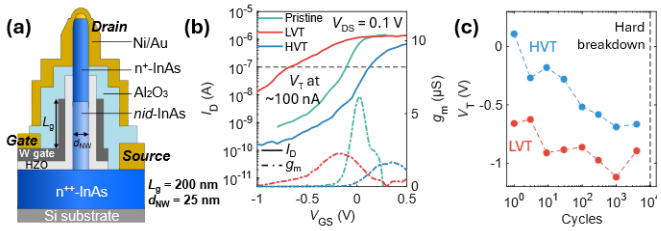

Fig. 1. (a) The Schematic of a vertical GAA FeFET based on a single InAs nanowire. (b) Transfer characteristics before (pristine) and after ferroelectric switching in LVT and HVT states, respectively. (c) V_T as a function of ferroelectric switching cycles.

In this work, we present a systematic study of the LFN characterization of an InAs vertical GAA FeFET over 1000 switching cycles. Earlier studies have shown that 1/*f* noise characterization enables monitoring of oxide trap density along the gate stack in III-V vertical GAA MOSFETs [21], [22]. Here, similar analysis is applied to InAs FeFETs. The dynamic trapping/de-trapping process in the ferroelectric gate oxide allows us to understand how the oxide trap density (N_T) is affected by field cycling and the potential origin of the LFN.

II. Device Structure

Fig. 1(a) illustrates a schematic of a vertical InAs GAA FeFET. The device consists of a 200-nm non-intentionally doped (*nid*) InAs and a 300-nm n^+-doped InAs segment at the top, forming the channel and drain, respectively, while a 260-nm-thick n^{++}-InAs buffer layer serves as the source. A 12-nm ferroelectric HZO ($Hf_{0.5}Zr_{0.5}O_2$) film is used for the gate oxide. Detailed fabrication steps have been reported earlier [11].

III. Electrical Characterization and Analysis

Electrical characterization was performed using a Keysight B1500A Parameter Analyzer consisting of B1530A waveform generator/fast measurement units (WGFMUs). The transfer characteristics of ferroelectric switching are shown in Fig. 1(b). By programing the polarization in the HZO gate oxide using ±5

This work was supported in part by Swedish Research Council Electronics beyond kT/q (Grant Agreement No. 2016-06186) and in part by the European Research Council DYNAMISM (Grant Agreement No. 101019147).

All authors are with the Department of Electrical and Information Technology, Lund University, SE-221 00 Lund, Sweden (e-mail: zhongyunshen.zhu@eit.lth.se).

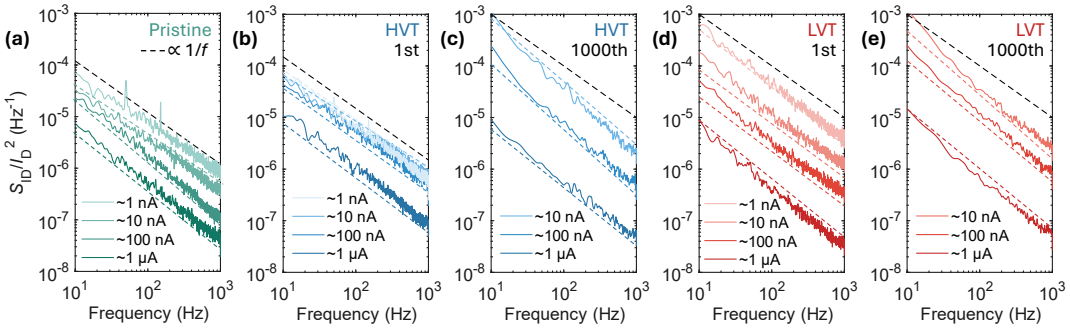

Fig. 2. Frequency-dependent normalized drain current noise power spectral density (S_{ID}/I_D^2) of the FeFET at different current levels in various states: (a) pristine, (b) HVT first cycle, (c) HVT 1000th cycle, (d) LVT first cycle, and (e) LVT 1000th cycle. Each curve represents an averaged result from 10 measurements. The colored dashed lines serve as guides to indicate the trend.

V/100 ns square pulse, a ferroelectric hysteresis with a memory window of ~0.8 V is measured by defining the threshold voltage (V_T) at $I_D \approx 100$ nA. Compared to the pristine state, a similar on-current of 1.5 μA with reduced (transconductance) g_m are observed in both the low-V_T (LVT) and high-V_T (HVT) state. The g_m reduction is a result of degradation in gate modulation after ferroelectric switching mainly due to more charge trapping/de-trapping in the gate oxide, which has been also found in Si FeFETs [23]. A relatively high subthreshold swing (SS) is measured in both the on- and off-state for all states, consistent with and explained by our previous work using the same device structure [11]. Fig. 3(c) shows an endurance of >4000 in the InAs FeFET, limited by hard breakdown after 10^4 cycles. A likely explanation is that HZO annealed at higher temperatures becomes prone to leakage. In contrast, an improved endurance was observed in a device with the same HZO but annealed at a lower temperature [12].

For the LFN measurements, a fast current measurement with remote sense/switch units in the WGFMU was used for time-domain I_D characteristics of the FeFET at various V_{GS}. The I_D noise power spectral density (S_{ID}) was then obtained using fast Fourier transform by employing the Welch method [24], [25]. Several devices were measured, and each I_D-t measurement was repeated 10 times to achieve an average S_{ID} at each I_D level. The normalized I_D noise power spectral density (S_{ID}/I_D^2) of the FeFET for different states (pristine, low- and high-V_T states) is shown in Fig. 2, revealing a strong characteristic $1/f^{\gamma}$ behavior where $\gamma = -\partial \ln S_{ID}/\partial \ln f$. Three or four different I_D levels ranging from 1 nA to 1 μA were selected to show the LFN in the off-state, flat-band state ($V_{GS} \approx V_T$), and on-state, respectively, with γ varying from 0.9 to 1.3. A γ value nearly 1 typically suggests a relatively uniform distribution of N_T along the HZO gate oxide [19], [26]. During ferroelectric cycling, the minimum off-currents in both polarization states increase due to charge trapping, exceeding 1 nA after 1000 cycles. Notably, in the first cycle, S_{ID}/I_D^2 at $I_D \approx 1$ nA increases further in the LVT state, while it remains relatively low in the HVT and pristine state. This trend correlates with the SS characteristics observed in these states as shown in Fig. 1(b).

Figs. 3(a-e) show S_{ID}/I_D^2 at various I_D levels with $f = 10$ Hz in different cases. S_{ID}/I_D^2-I_D dependencies at higher frequencies, such as 100 Hz, exhibits nearly identical trends and is therefore only presented in the HVT state. Additionally, a frequency of 10 Hz is commonly used for LFN analysis [18], [21]. The results indicate that the LFN remains similar at a high I_D level while it significantly increases at the I_D level around and below V_T in both polarization states with cycling. Therefore, we mainly focus the analysis on LFN characteristics at currents in the sub- and near-V_T current levels. For MOSFETs, LFN is typically described by two mechanisms: carrier number fluctuation (CNF) and mobility fluctuation (MF) [15], [27]. CNF is primarily driven by the variations of channel potential energy resulting from electrons tunneling in and out of traps in the gate oxide and the channel itself due to defects in the semiconductor, which causes I_D fluctuation. According to this model, S_{ID}/I_D^2 is expected to be proportional to $(g_m/I_D)^2$ as described below:

$$\frac{S_{ID}}{I_D^2} = S_{V_{fb}} \frac{g_m^2}{I_D^2}. \quad (1)$$

The proportional coefficient S_{Vfb} represents the flatband voltage (V_{fb}) noise power spectral density and it is also related to the device parameters as given by

$$S_{V_{fb}} = \frac{q^2 kT\lambda N_T}{f^{\gamma} L_g W_g C_{ox}^2}, \quad (2)$$

where q is the elemental charge, k the Boltzmann constant, T the temperature, $\lambda \approx 0.13$ nm the tunneling attenuation length considering the tunneling barrier of HZO, W_g the channel width, and C_{ox} the gate oxide capacitance. On the other hand, S_{ID}/I_D^2 is usually found to be proportional to $1/I_D$ in the MF model:

$$\frac{S_{ID}}{I_D^2} = \frac{\alpha_H \mu_{eff} 2kT}{f L_g^2 I_D}, \quad (3)$$

where α_H is Hooge's parameter, μ_{eff} the effective channel mobility of the device.

Given the above models, we found that in our FeFETs S_{ID}/I_D^2-I_D fits well with $(g_m/I_D)^2$ at high currents while follows $1/I_D$ trend at low currents before [Fig. 3(a)] and after ferroelectric switching during the first cycle in both states [Figs. 3(b) and (d)]. After 1000 cycles, S_{ID}/I_D^2 significantly increases in the subthreshold region, and fits well also with $(g_m/I_D)^2$ in both states [Figs. 3(c) and (e)]. These results indicate that CNF becomes the dominant source of the LFN in a wide I_D range during cycling, while MF mainly occurs at low I_D levels in the subthreshold region, particularly for the first cycle.

Notably, the impact of ferroelectric switching cycling on the LFN is different for the two polarization states. For the LVT state, S_{ID}/I_D^2 increases rapidly for low I_D levels [Fig. 3(d)] in the first cycle but remains almost consistent after 1000 cycles [Fig. 3(e)]. This leads to a high α_H already during the first cycle and only a slight increase after 1000 cycles [Figs. 3(d-e)]. In the case of the HVT state, except for I_D levels above V_T, S_{ID}/I_D^2 increases significantly after 1000 cycles [Fig. 3(c)] as compared to that in the first cycle [Fig. 3(b)]. Similarly, α_H is almost

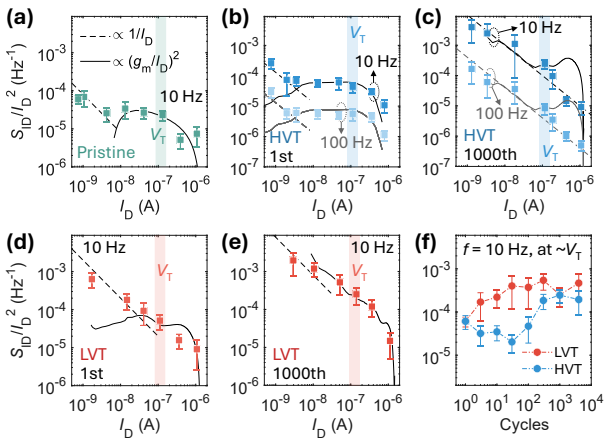

Fig. 3. S_{ID}/I_D^2 versus I_D in various states: (a) pristine, (b) HVT first cycle, (c) HVT 1000th cycle, (d) LVT first cycle, and (e) LVT 1000th cycle. (f) S_{ID}/I_D^2 versus switching cycles in the two polarized states. The error bars denote the standard deviation of 10 measurements for each date point.

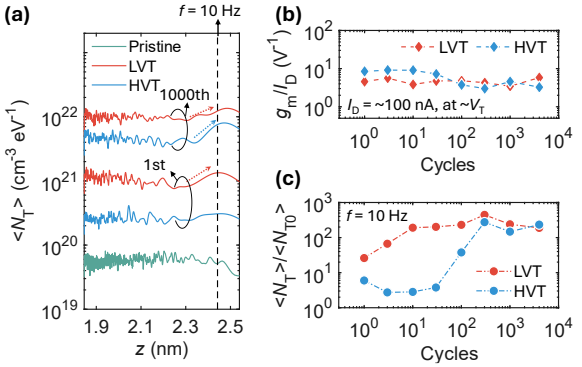

Fig. 4. (a) Average N_T ($<N_T>$) versus oxide depth z (z = 0 nm defined as the channel/HZO interface) before and after ferroelectric switching. Dashed arrows indicate the increase of $<N_T>$ after $z \approx 2.3$ nm. (b) g_m/I_D and (c) $<N_T>/<N_{T0}>$ as a function of switching cycles in the two states. All plotted data are obtained at V_T with $I_D \approx 100$ nA.

identical to the pristine state with an order of 10^{-5}, which is in line with other reported III-V nanowire MOSFETs [22], [28], but increases by nearly two orders of magnitude after 1000 cycles [Figs. 3(b-c)]. The distinct difference of α_H change in the two states likely arises from different polarization effects in the naturally n-type InAs channel. In the LVT state, strong channel accumulation leads to high HZO polarization, enhancing remote phonon scattering and increasing α_H immediately after switching [18]. Conversely, the n-type channel struggles to achieve strong inversion, resulting in reduced polarization and a lower α_H in the HVT state. During cycling, an increase in interface charges may compensate for the hole deficiency at the channel interface to enhance the polarization in the HZO, thereby increasing MF or α_H substantially after 1000 cycles. Additional impact from asymmetric remanent polarization may exist in HZO of our scaled FeFETs [29], leading to different effects on LFN characteristics in the two states.

Apart from low I_D levels, the LFN in the I_D regime near V_T gradually increases during cycling and reaches saturation after 1000 cycles in both polarization states [Fig. 3(f)]. Unlike the trend in the LVT state where S_{ID}/I_D^2 increases immediately after the first cycle and saturates after 300 switching cycles, the LFN firstly decreases slightly and then increases rapidly after 30 cycles until saturation in the HVT state. At ~V_T, the LFN is expected to primarily originate from CNF as S_{ID}/I_D^2 fits well with $(g_m/I_D)^2$ in all cases shown in Fig. 3. Thus, it is reasonable to correlate this to charge trapping/de-trapping in the HZO gate oxide, which is typically influenced by the ferroelectric switching [30], [31].

To understand the evolution of the LFN at ~V_T during ferroelectric cycling, we carried out further analysis on the relationship between N_T and S_{ID}/I_D^2 based on Equation (1-2). Fig. 4(a) shows that $<N_T>$ (N_T averaged by 10 measurements) is almost constant along the depth of the gate oxide (z) from the interface in all cases, indicating a uniform oxide trap distribution corresponding to $\gamma \approx 1$ as discussed. At 10 Hz, $<N_T>$ in the pristine state is ~5×10^{19} cm^{-3} eV^{-1}, in line with GAA InAs nanowire MOSFETs with HfO_2 gate dielectric [21] despite somewhat higher than other III-V implementations [32]. This indicates no substantial degradation when replaced with HZO gate oxide for InAs nanowire FeFETs. After ferroelectric switching for 1000 cycles, the increased charge trapping caused by defects in the ferroelectric HZO gate oxide mainly leads to a rise of about two orders of magnitude in $<N_T>$ with a similar level (near 10^{22} cm^{-3} eV^{-1}) in both states [Fig. 4(a)]. A potential overestimation of $<N_T>$ may arise from additional noise sources, such as I_D fluctuations in the access region [33], which contribute to S_{ID}/I_D^2 independently of cycling. Unlike the sharp increase in $<N_T>$ observed in the LVT state after the first cycle, the HVT state exhibits only a slight initial rise, followed by a significant increase after 100 cycles. This could stem from the negative V_T shift observed during cycling in the HVT state [Fig. 1(c)], as noted in other scaled HZO-based FeFETs [34], [35], [36]. This shift may lead to different trap distributions for the two states during the first cycle, but a similar distribution after repeated switching due to the reduced memory window and hence a similar V_T.

Notably, $<N_T>$ tends to rise from $z \approx 2.3$ nm for both states after 1000 cycles but only for the LVT state in the first cycle [Fig. 4(a)]. This accounts for the lower γ (≈ 0.9) in the HVT state during the first cycle and equally high γ (≈ 1.3) in both states after 1000 cycles (Fig. 2). According to CNF model in Equation (1-2), the LFN mainly depends on $<N_T>$ and g_m/I_D, both of which are thus examined in relation to ferroelectric switching cycles. Fig. 4(b) shows that g_m/I_D remains almost identical at ~V_T during cycling in both states. On the other hand, $<N_T>$ change with respect to that in the pristine state ($<N_{T0}>$) resembles the trend of S_{ID}/I_D^2 as a function of cycles [Fig. 4(c)]. The result confirms that N_T increase at corresponding V_T for both polarization states is the key source of the LFN increase.

IV. Conclusion

We present a systematic study on the LFN characteristics of an InAs vertical GAA FeFET. The 1/f noise level before ferroelectric switching is in line with previous reports of InAs GAA MOSFETs, indicating no degradation of HZO quality during integration. After 1000 cycles of ferroelectric switching, the 1/f noise increases by nearly one order of magnitude in the subthreshold region, which is mainly correlated to increased mobility fluctuations and oxide trap density. These findings may provide valuable insights for further optimization of fabrication processes and write/read operation in scaled FeFETs to reduce the impact of ferroelectric cycling on the LFN, thus improving device reliability.

REFERENCES

[1] A.I. Khan, A. Keshavarzi, and S. Datta, "The future of ferroelectric field-effect transistor technology," *Nat. Electron.*, vol. 3, no. 10, pp. 588–597, Oct. 2020, doi: 10.1038/s41928-020-00492-7.

[2] H. Mulaosmanovic, E.T. Breyer, S. Dünkel, S. Beyer, T. Mikolajick, and S. Slesazeck, "Ferroelectric field-effect transistors based on HfO2: a review," *Nanotechnology*, vol. 32, no. 50, p. 502002, Sep. 2021, doi: 10.1088/1361-6528/ac189f.

[3] S. Dünkel, M. Trentzsch, R. Richter, P. Moll, C. Fuchs, O. Gehring, M. Majer, S. Wittek, B. Müller, T. Melde, H. Mulaosmanovic, S. Slesazeck, S. Müller, J. Ocker, M. Noack, D. . -A. Löhr, P. Polakowski, J. Müller, T. Mikolajick, J. Höntschel, B. Rice, J. Pellerin, and S. Beyer, "A FeFET based super-low-power ultra-fast embedded NVM technology for 22nm FDSOI and beyond," in *2017 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2017, p. 19.7.1-19.7.4. doi: 10.1109/IEDM.2017.8268425.

[4] E. Cha, A. Ferraris, P. Mueller, H. . -C. Han, D. Caimi, M. Sousa, C. Enz, and C. B. Zota, "Cryogenic InGaAs HEMTs with Reduced On-Resistance using Strained Ohmic Contacts," in *2023 International Electron Devices Meeting (IEDM)*, Dec. 2023, pp. 1–4. doi: 10.1109/IEDM45741.2023.10413869.

[5] A. Ferraris, E. Cha, P. Mueller, T. Morf, M. Prathapan, M. Sousa, H. . -C. Han, C. Enz, and C. B. Zota, "Cryogenic InGaAs HEMT-Based Switches For Quantum Signal Routing," in *2022 International Electron Devices Meeting (IEDM)*, Dec. 2022, p. 4.6.1-4.6.4. doi: 10.1109/IEDM45625.2022.10019536.

[6] M. Karthik Ram, H. Dahlberg, and L. -E. Wernersson, "Cryogenic Ferroelectricity of HZO Capacitors on a III–V Semiconductor," *IEEE Electron Device Lett.*, vol. 45, no. 10, pp. 1827–1830, Oct. 2024, doi: 10.1109/LED.2024.3448378.

[7] A. E. O. Persson, S. Andrić, L. Fhager, and L. -E. Wernersson, "RF Characterization of Ferroelectric MOS Capacitors," *IEEE Electron Device Lett.*, vol. 45, no. 9, pp. 1653–1656, Sep. 2024, doi: 10.1109/LED.2024.3428971.

[8] K. Ko, D. -H. Ahn, H. Suh, B. -K. Ju, and J. -H. Han, "Effects of Al2O3 Interfacial Layer Thickness for HZO/InGaAs Ferroelectric Capacitors With Superior Polarization and MOS Interface Properties," *IEEE Trans. Electron Devices*, vol. 70, no. 12, pp. 6237–6243, Dec. 2023, doi: 10.1109/TED.2023.3326428.

[9] K. Ko, D. -H. Ahn, J. -Y. Jeong, B. -K. Ju, and J. -H. Han, "Design Points of InGaAs MFMIS Tunnel FET for Large Memory Window and Stable Ferroelectric Memory Operation," *IEEE Trans. Electron Devices*, vol. 71, no. 10, pp. 6435–6441, Oct. 2024, doi: 10.1109/TED.2024.3449255.

[10] P. Huang, M. Y. Chen, Q. H. Luc, J. Y. Wu, N. A. Tran, and E. Y. Chang, "Radio Frequency Characteristics of InGaAs FE-FETs With Scaled Channel Length," *IEEE Trans. Electron Devices*, vol. 70, no. 2, pp. 443–448, Feb. 2023, doi: 10.1109/TED.2022.3228971.

[11] A. E. O. Persson, Z. Zhu, R. Athle, and L. -E. Wernersson, "Integration of Ferroelectric HfxZr1-xO2 on Vertical III-V Nanowire Gate-All-Around FETs on Silicon," *IEEE Electron Device Lett.*, vol. 43, no. 6, pp. 854–857, Jun. 2022, doi: 10.1109/LED.2022.3171597.

[12] Z. Zhu, A.E.O. Persson, and L.-E. Wernersson, "Sensing single domains and individual defects in scaled ferroelectrics," *Sci. Adv.*, vol. 9, no. 5, p. eade7098, Feb. 2023, doi: 10.1126/sciadv.ade7098.

[13] Z. Zhu, A.E.O. Persson, and L.-E. Wernersson, "Reconfigurable signal modulation in a ferroelectric tunnel field-effect transistor," *Nat. Commun.*, vol. 14, no. 1, p. 2530, May 2023, doi: 10.1038/s41467-023-38242-w.

[14] Z. Zhu, A.E.O. Persson, and L.-E. Wernersson, "Multifunctional Reconfigurable Operations in an Ultra-Scaled Ferroelectric Negative Transconductance Transistor," *ACS Nano*, vol. 18, no. 42, pp. 28977–28985, Oct. 2024, doi: 10.1021/acsnano.4c09598.

[15] M. Haartman and M. Östling, *Low-frequency noise in advanced MOS devices*. Springer Science & Business Media, 2007.

[16] H. Zhu, B. Ye, C. Tang, X. Li, Q. Sun, and D. W. Zhang, "Improving Low-Frequency Noise in 14-nm FinFET by Optimized High-k/Metal Gate Thermal Processing," *IEEE Electron Device Lett.*, vol. 42, no. 8, pp. 1112–1115, Aug. 2021, doi: 10.1109/LED.2021.3091488.

[17] T. Gong, Q. Wu, Y. Huang, H. Jiang, J. Yang, Q. Luo, S. S. Chung, and M. Liu, "First Demonstration of a Bayesian Machine based on Unified Memory and Random Source Achieved by 16-layer Stacking 3D Fe-Diode with High Noise Density and High Area Efficiency," in *2023 International Electron Devices Meeting (IEDM)*, Dec. 2023, pp. 1–4. doi: 10.1109/IEDM45741.2023.10413799.

[18] W. Shin, J. -H. Bae, S. Kim, K. Lee, D. Kwon, B. -G. Park, D. Kwon, and J. -H. Lee, "Effects of High-Pressure Annealing on the Low-Frequency Noise Characteristics in Ferroelectric FET," *IEEE Electron Device Lett.*, vol. 43, no. 1, pp. 13–16, Jan. 2022, doi: 10.1109/LED.2021.3127175.

[19] W. Shin, J.-H. Bae, J. Kim, R.-H. Koo, J.-J. Kim, D. Kwon, and J.-H. Lee, "Variability analysis of ferroelectric FETs in program operation using low-frequency noise spectroscopy," *Appl. Phys. Lett.*, vol. 121, no. 16, p. 163501, Oct. 2022, doi: 10.1063/5.0111309.

[20] H. Yuan, Y. Huang, T. Gong, Y. Wang, P. Jiang, W. Wei, Y. Yang, J. Chai, Z. Wu, X. Wang, and Q. Luo, "Spatial and Energetic Mapping of Traps in FeFET During Endurance Process by Advanced Trap Characterization Platform," *IEEE Electron Device Lett.*, vol. 45, no. 12, pp. 2371–2374, Dec. 2024, doi: 10.1109/LED.2024.3469372.

[21] M. Hellenbrand, E. Memišević, M. Berg, O. -P. Kilpi, J. Svensson, and L. -E. Wernersson, "Low-Frequency Noise in III–V Nanowire TFETs and MOSFETs," *IEEE Electron Device Lett.*, vol. 38, no. 11, pp. 1520–1523, Nov. 2017, doi: 10.1109/LED.2017.2757538.

[22] M. S. Ram, J. Svensson, S. Skog, S. Johannesson, and L. -E. Wernersson, "Low-Frequency Noise in Vertical InAs/InGaAs Gate-All-Around MOSFETs at 15 K for Cryogenic Applications," *IEEE Electron Device Lett.*, vol. 43, no. 12, pp. 2033–2036, Dec. 2022, doi: 10.1109/LED.2022.3216022.

[23] N. Tasneem, Z. Wang, Z. Zhao, N. Upadhyay, S. Lombardo, H. Chen, J. Hur, D. Triyoso, S. Consiglio, K. Tapily, R. Clark, G. Leusink, S. Kurinec, S. Datta, S. Yu, K. Ni, M. Passlack, W. Chern, and A. Khan, "Trap Capture and Emission Dynamics in Ferroelectric Field-Effect Transistors and their Impact on Device Operation and Reliability," in *2021 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2021, p. 6.1.1-6.1.4. doi: 10.1109/IEDM19574.2021.9720615.

[24] W. Wu, H. Wu, W. Sun, M. Si, N. Conrad, Y. Zhao, and P. D. Ye, "Mobility Fluctuation-Induced Low-Frequency Noise in Ultrascaled Ge Nanowire nMOSFETs With Near-Ballistic Transport," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2573–2577, Jun. 2018, doi: 10.1109/TED.2018.2822813.

[25] S. Watanabe, H. Sugawara, R. Häusermann, B. Blülle, A. Yamamura, T. Okamoto, and J. Takeya, "Remarkably low flicker noise in solution-processed organic single crystal transistors," *Commun. Phys.*, vol. 1, no. 1, p. 37, Jul. 2018, doi: 10.1038/s42005-018-0037-0.

[26] O. Phadke, K. A. Aabrar, Y. -c. Luo, S. G. Kirtania, A. I. Khan, S. Datta, and S. Yu, "Low-Frequency Noise Characteristics of Ferroelectric Field-Effect Transistors," in *2023 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2023, pp. 1–4. doi: 10.1109/IRPS48203.2023.10117771.

[27] G. Ghibaudo, O. Roux, Ch. Nguyen-Duc, F. Balestra, and J. Brini, "Improved Analysis of Low Frequency Noise in Field-Effect MOS Transistors," *Phys. Status Solidi A*, vol. 124, no. 2, pp. 571–581, Apr. 1991, doi: 10.1002/pssa.2211240225.

[28] K.-M. Persson, B.G. Malm, and L.-E. Wernersson, "Surface and core contribution to 1/f-noise in InAs nanowire metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 103, no. 3, p. 033508, Jul. 2013, doi: 10.1063/1.4813850.

[29] W. Shin, J. -H. Bae, D. Kwon, R. -H. Koo, B. -G. Park, D. Kwon, and J. -H. Lee, "Investigation of Low-Frequency Noise Characteristics of Ferroelectric Tunnel Junction: From Conduction Mechanism and Scaling Perspectives," *IEEE Electron Device Lett.*, vol. 43, no. 6, pp. 958–961, Jun. 2022, doi: 10.1109/LED.2022.3168797.

[30] N. Gong and T. -P. Ma, "A Study of Endurance Issues in HfO2-Based Ferroelectric Field Effect Transistors: Charge Trapping and Trap Generation," *IEEE Electron Device Lett.*, vol. 39, no. 1, pp. 15–18, Jan. 2018, doi: 10.1109/LED.2017.2776263.

[31] S. Zhao, F. Tian, H. Xu, J. Xiang, T. Li, J. Chai, J. Duan, K. Han, X. Wang, W. Wang, and T. Ye, "Experimental Extraction and Simulation of Charge Trapping During Endurance of FeFET With TiN/HfZrO/SiO2/Si (MFIS) Gate Structure," *IEEE Trans. Electron Devices*, vol. 69, no. 3, pp. 1561–1567, Mar. 2022, doi: 10.1109/TED.2021.3139285.

[32] C. Möhle, C.B. Zota, M. Hellenbrand, and E. Lind, "1/f and RTS noise in InGaAs nanowire MOSFETs," *Spec. Issue Insul. Films Semicond. INFOS 2017*, vol. 178, pp. 52–55, Jun. 2017, doi: 10.1016/j.mee.2017.04.038.

[33] R. K. Kammeugne, C. Theodorou, C. Leroux, X. Mescot, L. Vauche, R. Gwoziecki, S. Becu, M. Charles, E. Bano, and G. Ghibaudo, "Thorough Investigation of Low Frequency Noise Mechanisms in AlGaN/GaN and Al2O3/GaN HEMTs," in *2021 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2021, p. 39.4.1-39.4.4. doi: 10.1109/IEDM19574.2021.9720522.

[34] A. J. Tan, M. Pešić, L. Larcher, Y. -H. Liao, L. -C. Wang, J. -H. Bae, C. Hu, and S. Salahuddin, "Hot Electrons as the Dominant Source of Degradation for Sub-5nm HZO FeFETs," in *2020 IEEE Symposium on VLSI Technology*, Jun. 2020, pp. 1–2. doi: 10.1109/VLSITechnology18217.2020.9265067.

[35] S. Dutta, H. Ye, W. Chakraborty, Y. . -C. Luo, M. S. Jose, B. Grisafe, A. Khanna, I. Lightcap, S. Shinde, S. Yu, and S. Datta, "Monolithic 3D Integration of High Endurance Multi-Bit Ferroelectric FET for Accelerating Compute-In-Memory," in *2020 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2020, p. 36.4.1-36.4.4. doi: 10.1109/IEDM13553.2020.9371974.

[36] C. -Y. Liao, K. -Y. Hsiang, Z. -F. Lou, H. -C. Tseng, C. -Y. Lin, Z. . -X. Li, F. . -C. Hsieh, C. . -C. Wang, F. . -S. Chang, W. . -C. Ray, Y. . -Y. Tseng, S. T. Chang, T. . -C. Chen, and M. H. Lee, "Endurance > 1011 Cycling of 3D GAA Nanosheet Ferroelectric FET with Stacked HfZrO2 to Homogenize Corner Field Toward Mitigate Dead Zone for High-Density eNVM," in *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Jun. 2022, pp. 1–2. doi: 10.1109/VLSITechnologyandCir46769.2022.9830345.