# Vertical III-V nanowire tunnel field-effect transistors

## a circuit perspective

Rangasamy, Gautham

2023

*Document Version:*
Publisher's PDF, also known as Version of record

# Vertical III-V Nanowire Tunnel Field-Effect Transistors: A Circuit Perspective

Doctoral Thesis

*Gautham Rangasamy*

Department of Electrical and
Information Technology
Lund, December 2023

Academic thesis for the degree of Doctor of Philosophy, which, by due permission of the Faculty of Engineering at Lund University, will be publicly defended on Friday, $15^{th}$ December 2023, at 9:15 a.m. in lecture hall E:B, Department of Electrical and Information Technology, Ole Römers Väg 3, 223 63 Lund, Sweden. The thesis will be defended in English.

The Faculty Opponent will be Francis Balestra, Director of Research CNRS, Paris, France.

*Organisation:*
LUND UNIVERSITY
Department of Electrical and Information Technology
Ole Römers Väg 3
223 63 Lund
Sweden

*Document Type:*
DOCTORAL THESIS

*Date of Issue:*
December 2023

*Sponsoring Organisation(s):*
Swedish Foundation for Strategic Research (SSF)
Swedish Research Council (VR)
European Union (EU)

*Author:*
Gautham Rangasamy

*Title:*
Vertical III-V Nanowire Tunnel Field-Effect Transistors: A Circuit Perspective

*Abstract:*
The energy scaling of integrated circuits has reached a limit because the operating voltage of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFET) based switches has reached its minimum value. MOSFETs are limited by thermionic emission and cannot achieve a subthreshold swing (SS) below 60 mV/decade at room temperature. Tunnel Field-Effect Transistors (TFET), which operate on field modulation of band-to-band tunneling (BTBT), can deliver SS less than 60 mV/dec and are considered as a potential alternative for MOSFETs to further scale down the supply voltage.
This thesis work studied the capabilities and limitations of n-type TFETs based on III-V vertical nanowires and their circuit implementation. TFETs were fabricated using vertical InAs/GaSb or InAs/InGaAsSb/GaSb nanowires of high material quality, switching from InAs/GaSb to InAs/InGaAsSb/GaSb allowed for optimization of the heterojunction, resulted in improvement of device metrics. Along with heterostructure optimization, the dopant introduction and concentration were systematically varied to achieve devices with record performance. These devices achieved a minimum subthreshold swing of 42 mV/decade and a record high $I_{60}$ of 1.2 $\mu$A/$\mu$m at a drive voltage of 0.5 V. The stability and high yield of the process allowed for statistical study of correlations between important device parameters such as $I_{60}$, on-current, subthreshold swing, and off-current. The implementation of circuits was also aided by sufficient process repeatability and yield.
To implement circuits based on these TFETs, the fabrication process was optimized with introduction of vias and non-organic spacers. Voltage based circuits in the following configurations were implemented: a current mirror, a diode-connected inverter and a cascode buffer. Individual TFETs in the circuit operate well below 60 mV/dec operation with minimum achieved subthreshold swing (SS) of 30 mV/dec at drain voltage of 400 mV. In circuit operation, individual devices were connected via FEOL and are biased at 300 mV supply voltage, with an input frequency of 200 kHz. To explore current-mode based design principle, we have implemented a current conveyor circuit, which exhibits large-signal voltage gain of 0.89 mV/mV, a current gain of 1 nA/nA and an operating frequency of 320 kHz.
Additionally, self-heating in a vertical nanowire device was examined using pulsed IV methodology. The results indicate that the intrinsic temperature rises to 385 K when the device is operated in DC at room temperature (300 K) with a thermal time constant of 1 $\mu$s. We find that self-heating is a limiting factor for device performance.

*Keywords:*
Low-Power Electronics, Self-Heating, Steep Slope Devices, Tunnel Field-Effect Transistors, Vertical Nanowire, III-V Semiconductors.

*Classification System and/or Index Terms*
Electronic Engineering, Nanotechnology

*Language:*
English

*Supplementary Bibliographical Information:*
–

*ISBN (printed):*
978-91-8039-887-9

*Key title and ISSN:*
Series of Licentiate and Doctoral Theses; ISSN 1654-790X 166

*ISBN (digital):*
978-91-8039-886-2

*Recipient's Notes:*

*Number of Pages:*
???

*Price:*

*Security Classification:*
Unclassified



*Signature:* *Gautham Rangasamy* *Date:* 15 December 2023

# Vertical III-V Nanowire Tunnel Field-Effect Transistors: A Circuit Perspective

Doctoral Thesis

*Gautham Rangasamy*


LUND
UNIVERSITY

Department of Electrical and
Information Technology

Lund, December 2023

Gautham Rangasamy
Department of Electrical and Information Technology
Lund University
Ole Römers Väg 3, 223 63 Lund, Sweden

Series of Licentiate and Doctoral Theses
ISSN 1654-790X 166
ISBN 978-91-8039-887-9 (printed)
ISBN 978-91-8039-886-2 (digital)


This thesis is typeset using LaTeX $2_\varepsilon$ with the body text in Palatino and Goudy Initials, headings in Helvetica, text in figures in Arial, and the body text in Appendix A in Computer Modern.

Frontispiece: Array of nanowires

Printed by Tryckeriet i E-huset, Lund University, Lund, Sweden.

*To Yalini*

*"It's true that everything we wish for will not come to be, but things that we must do must always begin with a wish"*

- Kishimoto

# Abstract

The energy scaling of integrated circuits has reached a limit because the operating voltage of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFET) based switches has reached its minimum value. MOSFETs are limited by thermionic emission and cannot achieve a subthreshold swing (SS) below 60 mV/decade at room temperature. Tunnel Field-Effect Transistors (TFET), which operate on field modulation of band-to-band tunneling (BTBT), can deliver SS less than 60 mV/dec and are considered as a potential alternative for MOSFETs to further scale down the supply voltage.

This thesis work studied the capabilities and limitations of n-type TFETs based on III-V vertical nanowires and their circuit implementation. TFETs were fabricated using vertical InAs/GaSb or InAs/InGaAsSb/GaSb nanowires of high material quality, switching from InAs/GaSb to InAs/InGaAsSb/GaSb allowed for optimization of the heterojunction, resulted in improvement of device metrics. Along with heterostructure optimization, the dopant introduction and concentration were systematically varied to achieve devices with record performance. These devices achieved a minimum subthreshold swing of 42 mV/decade and a record high $I_{60}$ of 1.2 $\mu$A/$\mu$m at a drive voltage of 0.5 V. The stability and high yield of the process allowed for statistical study of correlations between important device parameters such as $I_{60}$, on-current, subthreshold swing, and off-current. The implementation of circuits was also aided by sufficient process repeatability and yield.

To implement circuits based on these TFETs, the fabrication process was optimized with introduction of vias and non-organic spacers. Voltage based circuits in the following configurations were implemented: a current mirror,

a diode-connected inverter and a cascode buffer. Individual TFETs in the circuit operate well below 60 mV/dec operation with minimum achieved subthreshold swing (SS) of 30 mV/dec at drain voltage of 400 mV. In circuit operation, individual devices were connected via FEOL and are biased at 300 mV supply voltage, with an input frequency of 200 kHz. To explore current-mode based design principle, we have implemented a current conveyor circuit, which exhibits large-signal voltage gain of 0.89 mV/mV, a current gain of 1 nA/nA and an operating frequency of 320 kHz.

Additionally, self-heating in a vertical nanowire device was examined using pulsed IV methodology. The results indicate that the intrinsic temperature rises to 385 K when the device is operated in DC at room temperature (300 K) with a thermal time constant of 1 $\mu$s. We find that self-heating is a limiting factor for device performance.

# Popular Science Summary

The unimaginable proliferation of electronics in our daily life, be it computing, healthcare, communication, transport, or leisure has fundamentally changed our way of living. The convenience and improvement in quality of our daily life is enabled by terabytes in data storage, data processing, data communication enabled by trillions of transistors, guzzling terawatts of power. With the emergence of new fields in AI, Neuromorphic Computing, Quantum Computing, Internet of Things, to name a few, we can be rest assured of further increase in electronic systems in our daily life. It puts us in an fascinating time, quasi -science fiction even, as we speculate on the enormous potential the field will bring. The caveat, of course, is the enormous increase in data produced and the accompanying energy consumption.

As all the electronics system are made with transistors, designing more energy efficient transistors could be one way of mitigating the increasing energy consumption. Transistor, in essence, is an electronic switch, which controls the flow of charges between two charge reservoirs, source and drain. The gate, the controlling terminal, determines the amount of current flow between the terminals. This concept can be implemented by exploiting a variety of physical phenomena, material systems, and device architectures. Over the past decades, Si based Metal-Oxide-Semiconductor Field-Effect Transistors working on principles of thermionic emissions were favored. This emerged in part due to their ability to maintain their functionality when their physical dimensions and supply voltages were scaled down, leading to lower power consumption. Below 10 nm, miniaturization of transistors hit a roadblock due

to the degradation of the transistor to switch between the on- and off-states due to quantum effects.

With this view in mind, a simple proposition can be made. Instead of suppressing these quantum effects at low dimensions, we could exploit them to solve our power consumption issues. Tunnel FET is one such device where we use our adversity to our advantage and utilize quantum mechanical tunneling to make low power switches. This proposition forms the basis of the thesis work. We explore the feasibility of TFETs in low-power domain and how they would perform compared to conventional transistors. Building on the knowledge that III-V materials offer better performance and vertical structure improves packing density, vertical III-V TFETs were employed. These TFETs achieved in the thesis work are state-of-the-art, lowering the energy consumption with respect to MOSFETs. We pushed on study their circuit performance in voltage and current modes of operation, across military temperature range, from $-55\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$. We found TFETs were able to maintain the same functionality as MOSFETs at lower power consumption. This feels like an important step for TFETs to go from being a promising candidate to a credible compliment for MOSFETs in energy efficeint systems.

# Acknowledgments

It is hard not to compare my PhD journey with that of Test cricket. The principles remain the same for both. Take the failures, don't blame the circumstance and keep ploughing away as conditions will change favourable. The biggest similarity though is both of them are a team sport. I would like to begin by thanking my captain/ supervisor Lars-Erik. I appreicate your guidance and support throughout this journey. Yoru leadership skills are par none and hoepfully I imbibed some of it.

I would like to thank Lars Ohlsson Fhager, my co-supervisor, for the abundant time we spent discussing ideas, some great, some good and rest forgotten. Of your many admirable qualities, your approach of explaining complex ideas and attention to detail are the ones I admired the most. I would also like to thank my other co-supervisor Johannes Svensson. I am grateful for his help in structuring my thesis and innumerable advice in both the technical and personal front. Thank you Erik, for all the conversations we had over the years. It was delightful.

Of course, the journey is not worth taking without your fellow mates. I would like to thank Zhongyunshen Zhu for the infinite discussions we had about TFET, processing, career and life. Abinaya Krishnaraja for introducing me to fabrication process. Heera Menon, for the friendship, patience and lots of dinners. You are the best cook ever. Navya and Anton, for all the time we spent in the badminton court and the conversations.

I would also like to extend my gratitude to all the remarkable colleagues within the division who made the work environment not only vibrant but also relaxing with full of fun. So a great thanks goes to you, Marcus, Saketh, Phillipp, André, Hannes, Karthik, Ben, Ngoc Duc, Heera, Lars, Mattias, Anette, Navya, Patrik, Louise, Lasse, Markus, Fredrik, Karl-Magnus,

Stefan, Sebastian, Olli-Pekka, Paula, Niklas, Daniel, Mats, Johan, Andrea, and Alexandros.

Furthermore, I want to thank all the engineers and technicians in both NanoLund and EIT lab. My thesis wouldn't be possible to be completed without your tremendous help.

A shout out to my boys for all the adventures and a fond memories. Sekase, Chetase, Bangase, Thagapps, Wasim, Shaafi, Kamalesh, Krishnamoorthy, Anand, Satish, Vishal, Balaji G, Sanjay, Stephen, Gurunathar, Balaji R, Sandeep, Vivek, Yasser, Murali, Mohan, Prasanna, Nishant and Kamal. Thank you to Ferdinand, for introducing me to the wonderful sport of kickboxing and all the long conversations and mentorship.

Finally, I would like to thank my family for your unconditional love and forever support in my entire life.

*Gautham Rangasamy*
Lund, December 2023

# Contents

# Preface

This thesis is a summary of five-year work in *Nanoelectronics Group* (belonging to *Division of Electromagnetics & Nanoelectronics* since 2022) at Department of Electrical and Information Technology, Lund University. This work presents systematic investigation of III-V based vertical nanowire tunnel field-effect transistors, their circuit implementation and their self-heating investigation for low-power systems. The work was supervised by Professor *Lars-Erik Wernersson*, Dr. *Lars Ohlsson Fhager* and Dr. *Johannes Svensson*.

## STRUCTURE OF THE THESIS

- **INTRODUCTION**
  The Introduction provides a broad and comprehensive view of the included publications and combines related work together. The Introduction is intended to be comprehensible for aspiring readers with a Master's degree in physics, electrical engineering or a related subject.

- **APPENDICES**

  **A Fabrication Steps of Vertical Nanowire Tunnel Field-Effect Transistors**
  Appendix A provides detailed steps of vertical device fabrication included in this thesis.

- **PAPERS**
  The papers forming the main body of the thesis are reproduced in the back and listed in the following.

## INCLUDED PAPERS

The following papers form the main body of this thesis and are appended in the back of the thesis.

**Paper I:** G. Rangasamy, Z. Zhu, and L.-E. Wernersson, "High Current Density Vertical Nanowire TFETs with $I_{60}$> 1 $\mu$A/$\mu$m", *IEEE Access*, vol. 11, pp. 95692–95696, 2023, doi: 0.1109/ACCESS.2023.3310253.

► *I developed the process scheme, fabricated the device, did the characterization, and wrote the paper.*

**Paper II:** G. Rangasamy, Z. Zhu, and L.-E. Wernersson, "Impact of Source Positioning and Doping on Performance of Vertical III-V Nanowire Tunneling Field Effect Transistors", *IEEE Transactions on Electron Devices*, (Manuscript)

► *I developed the process scheme, fabricated the device, did the characterization, and wrote the paper.*

**Paper III:** G. Rangasamy, Z. Zhu, L.O. Fhager, and L.-E. Wernersson, "$g_m/I_d$ Analysis of vertical nanowire III–V TFETs", *Electronics Letters*, vol. 59, no. 18, pp.e12954, Jul. 2023, doi: 10.1049/ell2.12954.

► *I developed the process scheme, fabricated the device along with the circuits, did the characterization and circuit analysis and wrote the paper.*

**Paper IV:** G. Rangasamy, Z. Zhu, L.O. Fhager, and L.-E. Wernersson, "TFET Circuit Configurations Operating below 60 mV/dec", *IEEE Transactions on Nanotechnology*, (Under Review)

► *I developed the process scheme, fabricated the device along with the circuits, did the characterization and circuit analysis and wrote the paper.*

**Paper V:** G. Rangasamy, M.S. Ram, L.O. Fhager, and L.-E. Wernersson, "Self-Heating in Gate-All-Around Vertical III-V InAs/InGaAs MOSFETs", *IEEE Electron Device Letters*, vol. 44, no. 7, pp. 1212–1215, Jul. 2023, doi: 10.1109/LED.2023.3273785.

► *I developed the measurement scheme, did the characterization, self-heating analysis and wrote the paper.*

# Acronyms and Symbols

Here, important acronyms, abbreviations, and symbols are listed, which are recurring throughout the thesis. Some parameters, which only occur in a narrow context, are intentionally omitted; some parameters are used in more than one way, but the context is always explicitly clarified in the corresponding text. Some (compound) units are provided with prefixes to reflect the most commonly encountered notations in the literature.

## ACRONYMS AND ABBREVIATIONS

| | |
|---|---|
| **3D** | Three Dimensional |
| **$Al_2O_3$** | Aluminium Oxide |
| **ALD** | Atomic Layer Deposition |
| **Ar** | Argon |
| **As** | Arsenic |
| **$AsH_3$** | Arsine |
| **Au** | Gold |
| **BEOL** | Back-End-of-Line |
| **BOE** | Buffered Oxide Etchant |
| **BTBT** | Band-to-Band Tunneling |
| **$C_4F_8$** | Octafluorocyclobutane |
| **$CH_3COOH$** | Acetic acid |
| **CMOS** | Complementary Metal-Oxide-Semiconductor |
| **DC** | Direct Current |

| | |
|---|---|
| **DE** | Digital Etch |
| **DEZn** | Diethylzinc |
| **DI** | Deionized |
| **DIBL** | Drain Induced Barrier Lowering |
| **DOS** | Density Of States |
| **EBL** | Electron-Beam Lithography |
| **EOT** | Equivalent Oxide Thickness |
| **FEOL** | Front-End-of-Line |
| **FET** | Field-Effect Transistor |
| **Ga** | Gallium |
| **GAA** | Gate-All-Around |
| **GaAs** | Gallium Arsenide |
| **GaSb** | Gallium Antimonide |
| **Ge** | Germanium |
| **H** | Hydrogen |
| **$H_2O$** | Water |
| **$H_2SO_4$** | Sulphuric acid |
| **$H_3PO_4$** | Phosphoric acid |
| **HCl** | Hydrochloric acid |
| **Hf** | Hafnium |
| **$HfO_2$ Hafnium dioxide** | Nitric acid |
| **IC** | Integrated circuit |
| **ICP** | Inductively Coupled Plasma |
| **In** | Indium |
| **InAs** | Indium Arsenide |
| **InGaAs** | Indium Gallium Arsenide |
| **InGaAsSb** | Indium Gallium Arsenide Antimonide |
| **InP** | Indium Phosphide |
| **IoT** | Internet-of-Things |
| **IPA** | Isopropyl Alcohol |
| **Mo** | Molybdenum |
| **$MoS_2$** | Molybdenum disulphide |
| **MOSFET** | Metal-Oxide-Semiconductor Field-Effect Transistor |
| **MOVPE** | Metal-Organic Vapor-Phase Epitaxy |
| **$N_2$** | Nitrogen |

| | |
|---|---|
| **NaOH** | Sodium hydroxide |
| **NDR** | Negative Differential Resistance |
| **Ni** | Nickel |
| **$O_2$** | Oxygen |
| **$O_3$** | Ozone |
| **PVCR** | Peak-to-Valley Current Ratio |
| **RIE** | Reactive-Ion Etch |
| **SEM** | Scanning Electron Microscopy |
| **$SF_6$** | Sulfur hexafluoride |
| **SiGe** | Silicon Germanium |
| **SiO** | Silicon monoxide |
| **$SiO_2$** | Silicon dioxide |
| **Sn** | Tin |
| **SS** | Subthreshold Swing |
| **TASE** | Template Assisted Selective Epitaxy |
| **TAT** | Trap Assisted Tunneling |
| **TDMAHf** | Tetrakis(dimethylamido)hafnium(IV) |
| **TEM** | Transmission Electron Microscopy |
| **TESn** | Tetraethyltin |
| **TFET** | Tunnel Field-Effect Transistor |
| **Ti** | Titanium |
| **TiN** | Titanium Nitride |
| **TMAH** | Tetramethylammonium hydroxide |
| **TMAl** | Trimethylaluminum |
| **TMD** | Transition metal dichalcogenides |
| **TMGa** | Trimethylgallium |
| **TMIn** | Trimethylindium |
| **TMSb** | Trimethylantimony |
| **ULP** | Ultra Low Power |
| **UV** | Ultraviolet |
| **VLS** | Vapor Liquid Solid |
| **W** | Tungsten |
| **WKB** | Wentzel-Kramers-Brillouin |
| **WZ** | Wurtzite |

| | |
|---|---|
| **XEDS** | Energy-dispersive X-ray spectroscopy |
| **XPS** | X-ray Photoelectron Spectroscopy |
| **XRD** | X-Ray Diffraction |
| **ZB** | Zincblende |
| **Zn** | Zinc |

## LATIN SYMBOLS

| | | |
|---|---|---|
| $C_{ins}$ | F | Insulator Capacitance |
| $C_s$ | F | Semiconductor Capacitance |
| $E_F$ | eV | Fermi Level Energy |
| $E_g$ | eV | Band Gap |
| $E_{c,c}$ | eV | Channel Conduction Band Energy |
| $E_{v,s}$ | eV | Channel Valence Band Energy |
| $E_{F,s}$ | eV | Source Fermi Level Energy |
| $f$ | Hz | Frequency |
| $g_d$ | S, $\mu S\,\mu m^{-1}$ | Output Conductance, often normalised by gate width |
| $g_m$ | S, $\mu S\,\mu m^{-1}$ | Transconductance, often normalised by gate width |
| $I_D$ | A, $\mu A\,\mu m^{-1}$ | Drain Current, often normalised by the gate width |
| $I_{DS}$ | A, $\mu A\,\mu m^{-1}$ | Source-to-Drain Current, often normalised by the gate width |
| $I_G$ | A, $\mu A\,\mu m^{-1}$ | Gate Current, often normalised by the gate width |
| $I_S$ | A, $\mu A\,\mu m^{-1}$ | Source Current, often normalised by the gate width |
| $I_{OFF}$ | A, $\mu A\,\mu m^{-1}$ | Off-current, often normalised by the gate width |
| $I_{ON}$ | A, $\mu A\,\mu m^{-1}$ | On-current, often normalised by the gate width |

| | | |
|---|---|---|
| $k_B$ | | $\approx 1.381 \times 10^{-23}$ kg m$^2$ K$^{-1}$ s$^{-1}$, Boltzmann Constant |
| $L_G$ | m | Gate Length |
| $m_0$ | | $\approx 9.109 \times 10^{-31}$ kg, Electron Rest Mass |
| $m^*$ | $m_0$ | Effective Mass |
| $q$ | | $\approx 1.602 \times 10^{-19}$ C, Elemental Charge |
| $R_{on}$ | $\Omega$ | Drain-to-Source Voltage |
| $T$ | K | Temperature |
| $V_{DS}$ | V | Drain-to-Source Voltage |
| $V_{GD}$ | V | Gate-to-Drain Voltage |
| $V_{GS}$ | V | Gate-to-Source Voltage |
| $V_T$ | V | Threshold Voltage |
| $V_{Th}$ | V | Thermal Voltage |

## GREEK SYMBOLS

| | | |
|---|---|---|
| $\alpha$ | eV$^{-1}$ | Non-Parabolicity Factor |
| $\varepsilon$ | eV$^{-1}$ | Electric field |
| $\kappa$ | | Dennard Scaling Factor, Relative Permittivity |

## FUNCTIONS AND OPERATORS

| | |
|---|---|
| $\ln(\cdot)$ | Natural logarithm |
| $\log(\cdot)$ | Logarithm to the base 10 |
| $\sin(\cdot)$ | sine |

# INTRODUCTION

# 1

# Introduction

Electronics applications permeate our lives and most human societies in countless ways. From smartphones to computers, from networks to databases, from AI to quantum computing, these inventions and their constant enhancements have enabled many possibilities. Transistors are the essential component of electronics, and their impact is so immense that they are the most widely manufactured human product ever. The transistor, a three-terminal device, which controls the flow of electrons between two electron reservoirs have been implemented in myriad of ways exploiting different physical phenomena and plethora of material systems. In this chapter, we provide look into one such transistor which works on quantum mechanical tunneling, the Tunnel Field-Effect Transistors (TFET). We discuss its operation, figures of merit, and provide a context and motivation for investigations taken in this thesis work.

## 1.1 MOTIVATION FOR CONDUCTED RESEARCH

A transistor operates as a current regulator over several decades of magnitude by controlling a voltage between the terminals. This functionality has led to design and implementation of various kinds of transistors, which form the essential building block in most electronic systems. A daily example is the billions of transistors that make up every single processor in our computers, laptops, and smartphones. Transistors are also used in audio and wireless communication amplifiers, in power supply controllers or as sensors.
The rapid development of the metal-oxide-semiconductor field-effect transistor (MOSFET) since its invention in the 1950s has been driven mainly

by the continuous miniaturisation of the device dimensions and by the occasional introduction of a new material or a change in the device geometry. Feature sizes have now decreased to the thickness of only a few atomic layers, thereby, geometric scaling is facing fundamental physical limits. Since about the beginning of the 21st century, for further improvement of the device performance in terms of energy efficiency and speed, new materials, new architectures, have been the the focus of research efforts [1,2].

One of the challenges for future transistor design is the so-called "Boltzmann tyranny" that limits the scaling of the supply voltage as CMOS technology approaches its thermal and reliability limits [3]. The MOSFET works by using the gate electrode to change the potential barrier between the source and the channel, which controls the injection of charge carriers into the channel. However, the carriers follow Boltzmann statistics and there is a small fraction of high-energy carriers that can cross the barrier. This fraction increases with temperature T and makes the MOSFET operate at the thermionic limit of kT/q (where k is Boltzmann's constant and q is the charge of an electron). The gate voltage needs to change by at least 60 mV at room temperature to cause a tenfold change in source-to-drain current , and this sets a lower bound on the minimum threshold voltage of about 200 mV to keep the off-state leakage current low. The need for a minimum gate overdrive voltage of about 300 mV above the threshold voltage to provide enough on-state current sets the minimum operating voltage of the MOSFET at 500 mV. The inability to scale supply voltage below 500 mV will prevent CMOS technology from reaching low switching energies and sets a practical limit for hyperscaling. To overcome this, we need radical changes in the fundamental switching mechanisms of MOSFETs.

TFET devices are one approach to achieve subthermal switching while operating at low supply voltages. A TFET uses a reverse biased p-i-n interband tunnel junction instead of a conventional n-MOSFET, which is made of n-type sources and p-type channels. The subthreshold slope in such a device is not limited to 60 mV per decade. Here, the thermal tail of the electrons in the valence band of the p+ source is abruptly truncated by the band edge of the channel and can lead to steeper switching characteristics as the TFET is turned on. Operation of TFETs will be elaborated later in the chapter.

This thesis summarises detailed fabrication and characterisation work on III-V nanowire TFETs, in vertical device architectures, which employ both new materials with respect to the industry standard Si, and a new device architecture with respect to the conventional lateral device orientation, all while being compatible with existing Si fabrication technology. For TFETs to be competitive in low power domian, it's current levels has to be substantially improved.

The first part of the thesis discusses the heterostrucuture engineering adopted to improve the device characteristics. A TFET can, in principle, operate with larger transconductance to current ratio than traditional field effect transistors in the sub-threshold region. In addition, the higher output resistance offered by TFET-based designs allows achieving significantly higher intrinsic voltage gain and higher maximum-oscillation frequency at low current levels. Moreover, TFET-based circuits exhibit superior performance advantages in track-and-hold circuits, ambient radio-frequency power scavenging and digital to analog converters [4–8]. All these findings indicate that the TFET based circuits has a good application prospect in the low-power domain. Despite these advantages, circuit design based on TFETs haven't been experimentally verified. This thesis work try to tackle this deficiency in research landscape as well. By adopting a vertical architecture, the gate length is decoupled from the footing area, which greatly improves the packing density. The improvement in packing density, affects the heat transport in the chip. The final section of the thesis studies the self-heating behaviour of vertical nanowires.

## 1.2 TFET OPERATION

Before exploring the operation of TFETs, a brief introduction on MOSFET operation is warranted, so that we can compare and contrast their operating behaviour. Both transistors transport charges between the source and the drain terminals, with gate terminal modulating the amount of charge transfer albeit with a different operating principle. For easier analysis, we are going to consider only n-type for both devices. The schematic cross section and band diagram of both devices are shown in Fig. 1.1. Let's take the operating principle of MOSFETs. The doped n-type source and the drain terminals are reservoirs of charges. The p- type channel constitutes an energy barrier between these terminals. By applying a gate voltage, an electric field is created in the channel which modulates this energy barrier. As gate voltage increases, the barrier energy decreases, and electrons can surmount the lowered energy barrier and move from source to drain. To improve current levels, the drain-source voltage can be increased.

TFET, on the other hand, rely on band-to-band tunneling (BTBT) to transfer the charges between the terminals [9–11]. This is enabled by the device structure of the TFET, which consists of lightly doped p-type source, an intrinsic channel and a highly doped n-type drain, not unlike an p-i-n diode. Structurally, the TFET has asymmetric doping of the drain and source when compared to a conventional MOSFET. The corresponding band diagrams of an nTFET transitioning from the off- to the on-state are shown in Fig. 1.2b

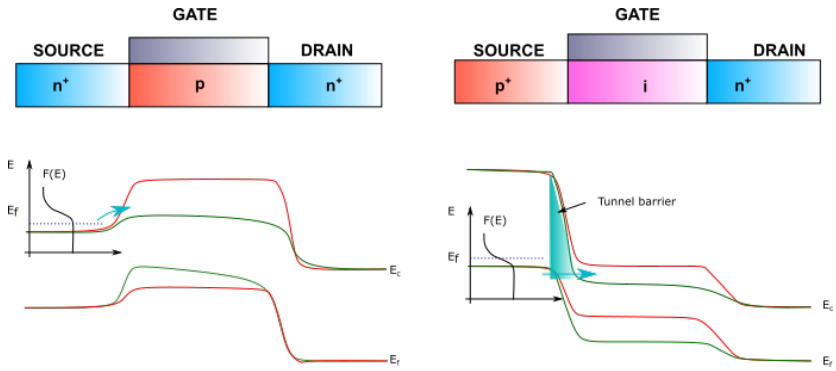


**Figure 1.1:** The cross section and the band diagram at on- and off-state for a) a MOSFET and b) a TFET are shown.

under positive $V_{DS}$ bias. As in a backward diode, the interband overlap of the source and channel regions enables the conduction of carriers by means of band-to-band tunneling. However, in the off-state, the band gap in the channel acts as an energy filter, cutting off the availability of states for tunneling. As a consequence, $I_{OFF}$ in a TFET results ideally only from thermionic emission above a barrier approximately equal to the energy band gap, $E_G$. Other processes that contribute to the OFF-state leakage currents are associated with Shockley-Read-Hall (SRH) generation and trap-assisted tunneling (TAT). Referring again to Fig. 1.2b, if a positive gate voltage is applied, the bands in the channel move to lower energies reaching a crossing point where the conduction band in the channel begins to overlap with the valence band in the source. This corresponds to the onset of BTBT where electrons tunnel from the source valence band into the channel through a tunneling barrier. The tunneling probability is exponentially dependent on the tunneling distance. The BTBT generation processes can result either from direct transition between the maximum of the valence band and the minimum of the conduction band at the tunneling window or via a phonon-meditated indirect transition [6].

The gate voltage modulates both the tunneling probability and the availability of states to tunnel into, within a tunneling window given by the interband overlap. These two contributions allow for two different mechanisms for realizing SS steeper than 60 mV/dec. Unlike the MOSFET where the slope of the $I_D$–$V_{GS}$ transfer characteristic has a fixed swing in the subthreshold regime, the SS of a TFET is not constant but depends on $V_{GS}$. The key current defining the upper bound of this region is defined as sub-threshold current at SS = 60 mV/dec and is denoted by $I_{60}$. SS and $I_{60}$ metrics form the basis of benchmarking TFETs in this work.

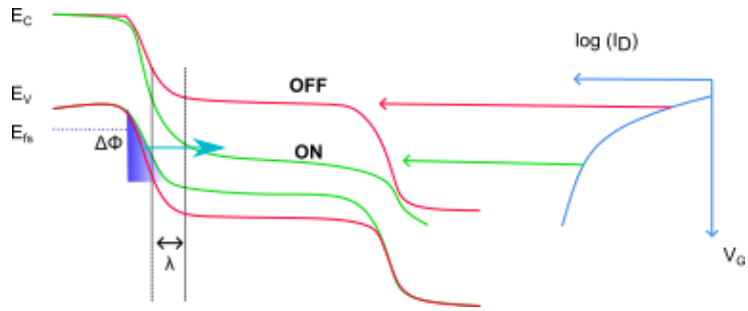


**Figure 1.2:** a) Energy band diagrams for off- and on-state for a TFET. Each band diagram variation corresponds to a specific point in the $I_D$–$V_{GS}$ characteristic indicated in b) the right panel.

### 1.2.1 BAND-TO-BAND TUNNELING

In this section, a simple analytical theory is derived to lay out some general TFET design rules and to illustrate under what circumstances subthermal SS can be achieved. As illustrated in Fig. 1.2a, only carriers within the tunneling window can contribute to the transport. Using Landauer formalism [12], the drain current per unit width can be written as

$$I_{\mathrm{D}} = \frac{2q}{h} \int_{E_{\mathrm{C,CH}}}^{E_{\mathrm{V,S}}} T_{\mathrm{BTBT}}(E) \left[ f_{\mathrm{S}}(E) - f_{\mathrm{D}}(E) \right] \mathrm{d}E, \tag{1.1}$$

where h is Planck's constant, $f_S$(E) and $f_D$(E) are the source and drain Fermi distribution functions, and $T_{BTBT}$(E) is the BTBT tunneling probability. The direct BTBT probability can be evaluated analytically by means of the Wentzel-Kramers- Brillouin (WKB) approximation,

$$T_{\mathrm{BTBT}} = \exp\left( -2 \int_{x_1}^{x_2} k_{\mathrm{X}}(x, E)\, \mathrm{d}x \right), \tag{1.2}$$

where $x_1$ and $x_2$ are the classical turning points defining the tunneling path length and $k_X$ is the imaginary wave vector obtained through the Kane two-band model [13]. Assuming a triangular potential barrier at the source/channel interface, i.e., constant electric field over the tunneling path, the transmission probability can be written as

$$T_{\mathrm{BTBT}} = \exp\left( -\frac{4\Lambda\sqrt{2m^*}E_{\mathrm{G}}^{3/2}}{3q\hbar\left(\Delta\phi + E_{\mathrm{G}}\right)} \right). \tag{1.3}$$

In the above equation, $\Lambda$ is the width of the transition region at the source/channel interface, i.e., the tunneling width, $m^*$ is the reduced tun-

neling mass, h is the reduced Planck's constant, and $E_G$ is the semiconductor energy gap. The tunneling width is given by the sum of the depletion width in the source, $W_D$, and the scaling length of the gated region, $\lambda$, i.e., $\Lambda = W_D + \lambda$ [14]. It is useful to relate the source depletion width and channel scaling lengths to the device parameters; we can approximate $W_D$ with the Debye length in the source region

$$W_{\mathrm{D}} = \sqrt{\frac{\varepsilon_{\mathrm{S}} k_{\mathrm{B}} T}{q^2 N_{\mathrm{D}}}},$$

where $\epsilon_s$ is the semiconductor permittivity and $N_D$ is the doping in the source. The expression for the channel scaling length depends on the channel geometry. In the case of a vertical gate-all-around (GAA) nanowire structure assuming a non- parabolic expansion of the vertical potential distribution, and assuming a very thin nanowire channel, the natural length is given by

$$\lambda \approx \pi \frac{t_{ox} + r_{nw}}{2.4},$$

where $r_{nw}$ is the nanowire radius and $t_{ox}$ is the oxide thickness [15].

The BTBT current is determined by both the transmission probability and the occupation functions at the two sides of the tunnel junction within the tunneling window. If we assume a drain-source bias large enough to suppress any back injection from the drain to the source [16],

$$\begin{aligned} I_{\mathrm{D}} &\approx \frac{2q}{h} T_{\mathrm{BTBT}} k_{\mathrm{B}} T \left[ F_0 \left( \frac{E_{\mathrm{FS}} - E_{\mathrm{C,CH}}}{k_{\mathrm{B}} T} \right) - F_0 \left( \frac{E_{\mathrm{FS}} - E_{\mathrm{V,S}}}{k_{\mathrm{B}} T} \right) \right] \\ I_D &= \frac{2q}{h} T_{\mathrm{BTBT}} k_{\mathrm{B}} T \ln \left[ \frac{1 + \exp\left( \frac{E_{\mathrm{FS}} - E_{\mathrm{V,S}} + \Delta\phi}{k_{\mathrm{B}} T} \right)}{1 + \exp\left( \frac{E_{\mathrm{FS}} - E_{\mathrm{V,S}}}{k_{\mathrm{B}} T} \right)} \right] \end{aligned} \tag{1.4}$$

In the off-state, leakage contributions dominate TFET current. Eq. 1.3 indicates that narrow band gap materials are necessary to achieve BTBT transmission probability close to unity. When a narrow band gap material is employed, $I_{ON}$ increases according to Eq. 1.2.1, but the thermionic current, $I_{TH}$, becomes significant as well.

$$
\begin{aligned}
I_{\mathrm{TH}} &= \frac{2q}{h}\int_{E_{\mathrm{C,S}}}^{+\infty} f_{\mathrm{S}}(E)\mathrm{d}E \\
&\approx \frac{2q}{h}k_{\mathrm{B}}T\exp\left(-\frac{E_{\mathrm{G}}+E_{\mathrm{V,S}}-E_{\mathrm{F,S}}}{k_{\mathrm{B}}T}\right)
\end{aligned}
\tag{1.5}
$$

A TFET has two tunneling junctions, one at the source-channel interface and the other at the drain-channel interface. When an negative gate voltage is applied, the valence band of channel and conduction band at the drain opens up, leading to hole injection into the channel. This ambipolar behaviour is undesirable as it increases the off-state conduction, leading to higher power dissipation. In this work, the ambipolar behaviour is suppressed by reducing the drain doping at the expense of the channel resistance. A weaker gate control on the drain-side by introduction of field-plate is adopted as well [17, 18]. The fabrication techniques used are discussed further in Chapter 2 while the effects of ambipolarity in circuit operation are discussed in Chapter 3.

For 1D TFETs, direct source-drain tunneling dominates the off-state leakage, especially for low $E_G$ and small m* materials. Trap-assisted tunneling is another important parasitic conduction mechanism often called into play to explain the deviations observed between simulated and measured TFET characteristics. A comprehensive study on affects of these leakages in TFET performance is shown in previous studies conducted in our group [19].

### 1.2.2 NEGATIVE DIFFERENTIAL REGION

A common feature of TFETs is the negative differential resistance (NDR) that occurs when the source and drain are reversely biased ($V_{SD} > 0$) in a common drain configuration (Fig. 1.3). This indicates the presence of a tunneling junction in the device, similar to what happens in Esaki diodes, which are p-n junctions with reverse bias [20, 21]. The mechanism behind this phenomenon is explained in Fig. 1.3 b–e. As $V_{SD}$ increases, the source band edges move downward and create a larger tunneling window. This results in a higher tunneling current until the source valence band aligns with the channel conduction band, reaching the peak current at $V_{SD} = V_P$.

If $V_{SD}$ continues to increase, the tunneling path is blocked and the current drops (Fig. 1.3d), creating an NDR region (Fig. 1.3a). When the source bands are lowered enough that carriers can thermally overcome the energy barrier (Fig. 1.3 e), the current rises sharply again. Therefore, a typical TFET shows a peak and a valley in the current, and their ratio (PVCR) is used as a measure of the quality of the tunnel junction. However, not all TFETs exhibit NDR, and this depends on the design and material of the structure.

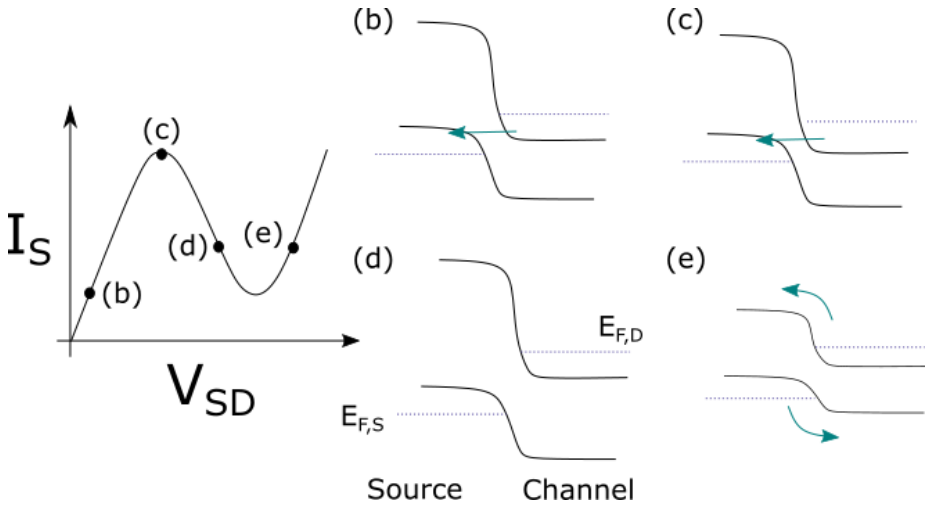


**Figure 1.3:** NDR I-V curve of a TFET at a fixed $V_G$. $V_P$ is the corresponding voltage at the current peak and the peak-valley current ratio (PVCR) typically describes how strong the NDR effect is. (b)-(e) The corresponding changes in band diagram.

### 1.2.3 TFET QUADRANTS OF OPERATION

Fig. 1.4 summaries the varies modes of operation of a TFET under different biasing conditions. Designing circuits with TFET is tricky as a slight variation in baising conditions, changes the device operation of the transistor. On the other hand, the versatility offered by TFETs finds application in various low-power systems. To explore this further, we look into voltage-mode and current-mode operations of TFET circuits in chapter 3.

## 1.3 GEOMETRIES

In 1974, Dennard formulated that the transistor operating characteristics are preserved if all the transistor dimensions and supply voltage are scaled by the same factor [22]. This came to be known as Dennard's law and preserving constant power density became a guiding principle in scaling the transistor and associated interconnects. Reducing the area of the transistor reduces the necessary drive voltage and the capacitance thereby allowing circuits to operate at higher frequencies at the same power density. Beginning with the 65 nm node size, the supply voltage reduction became unfeasible due to non-scalability of the threshold voltage. The effects were further exasperated by the increasing leakage currents with scaling, with power supply voltage

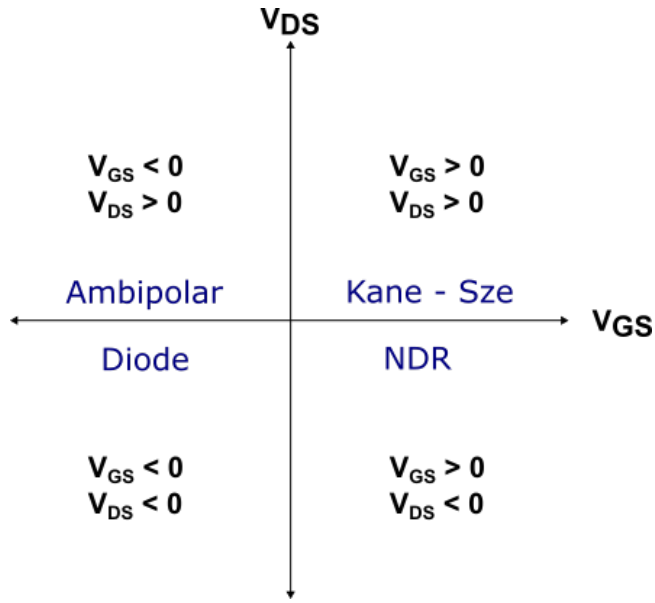


**Figure 1.4:** The operation of n-type TFET based on the bias voltages applied.

saturating at 0.5 V. The power wall led to multicore scaling whereby the number of cores per die was increased to maintain the performance growth. The power constraints prevent all cores to be utilized simultaneously, leading to an interesting scenario where even though the number of transistors in a chip can be increased, in accordance with Moore's law, they cannot be fully utilized.

The transistor scaling though continued unabated thanks to the introduction of new channel materials like SiGe, strained-Si; high-k gate oxide, metal stack and new process development schemes such as self-aligned multi-patterning lithography techniques [23–27]. A different trend also emerged, known as More-than-Moore (MtM), where the focus is functional diversification of devices for niche applications in automotive, medical, communication, infotainment, security etc. Here, device architectures consisting of multi-gate architecture, 3D stacked nanosheets/ribbons with gate-all-around configuration in lateral devices to improve gate control on the channel are explored for reducing leakage. The gate control over the channel must be as efficient as possible. Initially, it was achieved by increasing the coupling of gate voltage with the channel potential by reducing the effective oxide thickness. Once the near defect free high-k material was utilized for gate oxide, further the enhancement of gate control over the channel can be attained by using

a double gate or gate all around configurations, rather than a single gate configuration [28–30]. The gate configurations are shown in the Fig. 1.5.

A transition from horizontal to vertical transport has also been suggested to reduce device footprint. Such vertical devices have recently been demonstrated by IBM, Zurich, CQEST, Japan, KAIST, South Korea, among others [30–32]. In this thesis work, we concentrate on such a vertical nanowire structure with gate-all-around geometry.Due to high current density and low cross-sectional area, the local temperature may be higher in a vertical transistor structure due the limited volume for heat dissipation from the nanowire into the substrate [44]. Furthermore, due to the confined geometry and larger surface-to-volume ratio, the phonon-boundary scattering in III-V vertical nanowire is expected to be more prominent than in FinFETs and we may expect increased thermal resistance. Chapter 4 studies the effect of self-heating on device performance.

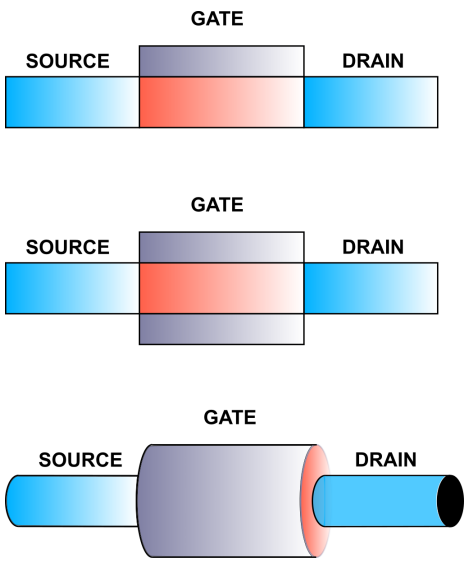


**Figure 1.5:** (a) Single-gate (SG), (b) double-gate (DG), and (c) gate-allaround (GAA) geometries.

## 1.4 MATERIALS AND DEVICE PERFORMANCE

Silicon has been the mainstay of semiconductor industry due to it's abundance, ease of forming insulating oxides and high density of state (DOS). The use of silicon in MOSFETs have worked remarkably well, even in MtM era. With regards to TFET though, they suffer from low on-currents. To improve

the current levels, materials with lower effective mass, narrower band-gap and shorter transition length is needed, as dictated by the tunneling probability equations. III-V semiconductors are one such class of direct band gap material that allows for band gap engineering and optimization of the junction to reach higher on- currents than what TFETs made of group IV are able to achieve. Table 1 shows the BTBT material parameters for Si, Ge and different III-V materials. Referring to Eq. 1.2, we prefer materials with narrower bandgap and $\Lambda$, i.e. higher values for parameters A and B.

Using III- V semiconductors, TFETs with homojunction or heterojunction (staggered or broken band-gap alignment) have been demonstrated. However, due to a higher number of defects in the bulk and at the interfaces, no device have demonstrated ability to operate well below the thermal limit while maintaining high subthermal current levels. Both, Ahn et. al. and Alain et. al. has fabricated planar InGaAs TFETs with homojunction, which were able to reach a minimum subthreshold swing of 57 and 54 mV/decade at $V_{GS}$ = 0.1 V, respectively [33, 34]. To improve the current further, usage of staggered heterojunction is necessary. So far the TFETs with staggered heterojunction have demonstrated the best combination of currents and subthreshold swing. Dewey et. al. used a undoped $In_{0.7}Ga_{0.3}As$ pocket to form a staggered heterojunction in an InGaAs TFET, which resulted in three times higher current levels than comparable TFET with a homojunction [35]. Zhou et. al. demonstrated vertical TFETs with broken heterojunction implemented using InAs/GaSb. These devices reached 180 µA/µm at $V_{GS}$ = $V_{DS}$= 0.5 V, with a minimum subthreshold swing of 200 mV/decade. Dit could be reduced by using forming gas annealing, which improved the minimum subthreshold swing to 150 mV/decade [36]. By using template-assisted growth, lateral InAs/GaSb nanowire TFETs with gate-all-around were demonstrated by Cutaia et. al [37]. nTFETs achieved an average subthreshold swing of 140 mV/decade and an on-current of 40 µA/µm at $V_{GS}$ = $V_{DS}$ = 0.5 V. The on-current and subthreshold swing of these devices were limited by the undoped source, which resulted in source depletion. Tomioka et. al. demonstrated vertical nanowire InAs/Si TFETs with minimum subthreshold swing of 21 mV/decade at $V_{GS}$ = 1 V and on-current of 1 µA/µm at $V_{GS}$ = $V_{DS}$ = 1 V. InAs nanowires, with a diameter of 30 nm, were in these devices grown on a Si-wafer utilizing template-assisted growth [38].

As these presented publications show, there are several challenges to overcome when designing TFETs based on group IV or III-V semiconductors. An abrupt tunneling junction is required both for composition and doping. The interface between III-Vs and high-k needs to exhibit a very low Dit to reduce defect assisted tunneling (DAT) [19, 39]. Furthermore, an ultra-thin geometry is needed for robust electrostatic control. TFETs based on

**Table 1.1:** BTBT parameters from Kane's formalism. Data is taken from [45, 46].

| Semiconductor | Eg(eV) | me( *mo) | A($cm^{-3}s^{-1}$) | B($cm^{-3}s^{-1}$) |
|---|---|---|---|---|
| Si | 1.12 | 0.2 | 4*$10^{14}$ | 19*$10^{6}$ |
| InAs | 0.35 | 0.023 | 1.7*$10^{20}$ | 1.3*$10^{6}$ |
| $In_{0.53}Ga_{0.47}As$ | 0.74 | 0.043 | 1.6 *$10^{20}$ | 5.6 *$10^{6}$ |
| $In_{0.73}Ga_{0.27}As$ | 0.77 | 0.045 | 1.7 *$10^{20}$ | 6.3 *$10^{6}$ |
| $GaAs_{0.5}Sb_{0.5}$ | 1.34 | 0.08 | 1.6 *$10^{20}$ | 18 *$10^{6}$ |

two-dimensional materials (2DMs) show some desirable properties, however these novel materials also require more material research and development to improve the currents [40–42]. In this work, we take established III-V materials as a base for improving the current levels in a TFET. A meticulous control of heterojunction is needed to improve the device performance, thereby III-V materials which offer extensive options on band-structure engineering are preferred. Furthermore, in Lund University, we have been able to make near-defect free heterostructures, which improves device off-state performance [43, 44].

## 1.5 METRICS FOR TRANSISTOR PERFORMANCE

In a transistor, the current is controlled using a gate, drain and source voltages. All data presented in this thesis is measured using common-source configuration, which means that the source is the common voltage reference for the gate and drain voltages. Thereby, the gate voltage is written as $V_{GS}$ and drain to source voltage as $V_{DS}$. To make a proper characterization of the transistor there are a number of metrics that are used, and these will be described below.

### 1.5.1 DRIVE CURRENT

Transfer (linear and logarithmic) and output graphs are shown in Fig. 1.6 a, b and c, respectively. These two graphs describe the dependence of the current, that flows between the source and drain, on the gate and drain voltages. As the transistor switches from off- to on-state, the current will change its magnitude with several orders, thereby to study the off-characteristics the current in the transfer graph is plotted using a logarithmic scale, Fig. 1.6 b.

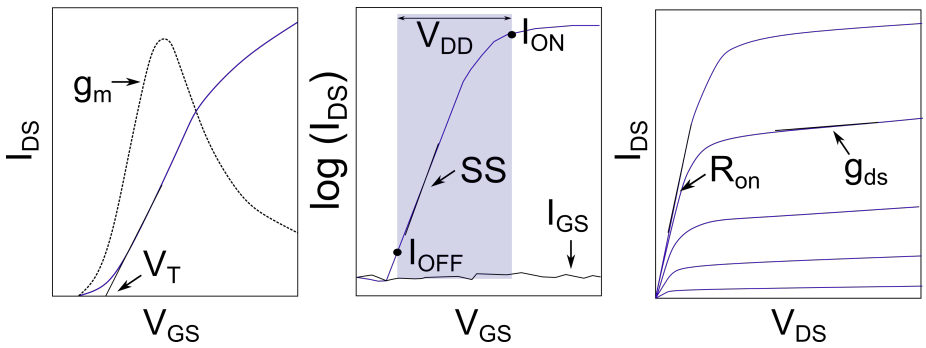


**Figure 1.6:** Electrical characteristics of a vertical InAs nanowire TFET (a) Transfer curves of a transistor in linear scale, where $g_m$ is the transconductance and $V_T$ is the threshold voltage. (b) Transfer curve in logaramithic scale, indicating on- and off-currents, gate current and subthreshold swing and (c) Output characteristics, where $g_{ds}$ is the output conductance and $R_{on}$ is on-resistance.

Using these graphs, metrics that are important for transistors performance can be determined. For the digital circuits, the ratio between the off- and on-current is of importance, thus it is important to clearly see the difference between the zero and one state. In general, when discussing currents for digital applications, usage of $I_{OFF}$ and $I_{ON}$ is common. $I_{ON}$ is usually determined with reference to $I_{OFF}$, in this work $I_{OFF}$ is always taken as 1 nA/$\mu$m. The currents are normalized to diameter of InAs drain, which is between 20-22 nm, depending on the specific device.

### 1.5.2 TRANSCONDUCTANCE

From the transfer curve, the transconductance ($g_m$) can be extracted. Definition of the transconductance is partial derivative of the drain current with respect to the gate voltage.

$$g_{\mathrm{m}} = \partial I_{\mathrm{D}} / \partial V_{\mathrm{G}}$$

This metric describes how effective a transistor amplifies a small voltage on the gate, which is an important metric for analog applications where the transistor is used to amplify signals. However, also in digital circuits high $g_m$ is beneficial, as a high $g_m$ and low subthreshold swing allows for large on-current.

### 1.5.3 OUTPUT CONDUCTANCE

The dependence of the output current on a change of the drive voltage ($V_{DS}$) is described by output conductance, defined as

$$g_{\mathrm{ds}} = \partial I_{\mathrm{D}} / \partial V_{\mathrm{DS}}.$$

The output conductance ($g_{ds}$) is extracted in the saturated region of the output graph as shown in Fig. 1.6 c. Preferably this value should be as low a possible to ensure linearity and a good gain when the transistors are used as amplifiers. For an ideal MOSFET, the value is zero. However, in real devices drain-induced-barrier lowering (DIBL) and channel length modulation will increase the output conductance.

### 1.5.4 THRESHOLD VOLTAGE

The threshold voltage ($V_T$) is used as a reference point when the transistor switches between its off- and on-state. The threshold voltage of a device is in one definition extracted by fitting a line to the point at $g_{m,max}$ and extrapolating the line down to the x-axis as shown in Fig. 1.6 a. Depending if the $V_T$ is positive or negative the transistor is said to be an enhancement or depletion mode device, respectively. If the gate voltage is zero, a depletion mode device is in the on-state and a enhancement mode device is in the off-state. Enhancement mode transistors are important for both digital and analog circuits so that the transistor is turned off when no gate is applied. This ensures that the static power consumption is minimal.

### 1.5.5 SUBTHRESHOLD SLOPE

The subthreshold slope is a partial derivative of the drain current on a logarithmic scale with respect to the gate voltage in the subthreshold region of the transistor. In the literature, the numbers that are provided for this metric represents the inverse subthreshold slope which is also referred to as subthreshold swing [10].

$$\mathrm{SS} = \frac{\partial V_{\mathrm{G}}}{\partial log(I_{\mathrm{D}})} = \ln(10)\frac{k_{\mathrm{B}}T}{q}(1 + \frac{C_{\mathrm{dep}}}{C_{\mathrm{ox}}}) \geq \ln(10)\frac{k_{\mathrm{B}}T}{q} \approx 60\,\mathrm{mV/dec}\,(300\,\mathrm{K})$$

### 1.5.6 $I_{60}$

For TFETs to compliment MOSFETs at low power applications, SS must be maintained below 60 for several decades of current levels. Furthermore, the highest current level where the subthreshold characteristics exhibit a transition from sub- to super-60 mV/decade behavior should be greater than

1 $\mu$A/$\mu$m. To quantify these current levels under 60 mV/dec, we use $I_{60,min}$ and $I_{60,max}$ as defined in Fig. 1.7.

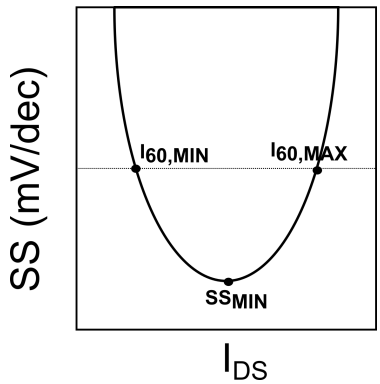


**Figure 1.7:** Subthreshold swing vs drain current, showing the definition of minimum SS, $I_{60,min}$ and $I_{60,max}$.

# 2

# TFET Fabrication and Heterostructure engineering

In chapter 1, we discussed the superior TFET performance offered by III-V material with respect to group IV elements. This is achieved in part due to near defect free growth of the III-V nanowire, along with optimal band strucuture engineering. In this chapter, we elaborate on the nanowire growth, TFET fabrication process, and the optimization of heterostructure to improve the device performance.

## 2.1 NANOWIRE GROWTH

There are two favoured approaches for the growth of semiconductor nanowires; top-down or bottom-up processing. In the top-down approach, thin-films of the desired structure are grown on the wafer and then are selective etched to provide the desired nanowire. In the bottom-up approach, seed-particles are used to catalyze the growth in desired region [47]. Nanowires of both group IV and III-V materials have been grown using this method, including Si, Ge, InAs, InP, GaAs, GaSb, InGaAs, etc [48–50].

In the bottom-up method, gas-phase precursors of the desired material composition and are used to grow the nanowire in the presence of nanoparticle catalyst. In this work, a bottom-up method is used with Au-seed as catalysts that are positioned on an InAs layer on top of a Si-wafer. The use of Si wafers make it compatible with existing processing techniques and an simple way to integrate III-V materials in Si. Nanoparticle dimensions of the catalyst particle which is the basis for the growth are defined with EBL. The size of the particles is determined by the electron dose, the resist thickness, and the thickness of the evaporated metal layer.

This process allows for simple scaling of the numbers of nanowires in every device. The growth of the nanowires is performed using metalorganic vapor phase epitaxy (MOVPE). Group III-precursors (TMGa, TMIn) and group V-precursors (TMSb, $AsH_3$) are used as source materials. In theory, the composition and crystal structure of the nanowires are controlled by the growth temperature, and the amount of and ratio between the precursors in the chamber. However, this picture is more complicated in reality since the ratio that matters is the ratio between the precursors in the direct proximity of the seed particles . This ratio is influenced by the surface of the sample and the distance between the seed particles as they are competing against each other for the material. The growth direction for the nanowires is <111>, with the crystal structure being either zincblende (ZB) or wurtzite (WZ). It should be mentioned that the crystal structure a material exhibits in bulk is not necessarily the same within the nanowires grown with the bottom-up method. InAs have ZB in bulk, but for certain growth conditions it could be WZ. Furthermore, some of the regions of the nanowires need to be doped to reduce resistance and suppress ambipolarity and related properties. These dopants are introduced during the growth using TESn for n-doping and DEZn for p-doping. Adding these materials can further complicate the growth and influence the morphology of the nanowires [51,52].

## 2.2 FABRICATION PROCESS OF VERTICAL NANOWIRE TRANSISTORS

TFET devices in this work were fabricated by the steps described in this section. For interested readers there is a more detailed description in Appendix A.

1. **Digital etching**: A method to reduce the size of InAs nanowires is to oxidize them with ozone and then remove the oxide layer with citric acid. This is called digital etch. The procedure is repeated until the InAs nanowires reach the desired diameter. The GaSb shell that forms during the synthesis is also eliminated.
2. **High-k**: After the digital etch step, the nanowire is covered in a trilayer high-k dielectric consisting of of 1 nm $Al_2O_3$/ 3 nm $HfO_2$/ 30 nm $Al_2O_3$. High-k are deposited using atomic layer deposition (ALD) at temperatures of 300 °C, 120 °C, and 100 °C, respectively. Prior to the start of the deposition of the $Al_2O_3$, a couple of Al pulses are used to clean the surface thereby improving the interface between the high-k and III-V material.
3. **Bottom-spacer**: A number of different materials (S1800 photo-resist, Silicon oxide (SiOx) and bilayer-stack of $HfO_2$-$Al_2O_3$ with effective

oxide thickness of 1 nm have been used to form the bottom-spacer for the transistors in this work.

4. **InAs-mesa**: A mesa formation step was introduced to etch away the first spacer with HF (1:400) and the underlying InAs ($H_3PO_4$) to isolate the individual nanowires.
5. **Gate**: A 30-nm-thick tungsten (W) film was sputtered on the nanowires. The physical gate-length was set by spin-coating the sample with organic photo-resist (S1800) which covers the nanowires completely. Using Oxygen plasma, the thickness of the resist was reduced to the desired gate length. Using reactive ion etching (RIE), the tungsten was removed from the exposed surfaces with a $SF_6$ in Argon atmosphere.
6. **Top-spacer**: The top-spacer for all transistors fabricated in this work is produced using 10 nm $Al_2O_3$. This differs from the previous generation TFETs produced in the group where organic spacers were preferred. An inorganic spacer was preferred to make it suitable to circuit design and more temperature resilient.
7. **Via-holes**: Using S1800 and UV-lithography the via holes are defined. The holes through the spacers are made using reactive etching and wet etching.
8. **Removing of the high-k**: The high-k on the top of the nanowire and in the drain via-hole is removed with HF(1:400).
9. **Top-metal and contact-pads**: The top-metal is made of Ni and Au, applied by either sputtering or evaporation. S1813 and UV-lithography is used to mask areas where the pads would be. The metal film in uncovered areas is removed using wet-etching.
10. To facilitate circuit design, contacts between TFETs are made using UV-lithography connecting individual transistors in the front-end-of-line (FEOL).

### 2.2.1 CURRENT STATUS OF TFETS

Esaki diodes form the basis for TFETs, as covered in Chapter 1. In 2004, Appenzeller et al., demonstrated the sub-thermal switching of dual gated carbon nanotube FET by tunneling, the potential use of TFET for beyond CMOS began being extensively explored. Si TFET was the first choice for research due to its compatibility with the current fabrication process and the established high-quality interface to high-k gate oxides. But the large and indirect bandgap of Si reduced the tunneling efficiency resulting in insufficient performance. Strained Si and SiGe have been explored to achieve narrow bandgap and direct tunneling [53].

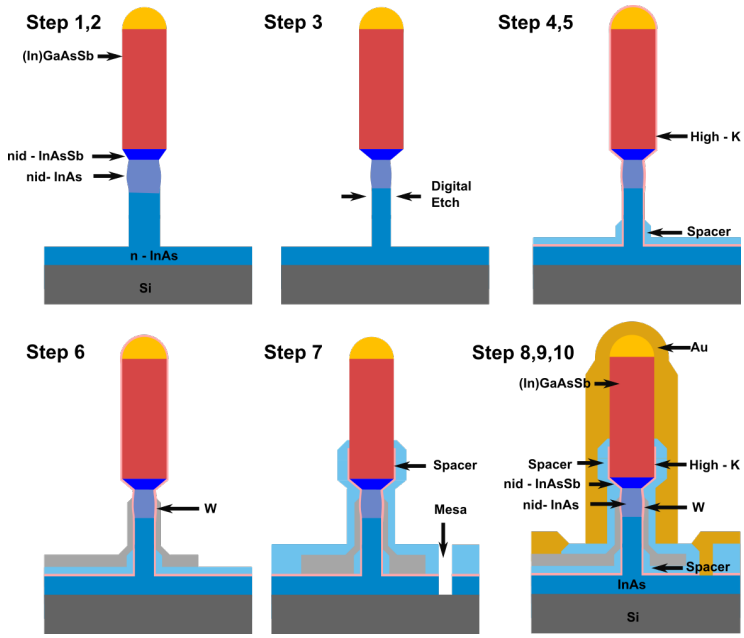


**Figure 2.1:** The processing steps involved in the fabrication of TFETs.

Knoch et al., provided the first insights into improving the performance by using a type-II near-broken band lineup. III-V semiconductors with a wealth of high carrier mobility materials allowing band gap engineering was found to be an appealing candidate for TFETs. Initial implementations of III-V TFETs were on III-V substrates since the large lattice mismatch to Si substrate would lead to high defect density. Seabaugh et al., studied planar InAs/AlGaSb, InAs/InP and InAs/GaSb airbridge TFETs with gate both in-line and normal to the tunneling direction. Contact and access resistances were seen to limit the performance and was circumvented using forming gas anneal (FGA) and SiNx passivation [54]. Datta et al., explored InGaAs TFET as homojunctions, highly doped pocket at the junction and InGaAs/GaAsSb heterojunction and found that tuning the Sb:As ratio of the source helps vary the band offset and hence the tunnel barrier width. Pulsed I-V measurements that mitigate the effects of interface traps on the transistor characteristics and the first report of RF characterization of TFET was demonstrated [55].

Zhao et al., improved the dry etching process for a top-down fabricated NW and demonstrated the first fully vertical III-V TFET with S = 79 mV/dec. Improving the spacer technology helped reduce the S further down to 53 mV/dec. Alian et al., reported InGaAs/GaAsSb vertical NW TFET with S =

47 mV/dec and $I_{ON}$ = 0.7 $\mu$A/$\mu$m. Development of EOT scaling process and analysis of defects helped in the realization of the steep switching devices.

Moselund et al., were among the first few to integrate III-V TFETs on Si substrate by utilizing template-assisted selective area growth of NW. InAs/Si p-TFET achieving S = 70 mV/dec and $I_{ON}$ = 4 $\mu$A/$\mu$m at $V_{DS}$ = -0.5 V had been presented [56].

Heterojunction engineering to achieve balanced on- and off-state performance led to previous works of TFET with S = 48 mV/dec and $I_{ON}$ = 10 $\mu$A/$\mu$m for $I_{OFF}$ = 1 nA/mm at $V_{DS}$ = 0.3 V. For a TFET to be competitive with MOSFET, the $I_{60}$ and $I_{ON}$ must ideally be 1-10 $\mu$A/$\mu$m and 10-100 $\mu$A/$\mu$m while meeting the $I_{OFF}$ requirements for the specific applications. For circuit design, the nuance is set on improving sub-threshold current levels. To compete with MOSFETs at low power applications, the $I_{60}$ should be greater than 1mA/mm at $V_{GS}$ of 100 mV.

## 2.3 IMPROVING THE CURRENT LEVELS

Heterostructure TFETs are sensitive to epitaxy as BTBT is spatially confined within a very short distance across the tunnel junction. Thus, a slight modification at the heterojunction can substantially change the performance. In this section, we look into two aspects; the position of source dopant and the source dopant concentration, and understand their effects on TFET current levels. As described in Chapter 1, $I_{60}$ and SS would be the key parameters to benchmark the device performance.

### 2.3.1 HETEROSTRUCTURE ENGINEERING

Band alignment at the tunnel junction can be varied by changing the composition of the source segment [57, 58]. In paper II, one such variation analysis is performed. A systematic evaluation of delaying the introduction of Ga (TMGa) and Zn dopant (DEZn) into the source segment is performed to study the inflence in SS and $I_{60}$. Four different sample, A-D was evaluated in the series, based on the introduction time variation (Table 2.1). Fig. 2.2 shows the transfer characteristics and subthreshold swing (SS) of representative devices for samples A-D at $V_{DS}$ of 500 mV. The compositional variation due to delay in DEZn introduction shifts the valence and conduction band to lower energies, leading to a decrease the effective tunnel barrier. This changes the heterojunction from staggered to near broken, thereby improving current levels. Delaying TMGa seems to have no effect on device properties.

The main optimization in growth which led to improvement in device parameters was to delay the introduction Zn dopant into the source segment.

**Table 2.1:** Sample list used to evaluate the nanowire source growth. TMSb is introduced first, followed by TMGa and DeZn; delayed by the time(s) mentioned in the table.

| Sample | TnSb | TMGa delay (s) | DeZn delay (s) |
|---|---|---|---|
| A | 0 | 5 | 5 |
| B | 0 | 8 | 8 |
| C | 0 | 10 | 8 |
| D | 0 | 5 | 0 |

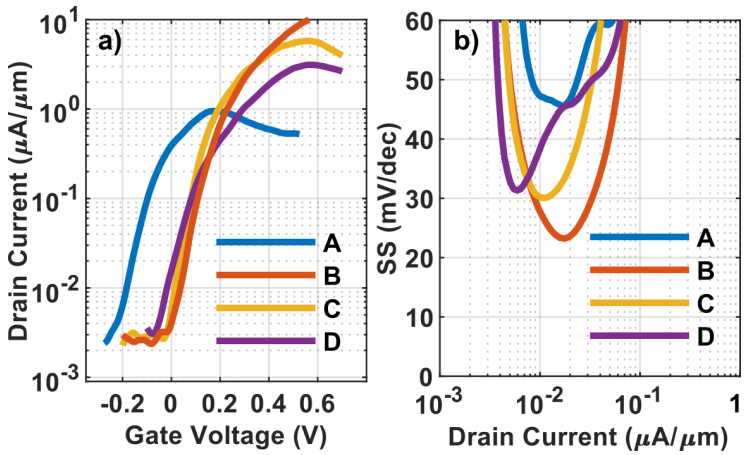


**Figure 2.2:** (a) Measured transfer characteristics of representative devices from A-D for $V_{DS}$ of 0.3 V and (b) respective subthreshold swing vs drain current. The lowest slope is 26 mV/dec for sample B.

It results in a longer unintentionally doped InAsSb segment which has a narrower bandgap than InAs. Due to the doping delay, the majority of the tunneling occurs at the p-(In)GaAsSb/nid-InAsSb interface, leading to a larger energy window for tunneling compared to that of InAs channel according to the band diagram in Fig. 2.3. Combined with that the carrier effective mass in InAsSb is smaller than that in InAs, the tunneling current thereby would increase, resulting in a higher $I_{ON}$.

### 2.3.2 DOPANT LEVELS

Even though the TFETs device parameters were improved by optimization of dopant positioning in the source, the goal of $I_{60} > 1$ $\mu$A/$\mu$m was not achieved.

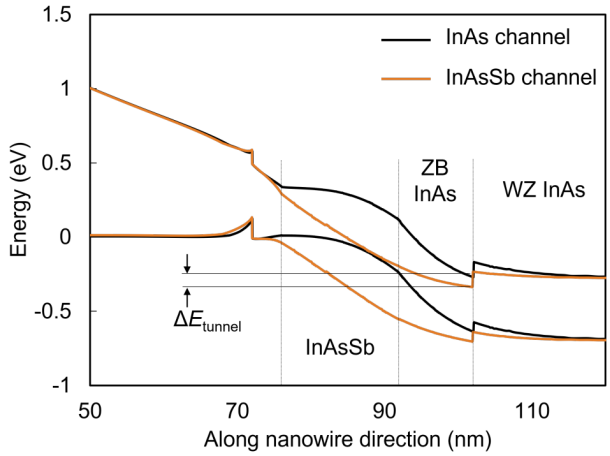


**Figure 2.3:** Band diagram simulation of heterojunction TFETs with InAsSb channel compared to InAs channel. $\Delta E_{tunnel}$ indicates a larger energy window for tunneling in the case of InAsSb channel.

One way to improve the performance further is by optimization of dopant levels in the source [59–62]. A careful study in variation of doping level was conducted in paper I and II. High levels of doping will lead to introduction of states in the bandgap which increases subthreshold swing. These states affect the valence band-edge of the source and reduce the filtering efficiency of carriers in the Fermi-tail. Furthermore, high doping can lead to degeneracy, which diminishes filtering of charge carriers at the junction. Additionally, these bandgap states can cause more leakage paths that degrade the off-state when the channel has very few charges. On the other hand, too low source doping can result in source depletion, which affects the on-performance of the devices by increasing tunneling length and barrier height. Furthermore, a low source doping level will increase resistive loss and lower the current. Thereby, a detailed analysis of TFET device parameters is conducted by varying the source doping levels.

Among the devices, sample B and C exhibit the highest on-current, as discussed above. Device C exhibits a negative threshold voltage while device B, exhibits a positive threshold voltage. To minimise the static power dissipation, an enhancement mode device is preferred. Thereby, to optimize the device performance further by optimizing the source doping level, sample B was chosen as the best candidate. Choosing sample B as baseline, Zn dopant level concentration was varied from $0.5 \times 10^{19}$ cm$^{-3}$ to $3 \times 10^{19}$ cm$^{-3}$ with steps of $0.5 \times 10^{19}$ cm$^{-3}$, producing six samples E to J.

Fig. 2.5 (a) shows the transfer characteristics and $I_{60}$ statistics of TFETs for samples E-J at $V_{DS}$ of 500 mV. Lower doping causes source depletion and increases the barrier height and tunnelling distance. This leads to lower current. High doping gives rise to source degeneracy and softens the TFET turn on characteristics.

The device performance parameters increases with doping before peaking at an intermediate level. Thereby, for a constant density of states, TFET current level saturates at a certain doping level. This trend corresponds well with the reported analytical models [59, 61]. We get an optimized value for source doping at $1.5 \times 10^{19}$ $cm^{-3}$.

This level of optimization led to record performance device with an $I_{60}$ of 1.2 $\mu A/\mu m$ at $V_{GS}$ of 100 mV and $V_{DS}$ of 500 mV.

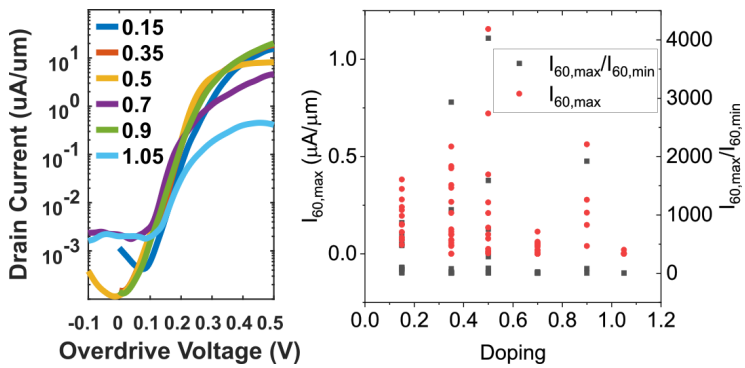


**Figure 2.4:** a) Transfer characteristics, and b) $I_{60}$ at $V_{DS}$ of 500 mV statistics of TFETs from E-J series

The following figure shows the SEM image of nanowire used in the first series A-D and the second series E-J. The variation in the source composition led to highest reported $I_{60}$.

## 2.4 BENCHMARKING OF DEVICES

In general, Si TFETs with homojunction exhibit the widest tunneling barrier and thereby also shows the lowest on-current and off-current. However, these devices operate well below the thermal limit reaching down to 20-30 mV/decade. In contrast, heterostructure TFETs with broken or near broken band-gap alignment exhibit the highest on-currents due to a thin barrier. In between the devices with the widest and thinnest tunneling barrier there are devices with a staggered heterojunction. Those devices exhibit higher currents

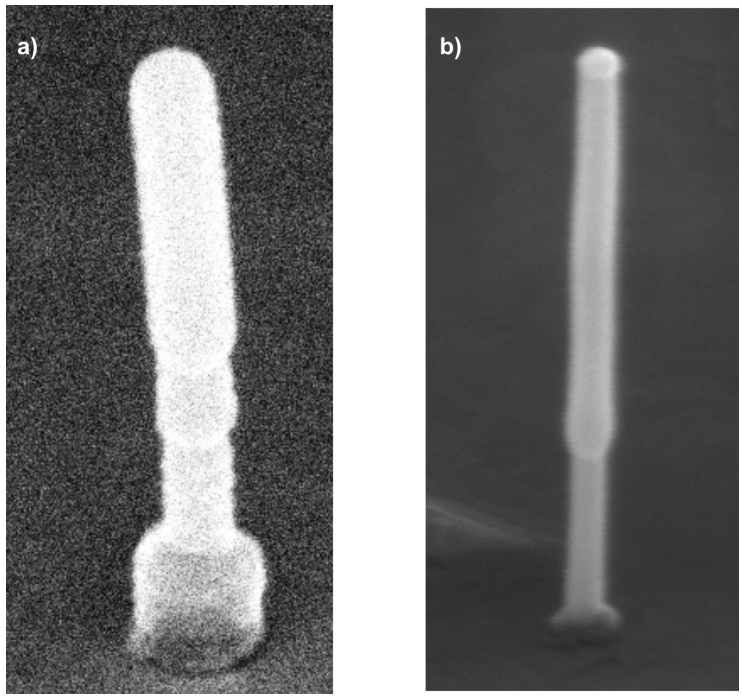


**Figure 2.5:** SEM images of nanowire used in a) Series A-D and b) series E-J

as compared to devices with a homojunction and with a lower subthreshold slope than devices with broken heterojunction.

The data from InAs/GaSb and InAs/InGaAs/GaSb nanowire TFETs in this thesis is benchmarked against some of the published data. Since the focus of the thesis is on low-power circuits based on TFETs, emphasis is placed on the current levels in the device in the subthreshold regime. The ON-currents, although an important metric, is usually benchmarked in regions where SS > 60 mV/dec and thereby are de-emphasized. [35, 42, 51, 52, 63–66].

Vertical InAs/(In)GaAsSb/GaSb nanowire TFET in this thesis have shown promising results. Data from two devices with different (In)GaAsSb compositions is presented. These devices exhibit a subthreshold swing of 26-45 mV/decade at $V_{GS}$ = 0.1 V, which is lower than what previous III-V TFETs have a demonstrated. Furthermore, operation below 60 mV/decade occurs at $I_{60} > 1\ \mu A/\mu m$ at $V_{DS}$ of 500 mV, much higher than what previously published devices have demonstrated. The strength of this data is the combination of large currents and operation well below 60 mV/decade, which are required for circuit applications.

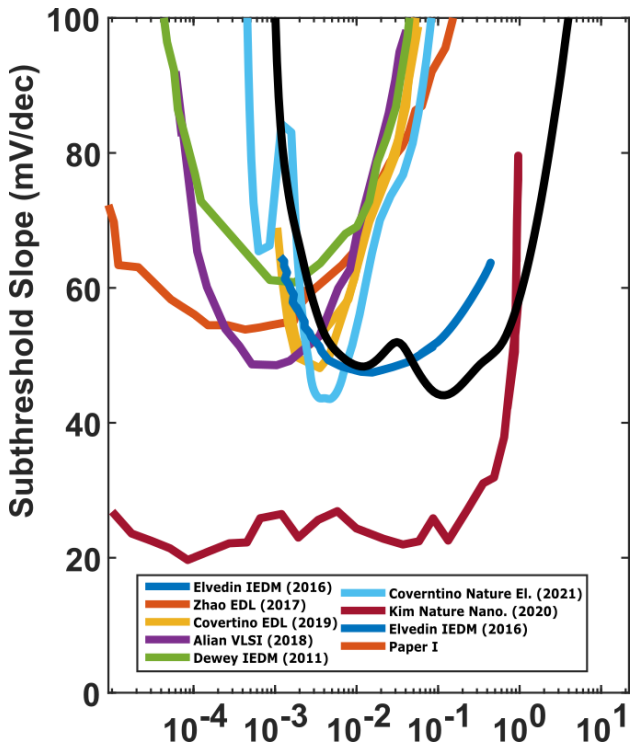


**Figure 2.6:** SS versus $I_D$ for different types of state-of-the-art III–V TFET based on both homojunction and heterojunction designs (thermionic limit is represented by dashed line). Among the presented devices, TFET in Paper I features the highest $I_{60}$.

# 3

# TFET based Circuits

Various claims has been made about potentila TFET circuit operation. Prominently, a TFET can operate with larger transconductance to current ratio ($g_m/I_d$) than traditional field effect transistors in the sub-threshold region [67]. In addition, the higher output resistance offered by TFET-based designs allows achieving significantly higher intrinsic voltage gain and higher maximum-oscillation frequency at low current levels [7, 8, 68]. These claims, though feasible, hasn't been validated with fabricated devices or circuits. Due to its p-i-n structure and operating principle, circuit design challenges in TFETs are quite different from MOSFETs. The major differences that emerge are as follows: TFET exhibits ambipolarity. For nTFETs, at sufficiently high negative gate-source voltage, the transistor turns on. Ambipolarity can be suppressed when the source doping is kept higher than the drain. This doping asymmetry poses a different challenge. At negative $V_{DS}$, the p-i-n diode is forward biased, and a negative differential region is observed. This limits TFET bias voltage rangewhen compared to MOSFET. In typical TFET output characteristics exhibit an exponential onset followed by distinct saturation. This exponential onset can be explained by the large quantum capacitance of the inversion channel in the on-state of the device and not by contact related effects. The way these affects circuit design are to be determined and quantified. Furthermore, analysis are also needed on temperature characteristics of TFET based circuits. BTBT mechanism has weak dependency with temperature which makes TFETs susceptible to performance variations with temperature. In this chapter, we look into all these aspects of TFET circuit operation by implementing voltage-mode and current-mode building block circuits and studying their performance.

## 3.1 VOLTAGE MODE DEVICES

The ability to duplicate signals accurately is important because it allows us to use an intermediate result as input to subsequent signal processing. Computation itself is, however, the result of combining signals and produce a result that is some function of the input signal. A digital system has many such ways of combining and manipulating signals. The most crucial of them are current mirror, inverter, buffer and differential amplifiers. In this section, we show experimental demonstration of various circuit building blocks designed with n-TFETs. Individual TFET devices are connected by front end of line (FEOL) process, to form the required circuit configuration.

### 3.1.1 CURRENT MIRROR

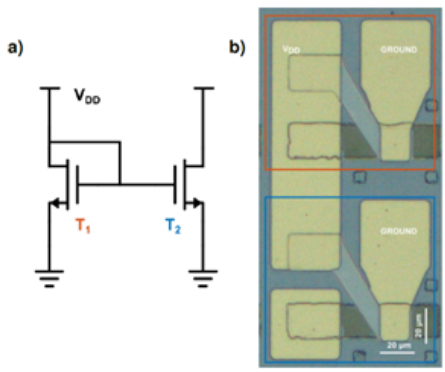


**Figure 3.1:** a) Current mirror schematic and b) FEOL implementation

A current mirror is a circuit block which copies the current flowing into or out of an input terminal by replicating the current in an output terminal. Fig. 3.1 (a) shows the circuit schematic while Fig. 3.1 (b) shows the top view of the fabricated current mirror. Fig. 3.2 (a) shows the current mirror operation. The drain potentials of the two transistors $T_1$ and $T_2$ are kept constant. As the gates are tied together, the $V_{GS}$ of $T_1$ and $T_2$ are the same. When both the devices are applied with the same $V_{DS}$, the current is mirror. We expect the same current as the voltages are the same, but the current in the $T_2$ is greater than that of $T_1$. This is due to a difference in the transmission probability of the two particular TFETs. Furthermore, this difference could also be caused by a difference in the threshold voltage of the individual transistors. These issues can be rectified with uniformity in heterostructure growth of the nanowires and in device processing. The difference in current level can be reduced by changing the drain voltage and the currents can be matched more closely. The

effects due to super-linear onset is absent in both TFETs. The fluctuations in the current level with regard to time is due to random telegraph signal noise. Two interesting observations are to be noted. The TFET based current mirrors are able to mirror current levels at 40 nA. For a MOSFET, the transistors have to be biased close to it's off state to get similar current levels, leading to stability issues. Secondly, the current mirror operation is not affected by drain voltage, leading to better precision matching in comparison with MOSFETs.

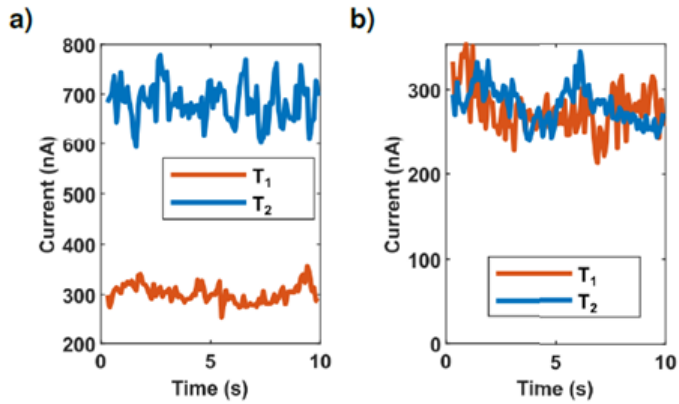


**Figure 3.2:** a) Current levels in current mirror at a) $V_{DS1}$ = $V_{DS2}$ = 500 mV, b) adjusted drain voltage of $V_{DS1}$ = 500 mV, $V_{DS2}$ = 400mV to have equal current

### 3.1.2 INVERTER

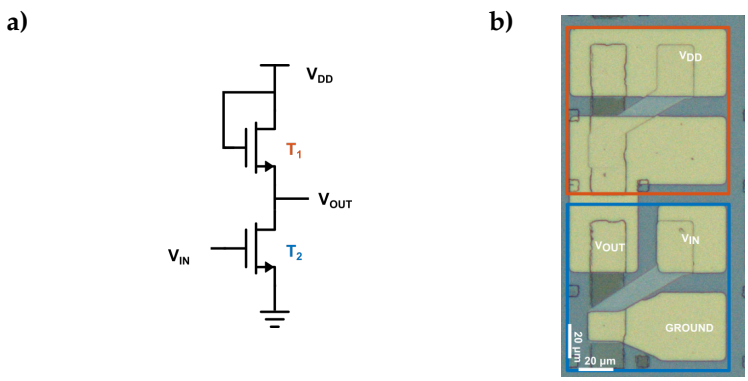


**Figure 3.3:** a) Inverter schematic and b) FEOL implementation

The inverter performs the logic operation of A to $\bar{A}$. When the input to the inverter is connected to ground, the output is pulled to $V_{DD}$ through the device $T_1$ (and $T_2$ shuts off). When the input terminal is connected to $V_{DD}$ , the output is pulled to ground through the $T_2$ device (and $T_1$ shuts off). TFET $T_1$ is operated in the diode mode, it effectively acts as a voltage-controlled resistor.

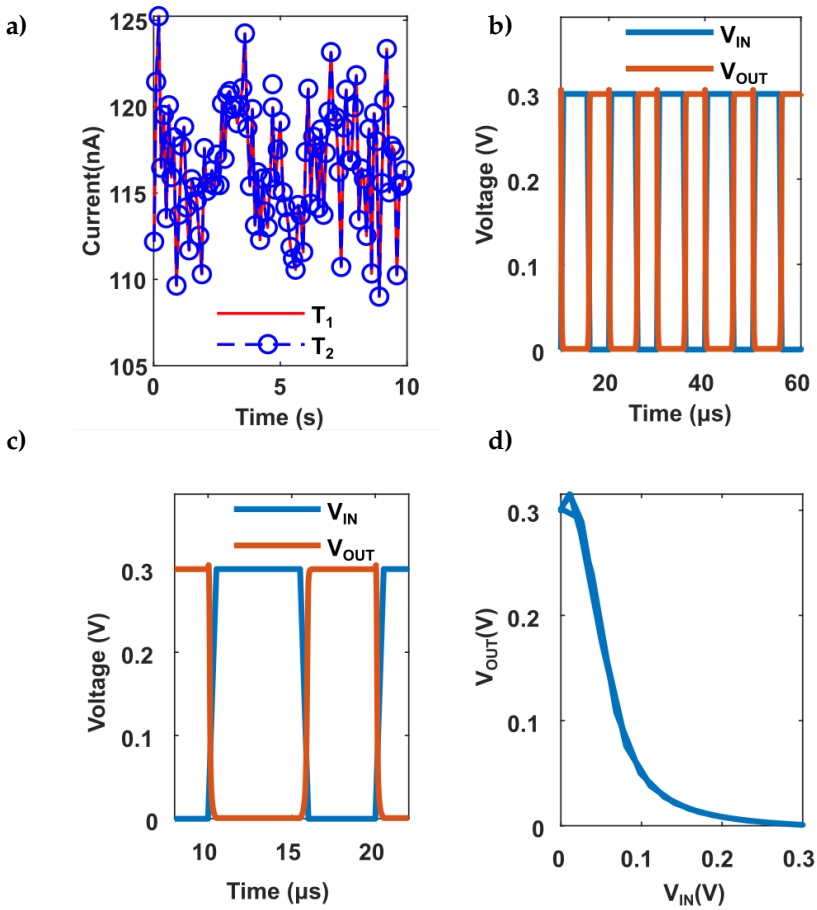


**Figure 3.4:** a) a) Measured current through $T_1$ and $T_2$, b) inverter operation at 200 kHz, and c) zoomed in view of the inverter operation d) VTC of the inverter.

The input signal is fed to the gate of TFET $T_2$, and the output is taken across its drain. The current through $T_1$ and $T_2$ are the same during the inverter operation. The drain voltage is 300 mV, and the input signal is a

square wave with amplitude of 300 mV, giving an inverted output across the drain of $T_2$. The maximum achieved frequency of operation is 200 KHz in the present setup. The output conductance of the transistor is 10 $\mu$A/$\mu$m. Since the current conduction in TFETs are controlled by the source/channel junction rather than the channel/gate junction as in a MOSFET, the drain influence to current conduction in saturation reduces, and TFET exhibits lower output conductance than MOSFETs, whose $g_{ds}$ is reported to be 200 $\mu$A/$\mu$m. A lower output conductance with a TFET can avoid complexity such as the cascode implementation and associated biasing power in analog designs.

### 3.1.3 CASCODE BUFFER

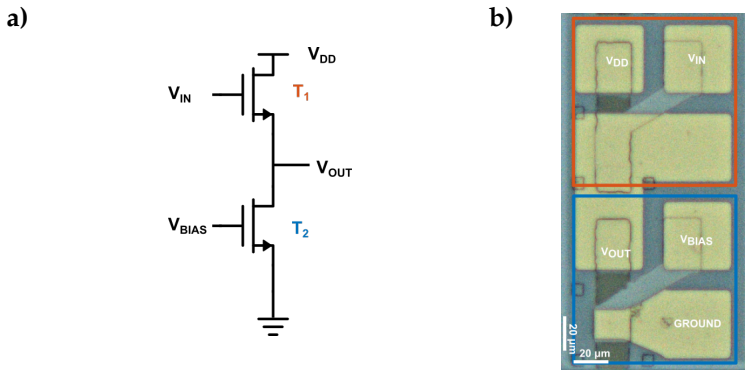


**Figure 3.5:** a) Cascode schematic and b) FEOL implementation

We observed in previous section that the output conductance of TFETs were significantly lower than MOSFETs. Thereby, using TFETs in source follower configuration would provide a higher output impedance and finds application as an impedance transformer. The circuit schematic of a source follower is shown in Fig.3.5 (a) while Fig.3.5 (b) shows the top view of the fabricated configuration. The input signal is fed to the gate of TFET $T_1$, and the output is taken across its source. TFET $T_2$ is operated as a voltage-controlled resistor with DC gate bias voltage $V_{BIAS}$. The transfer and output characteristics of TFET $T_2$ is shown in Fig. 3.7 (a) and (b) respectively. TFET $T_2$ exhibits subthermal operation, as seen in Fig. 3.7 (c). When $T_1$ is measured, it's source is connected to $T_2$ transistor, which acts like a load resistance during DC measurement. This leads to a high off current in $T_1$. This does not affect the operation of the configuration.

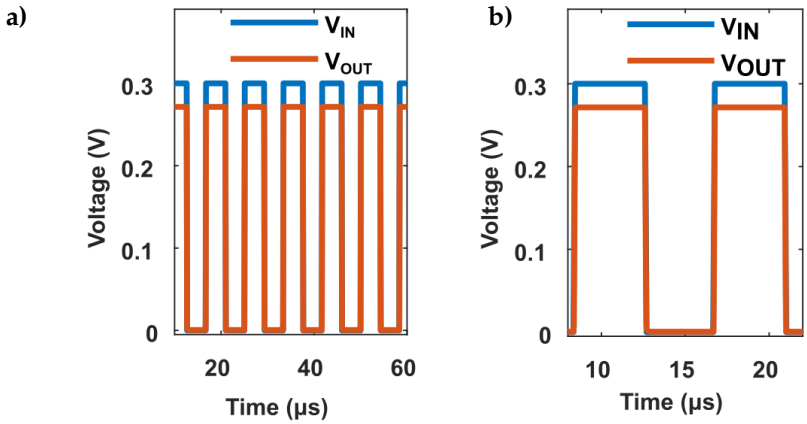


**Figure 3.6:** a) Cascode buffer operation at 120 kHz and b) extended view of the source follower operation.

The gate of $T_1$ is supplied with a square wave of 300 mV magnitude, with drain voltage of $T_1$ maintained at 300 mV. $T_2$ is operated as a source resistor, by applying gate voltage of 300 mV. The expected source follower operation is verified, with only a slight reduction in output peak voltage. The maximum operation frequency was 120 kHz due to parasitics in the current layout. Fig.3.6 (a) and (b) shows the buffer operation. Due to lower $g_{ds}$ of TFETs with respect to MOSFETs, we observe a higher output impedance in the buffer and thereby, lower voltage gain.

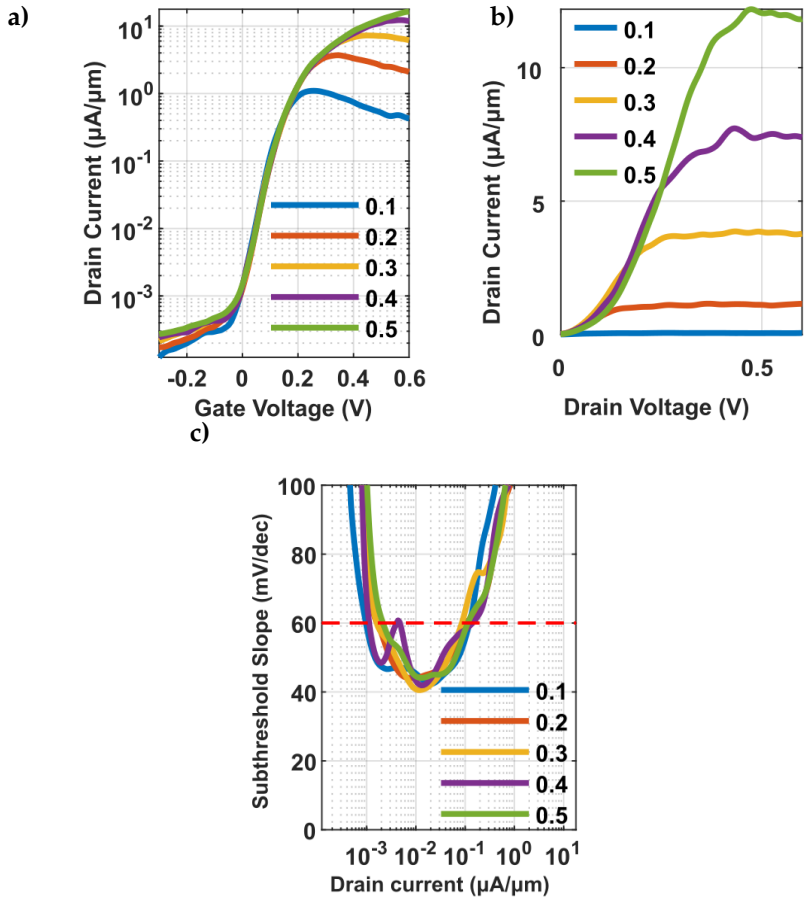


**Figure 3.7:** a) Transfer, b) output, and c) subthreshold slope characteristics of the $T_2$ vertical TFET in cascode configuration

## 3.2 CURRENT MODE DEVICES

The transfer and transconductance effciency of an individual fabricated TFET are shown in Fig. 3.8 (a) and (b). As seen in Fig. 3.8(a), device reaches on-current of 26 $\mu$A/$\mu$m at $V_{DS}$ = $V_{GS}$ of 500 mV. The device exhibits good electrostatics as verified by low drain induced barrier lowering (DIBL) of 20 mV/V. The transistor achieves minimum subthreshold swing(Smin) of 42 mV/dec at current level 12 nA/$\mu$m for $V_{DS}$ of 400 mV.

More importantly, for $V_{DS}$ of 100 mV, $SS_{MIN}$ is 44 mV/dec and is fairly constant across current from 9 nA/$\mu$m to 100 nA/$\mu$m. This is reflected

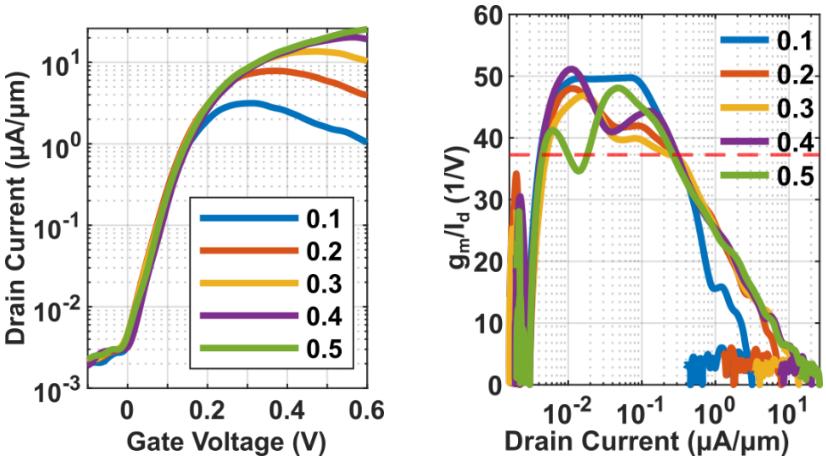


**Figure 3.8:** a) Transfer characteristics and b) gm/Id efficiency of a TFET

in the tranconductance efficiency $g_m/I_d$ as shown in Fig. 3.8(b). TFETs provide higher $g_m/I_d$ than the fundamental limit of MOSFETs of 38 $V^{-1}$. For $V_{DS}$ of 100 mV, it is 50 $V^{-1}$ and over an extended current range implying transistor amplification is balanced for a decade of current consumption. This observation forms the basis for using TFETs as a current mode circuit.

Taking $g_m/I_d$, given by,

$$g_m/I_d = \frac{1}{I_d}\frac{\partial I_d}{\partial V_{GS}} = \frac{\partial(lnI_d)}{\partial V_{GS}}$$

implies that the drain current is exponentially dependent on the gate voltage or transconductance, $g_m$ is linearly proportional to drain current. This means the TFET exhibits this translinear (TL) property and opens a new paradigm in circuit design with TFETs. TL circuit behaviour depend on current ratios within the circuit and are independent of operating current level [69]. The need for wide range of current in subthermal operation as discussed in Chapter 1, is prominent requirement for TL circuit implementation. To better understand the physics behind translinearity observed in a TFET, equations from chapter 1 are revisited.

$$I_{BTBT} = \frac{2q}{h} T_{BTBT}(E) V_{ON} \tag{3.1}$$

$$T_{\mathrm{BTBT}} = \exp\left(-\frac{4\Lambda\sqrt{2m^*}E_{\mathrm{G}}^{3/2}}{3q\hbar\left(\Delta\phi + E_{\mathrm{G}}\right)}\right) \tag{3.2}$$

The approximate the electric field along the nanowire direction is

$$\varepsilon \approx \frac{E_{gc} - \Delta E_v + qV_{on}}{q\lambda}, \tag{3.3}$$

$E_{gc}$ is the channel band gap. $-\Delta$ $E_v$ is the valence band energy difference, and $qV_{ON}$ is band bending due to the applied voltage. $\lambda$ is determined from Poisson's equation and approximately corresponds to the geometric length scale. In the above equation, all parameters other than are material properties. Thereby to derive an exponential relationship with applied voltage, only $\varepsilon$ needs to be engineered in the growth. Accounting for quantization in the InAs channel, GaSb energy level is adjusted with doping to provide the appropriate band alignment at $V_{DS}$ = 100 mV to give the exponential characteristics. Fig. 3.9 shows band diagram of this TFET heterostructure.

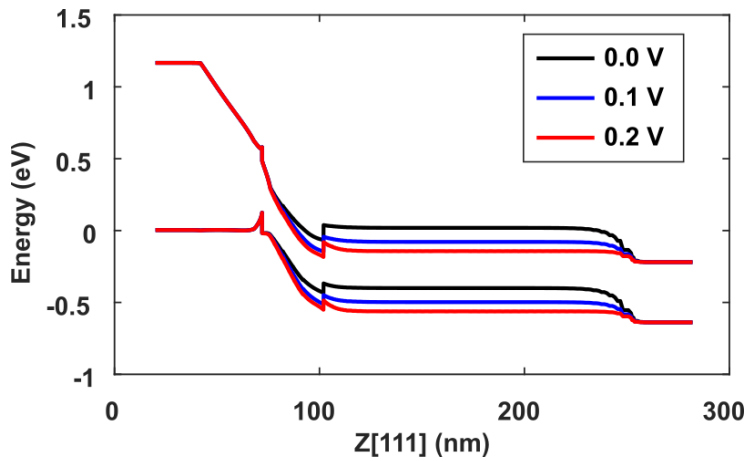


**Figure 3.9:** Band structure of TFET at $V_{GS}$ of 0, 100 mV and 200 mV with constant $V_{DS}$ of 100 mV

This leads to an interesting device aspect. At lower $V_{GS}$, the device can act in current mode and at higher $V_{GS}$, the device can act as a voltage-mode device.

Using this principle, the current-mode characteristics is further explored by analysing a Current-Conveyor. The current conveyor, CCI, was first proposed by Sedra in 1968 as a possible building block for circuit systems that required conveying current between two ports of different impedance levels. A more versatile implementation CCII was introduced a year later [70, 71]. The operation of the CCII current conveyor is such that if a voltage is applied to the high impedance input terminal Y, an equal potential will appear on the

input terminal X. In a similar fashion, an input current I being forced into terminal X will result in an equal amount of current flowing into terminal Z with high output impedance. As can be seen, the potential of X, being set by that of Y, is independent of the current being forced into port X. Similarly, the current through input Z, being fixed by that of X, is independent of the voltage applied at Z. Ideally the terminal X exhibits a short circuit input. In mathematical terms, the input-output characteristics of CCII can be described by the hybrid matrix equation below. Depending on the polarity of the current $I_z$, we can distinguish CCII+ and CCII- conveyors.

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

**Figure 3.10:** $n \times n$ transition matrix for a classical random walk.

To study current-mode-based circuit design feasibility, we implement a positive current conveyor, CCII+ (Fig.3.11 (a)), a circuit building block which finds application in a variety of instrumentation and communication systems today [70]. The circuit consists of a voltage follower, such that the voltage at input terminal X equals the potential applied at input terminal Y, along with a current mirror which equates the current at input terminal X to output terminal Z.

The circuit elements are implemented separately. Individual transistors in the present implementation of the circuit suffer from mismatch due to variability which is mitigated by changing the bias voltages in the individual transistors. The measured large-signal voltage transfer characteristics between terminal X and Y are shown in Fig.3.11(b). Over the linear range, the maximum voltage difference between the terminals is 10 mV. The voltage gain between the terminals is 0.89 mV/mV. The small-signal magnitude response has a bandwidth of 320 kHz. The measured current response between terminals X and Z is shown in Fig.3.11 (c). Measurements are plotted with current error (%) and power dissipation. The current mirroring operation is consistent over a wide range of currents, from 45 nA to 500 nA. The power dissipation of the mirroring operation ranges from 5 nW to 360 nW, demonstrating ultra-low power operation.

## 3.3 TEMPERATURE EFFECTS

TFETs have better temperature immunity than MOSFETS. This stems from weak dependency of BTBT tunnelling with temperature [51, 72]. For MOS-

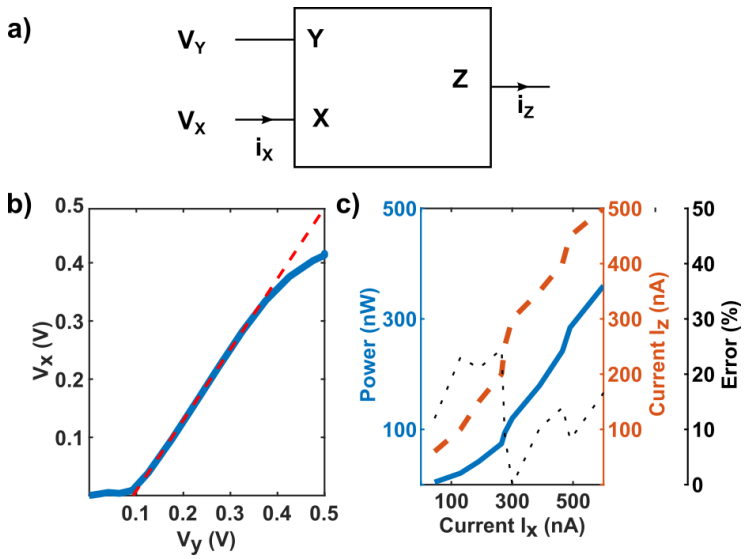


**Figure 3.11:** a) CCII block diagram b) measured voltage characteristics between terminals Y and X, and c) measured current levels and current error between terminals X and Z, along with power consumption.

FETs, especially in subthreshold region, the currents are exponentially dependent on temperature. Fig. 3.12 (a) shows the transfer characteristics of TFET for $V_{DS}$ of 0.3 V at temperatures from 223K to 323 K with 25 K increments and Fig. 3.12 (b), shows the corresponding SS. The minimum SS varies from 26 mV/dec to 56 mV/dec. The improvement of SS is primarily due to the reduction in trap assisted tunnelling (TAT). This increase is less than what is expected from thermionic emission, further confirming the BTBT mechanism. As the temperature raises, the traps in the heterostructure and oxide – channel interface are activated which increases TAT and degrades the performance of the device. The increase in current with temperature is due to this increase in TAT, which increases both the on-current and off-current. A slight increase in BTBT due to decrease in bandgap with temperature, also attributes to the current increase [51,72,73].

Fig. 3.13 (a), (b) and (c) shows the variation in device metrics with temperature. The threshold voltage varies by about 0.65 mV/K with temperature. Thereby, compared to MOSFETs, TFET is more immune to threshold voltage roll off. The shift in threshold voltage though leads to change in operating condition of the circuit. The impact of these effects is prominent in changing biasing of circuits and it is analysed using a current mirror.

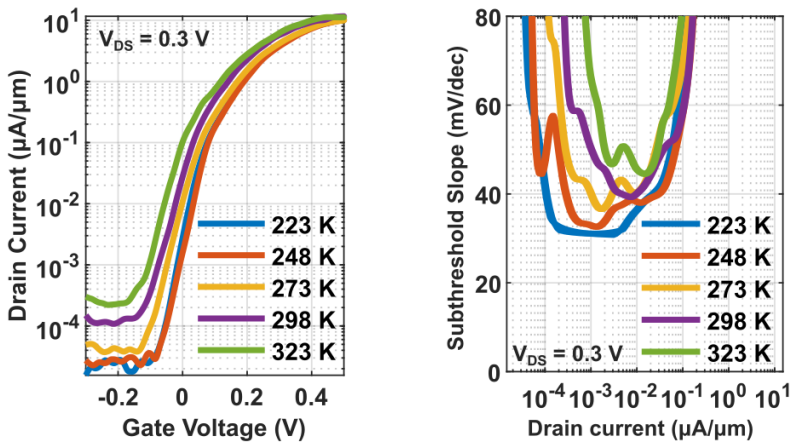


**Figure 3.12:** a) Transfer characteristics b) Subthreshold variation with temperature.

Fig. 3.13(d) shows the output current level of transistors $T_1$ and $T_2$ of the current mirror with respect to temperature. There is an increase in current level with temperature as expected. Due to temperature dependent variation of threshold voltage and transmission probability, the currents are not matched.

Fig. 3.14 shows the variation of SS and $I_{60,MAX}$ of the TFET with temperature from 223 K to 323 K at 25 K steps, for $V_{DS}$ of 100 mV. The data shows the difference between measured SS and thermal limit for MOSFETs increases with temperature. $I_{60,MAX}$, reduces only slightly with raise in temperature, making TFET based TL circuits robust for temperature fluctuation. Moreover, this confirms that BTBT is the dominant transport mechanism.

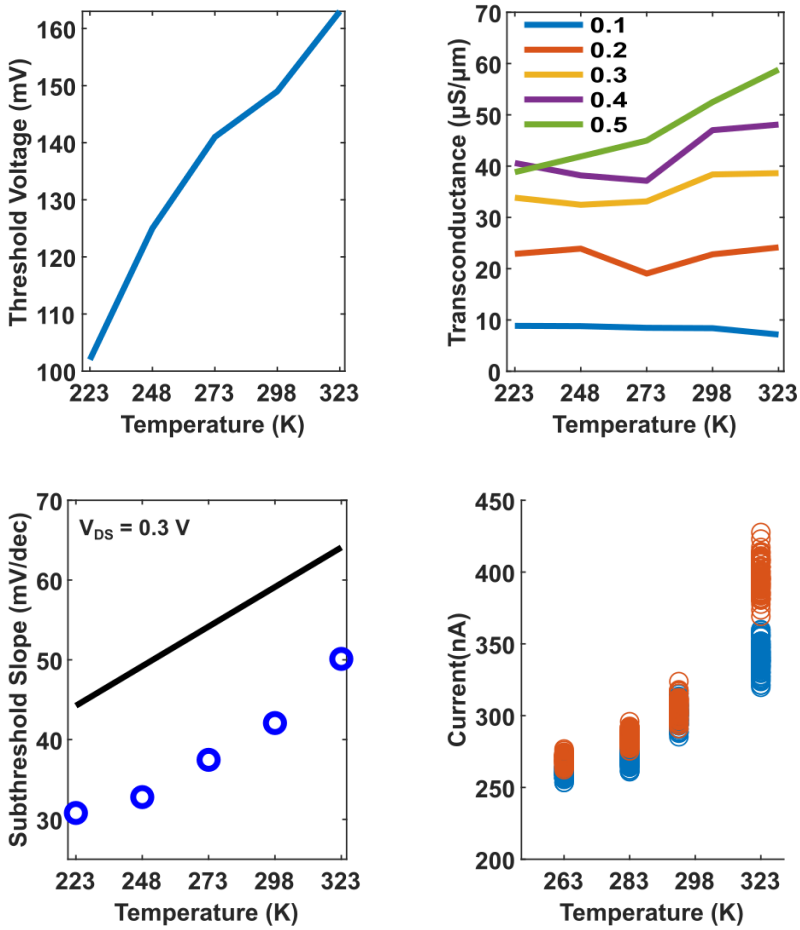


**Figure 3.13:** a) Variation of TFET characteristics with temperature for a) Threshold voltage b) $g_m$ c) SS and d) current in current mirror.

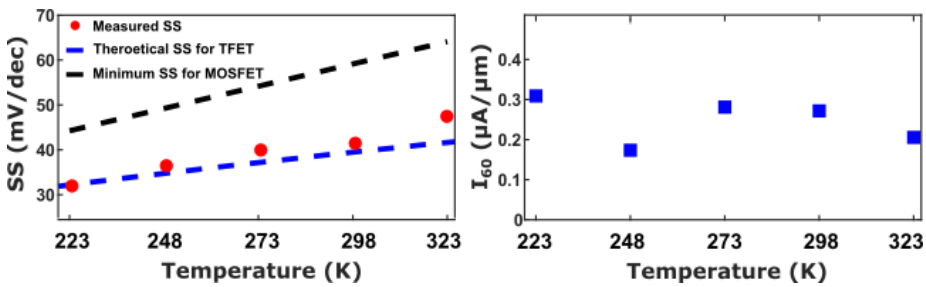


**Figure 3.14:** a) Variation of subthreshold slope and $I_{60,MAX}$ with temperature at $V_{DS}$ = 100 mV. The dotted black line indicates KT-line for minimum subthreshold swing from thermionic emission while dotted blue line indicates theoretical SS for TFETs and b) Variation of $I_{60}$ with tempeature.

# 4

# Self-Heating in Vertical Nanowires

Vertical MOSFETs allow for higher device density as channel length and metal lengths are decoupled. High mobility direct bandgap III-V vertical nanowires (VNW) on Si substrate, along with GAA architecture for better electrostatic control, leads to higher current drivability and finds application in analog and RF domains. Due to their confined geometry, larger surface-to-volume ratios, phonon scattering is more prominent in III-V VNW Transistors than FINFETs. Furthermore, due to higher power density and lower cross section area for heat dissipation from nanowire to the Si substrate, the heat transfer is more limited in the vertical structure. This leads to self-heating (SHE), which brings down the operating frequency and causes reliability issues. Analysing SHE is, therefore, a critical issue in III-V VNW MOSFET. A number of methods have been used to characterize self heating in a transistor, including small signal S-parameter based capacitance extraction, device simulation, pulsed measurements, in-situ breakdown and thermal imaging [74–78]. In this chapter, we describe a fairly simple technique using pulsed-IV measurements and virtual source model to deduce the heating effects in a nanowire. The heating network is modelled as an RC network, with resistive and capacitive thermal time elements with characteristic constants. From the network model, an analytical expression is deduced to extract the heating in the nanowire. The model can handle self-heating effects across a wide range of operating temperatures, from 50 K to 300 K.

## 4.1 MEASUREMENT SETUP

The pulsed measurement is configured as follows, as shown in Fig. 4.1. The WGFMU units are connected to the gate and the drain of the transistor, while

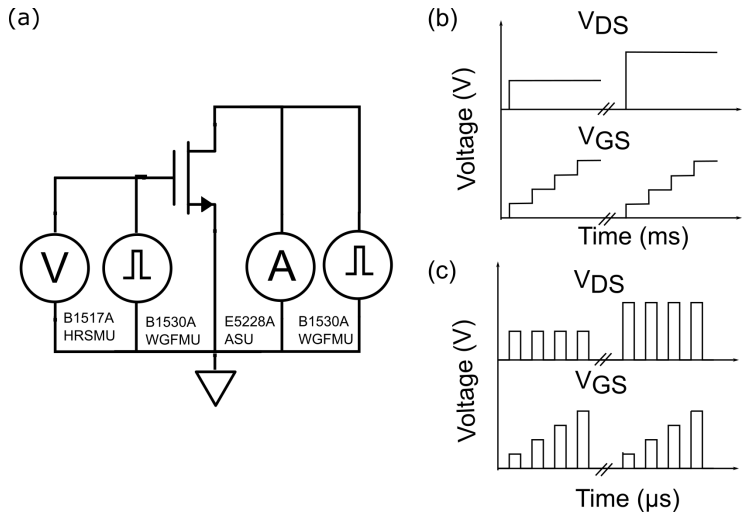


**Figure 4.1:** a) Measurement setup for pulsed IV characterization. Output signal sequence of used in characteristics measurement for b) DC measurements and c) Pulsed measurements.

the source is grounded. WGFMU generates square signals concurrently at the gate and drain terminals for pulse widths as programmed by the user. The subsequent current in the device is measured at the drain terminal. The duty cycle of the pulsed signal is kept to 0.001%. This is done so that the device can thermally relax before the next measurement is taken. As both drain and gate are pulsed, the effective electrical characterization time of the device is reduced by one order **in time** when compared with just pulsing one terminal. Pulse widths are increased from 300 ns to 100 µs in exponential timesteps. 300 ns is assumed to be SHE-free as no current increase is observed for lower pulse widths. Moreover, 100 ns forms the instrumentation limit for the setup. Lower pulse widths might cause transient oscillations, introducing measurement errors [79, 80]. The ambient temperature is varied to understand SHE across various device operating temperatures. The measurement averaging time is 10 ns, the sampling limit of the internal ADC.

## 4.2 PULSED IV BASED SELF-HEATING EXTRACTION

The pulsed IV methodology is presented in paper V. To investigate the heat dissipation within the transistor, we evaluate the different thermal components. The channel temperature during device operation is generally described using an electrothermal RC network, with a thermal resistance

($R_{TH}$) accounting for the power dissipation (P) and a thermal capacitance ($C_{TH}$) accounting for the frequency dependency. In the RC network, the channel temperature ($T_i$) and ambient temperature ($T_0$) act as two voltage terminals, and the power in the device is provided by the current source [74]. The temperature difference because of SHE, therefore, is

$$T_i - T_0 = \Delta T = R_{\mathrm{TH}}(T)P = R_{\mathrm{TH}}(T)V_{DS}I_D.$$

RTH(T) can be linearly expanded around the ambient temperature $T_0$,

$$R_{TH}(T_i) = R_{TH}(T_0)(1 + \alpha(T_i - T_0))$$

where $R_{TH}$ ($T_0$) is zero power thermal resistance and $\alpha$ is the temperature coefficient.

SHE supresses the current in the transistor and thereby, we will observe a difference in current levels measured between DC ($I_D$) and pulsed measurements, $I_{D0}$. This difference in current can be used to determine device temperature.

The current in a quasi-ballistic transistor, based on a virtual source model [81] is dependent on the injection velocity, $v_{inj}$, and the inversion charge at top of the barrier, $Q_{top}$. The current,$I_D$, is given by

$$I_D = \frac{\lambda}{\lambda + 2\ell} Q_{top} v_{inj}, \tag{4.1}$$

where $\lambda$ is the mean-free-path and l is the critical length.

At high drain voltage, where SHE is prominent, the thermionic flux injected back from drain is suppressed. The inversion charge is, thereby, only dependent on the injected positive flux from the source and the back-scattered negative flux. The observed increase in current during pulsed measurement can be attributed primarily to reduction in back-scattering.

Furthermore, the fractional change in quasi ballistic current is related to fractional change in long-channel mobility ($\mu$) by

$$\frac{\Delta I_D}{I_D} = \frac{\Delta \mu}{\mu}(1 - B)$$

where B is the ballistic figure of merit for the device [82].

In our geometry, $L_{Gate} > \lambda$ , and the ballistic current temperature dependency can be correlated with a temperature dependent mobility. At higher temperatures, the mobility (and hence ballisticity) decreases as an exponential function of temperature,

$$\mu = T^{1/k},$$

where k is the mobility degradation factor with temperature.

To determine the mobility degradation factor, we use the following equation taken from [83]

$$k = \frac{\frac{I_D}{g_m(V_{GS}-V_T)} - 1}{(V_{GS} - V_T)}.$$

The device temperature can thus be estimated from the saturated current by

$$T_i = T_0 \left( \frac{I_{d0}}{I_d} \right)^{1/k}$$

We can, therefore, quantify SHE in our III-V VNW MOSFETs with [75], where $R_{TH}$ ($T_0$) is determined by

$$\frac{1}{\Delta T} = \frac{1}{T_e \left[ \left( \frac{I_{D0}}{I_D} \right)^{1/k} - 1 \right]} = \frac{1}{R_{\mathrm{TH}}(T_0) P} - \alpha.$$

To determine the thermal capacitance, the pulse response to the RC thermal network is evaluated. As it is an exponentially decaying function, the capacitance can be quantified as [75],

$$-\frac{T_{pulse}}{R_{\mathrm{TH}}(T_0)} = C_{\mathrm{TH}} \ln \left\{ 1 - \frac{T_i \left[ \left( \frac{I_{D0}}{I_D} \right)^{1/k} - 1 \right]}{R_{\mathrm{TH}}(T_0) V_{DS} I_D} \right\}$$

## 4.3 SELF-HEATING IN VERTICAL III-V NANOWIRE

The pulsed-IV method is applied to vertical InAs/InGaAs nanowire MOSFET with nanowire diameter of 28 nm to deduce self-heating effects at temperatures of 50 K, 100K and 300 K. The transfer and output characteristics for various pulse widths at 50K are shown in Fig. 4.2 (a) and (b), with the pulsed measurement setup shown in Fig. 4.1. In Fig. 4.3 (a) we observe an increase in current level but no variation in threshold voltage. We can thereby, conclude that the first order effects of oxide charges do not affect the device operation in the pulse width range used. The variations observed is solely due to self-heating. The increase in current level is attributed to mobility variation of the device due to higher channel temperature in DC compared to pulsed voltage input. In Fig. Fig. 4.3 (b), negative output conductance ($g_{ds}$) is seen for DC

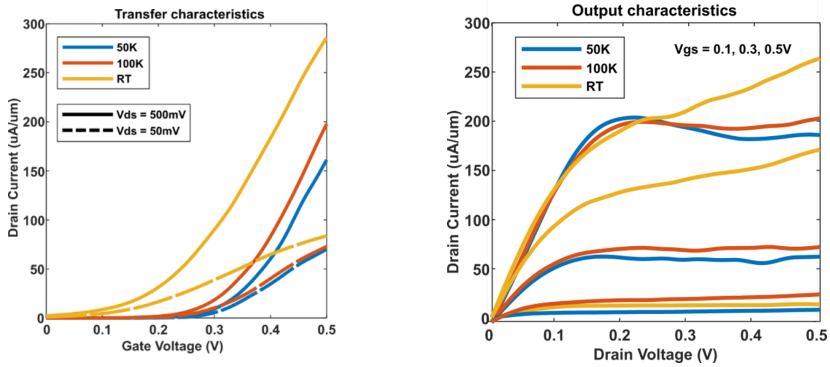


**Figure 4.2:** a) Transfer characteristics b) Output characteristics at temperatures 50K, 100K and 300K for vertical MOSFET. Notice the negative output conductance observed at $V_{DS}$ of 500 mV for temperatures 50 K and 100K, indicating SHE.

measurement, indicating self-heating. $g_{ds}$ varies with pulsed width indicating frequency dependency.

Based on Section 4.2, the thermal coefficient can be deduced from the inverse slope of 1/T vs 1/P plot as shown in **Fig. 4.4 (a)** and (b).

Thermal coefficient for the various ambient temperature is summarised in the table below.

| Temperature (K) | 50 | 100 | 300 | 300 (reverse bias direction) |
|---|---|---|---|---|
| RT(K/$\mu$W) | 2.66 | 4.7 | 34.67 | 5.6 |
| $\alpha(1/L)$ | 0.0024 | 0.0029 | 0.0028 | 0.0074 |

## 4.4 SELF HEATING ANALYSIS AT CRYOGENIC TEMPERATURE

To analyse the SHE effects at cryogenic temperatures, we take an deviation from the current equation 4.1, and

$$I_D = \frac{T}{2-T} Q_{top} v_{inj} \tag{4.2}$$

where

$$T = \frac{\lambda}{l}$$

and T is the transmission probability from the source to the channel.

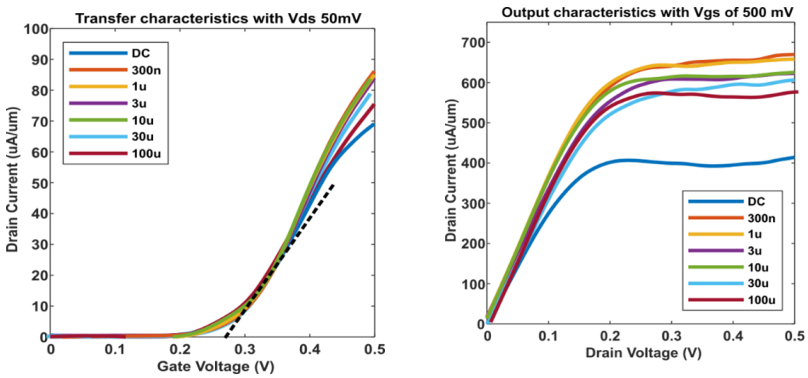


**Figure 4.3:** a) Transfer characteristics and b) output characteristics at temperature 50K and $V_{DS}$ of 500 mV for vertical MOSFET at pulses of 300 ns, 1$\mu$s, 3$\mu$s, 10$\mu$s, 30$\mu$s and 100$\mu$s along with DC for comparison. No shift in threshold voltage is observed and negative output conductance progressively goes down as pulse period decreases.

T can also be determined from the ratio of injection velocity to maximum injection velocity feasible.

$$T = \frac{V_{inj}}{V_{inj,max}}$$

At cryogenic temperature, the density of states for DC and pulsed measurements will be the same as the injection of the carriers from other subbands due to thermal freeze out. We can, thereby, assume $Q_{top}$ to be the same for both.

$V_{inj,max}$ is determined from

$$v_{inj,max} = v_t \frac{F_0(\eta_F)}{F_{-\frac{1}{2}}(\eta_F)}$$

where vt is the thermal velocity, $F_n$ is nth order Fermi-Dirac integral. Using this formula, $v_{inj,max}$ = $8.5 \times 10^7$ cm/s can be derived from 1-D single subband model with EOT = 1.5 nm and m*=0.031 me (based on non-parabolic band structure approximation).

We fit the DC and pulsed data to determine the $V_{inj}$ velocity. Fig. 4.5 shows the DC and pulsed data fitted, to extract the $V_{inj}$ velocity at 15 K.

The derived injection velocity is shown in the table below 4.1.

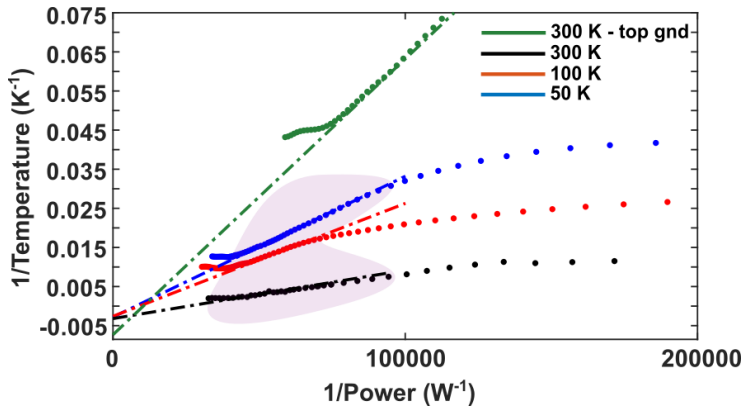


**Figure 4.4:** 1/T vs 1/P with ambient temperature of 50K, 100K and 300K.

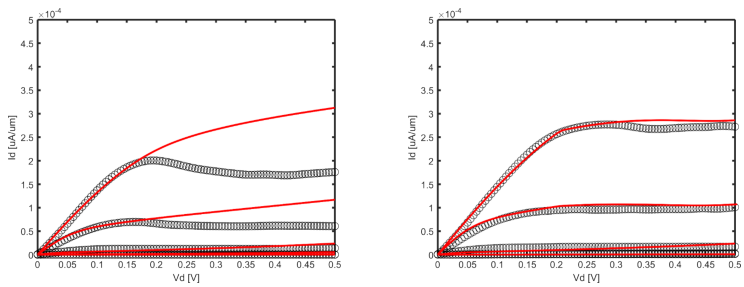


**Figure 4.5:** a) DC measurements b) Pulsed measurements at 300 ns at 15 K. The data is fitted using Virtual Source Model.

**Table 4.1:** Injection velocity for DC and pulsed measurements based on Virtual Source Model

| T(K) | $V_{inj,DC}$ (* $10^7$ cm/s) | $V_{inj,pulsed}$ (* $10^7$ cm/s) |
|---|---|---|
| 15 | 0.33 | 0.504629 |
| 50 | 0.612 | 0.92824 |
| 100 | 0.866 | 1.309699 |
| 300 | 1.5 | 2.494323 |

The measured drain current change versus low temperature and high temperature respectively is given by $\Delta I_D$. The change in current can be written as

$$\Delta I_D / I_D = \alpha(T - 300) \tag{4.3}$$

Differentiating Eq. 4.2 and substituting Eq. 4.3 in it, we obtain

$$\alpha = \frac{\left(\frac{1}{2} - \frac{4}{2+\frac{\lambda}{l}}\right)}{300} - \frac{\eta}{V_{ov}}$$

where $\eta$ is the shift in threshold voltage.

Based on the above equations and fitting it to the virtual source model, we obtain the thermal coefficient for various temperatures are, below.

**Table 4.2:** Thermal coefficient values

| T (K) | Alpha ($K^{-1}$) |
|---|---|
| 15 | 0.0016417 |
| 50 | 0.002435 |
| 100 | 0.002358 |
| 300 | 0.002638 |

A good fit between pulsed measurement based SHE and virtual source model fit values are found.

# 5

# Final words and Outlook

In this thesis, the prospect of III-V vertical nanowire TFETs on Si for low-power applications have been investigated. During the years, we evaluated several structures on the vertical nanowire TFETs, including but not limited to heterostructure engineering, non-organic spacers, mesa and field-plate structure, to improve the device performance. These improvements led to good performance improvements in the TFET device metrics. We have reported $I_{ON}$ of 42 $\mu$A/$\mu$m, transconductance of 205 $\mu$S/$\mu$m and SS of 40 mV/dec (at $V_{DS}$ = 500 mV for $I_{OFF}$ of 1 nA/$\mu$m). Furthermore, we report $I_{60}$ of 1.2 $\mu$A/$\mu$m, which is the highest reported value for a TFET. Realising the threshold of $I_{60} > 1\mu$A/$\mu$m at $V_{GS} < 0.1$ V, was a very important step. We can now confidently say TFETs are superior to MOSFETs for low-power applications.
This, also, created a good platform to explore TFET circuit capabilities. TFETs are a versatile device, which exhibits NDR, diode, transistor characteristics depending on it's biasing conditions. In order to better comprehend it's potential, we explored low-power design in voltage-mode configurations. TFETs were able to mirror currents at nA range, show inverter, buffer and differential operation. The frequency of operation was 200 kHz. Utilizing translinearity between transconductance and drain current demonstrated by the TFET, low power current-mode based analog IC design was explored. We have implemented a current conveyor circuit, which exhibits large-signal voltage gain of 0.89 mV/mV, current gain of 1nA/nA and an operating frequency of 320 kHz. TFETs were more robust to temperature and influences of drain voltages in comparison to conventional MOSFETs.

In a step to understand the challenges in heterogeneous integration, the effects of self-heating for a nanowire transistor was studied. Using pulsed IV measurements, the thermal impedences of the transistors were analysed. The

results indicate that the intrinsic temperature rises to 385 K when the device is operated in DC at room temperature (300 K) with a thermal time constant of 1 µs. We find that self-heating is a limiting factor for device performance and a major challenge that needs to be addressed.

# Bibliography


[1] S. Salahuddin, K. Ni, and S. Datta, "The era of hyper-scaling in electronics," *Nature Electronics*, vol. 1, no. 8, pp. 442–450, 2018.

[2] G. Fagas, J. P. Gallagher, L. Gammaitoni, and D. J. Paul, "Energy challenges for ict," in *ICT - Energy Concepts for Energy Efficiency and Sustainability*, G. Fagas, L. Gammaitoni, J. P. Gallagher, and D. J. Paul, Eds. Rijeka: IntechOpen, 2017, ch. 1. [Online]. Available: https://doi.org/10.5772/66678

[3] S. Salahuddin and S. Datta, "Can the subthreshold swing in a classical fet be lowered below 60 mv/decade?" in *2008 IEEE International Electron Devices Meeting*. IEEE, 2008, pp. 1–4.

[4] M. S. Kim, X. Li, H. Liu, J. Sampson, S. Datta, and V. Narayanan, "Exploration of low-power high-sfdr current-steering d/a converter design using steep-slope heterojunction tunnel fets," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 6, pp. 2299–2309, 2015. doi: doi: 10.1109/TVLSI.2015.2500160

[5] B. Sedighi, X. S. Hu, H. Liu, J. J. Nahas, and M. Niemier, "Analog circuit design using tunnel-fets," *IEEE transactions on circuits and systems I: regular papers*, vol. 62, no. 1, pp. 39–48, 2014. doi: 10.1109/TCSI.2014.2342371

[6] Q. Zhang, Y. Lu, C. A. Richter, D. Jena, and A. Seabaugh, "Optimum bandgap and supply voltage in tunnel fets," *IEEE Transactions on Electron Devices*, vol. 61, no. 8, pp. 2719–2724, 2014.

[7] H. Liu, X. Li, R. Vaddi, K. Ma, S. Datta, and V. Narayanan, "Tunnel fet rf rectifier design for energy harvesting applications," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 4, no. 4, pp. 400–411, 2014. doi: 10.1109/JETCAS.2014.2361068

[8] F. Settino, M. Lanuzza, S. Strangio, F. Crupi, P. Palestri, D. Esseni, and L. Selmi, "Understanding the potential and limitations of tunnel fets for low-voltage analog/mixed-signal circuits," *IEEE Transactions on Electron Devices*, vol. 64, no. 6, pp. 2736–2743, 2017. doi: 10.1109/TED.2017.2689746

[9] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *nature*, vol. 479, no. 7373, pp. 329–337, 2011.

[10] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond cmos logic," *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2095–2110, 2010.

[11] U. E. Avci, D. H. Morris, and I. A. Young, "Tunnel field-effect transistors: Prospects and challenges," *IEEE Journal of the Electron Devices Society*, vol. 3, no. 3, pp. 88–95, 2015.

[12] S. Datta, *Electronic transport in mesoscopic systems*. Cambridge university press, 1997.

[13] E. Kane, "Zener tunneling in semiconductors," *Journal of Physics and Chemistry of Solids*, vol. 12, no. 2, pp. 181–188, 1960.

[14] Y. Taur, J. Wu, and J. Min, "An analytic model for heterojunction tunnel fets with exponential barrier," *IEEE Transactions on Electron Devices*, vol. 62, no. 5, pp. 1399–1404, 2015.

[15] E. Lind, "High frequency iiiâ€"v nanowire mosfets," *Semiconductor Science and Technology*, vol. 31, no. 9, p. 093005, aug 2016. doi: 10.1088/0268-1242/31/9/093005. [Online]. Available: https://dx.doi.org/10.1088/0268-1242/31/9/093005

[16] J. Appenzeller, J. Knoch, M. T. Bjork, H. Riel, H. Schmid, and W. Riess, "Toward nanowire electronics," *IEEE Transactions on electron devices*, vol. 55, no. 11, pp. 2827–2845, 2008.

[17] A. Krishnaraja, J. Svensson, E. Lind, and L.-E. Wernersson, "Reducing ambipolar off-state leakage currents in III-V vertical nanowire tunnel FETs using gate-drain underlap," *Applied Physics Letters*, vol. 115, no. 14, p. 143505, 10 2019. doi: 10.1063/1.5115296. [Online]. Available: https://doi.org/10.1063/1.5115296

[18] A. Krishnaraja, J. Svensson, and L.-E. Wernersson, "Vertical inas/ingaassb/gasb nanowire tunnel fets on si with drain field-plate and eot = 1 nm achieving smin = 32 mv/dec and gm/id = 100 v-1," in *2020 IEEE Silicon Nanoelectronics Workshop (SNW)*, 2020. doi: 10.1109/SNW50361.2020.9131656 pp. 17–18.

[19] E. Memisevic, M. Hellenbrand, E. Lind, A. R. Persson, S. Sant, A. Schenk, J. Svensson, R. Wallenberg, and L.-E. Wernersson, "Individual defects in inas/ingaassb/gasb nanowire tunnel field-effect transistors operating below 60 mv/decade," *Nano Letters*, vol. 17, no. 7, pp. 4373–4380, 2017. doi: 10.1021/acs.nanolett.7b01455 PMID: 28613894. [Online]. Available: https://doi.org/10.1021/acs.nanolett.7b01455

[20] A. Seabaugh and R. Lake, *Tunnel Diodes*. John Wiley Sons, Ltd, 2003. ISBN 9783527600434. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/3527600434.eap541

[21] P. Thomas, M. Filmer, A. Gaur, D. J. Pawlik, B. Romanczyk, E. Marini, S. L. Rommel, K. Majumdar, W.-Y. Loh, M. H. Wong, C. Hobbs, K. Bhatnagar, R. Contreras-Guerrero, and R. Droopad, "Performance evaluation of in0.53ga0.47as esaki tunnel diodes on silicon and inp substrates," *IEEE Transactions on Electron Devices*, vol. 62, no. 8, pp. 2450–2456, 2015. doi: 10.1109/TED.2015.2445731

[22] R. Dennard, F. Gaensslen, H.-N. Yu, V. Rideout, E. Bassous, and A. LeBlanc, "Design of ion-implanted mosfet's with very small physical dimensions," *IEEE Journal of Solid-State Circuits*, vol. 9, no. 5, pp. 256–268, 1974. doi: 10.1109/JSSC.1974.1050511

[23] K. Mistry, M. Armstrong, C. Auth, S. Cea, T. Coan, T. Ghani, T. Hoffmann, A. Murthy, J. Sandford, R. Shaheed *et al.*, "Delaying forever: Uniaxial strained silicon transistors in a 90nm cmos technology," in *Digest of Technical Papers. 2004 Symposium on VLSI Technology, 2004.* IEEE, 2004, pp. 50–51.

[24] S. Datta, G. Dewey, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, R. Kotlyar, M. Metz, N. Zelick, and R. Chau, "High mobility si/sige strained channel mos transistors with hfo/sub 2//tin gate stack," in *IEEE International Electron Devices Meeting 2003*. IEEE, 2003, pp. 28–1.

[25] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-/spl kappa//metal-gate stack and its mosfet characteristics," *IEEE Electron Device Letters*, vol. 25, no. 6, pp. 408–410, 2004.

[26] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau *et al.*, "A 45nm logic technology with high-k+ metal gate transistors, strained silicon, 9 cu interconnect layers, 193nm dry patterning, and 100% pb-free packaging," in *2007 IEEE International Electron Devices Meeting*. IEEE, 2007, pp. 247–250.

[27] K. Henson, H. Bu, M. Na, Y. Liang, U. Kwon, S. Krishnan, J. Schaeffer, R. Jha, N. Moumen, R. Carter *et al.*, "Gate length scaling and high drive currents enabled for high performance soi technology using high-$\kappa$/metal gate," in *2008 IEEE International Electron Devices Meeting*. IEEE, 2008, pp. 1–4.

[28] N. Loubet, T. Hook, P. Montanini, C.-W. Yeung, S. Kanakasabapathy, M. Guillom, T. Yamashita, J. Zhang, X. Miao, J. Wang, A. Young, R. Chao, M. Kang, Z. Liu, S. Fan, B. Hamieh, S. Sieg, Y. Mignot, W. Xu, S.-C. Seo, J. Yoo, S. Mochizuki, M. Sankarapandian, O. Kwon, A. Carr, A. Greene, Y. Park, J. Frougier, R. Galatage, R. Bao, J. Shearer, R. Conti, H. Song, D. Lee, D. Kong, Y. Xu, A. Arceo, Z. Bi, P. Xu, R. Muthinti, J. Li, R. Wong, D. Brown, P. Oldiges, R. Robison, J. Arnold, N. Felix, S. Skordas, J. Gaudiello, T. Standaert, H. Jagannathan, D. Corliss, M.-H. Na, A. Knorr, T. Wu, D. Gupta, S. Lian, R. Divakaruni, T. Gow, C. Labelle, S. Lee, V. Paruchuri, H. Bu, and M. Khare, "Stacked nanosheet gate-all-around transistor to enable scaling beyond finfet," in *2017 Symposium on VLSI Technology*, 2017. doi: 10.23919/VLSIT.2017.7998183 pp. T230–T231.

[29] S.-W. Chang, P.-J. Sung, T.-Y. Chu, D. D. Lu, C.-J. Wang, N.-C. Lin, C.-J. Su, S.-H. Lo, H.-F. Huang, J.-H. Li, M.-K. Huang, Y.-C. Huang, S.-T. Huang, H.-C. Wang, Y.-J. Huang, J.-Y. Wang, L. W. Yu, Y.-F. Huang, F. K. Hsueh, C.-T. Wu, W. C.-Y. Ma, K.-H. Kao, Y. J. Lee, C.-L. Lin, R. W. Chuang, K.-P. Huang, S. Samukawa, Y. Li, W. H. Lee, T.-S. Chao, G. W. Huang, W.-F. Wu, J. Y. Li, J.-M. Shieh, W. K. Yeh, and Y.-H. Wang, "First demonstration of cmos inverter and 6t-sram based on gaa cfets structure for 3d-ic applications," in *2019 IEEE International Electron Devices Meeting (IEDM)*, 2019. doi: 10.1109/IEDM19573.2019.8993525 pp. 11.7.1–11.7.4.

[30] H. Jagannathan, B. Anderson, C.-W. Sohn, G. Tsutsui, J. Strane, R. Xie, S. Fan, K.-I. Kim, S. Song, S. Sieg, I. Seshadri, S. Mochizuki, J. Wang, A. Rahman, K.-Y. Cheon, I. Hwang, J. Demarest, J. Do, J. Fullam, G. Jo, B. Hong, Y. Jung, M. Kim, S. Kim, R. Lallement, T. Levin, J. Li, E. Miller, P. Montanini, R. Pujari, C. Osborn, M. Sankarapandian, G.-H. Son, C. Waskiewicz, H. Wu, J. Yim, A. Young, C. Zhang, A. Varghese, R. Robison, S. Burns, K. Zhao, T. Yamashita, D. Dechene, D. Guo, R. Divakaruni, T. Wu, K.-I. Seo, and H. Bu, "Vertical-transport nanosheet technology for cmos scaling beyond lateral-transport devices," in *2021 IEEE International Electron Devices Meeting (IEDM)*, 2021. doi: 10.1109/IEDM19574.2021.9720561 pp. 26.1.1–26.1.4.

[31] K. Tomioka, M. Yoshimura, and T. Fukui, "A iiiâ€"v nanowire channel on silicon for high-performance vertical transistors," *Nature*, vol. 488, no. 7410, pp. 189–192, Aug 2012. doi: 10.1038/nature11293. [Online]. Available: https://doi.org/10.1038/nature11293

[32] L. Wang, J. Jie, Z. Shao, Q. Zhang, X. Zhang, Y. Wang, Z. Sun, and S.-T. Lee, "Mos2/si heterojunction with vertically standing layered structure for ultrafast, high-detectivity, self-driven visibleâ€"near infrared photodetectors," *Advanced Functional Materials*, vol. 25, no. 19, pp. 2910–2919, 2015. doi: https://doi.org/10.1002/adfm.201500216. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/adfm.201500216

[33] A. Alian, Y. Mols, C. C. M. Bordallo, D. Verreck, A. Verhulst, A. Vandooren, R. Rooyackers, P. G. D. Agopian, J. A. Martino, A. Thean, D. Lin, D. Mocuta, and N. Collaert, "InGaAs tunnel FET with sub-nanometer EOT and sub-60mV/dec sub-threshold swing at room temperature," *Applied Physics Letters*, vol. 109, no. 24, p. 243502, 12 2016. doi: 10.1063/1.4971830. [Online]. Available: https://doi.org/10.1063/1.4971830

[34] D. H. Ahn, S. Ji, M. Takenaka, and S. Takagi, "Performance improvement of inxga1xas tunnel fets with quantum well and eot scaling," in *2016 IEEE Symposium on VLSI Technology*, 2016. doi: 10.1109/VLSIT.2016.7573443 pp. 1–2.

[35] G. Dewey, B. Chu-Kung, J. Boardman, J. M. Fastenau, J. Kavalieros, R. Kotlyar, W. K. Liu, D. Lubyshev, M. Metz, N. Mukherjee, P. Oakey, R. Pillarisetty, M. Radosavljevic, H. W. Then, and R. Chau, "Fabrication, characterization, and physics of iii–v heterojunction tunneling field effect transistors (h-tfet) for steep sub-threshold swing," in *2011 International Electron Devices Meeting*, 2011. doi: 10.1109/IEDM.2011.6131666 pp. 33.6.1–33.6.4.

[36] X. Zhao, A. Vardi, and J. A. del Alamo, "Sub-thermal subthreshold characteristics in top–down ingaas/inas heterojunction vertical nanowire tunnel fets," *IEEE Electron Device Letters*, vol. 38, no. 7, pp. 855–858, 2017. doi: 10.1109/LED.2017.2702612

[37] D. Cutaia, K. E. Moselund, H. Schmid, M. Borg, A. Olziersky, and H. Riel, "Complementary iii–v heterojunction lateral nw tunnel fet technology on si," in *2016 IEEE Symposium on VlSI Technology*. IEEE, 2016, pp. 1–2.

[38] K. Tomioka, M. Yoshimura, and T. Fukui, "Steep-slope tunnel field-effect transistors using iii–v nanowire/si heterojunction," in *2012 symposium on VLSI technology (VLSIT)*. IEEE, 2012, pp. 47–48.

[39] E. Memisevic, J. Svensson, E. Lind, and L.-E. Wernersson, "Vertical nanowire tfets with channel diameter down to 10 nm and point smin of 35 mv/decade," *IEEE Electron Device Letters*, vol. 39, no. 7, pp. 1089–1091, 2018. doi: 10.1109/LED.2018.2836862

[40] T. Roy, M. Tosun, X. Cao, H. Fang, D.-H. Lien, P. Zhao, Y.-Z. Chen, Y.-L. Chueh, J. Guo, and A. Javey, "Dual-gated mos2/wse2 van der waals tunnel diodes and transistors," *ACS nano*, vol. 9, no. 2, pp. 2071–2079, 2015.

[41] D. Sarkar, X. Xie, W. Liu, W. Cao, J. Kang, Y. Gong, S. Kraemer, P. M. Ajayan, and K. Banerjee, "A subthermionic tunnel field-effect transistor with an atomically thin channel," *Nature*, vol. 526, no. 7571, pp. 91–95, 2015.

[42] S. Kim, G. Myeong, W. Shin, H. Lim, B. Kim, T. Jin, S. Chang, K. Watanabe, T. Taniguchi, and S. Cho, "Thickness-controlled black phosphorus tunnel field-effect transistor for low-power switches," *Nature nanotechnology*, vol. 15, no. 3, pp. 203–206, 2020.

[43] E. Memisevic, J. Svensson, E. Lind, and L.-E. Wernersson, "Inas/ingaassb/gasb nanowire tunnel field-effect transistors," *IEEE Transactions on Electron Devices*, vol. 64, no. 11, pp. 4746–4751, 2017. doi: 10.1109/TED.2017.2750763

[44] L.-E. W. A. S. S. Sant, E. Memisevic, "Impact of non-idealities on the performance of inas/(in)gaassb/gasb tunnel fets," *Nanoelectronic Devices*, vol. 1, no. Tunnel FETs, 2018. doi: 10.21494/ISTE.OP.2018.0221

[45] B. Romanczyk, P. Thomas, D. Pawlik, S. L. Rommel, W.-Y. Loh, M. H. Wong, K. Majumdar, W.-E. Wang, and P. D. Kirsch, "Benchmarking current density in staggered gap In0.53Ga0.47As/GaAs0.5Sb0.5 heterojunction Esaki tunnel diodes," *Applied Physics Letters*, vol. 102, no. 21, p. 213504, 05 2013. doi: 10.1063/1.4808362. [Online]. Available: https://doi.org/10.1063/1.4808362

[46] W. Cao, D. Sarkar, Y. Khatami, J. Kang, and K. Banerjee, "Subthreshold-swing physics of tunnel field-effect transistors," *AIP Advances*, vol. 4, no. 6, p. 067141, 06 2014. doi: 10.1063/1.4881979. [Online]. Available: https://doi.org/10.1063/1.4881979

[47] R. G. Hobbs, N. Petkov, and J. D. Holmes, "Semiconductor nanowire fabrication by bottom-up and top-down paradigms," *Chemistry of materials*, vol. 24, no. 11, pp. 1975–1991, 2012.

[48] K. A. Dick, "A review of nanowire growth promoted by alloys and non-alloying elements with emphasis on au-assisted iii–v nanowires," *Progress in Crystal Growth and Characterization of Materials*, vol. 54, no. 3-4, pp. 138–173, 2008.

[49] R. Yu, S. Das, R. Hobbs, Y. Georgiev, I. Ferain, P. Razavi, N. D. Akhavan, C. A. Colinge, and J.-P. Colinge, "Top-down process of germanium nanowires using ebl exposure of hydrogen silsesquioxane resist," in *2012 13th International Conference on Ultimate Integration on Silicon (ULIS)*. IEEE, 2012, pp. 145–148.

[50] S. G. Ghalamestani, S. Johansson, B. M. Borg, E. Lind, K. A. Dick, and L.-E. Wernersson, "Uniform and position-controlled inas nanowires on 2 si substrates for transistor applications," *Nanotechnology*, vol. 23, no. 1, p. 015302, 2011.

[51] E. Memisevic, J. Svensson, E. Lind, and L.-E. Wernersson, "Inas/ingaassb/gasb nanowire tunnel field-effect transistors," *IEEE Transactions on Electron Devices*, vol. 64, no. 11, pp. 4746–4751, 2017. doi: 10.1109/TED.2017.2750763

[52] E. Memišević, J. Svensson, M. Hellenbrand, E. Lind, and L.-E. Wernersson, "Scaling of vertical inas–gasb nanowire tunneling field-effect transistors on si," *IEEE Electron Device Letters*, vol. 37, no. 5, pp. 549–552, 2016. doi: 10.1109/LED.2016.2545861

[53] J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube field-effect transistors," *Physical review letters*, vol. 93, no. 19, p. 196805, 2004.

[54] L. Knoll, Q.-T. Zhao, A. Nichau, S. Trellenkamp, S. Richter, A. Schäfer, D. Esseni, L. Selmi, K. K. Bourdelle, and S. Mantl, "Inverters with strained si nanowire complementary tunnel field-effect transistors," *IEEE Electron Device Letters*, vol. 34, no. 6, pp. 813–815, 2013. doi: 10.1109/LED.2013.2258652

[55] G. Zhou, Y. Lu, R. Li, Q. Zhang, Q. Liu, T. Vasen, H. Zhu, J.-M. Kuo, T. Kosel, M. Wistey, P. Fay, A. Seabaugh, and H. Xing, "Ingaas/inp tunnel fets with a subthreshold swing of 93 mv/dec and $i_{on}/i_{off}$ ratio near $10^6$," *IEEE Electron Device Letters*, vol. 33, no. 6, pp. 782–784, 2012. doi: 10.1109/LED.2012.2189546

[56] K. E. Moselund, H. Schmid, C. Bessire, M. T. Bjork, H. Ghoneim, and H. Riel, "Inas–si nanowire heterojunction tunnel fets," *IEEE Electron Device Letters*, vol. 33, no. 10, pp. 1453–1455, 2012. doi: 10.1109/LED.2012.2206789

[57] K. Nishi, M. Yokoyama, S. Kim, H. Yokoyama, M. Takenaka, and S. Takagi, "Study on electrical properties of metal/GaSb junctions using metal-GaSb alloys," *Journal of Applied Physics*, vol. 115, no. 3, p. 034515, 01 2014. doi: 10.1063/1.4862486. [Online]. Available: https://doi.org/10.1063/1.4862486

[58] J. Knoch and J. Appenzeller, "Modeling of high-performance p-type iii–v heterojunction tunnel fets," *IEEE Electron Device Letters*, vol. 31, no. 4, pp. 305–307, 2010. doi: 10.1109/LED.2010.2041180

[59] J. Min, J. Wu, and Y. Taur, "Analysis of source doping effect in tunnel fets with staggered bandgap," *IEEE Electron Device Letters*, vol. 36, no. 10, pp. 1094–1096, 2015. doi: 10.1109/LED.2015.2466676

[60] E. Memisevic, J. Svensson, E. Lind, and L.-E. Wernersson, "Impact of source doping on the performance of vertical inas/ingaassb/gasb nanowire tunneling field-effect transistors," *Nanotechnology*, vol. 29, no. 43, p. 435201, aug 2018. doi: 10.1088/1361-6528/aad949. [Online]. Available: https://dx.doi.org/10.1088/1361-6528/aad949

[61] M. Noguchi, S. Kim, M. Yokoyama, O. Ichikawa, T. Osada, M. Hata, M. Takenaka, and S. Takagi, "High ion/ioff and low subthreshold slope planar-type ingaas tunnel field effect transistors with zn-diffused source junctions," *Journal of Applied Physics*, vol. 118, no. 4, 2015.

[62] A. Alian, Y. Mols, C. Bordallo, D. Verreck, A. Verhulst, A. Vandooren, R. Rooyackers, P. Agopian, J. Martino, A. Thean *et al.*, "Ingaas tunnel fet with sub-nanometer eot and sub-60 mv/dec sub-threshold swing at room temperature," *Applied Physics Letters*, vol. 109, no. 24, 2016.

[63] C. Convertino, C. B. Zota, H. Schmid, D. Caimi, L. Czornomaz, A. M. Ionescu, and K. E. Moselund, "A hybrid iii–v tunnel fet and mosfet technology platform integrated on silicon," *nature electronics*, vol. 4, no. 2, pp. 162–170, 2021. doi: https://doi.org/10.1038/s41928-020-00531-3

[64] W. G. Vandenberghe, A. S. Verhulst, B. Sorée, W. Magnus, G. Groeseneken, Q. Smets, M. Heyns, and M. V. Fischetti, "Figure of merit for and identification of sub-60 mv/decade devices," *Applied Physics Letters*, vol. 102, no. 1, p. 013510, 2013. doi: https://doi.org/10.1063/1.4773521

[65] E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind, and L.-E. Wernersson, "Vertical inas/gaassb/gasb tunneling field-effect transistor on si with s = 48 mv/decade and ion = 10 $\mu$a/$\mu$m for ioff = 1 na/$\mu$m at vds = 0.3 v," in *2016 IEEE International Electron Devices Meeting (IEDM)*, 2016. doi: 10.1109/IEDM.2016.7838450 pp. 19.1.1–19.1.4.

[66] A. Krishnaraja, J. Svensson, E. Memisevic, Z. Zhu, A. R. Persson, E. Lind, L. R. Wallenberg, and L.-E. Wernersson, "Tuning of source material for inas/ingaassb/gasb application-specific vertical nanowire tunnel fets," *ACS Applied Electronic Materials*, vol. 2, no. 9, pp. 2882–2887, 2020. doi: https://doi.org/10.1021/acsaelm.0c00521

[67] L. Barboni, M. Siniscalchi, and B. Sensale-Rodriguez, "Tfet-based circuit design using the transconductance generation efficiency $g_m/I_d$ method," *IEEE Journal of the Electron Devices Society*, vol. 3, no. 3, pp. 208–216, 2015. doi: 10.1109/JEDS.2015.2412118

[68] N. Gupta, A. Makosiej, C. Anghel, A. Amara, and A. Vladimirescu, "Cmos sensor nodes with sub-picowatt tfet memory," *IEEE Sensors Journal*, vol. 16, no. 23, pp. 8255–8262, 2016. doi: 10.1109/JSEN.2016.2588280

[69] B. Gilbert, "Translinear circuits: A proposed classification," *Electronics letters*, vol. 1, no. 11, pp. 14–16, 1975.

[70] A. Sedra, G. W. Roberts, and F. Gohh, "The current conveyor: history, progress and new results," *IEE Proceedings G (Circuits, Devices and Systems)*, vol. 137, no. 2, pp. 78–87(9), April 1990. doi: 1010.1049/ip-g-2.1990.0015

[71] A. Sedra, "The current conveyor: history, progress and new results," *IEE Proceedings G (Circuits, Devices and Systems)*, vol. 137, pp. 78–87(9), April 1990. [Online]. Available: https://digital-library.theiet.org/content/journals/10.1049/ip-g-2.1990.0015

[72] R. Narang, M. Saxena, R. S. Gupta, and M. Gupta, "Impact of temperature variations on the device and circuit performance of tunnel fet: A simulation study," *IEEE Transactions on Nanotechnology*, vol. 12, no. 6, pp. 951–957, 2013. doi: 10.1109/TNANO.2013.2276401

[73] S. Migita, K. Fukuda, Y. Morita, and H. Ota, "Experimental demonstration of temperature stability of si-tunnel fet over si-mosfet," in *2012 IEEE Silicon Nanoelectronics Workshop (SNW)*. IEEE, 2012. doi: 10.1109/SNW.2012.6243315 pp. 1–2.

[74] K. Jenkins, J.-C. Sun, and J. Gautier, "Characteristics of soi fet's under pulsed conditions," *IEEE Transactions on Electron Devices*, vol. 44, no. 11, pp. 1923–1930, 1997. doi: 10.1109/16.641362

[75] C. Anghel, R. Gillon, and A. Ionescu, "Self-heating characterization and extraction method for thermal resistance and capacitance in hv mosfets," *IEEE Electron Device Letters*, vol. 25, no. 3, pp. 141–143, 2004. doi: 10.1109/LED.2003.821669

[76] D. Yakimets, G. Eneman, P. Schuddinck, T. H. Bao, M. G. Bardon, P. Raghavan, A. Veloso, N. Collaert, A. Mercha, D. Verkest, A. V.-Y. Thean, and K. De Meyer, "Vertical gaafets for the ultimate cmos scaling," *IEEE Transactions on Electron Devices*, vol. 62, no. 5, pp. 1433–1439, 2015. doi: 10.1109/TED.2015.2414924

[77] E. Lind, "High frequency iii–v nanowire mosfets," *Semiconductor Science and Technology*, vol. 31, no. 9, p. 093005, aug 2016. doi: 10.1088/0268-1242/31/9/093005

[78] B. Yu, L. Wang, Y. Yuan, P. M. Asbeck, and Y. Taur, "Scaling of nanowire transistors," *IEEE Transactions on Electron Devices*, vol. 55, no. 11, pp. 2846–2858, 2008. doi: 10.1109/TED.2008.2005163

[79] H. A. Nilsson, P. Caroff, C. Thelander, E. Lind, O. Karlström, and L.-E. Wernersson, "Temperature dependent properties of insb and inas nanowire field-effect transistors," *Applied Physics Letters*, vol. 96, no. 15, p. 153505, 2010. doi: 10.1063/1.3402760

[80] B. Cardoso Paz, M. Cassé, C. Theodorou, G. Ghibaudo, T. Kammler, L. Pirro, M. Vinet, S. de Franceschi, T. Meunier, and F. Gaillard, "Performance and low-frequency noise of 22-nm fdsoi down to 4.2 k for cryogenic applications," *IEEE Transactions on Electron Devices*, vol. 67, no. 11, pp. 4563–4567, 2020. doi: 10.1109/TED.2020.3021999

[81] M. Lundstrom, "Elementary scattering theory of the si mosfet," *IEEE Electron Device Letters*, vol. 18, no. 7, pp. 361–363, 1997. doi: 10.1109/55.596937

[82] ——, "On the mobility versus drain current relation for a nanoscale mosfet," *IEEE Electron Device Letters*, vol. 22, no. 6, pp. 293–295, 2001. doi: 10.1109/55.924846

[83] G. Ghibaudo, "New method for the extraction of mosfet parameters," *Electronics Letters*, vol. 24, no. 9, pp. 543–545, 1988. doi: 10.1049/el:19880369

# APPENDICES

# A

# Fabrication Steps of Vertical Nanowire Transistors

In this section the recipe used to fabricate TFETs in Papers I-IV will be presented.

## 1. SAMPLE CLEANING BEFORE NANOWIRE GROWTH

- The 4-inch Au-patterned wafer from Chalmers is protected with photoresist before dicing it into 1 $cm^2$ sample dies which must then be cleaned before nanowire growth.
- Clean the sample in acetone at 50 °C for 15 min.
- Transfer the sample to a beaker with fresh acetone and place in ultrasonic power bath for 10 min.
- Remove resist by rinsing in 40 °C acetone for 3 mins followed by IPA.
- Clean the sample using $O_2$ plasma ashing in Plasma Preen with metal cage for 15 s at 5 mbar.

## 2. GROWTH OF THE NANOWIRES

- The nanowires were grown using vapour-liquid-solid growth method by using gold as the seed particle. All growth was performed using metal organic vapor epitaxy (MOVPE) with following precursors: trimethylindium (TMIn), arsine (AsH3), trimethylgallium (TMGa), and trimethylantimony (TMSb). Doping was added to the source and drain regions using precursors: triethyltin (TESn) and diethylzinc (DEZn). The nanowire growth were done by Dr. Johannes Svensson and Dr.

Zhongyunshen Zhu.

3. **MASK**

- 4"x4" UV mask in soda lime with Chromium down was used for this work. GDSII file of used masks were Mask_TFET.gds, Mask_TFET_Ckt_V1.gds and Mask_TFET_Ckt_V2.gds.

4. **DIGITAL ETCHING**

- Inspect the grown nanowires in the SEM.
- To etch the InAs segment of the nanowire -
  a) Oxidize the nanowire using $O_3$ at 50 °Cfor 5 min.
  b) Wet-etch the sample in citric acid for 30 s.
  c) Rinse in DI water for 30 s.
  d) Rinse in IPA for 30 s.
  e) Monitor the thickness of the nanowire in SEM between the etch-cycles.

5. **GATE OXIDE AND BOTTOM SPACER DEPOSITION**

- Load the sample into the ALD Savannah immediately after the last digital etch cycle.
- Surface cleaning using 5 cycles TMAl.
- Deposit 5 cycles of $Al_2O_3$ at 300 °C.
- Deposit 27 cycles of $HfO_2$ at 120 °C.
- Deposit 300 cycles of $Al_2O_3$ at 100 °C.
- Monitor in SEM to confirm deposition thickness.

6. **BOTTOM SPACER DEFINITION**

- Pre-bake the sample in a hotplate at 120 °C for 2 mins.
- Spin coat the sample with S1813 photoresist at 60 s, 4000 rpm.
- Hard-bake the resist on a hotplate at 120 °C for 15 min.
- Etch S1813 in RIE-Trion using $O_2$ plasma at 15 sccm, 300 mTorr and 50 W to the desired length of the spacer. Etch rate is roughly 0.65 nm/s and varies depending on chamber conditions, previous etch recipe and material.
- Monitor in SEM at constant intervals for the desired length.
- Wet-etch $Al_2O_3$ in HF 1:400 for 25 s.

- Remove resist by rinsing in 40 °C acetone for 3 mins followed by IPA.

7. **BOTTOM GATE FORMATION**

- Sputter 30 nm W in AJA Orion at 16 sccm Ar-flow and 100 W DC power with rotation.
- Gate length definition:
  a) Pre-bake the sample in a hotplate at 120 °C for 2 mins.
  b) Spin coat the sample with S1813 photoresist at 60 s, 4000 rpm.
  c) Hard-bake the resist on a hotplate at 120 °C for 15 min.
  d) Etch S1813 in RIE-Trion using $O_2$ plasma at 15 sccm, 300 mTorr and 50 W to the desired length of the spacer. Monitor in SEM at constant intervals for the desired length.
  e) Etch W in RIE-Trion using $SF_6$:Ar at 45/25 sccm, 140 W and 185 mTorr for 45 s.
  f) Remove etch residues in Plasma Preen using $O_2$ plasma ashing for 45 s.
  g) Remove resist by rinsing in acetone followed by IPA.
- Gate pad definition:
  a) Pre-bake the sample in a hotplate at 120 °C for 2 mins.
  b) Spin coat the sample with S1813 photoresist at 60 s, 4000 rpm.
  c) Soft-bake the resist on a hotplate at 115 °C for 90 s.
  d) Pattern the gate pad using UV lithography for 5 s.
  e) Stir the sample in MF 319 developer for 60-70 s.
  f) Rinse in DI water.
  g) Hard-bake resist on hotplate at 120 °C for 15 min.
  h) Etch W in RIE-Trion using $SF_6$:Ar at 45/10 sccm, 140 W and 185 mTorr for 45 s.
  i) Remove etch residues in Plasma Preen using $O_2$ plasma ashing for 30 s.
  j) Remove resist by rinsing in acetone followed by IPA.

8. **MESA ETCH**

- Pre-bake the sample in a hotplate at 120 °C for 2 mins.
- Spin coat the sample with S1813 photoresist at 60 s, 4000 rpm.
- Soft-bake the resist on a hotplate at 115 °C for 90 s.
- Pattern the mesa structure using UV lithography for 5 s.

- Stir the sample in MF 319 developer for 60-70 s.
- Rinse in DI water.
- Hard-bake resist on hotplate at 120 °C for 15 min.
- Wet-etch planar InAs using 1:1:25 $H_3PO_4$:$H_2O_2$:$H_2O$ for 2 mins.
- Rinse in DI water.
- Remove etch residues in Plasma Preen using $O_2$ plasma ashing for 30 s.
- Remove resist by rinsing in 40 °C acetone for 3 mins followed by IPA.

9. **HIGH-K LENGTH DEFINITION**

- Pre-bake the sample in a hotplate at 120 °C for 2 mins.
- Spin coat the sample with S1813 photoresist at 60 s, 4000 rpm.
- Hard-bake the resist on a hotplate at 120 °C for 15 min.
- Etch S1813 in RIE-Trion using $O_2$ plasma at 15 sccm, 300 mTorr and 50 W to the desired length of the spacer. Monitor in SEM at constant intervals for the desired length.
- Wet-etch bilayer high-k, $HfO_2$-$Al_2O_3$, in HF 1:400 for 6 min 45 s.
- Remove resist by rinsing in 40 °C acetone for 3 mins followed by IPA.

10. **TOP SPACER FORMATION**

- Load the sample into the ALD Savannah.
- Surface cleaning using 5 cycles TMAl.
- Deposit 100 cycles of $Al_2O_3$ at 120 °C.
- Monitor in SEM to confirm deposition thickness.

11. **VIA-HOLE FORMATION FOR CONTACT PADS**

- Spin coat the sample with S1813 photoresist at 60 s, 4000 rpm.
- Soft-bake the resist on a hotplate at 115 °C for 90 s.
- Pattern the gate and drain via-holes using UV lithography for 5 s.
- Stir the sample in MF 319 developer for 60-70 s.
- Rinse in DI water.
- Hard-bake resist on hotplate at 120 °C for 15 min.
- Etch the top spacer in the via-holes in RIE-Trion using $O_2$ plasma at 15 sccm, 300 mTorr and 50 W.

- Remove resist by rinsing in acetone followed by IPA.
- Spin coat the sample with S1813 photoresist at 60 s, 4000 rpm.
- Soft-bake the resist on a hotplate at 115 °Cfor 90 s.
- Pattern the drain via-hole using UV lithography for 5 s.
- Stir the sample in MF 319 developer for 60-70 s.
- Rinse in DI water.
- Hard-bake resist on hotplate at 120 °C for 15 min.
- Remove the trilayer high-k oxide in the via-hole using HF 1:400 for 3 min 45 s.
- Remove resist by rinsing in 40 °C acetone for 3 mins followed by IPA.

12. **TOP CONTACT**

- Remove high-k $Al_2O_3$ on top of the nanowire using BOE 30:1 for 25 s.
- Load the sample immediately into the sputter AJA Orion deposition chamber.
- Sputter 10 nm Ni at 9 sccm Ar-flow and 100 W DC power with rotation.
- Sputter 200 nm Au at 9 sccm Ar-flow and 100 W DC power with rotation.
- Spin coat the sample with S1813 photoresist at 60 s, 4000 rpm.
- Soft-bake the resist on a hotplate at 115 °C for 90 s.
- Pattern the contact pads using UV lithography for 5 s.
- Stir the sample in MF 319 developer for 60-70 s.
- Rinse in DI water.
- Hard-bake resist on hotplate at 120 °C for 15 min.
- Wet-etch Au using KI-based etchant for 25 s.
- Wet-etch Ni using 1:2.5:2.5:5 $CH_3COOH$:$HNO_3$:$H_2SO_4$:$H_2O$ for 100 s.
- Remove resist by rinsing in acetone followed by IPA.