# A Novel Bipolar PFC Converter for Battery Charging Application

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2024

*Document Version:*
Publisher's PDF, also known as Version of record

2024

Master's Thesis

# A Novel Bipolar PFC Converter for Battery Charging Application

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MVM Smart Power Laboratórium

2024.05.24.

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# MSC THESIS TASK DESCRIPTION

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Candidate for MSc degree in Electrical Engineering

## *A Novel Bipolar PFC Converter for Battery Charging Application*

Power electronic converters are pivotal when it comes to designing any charging scheme, regardless of the battery capacity. Nowadays, Power Factor Correction (PFC) converters have become popular due to their simple configuration. Single-Ended Primary-Inductor Converter (SEPIC) and Cuk PFC converters are preferred over Buck-Boost converters in this regard due to their higher efficiencies, lower current ripples, and continuous input current features. Despite having almost identical configurations, SEPIC and Cuk converters have their pros and cons. That being said, these two converters can be controlled together with a single switch to obtain a bipolar output. This novel bipolar converter holds the advantages of both the aforementioned converters. In addition, the inclusion of a switched-inductor configuration at the input side exhibits higher voltage gain in the lower duty cycle, resulting in lower conduction losses in the switch. Subsequently, the coexistence of SEPIC and Cuk converters ensures interleaved operation, which necessitates only half the switching frequency compared to that of a single converter, reducing the power losses during reverse recovery transitions of the diodes. Last but not least, the presence of a single switch at the input side makes it easier to design and control the gate driver to provide a steady bipolar DC-link voltage, which can be fed to two Dual Active Bridge (DAB) or Phase-Shifted Full-Bridge (PSFB) converters to charge two batteries of different capacities simultaneously, providing the galvanic isolation at the same time. While the bipolar converter ensures the PFC operation, the following DAB or PSFB converters account for the typical constant-current and constant-voltage (CC-CV) charging mechanism.

Tasks to be performed by the student will include:

- ✓ Steady-state analysis and analytical modeling
- ✓ Additional design-oriented analyses and dynamic behavior of the proposed model
- ✓ Robust control mechanism in the face of different performance parameters
- ✓ Comparison with existing topologies and the latest state-of-the-art
- ✓ If possible, prototype testing in Power Hardware in the Loop (PHIL) environment

**Supervisor at the department:** Dr. Dávid Raisz, associate professor

Budapest, 19th February 2024

/ Dr. József Ladányi /
Associate professor
Head of the Department

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I, **Md Abdullah Al-Hysam**, the undersigned, declare that the present MSc thesis work has been prepared by myself and without any unauthorized help or assistance. Only the specified sources (references, tools, etc.) were used. All parts taken from other sources, word by word or after rephrasing but with identical meaning, were unambiguously identified with explicit reference to the sources utilized.

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Budapest, 24 June 2024

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**Md Abdullah Al-Hysam**

# ACKNOWLEDGEMENT

I express my deepest gratitude to my supervisor and research advisor, **Dr. Dávid Raisz**, Associate Professor, Department of Electric Power Engineering, Budapest University of Technology and Economics, for his relentless support, persistent guidance, continuous supervision, and invaluable suggestions during the entire research work. I want to thank **Dr. Csaba Farkas** for his prompt response regarding any academic matters during my two-year master's journey. Honestly, he was the one who helped me connect with **Dr. Dávid** based on my research interest. Moreover, I wish to acknowledge and express my appreciation to **Zaid Ali** and **Bence Sütő**, who helped me with the imperix rapid prototyping. I also want to address the contributions of my parents and my wife, **Fausiya Zaman Suha**, whose unconditional love and support inspired me to reach beyond the boundaries and think out of the box. Finally, I thank the **MVM Smart Power Laboratory** for their patient assistance during the thesis work.

## *Nomenclature*

| Symbol(s) | Meaning |
|---|---|
| $v, i, d$ | AC quantities |
| $V, I, D$ | DC quantities |
| $\langle v \rangle, \langle i \rangle$ | Averaged quantities |
| $\hat{v}, \hat{\imath}, \hat{d}$ | Dynamic quantities |

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# ABSTRACT

Power electronic converters are pivotal while designing any charging scheme, regardless of the battery capacity and application. Nowadays, Power Factor Correction (PFC) converters have become popular for various battery charging systems due to their simple configurations. Single-Ended Primary-Inductor Converter (SEPIC) and Cuk PFC converters are preferred over buck-boost converters in this regard due to their higher efficiencies, lower current ripples, and continuous input current features. Despite having almost identical configurations, SEPIC and Cuk converters have their pros and cons. That being said, these two converters can be controlled together with a single switch to obtain a bipolar output. This novel bipolar converter holds the advantages of both the converters mentioned earlier. In addition, the inclusion of a switched-inductor configuration at the input side exhibits a higher voltage gain in a lower duty cycle, resulting in a reduced conduction loss in the switch. Moreover, the coexistence of SEPIC and Cuk converters ensures an interleaved mechanism, which necessitates only half the switching frequency compared to that of a single converter, reducing the power losses during reverse recovery transitions of the diodes. Apart from that, the presence of a single switch at the input side makes it easier to design and control the gate driver to provide a steady bipolar DC-link voltage, which can be fed to two Dual Active Bridge (DAB) or Phase-Shifted Full-Bridge (PSFB) converters to charge two batteries of different capacities simultaneously, providing the galvanic isolation at the same time. While the bipolar converter ensures the PFC control, the following DAB or PSFB converters account for the typical constant-current and constant-voltage (CC-CV) charging mechanism. Therefore, the proposed bipolar PFC converter, based on a hybrid SEPIC-Cuk combination, not only improves the power quality, such as input power factor and total harmonic distortion (THD), but also makes the control circuitry simple and concise due to its simplistic architecture. On top of that, the derived small-signal model and the average current mode (ACM) control strategy facilitate realizing the converter dynamics with reduced poles and considerably reduced overshoot, settling and rise time. Last but not least, a complete design guideline and soft-switching control technique for the cascaded PSFB and DAB converters were obtained to improve the efficiency at the DC-DC power stage. Finally, the novel hybrid bipolar PFC converter was tested in the Power Hardware-in-the-Loop (PHIL) laboratory environment.

# 1 INTRODUCTION

Between 2010 and 2015, the transportation sector's contribution to the world's energy-related $CO_2$ emissions was roughly *23%*, with an annual increase rate of *2.5%*. The demand for fossil fuels is also progressively rising because of the improvements in the transportation system. Typical Internal Combustion Engines have only around *20%* efficiency, meaning that the remaining energy is lost in the form of heat and greenhouse gases as a byproduct of combustion [1]. Therefore, alternative clean, efficient, intelligent, and environmentally friendly urban transportation has become one of the most pressing needs of our time. Besides, the rising cost of fossil fuels, combined with growing environmental concerns, has heightened interest in the development and research of electric vehicle propulsion technology. Moreover, automakers have been experimenting with various types of propulsion motors and energy conversion systems in conjunction with modern power conversion technology [2]. Electric vehicles with artificial intelligence can also improve traffic safety and road usage [3]. Apart from that, the reduction of $CO_2$ emissions and energy reliance in industrialized economies may require significant action in the transportation sector to reduce fossil fuel consumption. Hence, the widespread adoption of fully electric and hybrid electric vehicles entails considerable research and development expenditures. Substantial improvements and alterations in power grid management, like smart grids, rapid charging station design, and the potential use of on-board energy storage systems as a backup of surplus energy, known as Vehicle to Grid (V2G), produced by renewable energies, are receiving a lot of research attention [4]. With this shift in strategy, the technical world anticipates significant technological breakthroughs, resulting in a product that will lead the global market in the following years. The propulsion system, which provides the tractive effort to propel a vehicle, is a vital subsystem in an EV. This propulsion system includes an energy storage system, a power converter, a propulsion motor, and related controllers [5]. As a result, the broad adoption of fully electric and hybrid electric vehicles necessitates significant R&D investments in power electronic converters [6].

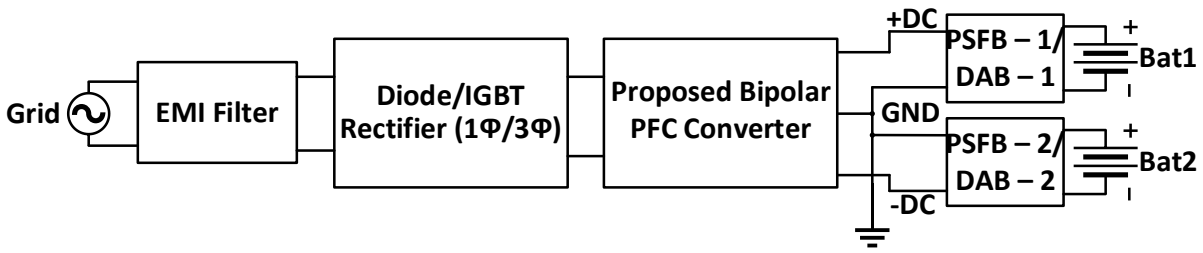



**Fig. 1.1: Proposed Charging System**

In this thesis, a holistic bipolar PFC converter with a switched-inductor-based gain-enhancing technology is proposed. The simplistic architecture, merging SEPIC and Cuk converters with the help of only one Insulated Gate Bipolar Transistor (IGBT), allows the model to operate in both the single-phase and three-phase inputs, depending on the capacity of the battery, with the same control circuitry. While the single-phase version can be suitable for low-capacity battery charging applications, the three-phase version is more suited for charging high-capacity batteries. Apart from that, the topology is so flexible that it can be used with both the diode-bridge and IGBT-bridge rectifiers, making it possible for future bidirectional applications. The gain-enhancing feature allows the converter to operate in the lower duty cycle, resulting in fewer conduction losses. The interleaved operation of

SEPIC and Cuk converters requires half the switching frequency compared to a single converter, reducing the reverse recovery losses of the power diodes. The current flows in parallel and series through the switched-inductor during the on and off periods, respectively, which exhibits the voltage gain, followed by –

$$\left|\frac{V_{01}}{V_{S,rms}}\right| = \left|\frac{V_{02}}{V_{S,rms}}\right| = \frac{D(1+D)}{D'} \qquad (1.1)$$

Here, *D* is the duty cycle of the proposed converter, and *D' = (1-D)*. Therefore, the voltage gain for each bipolar DC-link is *(1+D)* times higher than that of the conventional SEPIC and Cuk converters.

The hybrid bipolar converter maintains a steady bipolar DC-link voltage, which can simultaneously be fed to two Dual Active Bridge (DAB) or Phase-Shifted Full-Bridge (PSFB) converters, as illustrated in Fig. 1.1. The average current mode (ACM) control strategy makes the bipolar topology better immune to noise. The robustness of the tuned Proportional and Integral (PI) controllers, with the help of the small-signal model, ensures the converter responds faster to sudden load changes while ensuring the power factor correction (PFC). On the other hand, the following DAB or PSFB converters are responsible for ensuring the constant-current and constant-voltage (CC-CV) charging behavior. Incorporating DAB paves the way for future bidirectional power flow.

## 1.1 Research Objectives

- ✓ Steady-state analyses and analytical modeling
- ✓ Additional design-oriented analyses and dynamic behavior of the proposed model
- ✓ Robust control mechanism in the face of different performance parameters
- ✓ Comparison with existing topologies and the latest state-of-the-art
- ✓ Prototype testing in the Power Hardware-in-the-Loop (PHIL) laboratory environment

## 1.2 Research Methodology

A plethora of literature on Switched-Mode Power Supply-based charging systems was studied to discover the research gap. Different design-oriented analyses were carried out to thoroughly investigate the model's feasibility. Altair PSIM was used to identify the current and voltage direction across the passive elements, while Microsoft Visio was used to draw the necessary figures. Finally, MATLAB/Simulink was used to design the controller, which was later used to implement a prototype in the Power Hardware-in-the-Loop (PHIL) laboratory environment.

## 1.3 Research Orientation

**Chapter 2** will discuss the literature review and research gap, followed by research contributions. **Chapter 3** will shed light on the detailed description of the proposed charging solution. Steady-state analyses and converter design guidelines will be thoroughly investigated in **Chapter 4**. The mathematical foundation to realize the dynamic behaviors of the converters will be solidly developed in **Chapter 5**. The designed controllers will be adequately explained in **Chapter 6**. The simulation and experimental results of the proposed topology will be presented in **Chapter 7**, where a comparison will also be made with some of the relevant existing models. Finally, **Chapter 8** will conclude by highlighting the significant findings and the prospect of the thesis.

# 2 LITERATURE REVIEW

The availability and effectiveness of charging infrastructure are significant obstacles to EV adoption. Typical EV chargers convert alternating current (AC), taken from the grid, into direct current (DC), which is then stored in the batteries as a form of electrical energy [7]. As a power conversion unit, the efficiency of such chargers is crucial in the face of power losses that may affect the charging time, cost of electricity, and battery life. That being said, several power electronics converter-based charging schemes are currently being researched. One such topology involves a solar-powered EV charging station, consisting of a front-end buck-boost DC-DC converter, followed by a phase-shifted full-bridge (PSFB) converter and a buck converter [8], which requires three stages of power conversion with lots of semiconductor switches that may incur a significant amount of power loss due to the hard-switching architecture. On top of that, the front-end buck-boost converter draws discontinuous input current from the mains. Except that, the charging system is designed for a DC input. In contrast, most of our available power input is AC, meaning an additional PFC rectifier would be needed, had it been operated with an AC input. A ripple-free fast charging system is based on three-phase grid-tied interleaved converters involving three separate three-phase rectifiers, followed by another three DC-DC interleaved choppers [9]. In this topology, there are two power conversion stages, each having three power converters with six semiconductor switches, meaning that there are thirty-six semiconductor switches in total, which may cause a considerable power loss, making it unsuitable for charging low or medium-capacity batteries. Despite having the capability to use three-phase input for fast charging, controlling such a number of switches necessitates an overly complex control strategy to implement. An extremely fast charging model, consisting of three interleaved PFC converters and three interleaved isolated DC-DC converters, has been thoroughly investigated [10]. While this model is suitable for fast charging with galvanic isolation, usage of multiple power conversion stages will require a large number of power switches that will result in a significant power loss due to hard-switching and account for a complicated control mechanism. An integrated on-board single-phase EV charger incorporates two traction inverters [11]. Although this model eliminates the necessity of fast-switching of the inverters to mitigate the power loss because of hard-switching, two traction inverters with six switches interfacing with the motor drive may still incur considerable switching losses, affecting the overall efficiency.

Among different proposed power electronic converter-based charging schemes, another potential configuration involves a full-bridge front-end converter followed by a bidirectional Dual Active Bridge converter [12]. While this configuration fits for charging batteries with large capacities, controlling a large number of power switches with a bidirectional power flow to ensure a constant-current and constant-voltage (CC-CV) mode of operation can still be investigated. Zero-voltage switching (ZVS) has been a popular concept for mitigating switching losses across power switches. Two interleaved boost PFC converters, including an auxiliary circuitry involving passive elements between two phases, can ensure such a ZVS technique [13]. This topology can be an ideal substitute for the H-bridge, which is well-known in automotive applications. Voltage mode controller has been implemented in this model. The controller's attempt to regulate the voltage to a DC value causes issues in the voltage control loop. Nevertheless, the double-frequency component is overlaid with the DC value of the feedback signal. As a result, the controller cannot separate the double-frequency ripple from the closed-loop control

system. Incorporating a current mode controller may resolve this issue, which necessitates separate research.

A universal wide-ranging high power density charging system was developed using an LCL-T resonant network-based Dual Active Bridge converter [14]. While the full-bridge and the stacked half-bridge rectifiers are used for low-voltage (LV) and high-voltage (HV) charging schemes, respectively, the overall topology has become overcomplicated due to the presence of too many power switches and passive elements. On top of that, the system is designed for a DC input, meaning that an additional PFC circuitry and control scheme are required, should it be operated with an AC input. A bidirectional multichannel Cuk converter was assessed for auxiliary and backup power supply in the telecommunication area, enabling flexible and efficient charging of LV batteries [15]. Although this model stands as the first-ever bidirectional Cuk topology, the total component count has doubled, that too for charging LV batteries, which may deteriorate the overall efficiency, and such a large number of passive elements may have a detrimental effect on the converter dynamics. A bidirectional charging system with a relatively higher peak efficiency is proposed by discarding the high-frequency isolation transformer from the typical Dual Active Bridge converters [16]. The absence of a high-frequency transformer can potentially reduce the power losses and the number of required power switches, resulting in higher efficiency. On the contrary, insurmountable control complexities may result due to the removal of the isolation transformer, making it nearly impossible to design the analog control circuitry with isolation between two different power grounds. Such circumscription is well acknowledged in the literature, though.

Interleaved and bridgeless boost PFC converters have been discussed among different front-end PFC topologies for battery charging systems [17]. Although the front-end converters improve the power quality, additional DC-DC power converters with continuous output current features are needed since boost converters have discontinuous output current characteristics. A unidirectional, non-isolated, high-current battery charger comprises a bridgeless boost PFC at the input stage and an interleaved buck converter at the output stage [18]. However, such a non-isolated topology is unsuitable for charging HV batteries and rules out any possibilities of future V2G applications. Different charge balancing methods, based on soft-switching of power converters, have also been investigated for battery management systems (BMS) to improve battery life cycle and safety [19]. The PFC capabilities of such topologies necessitate further research attention. A novel active-clamped half-bridge (HB) converter with a ZVS feature and improved efficiency for wireless inductive power transfer (IPT) charging application was proposed and implemented [20]. In addition, a new simple hybrid (nonlinear and linear) dual-loop control strategy was developed to improve power quality. Despite all these performance enhancements, the output current is discontinuous in nature, resulting in a larger charging current ripple.

An isolated bridgeless discontinuous conduction mode (DCM)-operated Zeta PFC converter was proposed for solar photovoltaic (PV) system-aided household battery charging system [21]. Due to the availability of only single-phase input and DCM operating principle, this model may be unsuitable for large-capacity batteries. Apart from that, the complete CC-CV control strategy has yet to be deployed. Several battery charging converter topologies that are suitable for domestic, industrial, and commercial applications like EVs were thoroughly investigated with available constituents of the converter topologies, design standards, modulations, and control techniques [22]. Among the assessed

topologies, the PFC capabilities of some converters and soft-switching of some architectures are deemed necessary. A dual-input buck-boost topology-based EV charger was proposed [23]. Although the dual input feature makes it possible to charge the battery from both on-board and off-board sources, the discontinuous output current anomaly persists in this topology, resulting in considerable charging current ripple. Different converter topologies and their control strategies were comprehensively discussed for ultra-fast off-board EV chargers [24]. Such a thorough review comes in handy while reproducing any of the assessed architectures for further improvement.

A *48 V – 100 Ah* two-stage on-board EV charger consists of an interleaved boost PFC converter, followed by a PSFB converter [25]. The hard-switching nature of both converters can have a detrimental effect on the system's overall efficiency if subjected to fast-switching. A soft-switched boost PFC converter cascaded with a buck converter was also developed [26]. Although this model alleviates the switching losses involved in its hard-switching counterparts, the potential of this model for HV and large-capacity batteries has yet to be explored. Another bidirectional current mode controlled Cuk converter was proposed with partial-power architecture [27]. However, this model requires another PFC stage if operated with AC mains. A single-phase bridgeless Cuk converter with reduced component count has been proposed with voltage mode control [28]. Nevertheless, without implementing the current mode control, this topology may exhibit poor performance while dealing with high power, thus making it unsuitable for large-capacity battery charging applications.

A *1.2 MHz* soft-switched front-end inverter with *99.5%* peak efficiency was developed and experimentally validated [29]. Such a front-end converter with high power density can pave the way for future V2G applications. An active power decoupling architecture named Floating Capacitor Integrated Dual Active Bridge (FCI-DAB) for AC-DC power conversion is introduced with an active energy buffer, compensating for the power fluctuation [30]. In contrast to conventional single-stage converters, filtering the fluctuating instantaneous power at the primary side has benefits like lowering the RMS current in the secondary side of the converter and reducing the conduction losses. A *5 kW* unidirectional multi-level front-end boost PFC converter with reduced switch count was designed for a wireless EV charging system [31]. Despite improving crucial parameters like efficiency and THD, the prototype is unsuitable for bidirectional power flow.

A bridgeless converter was developed by merging Cuk and SEPIC converters, where two high-frequency transformers were used to provide galvanic isolation to the battery [32]. Although the bridgeless topology reduces the semiconductor losses compared to the typical PFC converters, this model may be unsuitable for charging large-capacity batteries due to the limitation of operating only with the single-phase input. Subsequently, the usage of two high-frequency transformers, that too for single-phase input, may be inconvenient. An isolated SEPIC-Cuk converter merged with a three-phase inverter was proposed for large-scale PV applications [33]. Although this topology was proposed for PV applications, it has the potential to charge large-scale batteries as well. Previously, the very same converter was proposed to obtain a bipolar output with a larger voltage gain [34], where the switched-inductor arrangement, replacing the input inductor, provides a relatively higher gain than the conventional converters [35].

The transformation of EVs has brought about a new set of challenges in the realm of transportation. Despite being omnipresent and entrenched in the socio-economic landscape and their environmental

benefits, the widespread adoption of EVs has led to emerging issues related to charging infrastructure and energy management [36]. One of the primary concerns is the impact on the electricity grid caused by the simultaneous charging of numerous EVs, especially during peak hours. This phenomenon risks grid stability and poses challenges in effectively managing energy demand [37][38]. Several studies show that Vehicle-to-Grid (V2G) technology has emerged as a promising solution to address such challenges [39]–[42]. EV batteries can store energy while charging and release it back to the grid when needed, allowing the bidirectional power flow between EVs and the grid, thanks to the V2G technology [43]. With this feature, EVs become mobile energy storage systems that promote renewable energy integration and improve grid stability [44].

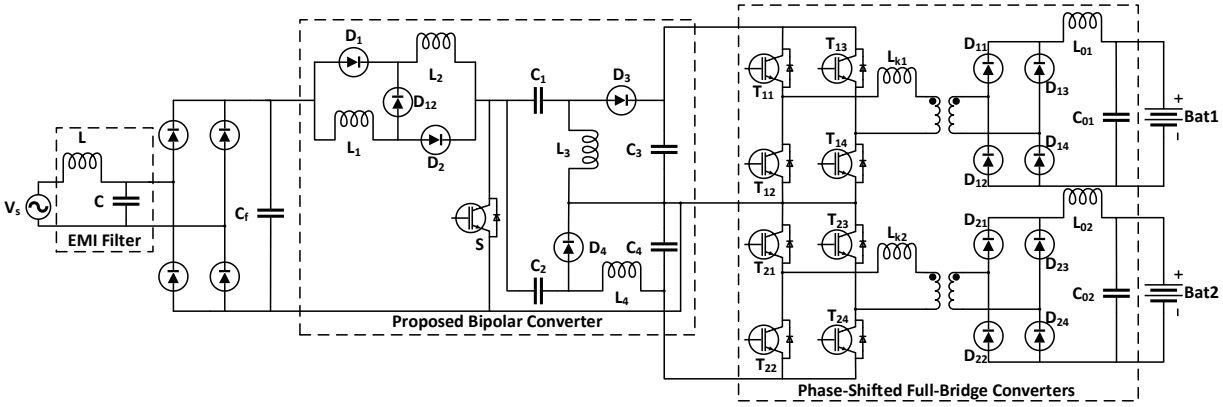
The importance of bidirectional converters in V2G systems cannot be overstated. These converters work as the critical interface between EVs and the grid, facilitating seamless energy exchange in both directions. By enabling bidirectional power flow, these converters allow a range of functionalities, including vehicle-to-home (V2H) energy supply during power outages, cutting peak hours to reduce pressure on the grid, and participation in extra services to support grid stability. In short, bidirectional converters play a crucial part in unlocking the full potential of V2G technology, offering benefits not only to EV owners but also to the broader electricity grid and society overall. As the transition to EVs accelerates, developing and deploying efficient bidirectional converters will be essential in realizing the vision of a cleaner, more sustainable transportation ecosystem.

## 2.1 Research Contribution

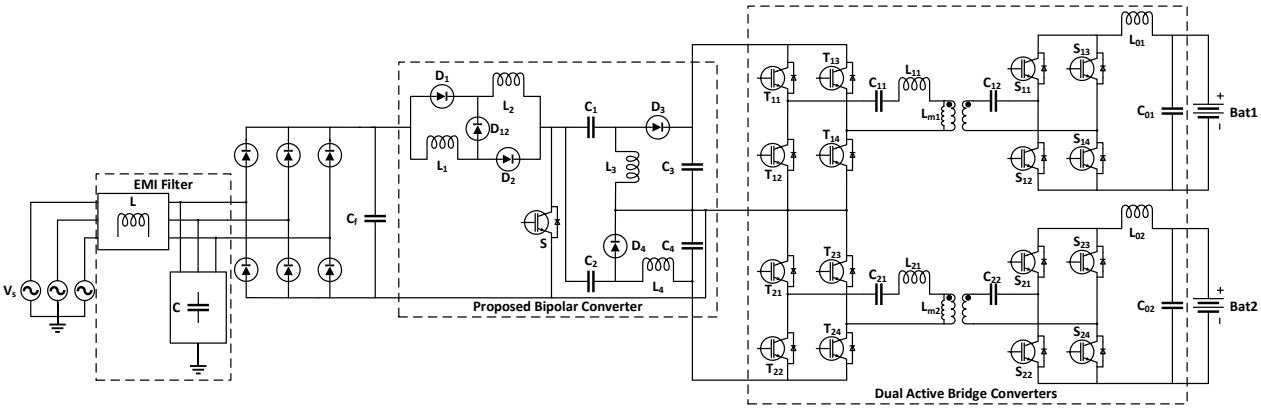
The thesis contributes to several aspects of Power Electronics-dominated charging solutions. First of all, a novel high-gain bipolar PFC converter was developed from SEPIC and Cuk converters. The salient feature of this topology is that it can charge two batteries simultaneously from the supply mains without violating the *IEC 61000-3-2* standard. PSFB converters were used in the DC-DC power stage for household energy storage systems, whereas DAB converters were used for EV charging systems. Soft-switching control was ensured for both PSFB and DAB topologies to reduce switching losses. Small-signal models of all the converters involved in the thesis were derived to realize the dynamic behaviors, paving the way for controller design. Finally, the novel bipolar converter was tested in the Power Hardware-in-the-Loop (PHIL) environment at the Smart Power Laboratory.

# 3 OVERVIEW OF THE PROPOSED CHARGING SOLUTION

The overall charging system comprises three power converters. The novel bipolar converter is modeled for the PFC stage of both household and EV energy storage systems. Two PSFB converters are connected to the bipolar output of the PFC converter to charge two household batteries simultaneously. DAB converters are typically integrated with modern EV battery management systems for potential V2G functionality [7]. The bipolar PFC converter can be installed in the ultra-fast charging station, which can charge two EVs simultaneously.




(a)




(b)

**Fig. 3.1: Proposed (a) household, (b) off-board EV charging systems**

As seen from Fig. 3.1, the off-board EV charging system uses a three-phase input, while the household energy storage system uses a single-phase supply. The ultra-fast EV charging draws significant current from the mains, which is why a three-phase supply is more viable than a single-phase one. In contrast, typical household connections are single-phase ones, and the capacity of the batteries is not as high as that of EVs, meaning that single-phase mains can be suitable for charging such household batteries.

## 3.1 The Novel Bipolar PFC Converter

The topology comprises a SEPIC converter merged with a Cuk converter. The input inductors of the corresponding converters are replaced by a switched-inductor arrangement, resulting in a higher

voltage gain in a lower duty cycle. The upper SEPIC side provides a positive DC output, while the lower Cuk side provides a negative DC output, making it a bipolar converter.

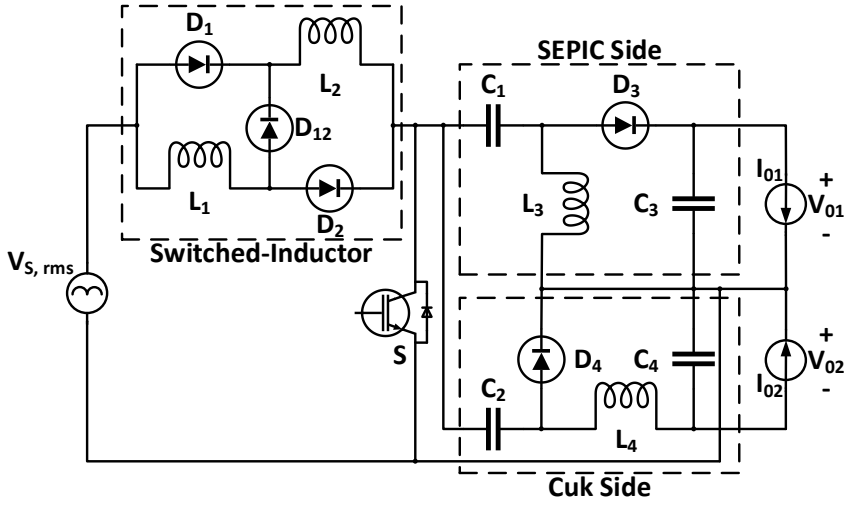



**Fig. 3.2: The novel bipolar PFC converter**

### 3.1.1 Operating Principle

The input voltage, $V_s$, is rectified to a DC voltage, $V_{s,\,rms}$, which supplies the current to the converter. The input current is divided into two parts and flows through two parallel inductors, $L_1$ and $L_2$, due to the forward bias of diodes, $D_1$ and $D_2$, and the reverse bias of diode, $D_{12}$. The resulting current flows to the neutral point through the IGBT since the current flows through the less resistive path due to the IGBT being on. The link capacitor $C_1$ charges the output inductor $L_3$, and the output capacitor $C_3$ provides the positive DC-link output to the load, given that both the capacitors were charged during the previous switching cycle. Both $D_3$ and $D_4$ diodes are reverse-biased at this moment. Meanwhile, the link capacitor, $C_2$, charges the output inductor, $L_4$, and the output capacitor, $C_4$, whereas $C_4$ provides the negative DC-link output to the load.

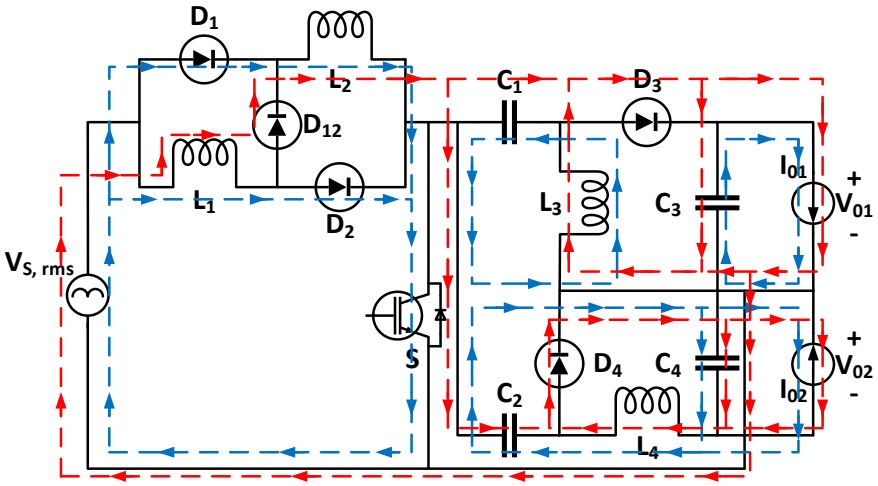



**Fig. 3.3: Current direction through the bipolar PFC converter ($S_{on}$ = blue, $S_{off}$ = red)**

On the other hand, the input current flows through the inductors, $L_1$ and $L_2$, in series as the diodes, $D_1$ and $D_2$, are now reverse biased while the diode, $D_{12}$, is forward biased before it charges both the link capacitors $C_1$ and $C_2$. In this switching scenario, the $D_3$ and $D_4$ diodes are forward-biased, establishing current flowing paths to charge the output capacitors $C_3$ and $C_4$. Nevertheless, $C_3$ and $C_4$ capacitors continue providing positive and negative DC-link voltages to the loads, respectively. It can be noted that the bipolar converter operates with only one active switch. Therefore, the hard-switching of that only active switch will not have any detrimental effect on the system's overall efficiency. Nonetheless, the selection of the passive elements, the switching frequency in the hard-switching context, and the control circuitry design for that operating frequency will be briefly discussed in the following chapters.

## 3.2 PSFB Converters

Two PSFB converters are connected to the bipolar output of the PFC converter to charge two household batteries simultaneously. The high-frequency transformers (HFT) of PSFB converters ensure the galvanic isolation of the batteries. Four active switches, $T_{11}$, $T_{12}$, $T_{13}$, and $T_{14}$, act as an inverter by chopping the DC output of the PFC converter. The HFT steps down the AC voltage as per the battery requirement. Four diodes, $D_{11}$, $D_{12}$, $D_{13}$, and $D_{14}$, revert the DC voltage. However, this DC voltage is accompanied by several high-frequency components (e.g., switching frequencies of the PFC and PSFB converters). Hence, the output LC filter, formed by $L_{01}$ and $C_{01}$, has been used to suppress those high-frequency components and pass only the desired DC output.

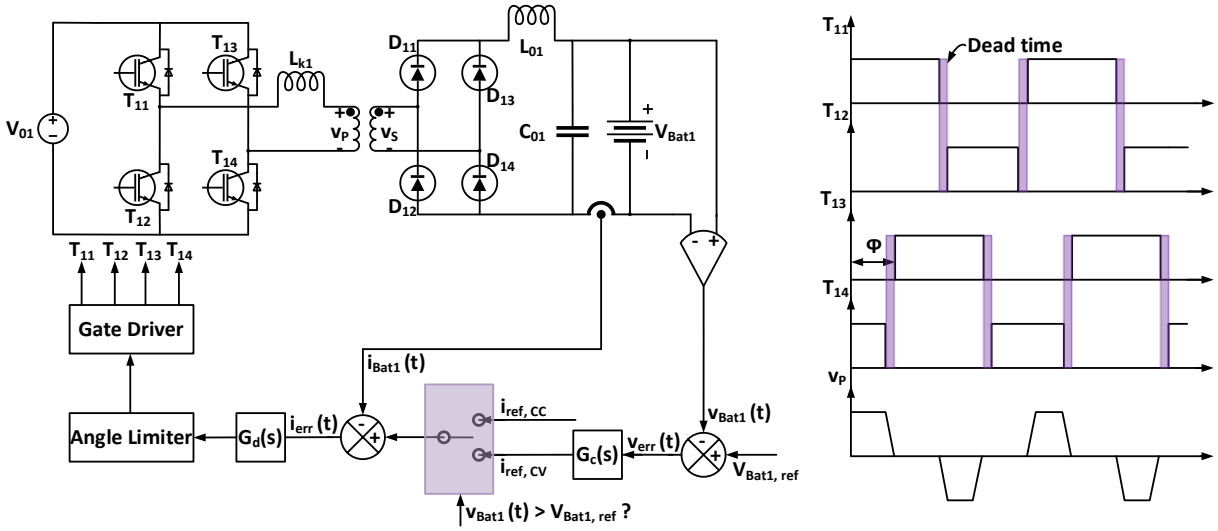



**Fig. 3.4: A soft-switched PSFB converter and its switching arrangement**

### 3.2.1 Operating Principle

The leakage inductor, $L_{k1}$, and appropriate dead-time in the complementary gating pulses ensure the soft-switching to reduce switching losses, allowing such converters to operate in significantly higher operating frequencies. The phase difference, $\Phi$, between $T_{11}$ and $T_{13}$ determines the magnitude of the AC output, $v_p$. When $T_{11}$ and $T_{14}$ are on, $v_p$ equals the $V_{01}$, and the leakage inductor, $L_{k1}$, charges. During the dead-time, corresponding parasitic capacitances and body diodes of the IGBTs establish the discharge path of $L_{k1}$. Hence, zero-voltage turn-off of $T_{14}$ and zero-voltage turn-on of $T_{13}$ can be ensured at the end of the dead-time. HFT is short-circuited through $T_{11}$ and $T_{13}$, thus appearing zero-voltage at

$v_p$. After the end of this period, the zero-voltage turn-off of $T_{11}$ and zero-voltage turn-on of $T_{12}$ occur during the dead-time, and the next operating cycle is executed. A negative magnitude of $V_{01}$ appears at $v_p$ through $T_{12}$ and $T_{13}$. Finally, after zero-voltage turn-off of $T_{13}$ and zero-voltage turn-on of $T_{14}$ during the following dead-time, HFT is again short-circuited through $T_{12}$ and $T_{14}$, resulting in zero-voltage across $v_p$. Finally, the next switching period is initiated, and the operating cycles repeat. The zero-voltage transition (ZVT) of the active switches during the dead-time and how the current flowing path is established through the leakage inductor, corresponding parasitic capacitances, and body diodes of the switches are nicely described in [45]. The design guidelines of the passive elements and the dynamic behavior will be discussed in Chapter 4 and Chapter 5, respectively. Lastly, the typical CC-CV battery charging algorithm has been implemented in the control system of the PSFB converters, which will be discussed further in Chapter 6.

## 3.3 DAB Converters

DAB converters are typically part of EV battery management systems, suitable for both off-board and on-board charging schemes with possible V2G functionality. Like PSFB converters, the HFT transformers of DAB converters provide galvanic isolation to the EV batteries. The DAB converters in the proposed charging models incorporate a fourth-order CLLC resonant tank to overcome the discrepancies in the third-order CLL converters. Hence, soft-switching can be ensured for a bidirectional mode of operation (e.g., zero-voltage switching (ZVS) during charging mode and zero-current switching (ZCS) during discharging mode) [46].

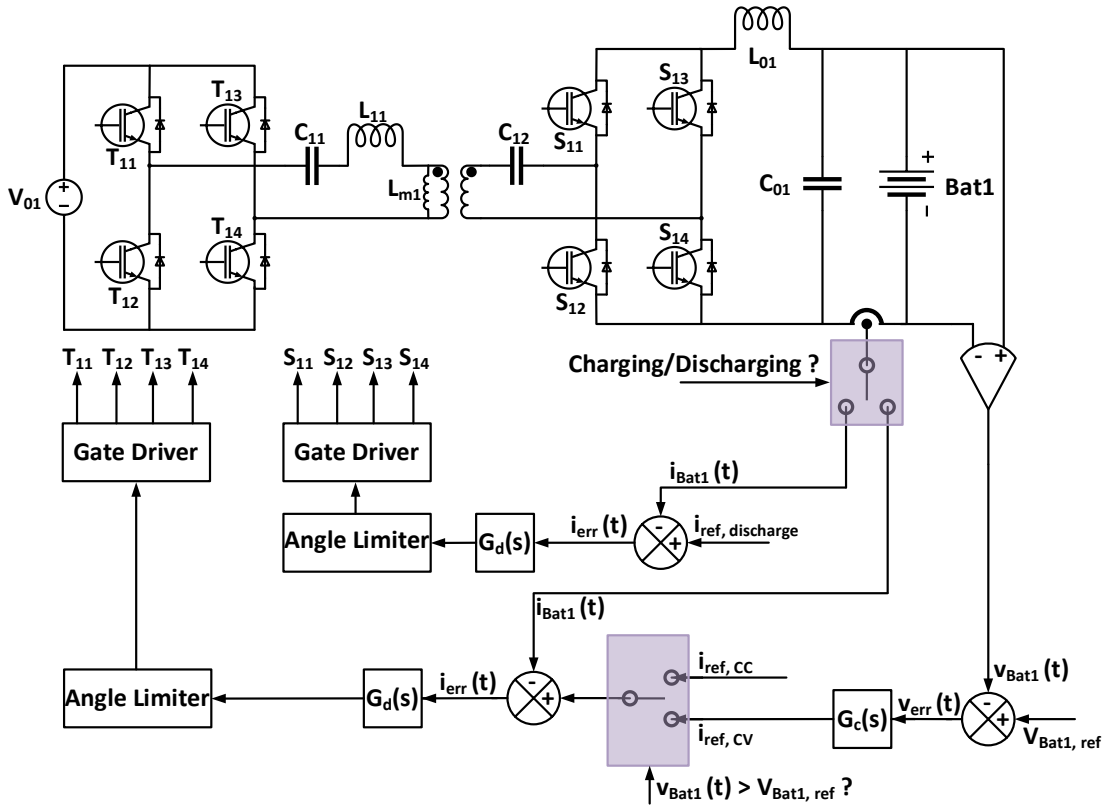



**Fig. 3.5: A soft-switched DAB converter with a CLLC tank**

### 3.3.1 Operating Principle

The basic working principle of DAB and PSFB converters are almost the same, albeit the first active bridge ($T_{11}$, $T_{12}$, $T_{13}$, and $T_{14}$) can be controlled in the charging mode, whereas the second active bridge ($S_{11}$, $S_{12}$, $S_{13}$, and $S_{14}$) can be controlled in the discharging mode. CLLC resonant tank ensures soft-switching in both directions of power flow, for which dead-time control in the gating pulses is desirable. Such soft-switching control tactics are adequately explained in [47]. The following chapters will thoroughly discuss the resonant tank's design parameters, the converter's dynamic behavior, and the associated control system to ensure the CC-CV charging technique.

# 4 STEADY-STATE ANALYSES AND DESIGN GUIDELINES

## 4.1 Objective

This chapter aims to derive the voltage and current gains of the novel bipolar PFC converter in the ideal scenario, determine the voltage and current stresses across the semiconductor switches, and then incorporate lossy elements to prove the efficiency enhancement analytically. Except that, the design guidelines of all the passive elements involved in the complete charging system, such as EMI filters, output filters, leakage inductors, resonant tanks, etc., will be thoroughly developed with proper mathematical justifications.

## 4.2 The Novel Bipolar PFC Converter

According to the operating principle of the converter, it can be translated into two subcircuits, as depicted in Fig. 4.1 and 4.2. When the switch is turned on, the input current, *I*, is divided into two parts and flows through inductors, $L_1$ and $L_2$, in parallel. The capacitor current, $i_{C1}$, flows through the inductor, $L_3$, while the capacitor current, $i_{C2}$, flows through the inductor, $L_4$, the filter capacitor, $C_4$, and the load connected to the negative DC-link. Meanwhile, the filter capacitor, $C_3$, supplies the load connected to the positive DC-link.

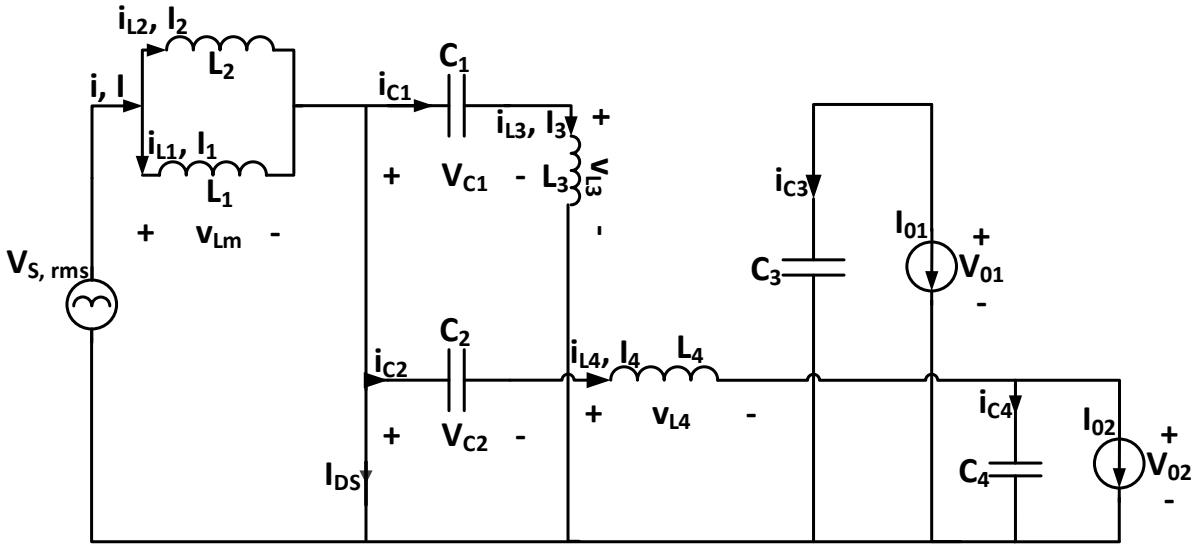



**Fig. 4.1: First sub-interval when the switch is on**

Applying Kirchhoff's Voltage Law (KVL) across the loops formed by the inductors, $L_1$, $L_2$, $L_3$, and $L_4$, corresponds to –

$$v_{Lm} = V_{S,rms}, v_{L3} = -V_{C1}, v_{L4} = -V_{C2} - V_{02} \quad (4.1)$$

Now, applying Kirchhoff's Current Law (KCL) across the nodes connecting the capacitors, $C_1$, $C_2$, $C_3$, and $C_4$, followed by small-ripple approximations, corresponds to –

$$i_{C1} = I_3, i_{C2} = I_4, i_{C3} = -I_{01}, i_{C4} = I_4 - I_{02} \quad (4.2)$$

On the other hand, the input current, *I*, flows through the inductors, $L_1$ and $L_2$, in series before it divides into $i_{C1}$ and $i_{C2}$ when the switch is off. The capacitor current, $i_{C1}$, then divides among the inductor current, $i_{L3}$, the capacitor current, $i_{C3}$, and the positive DC-link current, $I_{01}$. In contrast, the capacitor current, $i_{C2}$, flows to the ground. In the meantime, the inductor current, $i_{L4}$, originates from the ground and flows through the capacitor, $C_4$, and the load, connected to the negative DC-link.

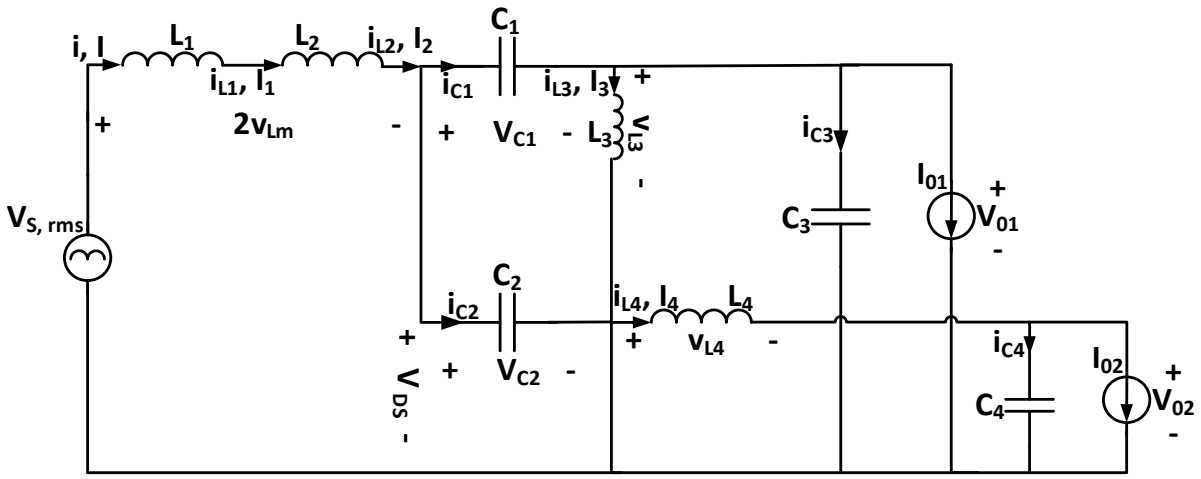



**Fig. 4.2: Second sub-interval when the switch is off**

Applying KVL across the loops formed by the inductors, $L_1$, $L_2$, $L_3$, and $L_4$, corresponds to –

$$v_{Lm} = \frac{V_{S,rms} - V_{C1} - V_{01}}{2} = \frac{V_{S,rms} - V_{C2}}{2}, v_{L3} = V_{01}, V_{L4} = -V_{02} \quad (4.3)$$

Now, applying KCL across the nodes connecting the capacitors, $C_1$, $C_2$, $C_3$, and $C_4$, followed by small-ripple approximations, corresponds to –

$$i_{C1} + i_{C2} = I,\ i_{C3} = i_{C1} - I_3 - I_{01}, i_{C4} = I_4 - I_{02} \quad (4.4)$$

### 4.2.1 Voltage Gain Analyses

Applying volt-second balance across the inductors, $L_1$, $L_2$, $L_3$, and $L_4$, leads to –

$$\langle v_{Lm} \rangle = V_{S,rms} D + \frac{V_{S,rms} - V_{C1} - V_{01}}{2} D' = V_{S,rms} D + \frac{V_{S,rms} - V_{C2}}{2} D' = 0 \quad (4.5)$$

$$\langle v_{L3} \rangle = -V_{C1} D + V_{01} D' = 0 \quad (4.6)$$

$$\langle v_{L4} \rangle = (-V_{C2} - V_{02}) D + (-V_{02}) D' = 0 \quad (4.7)$$

Solving (4.5), (4.6), and (4.7) leads to –

$$V_{01} = V_{S,rms} \frac{D(1+D)}{D'} \quad (4.8)$$

$$V_{02} = -V_{S,rms} \frac{D(1+D)}{D'} \quad (4.9)$$

$$V_{C1} = V_{01}\frac{D'}{D} = V_{S,rms}\frac{D(1+D)}{D'}\frac{D'}{D} = V_{S,rms}(1+D) \quad (4.10)$$

$$V_{C2} = -V_{02}\frac{1}{D} = V_{S,rms}\frac{D(1+D)}{D'}\frac{1}{D} = V_{S,rms}\frac{(1+D)}{D'} \quad (4.11)$$

### 4.2.2 Current Gain Analyses

Now, applying ampere-second balance across the capacitors, $C_1$, $C_2$, $C_3$, and $C_4$, leads to –

$$\langle i_{C1}\rangle = I_3 D + (I - i_{C2})D' = 0 \quad (4.12)$$

$$\langle i_{C2}\rangle = I_4 D + (I - i_{C1})D' = 0 \quad (4.13)$$

$$\langle i_{C3}\rangle = -I_{01}D + (i_{C1} - I_3 - I_{01})D' = 0 \quad (4.14)$$

$$\langle i_{C4}\rangle = I_4 - I_{02} = 0 \quad (4.15)$$

Solving (4.12), (4.13), (4.14), and (4.15) leads to –

$$I_3 = I_{02}D - I_{01}(1+D) \quad (4.16)$$

$$I_4 = I_{02} \quad (4.17)$$

$$I = (I_{01} - I_{02})\frac{D(1+D)}{D'} \quad (4.18)$$

### 4.2.3 Voltage and Current Stresses on the Switch and Diodes

According to Fig. 4.1,

$$I_{DS} = I - I_3 - I_4 = (I_{01} - I_{02})\frac{1+D}{D'} \quad (4.19)$$

$$V_{D3} = -V_{01} = -V_{S,rms}\frac{D(1+D)}{D'} \quad (4.20)$$

$$V_{D4} = V_{02} = -V_{S,rms}\frac{D(1+D)}{D'} \quad (4.21)$$

And, according to Fig. 4.2,

$$V_{DS} = V_{C2} = V_{S,rms}\frac{(1+D)}{D'} \quad (4.22)$$

$$I_{D3} = i_{C1} - I_3 = [I_{01}(1+D) - I_{02}D]\frac{1}{D'} \quad (4.23)$$

$$I_{D4} = i_{C2} - I_4 = \frac{-I_{02}}{D'} \quad (4.24)$$

### 4.2.4 Selection of Passive Elements

#### *4.2.4.1 Selection of Inductors*

Inductor voltages are equal to the corresponding inductances times the rate of change of the respective inductor currents. Therefore, during the first sub-interval,

$$\frac{di_{L1}}{dt} = \frac{v_{Lm}}{L_1} = \frac{V_{S,rms}}{L_1}, \frac{di_{L2}}{dt} = \frac{v_{Lm}}{L_2} = \frac{V_{S,rms}}{L_2}, \frac{di_3}{dt} = \frac{v_{L3}}{L_3} = \frac{-V_{C1}}{L_3}, \frac{di_4}{dt} = \frac{v_{L4}}{L_4} = \frac{-V_{C2} - V_{02}}{L_4} \quad (4.25)$$

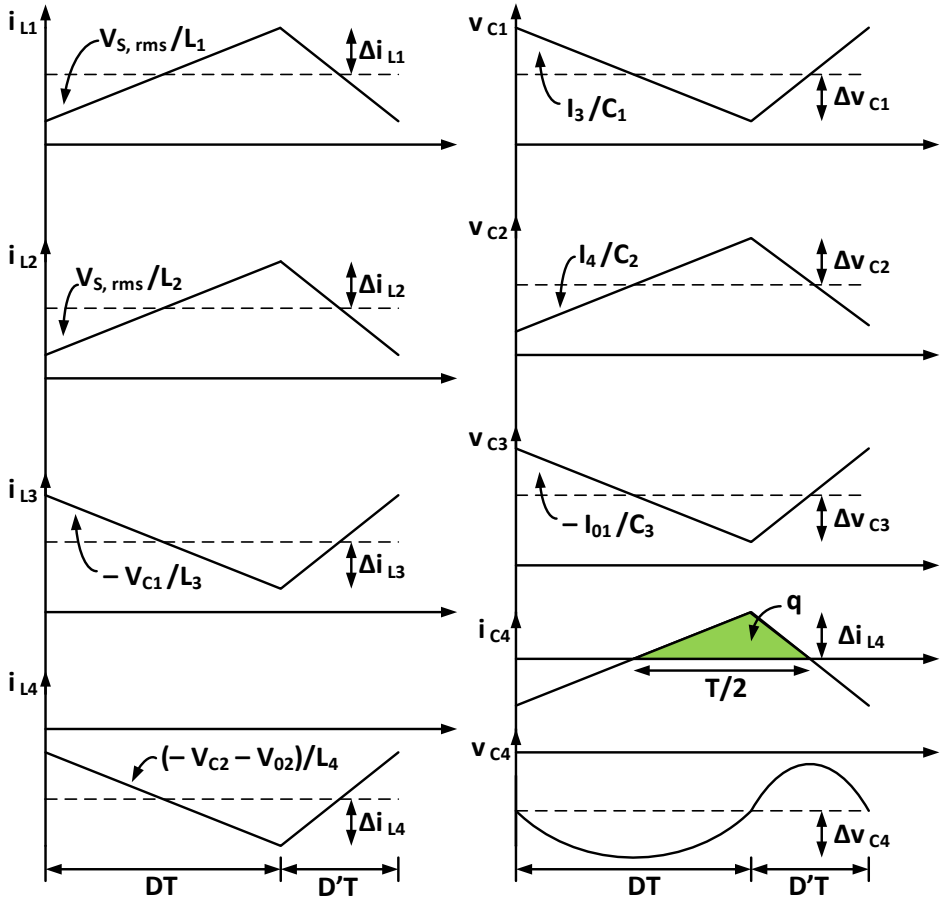



**Fig. 4.3: Current and Voltage waveshapes across the Passive Elements**

If the current ripples through the inductors, $L_1$, $L_2$, $L_3$, and $L_4$, are $\Delta i_{L1}$, $\Delta i_{L2}$, $\Delta i_{L3}$, and $\Delta i_{L4}$, respectively, then according to Fig. 4.3 –

$$2\Delta i_{L1} = \frac{V_{S,rms}}{L_1} DT, 2\Delta i_{L2} = \frac{V_{S,rms}}{L_2} DT, -2\Delta i_{L3} = \frac{-V_{C1}}{L_3} DT =, -2\Delta i_{L4} = \frac{-V_{C2} - V_{02}}{L_4} DT \quad (4.26)$$

Therefore,

$$L_1 = \frac{V_{S,rms} DT}{2\Delta i_{L1}} \quad (4.27)$$

$$L_2 = \frac{V_{S,rms} DT}{2\Delta i_{L2}} \quad (4.28)$$

$$L_3 = \frac{V_{C1}}{2\Delta i_{L3}} DT = \frac{V_{S,rms}}{2\Delta i_{L3}} D(1+D)T \tag{4.29}$$

$$L_4 = \frac{V_{C2} + V_{02}}{2\Delta i_{L4}} DT = \frac{V_{S,rms}}{2\Delta i_{L4}} D(1+D)T \tag{4.30}$$

#### *4.2.4.2 Selection of Capacitors*

Capacitor currents are equal to the corresponding capacitances times the rate of change of the respective capacitor voltages. Therefore, during the first sub-interval,

$$\frac{dv_{C1}}{dt} = \frac{i_{C1}}{C_1} = \frac{I_3}{C_1}, \frac{dv_{C2}}{dt} = \frac{i_{C2}}{C_2} = \frac{I_4}{C_2}, \frac{dv_3}{dt} = \frac{i_{C3}}{C_3} = -\frac{I_{01}}{C_3} \tag{4.31}$$

If the voltage ripples across the capacitors, $C_1$, $C_2$, and $C_3$, are $\Delta v_{C1}$, $\Delta v_{C2}$, and $\Delta v_{C3}$, respectively, then according to Fig. 4.3 –

$$-2\Delta v_{C1} = \frac{I_3}{C_1} DT = \frac{I_{02}D - I_{01}(1+D)}{C_1} DT,$$
$$2\Delta v_{C2} = \frac{I_4}{C_2} DT = \frac{I_{02}}{C_2} DT, -2\Delta v_{C3} = -\frac{I_{01}}{C_3} DT \tag{4.32}$$

Hence,

$$C_1 = \frac{I_{01}(1+D) - I_{02}D}{2\Delta v_{C1}} DT \tag{4.33}$$

$$C_2 = \frac{I_{02}}{2\Delta v_{C2}} DT \tag{4.34}$$

$$C_3 = \frac{I_{01}}{2\Delta v_{C3}} DT \tag{4.35}$$

However, the capacitor, $C_4$, cannot be obtained by the so-called small-ripple approximation since it leads to zero current ripple in the corresponding capacitor. Therefore, the charge-balance tactic will be applied in this regard. If the charge stored in the capacitor, $C_4$, during the entire switching period, $T$, is $q$, then according to Fig. 4.3 –

$$q = C_4(2\Delta v_{C4}) = \frac{1}{2}\Delta i_{L4}\frac{T}{2} \tag{4.36}$$

$$C_4 = \frac{D(1+D)}{16}\frac{V_{S,rms}T^2}{\Delta v_{C4}L_4} \tag{4.37}$$

### 4.2.5 Efficiency Analysis

The topology for determining the gains and design guidelines comprises ideal inductors and capacitors. Nonetheless, the practical converters are associated with some losses. Inductors are made with wires, which have small resistances. Furthermore, the diodes have forward voltage drops and forward resistances. The switch, be it IGBT or MOSFET, also has on-state resistance. All these resistive elements

contribute to conduction losses. To model these losses, Fig. 4.1 and 4.2 can be redrawn like Fig. 4.4 and Fig. 4.5, respectively. However, another type of loss, called switching loss, is caused by the reverse recovery transitions of the diodes, which will be discussed in Section 4.5.

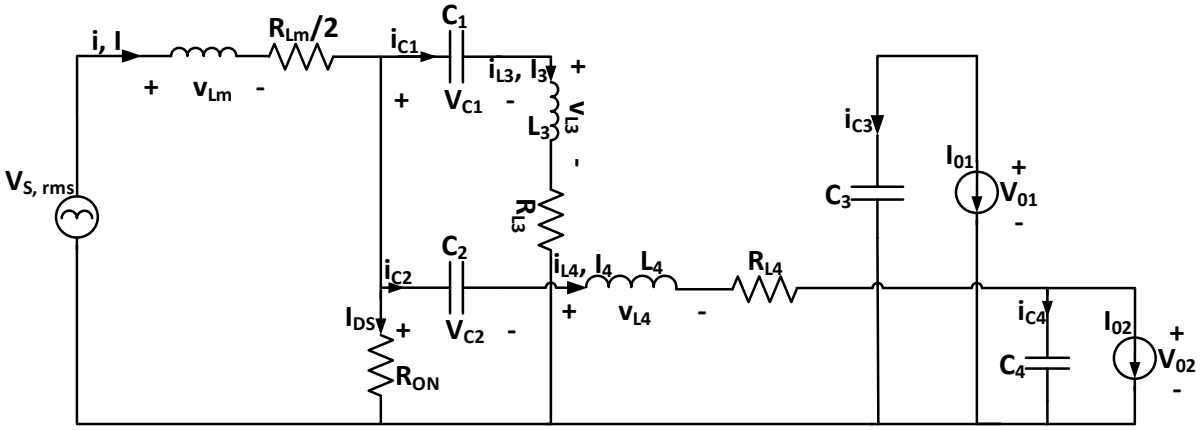



**Fig. 4.4: First sub-interval including resistive elements when the switch is on**

Applying different circuit theorems in the circuit of Fig. 4.4 leads to –

$$v_{Lm} = V_{S,rms} - I\frac{R_{Lm}}{2} - (I - I_3 - I_4)R_{ON} \tag{4.38}$$

$$v_{L3} = -V_{C1} - I_3R_{L3} + (I - I_3 - I_4)R_{ON} \tag{4.39}$$

$$v_{L4} = -V_{C2} - V_{02} - I_4R_{L4} + (I - I_3 - I_4)R_{ON} \tag{4.40}$$

$$i_{C1} = I_3 \tag{4.41}$$

$$i_{C2} = I_4 \tag{4.42}$$

$$i_{C3} = -I_{01} \tag{4.43}$$

$$i_{C4} = I_4 - I_{02} \tag{4.44}$$

Similarly, the same circuit theorems can be applied in the circuit of Fig. 4.5, leading to –

$$v_{Lm} = \frac{V_{S,rms}}{2} - \frac{V_{C1}}{4} - \frac{V_{C2}}{4} - \frac{V_{01}}{4} - \frac{V_D}{2} + \frac{I_3R_D}{4} + \frac{I_4R_D}{4} - \frac{IR_D}{4} - IR_{Lm} \tag{4.45}$$

$$v_{L3} = V_D - \frac{V_{C1}}{2} + \frac{V_{C2}}{2} + \frac{V_{01}}{2} - \frac{I_3R_D}{2} - \frac{I_4R_D}{2} - I_3R_{L3} + \frac{IR_D}{2} \tag{4.46}$$

$$v_{L4} = V_D + \frac{V_{C1}}{2} - \frac{V_{C2}}{2} + \frac{V_{01}}{2} - V_{02} - \frac{I_3R_D}{2} - \frac{I_4R_D}{2} - I_4R_{L4} + \frac{IR_D}{2} \tag{4.47}$$

$$i_{C1} = -\frac{V_{C1} - V_{C2} + V_{01} - I_3R_D + I_4R_D - IR_D}{2R_D} \tag{4.48}$$

$$i_{C2} = \frac{V_{C1} - V_{C2} + V_{01} - I_3R_D + I_4R_D + IR_D}{2R_D} \tag{4.49}$$

$$i_{C3} = -\frac{V_{C1} - V_{C2} + V_{01} + I_3R_D + I_4R_D - IR_D + 2I_{01}R_D}{2R_D} \quad (4.50)$$

$$i_{C4} = I_4 - I_{02} \quad (4.51)$$

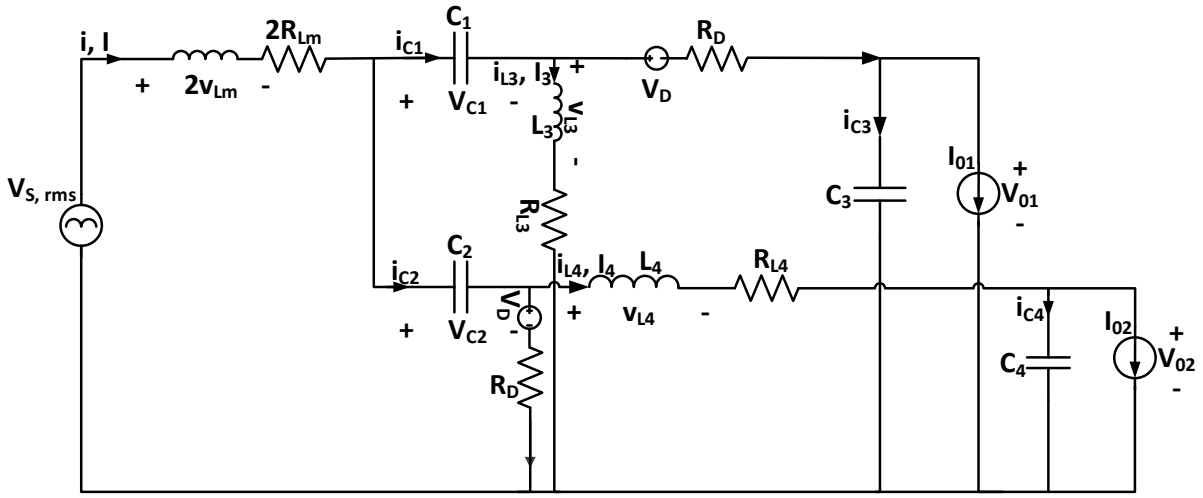



**Fig. 4.5: Second sub-interval including resistive elements when the switch is off**

Now, applying volt-second balance across the inductors, $L_1$, $L_2$, $L_3$, and $L_4$, and ampere-second balance across the capacitors, $C_1$, $C_2$, $C_3$, and $C_4$, leads to –

$$\langle v_{Lm} \rangle = \left[V_{S,rms} - I\frac{R_{Lm}}{2} - (I - I_3 - I_4)R_{ON}\right]D + \left[\frac{V_{S,rms}}{2} - \frac{V_{C1}}{4} - \frac{V_{C2}}{4} - \frac{V_{01}}{4} - \frac{V_D}{2} + \frac{I_3R_D}{4} + \frac{I_4R_D}{4} - \frac{IR_D}{4} - IR_{Lm}\right]D' = 0 \quad (4.52)$$

$$\langle v_{L3} \rangle = [-V_{C1} - I_3R_{L3} + (I - I_3 - I_4)R_{ON}]D + \left[V_D - \frac{V_{C1}}{2} + \frac{V_{C2}}{2} + \frac{V_{01}}{2} - \frac{I_3R_D}{2} - \frac{I_4R_D}{2} - I_3R_{L3} + \frac{IR_D}{2}\right]D' = 0 \quad (4.53)$$

$$\langle v_{L4} \rangle = [-V_{C2} - V_{02} - I_4R_{L4} + (I - I_3 - I_4)R_{ON}]D + \left[V_D + \frac{V_{C1}}{2} - \frac{V_{C2}}{2} + \frac{V_{01}}{2} - V_{02} - \frac{I_3R_D}{2} - \frac{I_4R_D}{2} - I_4R_{L4} + \frac{IR_D}{2}\right]D' = 0 \quad (4.54)$$

$$\langle i_{C1} \rangle = I_3D + \left[-\frac{V_{C1} - V_{C2} + V_{01} - I_3R_D + I_4R_D - IR_D}{2R_D}\right]D' = 0 \quad (4.55)$$

$$\langle i_{C2} \rangle = I_4D + \left[\frac{V_{C1} - V_{C2} + V_{01} - I_3R_D + I_4R_D + IR_D}{2R_D}\right]D' = 0 \quad (4.56)$$

$$\langle i_{C3} \rangle = -I_{01}D + \left[-\frac{V_{C1} - V_{C2} + V_{01} + I_3R_D + I_4R_D - IR_D + 2I_{01}R_D}{2R_D}\right]D' = 0 \quad (4.57)$$

$$\langle i_{C4} \rangle = I_4 - I_{02} = 0 \quad (4.58)$$

Finally, solving from (4.52) to (4.58) leads to –

$$I = (I_{01} - I_{02})\frac{D(1+D)}{D'} \tag{4.59}$$

$$V_{01} = V_{S,rms}\frac{D(1+D)}{D'} - V_D - (I_{01} - I_{02})\left[R_{ON}\frac{D(1+D)}{D'^2} + R_{Lm}\frac{D^2(1+D')}{D'^2}\right] - I_{01}\left(\frac{R_D}{D'} + R_{L3}\right) \tag{4.60}$$

$$V_{02} = -V_{S,rms}\frac{D(1+D)}{D'} + V_D + (I_{01} - I_{02})\left[R_{ON}\frac{D(1+D)}{D'^2} + R_{Lm}\frac{D^2(1+D')}{D'^2}\right] - I_{02}\left(\frac{R_D}{D'} + R_{L4}\right) \tag{4.61}$$

Efficiency can be calculated analytically with the help of the derived expressions of the input current, $I$, and output voltages, $V_{01}$ and $V_{02}$.

The input power, $P_{in} = V_{S,rms}I$ (4.62)

The output power, $P_{out} = V_{01}I_{01} + V_{02}I_{02}$ (4.63)

Therefore, the efficiency, $\eta$, can be expressed as the following –

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{01}I_{01} + V_{02}I_{02}}{V_{S,rms}I} = \frac{V_{01}}{V_{S,rms}}\frac{I_{01}}{I} + \frac{V_{02}}{V_{S,rms}}\frac{I_{02}}{I} \tag{4.64}$$

Fig. 4.6 illustrates the efficiency as a function of the duty cycle, $D$. An analytical comparison has been made with conventional SEPIC and Cuk converters from which the bipolar converter was derived.

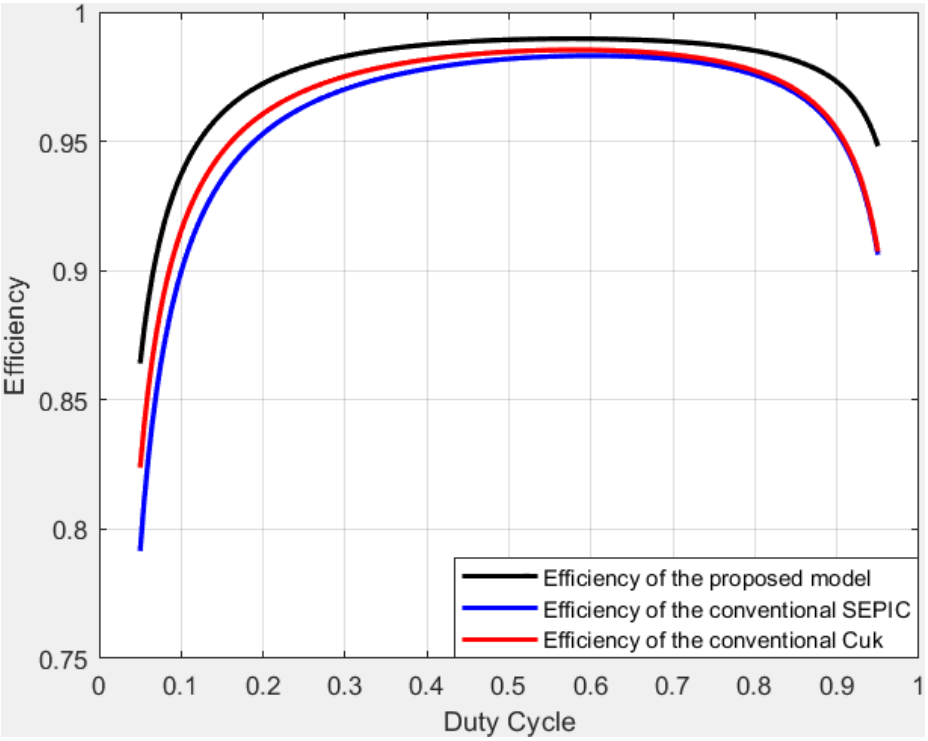



**Fig. 4.6: Efficiency vs. duty cycle**

Analytical expressions of SEPIC and Cuk converters, used for the comparison, were derived in [48]. The gain-enhancing switched-inductor configuration allows the bipolar converter to achieve a higher voltage while operating in a lower duty cycle, which reduces the conduction losses across the power switch and semiconductor diodes. On top of that, currents are shared between SEPIC and Cuk inductors, resulting in lower current stresses and fewer conduction losses.

## 4.3 PSFB Converters

Two PSFB converters have been cascaded with the bipolar output of the novel PFC converter to charge two household batteries simultaneously. The rating of such batteries, considered for a single-phase charging system, was *48 V – 300 Ah*. The nominal charging current for such a Li-ion battery is *130 A*, the cut-off battery voltage is *36 V*, and the highest allowable cell voltage above which the constant-voltage (CV) mode must be activated is *55 V* [49]. Therefore, the nominal power of each of the two PSFB converters can be calculated as the following –

Minimum power, $P_{min} = 36V \times 130A = 4.68kW$

Maximum power, $P_{max} = 55V \times 130A = 7.15kW$

### 4.3.1 Leakage Inductor and Dead-Time Selection

To ensure the zero-voltage turn-on of $T_{13}$, a dead-time is required between the turn-off of $T_{14}$ and the turn-on of $T_{13}$. The resonance among the leakage inductor, $L_{k1}$, the parasitic capacitance of the switch, $C_{MOS}$, and the transformer winding capacitance, $C_{TR}$, results in a sinusoidal voltage that peaks at one-fourth of the resonant period. Therefore,

$$\boldsymbol{\delta_{Tmax} = \frac{T}{4} = \frac{\pi}{2}\sqrt{L_{k1}(C_{MOS} + C_{TR})}} \qquad \textbf{(4.65)}$$

The dead-time, $\delta_{Tmax}$ between $T_{13}$ and $T_{14}$, and the leakage inductor, $L_{k1}$, can be calculated accordingly using (4.65). It is worth noting that the ZVS of $T_{13}$ and $T_{14}$ depends on the converter load, and the current through $L_{k1}$ may not sufficiently charge/discharge the parasitic capacitances to turn on the antiparallel diodes if subjected to light loads [50].

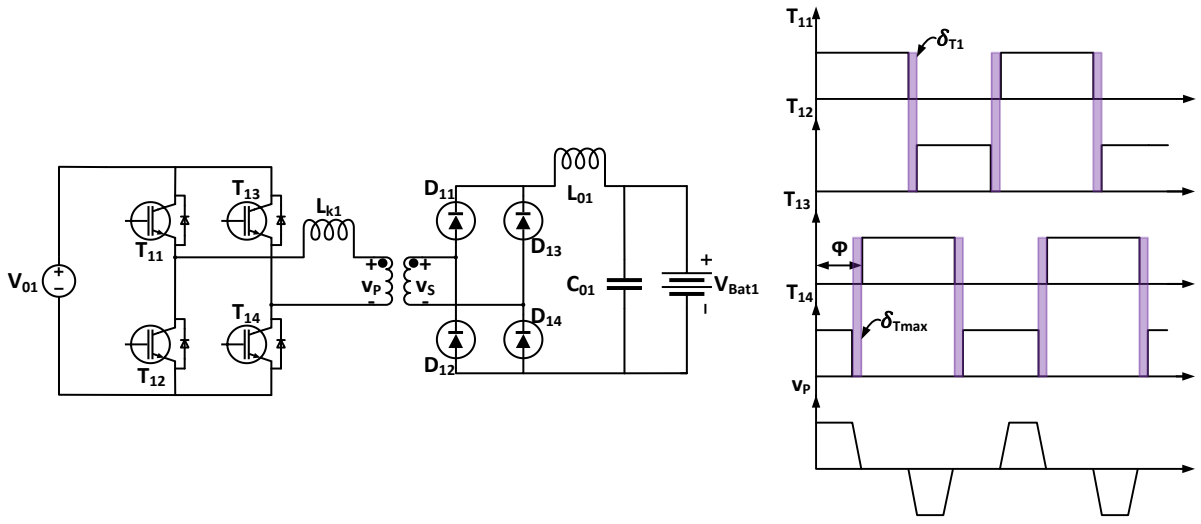



**Fig. 4.7: A ZVS PSFB converter with dead-time switching configuration**

Conversely, the dead-time to ensure ZVS between $T_{11}$ and $T_{12}$ is calculated differently. The current in the primary side of the HFT reaches its peak value, $I_P$, before $T_{11}$ is turned off. The energy at that time to simultaneously charge the parasitic capacitance of $T_{11}$ and discharge the parasitic capacitance of $T_{12}$ equals the stored energy in $L_{k1}$ and the energy in the filter inductor, $L_{01}$, since the filter inductor current has yet to freewheel through the diode bridge rectifier until the secondary voltage of the HFT reaches zero. The parasitic capacitances of the switches can be assumed to be charged linearly with a constant current as the accumulated energy in the filter inductor is comparatively more significant than the required quantity to charge/discharge the capacitances at the primary side of the HFT. Hence,

$$\boldsymbol{4C_{MOS}V_{01} + C_{TR}V_{01} = I_P\delta_{T1}} \qquad (\mathbf{4.66})$$

The dead-time, $\delta_{T1}$, between $T_{11}$ and $T_{12}$ to ensure ZVS can be obtained from (4.66).

### 4.3.2 Output Filter Selection

In this thesis, the soft-switching architecture of PSFB converters, used for household energy storage systems, is based on the power charging unit discussed in [51]. If the peak-to-peak switching ripple current in the output filter inductor, $L_{01}$, is $\Delta i_{L1}$, then according to the mentioned architecture –

$$\boldsymbol{L_{01} = \frac{[nV_{DC1} - \{V_{Bat1}(t) - V_{DC1}\}]D_{eff}T_s}{\Delta i_{L1}}} \qquad (\mathbf{4.67})$$

Here, $n$ is the turns-ratio of the HFT, $V_{DC1}$ is the output voltage of the first PSFB converter, $V_{Bat1}(t)$ is the highest allowable cell voltage of the first household battery, $T_s$ is the switching period, and $D_{eff}$ is the effective duty cycle, which will be discussed further in the next chapter as it is related to the dynamic behavior of PSFB converters.

The peak-to-peak ripple current, $\Delta i_{L1}$, in the filter inductor, $L_{01}$, will flow through the filter capacitor, $C_{01}$, and only the DC component should flow toward the battery. If the current flowing through the capacitor, $C_{01}$, is $i_{C01}$, then –

$$\boldsymbol{i_{C01} = \Delta i_{L1}} \qquad (\mathbf{4.68})$$

And, as the capacitor current is directly proportional to the rate of change of voltage across it,

$$\boldsymbol{\frac{i_{C01}}{C_{01}} = \frac{dV_{DC1}}{dt}} \qquad (\mathbf{4.69})$$

If the corresponding capacitor's peak-to-peak ripple voltage is $\Delta v_{dc1}$, and the effective duty cycle is $D_{eff}$, then –

$$\boldsymbol{\frac{i_{C01}}{C_{01}}D_{eff}T_s = \Delta v_{dc1} = \frac{\Delta i_{L1}}{C_{01}}D_{eff}T_s} \qquad (\mathbf{4.70})$$

Finally,

$$\boldsymbol{C_{01} = \frac{\Delta i_{L1}}{\Delta v_{dc1}}D_{eff}T_s = \frac{[nV_{DC1} - \{V_{Bat1}(t) - V_{DC1}\}]D_{eff}{}^2T_s{}^2}{L_{01}\Delta v_{dc1}}} \qquad (\mathbf{4.71})$$

## 4.4 DAB Converters

Two DAB converters with CLLC resonant tank circuits have been cascaded with the bipolar output of the novel PFC converter to charge two EV batteries simultaneously. Such a system, comprising the single-input multiple-output (SIMO) converter, has formed an ultra-fast off-board charging station. On top of that, the DAB converters, which are typically part of on-board EV charging systems, keep up with the possibility of V2G functionality. The rating of the EV batteries, considered for a three-phase off-board charging system, was chosen as *360 V – 150 Ah*. The nominal charging current for such a Li-ion battery is *65 A*, the cut-off battery voltage is *270 V*, and the highest allowable cell voltage above which the constant-voltage (CV) mode must be activated is *415 V* [49]. Therefore, the nominal power of each of the two DAB converters can be calculated as the following –

Minimum power, $P_{min} = 270V \times 65A = 17.55kW$

Maximum power, $P_{max} = 415V \times 65A = 26.975kW$

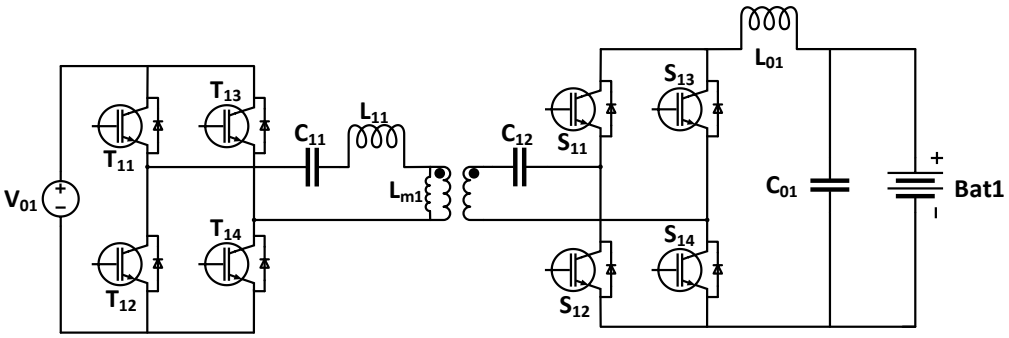



**Fig. 4.8: A CLLC resonant DAB converter**

### 4.4.1 CLLC Resonant Tank Selection

The CLLC resonant DAB converters were controlled using the phase-shift modulation technique proposed in [46]. The design parameters in the context of such a modulation technique have also been derived from the cited Ph.D. dissertation.

$$C_{11} = \frac{\pi P_{max}}{16(1+k)nf_s V_{DC1} V_{Bat1}(t)} \quad (4.72)$$

$$C_{12} = \frac{\pi n P_{max}}{16 f_s V_{DC1} V_{Bat1}(t)} \quad (4.73)$$

$$L_{11} = \frac{4nk V_{DC1} V_{Bat1}(t)}{\pi^3 f_s P_{max}} \quad (4.74)$$

$$L_{m1} = \frac{4n V_{DC1} V_{Bat1}(t)}{\pi^3 f_s P_{max}} \quad (4.75)$$

Here, $n$ is the turns-ratio of the HFT, $V_{DC1}$ is the output voltage of the first DAB converter, $V_{Bat1}(t)$ is the highest allowable cell voltage of the first EV battery, $f_s$ is the switching frequency, $k$ is the degree of freedom, and $P_{max}$ is the maximum output power of the converter.

### 4.4.2 Dead-Time Selection

DAB converters have two active bridges, unlike PSFB converters. The integrated CLLC resonant tank ensures soft-switching in both directions of power flow. Specifically, the ZVS turn-on occurs in the first active bridge, whereas the ZCS turn-on occurs in the second active bridge. The detailed calculation of dead-time to ensure soft-switching has been derived in [52]. Nonetheless, one should note that the dead-time is approximately the same for both PSFB and DAB converters for a given switching frequency and output power [53].

### 4.4.3 Output Filter Selection

According to [53], the output LC filter of DAB converters follows the same design guidelines of PSFB converters, derived in (4.67) and (4.71).

## 4.5 Selection of Switching Frequencies

In Subsection 4.2.5, losses in the bipolar PFC converter were modeled by the resistive elements in series with the passive components, on-state switching resistance, diode forward voltage drops, and resistances. While these losses depend on the load current, switching frequency does not affect them. But, in reality, the switching frequency has some effects on losses, although not as significant as the conduction losses if subjected to low switching frequencies. Nevertheless, this switching loss starts building up with the increasing switching frequency in a hard-switching context. So, the total converter loss can be expressed as the following –

$$\boldsymbol{P_{total} = P_{fixed} + P_{conduction} + W_{total} f_{switch}} \qquad (\mathbf{4.76})$$

Where,

$P_{fixed}$ = Fixed losses, independent of the load and switching frequency

$P_{conduction}$ = Conduction losses across the resistive elements

$W_{total}$ = Energy losses during the switching transitions of one switching period

$f_{switch}$ = Switching frequency of the converter

In the lower frequency, the converter components, including inductors, capacitors, diodes, and IGBT, need to be bigger in size, resulting in more conduction losses, and these losses decrease with the frequency increase. In contrast, switching losses increase with the rise in frequency due to the reverse recovery transitions of the diodes. Therefore, trad-off is often opted for when selecting a suitable switching frequency. Nonetheless, switching losses equal the conduction losses at a critical frequency.

$$\boldsymbol{f_{critical} = \frac{P_{conduction} + P_{fixed}}{W_{total}}} \qquad (\mathbf{4.77})$$

For the switching frequency greater than the critical frequency, switching losses start dominating the conduction losses, and the resulting efficiency decreases rapidly with further frequency increase. Fig. 4.9 depicts efficiency as a function of switching frequency on a logarithmic scale, presented in [54]. In the case of the proposed topology, such a trade-off led to a *50 kHz* switching frequency, given that the bipolar PFC converter operates in a hard-switching manner.

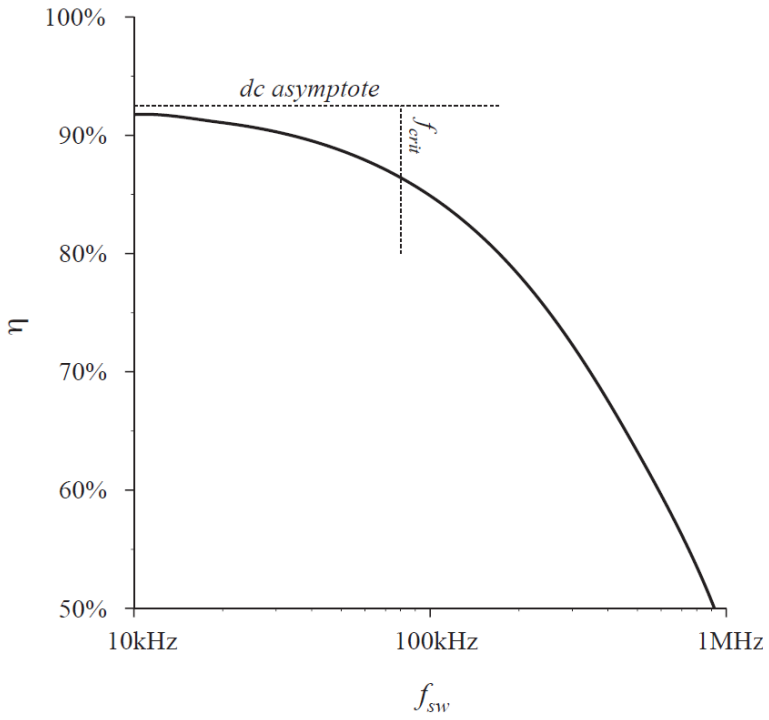



**Fig. 4.9: Efficiency (in %) vs. switching frequency [54]**

On the contrary, PSFB and DAB converters used in this thesis are subjected to soft-switching, meaning that higher switching frequencies can be selected for these converters to reduce the conduction losses. However, *MHz* range switching frequency results in a complicated dynamic response that necessitates relatively complex controllers to compensate [55]. Therefore, a *100 kHz* switching frequency was chosen for both PSFB and DAB converters for a moderate dynamic response, and the designed compensators will be precisely discussed in Chapter 6.

## 4.6 EMI Filter Design

EMI filters are required to avert the high switching reflection in the supply mains. The design parameters remain unchanged despite having two distinct charging infrastructures for household and EV charging applications. However, the same LC-type filter must be installed in all three phases of an EV charging scheme. All the passive elements associated with input filters have been designed according to [56].

$$\boldsymbol{C_{max} = \frac{I_{peak}}{2\pi f_L V_{peak}} tan(\theta)} \qquad (\mathbf{4.78})$$

Here, $I_{peak}$ and $V_{peak}$ are the peak values of the input current and voltage, respectively, $f_L$ is the line frequency, and $\Theta$ refers to the displacement angle between the input voltage and current. The filter capacitor, $C$, at the AC side, must not exceed half the value of $C_{max}$.

The analytical expression for the selection of the filter inductor, $L$, is as follows –

$$\boldsymbol{L = \frac{1}{4\pi^2 {f_c}^2 C}} \qquad (\mathbf{4.79})$$

Here, $f_c$ refers to the cut-off frequency, which is typically one-tenth of the switching frequency of the PFC converter.

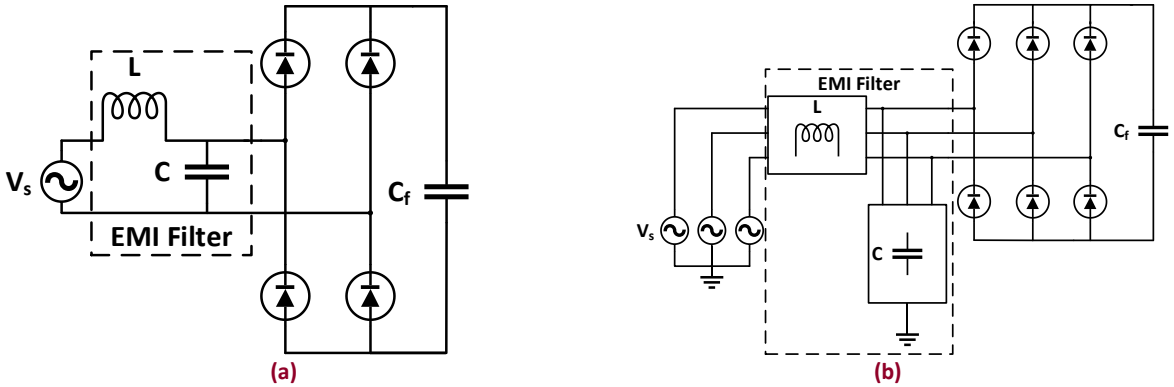



**Fig. 4.10: EMI Filters for (a) single-phase (household) and (b) three-phase (EV) charging systems**

The input filter capacitor, $C_f$, at the DC side, can be selected as the following –

$$\boldsymbol{C_f = C_{max} - C} \qquad (\mathbf{4.80})$$

A more comprehensive line impedance stabilization network (LISN) may be installed for better electromagnetic compatibility (EMC) performance to make the proposed charging solution commercially viable [57] – [62]. However, the design of such LISNs is beyond the scope of the thesis and may be subjected to future works.

## 4.7 Key Points

Table 4.1 and Table 4.2 summarize the key findings of Chapter 4.

**Table 4.1: Voltage and current stresses on different components of the bipolar PFC converter**

| Components | Symbols | Voltage Stress | Current Stress |
|---|---|---|---|
| IGBT | $S$ | $V_{S,rms}\frac{(1+D)}{D'}$ | $(I_{01}-I_{02})\frac{1+D}{D'}$ |
| Diodes | $D_1$, $D_2$ | $V_{S,rms}$ | $I_{01}\frac{D(1+D)}{2D'}-I_{02}\frac{D(1+D)}{2D'}$ |
| | $D_{12}$ | $V_{S,rms}$ | $I_{01}\frac{D(1+D)}{D'}-I_{02}\frac{D(1+D)}{D'}$ |
| | $D_3$ | $V_{S,rms}\frac{D(1+D)}{D'}$ | $[I_{01}(1+D)-I_{02}D]\frac{1}{D'}$ |
| | $D_4$ | $V_{S,rms}\frac{D(1+D)}{D'}$ | $\frac{I_{02}}{D'}$ |
| Inductors | $L_1$, $L_2$ | NA | $I_{01}\frac{D(1+D)}{D'}-I_{02}\frac{D(1+D)}{D'}$ |
| | $L_3$ | | $I_{02}D-I_{01}(1+\mathrm{D})$ |
| | $L_4$ | | $I_{02}$ |
| Capacitors | $C_1$ | $V_{S,rms}(1+D)$ | NA |
| | $C_2$ | $V_{S,rms}\frac{(1+D)}{D'}$ | |
| | $C_3$, $C_4$ | $V_{S,rms}\frac{D(1+D)}{D'}$ | |

It should be noted that the proposed bipolar PFC converter supplies power to two PSFB or DAB converters at a time, meaning that the nominal power of that converter must be twice the power of a PSFB or DAB converter. Therefore, the maximum power rating of the bipolar PFC converter for the household energy storage system is *14.3 kW*, while the rating is *53.95 kW* for the off-board EV charging system. The reactive elements have been calculated according to the analytical expressions derived throughout this chapter.

**Table 4.2: Design parameters of the complete charging system**

| Components | Symbols | Analytical Expression | Chosen Values |
|---|---|---|---|
| Inductors | $L$ | $\frac{1}{4\pi^2 {f_c}^2 C}$ | *5 mH* (Household)<br>*2 mH* (EV) |
| | $L_1$, $L_2$ | $\frac{V_{S,rms} DT}{2\Delta i_{L1,L2}}$ | *10 mH* |
| | $L_3$, $L_4$ | $\frac{V_{S,rms}}{2\Delta i_{L3,L4}} D(1+D)T$ | *10 mH*, *20 mH* |
| | $L_{k1}$, $L_{k2}$ | $\frac{4{\delta_{Tmax}}^2}{\pi^2 (C_{MOS} + C_{TR})}$ | *1 µH* |
| | $L_{11}$, $L_{21}$ | $\frac{4nkV_{DC1,DC2} V_{Bat1,Bat2}(t)}{\pi^3 f_s P_{max}}$ | *16 µH* |
| | $L_{m1}$, $L_{m2}$ | $\frac{4nV_{DC1,DC2} V_{Bat1,Bat2}(t)}{\pi^3 f_s P_{max}}$ | *8 µH* |
| | $L_{01}$, $L_{02}$ | $\frac{\left[nV_{DC1,DC2} - \{V_{Bat1,Bat2}(t) - V_{DC1,DC2}\}\right] D_{eff} T_s}{\Delta i_{L1,L2}}$ | *1 mH* (Household)<br>*5 mH* (EV) |
| Capacitors | $C$ | $< \frac{I_{peak}}{4\pi f_L V_{peak}} tan(\theta)$ | *150 µF* (Household)<br>*600 µF* (EV) |
| | $C_f$ | $\frac{I_{peak}}{2\pi f_L V_{peak}} tan(\theta) - C$ | *300 µF* (Household)<br>*1500 µF* (EV) |
| | $C_1$ | $\frac{I_{01}(1+D) - I_{02}D}{2\Delta v_{C1}} DT$ | *3000 µF* |
| | $C_2$ | $\frac{I_{02}}{2\Delta v_{C2}} DT$ | *3000 µF* |
| | $C_3$ | $\frac{I_{01}}{2\Delta v_{C3}} DT$ | *5600 µF* |
| | $C_4$ | $\frac{D(1+D)}{16} \frac{V_{S,rms} T^2}{\Delta v_{C4} L_4}$ | *5600 µF* |
| | $C_{11}$, $C_{21}$ | $\frac{\pi P_{max}}{16(1+k) n f_s V_{DC1,DC2} V_{Bat1,Bat2}(t)}$ | *100 nF* |
| | $C_{12}$, $C_{22}$ | $\frac{\pi n P_{max}}{16 f_s V_{DC1,DC2} V_{Bat1,Bat2}(t)}$ | *1 µF* |
| | $C_{01}$, $C_{02}$ | $\frac{\left[nV_{DC1,DC2} - \{V_{Bat1,Bat2}(t) - V_{DC1,DC2}\}\right] {D_{eff}}^2 {T_s}^2}{L_{01,02} \Delta v_{dc1,dc2}}$ | *300 µF* (Household)<br>*600 µF* (EV) |

# 5 DYNAMIC MODELING OF THE SYSTEM

## 5.1 Objective

This chapter aims to realize the dynamics of all the converters involved in the charging system, which will be critical while designing the controllers for the mentioned converters. However, deriving small-signal models for higher-order converters is not always straightforward. To address such challenges, some advanced design-oriented tools, such as the switch-averaging technique, extra element theorem (EET), and null double injection, were investigated, which are not trivial.

## 5.2 Averaged Switch Modeling of the Bipolar Converter

According to [63], the switch-averaging technique can obtain transient and frequency responses of any power electronics system of interest. However, the time-invariant network containing converter reactive elements must be separated from the switch network, and the switching ports must be defined to apply such a technique.

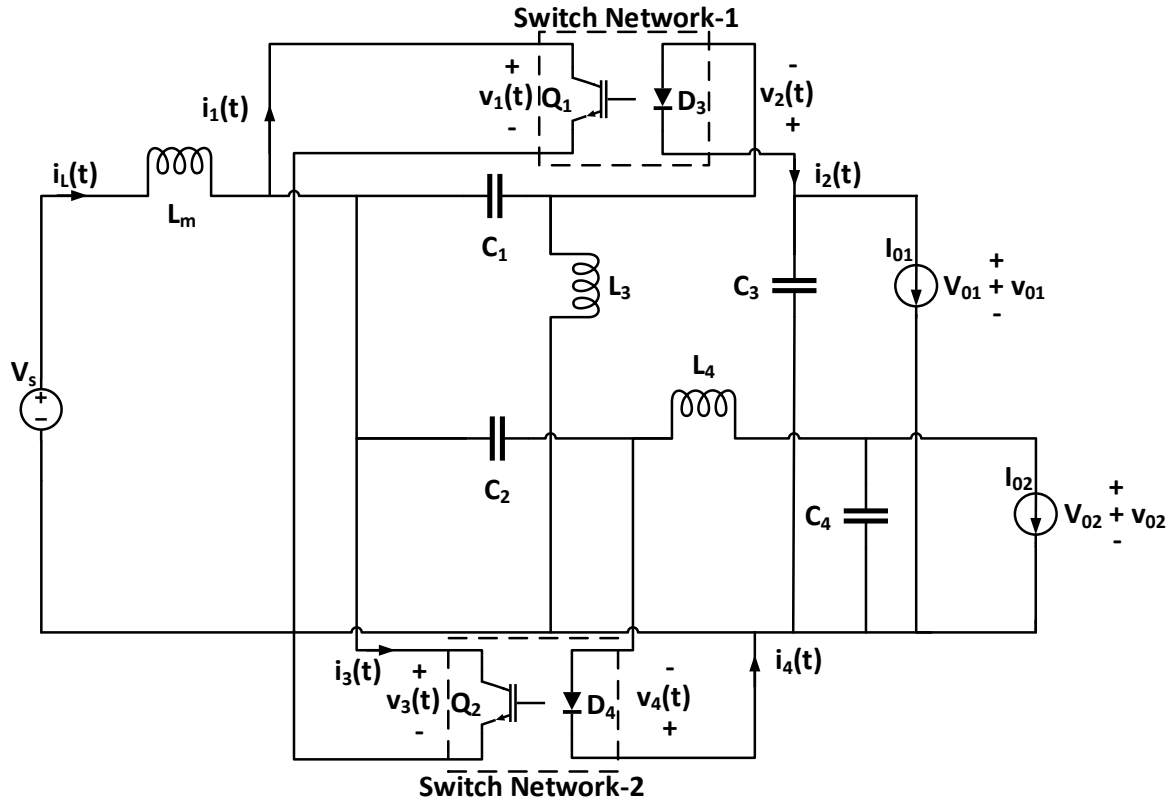



**Fig. 5.1: Remodeled bipolar converter for averaged switch modeling**

Although the front-end bipolar PFC converter has a single switch, for the sake of analysis, that only switch has been realized by two switches connected in parallel, paving the way to obtain two switch networks in accordance with two output diodes, $D_3$ and $D_4$. A single inductor, $L_m$, has replaced the switched-inductor configuration to reduce the complexity of the system. As shown in Fig. 5.1, the remodeled system is now suitable for applying the switch-averaging technique. It should be noted that both switch networks have identical configurations. Therefore, opting for any averaged or linearized model in the case of one will similarly apply to the remaining one.

Fig. 5.2 illustrates the necessary voltage and current waveshapes across the switching ports of the first network.

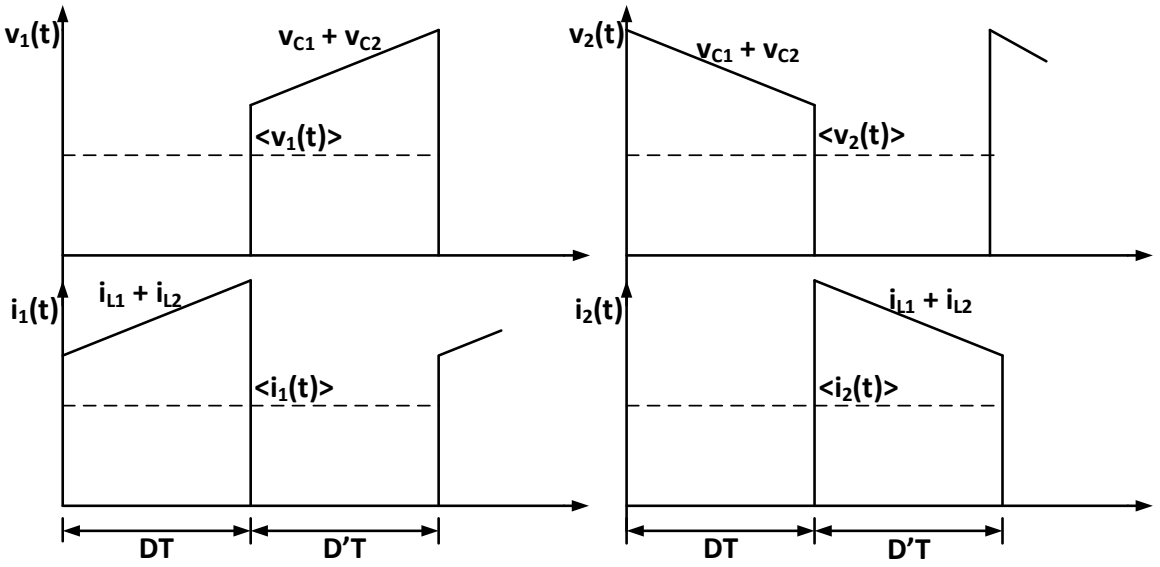



**Fig. 5.2: Voltage and current waveshapes across the switching ports of the first network**

Applying small ripple approximation leads to –

$$\langle v_1(t)\rangle_T = d'(t)[\langle v_{C1}(t)\rangle_T + \langle v_{C2}(t)\rangle_T] \quad (5.1)$$

$$\langle i_1(t)\rangle_T = d(t)[\langle i_{L1}(t)\rangle_T + \langle i_{L2}(t)\rangle_T] \quad (5.2)$$

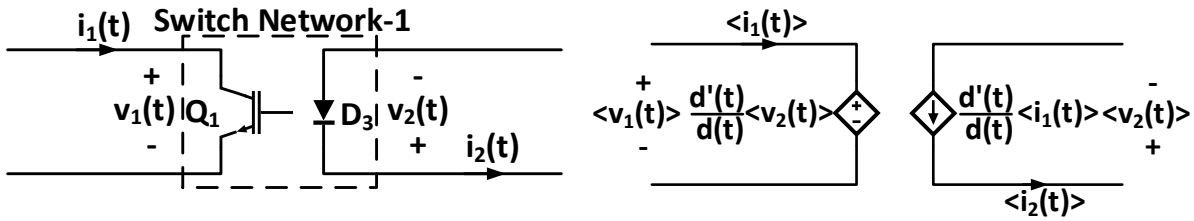
$$\langle v_2(t)\rangle_T = d(t)[\langle v_{C1}(t)\rangle_T + \langle v_{C2}(t)\rangle_T] \quad (5.3)$$

$$\langle i_2(t)\rangle_T = d'(t)[\langle i_{L1}(t)\rangle_T + \langle i_{L2}(t)\rangle_T] \quad (5.4)$$

Combining (5.1), (5.2), (5.3), and (5.4) results in –

$$\langle v_1(t)\rangle_T = \frac{d'(t)}{d(t)}\langle v_2(t)\rangle_T \quad (5.5)$$

$$\langle i_2(t)\rangle_T = \frac{d'(t)}{d(t)}\langle i_1(t)\rangle_T \quad (5.6)$$




(a) (b)

**Fig. 5.3: (a) First switch network and (b) its averaged model**

To obtain the dynamic equations of the switch network, perturbation and linearization of the averaged waveforms are required. Therefore,

$$d(t) = D + \hat{d}(t), \langle v_1(t)\rangle_T = V_1 + \hat{v}_1(t), \langle i_1(t)\rangle_T = I_1 + \hat{\imath}_1(t),$$
$$\langle v_2(t)\rangle_T = V_2 + \hat{v}_2(t), \langle i_2(t)\rangle_T = I_2 + \hat{\imath}_2(t) \quad (5.7)$$

Now, the voltage equation becomes –

$$(D + \hat{d})(V_1 + \hat{v}_1) = (D' - \hat{d})(V_2 + \hat{v}_2) \quad (5.8)$$

Eliminating non-linear terms from (5.8) leads to –

$$(V_1 + \hat{v}_1) = \frac{D'}{D}(V_2 + \hat{v}_2) - \hat{d}\frac{V_1}{DD'} \quad (5.9)$$

Similarly, the current equation becomes –

$$(D + \hat{d})(I_2 + \hat{\imath}_2) = (D' - \hat{d})(I_1 + \hat{\imath}_1) \quad (5.10)$$

Eliminating non-linear terms from (5.10) results in –

$$(I_2 + \hat{\imath}_2) = \frac{D'}{D}(I_1 + \hat{\imath}_1) - \hat{d}\frac{I_2}{DD'} \quad (5.11)$$

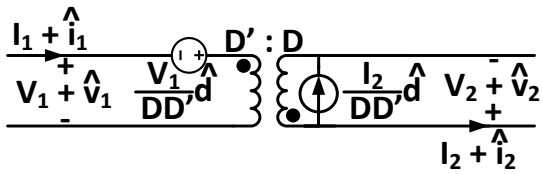



Fig. 5.4: Linearized average model of the first switch network

After replacing the switch networks with their linearized average models, Fig. 5.1 can be redrawn like Fig. 5.5.

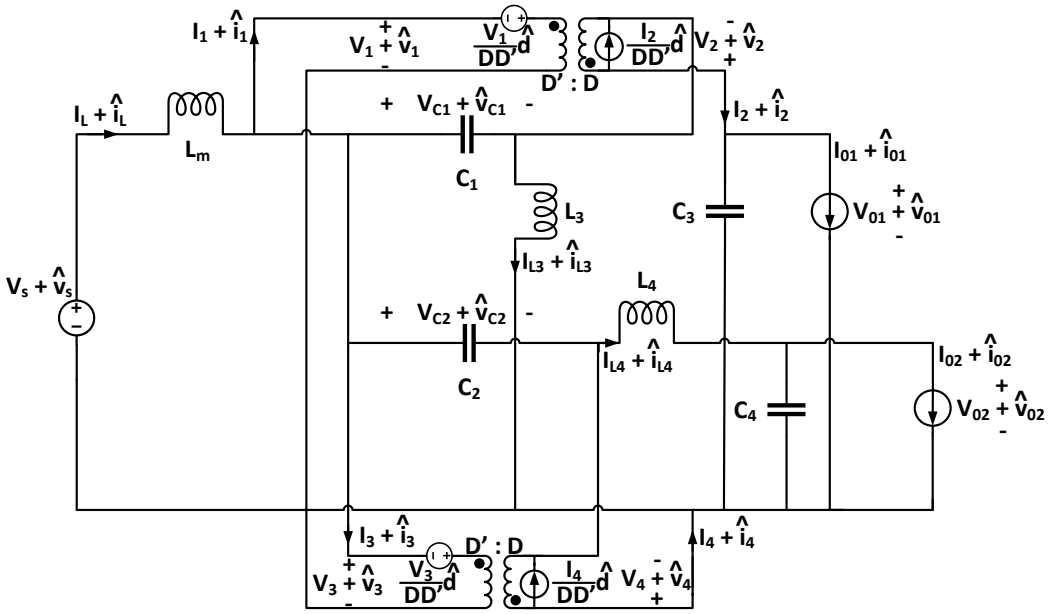



Fig. 5.5: Remodeled bipolar converter with its linearized average switch networks

However, the network depicted in Fig. 5.5, comprising two switch networks, is still complicated in determining the necessary equations for finding appropriate transfer functions. R. D. Middlebrook's extra element theorem (EET) can be applied here to break down the model into two parts, overcoming the hurdles one may face while analyzing the whole model at once. One can assume that the cumulative actions of $V_3$ and $I_4$ sources nullify the Cuk output, $V_{02}$. Hence, only the SEPIC side of Fig. 5.5 remains active for the time being, and the dynamic analysis can be realized using a SEPIC converter analysis. Similarly, the simultaneous acts of $V_1$ and $I_2$ sources nullify the SEPIC output, $V_{01}$, and at that time, the dynamic analysis is limited to the Cuk side. This is the so-called null double injection derived from EET [64].

### 5.2.1 SEPIC Side of the Converter

After applying the null double injection, the linearized average switch model of Fig. 5.5 is reduced to the model shown in Fig. 5.6.

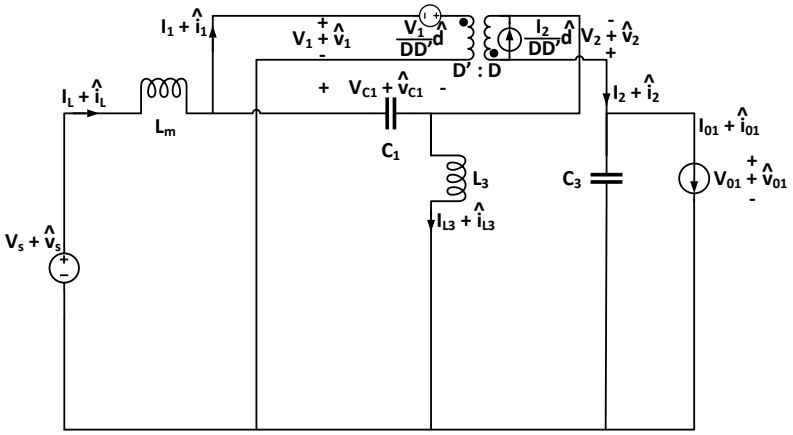



**Fig. 5.6: SEPIC side of the bipolar converter**

It can be noted that the network, illustrated in Fig. 5.6, has two types of input sources. One is the duty cycle input, $d$, while the other is the power input, $v_s$. The superposition theorem can be applied to derive the control-to-output and duty cycle-to-control transfer functions by placing $v_s = 0$, and the line-to-output transfer function by setting $d = 0$.

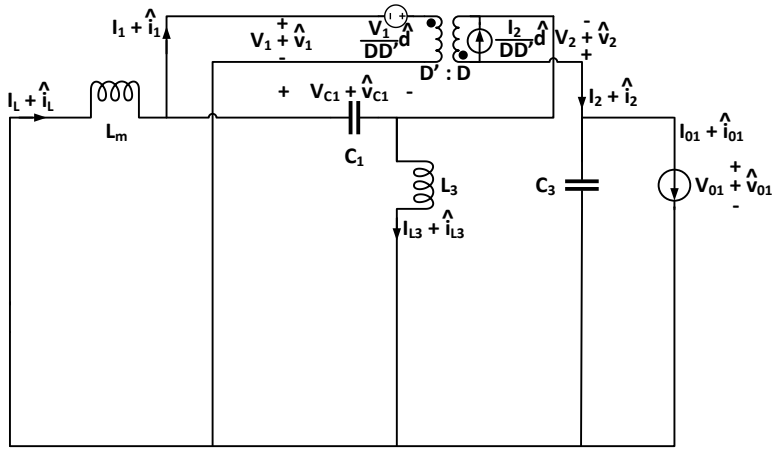



**Fig. 5.7: SEPIC side when $v_s = 0$**

By applying fundamental circuit theorems in the network, shown in Fig. 5.7, one can derive control-to-output, duty cycle-to-control, and duty cycle-to-output transfer functions.

The control-to-output transfer function,

$$G_{vc1}(s) = \frac{\hat{v}_{01}(s)}{\hat{\imath}_1(s)} = -\frac{I_{01}L_m D}{V_{01}C_3 D'} \frac{s^3 - \omega_4 s^2 + \omega_5 s - \omega_6}{s^3 + \omega_1 s^2 + \omega_2 s + \omega_3} \tag{5.12}$$

The duty cycle-to-control transfer function,

$$G_{id1}(s) = \frac{\hat{\imath}_1(s)}{\hat{d}(s)} = \frac{V_{01}}{L_m D} \frac{s^3 + \omega_1 s^2 + \omega_2 s + \omega_3}{s^4 + a_1 s^3 + a_2 s^2 + a_3 s + a_4} \tag{5.13}$$

The duty cycle-to-output transfer function,

$$G_{vd1}(s) = \frac{\hat{v}_{01}(s)}{\hat{d}(s)} = -\frac{I_{01}}{C_3 D'} \frac{s^3 - \omega_4 s^2 + \omega_5 s - \omega_6}{s^4 + a_1 s^3 + a_2 s^2 + a_3 s + a_4} \tag{5.14}$$

Where,

$$\omega_1 = \frac{I_{01}}{V_{01}C_3}\left[1 + D\left(1 + \frac{C_3}{C_1}\right)\right], \omega_2 = \frac{D}{L_3 C_1}\left[1 + \frac{L_3}{C_3}\left(\frac{I_{01}}{V_{01}}\right)^2\right], \omega_3 = \frac{I_{01}}{V_{01}}\frac{2D}{L_3 C_1 C_3},$$
$$\omega_4 = \frac{V_{01}}{I_{01}}\frac{D'^2}{DL_m}\left(1 + \frac{L_m}{L_3}\right), \omega_5 = \frac{D}{L_3 C_1}, \omega_6 = \frac{V_{01}}{I_{01}}\frac{D'^2}{DL_m L_3 C_1},$$
$$a_1 = \frac{I_{01}}{V_{01}C_3}, a_2 = \frac{1}{L_m C_1}\left[\frac{L_m}{L_3}\left(D^2 + \frac{C_1}{C_3}D'^2\right) + D'^2\left(1 + \frac{C_1}{C_3}\right)\right],$$
$$a_3 = \frac{I_{01}}{V_{01}}\frac{1}{L_m C_1 C_3}\left(\frac{L_m}{L_3}D^2 + D'^2\right), a_4 = \frac{D'^2}{L_m L_3 C_1 C_3} \tag{5.15}$$

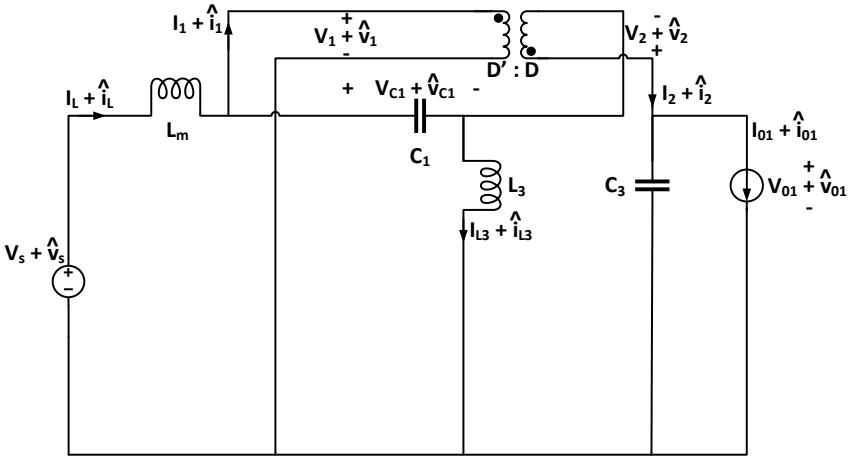



Fig. 5.8: SEPIC side when *d = 0*

Now, according to Fig. 5.8, the line-to-output transfer function,

$$G_{vs1}(s) = \frac{\hat{v}_{01}(s)}{\hat{v}_s(s)} = \frac{b_2 s^2 + b_1 s + b_0}{s^4 + d_3 s^3 + d_2 s^2 + d_1 s + d_0} \tag{5.16}$$

Where,

$$b_0 = \frac{V_s}{C_1C_3L_mL_3}, b_1 = 0, b_2 = \frac{V_s(L_m + L_3)}{C_3L_mL_3}, d_0 = \frac{D'^2}{C_1C_3L_mL_3}, d_1 = \frac{I_{01}}{V_{01}C_1C_3}\left(\frac{D'^2}{L_m} + \frac{D^2}{L_3}\right),$$
$$d_2 = \frac{D^2(C_1 + C_3)(L_m + L_3) - (2D - 1)(C_1L_m + C_1L_3 + C_3L_3)}{C_1C_3L_mL_3}, d_3 = \frac{I_{01}}{V_{01}C_3} \quad (5.17)$$

### 5.2.2 Cuk Side of the Converter

When the cumulative effects of $V_1$ and $I_2$ sources null the SEPIC output, $V_{01}$, Fig. 5.5 can be realized by a reduced model, shown in Fig. 5.9.

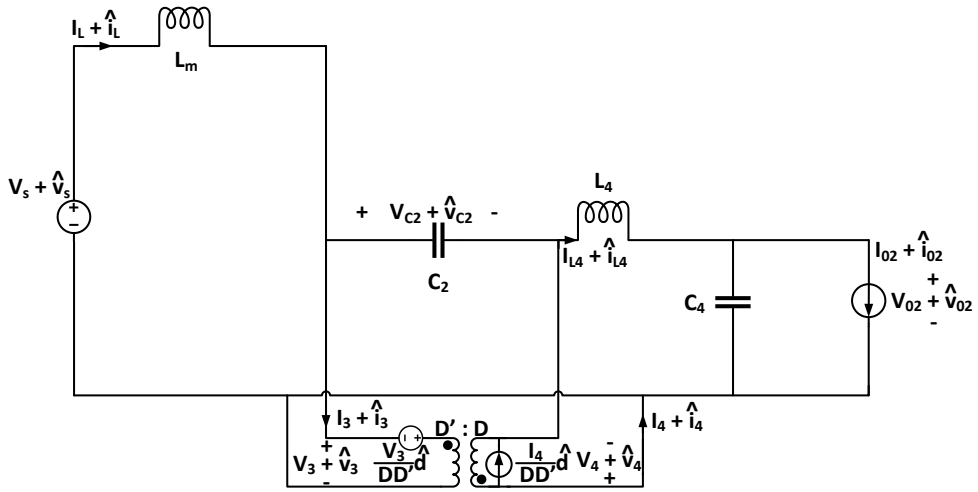



Fig. 5.9: Cuk side of the bipolar converter

The superposition theorem can also be applied to Fig. 5.9 to derive the necessary transfer functions of the Cuk side. Firstly, the source input, $V_s$, will be set to zero to find the transfer functions associated with the duty cycle input. Then, the duty cycle input, $d$, will be set to zero to derive the line-to-output transfer function.

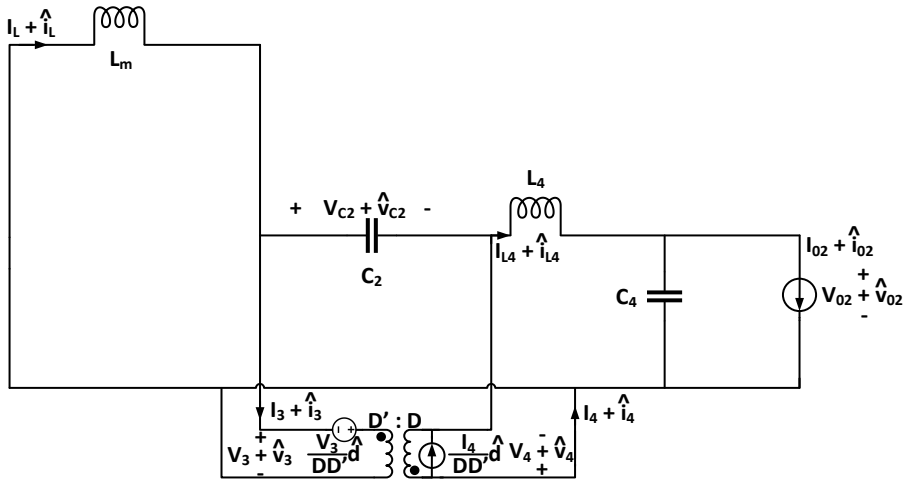



Fig. 5.10: Cuk side when $v_s = 0$

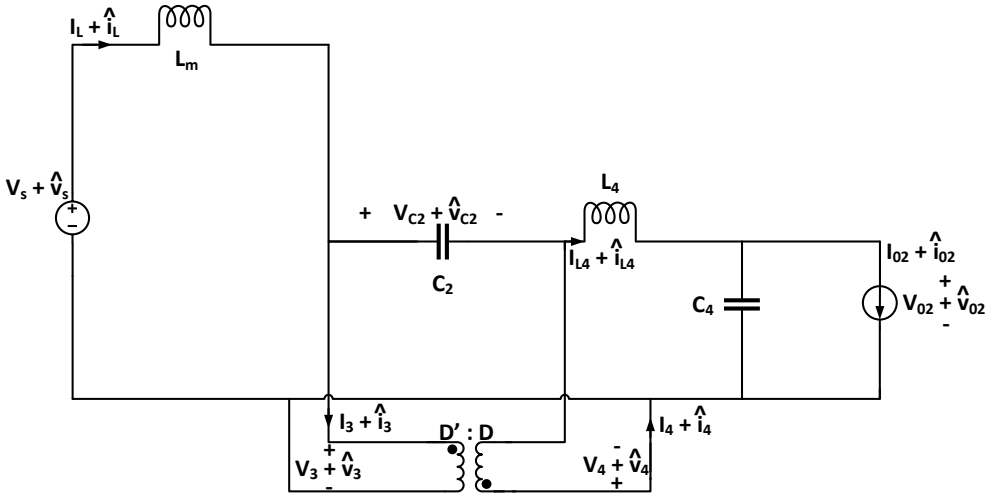



**Fig. 5.11: Cuk side when *d = 0***

The duty cycle-to-output transfer function,

$$G_{vd2}(s) = \frac{\hat{v}_{02}(s)}{\hat{d}(s)} = -\frac{V_{02}}{DD'}\frac{c_2 s^2 - c_1 s + c_0}{k_4 s^4 + k_3 s^3 + k_2 s^2 + k_1 s + k_0} \quad (5.18)$$

The line-to-output transfer function,

$$G_{vs2}(s) = \frac{\hat{v}_{02}(s)}{\hat{v}_s(s)} = -\frac{D}{D'}\frac{1}{k_4 s^4 + k_3 s^3 + k_2 s^2 + k_1 s + k_0} \quad (5.19)$$

Where,

$$c_0 = 1, c_1 = \frac{D^2 L_m I_{02}}{D'^2 V_{02}}, c_2 = \frac{L_m C_2}{D'}, k_0 = 1, k_1 = \frac{L_4 I_{02}}{V_{02}} + \frac{D^2 L_m I_{02}}{D'^2 V_{02}},$$
$$k_2 = \frac{L_m C_2}{D'^2} + L_4 C_4 + \frac{D^2 L_m C_4}{D'^2}, k_3 = \frac{L_m L_4 C_2 I_{02}}{D'^2 V_{02}}, k_4 = \frac{L_m L_4 C_2 C_4}{D'^2} \quad (5.20)$$

By eliminating all the insignificant quantities, according to [65], the control-to-output transfer function becomes –

$$G_{vc2}(s) = \frac{\hat{v}_{02}(s)}{\hat{i}_3(s)} = \frac{V_{02}}{I_{02} + sV_{02}C_4} \quad (5.21)$$

The duty cycle-to-control transfer function,

$$G_{id2}(s) = \frac{\hat{i}_3(s)}{\hat{d}(s)} = \frac{\hat{v}_{02}(s)}{\hat{d}(s)} \times \frac{\hat{i}_3(s)}{\hat{v}_{02}(s)} = \frac{G_{vd2}(s)}{G_{vc2}(s)} \quad (5.22)$$

### 5.2.3 Input Side of the Converter

The input inductor, $L_m$, is shared by both the SEPIC and Cuk sides of the bipolar converter, as depicted in Fig. 5.5. Therefore, the SEPIC input current, $i_1$, and the Cuk input current, $i_3$, result in the inductor current, $i_L$.

$$\hat{\boldsymbol{i}}_{\boldsymbol{L}}(\boldsymbol{s}) = \hat{\boldsymbol{i}}_{\boldsymbol{1}}(\boldsymbol{s}) + \hat{\boldsymbol{i}}_{\boldsymbol{3}}(\boldsymbol{s}) \tag{5.23}$$

Now, according to the principle of linear time-invariant (LTI) system to design lead-lag compensators [66], the combined duty cycle-to-control transfer function,

$$\boldsymbol{G}_{\boldsymbol{id}}(\boldsymbol{s}) = \frac{\hat{\boldsymbol{i}}_{\boldsymbol{L}}(\boldsymbol{s})}{\hat{\boldsymbol{d}}(\boldsymbol{s})} = \boldsymbol{G}_{\boldsymbol{id1}}(\boldsymbol{s}) + \boldsymbol{G}_{\boldsymbol{id2}}(\boldsymbol{s}) \tag{5.24}$$

## 5.3 Small-Signal Modeling of Single/Dual Active Bridge Converters

According to [67], small-signal models of any phase-shift modulated converters can be derived from a typical buck topology.

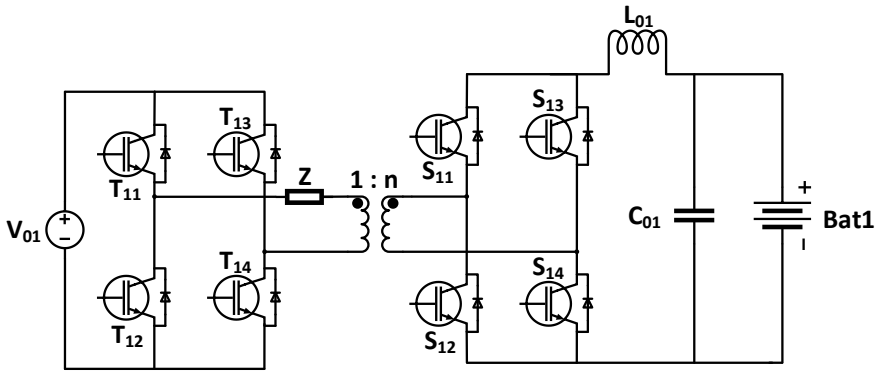



**Fig. 5.12: A simplified dual active bridge converter**

In Fig. 5.12, the impedance, *Z*, represents any reactive elements between two bridges. For PSFB converters, *Z* refers to the leakage inductors $L_{k1}$ and $L_{k2}$, whereas for DAB converters, it refers to CLLC resonant tank circuits.

The effective duty cycle of the network, shown in Fig. 5.12, is as follows –

$$\boldsymbol{d}_{\boldsymbol{eff}} = \hat{\boldsymbol{d}}_{\boldsymbol{eff}} + \boldsymbol{D}_{\boldsymbol{eff}} \tag{5.25}$$

The time delay to increase the secondary voltage in association with the increase in charging current, $\hat{\imath}_b$, can be calculated as –

$$\Delta \boldsymbol{t} = \boldsymbol{2n}\hat{\boldsymbol{i}}_{\boldsymbol{b}}\frac{\boldsymbol{Z}}{\boldsymbol{\omega}_{\boldsymbol{s}}\boldsymbol{V}_{\boldsymbol{01}}} \tag{5.26}$$

The change in effective duty cycle because of this effect,

$$\hat{\boldsymbol{d}}_{\boldsymbol{i}} = -\frac{\Delta \boldsymbol{t}}{\boldsymbol{T}_{\boldsymbol{s}}/\boldsymbol{2}} = -\frac{\boldsymbol{4nZf}_{\boldsymbol{s}}}{\boldsymbol{\omega}_{\boldsymbol{s}}\boldsymbol{V}_{\boldsymbol{01}}}\hat{\boldsymbol{i}}_{\boldsymbol{b}} = -\frac{\boldsymbol{A}}{\boldsymbol{nV}_{\boldsymbol{01}}}\hat{\boldsymbol{i}}_{\boldsymbol{b}} \tag{5.27}$$

Here, $\omega_s$, $f_s$, and $T_s$ are the converter switching frequency in radian, switching frequency in hertz, and time period, respectively. And, $A = \frac{4n^2 Z f_s}{\omega_s}$.

When an increasing input voltage perturbs the steady-state operation, the current slope at the primary side will increase to reach the reflected charging current faster than that of an unperturbed operation. As a result, the resultant duty cycle on the secondary side will increase. Thus, the change of effective duty cycle as a function of the increasing input voltage can be calculated as –

$$\Delta t = n\left(2I_b - \frac{V_b}{L_{01}}D'\frac{T_s}{2}\right)\left(\frac{Z}{\omega_s V_{01}} - \frac{Z}{\omega_s(V_{01}+\hat{v}_{01})}\right) \tag{5.28}$$

$$\Delta t = n\left(2I_b - \frac{V_b}{L_{01}}D'\frac{T_s}{2}\right)\frac{Z}{\omega_s V_{01}(V_{01}+\hat{v}_{01})}\hat{v}_{01} \tag{5.29}$$

Under the small-signal assumption,

$$\Delta t = n\left(2I_b - \frac{V_b}{L_{01}}D'\frac{T_s}{2}\right)\frac{Z}{\omega_s {V_{01}}^2}\hat{v}_{01} \tag{5.30}$$

Now, the change in effective duty cycle by this effect can be calculated as the following –

$$\hat{d}_v = \frac{\Delta t}{T_s/2} = \left(I_b - \frac{V_b}{L_{01}}D'\frac{T_s}{4}\right)\frac{4nZf_s}{\omega_s {V_{01}}^2}\hat{v}_{01} \tag{5.31}$$

The complementary duty cycle, *D'*, should be small enough to mitigate the conduction losses because of the circulating currents at the converter primary side that results in neglecting the term when the converter operation is subjected to deep continuous conduction mode (CCM) [50]. Hence,

$$\hat{d}_v = \frac{4nZf_s I_b}{\omega_s {V_{01}}^2}\hat{v}_{01} = \frac{AI_b}{n{V_{01}}^2}\hat{v}_{01} \tag{5.32}$$

Finally, the total change in the effective duty cycle becomes –

$$\hat{d}_{eff} = \hat{d} + \hat{d}_i + \hat{d}_v \tag{5.33}$$

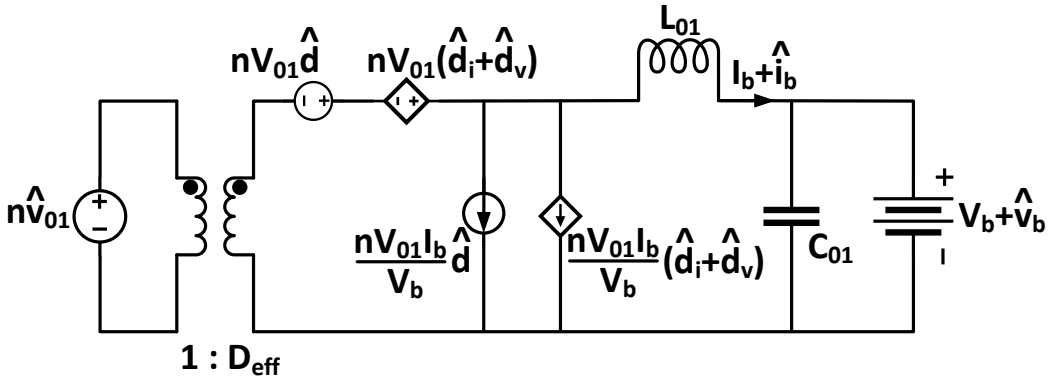



**Fig. 5.13: Small-signal model of general phase-shift modulated converters**

Fig. 5.13 represents the small-signal model of general phase-shift modulated converters derived from (5.25) – (5.33).

The duty cycle-to-output transfer function,

$$\boldsymbol{G_{i_b d}(s) = \frac{\hat{i}_b(s)}{\hat{d}_{eff}(s)} = nV_{01}k_{id}\frac{1+\frac{s}{\omega_z}}{\frac{s^2}{{\omega_p}^2}+\frac{s}{Q\omega_p}+1}} \quad (5.34)$$

Where,

$$\boldsymbol{k_{id} = \frac{I_b}{V_b + AI_b}, \omega_z = \frac{I_b}{V_b C_{01}}, \omega_p = \sqrt{\frac{AI_b}{V_b L_{01} C_{01}} + \frac{1}{L_{01} C_{01}}}, Q = \frac{1}{\omega_p}\frac{A+\frac{V_b}{I_b}}{AC_{01}\frac{V_b}{I_b}+L_{01}}} \quad (5.35)$$

For the PSFB converter, illustrated in Fig. 4.7, $Z = \omega_s L_{k1}$, while for the DAB converter, depicted in Fig. 4.8, $Z = \frac{1}{\omega_s C_{11}} + \omega_s L_{11} + \frac{1}{n^2 \omega_s C_{12}}$.

## 5.4 Key Points

Among all the derived expressions in this chapter, the transfer functions of interest have been presented in Table 5.1. It should be noted that these transfer functions will be considered while designing the controllers for the respective converters in Chapter 6.

**Table 5.1: Converters' transfer functions**

| Transfer Function Names | Symbols | Equation No. |
|---|---|---|
| SEPIC side control-to-output | $G_{vc1}(s)$ | (5.12) |
| Cuk side control-to-output | $G_{vc2}(s)$ | (5.21) |
| Combined duty cycle-to-control | $G_{id}(s)$ | (5.24) |
| PSFB/DAB duty cycle-to-output | $G_{ibd}(s)$ | (5.34) |

# 6 CONTROLLER DESIGN

## 6.1 Objective

The main objective of this chapter is to design lead-lag compensators for the associated control systems of the converters of interest with the help of relevant transfer functions derived in Chapter 5. In addition, the control method used in this thesis will be explicitly explained. Lastly, the discrepancy between the analytically found compensator transfer functions and the actual transfer functions used in the complete charging system design will be adequately justified.

## 6.2 Bipolar PFC Converter Control

The front-end bipolar PFC converter in the thesis is responsible for improving the power quality. The converter provides bipolar DC-link voltages that can be fed as inputs to ultra-fast DC-DC charging converters. Fig. 6.1 represents the control mechanism of the bipolar PFC converter in a block diagram.

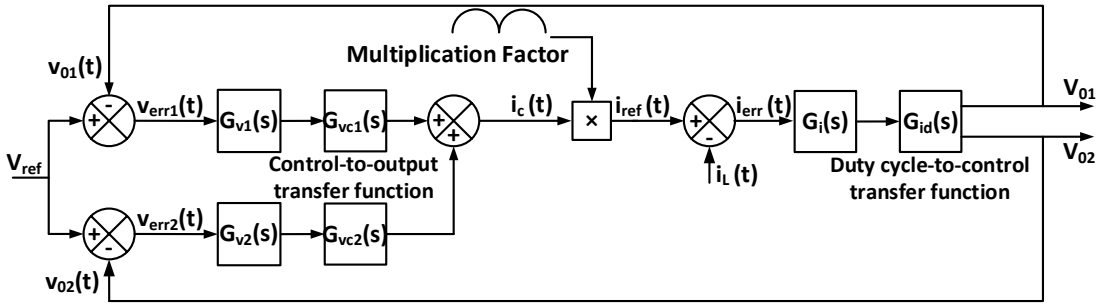



Fig. 6.1: Block diagram of the bipolar PFC converter control

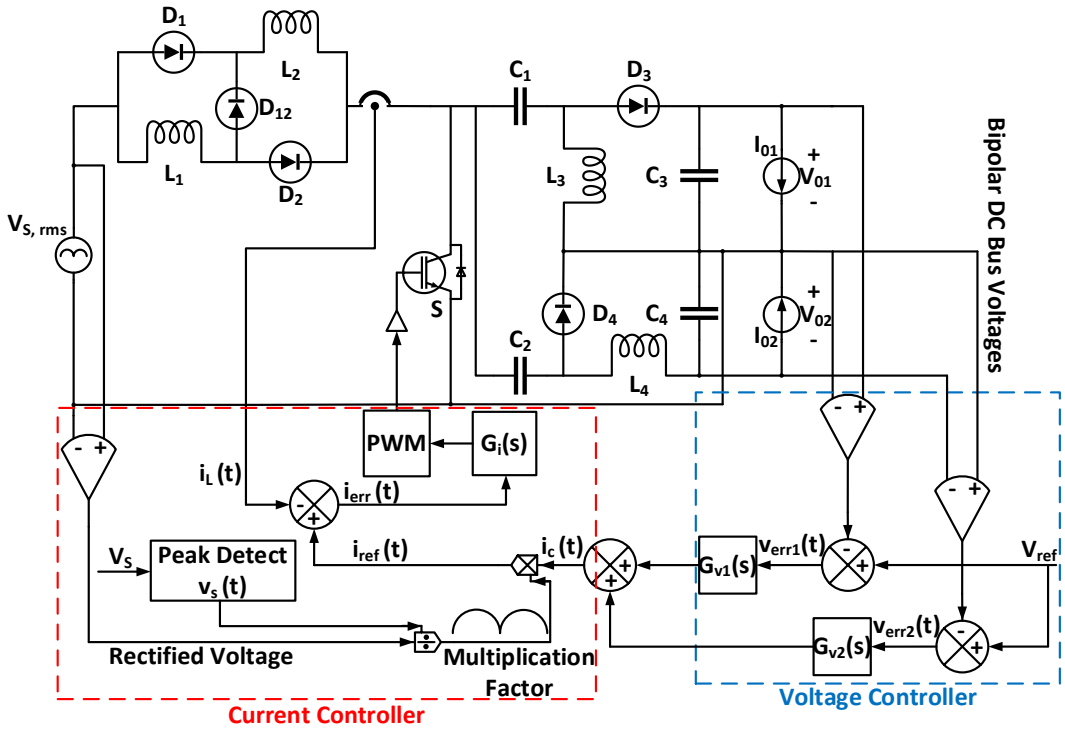



Fig. 6.2: Control system of the bipolar PFC converter

Fig. 6.2 illustrates the complete control system of the bipolar PFC converter. The instantaneous DC bus voltages are compared with a reference set point, $V_{ref}$, generating two error signals. These error signals pass through two voltage compensators. The compensated signals are then summed up and associated with a multiplication factor. The multiplication factor in question persistently tracks the power drawn from the mains with the help of a peak-detecting signal, thus ensuring PFC control [68]. The resultant signal, $i_{ref}(t)$, is compared with the instantaneous switched-inductor current to generate another error signal, which goes through the current compensator. The compensated current signal finally generates the necessary pulse-width modulation (PWM) signals for the gate driver. This is the so-called average current mode (ACM) control [69]. It is noticeable that there are two voltage compensators and one current compensator in the PFC control stage.

### 6.2.1 Designing the Current Compensator

The first step of any ACM-controlled converter is to design the current compensator, for which the transfer function of interest is the duty cycle-to-control transfer function, $G_{id}(s)$. Fig. 6.3 illustrates both the uncompensated and compensated frequency responses of $G_{id}(s)$.

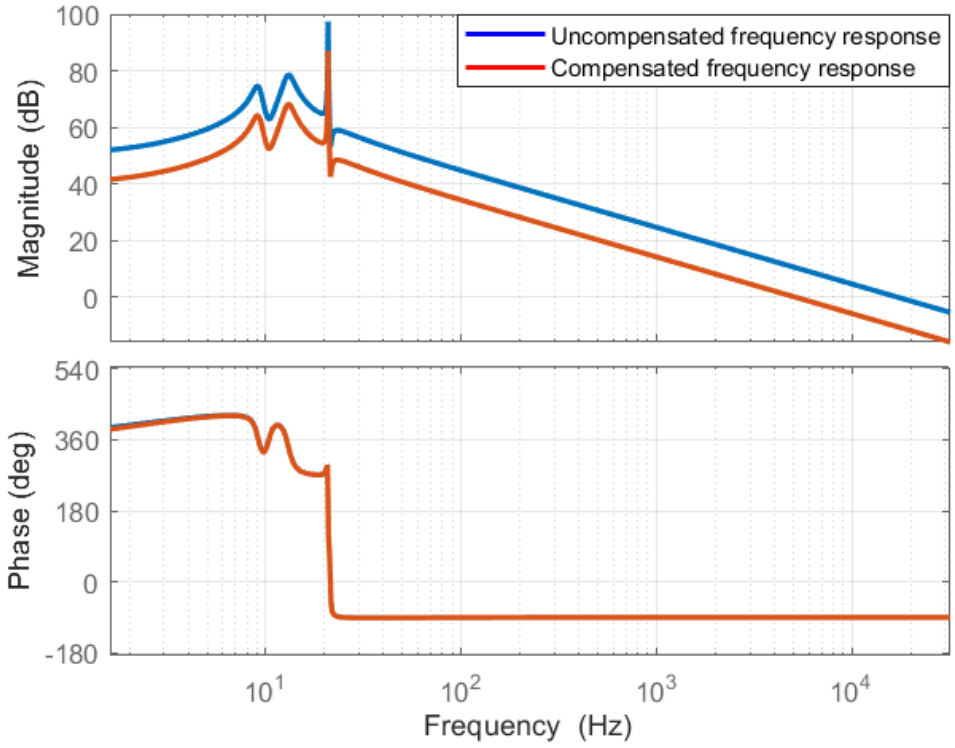



**Fig. 6.3: Frequency response of the duty cycle-to-control transfer function**

As seen in Fig. 6.3, the uncompensated gain crossover frequency is *17 kHz*, and the corresponding phase value is *-90* degrees. Therefore, the phase margin, which is the difference between the phase at crossover frequency and the *±180* degree axis, becomes *90* degrees. According to the phase margin test, the open-loop system remains stable and has an adequate phase margin, eliminating the need for any lead compensator, i.e., proportional-derivative (PD) [70]. However, a lag compensator, such as the proportional-integral (PI) compensator, is still required to shift the crossover frequency to *5 kHz*, which is one-tenth of the switching frequency, *50 kHz* [69]. A PI compensator of proportional gain, $k_p = 0.3$, and integral gain, $k_i = 0.25$, satisfies the mentioned criteria.

### 6.2.2 Designing the SEPIC Side Voltage Compensator

After the current compensator is designed, the remaining voltage compensators can also be designed in the same manner. While designing the SEPIC side voltage compensator, one must consider the SEPIC side control-to-output transfer function, $G_{vc1}(s)$. Fig. 6.4 depicts the uncompensated and compensated frequency responses of $G_{vc1}(s)$.

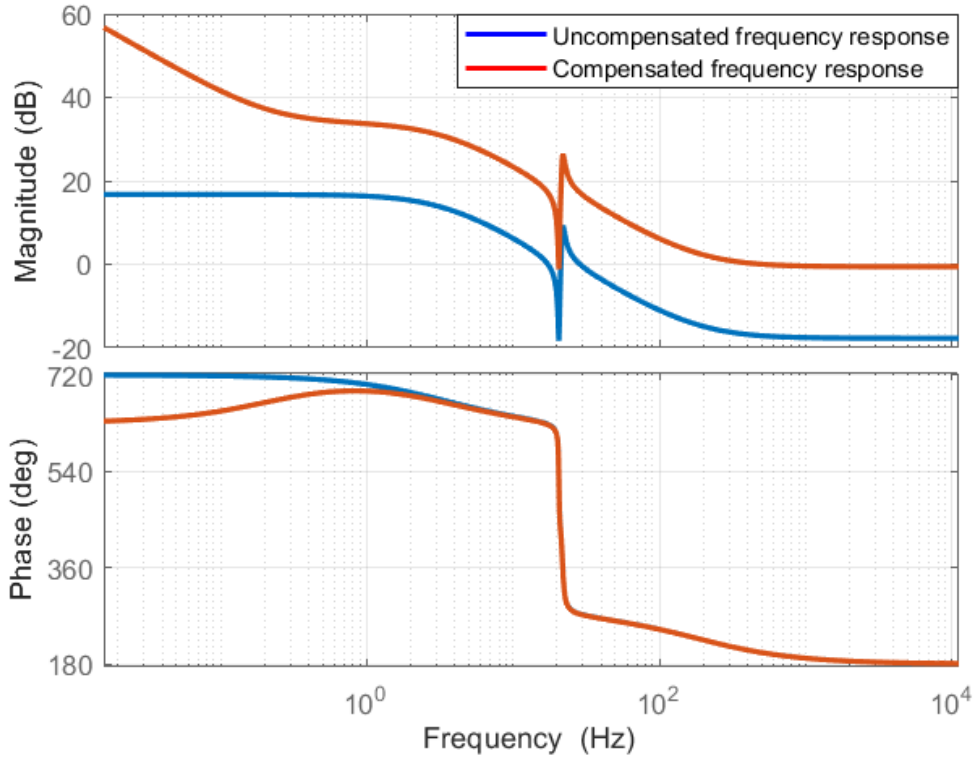



**Fig. 6.4: Frequency response of the SEPIC side control-to-output transfer function**

As seen in Fig. 6.4, the uncompensated gain crossover frequency is *17 Hz*, and the corresponding phase value is *270* degrees. Therefore, the phase margin, which is the difference between the phase at crossover frequency and the *±180* degree axis, becomes *90* degrees. According to the phase margin test, the open-loop system remains stable and has an adequate phase margin, eliminating the need for any lead (PD) compensator [70]. However, a lag (PI) compensator is still needed to shift the crossover frequency to *500 Hz*, which is one-tenth of the crossover frequency of the compensated duty cycle-to-control transfer function, $G_{id}(s)$, *5 kHz* [69]. A PI compensator of proportional gain, $k_p = 7.2$, and integral gain, $k_i = 10$, satisfies the mentioned criteria.

### 6.2.3 Designing the Cuk Side Voltage Compensator

The same methodology can be used to design the Cuk side voltage compensator. Nonetheless, the Cuk side control-to-output transfer function, $G_{vc2}(s)$, must be considered. Fig. 6.5 shows both the uncompensated and compensated frequency responses of $G_{vc2}(s)$. As seen in Fig. 6.5, the uncompensated gain crossover frequency is *28.4 Hz*, and the corresponding phase value is *-86.7* degrees. Therefore, the phase margin, which is the difference between the phase at crossover frequency and the *±180* degree axis, becomes *93.3* degrees. According to the phase margin test, the open-loop system remains stable and has an adequate phase margin, eliminating the need for any lead

(PD) compensator [70]. However, a lag (PI) compensator is still needed to shift the crossover frequency to *500 Hz*, which is one-tenth of the crossover frequency of the compensated duty cycle-to-control transfer function, $G_{id}(s)$, *5 kHz* [69]. A PI compensator of proportional gain, $k_p = 17.7$, and integral gain, $k_i = 10$, satisfies the mentioned criteria.

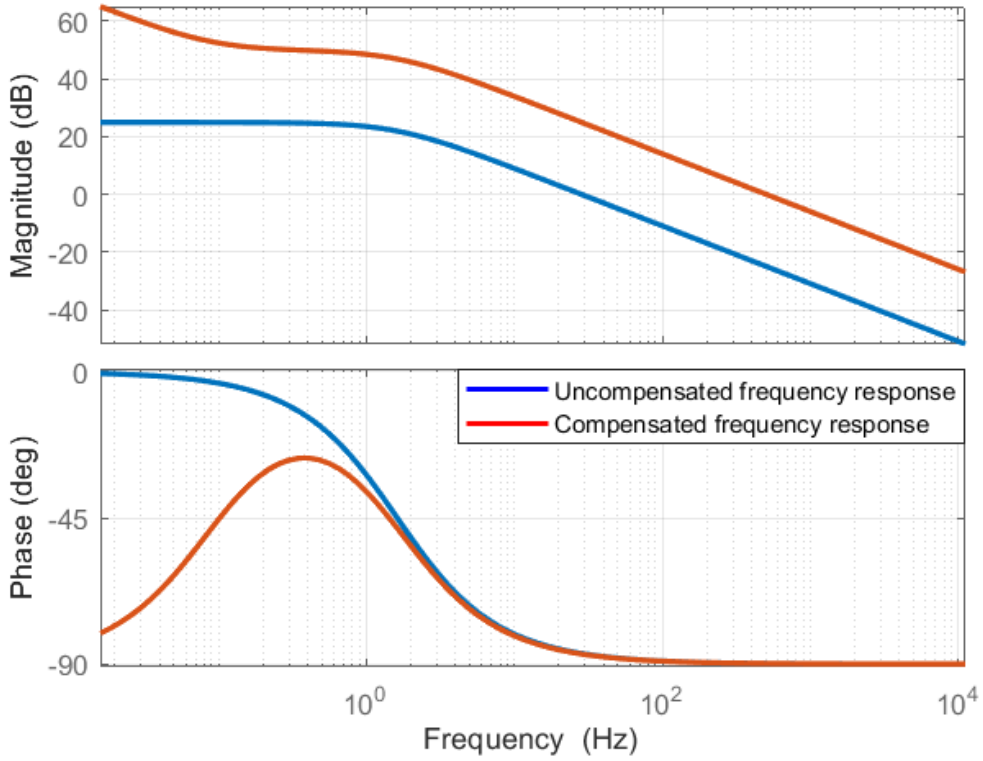



**Fig. 6.5: Frequency response of the Cuk side control-to-output transfer function**

## 6.3 PSFB and DAB Converters Control

Batteries are interfaced with the electric system through PSFB and DAB converters. So, the conventional CC-CV control strategy has been implemented along with these converters' control systems. The operating principles of how these converters were controlled have already been discussed in Subsections 3.2.1 and 3.3.1. However, the focal point of Section 6.3 is to design the necessary compensators and implement the CC-CV algorithm inside the voltage compensators.

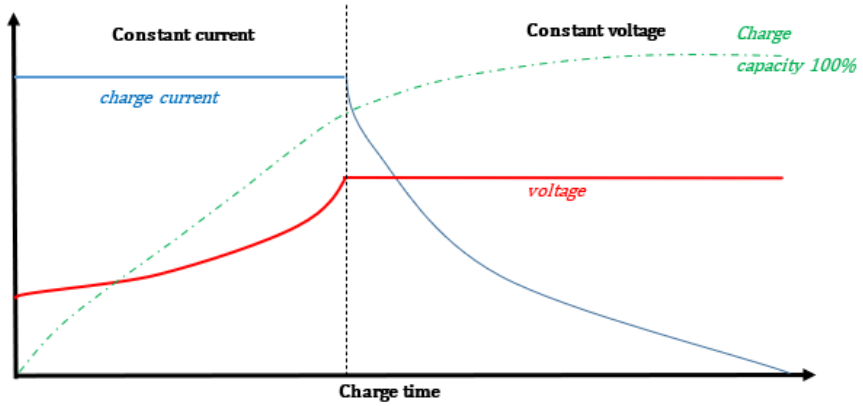



**Fig. 6.6: CC-CV mode of operation**

### 6.3.1 Designing the CV Mode Compensator for both the PSFB and DAB Converters

Fig. 6.6 illustrates the typical constant-current and constant-voltage (CC-CV) mode of operation.

$$Current = \begin{cases} Maximum\ charging\ current, if\ V_{bat} < V_{max} \\ \left(k_p + k_i \frac{1}{s}\right)(V_{max} - V_{bat}), \quad if\ V_{bat} \geq V_{max} \end{cases} \quad (\mathbf{6.1})$$

Where,

$V_{max}$ is the maximum allowed battery voltage.

$V_{bat}$ is the instantaneous battery voltage.

$k_p$ and $k_i$ are the controller's proportional and integral gain parameters, respectively.

As depicted in Fig. 3.4 and 3.5, a logic controller unit decides the operating mode. Until the instantaneous battery voltage reaches a preset maximum voltage setpoint, both the converters are controlled by a reference current, $i_{ref,\ CC}$, thereby charging the batteries in the constant-current (CC) mode. As soon as the battery voltage reaches the maximum voltage setpoint, the converters in question are controlled by a gradually decreasing reference current, $i_{ref,\ CV}$, thus activating the constant-voltage (CV) mode. The timely changing reference current is generated according to (6.1) when the CV mode is activated. Hence, the voltage compensator, $G_c(s)$, keeps the battery terminal voltage constant at a higher state of charge (SOC) by persistently reducing the charging current reference. The dynamic models of the associated batteries are beyond the scope of the thesis. As a result, the voltage compensator, $G_c(s)$, was designed according to the Ziegler-Nichols (ZN) approach presented in [71]. However, the ZN approach involves a so-called critical gain at which the output of the control loop starts oscillating. An optimal critical gain was determined with the help of the Routh-Hurwitz criterion [70][72]. Finally, a PI compensator of proportional gain, $k_p = 100$, and integral gain, $k_i = 10$, has been optimized for the best performance. It is noticeable from Fig. 3.5 that the DAB converter control system comprises two logical operators. The additional logic controller determines the charging or discharging mode of operation, deciding which active bridge to control.

### 6.3.2 Designing the CC Mode Compensator for the PSFB Converter

The same methodology used in Subsections 6.2.1, 6.2.2, and 6.2.3 can be used to design the CC mode compensators for both the PSFB and DAB converters. However, the PSFB and DAB duty cycle-to-output transfer functions, $G_{ibd}(s)$, must be considered. In order to design the compensator for the PSFB converter, only the PSFB duty cycle-to-output transfer function needs to be considered. Fig. 6.7 shows both the uncompensated and compensated frequency responses of $G_{ibd}(s)$. As seen in Fig. 6.7, the uncompensated gain crossover frequency is *11.2 kHz,* and the corresponding phase value is *-90* degrees. Therefore, the phase margin, which is the difference between the phase at crossover frequency and the *±180* degree axis, becomes *90* degrees. According to the phase margin test, the open-loop system remains stable and has an adequate phase margin, eliminating the need for any lead (PD) compensator [70]. However, a lag (PI) compensator is still needed to shift the crossover frequency to *10 kHz*, which is one-tenth of the switching frequency, *100 kHz* [73]. A PI compensator of proportional gain, $k_p = 0.9$, and integral gain, $k_i = 10$, satisfies the mentioned criteria.

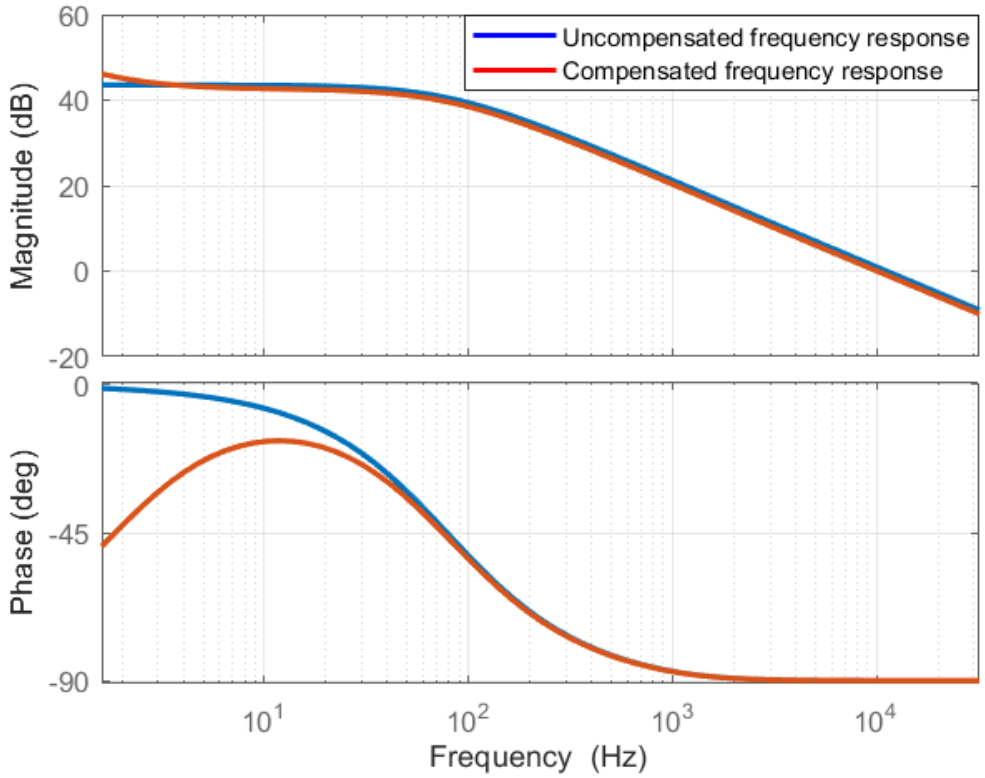



Fig. 6.7: Frequency response of the PSFB duty cycle-to-output transfer function

### 6.3.3 Designing the CC Mode Compensator for the DAB Converter

At this point, the transfer function of interest is the DAB duty cycle-to-output transfer function.

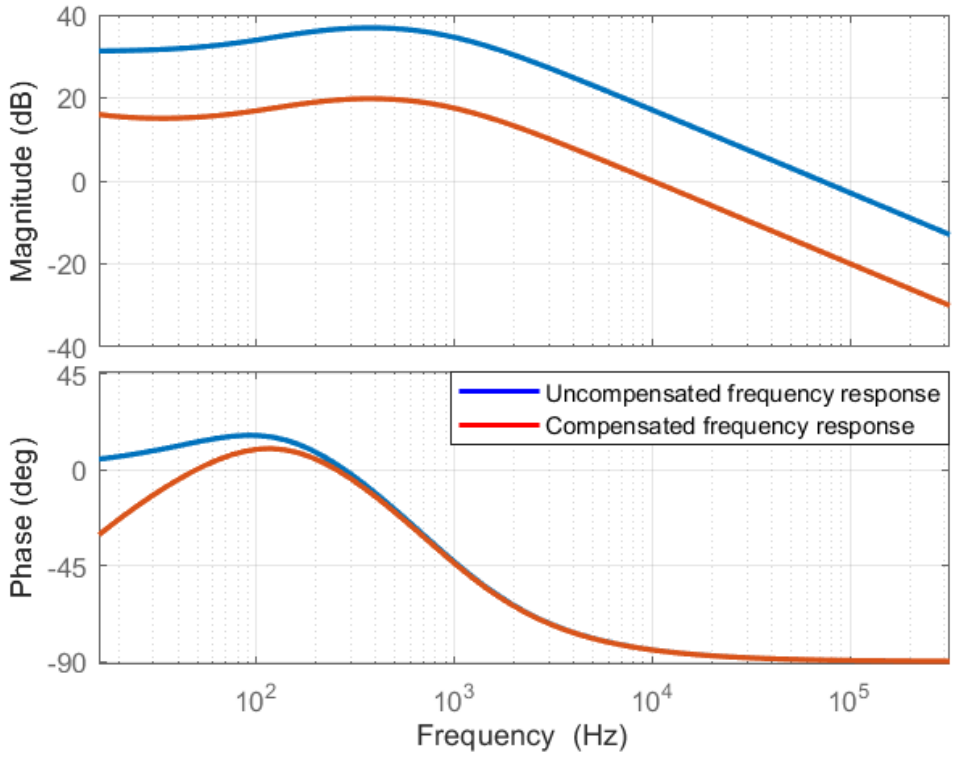



Fig. 6.8: Frequency response of the DAB duty cycle-to-output transfer function

Fig. 6.8 depicts both the uncompensated and compensated frequency responses of $G_{ibd}(s)$. As noticed in Fig. 6.8, the uncompensated gain crossover frequency is *71.4 kHz*, and the corresponding phase value is *-89.2* degrees. Therefore, the phase margin, which is the difference between the phase at crossover frequency and the *±180* degree axis, becomes *90.8* degrees. According to the phase margin test, the open-loop system remains stable and has an adequate phase margin, eliminating the need for any lead (PD) compensator [70]. However, a lag (PI) compensator is still required to shift the crossover frequency to *10 kHz*, which is one-tenth of the switching frequency, *100 kHz* [73]. A PI compensator of proportional gain, $k_p = 0.14$, and integral gain, $k_i = 10$, satisfies the mentioned criteria.

## 6.4 Discrepancies Between Analytical and Practical Compensators

The designed compensators so far are solely based on the analytically found transfer functions by perturbing and linearizing the circuit quantities. It should be noted that the complete charging system has additional reactive elements, i.e., EMI filters and switched-inductors, which were discarded to simplify the dynamic modeling. On top of that, all these reactive elements have parasitic resistances, too. Nevertheless, such omitted elements have distinct dynamic responses, which may affect the designed controllers. It can be regarded as a drawback of such design-oriented tools. However, they always provide a good approximation, facilitating the design procedures by leading the designers toward a proper direction. At this point, the challenge is to tweak the controllers that have already been designed according to the physical system. One way around this is to introduce damping circuits to the EMI filters so that they no longer affect the already designed controllers [74]. Alternatively, one may go through a trial-and-error process to come up with the optimized parameters for the physical system. The latter methodology was adopted in the context of the thesis. However, incorporating the ZN technique also accelerates the process of finding such optimized parameters [71].

## 6.5 Key Points

Table 6.1 summarizes the key findings of Chapter 6, including the analytically found and optimized compensators' transfer functions.

**Table 6.1: Compensators' transfer functions**

| Compensator Names | Symbols | Analytically Found Transfer Functions | Actual Transfer Functions |
|---|---|---|---|
| Current Compensator | $G_i(s)$ | $\frac{3}{10}+\frac{1}{4s}$ | $10+\frac{1}{4s}$ |
| SEPIC Side Voltage Compensator | $G_{v1}(s)$ | $\frac{36}{5}+\frac{10}{s}$ | $\frac{1}{4}+\frac{10}{s}$ |
| Cuk Side Voltage Compensator | $G_{v2}(s)$ | $\frac{177}{10}+\frac{10}{s}$ | $\frac{1}{4}+\frac{10}{s}$ |
| CV Mode Compensator | $G_c(s)$ | $100+\frac{10}{s}$ | $100+\frac{10}{s}$ |
| CC Mode Compensator (PSFB) | $G_d(s)$ | $\frac{9}{10}+\frac{10}{s}$ | $10+\frac{10}{s}$ |
| CC Mode Compensator (DAB) | $G_d(s)$ | $\frac{7}{50}+\frac{10}{s}$ | $5+\frac{10}{s}$ |

# 7 SIMULATION AND EXPERIMENTAL RESULTS

## 7.1 Objective

This chapter aims to test both the household and EV charging schemes in a simulation environment and experimentally validate the simulation result in the Power Hardware-in-the-Loop (PHIL) laboratory environment. In addition, several performance parameters will be investigated and graphically presented. Subsequently, the grid-supporting potentials of the designed DAB converters with CLLC resonant tank circuits will be instigated by reproducing the front-end soft-switching inverter proposed in [29]. Finally, the promising result will be compared with some relevant state-of-the-art.

## 7.2 Simulation Results

### 7.2.1 Simulation Assumptions

At first, the complete charging system was simulated in Simulink. The following assumptions were made for the simulation purpose –

- Losses were modeled by the series resistances along with the passive elements.
- Diode reverse recovery losses were not modeled. Nevertheless, the existing diode package in Simulink was used.
- Losses in the compensators were discarded.
- All the design parameters were calculated according to Table 4.2.

### 7.2.2 Supply Voltage and Current

The novel bipolar PFC converter has been implemented to improve the power quality. Fig. 7.1 illustrates the supply voltage and current waveshapes for household and EV energy storage systems. Both the figures clearly show that the voltage and current remain in phase, meaning that the power factor is nearly at unity, thus ensuring the PFC control. It is also noticeable that a very insignificant amount of harmonics is present in the input currents in both cases. The Fast Fourier Transformation (FFT) analyses of the input currents, as in Fig. 7.2, show that the Total Harmonic Distortions (THD) do not violate the *IEC 61000-3-2* standard. Therefore, the power quality has improved considerably despite the high power ratings of the converter for charging two batteries simultaneously.

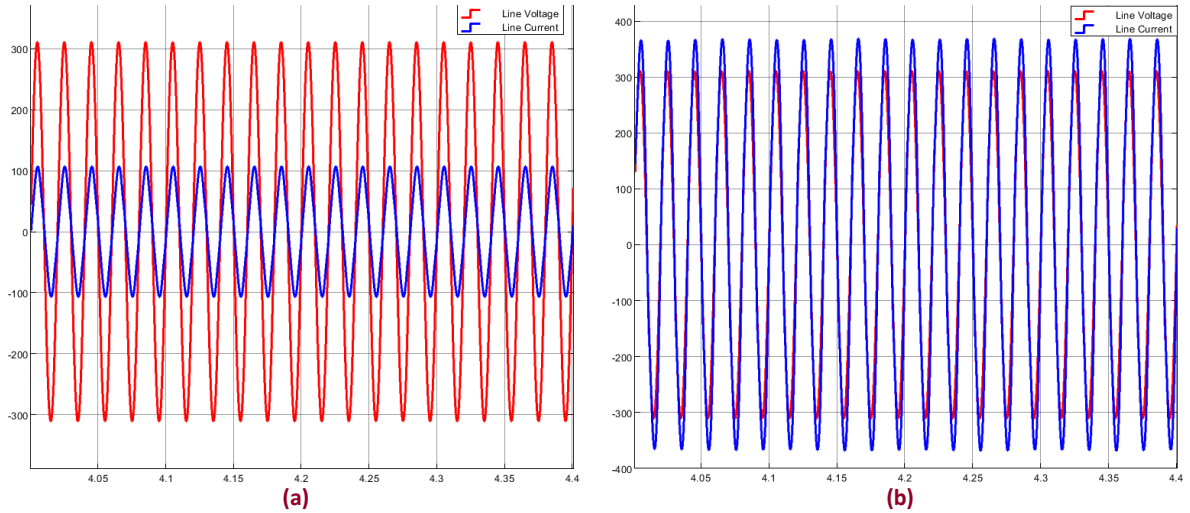
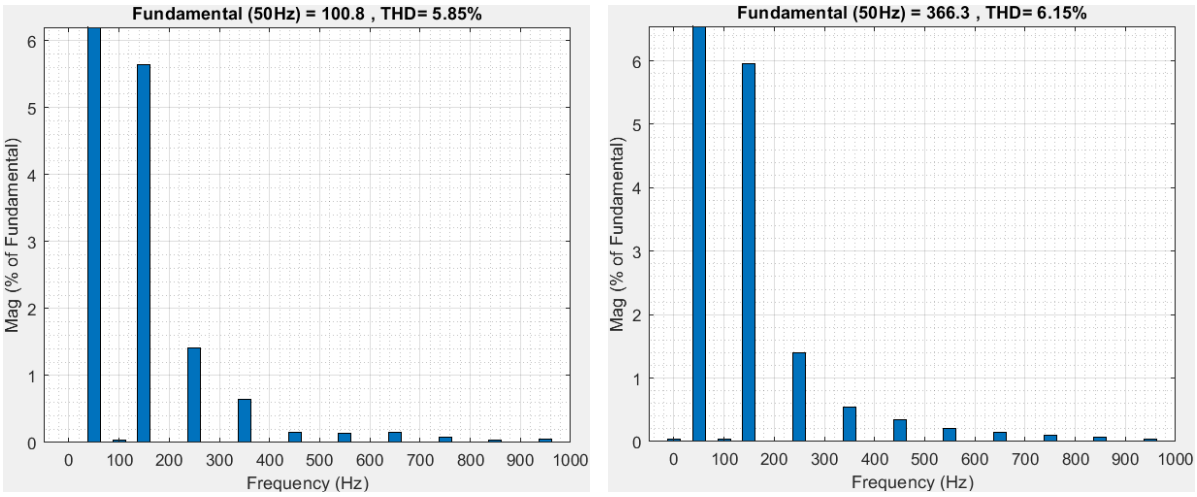



**Fig. 7.1: Source voltage and current waveshapes for (a) household and (b) EV charging system**

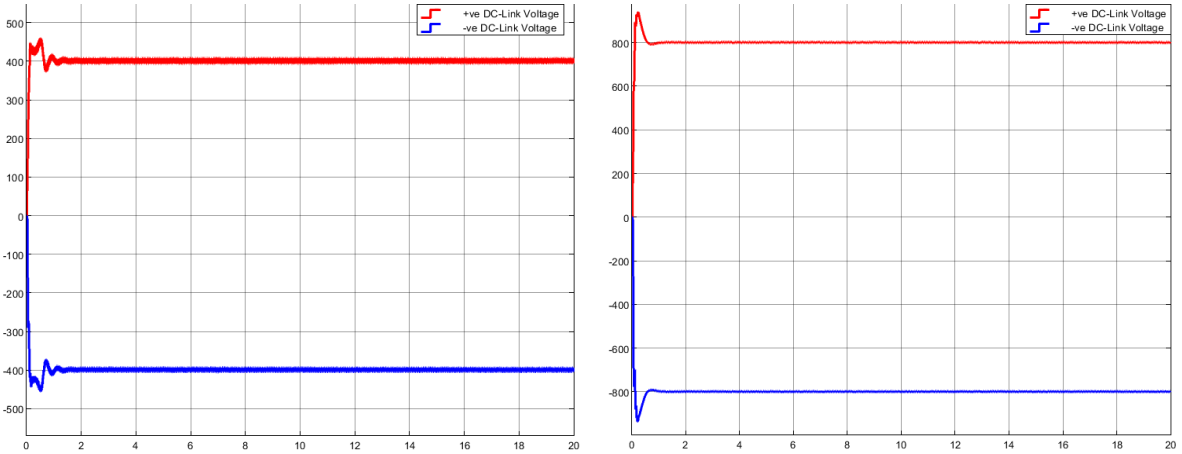



(a) (b)

**Fig. 7.2: Source current of (a) household and (b) EV charging system in the FFT domain**

### 7.2.3 Bipolar DC Bus Voltages

Fig. 7.3 depicts the regulated DC bus voltages for household and EV charging systems. The household energy storage system necessitates *±400 V* bus voltages, whereas the off-board EV energy storage system requires *±800 V* bus voltages. Based on the interfaced battery voltage ratings, cascaded PSFB and DAB converters further step down the bus voltages. One can notice that the voltages are perfectly regulated throughout the CC-CV transitions despite some negligible overshoots in the beginning.




(a) (b)

**Fig. 7.3: Bipolar DC-link voltages for (a) household and (b) EV charging system**

### 7.2.4 Battery Voltages and Currents

Fig. 7.4 shows the battery voltages and charging currents for the household and EV energy storage systems. By dint of the novel bipolar PFC converter, two batteries can be charged simultaneously from supply mains. As discussed in Sections 4.3 and 4.4, the household batteries are *48 V – 300 Ah*, and the EV batteries are *360 V – 150 Ah*. The simulation starts from *98.5%* SOC in both cases. Initially, the household batteries are charged with a constant *130 A* current. As soon as the battery voltages reach *55 V*, the charging currents start decreasing to keep the battery voltages constant. On the other hand, a constant charging current of *65 A* is maintained while charging the EV batteries in the CC mode. Similarly, the charging currents start reducing when the battery voltages reach *415 V* to keep the voltage levels consistent. It is visible from Fig. 7.4 that the designed controllers smoothly shift the

converter operating points when the transition from the constant-current (CC) mode to the constant-voltage (CV) mode occurs.

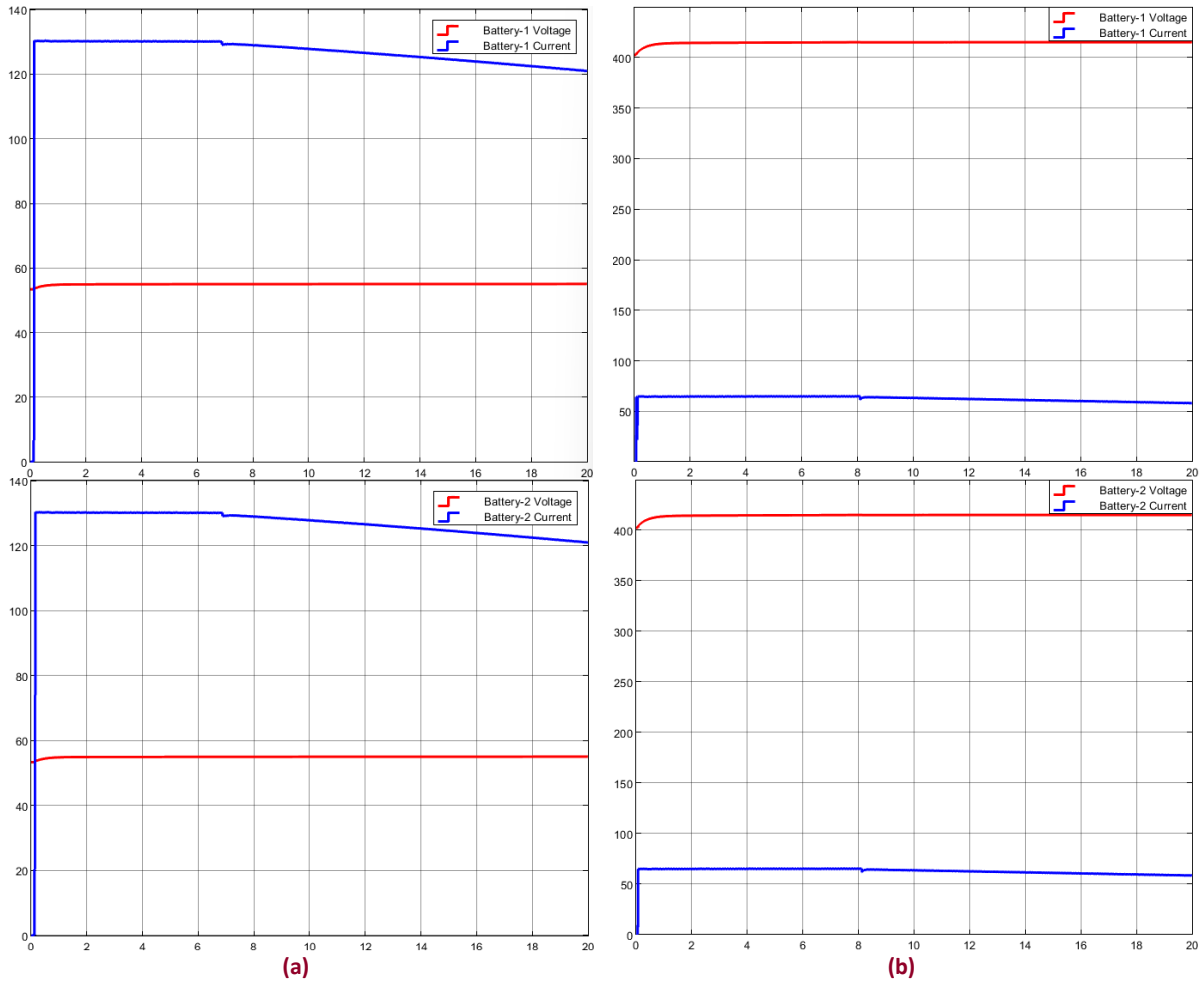



**Fig. 7.4: Battery voltage and charging current for (a) household and (b) EV charging system**

### 7.2.5 Comparison of the Performance Parameters

Table 7.1 and Table 7.2 show different performance parameters against different power ratings for household and EV charging systems, respectively.

**Table 7.1: Different performance parameters for the household charging system**

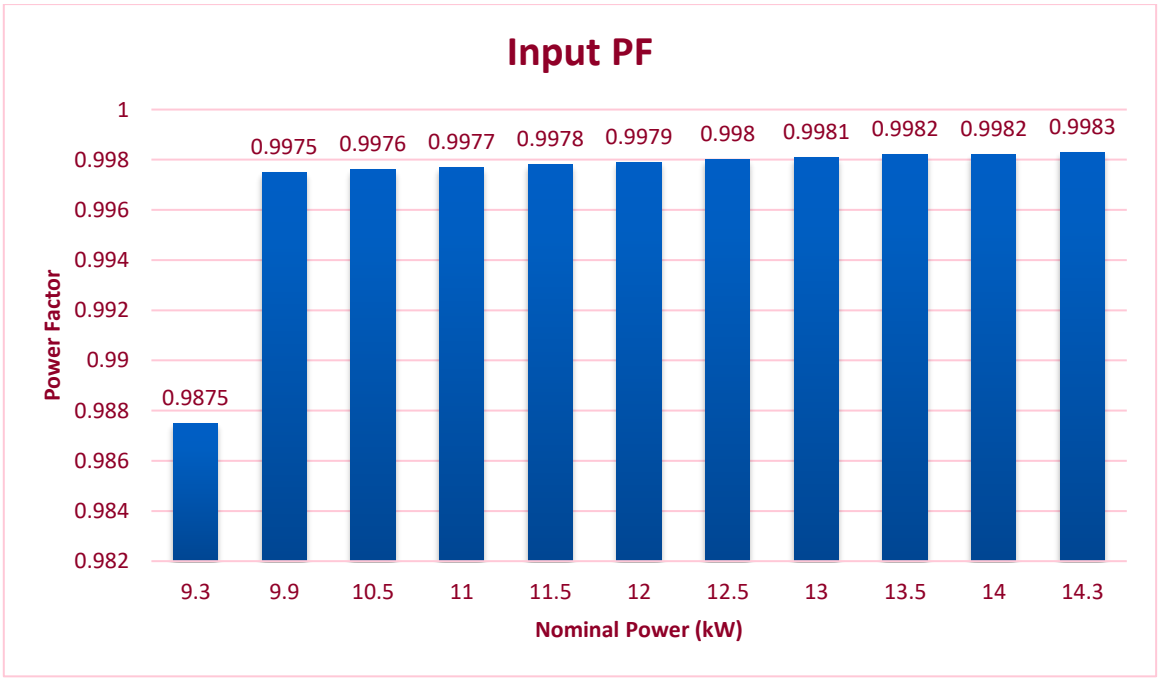
| Nominal Power (kW) | Input PF | Input Current THD (%) | Efficiency (%) |
|---|---|---|---|
| 9.3 | 0.9875 | 7.05 | 98.4 |
| 9.9 | 0.9975 | 7.03 | 98.7 |
| 10.5 | 0.9976 | 6.93 | 98.8 |
| 11 | 0.9977 | 6.78 | 99 |
| 11.5 | 0.9978 | 6.53 | 98.5 |
| 12 | 0.9979 | 6.45 | 99 |
| 12.5 | 0.998 | 6.27 | 98.4 |
| 13 | 0.9981 | 6.15 | 97.8 |
| 13.5 | 0.9982 | 6.02 | 98.3 |
| 14 | 0.9982 | 5.95 | 97.7 |
| 14.3 | 0.9983 | 5.85 | 98.1 |

**Table 7.2: Different performance parameters for the EV charging system**

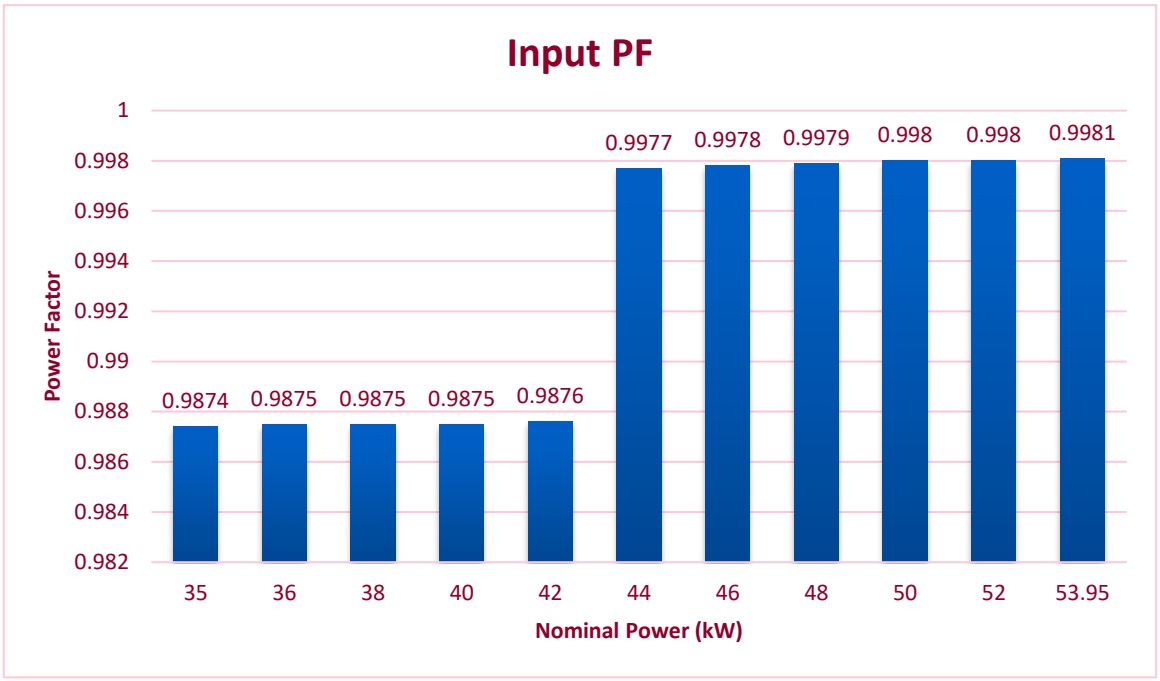
| Nominal Power (kW) | Input PF | Input Current THD (%) | Efficiency (%) |
|---|---|---|---|
| 35 | 0.9874 | 7.21 | 96.6 |
| 36 | 0.9875 | 7.15 | 96.4 |
| 38 | 0.9875 | 7.09 | 97.1 |
| 40 | 0.9875 | 7.01 | 96.8 |
| 42 | 0.9876 | 6.93 | 96.5 |
| 44 | 0.9977 | 6.78 | 97 |
| 46 | 0.9978 | 6.63 | 96.7 |
| 48 | 0.9979 | 6.47 | 96.2 |
| 50 | 0.998 | 6.31 | 95.8 |
| 52 | 0.998 | 6.24 | 96.3 |
| 53.95 | 0.9981 | 6.15 | 96.1 |

### *7.2.5.1 Input PF Comparison*

Power Factor Correction (PFC) is one of the salient features of the proposed topology. The low power factor means more deviation in the angle between the input voltage and current. The series impedance with the input source and the passive elements of the traditional SMPS converters result in low power factors. Nevertheless, the proposed topology substantially improves the input power factor. Fig. 7.5 compares input PF for household and EV energy storage systems against different power ratings. One can notice that both the charging networks exhibit the best PFC performance in the highest power ratings, and the performance deteriorates slightly in the lowest power ratings. This anomaly persists because the associated EMI filters were designed considering the maximum converter power ratings. Therefore, after a particular operating point, the designed EMI filters no longer remain optimal, resulting in the power factor dropping a bit under unity.




**(a)**

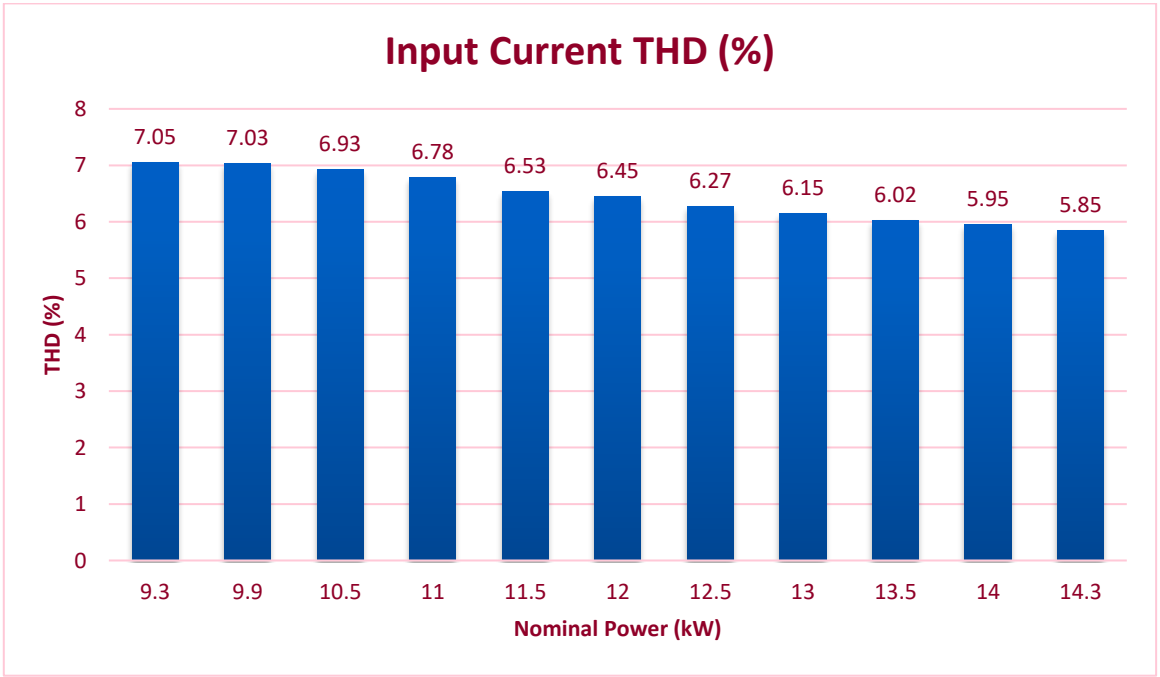



**(b)**

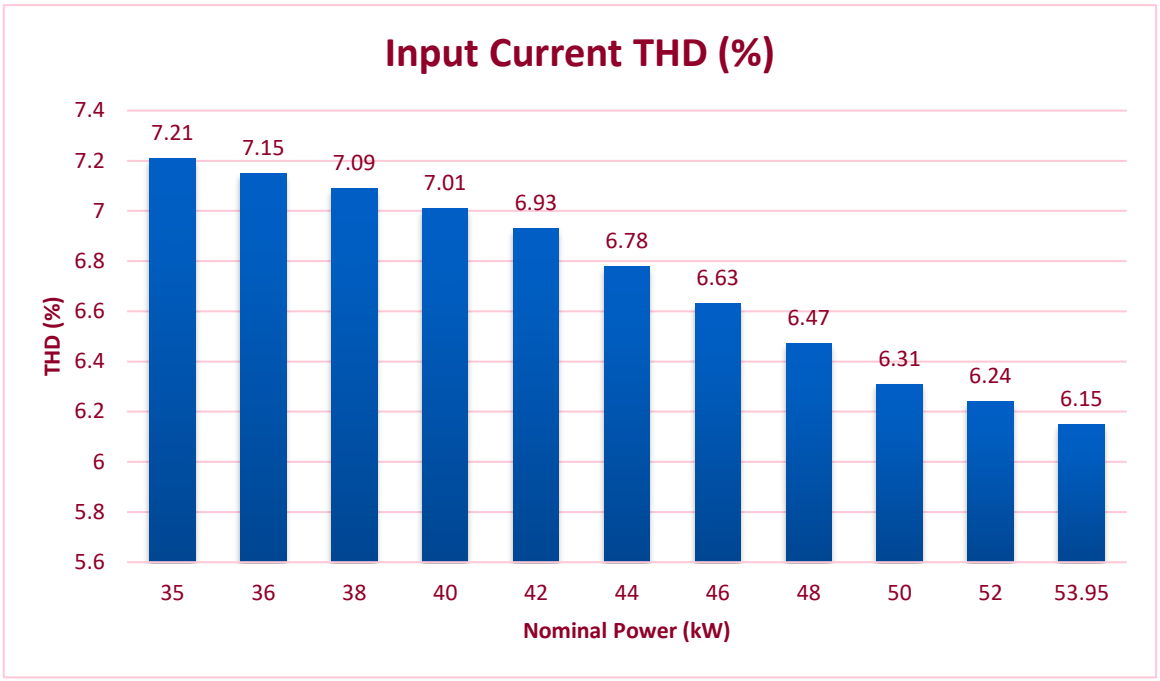
**Fig. 7.5: Input PF vs. nominal power for (a) household (b) EV charging system**

### *7.2.5.2 THD Comparison*

Switched-mode power supplies operate by rapidly switching the voltage on and off to regulate the output voltage, creating harmonic currents that are multiples of the fundamental frequency of the input voltage. Fig. 7.6 illustrates the input currents' THD (%) against different power ratings. The same explanation of Subsection 7.2.5.1 stands for which the THDs are the lowest under full load conditions.




**(a)**

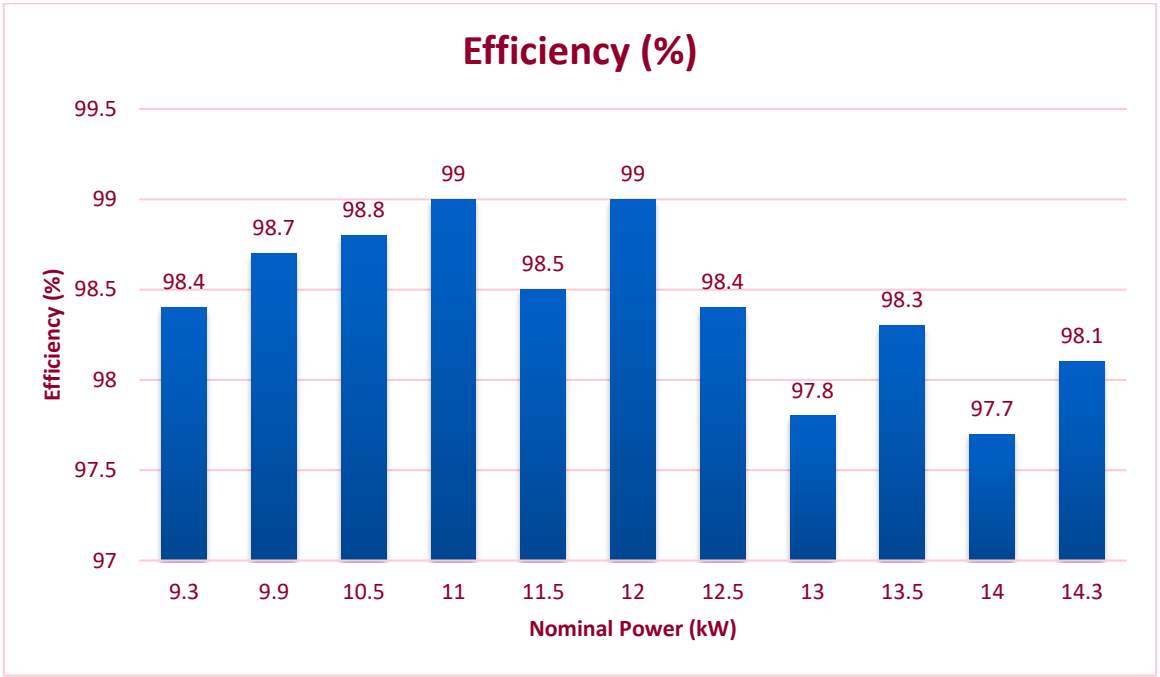



**(b)**

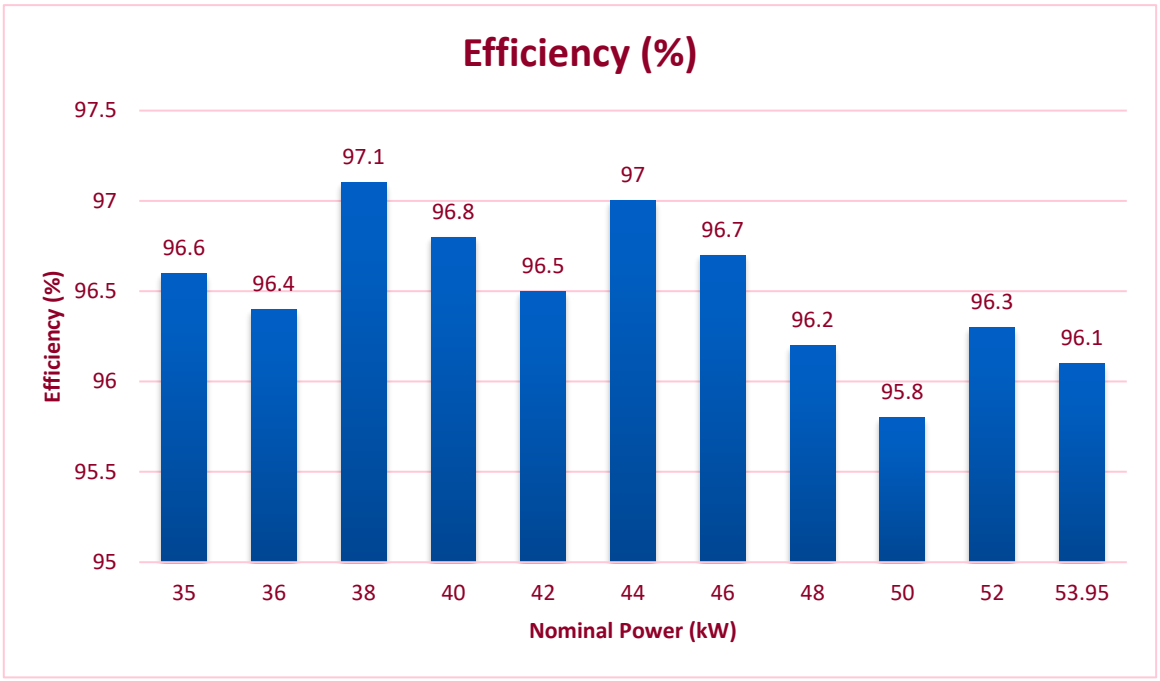
**Fig. 7.6: Input current THD (%) vs. nominal power for (a) household (b) EV charging system**

### *7.2.5.3 Efficiency Comparison*

Fig. 7.7 depicts efficiency (%) against various power ratings. It is noticeable that the efficiency peaks at *11 kW* and *12 kW* power ratings in the case of the household energy storage system and at *38 kW* rated power in the case of the EV charging system. By virtue of the proposed model's operating principle, the conduction losses increase at higher power ratings, reducing the overall efficiency a bit.




**(a)**

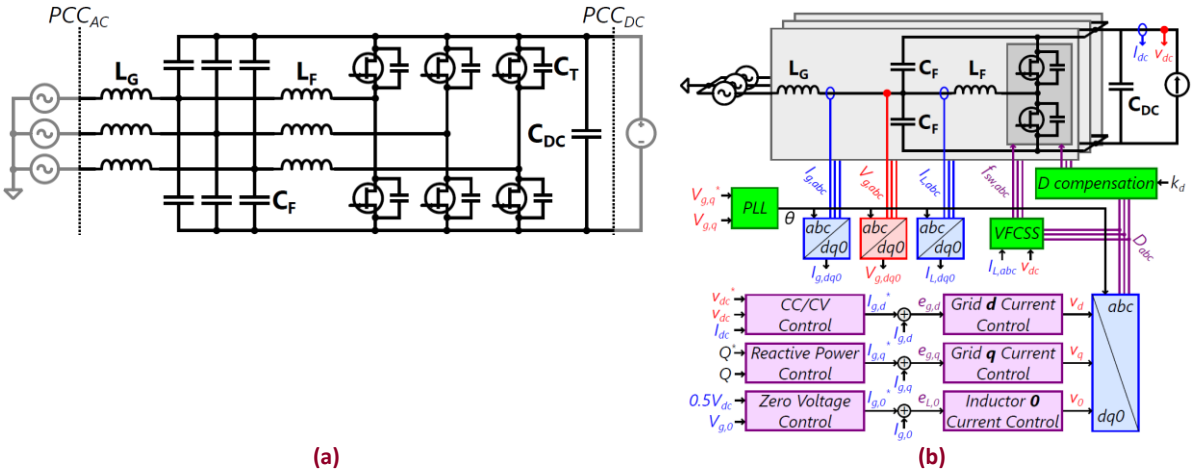



**(b)**

**Fig. 7.7: Efficiency (%) vs. nominal power for (a) household (b) EV charging system**

## 7.3 Grid-Supporting Potentials of DAB Converters

To effectively utilize EVs for grid services, soft-switching control strategies are desirable to mitigate switching losses. The DAB converters with CLLC resonant tank circuits, implemented in the thesis, are capable of soft-switching. However, a front-end inverter is required to feed the surplus energy from the EVs to the grid to activate the bidirectional mode for the grid-supporting feature. In such a case, the soft-switching inverter, presented in [29], was picked up for reproduction to investigate the bidirectional feature and grid-supporting potentials of the designed DAB converters. Fig. 7.8 illustrates the soft-switching architecture and its implemented control system. One may go through the literature to learn more about the soft-switching inverter model. However, developing such a grid-tied soft-switching inverter was beyond the scope of the thesis and may be subjected to future works.




**(a)** **(b)**

**Fig. 7.8: The soft-switching (a) inverter model and (b) its control system, presented in [29]**

### 7.3.1 Battery Voltage and Current

Fig. 7.9 illustrates the EV battery voltage and current in a time diagram. Initially, the battery was being charged with a constant *65 A* current. The negative value implies that the battery is taking power from the grid. Right before the eighth second, the battery voltage reaches *415 V*, thus activating the CV mode. The battery continued to charge with a gradually reducing current until the fifteenth second to keep the voltage constant. At the start of the fifteenth second, the battery current jumps to a positive value, meaning that the battery starts discharging, thus feeding the surplus energy to the grid. One may notice that there is no overshoot in the control dynamics during all these transitions. Such smooth transitions conclude that the designed DAB controllers, with the help of dynamic modeling in the thesis, have significant potential in grid services.

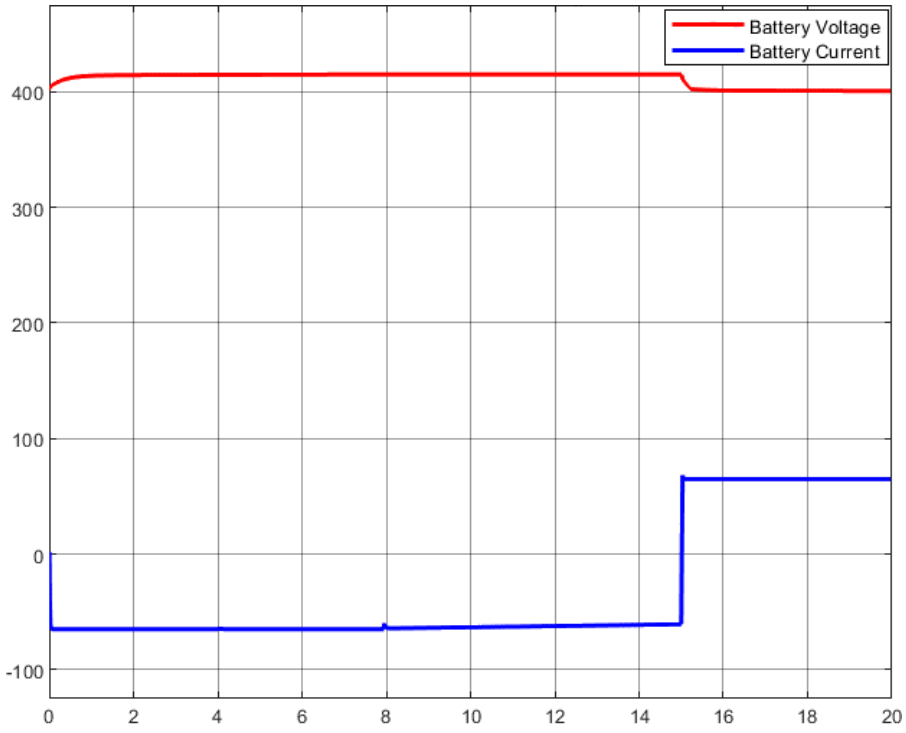
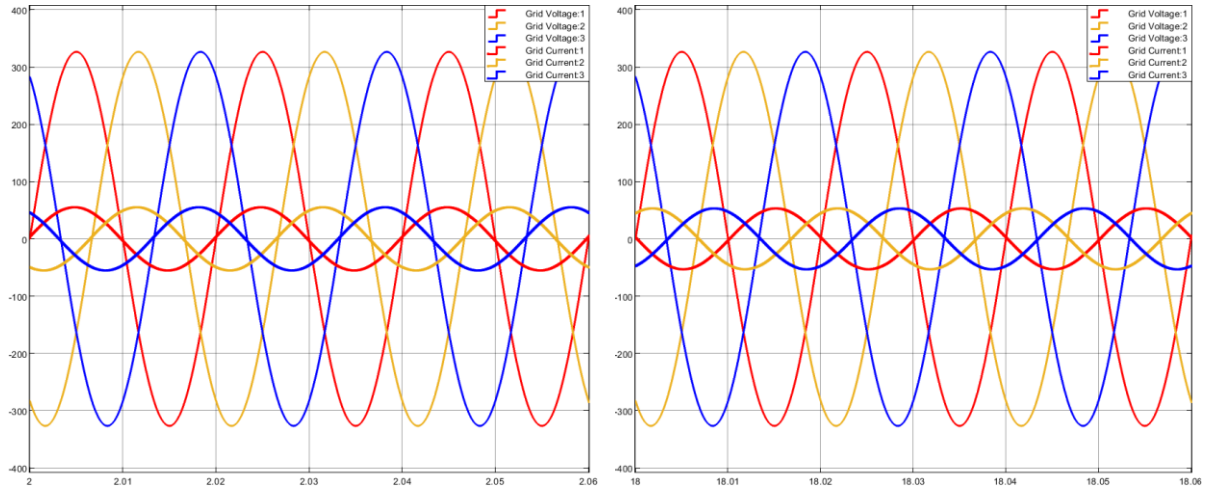



**Fig. 7.9: EV battery voltage and current during charging and discharging modes of operation**

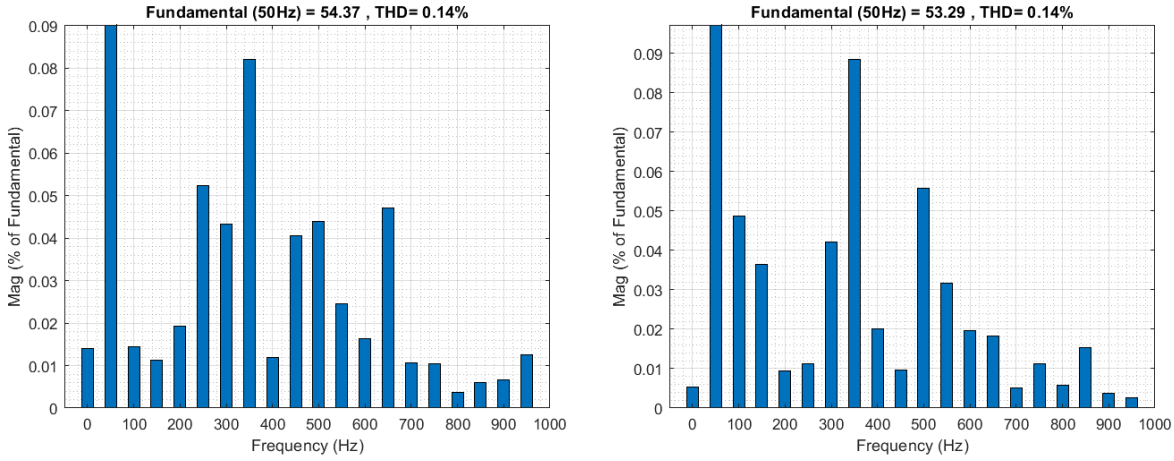
### 7.3.2 Grid Voltage and Current

Fig. 7.10 depicts grid voltage and current waveshapes in both charging and discharging modes of operation. During the charging mode, the phase voltages and line currents remain in phase, meaning that the battery takes power from the grid in a unity power factor without causing any distortions. On the other hand, the phase voltages and line currents are *180* degrees apart in the case of discharging mode, implying that the battery is supporting the grid with its surplus energy without any distortions. Fig. 7.11 illustrates the grid current in the FFT domain for both the charging and discharging modes of operation. It is clearly noticeable that the total harmonic distortion is only *0.14%* in both cases. Though such harmonics mitigation is a salient feature of the mentioned literature, the cascaded DAB converter, developed in the thesis, contributes to successfully interfacing EV batteries with the grid through the soft-switching inverter topology.




(a) (b)

**Fig. 7.10: Grid voltage and current waveshapes during (a) charging and (b) discharging mode**




(a) (b)

**Fig. 7.11: Grid current during (a) charging and (b) discharging mode in the FFT domain**

## 7.4 Prototype Testing of the Novel Bipolar PFC Converter

### 7.4.1 Hardware Configuration

The most significant part of the thesis was the development of a novel high-gain bipolar PFC converter. The developed bipolar PFC converter was experimentally validated in a PHIL environment using the imperix rapid prototyping solution. Fig. 7.12 depicts the conventional imperix template used in prototyping. The control algorithm was implemented inside the controller block, whereas the plant comprises the physical system. The controller is interfaced with the plant through a computer.

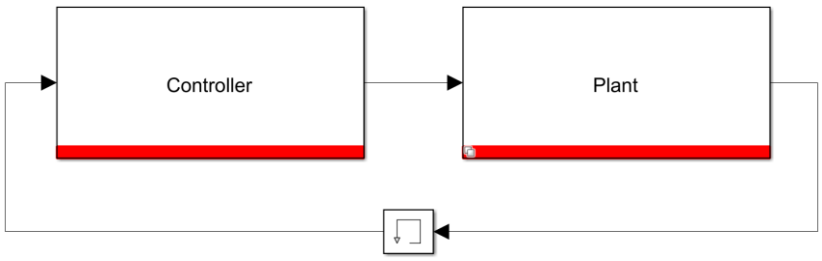



**Fig. 7.12: Imperix rapid prototyping template**

Fig. 7.13 illustrates the built prototype at the Smart Power Laboratory. The connections have been represented as a block diagram to conveniently present how the control unit is interfaced with the hardware system. The grid simulator, representing the grid, is directly connected to the EMI filter, input filter capacitor, and switched-inductors. The resistive loads are connected across the output filter capacitors. Analog sensors are connected between the loads and the control unit to sense the necessary voltage and current levels required as control inputs. Analog-to-digital converters (ADC) are implemented inside the control unit to translate the physical system into the digital domain. The user can control all the control parameters from the laptop, which is connected in a loop with the hardware through ethernet communication. Necessary PWM signals are generated by the control unit and sent to the imperix boom box, comprising IGBTs with anti-parallel diodes. While one IGBT was used as the controlling element, anti-parallel diodes of other IGBTs were used as the diodes of the converter. One may go through the imperix user manual to better understand how it works.

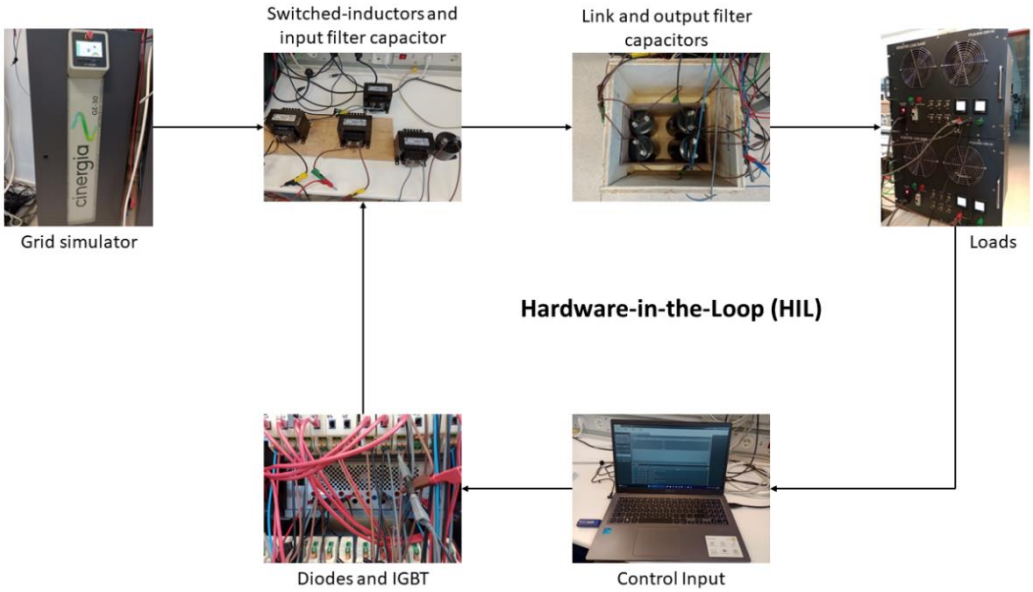



**Fig. 7.13: Implemented prototype of the bipolar PFC converter**

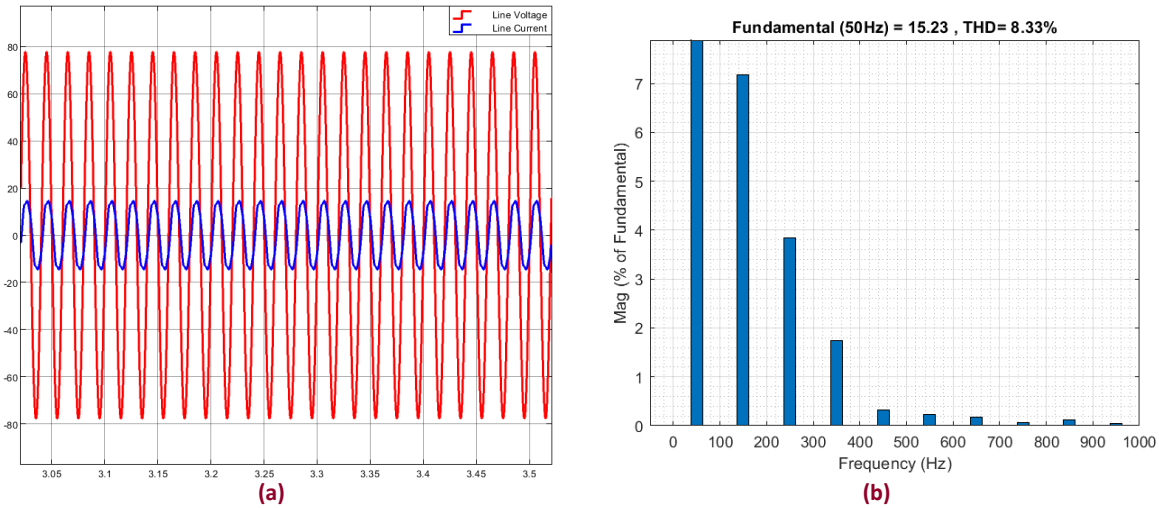
### 7.4.2 Design Specifications

The prototype was tested under two different conditions. The first one validates the PFC stage, while the other examines the dynamic behavior under different load conditions. Nonetheless, the output voltage references were varied during both cases. For the efficiency illustration, the nominal power of the converter was varied from *205 W* to *510 W*. The design parameters were recalculated according to the prototype power rating as the following –

- $f_{switch}$ = *20 kHz*
- Loads = *40 Ω* on each of the bipolar sides
- *L = 15 mH*, $L_1 = L_2 = L_3 = L_4$ = *2.5 mH*
- *C = 40 µF*, $C_f$ = *100 µF*, $C_1 = C_2$ = *360 µF*, $C_3 = C_4$ = *800 µF*

### 7.4.3 Source Voltage and Current

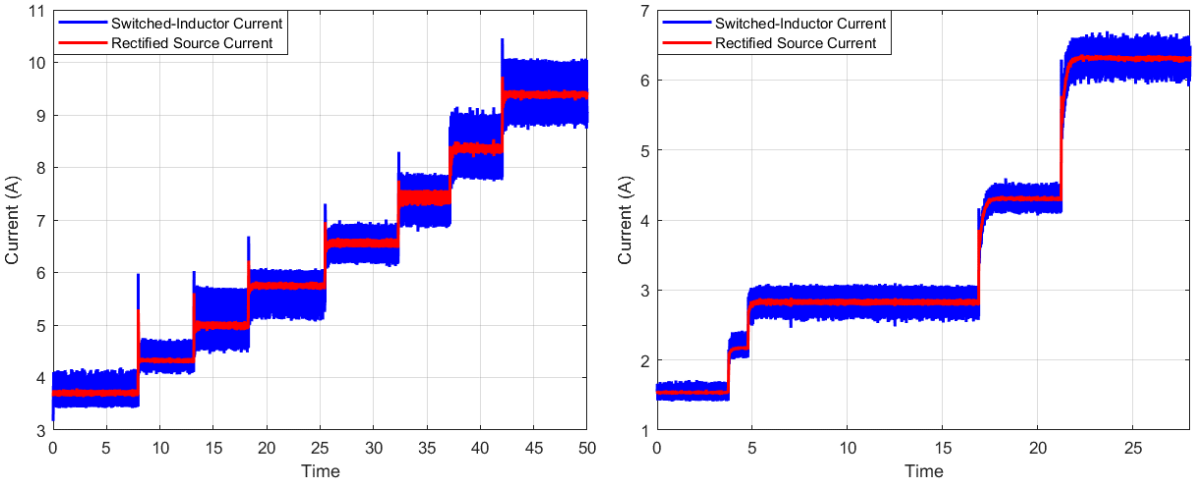
Fig. 7.14 (a) resembles the mains voltage and current waveforms of the prototype. *55* $V_{rms}$ AC voltage, generated by the grid simulator, was regarded as the source of the prototype. Fig. 7.14 (b) presents the source current in the FFT domain. The THD was *8.33%*, which is close to the simulation result.




(a) (b)

**Fig. 7.14: (a) Source voltage and current waveshapes, (b) source current in the FFT domain**

Fig. 7.14 ensures the power quality improvement, including the power factor correction (PFC) and harmonics reduction. Fig. 7.15 illustrates the rectified source current and the current through the switched-inductor configuration. It is visible that the rectified source current behaves like a moving average of the switched-inductor current, validating the operating principle of the converter. The transition instances resemble the change in converter dynamics.




(a) (b)

**Fig. 7.15: Switched-inductor and rectified source currents for (a) *55 $V_{rms}$* input, (b) *25 $V_{rms}$* input**

### 7.4.4 Regulated Bus Voltages

Fig. 7.16 depicts the regulated bus voltages for different input and output voltage levels. In Fig. 7.16 (a), *55 $V_{rms}$* input voltage was applied, and the output voltage reference was set at *60 V*. The bus reference voltage was gradually increased to *100 V*. The bipolar bus voltages immediately followed the reference with no overshoot and ringing. On the other hand, in Fig. 7.16 (b), *25 $V_{rms}$* input voltage was applied, and the initial output voltage reference was *25 V*. Right before the fifth second, one can notice two small disturbance events in Fig. 7.16 (b). These two disturbances refer to two sudden load changes. During the first disturbance, the load connected to the SEPIC side was reduced from *40 Ω* to *20 Ω*, while the second disturbance occurred at the time of a similar load change at the Cuk side. Such load-changing events can also be noticed in Fig. 7.15 (b), where both the rectified input current and the

switched-inductor current responded to the load changes at the same time instances. If the loads are halved, the input current must be doubled to keep the output voltages constant. This phenomenon can be noticed in Fig. 7.15 (b). Except for that, the output voltage reference was increased until *35 V*, and the bus voltages were found to be perfectly regulated, following the reference voltage level. Overall, in the case of all dynamic changes, be it load changes or changes in the output voltage reference, the controller responded perfectly with minimal settling time and without any overshoot, validating the credibility of the designed controller.

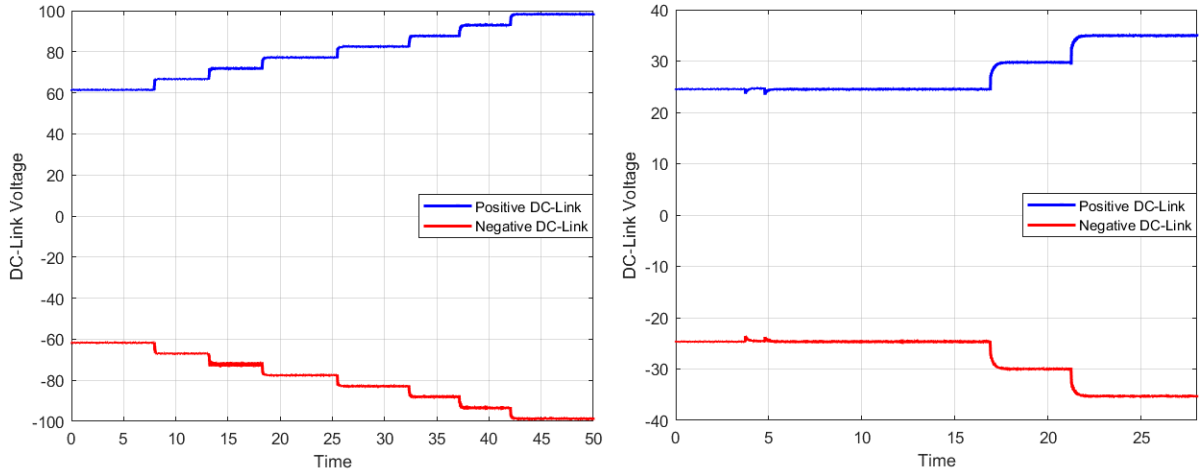



**Fig. 7.16: Regulated bipolar bus voltages for (a) *55* $V_{rms}$ input, (b) *25* $V_{rms}$ input**

### 7.4.5 Prototype Efficiency

Fig. 7.17 plots the efficiency of the prototype as a function of the converter power. The peak efficiency was *97.14%* at *345 W*. Although the peak efficiency found in the simulation result was *99%*, the prototype efficiency properly followed the analytical efficiency, derived after incorporating the conduction and semiconductor losses, presented in Fig. 4.6. Nevertheless, the *97.14%* peak efficiency of the prototype is still a significant improvement, compared to most of the state-of-the-art, discussed in the literature review.

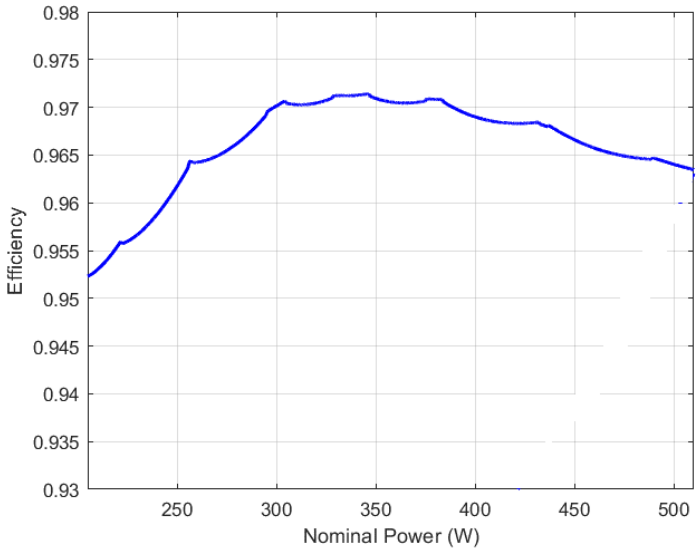



**Fig. 7.17: Efficiency (%) vs. nominal power of the prototype**

## 7.5 Result Comparison

Table 7.3 summarizes the key findings of the thesis and compares the performance parameters against the relevant state-of-the-art.

**Table 7.3: Result comparison**

| Topology | Input PF | THD (%) | Peak Efficiency (%) |
|---|---|---|---|
| Developed model | 0.9983 @household<br>0.9981 @EV<br>1 @Grid-supporting EV<br>0.9965 @prototype | 5.85 @household<br>6.15 @EV<br>0.14 @Grid-supporting EV<br>8.33 @prototype | 99 @simulation<br>97.14 @prototype |
| [8] | 0.95 | 5 | 91 |
| [11] | 0.9988 | 5 | 97 |
| [20] | 0.99 | 6 | 93.4 |
| [25] | 0.99 | 3.28 | 93 |
| [26] | 0.996 | 2.5 | 97.4 |
| [28] | 0.9994 | 3.49 | 94 |
| [30] | 0.99 | 4.85 | 93 |
| [31] | 1 | 1.57 | 97.2 |
| [32] | 0.99 | 4.1 | 91.8 |
| [75] | 0.988 | 15.4 | 90.1 |

# 8 CONCLUSION

The novel high-gain bipolar PFC converter-based charging system improves all the crucial parameters, making it an ideal front-end grid-interfacing unit regardless of the battery capacity and application. Efficiency enhancement has been proven analytically, backed by the simulation and experimental results. Switched-inductor configuration, replacing the input inductor of the traditional converters, exhibits a higher voltage gain in a lower duty cycle, resulting in fewer conduction losses. The peak efficiencies are *99%* and *97.14%* in simulation and laboratory environments, respectively. Subsequently, the input power factor persistently remains around unity for vibrant operating conditions. Harmonics suppression is also spot on, resulting in *5.85%* and *6.15%* input current THD for household and EV charging systems, respectively. Moreover, with the help of small-signal models, the designed controllers exhibit fast dynamic responses under different circumstances. Furthermore, the charging currents and the DC-link voltages are free from unnecessary switching ripples. The designed CLLC resonant tank circuit-based DAB converter and its associated controllers have been interfaced with the grid through a soft-switching inverter to investigate the grid-supporting feature, resulting in only *0.14%* THD in the grid current for both power flow directions. Last but not least, the soft-switching control for PSFB and DAB converters is also ensured by necessary dead-time calculation, considering all the parasitic elements present in such converters. Overall, after validating the outcomes in the Power Hardware-in-the-Loop (PHIL) laboratory environment, the proposed charging solution in the thesis has solidified its position as a future low-loss charging scheme for both household and EV (off-board and on-board) energy storage systems under a wide range of operating conditions.

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# APPENDIX

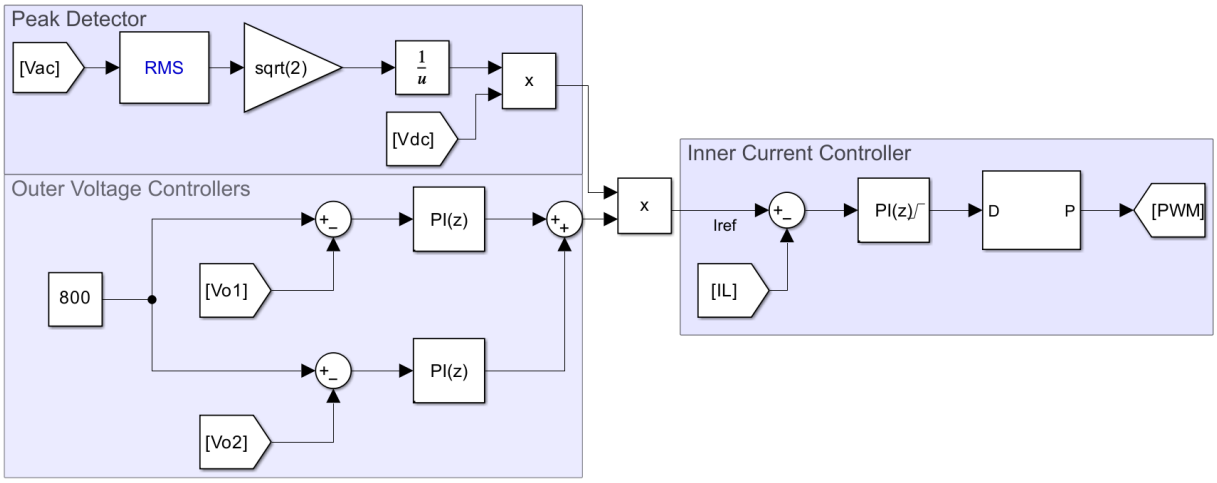


**Figure: PFC control of the bipolar converter, implemented in Simulink**

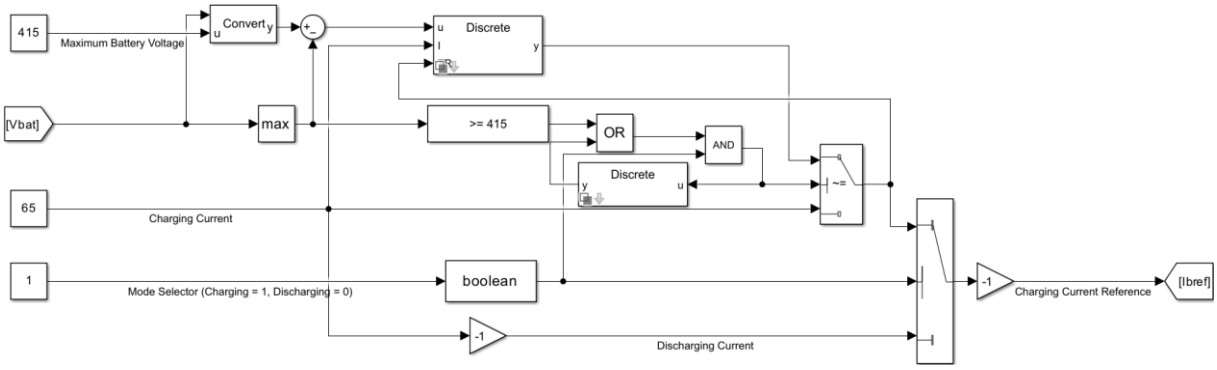


**Figure: CC-CV control algorithm, implemented in Simulink**

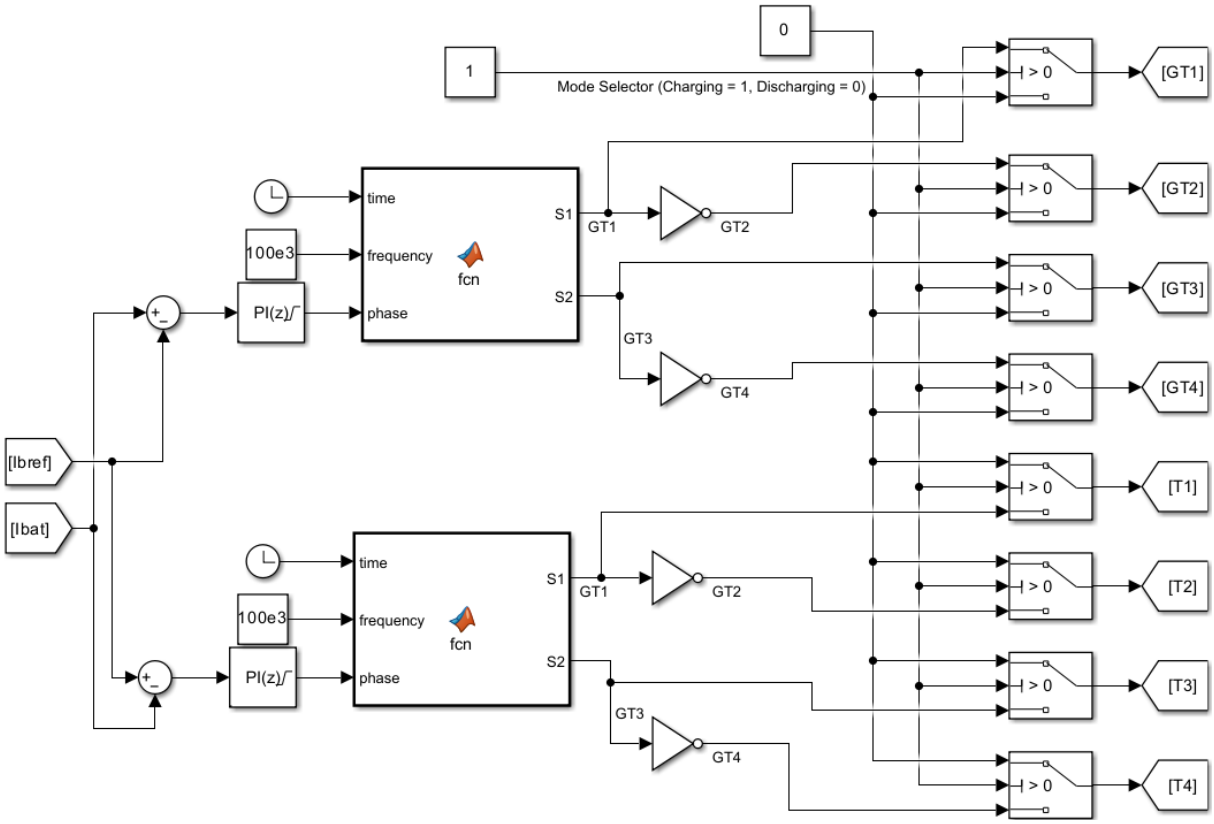


**Figure: DAB controller, implemented in Simulink**

## *PWM Functional Block for DAB Controller*

```
function [S1, S2] = fcn(time,frequency,phase)
T = 1/frequency;
S1 = 0;
S2 = 0;
y1 = mod(time,T);
if y1 < T/2
    S2 = 1;
end
phase_shift = T*phase/360;
y2 = mod(time+phase_shift,T);
if y2 < T/2
    S1 = 1;
end
```

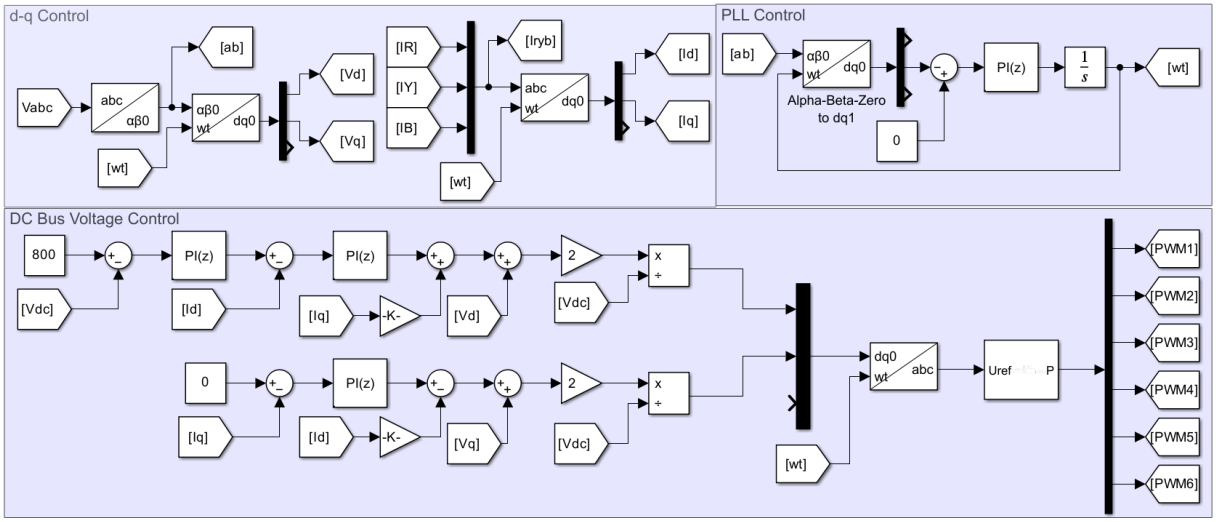


**Figure: Front-end soft-switching inverter control system for G2V and V2G functionality investigation**

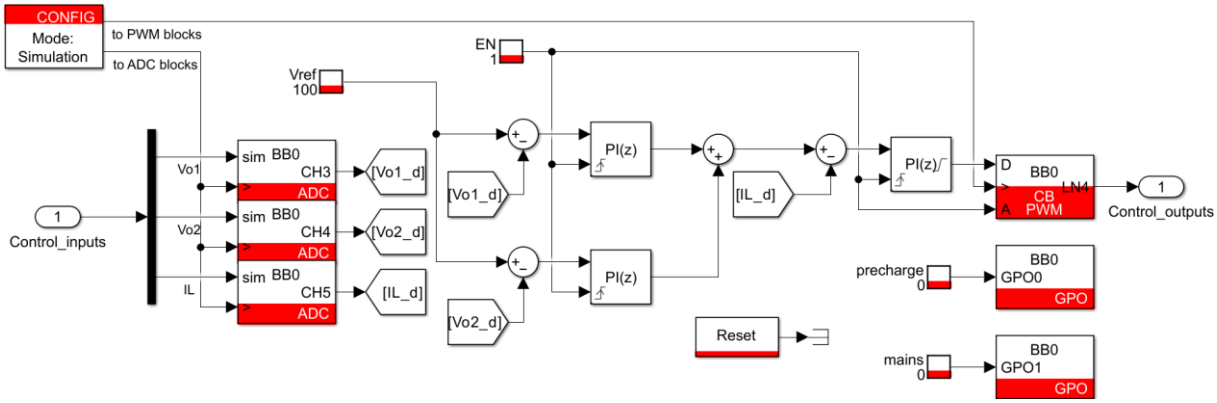


**Figure: Prototype controller, built in the imperix system**

## *Imperix Boom Box Sensor Configurations*

| Channel 3 | Channel 4 | Channel 5 |
|---|---|---|
| [input3] | [input4] | [input5] |
| low_impedance=no | low_impedance=no | low_impedance=no |
| gain=8 | gain=8 | gain=4 |
| filter_on=yes | filter_on=yes | filter_on=yes |
| filter_freq=6400 | filter_freq=6400 | filter_freq=6400 |
| limit_high=8.0 | limit_high=8.0 | limit_high=8.0 |
| limit_low=-8.0 | limit_low=-8.0 | limit_low=-8.0 |
| disable_safety=no | disable_safety=no | disable_safety=no |