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Cryogenic Ferroelectricity of HZO with an Aluminium Oxide Inter-layer

Mamidala Karthik Ram and Lars-Erik Wernersson

***Abstract*— In this work, we investigate the cryogenic performance of hafnia-based ferroelectric capacitors with and without an aluminium oxide (ALO) inter-layer, comparing conventional Metal-Ferroelectric-Metal (MFM) structures to Metal-Ferroelectric-Insulator-Metal (MFIM) counterparts. Devices employing $Hf_{0.5}Zr_{0.5}O_2$ as the ferroelectric layer were characterized from 300 K down to 10 K, targeting temperature ranges relevant to cryogenic logic and quantum memory. Our results reveal that the ultra-thin ALO interlayer effectively suppresses leakage across all temperatures while altering the coercive field symmetry and reducing remnant polarization as the temperature is reduced. Dynamic switching measurements and analysis show that MFM capacitors achieve near temperature-independent polarization switching at a 3.0 V WRITE amplitude. In contrast, MFIM devices show more pronounced temperature dependence in the switching behavior, particularly at temperatures below 77 K. While both the MFM and MFIM devices exhibit endurance > 10^7 cycles at 77 K and 10 K, the MFIM devices are more affected by polarization fatigue. Benchmarking against state-of-the-art literature values confirms that our MFM and MFIM structures demonstrate among the highest reported $2P_r$ values below 77 K at low operating voltages (≤ 3.5 V). These results highlight the promise of inter-layer-engineered hafnia capacitors for low-power cryogenic memory applications.**

***Index Terms*— Cryogenic, Ferroelectric, HZO, Phase Transition, FeRAM, Non-volatile Memory, Switching Dynamics, Inter-layer, Aluminium Oxide.**

I. Introduction

THE pursuit of non-volatile memory (NVM) technologies capable of operating at cryogenic temperatures (4.2 K to 77 K) is gaining momentum, driven by the demands of emerging quantum and high-performance computing architectures [1]. Proximal integration of memory with qubits and logic offers advantages such as reduced operating voltage, lower system latency, and a more compact hardware footprint [1],[2],[3]. Hafnium oxide-based ferroelectric materials have emerged as promising candidates for this role, thanks to their CMOS process compatibility and energy-efficient switching behavior [4],[5],[6],[7],[8],[9],[10]. However, gaining deeper insight into their switching characteristics across cryogenic temperatures is essential to evaluate their full potential for integration in future memory technologies.

Many studies have explored the effect of inter-layers on improving reliability in ferroelectrics and enhancing Resistive Random Access Memory (RRAM) performance. Still, most focus on room-temperature (RT) conditions [11],[12],[13]. Studies on memory devices incorporating inter-layers at cryogenic temperatures are scarce [6],[14]. Moreover, performance comparisons of inter-layer effects at cryogenic temperatures have been explored primarily for RRAMs rather than ferroelectrics [15],[16],[17].

In this study, we systematically evaluate the cryogenic performance of hafnia-based ferroelectric capacitors by comparing Metal-Ferroelectric-Metal (MFM) and Metal-Ferroelectric-Insulator-Metal (MFIM) structures, incorporating an ultra-scaled aluminium oxide (ALO) interlayer between $Hf_{0.5}Zr_{0.5}O_2$ (HZO) and the bottom electrode. Both static and dynamic polarization characteristics are studied from 300 K down to 10 K, with measurements taken at 14 intermediate temperatures spanning the cryogenic regime. To the best of our knowledge thus far, this is the first study to systematically compare MFM and MFIM capacitor performance across such a broad temperature range, with a particular focus on the 4.2 K to 77 K quantum memory window. The analysis includes leakage current measurements, coercive field evolution, polarization switching dynamics, capacitance–voltage characteristics, and endurance measurements up to 10^7 cycles. This comparison directly reveals the design trade-offs between the two structures. While the Al_2O_3 inter-layer suppresses leakage and stabilizes coercive fields under endurance cycling, it does so at the expense of remnant polarization amplitude. In contrast, MFM capacitors maintain a stronger remnant polarization but exhibit higher leakage and more field-cycling-induced imprint. These insights, combined with benchmarking against prior reports, offer preliminary guidelines for tailoring hafnia-based ferroelectrics toward different cryogenic memory applications such as ferroelectric Field-Effect Transistors (FeFETs), where leakage and switching stability are critical, versus ferroelectric random access memory (FeRAM), where higher polarization is prioritized.

II. Device Fabrication and Measurement Setup

To investigate the cryogenic properties of ferroelectric capacitors with $Hf_{0.5}Zr_{0.5}O_2$ as the switching layer, both Metal-Ferroelectric-Metal (MFM) and Metal-Ferroelectric-Insulator-Metal (MFIM) stacks are fabricated. The fabrication begins with a 10-nm-thick TiN bottom electrode (BE) deposition on a

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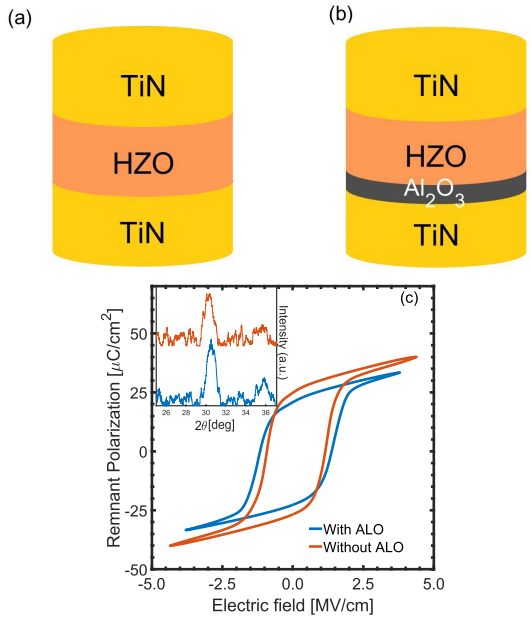

Fig. 1. (a) and (b) Cross-sectional schematics of the MFM and MFIM capacitor structures respectively. (c) *P–E* characteristics of both devices at room temperature after wake-up (10 kHz, 3.5 V), with inset showing GI-XRD confirming the presence of the o(111)/t(011) phase.

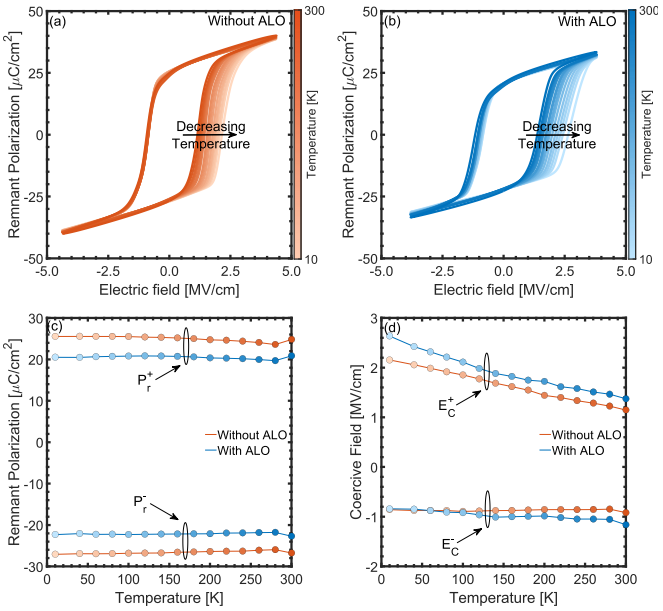

Fig. 2. *P-E* characteristics of the same $Hf_{0.5}Zr_{0.5}O_2$ capacitor after WU at RT and measured from 300 K to 10 K for the samples (a) without ALO and (b) with ALO where the colour bars indicate the temperatures. (c) Remnant polarization and (d) coercive field across the temperature range for both samples.

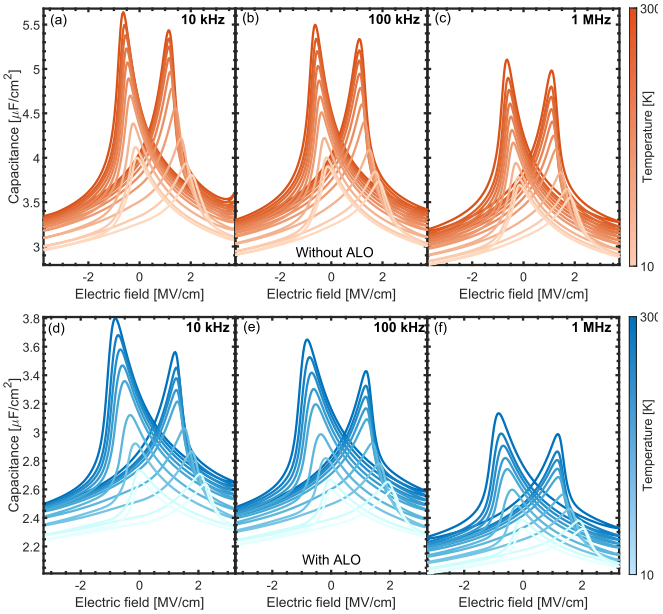

Fig. 3. *C-V* characteristics of the same $Hf_{0.5}Zr_{0.5}O_2$ capacitor after WU at RT and measured from 300 K to 10 K for the sample without ALO at (a) 10 kHz, (b) 100 kHz and (c) 1 MHz; for the sample with ALO at (d) 10 kHz, (e) 100 kHz and (f) 1 MHz

thermally oxidized Si substrate using physical vapor deposition (PVD). For MFIM capacitors, about 1.2-nm-thick Al_2O_3 (12 cycles) (ALO) inter-layer is subsequently deposited via atomic layer deposition (ALD) using trimethylaluminum (TMAl) and H_2O as precursors. This deposition is followed by an about 8-nm-thick $Hf_{0.5}Zr_{0.5}O_2$ layer deposited using ALD with alternating pulses of TDMA-Hf and TEMA-Zr for 40 cycles each. A 10 nm TiN top electrode (TE) is deposited via PVD, completing the stack. All samples undergo rapid thermal annealing (RTA) at 550 °C for 30 s to crystallize the ferroelectric layer. Device patterning is carried out using UV lithography followed by Ti/Au (5 nm/200 nm) contact deposition via electron-beam evaporation. Schematic illustrations of the MFM and MFIM capacitors are shown in Fig. 1(a) and (b), respectively. Electrical characterization is performed using a Keysight B1500 parameter analyzer equipped with B1530A waveform generators in a Lakeshore CRX-4K cryogenic probe station and the grazing incidence x-ray diffraction (GI-XRD) was obtained using a Bruker D8 Discover X-ray diffraction system.

III. Electrical Characterization and Analysis

All measurements (except leakage and GI-XRD measurements) are performed on devices first subjected to a wake-up operation (WU) at room temperature (RT). The wake-up operation consists of a 1 kHz bipolar signal with one thousand square pulses and a peak amplitude of 3.0 V at RT. Further, due to the differing insulator thicknesses of the MFM and MFIM capacitors, the total dielectric thickness is used for electric field calculation. Specifically, an 8 nm thickness corresponding to the HZO layer is used for the sample without ALO, while a combined thickness of 9.2 nm (8 nm HZO + 1.2 nm Al_2O_3) is used for the sample with ALO. The electric field is calculated as $E = V/t_{ox}$, where t_{ox} is the total insulator thickness, to maintain consistency across all electrical measurements performed in this study. Fig. 1(c) shows the polarization–electric field (*P–E*) characteristics of both devices measured at room temperature after wake-up, using a 10 kHz triangular bipolar signal with a peak amplitude of 3.5 V. The addition of the ALO inter-layer results in a slightly reduced remnant polarization and larger coercive fields [25]. The inset in Fig. 1(c) presents grazing-incidence X-ray diffraction patterns of the

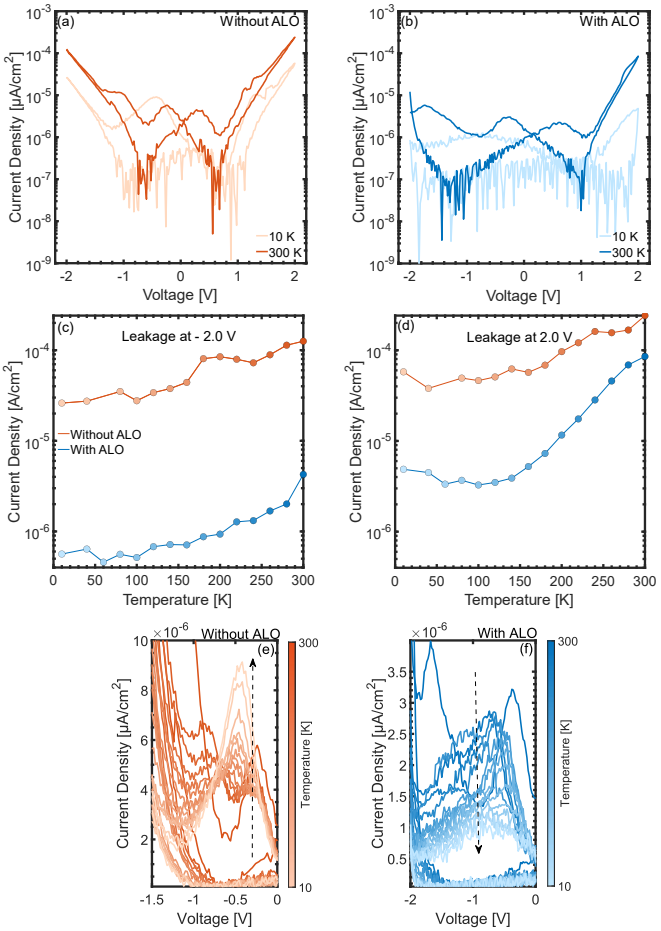

Fig. 4. *J-E* characteristics of the same pristine $Hf_{0.5}Zr_{0.5}O_2$ capacitor first measured at RT and measured from 300 K to 10 K for the samples (a) without ALO and (b) with ALO. Leakage currents at (c) -2.0 V and (d) 2.0 V across the temperature range for both the samples. Linear scale leakage current across all temperatures for the (e) without ALO and (f) with ALO samples where the colour bars indicate the temperatures.

two structures, recorded at an incidence angle of 0.5°. Both devices exhibit a diffraction peak at ≈ 30.5°, corresponding to the o(111)/t(011) phase, confirming the presence of the orthorhombic ferroelectric phase in HZO.

To study the temperature dependence of remnant polarization (P_r) and coercive fields (E_C), *P-E* characteristics are evaluated at multiple temperatures and can be seen in Figs. 2(a) and (b). Similar to Fig. 1(c), the devices are exposed to a 10 kHz triangular bipolar signal with a peak amplitude of 3.5 V after a wake-up operation, then cooled to 10 K, and the measurements are repeated. This measurement method ensures that temperature is the only variable in the study. As the temperature is lowered for either device, the gradual shift in the positive coercive field is quite evident. In contrast, no notable visual difference in the remnant polarization can be observed from the *P-E* characteristics for either device. To visualize the effect of temperature in more detail, the positive and negative remnant polarizations (P_r^+ and P_r^-) for both devices at each temperature can be seen in Fig. 2(c). A minor initial decrease in the remnant polarization is observed for both samples from 300 K to 280 K. However, beyond this point, the device without ALO exhibits a monotonic increase in remnant polarization down to 10 K. Notably, the remnant polarization at 10 K slightly exceeds its value at 300 K. This behavior is consistent with reports attributing enhanced low-temperature polarization to increased stabilization of the ferroelectric orthorhombic (o) phase, accompanied by a reduction in the monoclinic (m) and anti-ferroelectric tetragonal (t) phases at cryogenic temperatures [18],[19],[20],[21],[22]. The device with ALO shows a different trend, P_r increases from 280 K to approximately 140 K, beyond which it begins to saturate and subsequently decline. At 10 K, its P_r falls below the room-temperature value unlike the device without ALO. Earlier studies have reported that for thicker ferroelectric films, there is an expansion of the dead layer at the interfaces at cryogenic temperatures, which could lead to a reduction in remnant polarization [19]. Perhaps, the addition of an ultra-scaled approximately 1.2-nm-thick aluminium oxide inter-layer is sufficient to cause this phenomenon. Fig. 2(d) shows the temperature dependence on the positive and negative coercive fields (E_C^+ and E_C^-) for both the devices. As the temperature decreases, a clear increase in E_c^+ is observed for both samples which agrees with the Vopsaroiu model [23] extending it to lower temperatures. A similar temperature dependence was reported and modelled in [23], where a linear increase in the coercive field was observed between 493 K and 274 K, supported by electrical measurements. Reduced thermal energy and enhanced domain wall pinning at low temperatures necessitate higher fields for polarization reversal [6],[23],[24]. Interestingly, E_C^- remains nearly constant in the device without ALO, which may point to an underlying asymmetry in the energy landscape, potentially stemming from intrinsic material properties or asymmetric defect concentrations at the interfaces, favouring one polarization orientation. In contrast, the device with ALO exhibits a slight increase in E_C^- with decreasing temperature. This increase may suggest that the ALO inter-layer contributes to a partial reduction in switching asymmetry, potentially by screening internal built-in fields. It is also possible that the inter-layer modifies the spatial distribution of defects relative to free carriers, which could influence local field profiles and polarization switching behavior. The observed increase in coercive fields with decreasing temperature may be attributed to a combination of reduced trap-mediated screening and interfacial depolarization. At room temperature, trap-assisted tunneling likely provides additional charge that helps to screen ferroelectric polarization. As the temperature is lowered, this process becomes progressively weaker, reducing the availability of compensating charge [19]. In MFIM capacitors, this effect could be further amplified by the series-capacitance penalty of the ALO inter-layer, which redistributes the applied voltage between HZO and ALO. As a result, the effective field across the ferroelectric may be reduced, requiring a higher external field for polarization reversal. A related explanation was reported in [22], where suppressed charge-injection–assisted switching at low temperatures was linked to a reduction in remnant polarization at lower temperatures. While the exact interplay between these mechanisms remains open to further study, our results are

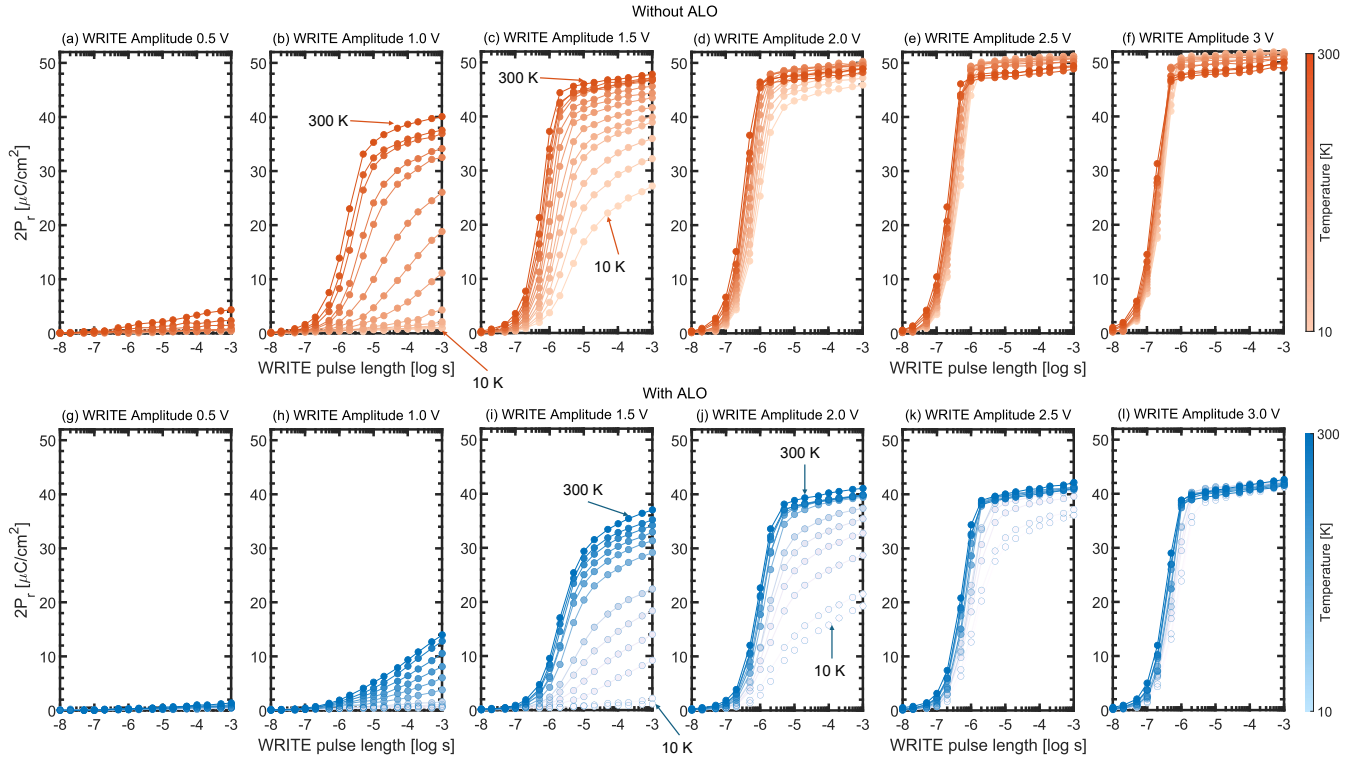

Fig. 5. Polarization switching dynamics of HZO capacitors with and without an ALO interlayer as a function of WRITE pulse width at various temperatures with different WRITE amplitudes where the colour bar indicates the temperatures. (a)–(f) correspond to the sample without ALO at WRITE amplitudes of 0.5 V to 3.0 V, respectively. (g)–(l) show the same for the sample with ALO.

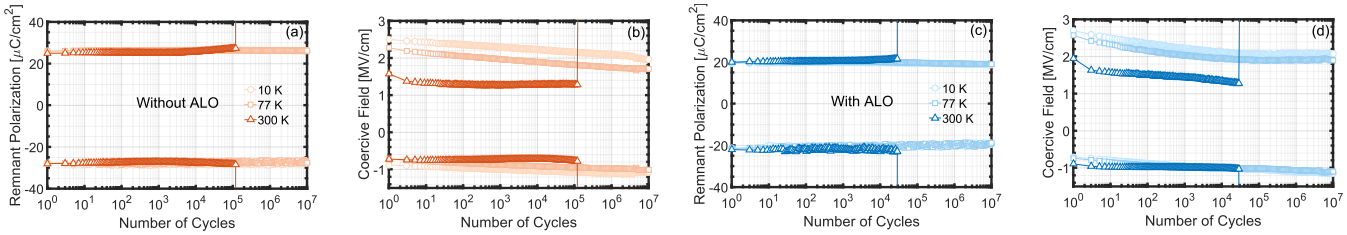

Fig. 6. Evolution of remnant polarization and coercive fields during endurance cycling of devices (a)–(b) without ALO and (c)–(d) with ALO at 300 K, 77 K, and 10 K. For all, the circular marker is 10 K, square marker is 77 K, and triangular marker is 300 K.

consistent with such interpretations.

Capacitance–voltage (*C–V*) characteristics of devices with and without ALO are shown in Fig. 3 for temperatures ranging from 300 K down to 10 K, measured at three frequencies (10 kHz, 100 kHz, and 1 MHz). At all frequencies, both devices exhibit the characteristic butterfly-shaped *C–V* response of ferroelectric HZO. With decreasing temperature, the *C–V* curves shift toward higher applied voltages while retaining the butterfly form, consistent with the trend observed in the *P–E* characteristics. In agreement with earlier reports [18], the overall capacitance magnitude decreases as temperature is lowered. The device with ALO consistently shows a lower peak capacitance than the device without ALO, which is attributed to the series addition of the Al_2O_3 interlayer capacitance and the associated depolarization effects. A frequency dependence is also evident. While both device types display dispersion between 10 kHz and 1 MHz, it is more pronounced in the device with ALO.

Current leakage measurements were conducted to investigate further the temperature dependence of leakage behavior in both capacitors. A pristine device was first measured at 300 K using a voltage sweep from − 2 V to + 2 V and back to − 2 V. The same device was subsequently cooled to 10 K, and the measurement was repeated. The device was then heated in steps back to 300 K, with the same leakage measurements performed at each intermediate temperature. Figs. 4(a) and (b) show the leakage current at 300 K and 10 K for the devices without ALO and with ALO, respectively. In either device, the leakage current is significantly lower at 10 K compared to 300 K, which is attributed to the suppression of thermionic emission at cryogenic temperatures. Figs. 4(c) and (d) display the leakage current values across the entire temperature range for both capacitors at ± 2 V. For the device without ALO, the leakage currents at − 2 V and + 2 V are nearly symmetrical and exhibit a near linear decrease with temperature, consistent with a thermionic emission-dominated transport mechanism. In contrast, the sample with ALO exhibits consistently lower leakage current across all temperatures and voltages, owing to

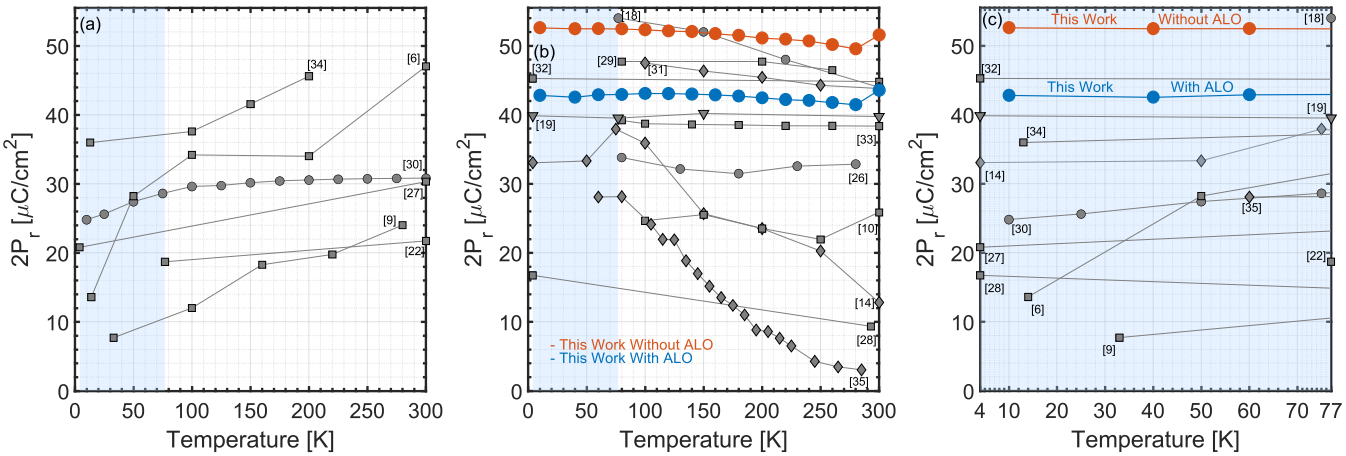

Fig. 7. Benchmarking of $2P_r$ at different temperatures reported in literature for devices operated at ≤3.5 V. (a) Studies where $2P_r$ decreases with decreasing temperature. (b) Studies where $2P_r$ remains stable or increases with decreasing temperature, including this work (with and without ALO). (c) Comparison within the cryogenic CMOS memory window (4 K –77 K), relevant for quantum computing applications. The regions coloured in blue highlight the cryo-CMOS memory temperature range.

the added tunneling barrier introduced by the aluminum oxide inter-layer. Interestingly, a pronounced asymmetry is observed in the device with ALO. The leakage current at − 2 V is nearly an order of magnitude lower than at + 2 V. This could be due to the ALO layer increasing the tunneling barrier under negative bias. Additionally, in Fig. 4(a), while the leakage current at ±2 V decreases at 10 K, a localized increase is seen near ≈ 0.6 V during the negative sweep, potentially due to polarization switching. To investigate this further, Figs. 4(e) and (f) show the negative sweep leakage currents for both devices on a linear scale. For the sample without ALO in Fig. 4(e), we observe that a current bump appears and becomes more pronounced as temperature decreases (as indicated by the arrow in the figure). This feature can be attributed to the polarization switching current, which may be enhanced by the emergence of the orthorhombic ferroelectric phase and suppression of monoclinic and tetragonal anti-ferroelectric phases at cryogenic temperatures [18],[19],[20],[21],[22]. At the same time, even having an ultra-scaled ≈ 1.2 nm aluminium oxide interlayer seems to prohibit this phenomenon. In contrast, a current peak is visible at room temperature for the sample with ALO in Fig. 4(f) but diminishes progressively at lower temperatures. This current variation suggests that the ultra-scaled (≈ 1.2 nm) ALO interlayer may inhibit phase evolution or suppress switching currents, possibly due to increased depolarization effects or interface-induced screening.

Fig. 5 illustrates the polarization switching dynamics of HZO capacitors with and without an ALO interlayer, as a function of WRITE pulse width, WRITE amplitude, and temperature. At a WRITE amplitude of 0.5 V [Figs. 5(a) and (g)], both devices exhibit negligible switching across all temperatures, with $2P_r$ remaining near zero. This behaviour confirms that 0.5 V is insufficient to overcome the coercive voltage in either device, consistent with previous findings on minimum switching thresholds in hafnia-based ferroelectrics. At 1.0 V, the sample without ALO [Fig. 5(b)] begins to show noticeable switching at higher temperatures, although switching remains suppressed at cryogenic temperatures. In contrast, the ALO sample [Fig. 5(h)] continues to exhibit minimal switching across the temperature range. This discrepancy aligns with the higher coercive fields measured in the ALO device [Fig. 2(d)], as reported in other studies where inter-layers increased the required switching voltage by altering the internal field distribution [11],[25]. With a WRITE amplitude of 1.5 V, the ALO sample [Fig. 5(i)] shows improved switching at higher temperatures, resembling the non-ALO device's behavior at 1.0 V. However, switching at 10 K remains negligible. Meanwhile, the non-ALO device [Fig. 5(c)] shows consistent polarization reversal across all temperatures, albeit with lower $2P_r$ at reduced temperatures. This behavior is expected due to stronger domain wall pinning and reduced domain mobility at low thermal energies. As the WRITE amplitude increases further from 2.0 – 3.0 V [Figs. 5(d–f), and (j–l)], both devices show enhanced switching. At 3.0 V, the non-ALO device demonstrates nearly uniform switching across all temperatures for pulse widths up to ~500 ns, with the $2P_r$ at 10 K even exceeding that at 300 K [Fig. 5(f)]. This observation agrees with the low-temperature trends seen in Fig. 2(c) and supports the view that higher fields can compensate for kinetic limitations at cryogenic temperatures [6],[9]. While improved at higher voltages, the ALO device still exhibits stronger temperature dependence. The $2P_r$ at 10 K remains below that at room temperature, and the switching uniformity is not as robust as in the non-ALO counterpart. This behavior may result from increased depolarization fields, interface screening, or inhibited domain wall motion introduced by the ultra-thin ALO layer, all of which are known to influence switching performance in scaled ferroelectric stacks. These results highlight a fundamental trade-off: while the ALO inter-layer effectively suppresses leakage (see Fig. 4), it also imposes switching limitations that must be balanced when designing ferroelectric devices for cryogenic logic and memory applications. The effect of this trade-off is found to be stronger at cryogenic conditions as compared to room temperature operation.

Fig. 6 summarizes the evolution of remnant polarization and coercive fields during endurance cycling for devices with and without the ALO inter-layer. All devices were first subjected to a wake-up sequence of 1000 bipolar square pulses (3.0 V, 1 kHz, RT). Endurance cycling was then carried out using triangular bipolar pulses (3.5 V, 10 kHz), consistent with the *P*–*E* measurements in Fig. 1(c) and Fig. 2, at 300 K, 77 K, and 10 K. For the MFM devices [Figs. 6(a)-(b)], robust switching is observed at 77 K and 10 K up to 10^7 cycles, while the 300 K device experiences breakdown earlier. In contrast, the MFIM devices [Figs. 6(c)-(d)] also maintain endurance beyond 10^7 cycles at cryogenic temperatures but exhibit a modest reduction in remnant polarization with cycling. These observations mirror the trends in Fig. 2, where the ALO devices consistently show slightly lower $2P_r$ than their non-ALO counterparts. A gradual imprint effect, reflected in the shift of the coercive field with cycling, is evident at 77 K and 10 K in both device types. However, the imprint appears more stabilized in the MFIM devices, where the change in the positive coercive field begins to saturate with cycling. At 300 K, however, the MFIM devices exhibit marginally lower endurance than their MFM counterparts, consistent with earlier reports on similar interlayer-based stacks [13]. This behaviour can be attributed to the role of the ALO inter-layer in suppressing leakage and limiting charge injection during field cycling. In addition, the presence of the inter-layer introduces voltage division across the stack, requiring a higher external field to achieve polarization switching [25]. The increased external stress and limited dynamic charge compensation, may accelerate interfacial degradation and contribute to earlier breakdown at room temperature. At cryogenic temperatures, where trap activity and leakage are inherently reduced, this trade-off becomes less pronounced, and the MFIM devices demonstrate stable switching and endurance beyond 10^7 cycles. This behaviour suggests that while the ALO devices sacrifice some polarization amplitude, they exhibit more stable switching fields under prolonged cycling at cryogenic temperatures. Taken together with their reduced leakage (Fig. 4), the capacitors with the ALO inter-layer may offer advantages for FeFET integration where memory window stability is critical, whereas the capacitors without the inter-layer, with higher remnant polarization, may be more suitable for FeRAM type cryogenic applications.

Finally, to assess the performance of our HZO-based ferroelectric capacitors, we benchmarked the 2 × remanent polarization ($2P_r$) against state-of-the-art ferroelectric capacitors reported in the literature, focusing on measurements performed at cryogenic temperatures under an operating voltage ≤ 3.5 V. The benchmarking results are summarized in Fig. 7. Specifically, Fig. 7(a) includes reports where $2P_r$ decreases with decreasing temperature ([6], [9], [22], [27], [30], [34]), while Fig. 7(b) shows studies where $2P_r$ remains stable or increases as temperature is reduced ([10], [14], [18], [19], [26], [28], [29], [31]–[33], [35]), along with the results of this work (with and without ALO). Fig. 7(c) highlights the temperature window relevant for CMOS-compatible cryogenic memory in quantum computing applications (4 K – 77 K, shaded in blue [1]). Within this regime, our devices exhibit competitive reported $2P_r$ values, with the sample without the ALO inter-layer consistently ~10 μC/cm^2 higher than the inter-layer case. To further substantiate these trends, the Supplementary Information includes: (i) a comprehensive benchmarking table listing ferroelectric material, thickness, interlayer material and thickness, applied voltage, and observed temperature dependence across reported studies, (ii) measured variation across five independent devices each for both samples with and without ALO, showing consistent $2P_r$ trends with temperature from 300 K down to 10 K and (iii) an inter-layer benchmarking comparison, where our MFIM devices are evaluated against other inter-layer-based capacitors from the literature. While many of these prior reports show strong temperature-driven variation in $2P_r$, our MFIM structures exhibit comparatively more stable and consistent performance, across the cryogenic temperature range. These results confirm that our HZO capacitors, with or without an ALO inter-layer, deliver competitive and consistent polarization performance at cryogenic temperatures and are promising candidates for future low-temperature memory applications.

IV. CONCLUSION

This study comprehensively evaluates the role of an ultrathin aluminium oxide inter-layer on the cryogenic behaviour of $Hf_{0.5}Zr_{0.5}O_2$-based ferroelectric capacitors. We demonstrate that MFIM structures significantly reduce leakage and modify coercive switching behavior, albeit with some suppression in remnant polarization and switching robustness at cryogenic temperatures. In contrast, MFM structures maintain strong and uniform switching even at 10 K, especially under a 3.0 V WRITE bias. Endurance measurements confirm stable operation up to 10^7 cycles without hard breakdown at cryogenic temperatures, and *C*–*V* analysis reveals consistent ferroelectric switching across frequencies. Comparative benchmarking reveals that both configurations provide top-performing cryogenic ferroelectric devices at low operating voltages. Similar trends were observed across multiple devices. These findings offer valuable design guidelines for advancing low-power, non-volatile cryogenic memory systems and integrating ferroelectric components into quantum computing infrastructure.

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