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Doping Incorporation in InAs nanowires characterized by capacitance measurements

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Sn and Se doped InAs nanowires are characterized using a capacitance-voltage technique where the threshold voltages of nanowire capacitors with different diameter are determined and analyzed using an improved radial metal-insulator-semiconductor field-effect transistor model. This allows for a separation of doping in the core of the nanowire from the surface charge at the side facets of the nanowire. The data show that the doping level in the InAs nanowire can be controlled on the level between 2×10^{18} to 1×10^{19} cm^{-3}, while the surface charge density exceeds 5×10^{12} cm^{-2} and is shown to increase with higher dopant precursor molar fraction. © *2010 American Institute of Physics.* [doi:10.1063/1.3475356]

I. INTRODUCTION

The metal-oxide-semiconductor field-effect transistor (MOSFET) technology follows Moore's law for device scaling, where transistors with better performance are developed for each generation. The wrap-gate nanowire technology offers a possibility to extend the validity of Moore's law beyond that of traditional planar devices due to improved electrostatic control,[1,2] that can easily be combined with high-mobility III/V nanowire channels.[3,4] However, one major requirement for the transistor design is the ability to increase and control the carrier concentration, which is normally achieved by doping. Even though doped nanowires have been presented in the literature,[5,6] there is still a need to improve the control and understanding of the carrier concentration in nanowire systems.

Traditionally, the carrier concentration is determined by Hall measurements, but due to their one-dimensional geometry, this technique cannot be applied to the nanowires. Instead, the common approach is to study the transport in gated nanowires and deduce the carrier concentration from the threshold voltage. However, this method is based on the gate capacitance that often is calculated only. Additionally, it is known from atom probe tomography studies that donor atoms tend to preferentially incorporate at the surface of the nanowire.[7] This affects the capacitance of the structure and hence the determined carrier concentration. It is thus of great importance to measure experimentally and study the capacitance for individual[8,9] as well as arrays of nanowires.[10]

We present an experimental study of vertical InAs nanowire capacitors. We vary the diameter to evaluate the nanowire carrier concentration by employing a radial metal-insulator-semiconductor field-effect transistor (MISFET) model. By varying the dopant precursor molar fraction we demonstrate how the dopants are introduced into the core of the nanowire, but also show how additional charges are formed at the surface of the nanowire during the doping process. In order to account for the two doping incorporation paths, we add the surface charge density to the radial MISFET model. The new model is shown to be adequate to explain the measured threshold voltages of capacitance-voltage (CV) characteristics and also allows quantifying the nanowire carrier concentration and the surface charge at the side facets of the nanowire.

II. EXPERIMENTAL DETAILS

The nanowire capacitor fabrication starts by defining Au seed particles with a density of 1 particle/μm^2 using electron beam lithography. After Au liftoff, the samples are transferred to an Aixtron AIX 200/4 low-pressure metal organic vapor phase reactor equipped with trimethylindium, tetraethyltin (TESn), di-tertiarybutyl selenide (DTBSe), and AsH$_3$ precursors. InAs nanowires are grown at a temperature of 450 °C at a V/III-ratio of 68. The dopant precursor molar fractions were varied between 1×10^{-7} and 10×10^{-7}. It was observed that the nanowire length decreased linearly with increasing TESn molar fraction; from 1.4 μm for TESn free growth down to 0.9 μm for TESn molar fraction of 6.3 $\times 10^{-7}$ with 5 min growth time, therefore the growth time was adjusted to obtain about 1 μm ($\pm 5\%$) long nanowires. In order to account for the length variation due to different Au particle diameter,[11] the nanowire length in each array were determined from scanning electron microscope (SEM) inspection.

In order to make the capacitors, the nanowires were coated with a 10 nm-thick HfO$_2$ layer deposited by atomic layer deposition (250 °C) directly after the growth and followed by thermal evaporation of a 100 nm-thick SiO$_x$ spacer layer. A nominally 50 nm-thick Cr and 100 nm-thick Au bilayer was deposited by sputtering, which resulted in roughly 1/3 of the thickness on the nanowire facets. The nanowire arrays were protected with a negative resist and the samples were wet etched to remove the unprotected Cr:Au

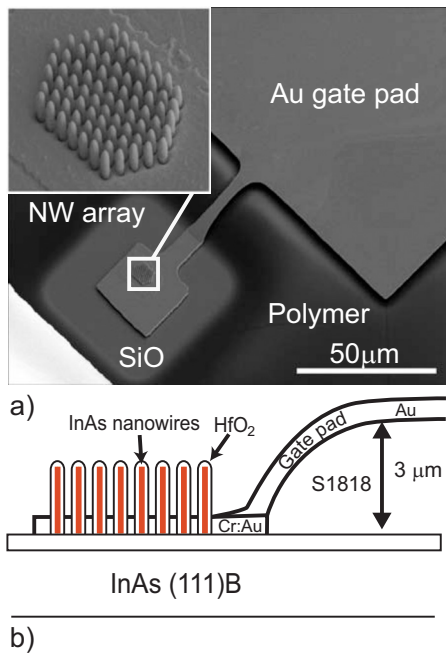a)Electronic mail: gvidas.astromskas@ftf.lth.se.

FIG. 1. (Color online) (a) SEM image of the finished capacitor. The inset shows a magnified image of the nanowire array. (b) Schematic of the nanowire capacitor structure. The frame capacitor is placed on top of S1818 surrounding the nanowire capacitors.
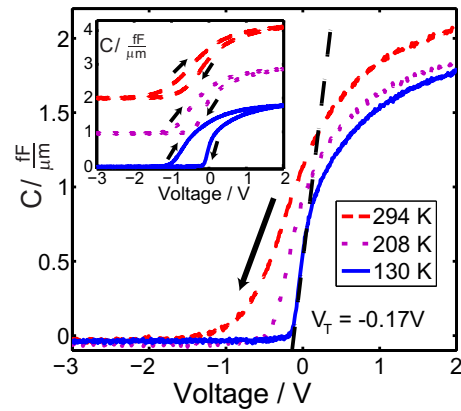

FIG. 2. (Color online) Measured CV characteristics of the nonintentionally doped InAs nanowire capacitor at different temperatures. The average nanowire diameter in this capacitor is 53 nm. The threshold voltage is linearly fitted on the down sweep of the CV curve. The inset compares the hysteresis obtained when voltage sweeping direction is changed, as marked by arrows (data are offset for clarity).

layer. The samples were spin-coated with a S1818 resist and the nanowire arrays were made accessible by means of optical lithography. The slope in the resist profile of S1818 allowed connecting the elevated gate pad to the nanowire capacitor array, as shown in Fig. 1. The device preparation was then finished by a 500 nm-thick sputtered Au gate pad defined by optical lithography and wet etching. The double step metal deposition process is used to reduce the parasitic capacitance of the gate pad. The fabricated samples contained capacitor arrays with varying nanowire diameter in the range of 44 to 54 nm with nominally 79 nanowires per array for Sn doped samples, while 2500 nanowires were defined in Se doped samples. The nanowire diameters were determined from SEM images taken after growth and the diameter spread within a single device was found to be less than 5%.

The fabricated capacitors were evaluated with an Agilent 4294A impedance analyzer in a Cascade probe station, equipped with a temperature control unit. The measurements were done with two probes of which one was placed on the nanowire gate pad and the other on a large (1–50 nF) frame capacitor in series with the nanowire capacitor. The complex impedance was measured at 100 MHz using a small AC modulation ($\Delta V = 20$ mV) on top of a dc bias V in the range from -3 to $+2$ V. The high measurement frequency was used to obtain a good signal to noise ratio and to suppress the influence of minority carriers as well as defect response at reverse bias. The capacitance was extracted from the measured impedance using a capacitance in series to resistance model, as less than 1 pA leakage currents were measured by DC. The typical capacitances were 700–1000 fF for Sn doped samples and 5–7 pF for the Se doped samples, while the parasitic plate capacitance was about 10% and 40% of

the total capacitance for 2500 and 79 nanowire capacitors, respectively. The parasitic plate capacitance was subtracted from the data to simplify the data analysis.

A. Determination of threshold voltages

We start by analyzing the measured CV characteristics of the nominally undoped InAs nanowire capacitor array at different temperatures, shown in Fig. 2. It is apparent that the CV curves shift toward more negative biases and that the accumulation capacitance increases as the temperature is raised. As nonintentionally doped InAs nanowires have a large background carrier concentration due to carbon incorporation,[12] the shift cannot be related to thermal activation of carriers across the band gap. A similar observation is also reported in the InAs and InSb MOSFET structures[13] and may after a more detailed analysis be attributed to thermal activation at the interface or within the dielectrics.

The CV curves of nanowire capacitors have a measurable hysteresis, which is present at all temperatures as shown in the inset of Fig. 2. As noted, the down sweep varies with temperature, but the up sweep is observed to be almost temperature independent. We interpret the degree of hysteresis to depend on charge trapping in the dielectrics as well as at the InAs/HfO_2 interface. As we experimentally observed that the up sweep curve slowly relaxes to the down sweep CV profile over time (not shown), only the capacitance measured during the down sweep of voltage ($+2$ V $\rightarrow -3$ V) was used in this study.

The CV characteristics of nominally undoped and nanowires grown under TESn molar fraction are compared at 130 K in Fig. 3(a). Similar curves were also obtained for the Se doped capacitors. It is apparent, that the use of dopant precursors during the growth affects the shape and the magnitude of the nanowire CV characteristics. The larger the dopant precursor molar fraction, the less steep is the CV curve. Also, at higher doping levels, the dopant precursor molar fraction considerably raises the depletion capacitance, which saturates at a level above zero. The effect of the nanowire diameter on the shape of the CV curves is less pronounced,
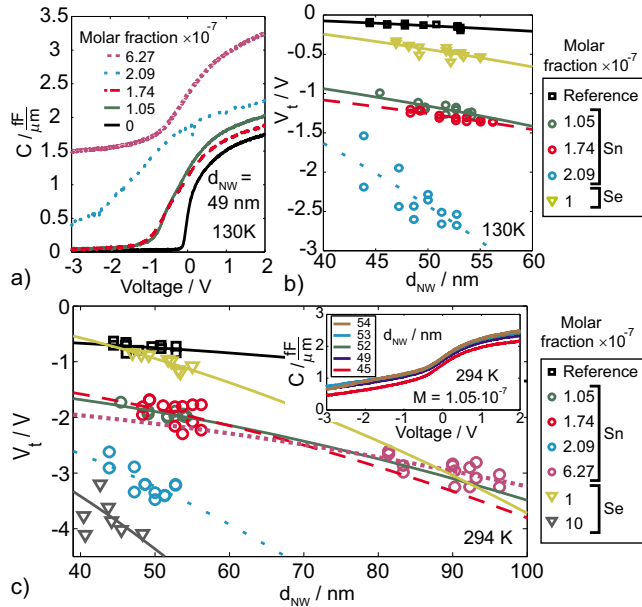
FIG. 3. (Color online) (a) Comparison of CV characteristics of different TESn molar fractions, (b) threshold voltage (V_T) vs nanowire diameter (d_{NW}) at 130 K, and (c) at room temperature. Solid curves show the best fit to the radial MISFET model. The inset in (c) compares CV characteristics of the sample grown with TESn precursor molar fraction of 1.05×10^{-7}.

only a minor increase is observed, as shown in the inset in Fig. 3(c). Also, the depletion capacitance for nanowires with different diameter remains essentially constant. Therefore, we conclude that different factors contribute to the CV profile when comparing capacitors with different dopant precursor molar fractions versus capacitors with different nanowire diameters.

In order to quantify the change of CV characteristics at different diameters or dopant precursor molar fractions, the threshold voltage (V_T) is determined for each CV curve by linearly extrapolating the CV profile around the inflection point to zero capacitance, as shown in Fig. 2. We plot V_T versus d_{NW} in Figs. 3(b) and 3(c) and observe that V_T decreases as the diameter is increased, as expected for a radial MISFET type device.[14] Interestingly, for doped samples using both TESn and DTBSe, the V_T data sets shift toward more negative biases and the magnitude of the shift depend on the dopant precursor molar fraction. This is consistent with the qualitative observations from the CV profiles. The threshold voltage is determined using linear extrapolation as measured CV characteristics do not follow the standard $1/C^2$ behavior used in planar geometries and explicit analytical models for nanowire CV relation are not yet available.

B. Modified radial MISFET model

It is observed in Fig. 2 that the depletion capacitance reaches zero under reverse bias, indicating that the nanowires are depleted. In this regime, the nanowire capacitor can be modeled as a simple radial MISFET device,[14] as shown in Fig. 4. The structure of the nanowire capacitor is composed of a semiconductor cylinder with radius R and constant carrier concentration (N_D) and is surrounded by a dielectric layer with thickness t_{ox}. We also add a surface charge density

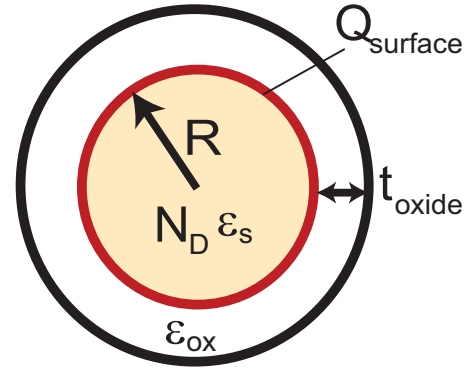FIG. 4. (Color online) (a) Schematic of the nanowire cross-section with surface charge density (Q_s) at the nanowire/oxide interface.

(Q_s) at the perimeter between the InAs nanowire and the HfO$_2$ in order to include threshold voltage (V_T) shifts in the model. Using Gauss law we then obtain the relationship

$$V_T = V_{FB} - \frac{q N_D R^2}{4 \varepsilon_0 \varepsilon_s} - \frac{q N_D R^2}{4 \varepsilon_0 \varepsilon_{ox}} \ln\left(\frac{R + t_{ox}}{R}\right)$$
$$- \frac{q Q_s R}{4 \varepsilon_0 \varepsilon_{ox}} \ln\left(\frac{R + t_{ox}}{R}\right). \quad (1)$$

Here, V_{FB} is the flat band voltage, ε_0 is the permittivity of vacuum, while ε_{ox} and ε_{InAs} are relative static dielectric constants of HfO$_2$ and InAs, respectively, with q being the elementary charge. The equation is valid under the full depletion approximation and for capacitors without inversion layer, which is the case for nanowires with zero depletion capacitance.

The formula can be simplified by making a first order Taylor expansion of the logarithm terms

$$V_T \approx V_{FB} - \frac{q Q_s t_{ox}}{4 \varepsilon_0 \varepsilon_{ox}} - \frac{q N_D t_{ox}}{4 \varepsilon_0 \varepsilon_{ox}} R - \frac{q N_D}{4 \varepsilon_0 \varepsilon_s} R^2$$
$$= V_0 + \frac{q N_D}{4 \varepsilon_0}\left(\frac{t_{ox} R}{\varepsilon_{ox}} - \frac{R^2}{\varepsilon_s}\right). \quad (2)$$

It is straightforward to identify that qualitatively the slope and the nonlinearity in the V_T versus nanowire diameter (d_{NW}) dependence will correspond to N_D, while the offset (V_0) will be proportional to Q_s.

Fittings to Eq. (1) are included in Figs. 3(b) and 3(c) as solid lines. We note a good agreement between the measured data and the model at the low temperature (130 K) and for devices that have a low doping level, whereas we find a larger scattering in the data at higher temperatures and for devices that show a nonzero depletion capacitance. We attribute the capacitance minima to the trap and minority carrier responses, which become stronger with increasing temperature and higher doping levels. We note that the depletion capacitance of nanowires is affected by the stray capacitances present in the samples. When the nanowire capacitors are fully depleted, the measured depletion capacitance is corrected to zero, allowing more precise V_T evaluation. However, this correction cannot be applied when the nanowires no longer are fully depleted, but exhibit a capacitance minima, leading to an increased scattering in the data.
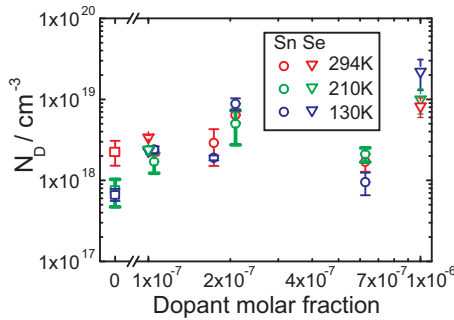
FIG. 5. (Color online) Nanowire doping concentration (N_D) vs the dopant precursor molar fraction. Errors are estimated as a 2σ deviation from the least square minima point. The nanowires grown with TESn precursor molar fraction of 6.27×10^{-7} have almost two times larger diameter than the size of the Au particle.

C. Nanowire doping

In order to determine the nanowire carrier concentration, we fit Eq. (1) to the V_T-d_{NW} plots using a least square method as shown in Fig. 3(b). A good fit is obtained for samples, exhibiting zero depletion capacitance, as discussed above. It is clear that not only the V_T is shifting with increasing precursor molar fraction, but also the slope of the fitted curves is increased as well. This indicates that higher dopant precursor molar fractions lead to higher doping levels in the nanowires. We also fit the room temperature data as shown in Fig. 3(c), where the same increase in the slope is observed. The only exception is the sample grown under the TESn precursor molar fraction of 6.27×10^{-7}. However, in this case, the large TESn precursor molar fraction also doubled the diameter of the nanowire.

Using the fitted data, we deduce the carrier concentration for all samples at three different temperatures as shown Fig. 5. The first observation is the increasing carrier concentration for higher dopant precursor molar fractions at all temperatures. Second, the carrier concentration shows little change with temperature, which is the case for semiconductors with shallow donor levels under a complete ionization. Therefore, we can conclude that Sn and Se are incorporated into InAs nanowire as donors, agreeing with results obtained using gated single nanowire structures.[15] The sample grown under TESn precursor molar fraction of 6.27×10^{-7} shows lower carrier concentration than samples grown under lower precursor flows, but this can be accounted by the doubled nanowire diameter, which effectively reduces the donor concentration.

D. Doping induced surface charges

We now analyze the shift in the nanowire CV characteristic in more detail and determine the surface charge density. We examine the offset voltage V_0, which is plotted in Fig. 6(a) as a function of dopant precursor molar fraction. Due to the increased scattering in V_T for not depleted nanowires, we focus our analysis to fully depleted nanowires. Here, we observe an increase in $|V_0|$ with higher precursor molar fraction. This indicates that the surface charge is related to the donor density where donors may incorporate at side facets of the nanowire.
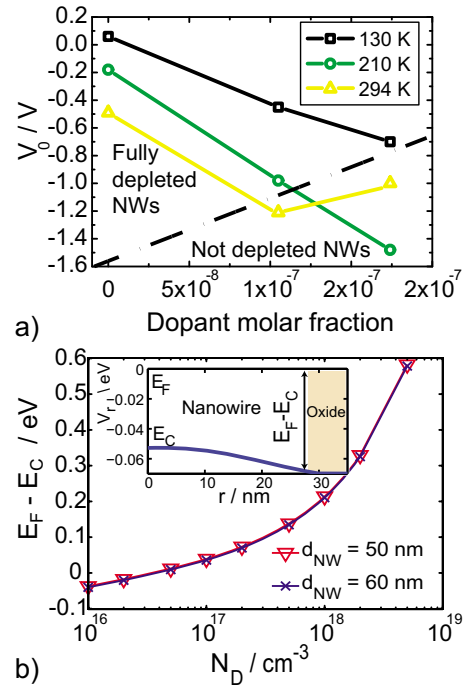

FIG. 6. (Color online) (a) Extracted offset voltage (V_0). The dashed line separates measured CV characteristics between fully and not depleted nanowires. Lines are to guide the eye. (b) The potential shift due to the state filling in the doped InAs nanowire. The inset shows a calculated nanowire band diagram for the doping density of 2×10^{17} cm^{-3}. A small band bending occurs due to the termination of the electron wave functions at the interface to the oxide, where an infinite quantum well is assumed.

We also have to take into account the strong shift in the Fermi level position as the doping level is increased in particular due to the low density of states of InAs.[16] We simulate the band diagram of the InAs nanowire using the method presented in Ref. 17, where the Fermi level position is adjusted to obtain zero net charge in the nanowire in order to simulate a flat band condition. We then deduce the difference between the Fermi level (E_F) and the conduction band edge (E_C) at the interface between InAs and HfO$_2$, as shown in Fig. 6(b). From the data, we note that the state filling cannot explain the observed V_0 increase by itself, because the maximum calculated E_F-E_C is less than 0.6 V, while the determined V_0 exceed 1 V. Although we do not include effects of Fermi level pinning at the interface or effects due to the nonparabolicity in the conduction band, this would only reduce the Fermi level shift. Hence our estimated Q_s values are regarded as a lower bound.

The dopant induced surface charge density is determined from the offset of the V_T-d_{NW} curve with respect to the reference sample and after subtracting the Fermi level shift due to the nanowire doping. This is calculated as: $qQ_{doping}t_{ox}/4\varepsilon_0\varepsilon_{ox} = V_0^{doped} - V_0^{ref} - [(E_F-E_C)^{doped} - (E_F-E_C)^{ref}]$ and is presented in Table I. It is clear that higher dopant precursor molar fractions cause higher surface charge densities. The temperature variation in Q_{doping} may be attributed to thermal activation of carriers from the dielectrics or the interface. The increasing surface charge density indicates that donors accumulate at the nanowire facets during the nanowire growth and that they are electrically active and contribute to the capacitive response of the nanowire. Similar doping pro-

TABLE I. Dopant induced surface charge density (Q_{doping}).

Molar fraction/10^{-7}	T (K)	Q_{doping} (cm^{-2})
1.1 (TESn)	130	5.22×10^{12}
1.1 (TESn)	208	1.15×10^{13}
1.7 (TESn)	130	1.05×10^{13}
1.7 (TESn)	208	2.42×10^{13}

file occurs in Ge nanowires, where large nanowire tapering is clearly responsible for the donor incorporation at the surface.[5,7] The CV characteristics broaden with increasing doping level as shown in Fig. 3(a), consistent with increasing trap density at the nanowire surface. For conventional capacitors, the broadening is usually associated with an energy dependent trap distribution. However, to estimate the trap density from our narrow band gap CV profiles, a good nanowire CV model is required that accounts for the carrier distribution in the InAs nanowire capacitor including the low density of states, the reduced dimensionality in the nanowire, the minority carriers, energy dependent defect profiles, and different doping profiles.

The offset voltages, and the surface charge density, of the Se doped samples were also evaluated from the data in Fig. 3(c). Interestingly, the obtained value for the low doped sample is close to V_0^{ref} independent of temperature. This indicates that Se incorporates less effectively at the nanowire surface as compared to Sn. A careful analysis also indicates a change of sign for this sample, although within the experimental error.

III. CONCLUSIONS

We evaluated Sn and Se doped InAs nanowires using a CV technique and deduced the carrier concentration and the surface charge density using a modified radial MISFET model. We observe that nanowire carrier concentration increases with the dopant precursor molar fraction. We also observe a shift in the nanowire threshold voltage with higher dopant precursor molar fractions that we attribute to a surface charge density related to donor incorporation at the nanowire facets. We also observe that the surface charge density increases with higher dopant precursor molar fraction.

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