III-V Nanowire Complementary Metal-Oxide Semiconductor Transistors Monolithically Integrated on Si

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Published in:
Nano Letters

DOI:
10.1021/acs.nanolett.5b02936

2015

III−V Nanowire CMOS Monolithically Integrated on Si

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III−V semiconductors have attractive transport properties suitable for low-power, high-speed complementary metal-oxide-semiconductor (CMOS) implementation, but major challenges related to co-integration of III−V n- and p-type metal-oxide-semiconductor field-effect transistors (MOSFETs) on low-cost Si substrates have so far hindered their use for large scale logic circuits. Using a novel approach to grow both InAs and InAs/GaSb vertical nanowires of equal length simultaneously in one single growth step, we here demonstrate n- and p-type, III−V MOSFETs monolithically integrated on a Si substrate with high I_{on}/I_{off} ratios using a dual channel, single gate-stack design processed simultaneously for both types of transistors. In addition, we demonstrate fundamental CMOS logic gates, such as inverters and NAND gates, which illustrate the viability of our approach for large scale III−V MOSFET circuits on Si.

Keywords: III−V, CMOS, nanowire, inverter, NAND, InAs, GaSb, low-power logic, Si

Geometric scaling has for decades been the main technology drive for integrated Si circuits whereas materials integration plays an important role in the continued technology evolution. In future generations, III−V semiconductors are considered candidates to replace Si as channel material in MOSFETs due to their high mobilities and injection velocities that will enable voltage scaling to reduce the power consumption at maintained performance[1]. The recently demonstrated superior performance of III−V MOSFETs as compared to their Si counterparts[2] may be used for CMOS either in a single channel, e.g. InGaAs[3], or a dual channel, e.g. InGaAs/Ge[4, 5] or InAs/GaSb[6] approach, with

benefits in simplicity for the single channel and performance for the dual channel approach. Previous efforts to integrate III−V materials on a Si platform have involved either transfer of channel material grown on a separate substrate[4, 6-11] or have exploited innovative growth techniques, such as aspect ratio trapping[12], rapid melt growth[3], lateral overgrowth[13] or template assisted growth[14], to avoid high defect densities. Until now, a two-step transfer technique of molecular beam epitaxy (MBE) grown InGaSb and InAs layers used by Nah et al.[8] has been the only successful integration of both n- and p-type III-V materials into CMOS circuits on Si substrates. However, such methods are challenging to implement for large scale manufacturing due to the high cost of the initial wafers and the limited wafer size. In contrast, nanowire growth enables high III−V crystal quality on various substrates e.g. Si, as strain may relax radially[15] and wafer scale device fabrication has been demonstrated[16]. While there have been several reports on vertical III-V nanowire n-MOSFETs on Si[17, 18], including demonstration of RF-circuits[19], demonstrations of p-MOSFET integration have been lacking. Here we present fabrication of fundamental III−V CMOS digital circuits on Si in a vertical device layout comprising a gate-all-around nanowire transistor architecture, demonstrating a straightforward processing path for dual channel, single gate-stack, all III−V CMOS on Si.

The vertical device geometry is attractive, since it allows for aggressive gate length scaling due to the superior electrostatics of the gate-all-around geometry and a small device footprint enabling high density circuits. In addition, Yakimets et al. have predicted power savings of 10-15% for a vertical device layout as compared to a lateral geometry for the 7 nm technology node[20]. In this work we have focused on InAs and GaSb as the channel materials based on their respective high electron and hole mobilities suitable to achieve high performance of both n- and p-type MOSFETs[1] and demonstrate the growth of both materials on Si substrates by metal-organic vapor phase epitaxy (MOVPE) in a single growth step. The growth step reduces the need for complex processing simplifying fabrication saving cost and time. Both n- and p-type MOSFETs exhibit high I_{on}/I_{off} ratios using the same gate stack, which is known to be a critical concern for III−V MOSFETs.

n-InAs and p-GaSb nanowire segments were sequentially grown from electron beam lithography (EBL) patterned Au-particles of different sizes by the vapour-liquid-solid mechanism as displayed in Figure 1a-c. The substrate is high resistivity p-type Si with a 260 nm highly n-doped InAs layer that enables a low access resistance, straightforward device isolation, and high frequency operation[21], which are substantial benefits as compared to growth approaches directly on Si[17, 22]. To achieve selective growth of both types of nanowires, we exploit the fact that the chemical potential of material dissolved in an Au particle during growth is increased with decreasing particle size due to the higher surface-to-volume ratio. Eventually, the chemical potential approaches that of the gas phase, reducing the driving force for material transport to the particles what is known as the Gibbs-Thompson effect[23]. Since the solubility for Sb in Au is small, the growth rate of GaSb is highly sensitive to the transport of Sb to the particle and thus for sufficiently small diameters, the growth can be completely suppressed. This size selective growth mechanism can be exploited for co-integration of InAs and InAs/GaSb nanowire arrays on the same Si substrate using a single growth run (Figure 1d) by first growing InAs and subsequently GaSb, and by precisely controlling the geometry and growth conditions as discussed in the following.

Scanning electron microscopy (SEM) inspection of nanowire arrays with different Au seed particle diameters (d_{Au}) and pitches showed a diameter increase in the top segment of the nanowires for Au particles with d_{Au} > 30 nm (Figure 2a). Transmission electron microscopy (TEM) with energy dispersive X-ray spectroscopy (XEDS) analysis (Supporting information figure S1) revealed that the diameter increase corresponds to the transition from InAs to GaSb. Such diameter increase has previously between attributed to the increased solubility of group III material in the Au particle in the presence of Sb[24]. For $d_{Au} \leq 30$ nm, no diameter increase could be discerned in SEM (Figure 2a) and TEM analysis of wires from such arrays reveal that either no or only a very short GaSb segment has been grown. To study the dependence of Au diameter and pitch on the resulting nanowire

76 dimensions, the lengths and diameters of the InAs and GaSb segments were determined using the
77 image analysis software NanoDim[25]. The length of the GaSb segments was found to increase with
78 increasing d_{Au} while the length of the InAs segments exhibited the opposite trend (Figure 2c). The
79 growth rate of InAs nanowires grown under similar conditions has been previously investigated and
80 although there is a complex dependence on the exact array geometry and growth time, the rate was
81 found to always decrease with Au diameter[12]. The observation of increased growth rate of GaSb for
82 increasing d_{Au} is in accordance with what is predicted from the Gibbs-Thomson effect and
83 corroborates previous results[23]. It can therefore be concluded that for $d_{Au} \leq 30$ nm the growth of a
84 GaSb segment is completely suppressed due to an insufficient supply of Sb for nucleation. This
85 difference in growth rate between InAs and GaSb can be exploited to precisely control the nanowire
86 length such that the InAs and InAs/GaSb nanowires reach the same final height which simplifies
87 device processing. The possibility to select geometry and growth conditions to achieve similar lengths
88 for the two types of nanowires simplifies the processing and device integration significantly since a
89 common gate level can be used for both InAs and GaSb MOSFETs.

90

91 The length of the InAs segments was found increase with increasing nanowire pitch (Figure 2e). This
92 effect can be attributed to the increasing competition for available precursor material collected from
93 the substrate surface between the nanowires for decreasing pitch[12]. In contrast, the GaSb segments
94 displayed no decrease in length down to 300 nm pitch, indicating that there is no competition for
95 material collected from the substrate most likely due to the longer distance to the substrate and a
96 shorter diffusion length of the precursors resulting in a smaller collection area. The diameters of both
97 segments were found to be independent of the Au pitch (Figure 2d) demonstrating that the
98 dependence of the InAs segment length on the pitch is not related to the nanowire diameter.

99

Transmission electron microscopy (TEM) was used to study InAs and InAs/GaSb nanowires grown from different d_{Au} (Figure 2h,i). The diffraction patterns from the InAs and the GaSb segments correspond to the wurtzite and zincblende crystal structures, respectively. Both segments are pure without any mixed crystal phases and the InAs segments have a stacking fault density of around 30 μm^{-1} and the GaSb segments have no stacking faults indicating a high crystal quality for both materials. XEDS analysis of the atomic constituents of the InAs segment revealed small amounts of Ga and Sb in a shell around the wire (supporting information figure S1). The thickness of this GaSb shell, which is formed during the growth of the GaSb segment, was calculated from the relative Ga content and the cross-section of the nanowire to be 1 nm.

Drive current matching between n- and p-type MOSFETs necessary for optimized circuit operation can be achieved by varying the number of nanowires in the two type of arrays. Thus far, we have demonstrated that the distance between InAs and InAs/GaSb nanowires can be as small as 200 nm (Figure 2f), which may enable a device packing density of n- and p-type MOSFETs difficult to obtain using other non-monolithic integration methods. The doping profile along the growth axis of the nanowires has been engineered to provide a non-intentionally doped channel and highly doped source/drain regions to reduce the access resistance. Sn was used as the n-type dopant for both the lower and upper part of the InAs segment, and Zn was used as the p-type dopant for the upper part of the GaSb segment (Figure 1c).

The broken band alignment of InAs and GaSb in combination with a high doping at the interface enables a high tunneling current, allowing the InAs segment to be used as an ohmic contact to the GaSb segment[26] where the gate is positioned in the p-MOSFETs. Vertical processing does not rely on high resolution lithography, but dimensions are instead defined by control of the deposition layer thicknesses or etch-back of deposited layers and thus allows for aggressive gate length scaling with accurate precision[18]. The subsequent device fabrication process includes atomic layer deposition of

the Al_2O_3 gate dielectric and the formation of mesas, spacer layers, metal electrodes and interconnects by means of UV-lithography, wet etching, reactive ion etching and sputtering (Methods, Figure 2g and Supporting Information Figure S2)[18, 27].

Individual transistors with 10 to 200 nanowires with a gate length of 200 nm have been processed simultaneously and electrically characterized. We obtain nanowire circumference normalized drive currents of I_{on} = 44 µA/µm and I_{on} = 7 µA/µm (Figure 3a) and transconductances of g_m = 95 µS/µm and g_m = 15 µS/µm at V_{ds} = 0.5 V and a gate overdrive $|V_{gs}-V_t|$= 0.5 V, for InAs and GaSb, respectively (Supporting Information Figure S3). The inverse subthreshold slope (*SS*) is 525 mV/decade and 300 mV/decade for InAs and GaSb, respectively. These relatively high values indicate that the gate action on the channel is not ideal and the electrostatics of these devices needs to be improved. To study the effect of the unintentional GaSb shell overgrown on the InAs segments, the GaSb shell was selectively removed by oxidation and wet etching in a different set of devices. This process is self-limiting and employed as a digital etching prior to the high-κ deposition (Supporting Information Figure S4). In particular, for devices where the GaSb shell has been removed by digital etching, a *SS* of 180 mV/decade over two orders of magnitude for both InAs and GaSb is obtained at 0.5 V supply voltage (Figure 3b) indicating an improved gate control. The removal of the GaSb shell also gives an I_{on}/I_{off} ratio of 10^3 and 10^4 with a V_{GS} swing of 1 V for InAs and GaSb MOSFETs, respectively. These results demonstrate that a common gate stack may indeed be used for both transistor types in III–V CMOS. Even though these performance metrics are less impressive as compared to previous reports on individual In(Ga)As[28] and GaSb[29] MOSFETs it should be considered that there is only a limited number of previous reports on III-V CMOS integration on Si[3, 6, 8, 30]. The two step transfer technique reported by Nah et al. yielded I_{on} = 80 µA/µm and I_{on} = 22 µA/µm at 0.5 V gate overdrive and *SS* = 84 mV/dec and *SS* = 156 mV/dec for n-InAs and p-InGaSb devices, respectively[8]. Yokoyama et al. used a more straightforward single transfer technique of InAs/GaSb layers to Si resulting in ambipolar transfer characteristics with I_{on} = 4 µA/µm (at V_{ds} = 1 V, V_{gs} = 2 V) and I_{on} = 2.4 µA/µm (at V_{ds} = -1 V, V_{gs}

151 = -4 V) for n- and p-type devices, respectively[30]. However, as discussed previously such transfer
152 techniques are challenging to scale to larger wafers and the need for initial III-V substrates is costly.
153 A more attractive route is to use monolithic integration techniques such as rapid melting growth[3] or
154 lateral overgrowth[13], however integration of both n- and p-type III-V transistors for CMOS circuits
155 with channels directly grown on the same Si substrate has not previously been demonstrated. To
156 improve the performance of our transistors, I_{on} and g_m have to be increased e.g. by the use of a self-
157 aligned gate structure to avoid long ungated nanowire segments[31]. Further, to decrease the
158 subthreshold slope the wire diameter should be reduced to improve electrostatics and the gate
159 dielectric deposition optimized[32].
160
161 In addition to individual MOSFETs, inverter circuits have also been fabricated as schematically
162 depicted in Figure 4a. A supply voltage (V_{dd}) between 0.25 and 1 V was applied to the top of the GaSb
163 p-MOSFETs while the bottom of the InAs n-MOSFETs was connected to ground (V_{gnd}). An input
164 voltage (V_{in}), applied to a gate electrode common for both transistors, was swept while the output
165 voltage (V_{out}) between the top of the InAs and the bottom of the GaSb nanowire arrays was
166 measured. The voltage transfer characteristics of a typical inverter exhibit a maximum voltage gain of
167 2 V/V at V_{dd}=0.5 V (Figure 4b). To study the transient response of the inverter, a 1 V square wave
168 input signal is applied as V_{in}. The output signal follows the input signal up to 1 kHz (Figure 4c) but at
169 higher frequencies it is distorted due to charging/discharging of the parasitic capacitances originating
170 from the gate-to-drain and gate-to-source electrode overlaps. To increase the operating frequency,
171 the gate and drain electrodes can be patterned using EBL, which has been shown to reduce parasitics
172 considerably[21]. Furthermore, NAND gates with two InAs n-MOSFETs connected in series and two
173 GaSb p-MOSFETs connected in parallel have also been implemented (Figure 4d,e). A supply voltage
174 of V_{dd} = 1 V is applied to the top of both of the GaSb p-MOSFETs while the bottom of one of the InAs
175 n-MOSFETs is grounded and its top contact connected to the bottom of the other InAs n-MOSFET.
176 Input voltages of V_{inA} / V_{inB} = ± 1 V used to for the four logic combinations '00', '01', '10' and '11' are

177 applied to two gate electrodes each connected to one pair of InAs / GaSb MOSFETs and the output
178 voltage (V_{out}) is measured between the n-InAs and the p-GaSb MOSFETs. The resulting output voltage
179 is low only for V_{inA} = V_{inB} = 1 V as expected. To improve the logic switching performance further, the
180 drive currents of both types of MOSFETs should be increased by using larger nanowire arrays.
181 In conclusion, we have demonstrated a novel method enabling the monolithic co-integration of InAs
182 and GaSb nanowires on Si substrates in one growth step. The lengths of the two materials can be
183 independently controlled by the Au seed particle size and pitch which is crucial for vertical device and
184 circuit fabrication using one gate level. That a single gate stack can be used for the fabrication of InAs
185 n- and GaSb p-MOSFETs with high I_{on}/I_{off} ratios is also benefical for simple device integration. The
186 realization of both inverters and an NAND gates demonstates that the fundamental building blocks
187 necessary for more advanced digital logic circuits can be implemented using III-V channel materials
188 directly grown on Si.
189
190
191 **METHODS**
192 **Nanowire growth**
193 Arrays of Au discs with a thickness of 15 nm and diameters from 22 nm to 42 nm were patterned by
194 EBL on substrates consisting of 250 nm highly doped InAs layers grown on Si(111) substrates. The
195 nanowires were grown using metalorganic vapor phase epitaxy (MOVPE) in an Aixtron 200/4 system
196 at a pressure of 100 mbar and a total flow of 13000 sccm. After annealing at 550°C in arsine (AsH_3),
197 the InAs segment was grown at 420°C using trimethylindium (TMIn) and arsine with a molar fraction
198 of X_{TMIn} = $2.79 \cdot 10^{-6}$ and X_{AsH3} = $1.92 \cdot 10^{-4}$,respectively. The bottom and top parts of the InAs segment
199 were n-doped by triethyltin (TESn) with a molar fraction of X_{TESn} = $6.99 \cdot 10^{-7}$ and $2.80 \cdot 10^{-6}$,
200 respectively, with an undoped segment inbetween. The sample was subsequently heated to 460°C in
201 arsine, where the switch to GaSb growth was initiated while heating to 500°C for continued GaSb

growth with trimethylgallium (TMGa) and trimethylantimony (TMSb) with a molar fraction of X_{TMGa} = $5.79 \cdot 10^{-5}$ and X_{TMSb} = $1.04 \cdot 10^{-6}$, respectively. In the top part of the GaSb segments diethylzinc (X_{DEZn} = $5.99 \cdot 10^{-6}$) is used for p-doping. The conditions for the GaSb growth have been optimized to suppress the growth of any GaSb segment for the smallest Au particles.

TEM analysis

For crystal structure investigation, a JEOL 3000F TEM operating at 300kV with a point resolution of 1.7 Å was used. For high resolution TEM and selective area electron diffraction (SAED), the nanowires were imaged in the <-101>/<11-20> zone axis. In addition, images were recorded using scanning TEM high angle annular dark field (STEM HAADF) for mass and thickness contrast. For chemical analysis, x-ray energy dispersive spectroscopy (XEDS) was used in both TEM and STEM mode. Nanowires were prepared for TEM analysis by mechanically breaking them off the growth substrate and transferred to copper grids covered with a lacey carbon layer.

Device processing

All post-growth lithography is performed using photolithography. Atomic layer deposition (ALD) of 40 cycles of Al_2O_3 at 250°C (EOT ≈ 1.7 nm) is used for the gate dielectric. The sample, for which the GaSb shell is removed, is oxidized for 10 min in ozone and etched 30 s in HF (1:100) just before ALD. Source mesa isolation is performed by etching the Al_2O_3 in buffered oxide etch (1:10) for 20 s, and the InAs buffer layer in H_3PO_4:H_2O_2:H_2O (1:1:25) for 3 min. Photoresist (S1828) baked at 200°C for 1 h is employed as the separating spacers between the source and gate electrodes, as well as between the gate and drain electrodes. Thick resist is initially spin coated to achieve good planarization after which the thickness of the spacers is set by reactive ion etching (RIE) with oxygen. Following the first spacer, a 60 nm tungsten gate metal is sputtered and the gate length is set by a photoresist that is thinned down by RIE, followed by a dry-etch of tungsten in a SF_6/Ar plasma. After the second photoresist spacer, a Ti/W/Au top contact is sputtered. The top contact is patterned using photolithography and the three metals are etched using KI, H_2O_2 and BOE (1:10).

Electrical characterization

DC characterization was carried out at room temperature using a Cascade 11000B probe station connected to a Keithley 4200 parameter analyzer.

1. del Alamo, J. A. *Nature* **2011,** *479*, 317.
2. Sanghoon, L.; Cheng-Ying, H.; Cohen-Elias, D.; Thibeault, B. J.; Mitchell, W.; Chobpattana, V.; Stemmer, S.; Gossard, A. C.; Rodwell, M. J. W. *IEEE Electron Device Lett.* **2014,** *35*, 621.
3. Yuan, Z.; Kumar, A.; Chen, C.-Y.; Nainani, A.; Griffin, P.; Wang, A.; Wang, W.; Wong, M. H.; Droopad, R.; Contreras-Guerrero, R.; Kirsch, P.; Jammy, R.; Plummer, J.; Saraswat, K. C. *Symposium on VLSI Technology* **2013**, 54.
4. Czornomaz, L.; Daix, N.; Cheng, K.; Caimi, D.; Rossel, C.; Lister, K.; Sousa, M.; Fompeyrine, J. *Electron Devices Meeting (IEDM)*, **2013**, 2.8.1.
5. Irisawa, T.; Oda, M.; Kamimuta, Y.; Moriyama, Y.; Ikeda, K.; Mieda, E.; Jevasuwan, W.; Maeda, T.; Ichikawa, O.; Osada, T.; Hata, M.; Tezuka, T. *Symposium on VLSI Technology* **2013**, 56.
6. Dey, A. W.; Svensson, J.; Borg, B. M.; Ek, M.; Wernersson, L.-E. *Nano Lett.* **2012,** *12*, 5593.
7. Ko, H.; Takei, K.; Kapadia, R.; Chuang, S.; Fang, H.; Leu, P. W.; Ganapathi, K.; Plis, E.; Kim, H. S.; Chen, S.-Y.; Madsen, M.; Ford, A. C.; Chueh, Y.-L.; Krishna, S.; Salahuddin, S.; Javey, A. *Nature* **2010,** *468*, 286.
8. Nah, J.; Fang, H.; Wang, C.; Takei, K.; Lee, M. H.; Plis, E.; Krishna, S.; Javey, A. *Nano Lett.* **2012,** *12*, 3592.
9. Ahn, J.-H.; Kim, H.-S.; Lee, K. J.; Jeon, S.; Kang, S. J.; Sun, Y.; Nuzzo, R. G.; Rogers, J. A. *Science* **2006,** *314*, 1754.
10. Daix, N.; Uccelli, E.; Czornomaz, L.; Caimi, D.; Rossel, C.; Sousa, M.; Siegwart, H.; Marchiori, C.; Hartmann, J. M.; Shiu, K.-T.; Cheng, C.-W.; Krishnan, M.; Lofaro, M.; Kobayashi, M.; Sadana, D.; Fompeyrine, J. *APL Materials* **2014,** *2*, 086104.
11. Nishi, K.; Yokoyama, M.; Yokoyama, H.; Hoshi, T.; Sugiyama, H.; Takenaka, M.; Takagi, S. *Symposium on VLSI Technology*, **2015**, 174.
12. Waldron, N.; Merckling, C.; Teugels, L.; Ong, P.; Ibrahim, S. A. U.; Sebaai, F.; Pourghaderi, A.; Barla, K.; Collaert, N.; Thean, A. V. Y. *IEEE Electron Device Lett.* **2014,** *35*, 1097.
13. Czornomaz, L.; Uccelli, E.; Sousa, M.; Deshpande, V.; Djara, V.; Caimi, D.; Rossell, M. D.; Erni, R.; Fompeyrine, J. *Symposium on VLSI Technology*, **2015**, 172.
14. Schmid, H.; Borg, M.; Moselund, K.; Gignac, L.; Breslin, C. M.; Bruley, J.; Cutaia, D.; Riel, H. *Appl. Phys. Lett.* **2015,** *106*, 233101.
15. Favre-Nicolin, V.; Mastropietro, F.; Eymery, J.; Camacho, D.; Niquet, Y. M.; Borg, B. M.; Messing, M. E.; Wernersson, L. E.; Algra, R. E.; Bakkers, E. P. A. M.; Metzger, T. H.; Harder, R.; Robinson, I. K. *New Jour. Phys.* **2010,** *12*, 035013.
16. Ghalamestani, S. G.; Johansson, S.; Borg, B. M.; Lind, E.; Dick, K. A.; Wernersson, L. E. *Nanotechnology* **2012,** *23*, 015302.
17. Tomioka, K.; Yoshimura, M.; Fukui, T. *Nature* **2012,** *488*, 189.
18. Persson, K. M.; Berg, M.; Borg, M. B.; Jun, W.; Johansson, S.; Svensson, J.; Jansson, K.; Lind, E.; Wernersson, L. E. *IEEE Trans. Electron Devices* **2013,** *60*, 2761.
19. Persson, K. M.; Berg, M.; Sjöland, H.; Lind, E.; Wernersson, L. E. *Electron. Lett.* **2014,** *50*, 682.
20. Yakimets, D.; Eneman, G.; Schuddinck, P.; Trong Huynh, B.; Bardon, M. G.; Raghavan, P.; Veloso, A.; Collaert, N.; Mercha, A.; Verkest, D.; Voon-Yew Thean, A.; De Meyer, K. *IEEE Trans. Electron Devices* **2015,** *62*, 1433.
21. Johansson, S.; Memisevic, E.; Wernersson, L. E.; Lind, E. *IEEE Electron Device Lett.* **2014,** *35*, 518.
22. Rehnstedt, C.; Martensson, T.; Thelander, C.; Samuelson, L.; Wernersson, L. E. *IEEE Trans. Electron Devices* **2008,** *55*, 3037.
23. Ek, M.; Borg, B. M.; Johansson, J.; Dick, K. A. *ACS Nano* **2013,** *7*, 3668.

24. Jeppsson, M.; Dick, K. A.; Wagner, J. B.; Caroff, P.; Deppert, K.; Samuelson, L.; Wernersson, L.-E. *Jour. Cryst. Growth.* **2008,** *310*, 4115.
25. NanoDim Software, http://www.nanodim.net.
26. Takei, K.; Madsen, M.; Fang, H.; Kapadia, R.; Chuang, S.; Kim, H. S.; Liu, C.-H.; Plis, E.; Nah, J.; Krishna, S.; Chueh, Y.-L.; Guo, J.; Javey, A. *Nano Lett.* **2012,** *12*, 2060.
27. Thelander, C.; Froberg, L. E.; Rehnstedt, C.; Samuelson, L.; Wernersson, L. E. *IEEE Electron Device Lett.* **2008,** *29*, 206.
28. Lee, S.; Chobpattana, V.; Huang, C. Y.; Thibeault, B. J.; Mitchell, W.; Stemmer, S.; Gossard, A. C.; Rodwell, M. J. W. *Symposium on VLSI Technology*, **2014**, 1.
29. Chu, R. L.; Chiang, T. H.; Hsueh, W. J.; Chen, K. H.; Lin, K. Y.; Brown, G. J.; Chyi, J. I.; Kwo, J.; Hong, M. *Appl. Phys. Lett.* **2014,** *105*, 182106.
30. Yokoyama, M.; Yokoyama, H.; Takenaka, M.; Takagi, S. *Symposium on VLSI Technology*, **2014**, 1.
31. Berg, M.; Persson, K. M.; Kilpi, O. P.; Svensson, J.; Lind, E.; Wernersson, L. E. *Electron Devices Meeting (IEDM)*, **2015**.
32. Fu, C. H.; Lin, Y. H.; Lee, W. C.; Lin, T. D.; Chu, R. L.; Chu, L. K.; Chang, P.; Chen, M. H.; Hsueh, W. J.; Chen, S. H.; Brown, G. J.; Chyi, J. I.; Kwo, J.; Hong, M. *Microelectronic Engineering* **2015,** *147*, 330.

Supporting Information. Compositional analysis by XEDS line scans of InAs-GaSb nanowires. SEM images of various stages in an inverter fabrication process. Linear transfer characteristics and transconductance of InAs and GaSb MOSFETs. SEM images of a InAs-GaSb nanowire before and after digital etching.

Acknowledgements

The authors would like to Erik Lind at the Department of Electrical and Information Technology, Lund University, for assistance. This work has been supported by the Swedish Research Council, the Swedish Foundation for Strategic Research, and the European Union 7th Framework Program E2SWITCH (Grant Agreement No. 619509).

Author Contributions

J.S. grew the nanowires. A.D. and J.S. fabricated the devices and circuits and did DC characterization and data analysis. D.J. performed TEM imaging and analysis. The project was directed and supervised by L-E.W. A.D. and J.S. wrote the manuscript with considerable input from L-E.W. All authors discussed the data and commented on the manuscript.

Competing financial interests

The authors declare no competing financial interests. Readers are welcome to comment on the online version of the paper. Correspondence and requests for materials should be addressed to L-E.W. (lars-erik.wernersson@eit.lth.se).

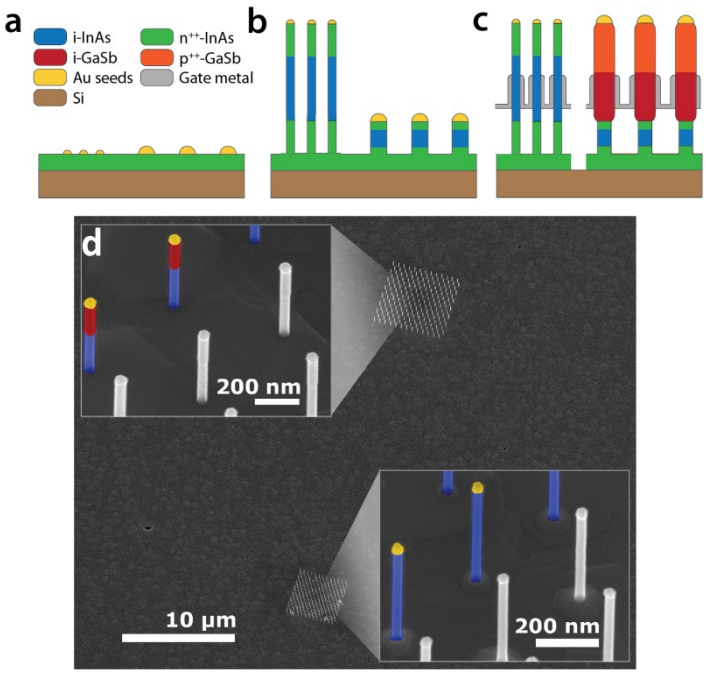

Figure 1. Schematic growth process and a SEM micrograph of a monolithic integration of InAs and GaSb nanowires on a Si substrate**.** (a) Au particles of different sizes are patterned by EBL on a Si substrate with a highly doped InAs layer. (b) InAs nanowire segments with an n-i-n doping profile are grown from the Au seed particles. The particle size and pitch is used to control the growth rate yielding both long thin wires and short wires with larger diameter simultaneously. (c) Growth continues with a GaSb segment with an i-p doping profile. The Gibbs-Thomson effect inhibits growth of GaSb on the thin InAs segments and careful tuning of the particle size and density is exploited to achieve similar total lengths of InAs and InAs/GaSb nanowires. The position of the gate for the n-InAs and p-GaSb MOSFETs and the InAs mesa isolation is indicated. (d) Partially colored SEM micrograph of InAs and InAs/GaSb nanowire arrays grown in a single MOCVD step.

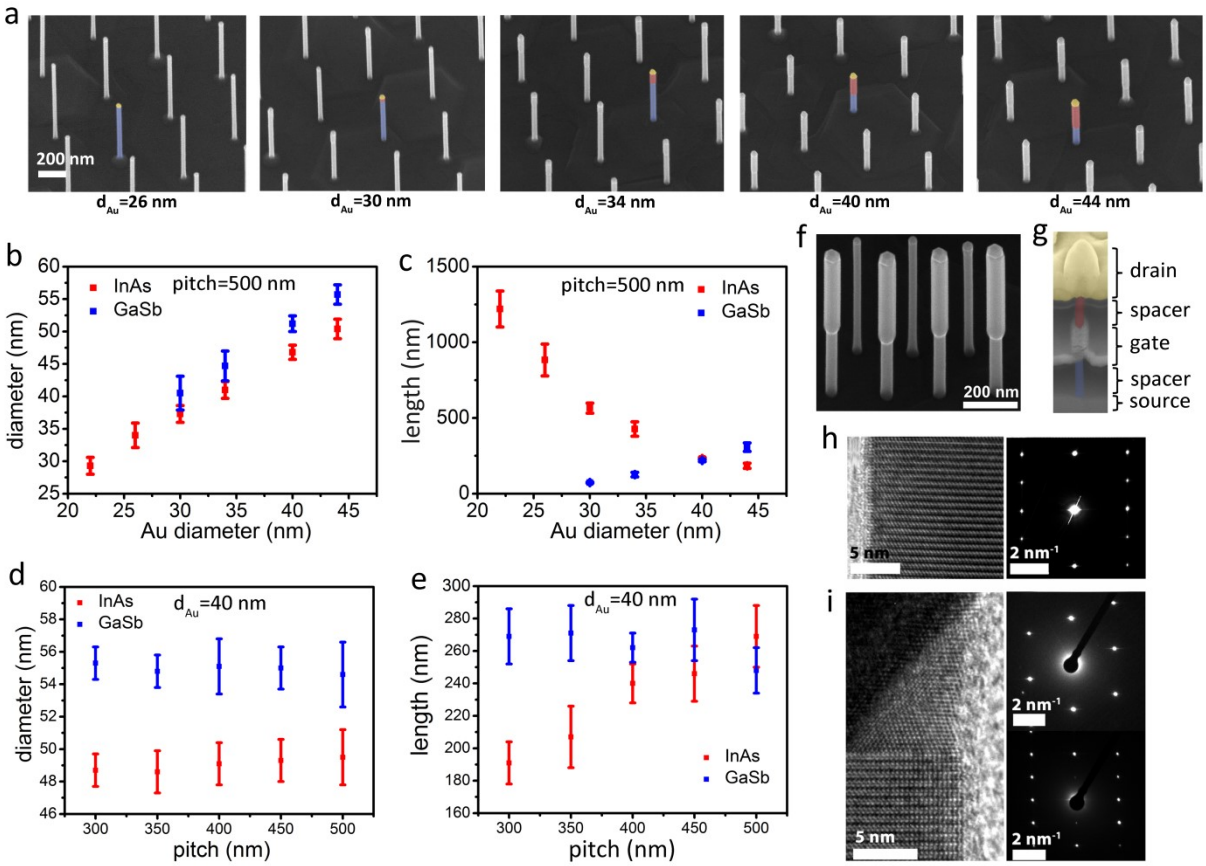

Figure 2. Control of nanowire dimensions. (a) Nanowires grown from Au particles with different diameter. The thinner and thicker nanowire segments have been attributed to InAs and GaSb respectively using XEDS analysis. The InAs segment is colored blue, the GaSb red and the Au particle yellow on single wires for clarity. For the smallest diameters the GaSb growth is completely suppressed. The GaSb segment length increases with increasing Au diameter while the InAs length decreases. (b) Diameter of the InAs and GaSb segments as a function of Au particle size. The mean diameter is calculated for 20 nanowires in each array and the error bars represent the standard deviation. An Au particle size d_{Au} > 30 nm is necessary for the nucleation of GaSb. The diameters of both segments are correlated to the Au size. (c) Length of the InAs and GaSb segments as a function of Au particle size. The lengths of the InAs and GaSb segments decrease and increase with increasing d_{Au} respectively. This opposite trend of the axial growth rate can be attributed to the Gibbs-Thomson effect lowering the growth rate of GaSb for smaller Au particles. (d) Nanowire diameter as a function of pitch between Au particles. (e) Length of InAs and GaSb segments as a function of Au pitch. The

349 InAs and GaSb segments have all a diameter of 49 nm and 55 nm, respectively. The error bars in
350 figures b to e represent the standard deviation. (f) InAs and InAs/GaSb nanowires with 200 nm pitch.
351 (g) Partially colored cross sectional SEM image (52° tilt) of a finished MOSFET with an InAs/GaSb
352 nanowire. (h) High resolution TEM image of an InAs nanowire with the corresponding diffraction
353 pattern indicating a high quality wurtzite crystal structure. (i) TEM image of the heterojunction in an
354 InAs/GaSb nanowire with the diffraction patterns from the top zincblende GaSb and the bottom
355 wurtzite InAs segment. The crystal interface to the wurtzite InAs segment is sharp and the
356 composition at the interface can be considered abrupt with only a 3.5 nm segment with intermediate
357 composition as determined from an XEDS line scan (Supporting Information Figure S1).

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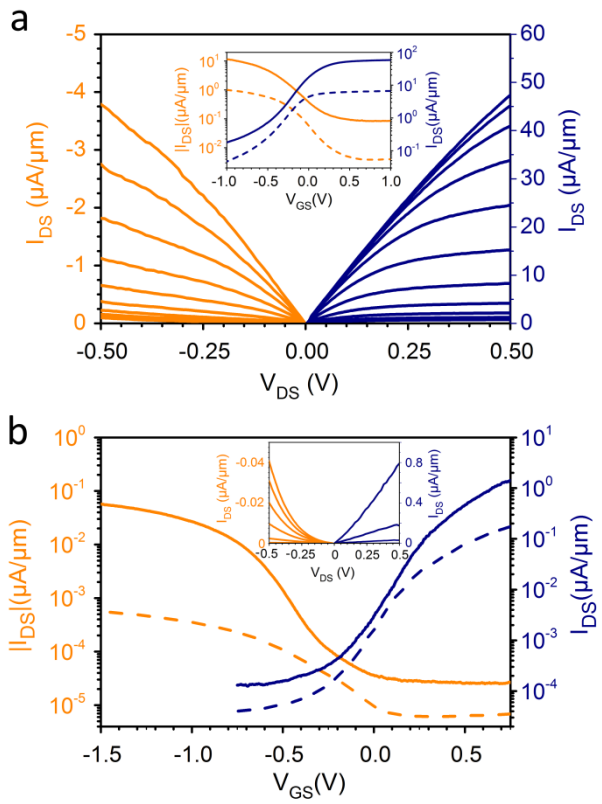

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361 **Figure 3.** Output and transfer characteristics of InAs and GaSb MOSFETs. (a) Output and
362 characteristics of an InAs MOSFET (blue) with a nanowire diameter d_{InAs} = 32 nm and a GaSb MOSFET
363 (orange) with d_{GaSb} = 48 nm with -0.50 < V_{gs} < 0.5 V (100 mV step). The inset displays the transfer
364 characteristics with $|V_{ds}|$= 50 mV (dashed) and $|V_{ds}|$= 500 mV (solid). (b) Transfer characteristics of

MOSFETs where the thin GaSb shell has been removed with $|V_{ds}|$= 50 mV (dashed) and $|V_{ds}|$= 500 mV (solid). The InAs MOSFET (blue) has d_{InAs} = 34 nm and the GaSb MOSFET (orange) has d_{GaSb} = 63 nm. The inset displays the output characteristics with 0 < V_{gs} < 0.75 V (250 mV step) for InAs and -1.4 V < V_{gs} < 0.2 V (100 mV step) for GaSb.

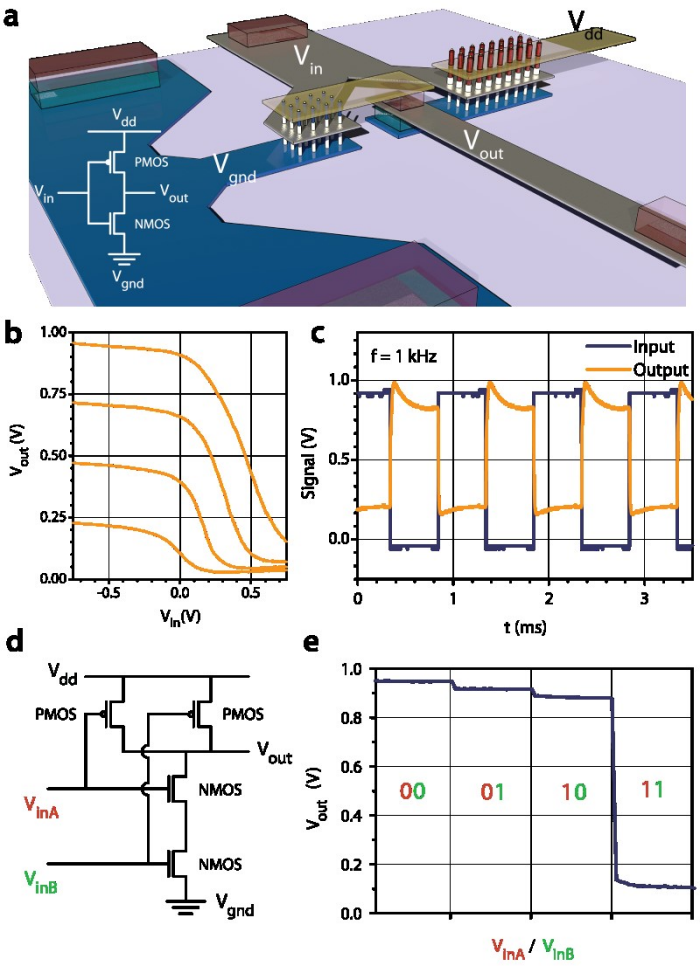

Figure 4. DC and AC inverter and NAND characteristics. (a) A schematic image of an inverter where the two spacer layers have been omitted for clarity. (b) Voltage transfer characteristics for an inverter with digitally etched nanowires for several supply voltages (V_{dd}) ranging from 0.25 V to 1V (0.25 V steps). (c) AC characterization of an inverter circuit operating at 1 kHz with a 1 V square-wave input signal. (d) NAND circuit schematic and (e) NAND characteristic with a power supply voltage of V_{dd}= 1 V and input voltages of V_{inA} / V_{inB} = ± 1 V.