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I. Abstract

In this work, we present a novel self-aligned gate-last fabrication process for vertical nanowire metal-oxide-semiconductor field-effect transistors. The fabrication method allows for exposure dose-defined gate lengths and a local diameter reduction of the intrinsic channel segment, while maintaining thicker highly doped access regions. Using this process, InAs nanowire transistors combining good on- and off-performance are fabricated demonstrating $Q = g_{m,max}/SS = 8.2$, which is higher than any previously reported vertical nanowire MOSFET.

II. Introduction

III-V compound semiconductors on Si substrates are expected to appear in commercial complementary metal-oxide-semiconductor (CMOS) implementations within a couple of years [1], taking advantage of the excellent transport properties of these semiconductors to reach faster and more energy-efficient circuits. One way to ensure high-quality materials for such highly lattice-mismatched integration, is through the use of a nanowire geometry [2]. Vertical nanowire MOSFETs allow for small footprints, as the channel and metal contact lengths are decoupled. It has been suggested that such integration can outperform lateral devices at highly scaled technology nodes [3], [4]. Furthermore, the geometry simplifies the fabrication of a gate-all-around transistor, which ensures good electrostatic control of the transistor channel. Reducing the nanowire diameter further improves electrostatics, but can also increase the series resistance from the ungated regions as well as increasing the metal-semiconductor contact resistance. One way of reducing these resistances is through high doping in the contact regions, which could be accomplished during nanowire growth. However, high-precision doping control of the nanowire core along the axial direction has proven very challenging [5], resulting in imprecise alignment of the electrodes and separation layers.

To address these issues, we have developed a self-aligned, gate-last process, allowing for local reduction of the nanowire diameter in the channel region using digital etching. InAs nanowires with a doped outer shell around an undoped core are used to implement transistors with a thin intrinsic channel and thicker doped contact regions. Furthermore, the process allows for the fabrication of MOSFETs with varying gate lengths, L_G, on the same sample. Using the described methods, the best combined performance of transconductance and subthreshold slope for any vertical nanowire MOSFET is demonstrated.
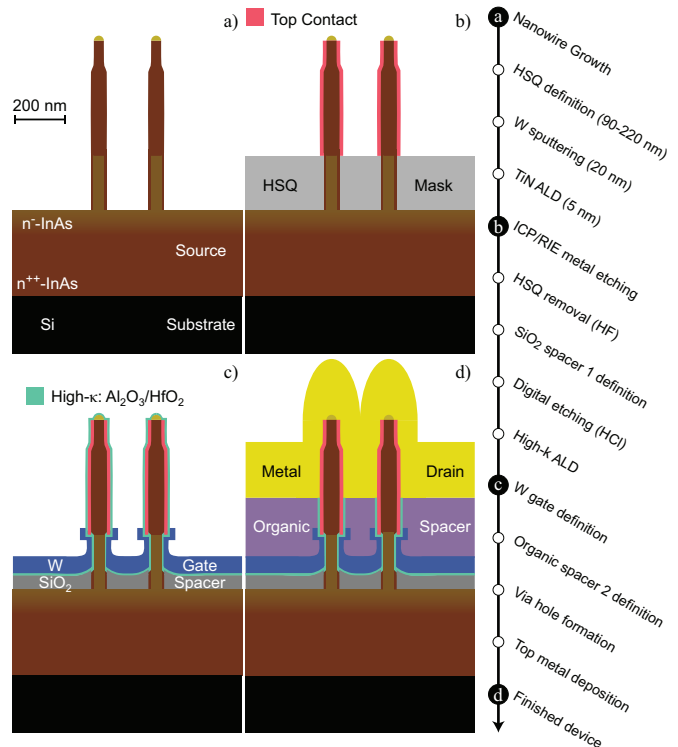

Fig. 1. Cross-sectional schematic illustrations of the most crucial steps in the self-aligned, gate-last fabrication process corresponding to the steps of the process flow chart.

III. Device fabrication

InAs nanowire MOSFETs are fabricated on lowly p-doped Si (111) substrates with an epitaxially grown InAs buffer layer [6]. The InAs layer serves both as a buffer layer for nanowire growth and as a low-resistive device bottom contact, avoiding transport over the InAs/Si heterojunction potential barrier [7]. The nanowires are grown using metal organic vapor-phase epitaxy (MOVPE) using the vapor-liquid-solid (VLS) method from electron-beam defined Au particles positioned in double-row arrays with 200 nm spacing. The nanowires consist of a 200 nm long undoped core segment with a diameter of 35 nm, followed by a 400 nm highly doped top segment. By increasing the group V to group III molar ratio in the second step, the highly n-doped InAs also overgrows on the undoped section, forming a 10 nm thick shell surrounding the undoped core, as illustrated in Fig. 1a.

To define the top contact, hydrogen silsesquioxane (HSQ) is applied and exposed with an electron beam at an acceleration voltage of 50 kV, where the exposure dose determines
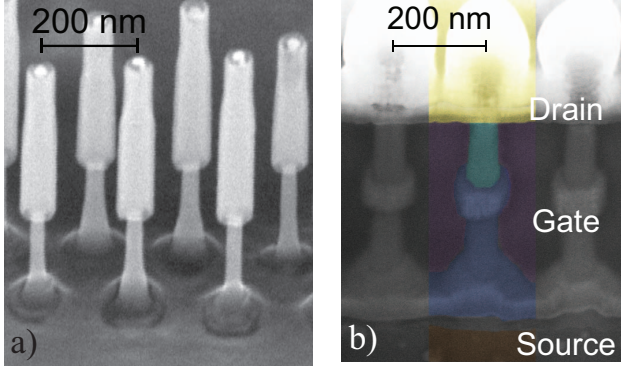
Fig. 2. Scanning electron micrographs of a) nanowires after thinning of the channel region using digital etching and b) after the complete fabrication. Both images are taken at a tilt of $52°$ from top-view.

Fig. 4. a) Output characteristics for the same transistor as in Fig. 3 together with the corresponding virtual source modeling. b) Voltage gain, $g_{\mathrm{m}}/g_{\mathrm{d}}$, as a function of g_{m} for the same device.

the thickness of the film after development. The top metal contact is formed by sputtering of $20\,\mathrm{nm}$ W and atomic layer deposition (ALD) of $5\,\mathrm{nm}$ TiN. The metal layers are dry etched anisotropically, removing the planar layer keeping only the metal on the nanowire sidewalls, as illustrated in Fig. 1b. The HSQ is subsequently wet etched using HF. SiO_2 is deposited using ALD followed by etch back of a spin-on resist. This resist serves as etch mask for HF wet etching of SiO_2 from the nanowire sidewalls, which results in a 20-nm-thick SiO_2 separation layer between gate and source. This spacer, together with the top metal, also serves as an etch mask for digital etching of the nanowires using alternating O_3 oxidation for $10\,\mathrm{min}$ at $50\,°\mathrm{C}$ and $HCl : H_2O$ (1:10) etching for $15\,\mathrm{s}$. The segment not protected by etch masks, corresponding to L_G, is ultimately determined by the exposure dose of the top metal definition, and in this case varied between 70 and $200\,\mathrm{nm}$. A channel diameter of $28\,\mathrm{nm}$ is fabricated while keeping thicker doped regions underneath the top contact and the bottom spacer. An ALD high-κ oxide, corresponding to an approximate EOT of $1.5\,\mathrm{nm}$, consisting of a bi-layer of Al_2O_3 and HfO_2, is deposited at $300\,°\mathrm{C}$ and $120\,°\mathrm{C}$, respectively. This is followed by gate metal sputtering of W and definition of the gate edge using an

etched back spin-on resist. An illustration can be seen in Fig. 1c, showing an overlapping gate on the top side and edge-to-edge alignment on the source-side. A $100\,\mathrm{nm}$ organic second spacer is fabricated followed by sputtering of the top metal electrode stack with the final device architecture shown in Fig. 1d. Scanning electron micrographs of the devices after the thinning of the channel region and after the complete fabrication are shown in Fig. 2a and Fig. 2b, respectively.

IV. RESULTS AND DISCUSSION

The transfer characteristics for a vertical InAs nanowire MOSFET with a channel diameter of $28\,\mathrm{nm}$ and a gate length of $190\,\mathrm{nm}$ can be seen in Fig. 3. A peak transconductance, $g_{\mathrm{m,max}}$, of $0.85\,\mathrm{mS}\,\mu\mathrm{m}^{-1}$, normalized to the circumference, and a minimum subthreshold swing, SS, of $154\,\mathrm{mV}\,\mathrm{dec}^{-1}$ is measured at $V_{\mathrm{DS}} = 0.5\,\mathrm{V}$. Furthermore, enhancement mode operation is observed with a $V_{\mathrm{T}} = 0.3\,\mathrm{V}$. The device characteristics are modeled using a virtual source model [8], and show good fit to measured transfer and output data, illustrated in Fig. 3a and Fig. 4a, using an injection velocity, v_{inj}, of $1.9 \times 10^7\,\mathrm{cm}\,\mathrm{s}^{-1}$ and an electron mobility, μ_{e}, of $1400\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$. Fig. 4b shows the voltage gain, $g_{\mathrm{m}}/g_{\mathrm{d}}$, as a function of g_{m} and V_{DS} for the same device. The good electrostatic control provides high gain at low
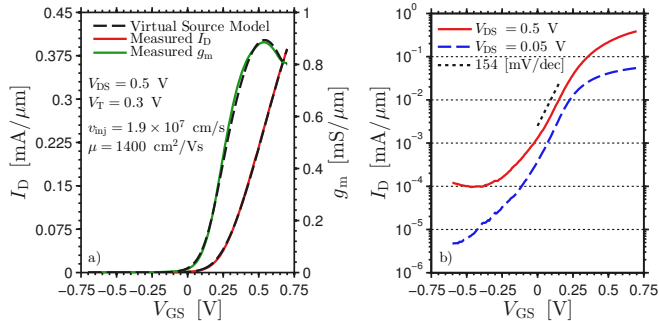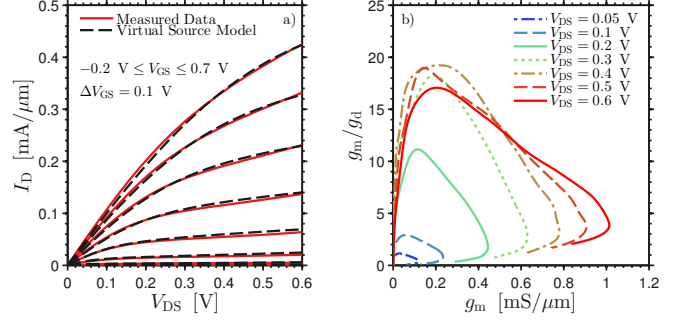

Fig. 3. Transfer characteristics with a) a linear scale and b) a logarithmic scale for a vertical InAs nanowire MOSFET consisting of 280 nanowires in parallel with a diameter of $28\,\mathrm{nm}$ and L_G of $190\,\mathrm{nm}$. The dashed black line of a) is a fitting of a virtual source model using an injection velocity, v_{inj}, of $1.9 \times 10^7\,\mathrm{cm}\,\mathrm{s}^{-1}$ and a mobility, μ, of $1400\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$.
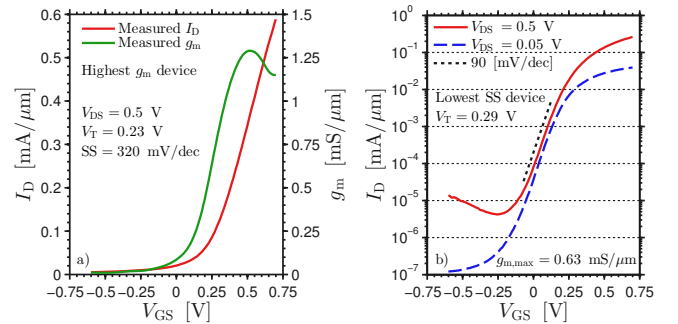

Fig. 5. Transfer characteristics for two different devices with a) being the one with the highest $g_{\mathrm{m,max}}$ of $1.29\,\mathrm{mS}\,\mu\mathrm{m}^{-1}$ and b) being the one with the lowest subthreshold swing of $90\,\mathrm{mV}\,\mathrm{dec}^{-1}$. Both transistors have a diameter of $28\,\mathrm{nm}$, but have different gate lengths, with a) and b) corresponding to $130\,\mathrm{nm}$ and $180\,\mathrm{nm}$, respectively.
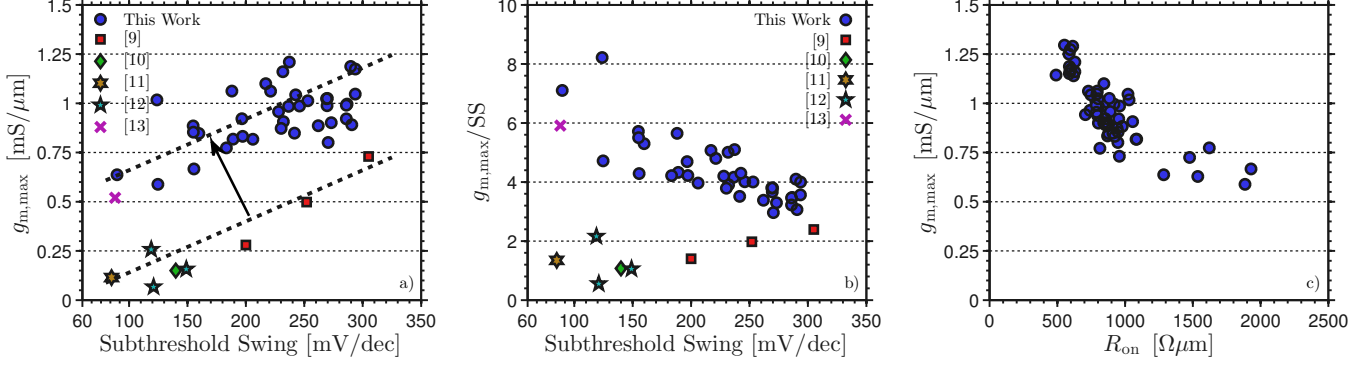
Fig. 6. a) Transconductance as a function of subthreshold swing for the fabricated devices in this work compared to other reported vertical III-V nanowire MOSFETs. Our values compare favorably to others both in terms of transconductance and subthreshold swing. b) $Q = g_{m,max}/SS$ as a function of SS for the same devices as a). A clear trend with increasing values for lower subthreshold swings, indicating that even higher performance can be expected with an improved gate stack. c) $g_{m,max}$, extracted at $V_{DS} = 0.5$ V, as a function of R_{on} for multiple devices fabricated in parallel. A large increase in $g_{m,max}$ is observed for lower R_{on}, demonstrating that the performance is limited by extrinsic series resistances. In the three graphs, data from identically fabricated devices positioned in an hexagonal geometry is included.
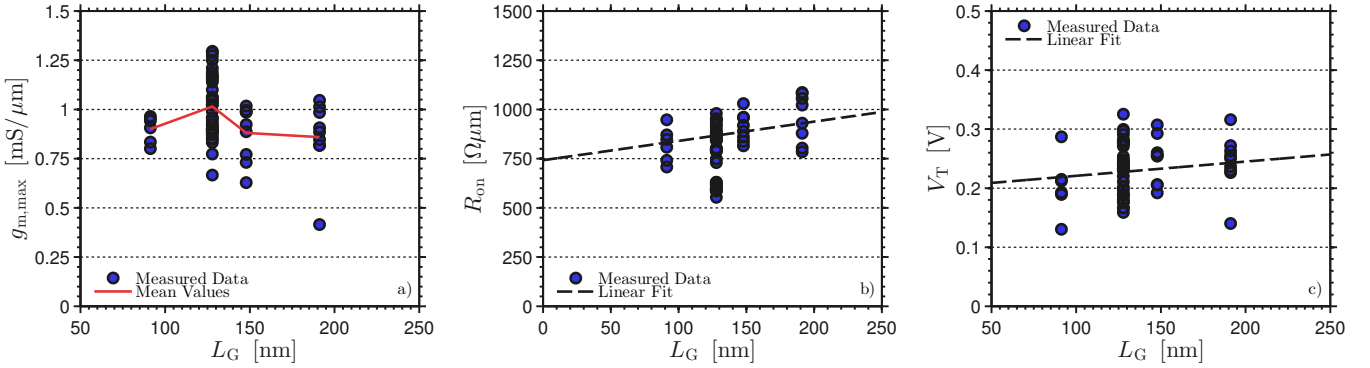

Fig. 7. a) Peak transconductance at $V_{DS} = 0.5$ V versus gate length for devices with the same diameter fabricated in parallel. A trace representing the mean transconductance at each gate length is included. A slight increase in g_m as L_G is reduced is observed down to 120 nm. b) On-resistance as a function of gate length. A linear extrapolation to zero L_G indicates an average access resistance of about 750 Ω μm. c) Threshold voltage versus gate length showing a small negative shift with shorter channels and a variation, on the order of 150 mV, between devices.

gate overdrive, although it is lowered as g_m approaches $g_{m,max}$, originating from series resistances on both the drain and source. The transfer characteristics for the devices with the highest $g_{m,max}$ and the lowest SS, corresponding to 1.29 mS μm^{-1} and 90 mV dec^{-1}, are shown in Fig. 5a and b, respectively. The DC performance metrics are extracted for 60 devices with varying gate lengths and compared to other vertical III-V nanowire MOSFETs [9]–[13]. Fig. 6a and b show that the fabricated devices with the self-aligned gate-last process compare favorably to other work, especially the improved $Q = g_{m,max}/SS$ [14] demonstrates that our fabrication method yields a good combination of on and off performance. The highest value for Q is 8.2, which is, to the authors knowledge, higher than for any previously demonstrated vertical nanowire MOSFET. Fig. 6c show $g_{m,max}$ plotted versus R_{on} and it indicates that g_m is limited by access resistance. From the virtual source modelling, shown in Fig. 3a, the intrinsic $g_{m,max}$ is estimated to 2.2 mS μm^{-1}.

Devices with different L_G in the range between 70 and 200 nm are fabricated by varying the first HSQ layer thick-ness. The impact of a varying L_G is shown for $g_{m,max}$, R_{on}, and the threshold voltage, V_T, in Fig. 7a-c, respectively. A small increase in g_m as L_G is reduced can be observed, combined with a lowering of V_T. From the R_{ON} dependency, an average access resistance for these devices of about 750 Ω μm is extracted, further indicating that the device DC performance is limited by access resistance. By comparing measurements when keeping the bottom of the nanowires grounded to top-ground measurements, it is found that the majority of the resistance is situated on the top side, probably due to high contact resistance at the W-InAs interface.

V. CONCLUSION

In this work, we have demonstrated the highest performance in terms of $g_{m,max}$ and SS for any vertical nanowire MOSFET, with $g_{m,max}$ reaching 1.29 mS μm^{-1} and SS of 90 mV dec^{-1}. This performance is achieved through the use of a novel self-aligned, gate-last fabrication process on a Si-substrate. The method allows for gate length scaling as well as separate optimization of the channel region and the contact regions.

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