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*Published in:*

Technical Digest - International Electron Devices Meeting, IEDM

*DOI:*

[10.1109/IEDM.2015.7409808](https://doi.org/10.1109/IEDM.2015.7409808)

2016

*Document Version:*

Peer reviewed version (aka post-print)

[Link to publication](#)

*Citation for published version (APA):*

Zota, C. B., Wernersson, L. E., & Lind, E. (2016). Single suspended InGaAs nanowire MOSFETs. *Technical Digest - International Electron Devices Meeting, IEDM*, 31.4.1-31.4.4. <https://doi.org/10.1109/IEDM.2015.7409808>

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# Single Suspended InGaAs Nanowire MOSFETs

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## I. ABSTRACT

We report on  $\text{In}_{0.85}\text{Ga}_{0.15}\text{As}$  NWFETs utilizing a single suspended (above the substrate) selectively grown nanowire as the channel. These devices exhibit  $g_m = 3.3 \text{ mS}/\mu\text{m}$  and subthreshold slope  $SS = 118 \text{ mV}/\text{dec}$ , both at  $V_{DS} = 0.5 \text{ V}$  and  $L_G = 60 \text{ nm}$ . This is the highest reported value of  $g_m$  for all MOSFETs and HEMTs, as well as a strong combination of on and off performance, with  $Q = g_m/SS = 28$ , the highest for non-planar III-V MOSFETs.

## II. INTRODUCTION

Indium-rich  $\text{In}_{1-x}\text{Ga}_x\text{As}$  nanowires are promising candidates as the channel in future CMOS technology for both high-performance and low-power applications. This is due to the high electron mobility and injection velocity offered by  $\text{In}_{1-x}\text{Ga}_x\text{As}$ , as well as the strong electrostatic control enabled by multiple-gate architectures, such as FinFETs and nanowire MOSFETs (NWFETs) [1]–[5]. A key issue is the nanowire formation scheme. Since surface scattering is strongly nanowire diameter-dependent, high-quality nanowire surfaces are important in order to maintain high  $I_{DS}$  as the diameter is scaled down. Several nanowire formation methods have been reported. In particular, vapor-liquid-solid growth, utilizing a metal particle catalyst, as well as etched-out nanowires have been widely studied. Electron mobility for diameters less than 30 nm is typically  $2000\text{--}5000 \text{ cm}^2/\text{Vs}$ , more than an order of magnitude lower than bulk mobility [6]. However, in deeply scaled, i.e. ballistic or quasi-ballistic devices, the interpretation of mobility and its relation to  $I_{DS}$  is not straightforward. Rather,  $I_{DS}$  is proportional to the mean free path  $\lambda$ . In fact,  $\text{In}_{1-x}\text{Ga}_x\text{As}$  is promising also for its long  $\lambda$ , shown in nanowires to be approximately an order of magnitude longer than that of Si [6]. At a given  $L_G$ , this results in transport closer to the ballistic limit.

NWFETs are also of interest in high-frequency applications, where the MOS-structure allows for scaling beyond the capabilities of traditional HEMT technology, and strong electrostatics can improve high-frequency metrics such as the voltage gain ( $A_V$ ) as well as  $f_t$  and  $f_{max}$ .

In this work, we demonstrate high-performance quasi-ballistic NWFETs utilizing a single selectively grown  $\text{In}_{0.85}\text{Ga}_{0.15}\text{As}$  nanowire suspended above the substrate, as the channel. We also determine the mean free path, and electron mobility of the nanowires, utilizing both room-temperature and low-temperature methods.

## III. DEVICE FABRICATION

Fig. 1(a) shows a schematic illustration of the nanowire formation process. The  $\text{In}_{1-x}\text{Ga}_x\text{As}$  composition of the nanowire is different from the nominal composition due

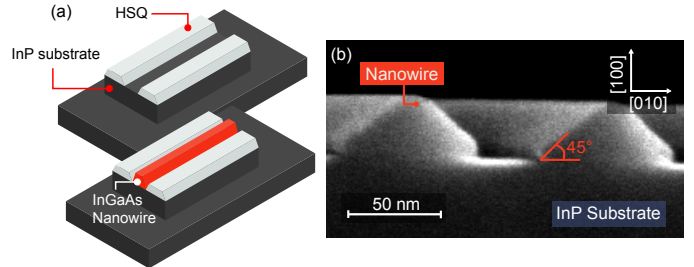


Fig. 1. (a) Schematic of the selective nanowire growth process. Areas of HSQ are patterned on semi-insulating InP:Fe. In the narrow space between HSQ areas, an  $\text{In}_{0.85}\text{Ga}_{0.15}\text{As}$  nanowire is formed during MOCVD growth. (b) Cross-sectional SEM image of wider reference nanowires oriented along [001], which is the same direction as in the fabricated devices.

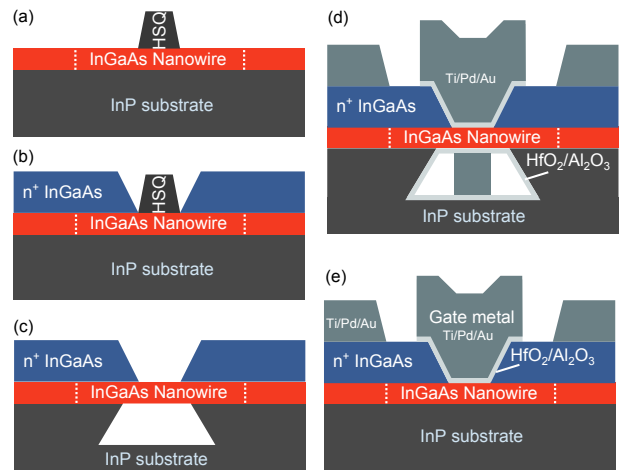


Fig. 2. (a) An HSQ dummy gate is patterned across the nanowire. (b)  $n^+$   $\text{In}_{0.63}\text{Ga}_{0.37}\text{As}$  contacts are regrown by MOCVD. (c) The InP underneath the nanowire is etched by HCl solution. Due to anisotropic etch rates, there is only very little etching underneath the contacts. (d) Final device in the suspended and (e) on-substrate configuration.

to growth interactions with the HSQ mask. From optical characterizations, it is determined to be  $\text{In}_{0.85}\text{Ga}_{0.15}\text{As}$ .

Fig. 2(a)–(e) illustrates the device fabrication. An HSQ dummy-gate is patterned across the nanowire, which after MOCVD regrowth of  $n^+$   $\text{In}_{0.63}\text{Ga}_{0.37}\text{As}$  ( $N_D = 5 \cdot 10^{19} \text{ cm}^{-3}$ ) defines the gate-length  $L_G$  of the device. The HSQ is removed by buffered oxide etch [Fig. 3(b)]. The orientations of the nanowire and the dummy gate are chosen as shown in Fig. 3 in order to obtain optimal crystal facets. The nanowires are suspended by selective etching of the InP:Fe substrate by  $\text{HCl}:\text{H}_2\text{O}$ . We also fabricate devices which have not suspended nanowires (on-substrate). The dimensions of the nanowire are scaled down by several cycles of ozone

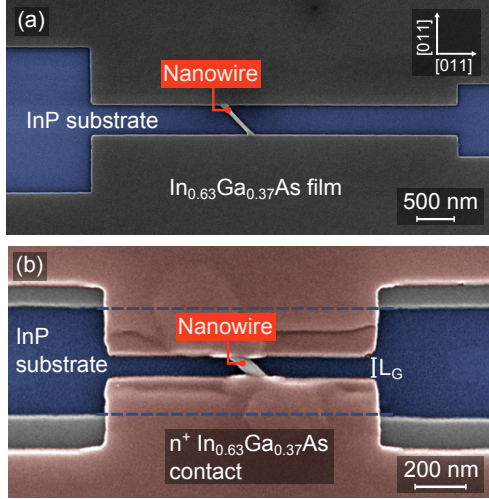


Fig. 3. (a) False-color SEM image of the device after nanowire regrowth [corresponding to Fig 1(a)]. The  $45^\circ$  tilt of the nanowire facilitates optimal directions for the subsequent InP etching, as well as optimal facets for the regrown contact layer. (b) False-color SEM image of the device after contact regrowth [corresponding to Fig. 2(c)]. (c) Schematic of the final device in the suspended configuration.

oxidation and diluted HCl etching. The final dimensions of the nanowire are  $W/H = 45/12$  nm. Ti/Pd/Au source and drain metal contacts are deposited by lift-off.

After  $(\text{NH}_4)_2\text{S}$  surface treatment, the gate oxide (10 cycles  $\text{Al}_2\text{O}_3$  and 60 cycles  $\text{HfO}_2$ ,  $\text{EOT} \approx 1.8$  nm) is deposited by ALD. The Ni/Pd/Au gate metal is subsequently deposited and patterned by lift-off, which finalizes the process. Fig. 3(c) shows a schematic of the final device.

#### IV. RESULTS AND DISCUSSION

The measurement data is normalized to the gated circumference of the nanowire, which has the shape seen in Fig. 1(b), i.e. defined by  $[110]$  sidewalls at  $45^\circ$  angles. Fig. 4(a) and (b) show output characteristics of devices in suspended and on-substrate configurations, respectively. They exhibit similar peak  $g_m$  and on-current. Fig. 5(a) shows a comparison of subthreshold characteristics for the same devices. The threshold voltage  $V_T$  is defined from linear extrapolation at maximum  $g_m$ . On-substrate nanowires exhibit minimum SS

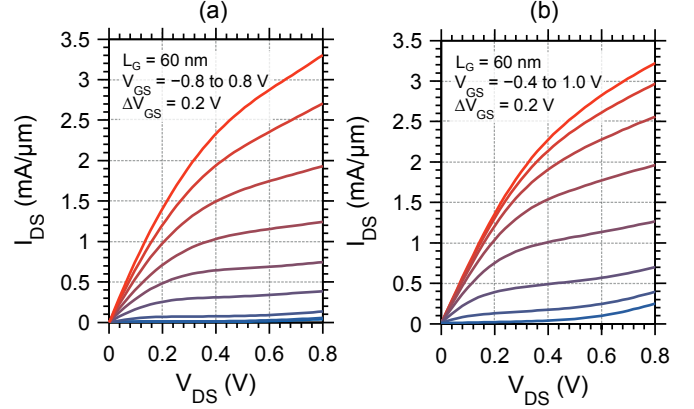


Fig. 4. Output characteristics of  $L_G = 60$  nm NWFETs in the (a) suspended and (b) on-substrate configurations. Both configurations exhibit similar  $R_{\text{ON}}$  and peak  $g_m$ .

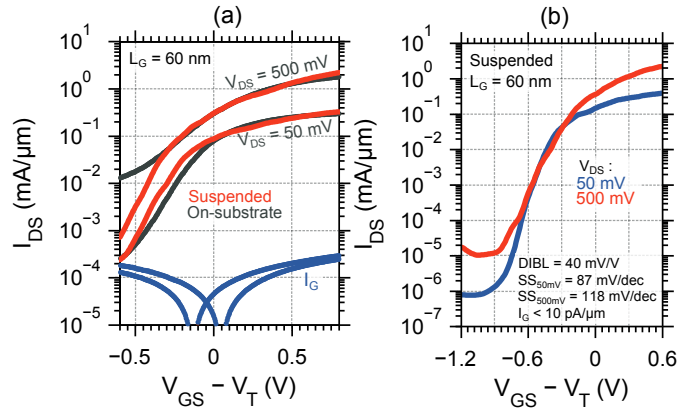


Fig. 5. (a) Subthreshold characteristics of  $L_G = 60$  nm NWFETs in the (red) suspended and (gray) on-substrate configurations. (b) Subthreshold characteristics of suspended  $L_G = 60$  nm NWFET with optimized gate and pad-to-pad leakage currents, which improves  $I_{\text{off}}$  and DIBL.

$= 316$  mV/dec and  $\text{DIBL} = 440$  mV/V, while suspended nanowires exhibit  $\text{SS} = 140$  mV/dec and  $\text{DIBL} = 200$  mV/V, all at  $V_{\text{DS}} = 0.5$  V. This shows the detrimental effect of the relatively small 300 meV band offset between  $\text{In}_{0.85}\text{Ga}_{0.15}\text{As}$  and the InP substrate. The reduction of DIBL is due to in part a reduction of the substrate leakage current, in part due to a reduced influence of the drain potential on the channel.

Fig. 5(b) shows subthreshold characteristics of an optimized (reduced gate and pad-to-pad leakages) suspended NWFET with  $L_G = 60$  nm, which exhibits  $\text{DIBL} < 40$  mV/V, minimum  $\text{SS} = 118$  mV/dec at  $V_{\text{DS}} = 0.5$  V and  $\text{SS} = 87$  mV/dec at  $V_{\text{DS}} = 0.05$  V. Transfer characteristics are shown in Fig. 6 for the same device as in Fig. 5(b). Devices with  $L_G = 60$  nm exhibit  $I_{\text{DS}} = 2.9$  mA/ $\mu\text{m}$ , corresponding to 160  $\mu\text{m}$ /nanowire, at  $V_{\text{DS}} = 0.5$  V and  $V_{\text{GS}} - V_T = 1.0$  V. The peak transconductance is  $g_m = 3.3$  mS/ $\mu\text{m}$  at  $V_{\text{DS}} = 0.5$  V, and  $Q = g_m/\text{SS}$  is 28. The  $g_m$ -peak is relatively wide, with  $g_m > 2.5$  mS/ $\mu\text{m}$  over a range of  $\sim 1$  V.

Peak transconductance versus  $L_G$  is shown in Fig. 7. In a ballistic device,  $g_m$  is proportional to the transmission

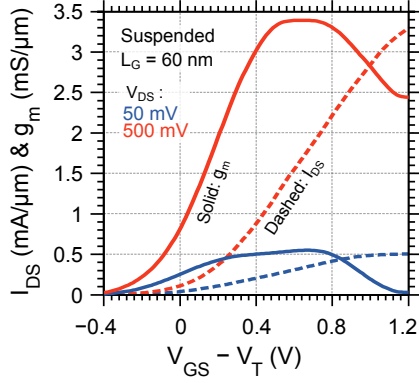


Fig. 6. Transfer characteristics of the same  $L_G = 60$  nm suspended NWFET as in Fig. 4(b) at  $V_{DS} = 0.5$  V.

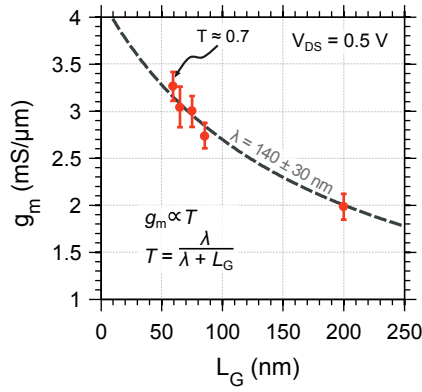


Fig. 7. Peak  $g_m$  versus  $L_G$  for suspended NWFETs at  $V_{DS} = 0.5$  V. Dashed traces show a fit of the transmission  $T$  to the data.

$T = \lambda / (L_G + \lambda)$  [7]. Dashed traces show a fit of  $T$  with  $\lambda = 140 \pm 30$  nm to the measurement data, which gives the effective electron mobility  $\mu_{\text{eff}} = q\lambda v_T / 2k_B T_L = 7000 \pm 1500 \text{ cm}^2/\text{Vs}$  from the Einstein relation.  $\mu_{\text{eff}}$  can alternatively be calculated from  $R_{\text{ON}}$  versus  $L_G$  shown in Fig. 8. In a ballistic FET,  $R_{\text{ON}} = (G_0 M)^{-1} (\lambda^{-1} L_G + 1) + R_P$ , where  $G_0 = 2e^2/h$  is the quantum conductance,  $M$  is the number of conducting sub-bands and  $R_P$  is the parasitic spreading access resistance. Fitting this equation to the measurement data and subtracting our calculated  $R_P$ , we again obtain  $\lambda_{\text{eff}} = 7000 \pm 1500 \text{ cm}^2/\text{Vs}$ . This is among the highest reported values for  $\text{In}_{1-x}\text{Ga}_x\text{As}$  nanowires of similar dimensions [6].

The on-resistance is  $R_{\text{ON}} = 130 \Omega\mu\text{m}$  at  $L_G = 60$  nm, which is  $2450 \Omega/\text{nanowire}$ . The contact resistance is  $R_C = 25 \Omega\mu\text{m}$ , the sheet resistance of the  $n^+$   $\text{In}_{0.63}\text{Ga}_{0.37}\text{As}$  contact layer is  $R_{\square} = 70 \Omega/\square$ , both calculated from TLM measurements (Fig. 9). The total spreading access resistance  $R_P$ , depends on  $R_C$ ,  $R_{\square}$  and the geometry of the contacts, as shown in Fig. 9, and was calculated as  $R_P = 150 \pm 50 \Omega$  by COMSOL 3D simulation.

Fig. 10 compares  $g_d$  of suspended and on-substrate NWFETs. At low  $V_{GS}$ , the reduced DIBL causes a reduction of  $g_d$  by a factor two. In the high- $V_{GS}$  regime,  $g_d$  converges, which may indicate non-linear access resistance. Fig. 10 also shows an improvement of the peak voltage gain  $A_V = g_m/g_d$

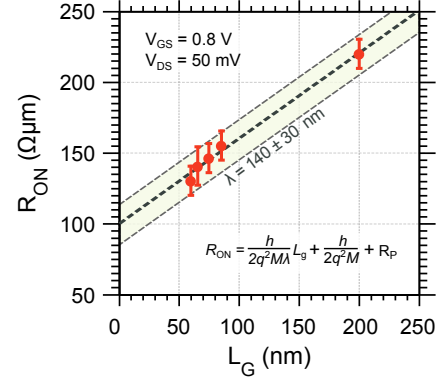


Fig. 8.  $R_{\text{ON}}$  versus  $L_G$  for suspended NWFETs. Dashed traces show a fit of  $R_{\text{ON}}$  from which  $\lambda$  is calculated.

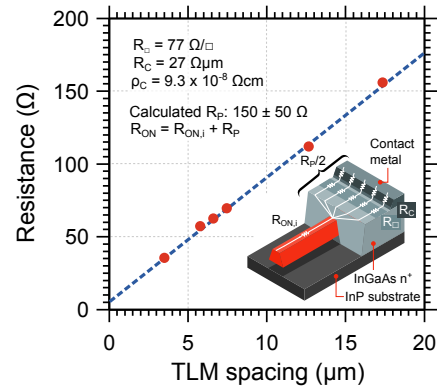


Fig. 9. Contact resistance  $R_C$  and sheet resistance  $R_{\square}$  as determined from on-sample TLM measurements. Inset shows a schematic of the parasitic spreading access resistance  $R_P$ .

from 5 to 12.5 for the suspended configuration while  $g_m$  still is  $> 2 \text{ mS}/\mu\text{m}$ , which is mainly due to the reduced  $g_d$ . This value is larger than for reported high-performance HEMTs by a factor two [8]. Fig. 11 shows a benchmark of  $g_m$  and SS for various planar and non-planar III-V MOSFETs.

Due to the discrete 1D subband band structure of the nanowire, the conductance  $G = I_{DS}/V_{DS}$  displays steps at low temperature,  $T_L = 10$  K. Fig. 12 shows the conductance at various  $V_{DS}$  for an  $L_G = 60$  nm suspended NWFET. The steps are visible mostly at low  $V_{DS}$ . The first three steps are at approximately  $0.7G_0$ ,  $1.4G_0$  and  $2.1G_0$ , which gives the transmission  $T = 0.7$  at  $L_G = 60$  nm. Since the transmission at  $L_G = 60$  nm from  $g_m$ - $L_G$  and  $R_{\text{ON}}$ - $L_G$  in Fig. 7 and 8 is also approximately 0.7, this is a sign that the conductance steps are indeed due to quantized sub-bands, rather than defect states. Since we obtain similar transmission at 10 K and room-temperature, this indicates that transport is surface roughness, rather than phonon, scattering limited [6].

Utilizing a semi-classical compact model with 2-band non-parabolic band structure, self-consistent corrections and empirical short-channel modeling, we have calculated the device performance in the ballistic limit, using the same EOT and device dimensions as for the fabricated devices. The inset of Fig. 12 shows low temperature conductance simulations,

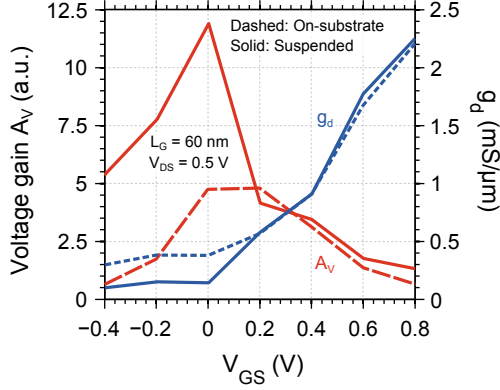


Fig. 10. Voltage gain  $A_V$  and output conductance  $g_d$  versus  $V_{GS}$  for suspended (solid traces) and on-substrate (dashed traces) NWFETs at  $V_{DS} = 0.5$  V and  $L_G = 60$  nm.

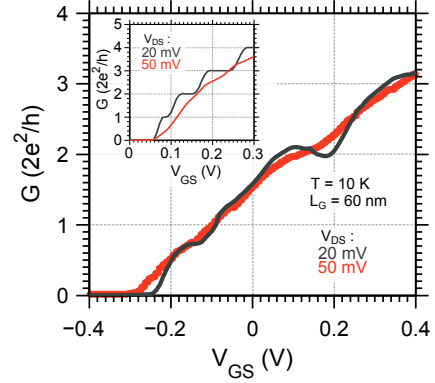


Fig. 12. Low-temperature conductance  $G = I_{DS}/V_{DS}$  for a suspended NWFET with  $L_G = 60$  nm. Inset shows simulated conductance at 10 K for a fully ballistic device.

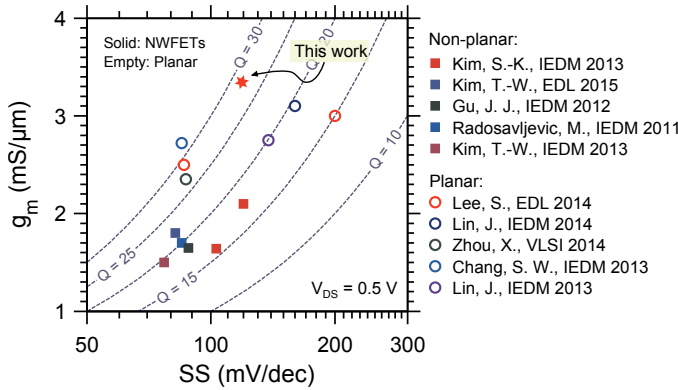


Fig. 11. Benchmark of  $Q = g_m/SS$  at  $V_{DS} = 0.5$  V for various planar and non-planar III-V MOSFETs. We compare with a suspended NWFET with  $L_G = 60$  nm.

clearly showing the expected conductance quantization at low  $V_{DS}$ . Fig. 13 shows the calculated ballistic current and transconductance at  $V_{DS} = 0.5$  V, indicating a peak  $g_m = 5.6$  mS/ $\mu$ m. The deviations between the modeled and measured data can be explained through oxide traps and scattering.

## V. CONCLUSION

In conclusion, we have demonstrated NWFETs with record-high  $g_m = 3.3$  mS/ $\mu$ m,  $SS = 118$  mV/dec at  $V_{DS} = 0.5$  V and  $DIBL = 40$  mV/V, enabled by a long mean-free path  $140 \pm 30$  nm and high effective electron mobility  $\lambda_{eff} = 7000 \pm 1500$  cm<sup>2</sup>/Vs as well as low parasitic resistances. This shows the potential of selectively regrown  $In_{1-x}Ga_xAs$  nanowires for both high-frequency and digital applications.

## VI. ACKNOWLEDGEMENTS

This work was supported in part by the Swedish Research Council, in part by the Knut and Alice Wallenberg Foundation, and in part by the Swedish Foundation for Strategic Research.

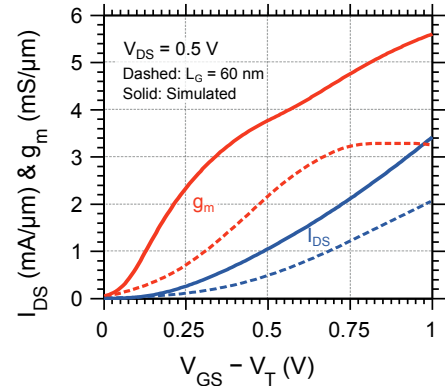


Fig. 13. Simulated transfer characteristics of a fully ballistic device. Dashed traces show a measured  $L_G = 60$  nm NWFET.

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