



LUND UNIVERSITY

Single suspended InGaAs nanowire MOSFETs

Zota, Cezar B.; Wernersson, Lars Erik; Lind, Erik

Published in:
Technical Digest - International Electron Devices Meeting, IEDM

DOI:
[10.1109/IEDM.2015.7409808](https://doi.org/10.1109/IEDM.2015.7409808)

2016

Document Version:
Peer reviewed version (aka post-print)

[Link to publication](#)

Citation for published version (APA):
Zota, C. B., Wernersson, L. E., & Lind, E. (2016). Single suspended InGaAs nanowire MOSFETs. *Technical Digest - International Electron Devices Meeting, IEDM*, 31.4.1-31.4.4.
<https://doi.org/10.1109/IEDM.2015.7409808>

Total number of authors:
3

General rights

Unless other specific re-use rights are stated the following general rights apply:
Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal

Read more about Creative commons licenses: <https://creativecommons.org/licenses/>

Take down policy

If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.

LUND UNIVERSITY

PO Box 117
221 00 Lund
+46 46-222 00 00

Single Suspended InGaAs Nanowire MOSFETs

Cezar B. Zota, Lars-Erik Wernersson and Erik Lind

Department of Electrical and Information Technology, Lund University, Box 118, Lund, Sweden

E-mail: Cezar.Zota@eit.lth.se. Phone: +46 46 222 80 62

I. ABSTRACT

We report on $\text{In}_{0.85}\text{Ga}_{0.15}\text{As}$ NWFETs utilizing a single suspended (above the substrate) selectively grown nanowire as the channel. These devices exhibit $g_m = 3.3 \text{ mS}/\mu\text{m}$ and subthreshold slope $SS = 118 \text{ mV}/\text{dec}$, both at $V_{DS} = 0.5 \text{ V}$ and $L_G = 60 \text{ nm}$. This is the highest reported value of g_m for all MOSFETs and HEMTs, as well as a strong combination of on and off performance, with $Q = g_m/SS = 28$, the highest for non-planar III-V MOSFETs.

II. INTRODUCTION

Indium-rich $\text{In}_{1-x}\text{Ga}_x\text{As}$ nanowires are promising candidates as the channel in future CMOS technology for both high-performance and low-power applications. This is due to the high electron mobility and injection velocity offered by $\text{In}_{1-x}\text{Ga}_x\text{As}$, as well as the strong electrostatic control enabled by multiple-gate architectures, such as FinFETs and nanowire MOSFETs (NWFETs) [1]–[5]. A key issue is the nanowire formation scheme. Since surface scattering is strongly nanowire diameter-dependent, high-quality nanowire surfaces are important in order to maintain high I_{DS} as the diameter is scaled down. Several nanowire formation methods have been reported. In particular, vapor-liquid-solid growth, utilizing a metal particle catalyst, as well as etched-out nanowires have been widely studied. Electron mobility for diameters less than 30 nm is typically $2000\text{--}5000 \text{ cm}^2/\text{Vs}$, more than an order of magnitude lower than bulk mobility [6]. However, in deeply scaled, i.e. ballistic or quasi-ballistic devices, the interpretation of mobility and its relation to I_{DS} is not straightforward. Rather, I_{DS} is proportional to the mean free path λ . In fact, $\text{In}_{1-x}\text{Ga}_x\text{As}$ is promising also for its long λ , shown in nanowires to be approximately an order of magnitude longer than that of Si [6]. At a given L_G , this results in transport closer to the ballistic limit.

NWFETs are also of interest in high-frequency applications, where the MOS-structure allows for scaling beyond the capabilities of traditional HEMT technology, and strong electrostatics can improve high-frequency metrics such as the voltage gain (A_V) as well as f_t and f_{max} .

In this work, we demonstrate high-performance quasi-ballistic NWFETs utilizing a single selectively grown $\text{In}_{0.85}\text{Ga}_{0.15}\text{As}$ nanowire suspended above the substrate, as the channel. We also determine the mean free path, and electron mobility of the nanowires, utilizing both room-temperature and low-temperature methods.

III. DEVICE FABRICATION

Fig. 1(a) shows a schematic illustration of the nanowire formation process. The $\text{In}_{1-x}\text{Ga}_x\text{As}$ composition of the nanowire is different from the nominal composition due

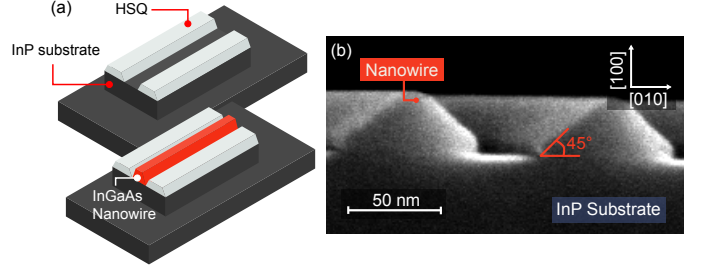


Fig. 1. (a) Schematic of the selective nanowire growth process. Areas of HSQ are patterned on semi-insulating InP:Fe. In the narrow space between HSQ areas, an $\text{In}_{0.85}\text{Ga}_{0.15}\text{As}$ nanowire is formed during MOCVD growth. (b) Cross-sectional SEM image of wider reference nanowires oriented along [001], which is the same direction as in the fabricated devices.

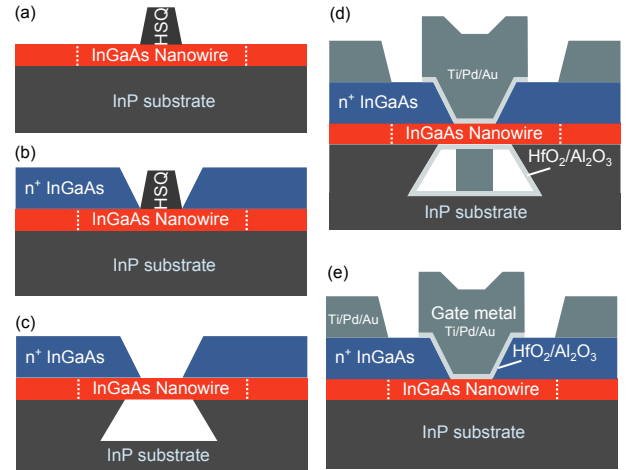


Fig. 2. (a) An HSQ dummy gate is patterned across the nanowire. (b) n^+ $\text{In}_{0.63}\text{Ga}_{0.37}\text{As}$ contacts are regrown by MOCVD. (c) The InP underneath the nanowire is etched by HCl solution. Due to anisotropic etch rates, there is only very little etching underneath the contacts. (d) Final device in the suspended and (e) on-substrate configuration.

to growth interactions with the HSQ mask. From optical characterizations, it is determined to be $\text{In}_{0.85}\text{Ga}_{0.15}\text{As}$.

Fig. 2(a)–(e) illustrates the device fabrication. An HSQ dummy-gate is patterned across the nanowire, which after MOCVD regrowth of n^+ $\text{In}_{0.63}\text{Ga}_{0.37}\text{As}$ ($N_D = 5 \cdot 10^{19} \text{ cm}^{-3}$) defines the gate-length L_G of the device. The HSQ is removed by buffered oxide etch [Fig. 3(b)]. The orientations of the nanowire and the dummy gate are chosen as shown in Fig. 3 in order to obtain optimal crystal facets. The nanowires are suspended by selective etching of the InP:Fe substrate by $\text{HCl}:\text{H}_2\text{O}$. We also fabricate devices which have not suspended nanowires (on-substrate). The dimensions of the nanowire are scaled down by several cycles of ozone

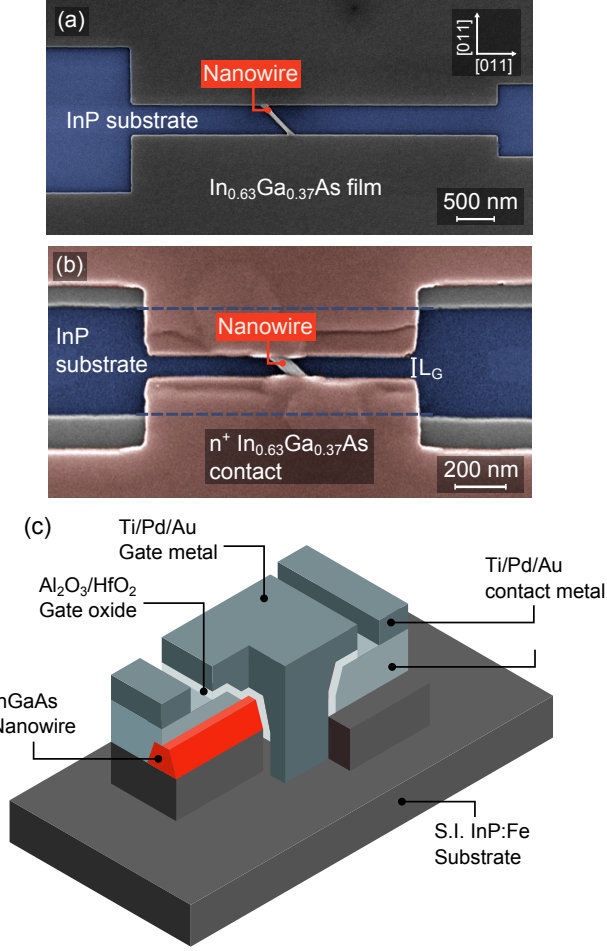


Fig. 3. (a) False-color SEM image of the device after nanowire regrowth [corresponding to Fig 1(a)]. The 45° tilt of the nanowire facilitates optimal directions for the subsequent InP etching, as well as optimal facets for the regrown contact layer. (b) False-color SEM image of the device after contact regrowth [corresponding to Fig. 2(c)]. (c) Schematic of the final device in the suspended configuration.

oxidation and diluted HCl etching. The final dimensions of the nanowire are $W/H = 45/12$ nm. Ti/Pd/Au source and drain metal contacts are deposited by lift-off.

After $(\text{NH}_4)_2\text{S}$ surface treatment, the gate oxide (10 cycles Al_2O_3 and 60 cycles HfO_2 , $\text{EOT} \approx 1.8$ nm) is deposited by ALD. The Ni/Pd/Au gate metal is subsequently deposited and patterned by lift-off, which finalizes the process. Fig. 3(c) shows a schematic of the final device.

IV. RESULTS AND DISCUSSION

The measurement data is normalized to the gated circumference of the nanowire, which has the shape seen in Fig. 1(b), i.e. defined by [110] sidewalls at 45° angles. Fig. 4(a) and (b) show output characteristics of devices in suspended and on-substrate configurations, respectively. They exhibit similar peak g_m and on-current. Fig. 5(a) shows a comparison of subthreshold characteristics for the same devices. The threshold voltage V_T is defined from linear extrapolation at maximum g_m . On-substrate nanowires exhibit minimum SS

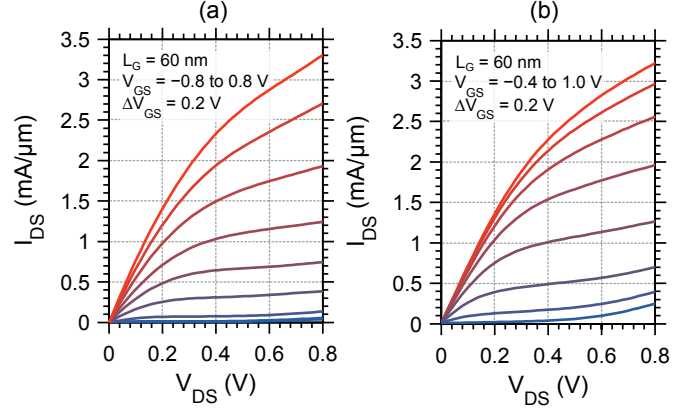


Fig. 4. Output characteristics of $L_G = 60$ nm NWFETs in the (a) suspended and (b) on-substrate configurations. Both configurations exhibit similar R_{ON} and peak g_m .

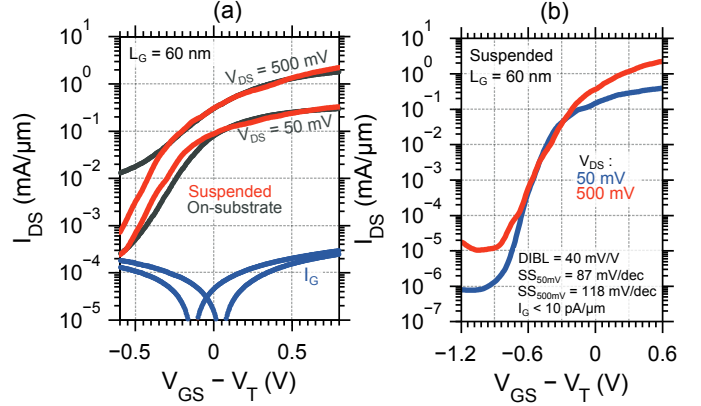


Fig. 5. (a) Subthreshold characteristics of $L_G = 60$ nm NWFETs in the (red) suspended and (gray) on-substrate configurations. (b) Subthreshold characteristics of suspended $L_G = 60$ nm NWFET with optimized gate and pad-to-pad leakage currents, which improves I_{off} and DIBL.

= 316 mV/dec and DIBL = 440 mV/V, while suspended nanowires exhibit $SS = 140$ mV/dec and DIBL = 200 mV/V, all at $V_{DS} = 0.5$ V. This shows the detrimental effect of the relatively small 300 meV band offset between $\text{In}_{0.85}\text{Ga}_{0.15}\text{As}$ and the InP substrate. The reduction of DIBL is due in part a reduction of the substrate leakage current, in part due to a reduced influence of the drain potential on the channel.

Fig. 5(b) shows subthreshold characteristics of an optimized (reduced gate and pad-to-pad leakages) suspended NWFET with $L_G = 60$ nm, which exhibits DIBL < 40 mV/V, minimum $SS = 118$ mV/dec at $V_{DS} = 0.5$ V and $SS = 87$ mV/dec at $V_{DS} = 0.05$ V. Transfer characteristics are shown in Fig. 6 for the same device as in Fig. 5(b). Devices with $L_G = 60$ nm exhibit $I_{DS} = 2.9$ mA/μm, corresponding to 160 μm/nanowire, at $V_{DS} = 0.5$ V and $V_{GS} - V_T = 1.0$ V. The peak transconductance is $g_m = 3.3$ mS/μm at $V_{DS} = 0.5$ V, and $Q = g_m/SS$ is 28. The g_m -peak is relatively wide, with $g_m > 2.5$ mS/μm over a range of ~1 V.

Peak transconductance versus L_G is shown in Fig. 7. In a ballistic device, g_m is proportional to the transmission

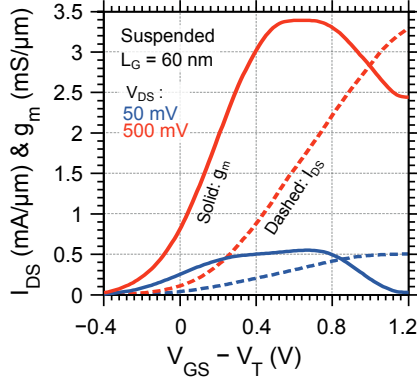


Fig. 6. Transfer characteristics of the same $L_G = 60$ nm suspended NWFET as in Fig. 4(b) at $V_{DS} = 0.5$ V.

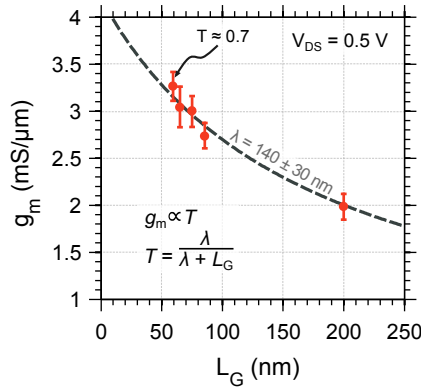


Fig. 7. Peak g_m versus L_G for suspended NWFETs at $V_{DS} = 0.5$ V. Dashed traces show a fit of the transmission T to the data.

$T = \lambda / (L_G + \lambda)$ [7]. Dashed traces show a fit of T with $\lambda = 140 \pm 30$ nm to the measurement data, which gives the effective electron mobility $\mu_{\text{eff}} = q\lambda v_T / 2k_B T_L = 7000 \pm 1500 \text{ cm}^2/\text{Vs}$ from the Einstein relation. μ_{eff} can alternatively be calculated from R_{ON} versus L_G shown in Fig. 8. In a ballistic FET, $R_{\text{ON}} = (G_0 M)^{-1} (\lambda^{-1} L_G + 1) + R_P$, where $G_0 = 2e^2/h$ is the quantum conductance, M is the number of conducting sub-bands and R_P is the parasitic spreading access resistance. Fitting this equation to the measurement data and subtracting our calculated R_P , we again obtain $\lambda_{\text{eff}} = 7000 \pm 1500 \text{ cm}^2/\text{Vs}$. This is among the highest reported values for $\text{In}_{1-x}\text{Ga}_x\text{As}$ nanowires of similar dimensions [6].

The on-resistance is $R_{\text{ON}} = 130 \text{ } \Omega \mu\text{m}$ at $L_G = 60$ nm, which is $2450 \text{ } \Omega/\text{nanowire}$. The contact resistance is $R_C = 25 \text{ } \Omega \mu\text{m}$, the sheet resistance of the n^+ $\text{In}_{0.63}\text{Ga}_{0.37}\text{As}$ contact layer is $R_{\square} = 70 \text{ } \Omega/\square$, both calculated from TLM measurements (Fig. 9). The total spreading access resistance R_P , depends on R_C , R_{\square} and the geometry of the contacts, as shown in Fig. 9, and was calculated as $R_P = 150 \pm 50 \text{ } \Omega$ by COMSOL 3D simulation.

Fig. 10 compares g_d of suspended and on-substrate NWFETs. At low V_{GS} , the reduced DIBL causes a reduction of g_d by a factor two. In the high- V_{GS} regime, g_d converges, which may indicate non-linear access resistance. Fig. 10 also shows an improvement of the peak voltage gain $A_V = g_m/g_d$

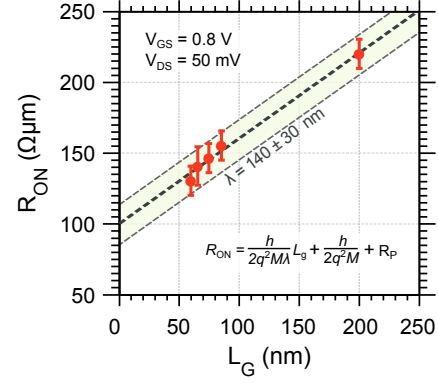


Fig. 8. R_{ON} versus L_G for suspended NWFETs. Dashed traces show a fit of R_{ON} from which λ is calculated.

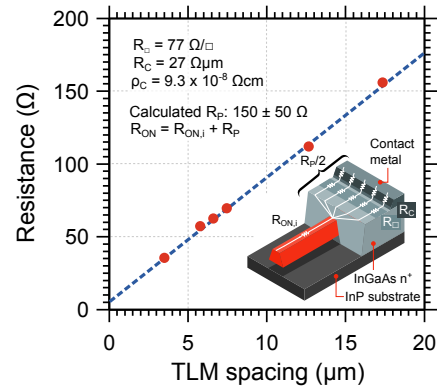


Fig. 9. Contact resistance R_C and sheet resistance R_{\square} as determined from on-sample TLM measurements. Inset shows a schematic of the parasitic spreading access resistance R_P .

from 5 to 12.5 for the suspended configuration while g_m still is $> 2 \text{ mS}/\mu\text{m}$, which is mainly due to the reduced g_d . This value is larger than for reported high-performance HEMTs by a factor two [8]. Fig. 11 shows a benchmark of g_m and SS for various planar and non-planar III-V MOSFETs.

Due to the discrete 1D subband band structure of the nanowire, the conductance $G = I_{\text{DS}}/V_{\text{DS}}$ displays steps at low temperature, $T_L = 10$ K. Fig. 12 shows the conductance at various V_{DS} for an $L_G = 60$ nm suspended NWFET. The steps are visible mostly at low V_{DS} . The first three steps are at approximately $0.7G_0$, $1.4G_0$ and $2.1G_0$, which gives the transmission $T = 0.7$ at $L_G = 60$ nm. Since the transmission at $L_G = 60$ nm from g_m - L_G and R_{ON} - L_G in Fig. 7 and 8 is also approximately 0.7, this is a sign that the conductance steps are indeed due to quantized sub-bands, rather than defect states. Since we obtain similar transmission at 10 K and room-temperature, this indicates that transport is surface roughness, rather than phonon, scattering limited [6].

Utilizing a semi-classical compact model with 2-band non-parabolic band structure, self-consistent corrections and empirical short-channel modeling, we have calculated the device performance in the ballistic limit, using the same EOT and device dimensions as for the fabricated devices. The inset of Fig. 12 shows low temperature conductance simulations,

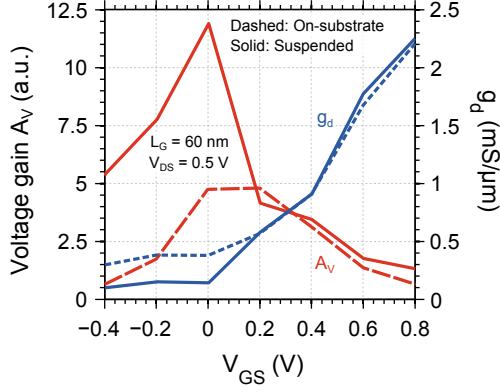


Fig. 10. Voltage gain A_V and output conductance g_d versus V_{GS} for suspended (solid traces) and on-substrate (dashed traces) NWFETs at $V_{DS} = 0.5$ V and $L_G = 60$ nm.

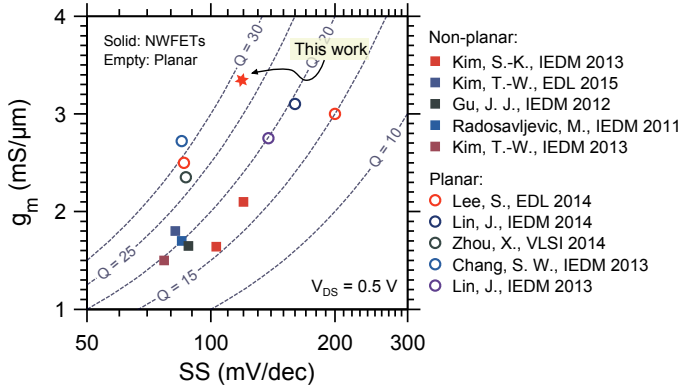


Fig. 11. Benchmark of $Q = g_m/SS$ at $V_{DS} = 0.5$ V for various planar and non-planar III-V MOSFETs. We compare with a suspended NWFET with $L_G = 60$ nm.

clearly showing the expected conductance quantization at low V_{DS} . Fig. 13 shows the calculated ballistic current and transconductance at $V_{DS} = 0.5$ V, indicating a peak $g_m = 5.6$ mS/μm. The deviations between the modeled and measured data can be explained through oxide traps and scattering.

V. CONCLUSION

In conclusion, we have demonstrated NWFETs with record-high $g_m = 3.3$ mS/μm, $SS = 118$ mV/dec at $V_{DS} = 0.5$ V and DIBL = 40 mV/V, enabled by a long mean-free path 140 ± 30 nm and high effective electron mobility $\lambda_{eff} = 7000 \pm 1500$ cm²/Vs as well as low parasitic resistances. This shows the potential of selectively regrown $In_{1-x}Ga_xAs$ nanowires for both high-frequency and digital applications.

VI. ACKNOWLEDGEMENTS

This work was supported in part by the Swedish Research Council, in part by the Knut and Alice Wallenberg Foundation, and in part by the Swedish Foundation for Strategic Research.

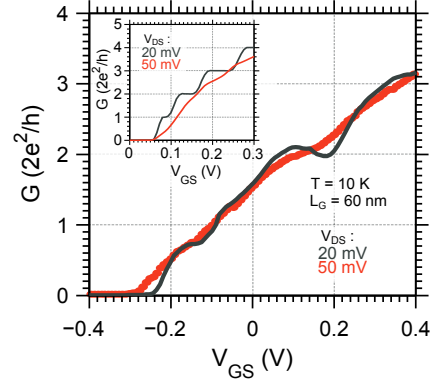


Fig. 12. Low-temperature conductance $G = I_{DS}/V_{DS}$ for a suspended NWFET with $L_G = 60$ nm. Inset shows simulated conductance at 10 K for a fully ballistic device.

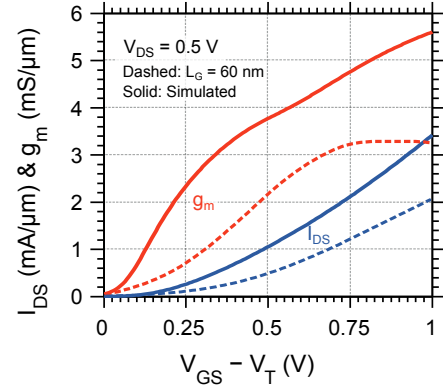


Fig. 13. Simulated transfer characteristics of a fully ballistic device. Dashed traces show a measured $L_G = 60$ nm NWFET.

REFERENCES

- [1] J. A. del Alamo, "Nanometre-scale electronics with III-V compound semiconductors," *Nature*, vol. 479, no. 7373, pp. 317–323, 2011.
- [2] H. Riel, L.-E. Wernersson, M. Hong, and J. A. del Alamo, "III-V compound semiconductor transistors from planar to nanowire structures," *MRS Bulletin*, vol. 39, no. 08, pp. 668–677, 2014.
- [3] J. Lin, D. A. Antoniadis, and J. A. del Alamo, "Novel intrinsic and extrinsic engineering for high-performance high-density self-aligned InGaAs MOSFETs: Precise channel thickness control and sub-40 nm metal contacts," in *Proc. IEDM*, 2014, p. 574.
- [4] T.-W. Kim *et al.*, " $L_G = 80$ nm tri-gate quantum-well $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect transistors with Al_2O_3/HfO_2 gate stack," *IEEE Electron Device Letters*, vol. 36, no. 3, pp. 223–225, 2015.
- [5] C. Y. Huang *et al.*, "Low power III-V InGaAs MOSFETs featuring InP recessed source/drain spacers with $I_{on} = 120$ $\mu A/\mu m$ at $I_{off} = 1$ nA/ μm and $V_{DS} = 0.5$ V," in *Proc. IEDM*, 2014, pp. 586–589.
- [6] A. C. Ford, J. C. Ho, Y.-I. Chueh, Y.-c. Tseng, Z. Fan, J. Guo, J. Bokor, and A. Javey, "Diameter-dependent electron mobility of InAs nanowires," *Nano Letters*, vol. 9, no. 1, pp. 360–365, 2009.
- [7] M. Lundstrom and Z. Ren, "Essential physics of carrier transport in nanoscale MOSFETs," *IEEE Transactions on Electron Devices*, vol. 49, no. 1, pp. 133–141, 2002.
- [8] T.-W. Kim, D.-H. Kim, and J. A. del Alamo, "60 nm self-aligned-gate InGaAs HEMTs with record high-frequency characteristics," in *Proc. IEDM*, 2010, pp. 30.7.1–30.7.4.