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InGaAs Nanowire MOSFETs with I_{ON} = 555 µA/µm at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V

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Abstract

We report on $In_{0.85}Ga_{0.15}As$ nanowire MOSFETs (NWFETs) with record performance in several key metrics for VLSI applications. These devices exhibit I_{ON} = 555 µA/µm (at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V), I_{ON} = 365 µA/µm (at I_{OFF} = 10 nA/µm and V_{DD} = 0.5 V) and a quality factor Q ≡ g_m/SS of 40, all of which are the highest reported for a III-V as well as silicon transistor. Furthermore, a highly scalable, self-aligned gate-last fabrication process is utilized, with a single nanowire as the channel. The devices use a 45° angle between the nanowire and the contacts, which allows for up to a 1.4 times longer gate length at a given pitch.

Introduction

$In_xGa_{x-1}As$ MOSFETs are expected to deliver high on-currents at a reduced V_{DD} of 0.5 V, making them suitable for VLSI applications. This is due to their high mobility, which enables increased transconductance g_m at a given L_G. For instance, we have recently demonstrated $In_{0.85}Ga_{0.15}As$ NWFETs with g_m = 3.3 mS/µm, surpassing that of all other III-V and silicon transistors, including HEMTs [4]. However, to achieve high I_{ON} at a specified I_{OFF} and V_{DD} = 0.50 V (an important VLSI metric) comparable to state-of-the-art silicon technology, the subthreshold slope must be near 60 mV/decade. This is challenging in III-V technology due to the oxide interface quality and small band gap, causing e.g. band-to-band-tunneling in the off-state. Recently, planar InAs MOSFETs with I_{ON} matching or surpassing that of silicon technology were reported [12]. In this work, we report on NWFETs with a new record of I_{ON} = 555 µA/µm at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V.

Device Fabrication

Fig. 1 shows a schematic of the fabricated device, and the process flow. The nanowires are formed by selective area growth, using hydrogen silsesquioxane (HSQ) as the MOCVD growth mask. The composition of the nanowire layer is $In_{0.63}Ga_{0.37}As$, while the nanowire is $In_{0.85}Ga_{0.15}As$, determined by EDX. Fig. 2(a)-(c) demonstrate the scalability of the selective growth process. A high-density nanowire-cluster with nanowire spacing of <10 nm is shown in fig. 2c. In this work, we characterize single-nanowire devices. The highly doped $In_{0.63}Ga_{0.37}As$ (N_D = 5 × 10^{19} cm^{-3}) contact layer is formed from a subsequent MOCVD growth step using HSQ as a dummy gate [Fig. 2(d)]. A 45° angle between the nanowire and the contacts is chosen in order to obtain optimal crystal facets. At a given pitch, this will also improve electrostatic control by allowing a longer gate length. After mesa isolation, Ti/Pd/Au is patterned and evaporated as the contact metal. The InP in the channel region is etched by HCl (1:1), in order for the metal to properly cover the sides of the nanowire. Several cycles of surface oxidation by ozone and diluted HCl etching is performed in order to reduce the dimensions of the nanowire. Surface passivation, by $(NH4)_2S$ (1:1) for 20 min, is followed by deposition of Al_2O_3/HfO_2 (EOT = 1.5 nm) by ALD at 300/100°C. Subsequently, an in-situ 12 hour post-deposition annealing step at 100°C in N_2 atmosphere is performed. Ni/Pd gate metal patterning and evaporation completes the process.

Results

Fig. 3(a)-(c) show subthreshold, transfer and output characteristics of an L_G = 70 nm NWFET with nanowire width and height W_{NW}/H_{NW} = 25/7 nm. Peak transconductance is $g_{m,peak}$ = 2.85 mS/µm. The subthreshold characteristics for the same device are shown in Fig. 4. The subthreshold slope (SS) is 80 mV/decade at both V_{DS} = 0.5 V and 50 mV. The drain-induced barrier-lowering (DIBL) is 43 mV/V at I_{DS} = 1 µA/µm. The device exhibits I_{ON} = 555 µA/µm at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V, which is the highest reported value for a MOSFET. The quality factor Q ≡ g_m/SS is 35 for this device. The on-resistance is R_{ON} = 177 Ωµm at V_{GS} > 1.4 V. The specific contact resistivity is $\rho_C = 7\times10^{-8}$ Ωcm^{-2} and the sheet resistance of the n^+ $In_{0.63}Ga_{0.37}As$ contact layer is $R_{\square}$ = 70 Ω/□, both calculated from TLM measurements.

Fig. 4 shows transfer characteristics for another L_G = 70 nm device with $g_{m,peak}$ = 2.65 mS/µm at V_{DS} = 0.5 V. The average SS over one, two and three decades is 65, 69 and 73 mV/decade, respectively, all at V_{DS} = 0.5 V. This device shows I_{ON} = 535 µA/µm at I_{OFF} = 100 nA/µm and I_{ON} = 365 µA/µm at I_{OFF} = 10 nA/µm, V_{DD} = 0.5 V. This is the highest reported I_{ON} at I_{OFF} = 10 nA/µm. DIBL is 56 mV/V at I_{DS} = 1 µA/µm. The quality factor Q ≡ g_m/SS is 40 for this device, which is the highest reported Q-factor for a MOSFET. The difference in SS between these devices may be explained by the discrete nature of traps in the small channel area (2 × 10^{-3} µm^2).

The hysteresis (Fig. 5) is ΔV_T = 60 mV for V_{GS} = 0.2-1.0 V, indicating high-quality oxide and oxide interface. I_{OFF} versus I_{ON} for several devices with L_G = 70 nm and W_{NW}/H_{NW} = 25/7 nm is shown in Fig. 6, measured at a swing of V_{DD} = 0.5 V. Fig. 7 shows SS versus L_G. Error bars show the standard deviation. SS and DIBL versus nanowire width W_{NW} is shown in Fig. 8 (H_{NW} = 7 nm). Data points are offset for clarity. Improved electrostatic control from use of smaller nanowires can clearly be observed. The trend indicates that SS can be further reduced by additional scaling down of W_{NW}. Fig. 9 and 10 show benchmarks of I_{ON} and Q for various planar and non-planar MOSFETs.

Conclusions

We have demonstrated highly scalable nanowire MOSFETs with record high performance in several key VLSI metrics. We have shown a device with g_m = 2.85 mS/µm, SS = 80 mV/decade and I_{ON} = 555 µA/µm at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V. We have also shown a device with g_m = 2.65 mS/µm and SS = 65 mV/decade, which gives a quality factor Q = 40.

Acknowledgements

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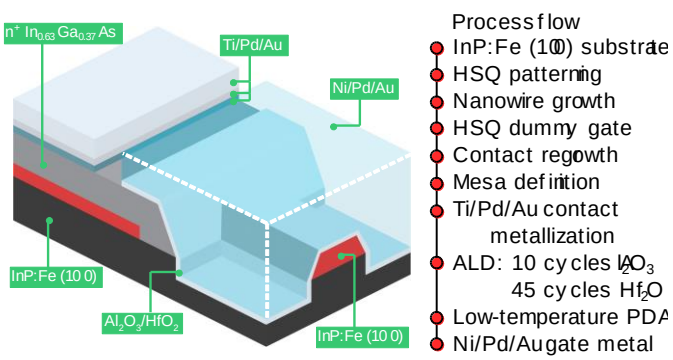

Fig. 1. Schematic of the final device, as well as the device fabrication process flow.

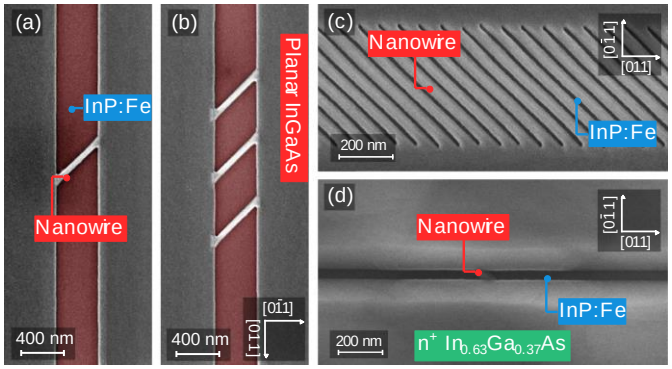

Fig. 2. (a-c) False-color SEM images showing the scalability of the NW fabrication process. (d) The device after contact regrowth.

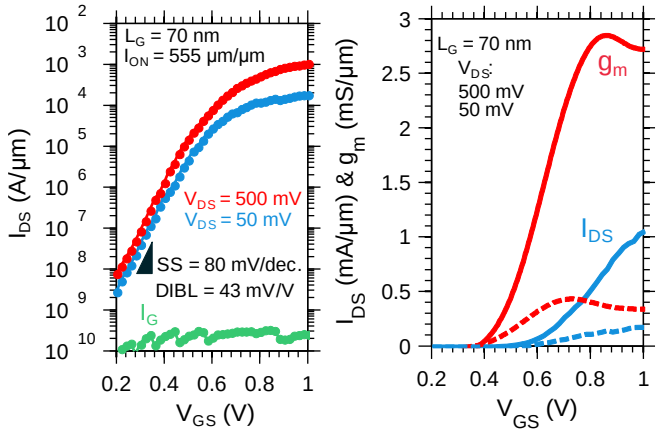

Fig. 3. (a) Subthreshold, (b) transfer and (c) output characteristics of the same L_G = 70 nm, W_{NW}/H_{NW} = 25/7 nm device. I_{ON} = 555 μA/μm at I_{OFF} = 100 nA/μm and V_{DD} = 0.5 V.

Fig. 4. (a) I_{DS}-V_{GS} for an L_G = 70 nm, W_{NW}/H_{NW} = 25/7 nm device.

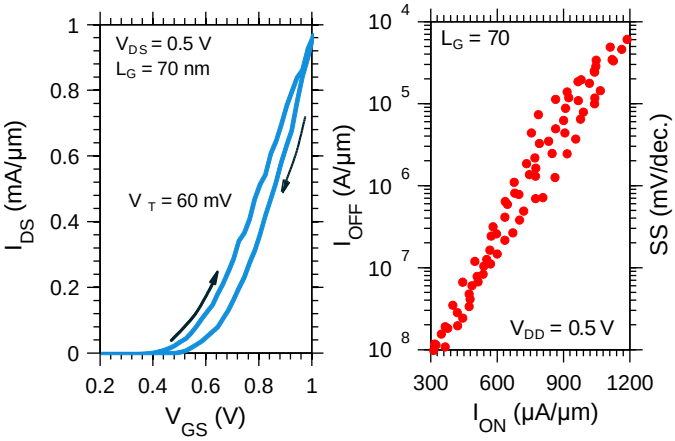

Fig. 5. (a) Hysteresis measurement of an L_G = 70 nm device.

Fig. 6. (a) I_{OFF} versus I_{OFF} for L_G = 70 nm devices.

Fig. 7. (a) SS versus L_G for W_{NW} = 25 nm devices.

Fig. 8. (a) SS and DIBL versus W_{NW} for L_G = 70 nm and H_{NW} = 7 nm devices.

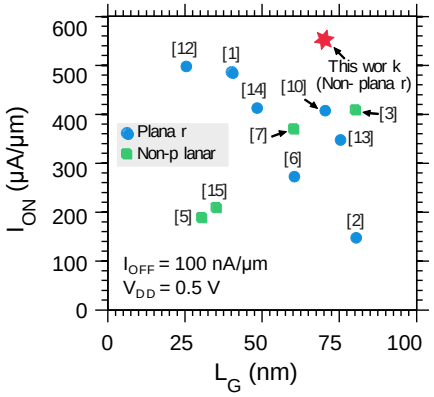

Fig. 9. Benchmark of I_{ON} at I_{OFF} = 100 nA/μm and V_{DD} = 0.5 V.

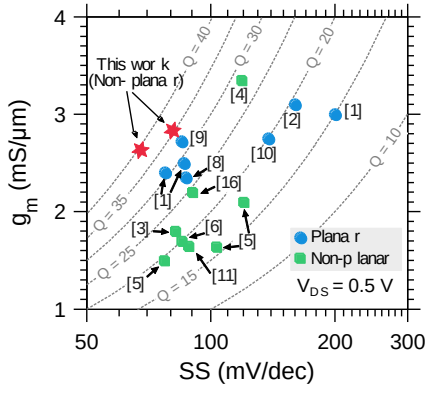

Fig. 10. Benchmark of Q = g_m/SS at V_{DS} = 0.5 V for various planar and non-planar III-V FETs.

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