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High-Frequency InGaAs Tri-gate MOSFETs with f_{max} of 400 GHz

C. B. Zota, F. Lindelöw, L.-E. Wernersson and E. Lind

We report on extremely scaled down tri-gate RF MOSFETs utilizing lateral nanowires as the channel, with gate length and nanowire width both of 20 nm. These devices exhibit simultaneous extrapolated f_t and f_{max} of 275 and 400 GHz at V_{DS} = 0.5 V, which is the largest combined f_t and f_{max}, as well as the largest f_{max} reported for all III-V MOSFET.

Introduction: Tri-gate (or non-planar) MOSFETs for RF-applications are motivated by that the use of a high-k oxide, rather than a semiconductor barrier (as in HEMTs) allows for higher gate capacitance in the MOSFET [1-2]. Furthermore, the tri-gate architecture improves short-channel effects, allowing for shorter gate length, L_G, without degradation of performance due to short-channel effects. Both these points enable higher ideal transconductance, g_m, in MOSFETs compared to HEMTs, assuming similar electron mobility. In fact, state-of-the-art III-V MOSFET devices exhibit g_m larger than that of record HEMTs, although they presently do not allow RF-compatible device designs [3-5].

In this work, we present RF-compatible tri-gate $In_{0.85}Ga_{0.15}As$ MOSFETs utilizing lateral nanowires (NWs) as the channel. Compared to our previous work, we have here further scaled down device dimensions, L_G and nanowire width, W_{NW} [6]. This enables higher g_m at V_{DS} = 0.5 V, which significantly improves f_t/f_{max} from 220/305 GHz to 275/400 GHz. The combined f_t and f_{max}, as well as the f_{max} of these devices represent the highest reported values for all III-V MOSFETs.

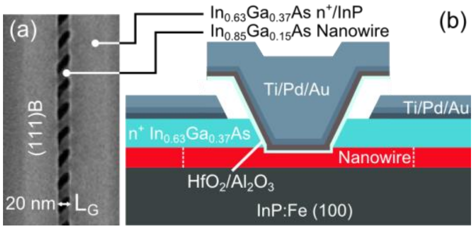

Fig. 1 *Device fabrication and device materials and design*

a SEM image of the device after contact regrowth, L_G is defined as the distance between n^+ contacts. (111)B denotes the crystal facet of the contact layer.

b Schematic figure of the fabricated device.

Fabrication: The device fabrication process is similar to what has been described elsewhere [7]. The device channel consists of 200 lateral $In_{0.85}Ga_{0.15}As$ nanowires, formed by selective area MOCVD growth on (100) InP:Fe (S.I.) substrate, split over two gate fingers. The nanowire width is 20 nm, and the height is 11 nm. The S/D highly doped regions are formed by a second MOCVD growth step of 40 nm n^+ $In_{0.63}Ga_{0.37}As$/100 nm InP with in-situ Sn-doping ($N_D = 5\times10^{19}$ cm^{-3}) in the doped layer (Fig. 1a). Subsequently, 1 nm/5 nm Al_2O_3/HfO_2 is deposited by ALD and Ti/Pd/Au by thermal evaporation, forming the gate stack. The regrown 100 nm InP is selectively etched by an HCl solution leaving a T-gate. S/D and pad metallization of Ti/Pd/Au completes the process (Fig. 1b).

Results: Fig. 2a shows transfer characteristics of a device with L_G = 20 nm measured at DC with a Keithley 4200 semiconductor characterization system. All data is normalized to the total gated periphery of the NWs (7 µm). At V_{DS} = 0.5 V, peak g_m is 2.1 mS/µm. Fig. 2b shows the scaling behaviour of peak g_m and on-resistance R_{on} versus L_G. R_{on} reaches 220 Ωµm at L_G = 20 nm. The total access resistance is estimated to 130 Ωµm from transmission line measurements.

RF-measurements where performed at 40 MHz to 67 GHz with an Agilent E8361A vector network analyser. On-chip pad de-embedding as well as off-chip two-port load-reflect-reflect-match calibration was performed. The total pad capacitances were approximately 20 fF.

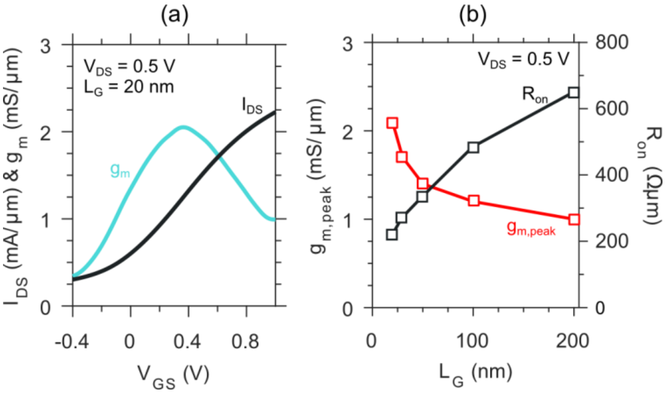

Fig. 2 *Device characteristics at DC.*

a Transfer characteristics of a L_G = 20 nm device.

b Scaling behaviour of peak g_m and R_{on} versus L_G.

A small-signal model was determined from the measured S-parameters, with a good fit to the measurement data [8]. Fig. 3 shows measured and modelled (dashed traces) unilateral power gain $|U|$, current gain $|h_{21}|^2$ and maximum available/stable gain (|MAG| and |MSG|) for a device with L_G = 20 nm. Extrapolated cut-off frequency f_t is 275 GHz and maximum oscillation frequency f_{max} is 400 GHz.

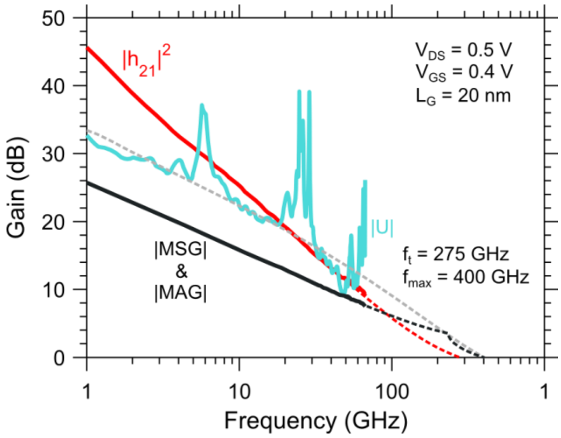

Fig. 3 *Measured and modelled (dashed traces) gain of an L_G = 20 nm device at V_{DS} = 0.5 V.*

The small-signal model, which is similar to that in [6], includes both the effect of border traps in the oxide, and impact ionization. Border traps are modelled using the distributed border trap model in [9]. Border traps introduce a frequency-dependency to g_m and g_d, as well as a frequency-dependent oxide loss, and explain the -10 dB slope of $|U|$ versus f [10]. Fig. 4a shows $g_{m,peak}$ for an L_G = 20 nm device extracted from the small-signal model at DC and 67 GHz (RF). $g_{m,peak}$ increases by approximately 13% in the latter case, to a maximum of 2.9 mS/µm at V_{DS} = 1.25 V, which is attributable to that trap responses are partially disabled at high frequency.

The effective gate resistance is ~5 Ω, and the source and drain resistances are ~2 Ω. The gate-to-source and gate-to-drain capacitances, C_{GS} and C_{GD}, are shown in Fig. 4b. At V_{DS} = 0.5 V, the total gate capacitance $C_{GS} + C_{GD}$ is 15 fF at peak g_m. This includes both the parasitic capacitance from the source and drain gate overlaps, and the intrinsic gate capacitance. The latter is estimated as $C_{gg,int} = (2/3)WLC_{ox}/(C_q + C_{ox})$, with the quantum capacitance $C_q = q^2m^*/\pi\hbar^2$, which is ~2 fF with m* = 0.04m_0. Thus, RF-performance is primarily limited by the parasitic overlap capacitance, which can be lowered by implementation of source and drain spacers.

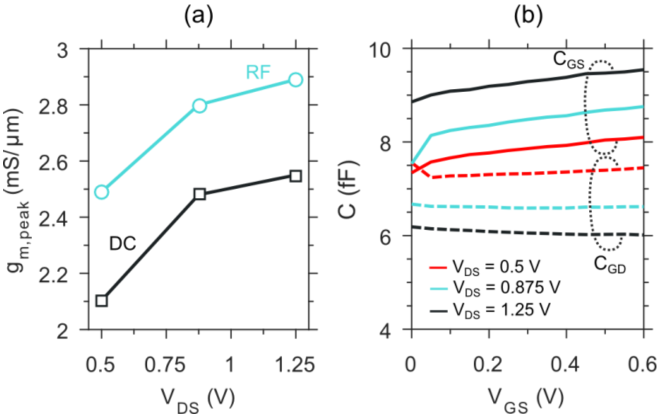

Fig. 4 *Peak g_m and capacitances*

a Peak g_m measured at both 40 MHz (DC) and 67 GHz (RF), for an L_G = 20 nm device.

b Gate-to-source, C_{GS}, and gate-to-drain, C_{GD}, capacitances measured at different V_{DS}.

Fig. 5 shows a benchmark of f_t, f_{max} and the geometric mean $\sqrt{f_t \times f_{max}}$ (dashed traces) for state-of-the-art III-V MOSFETs [11-18]. The geometric mean is 330 GHz for these devices, which is the highest reported value for a III-V MOSFET. Squares show planar devices, and triangles show non-planar devices.

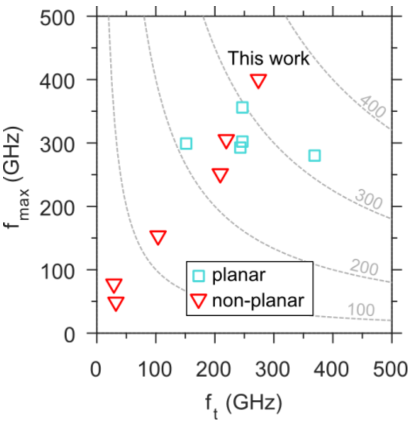

Fig. 5 *Benchmark of RF-performance for III-V MOSFETs*

Squares show planar devices, triangles show non-planar devices. V_{DS} and L_G varies between devices, but is 0.5 V and 20 nm, respectively, for this work. Dashed traces show the geometric mean.

Conclusion: We have demonstrated L_G = 20 nm $In_{0.85}Ga_{0.15}As$ tri-gate MOSFETs with record high-frequency performance, f_t = 275 GHz and f_{max} = 400 GHz at V_{DS} = 0.5 V.

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