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LUND UNIVERSITY

PO Box 117
221 00 Lund
+46 46-222 00 00

High-Frequency InGaAs Tri-gate MOSFETs with f_{max} of 400 GHz

C. B. Zota, F. Lindelöw, L.-E. Wernersson and E. Lind

We report on extremely scaled down tri-gate RF MOSFETs utilizing lateral nanowires as the channel, with gate length and nanowire width both of 20 nm. These devices exhibit simultaneous extrapolated f_i and f_{max} of 275 and 400 GHz at $V_{\text{DS}} = 0.5$ V, which is the largest combined f_i and f_{max} , as well as the largest f_{max} reported for all III-V MOSFET.

Introduction: Tri-gate (or non-planar) MOSFETs for RF-applications are motivated by that the use of a high-k oxide, rather than a semiconductor barrier (as in HEMTs) allows for higher gate capacitance in the MOSFET [1-2]. Furthermore, the tri-gate architecture improves short-channel effects, allowing for shorter gate length, L_G , without degradation of performance due to short-channel effects. Both these points enable higher ideal transconductance, g_m , in MOSFETs compared to HEMTs, assuming similar electron mobility. In fact, state-of-the-art III-V MOSFET devices exhibit g_m larger than that of record HEMTs, although they presently do not allow RF-compatible device designs [3-5].

In this work, we present RF-compatible tri-gate $\text{In}_{0.85}\text{Ga}_{0.15}\text{As}$ MOSFETs utilizing lateral nanowires (NWs) as the channel. Compared to our previous work, we have here further scaled down device dimensions, L_G and nanowire width, W_{NW} [6]. This enables higher g_m at $V_{\text{DS}} = 0.5$ V, which significantly improves f_i/f_{max} from 220/305 GHz to 275/400 GHz. The combined f_i and f_{max} , as well as the f_{max} of these devices represent the highest reported values for all III-V MOSFETs.

Fig. 1 Device fabrication and device materials and design

a SEM image of the device after contact regrowth, L_G is defined as the distance between n^+ contacts. (111)B denotes the crystal facet of the contact layer.

b Schematic figure of the fabricated device.

Fabrication: The device fabrication process is similar to what has been described elsewhere [7]. The device channel consists of 200 lateral $\text{In}_{0.85}\text{Ga}_{0.15}\text{As}$ nanowires, formed by selective area MOCVD growth on (100) InP:Fe (S.I.) substrate, split over two gate fingers. The nanowire width is 20 nm, and the height is 11 nm. The S/D highly doped regions are formed by a second MOCVD growth step of 40 nm n^+ $\text{In}_{0.63}\text{Ga}_{0.37}\text{As}/100$ nm InP with in-situ Sn-doping ($N_D = 5 \times 10^{19} \text{ cm}^{-3}$) in the doped layer (Fig. 1a). Subsequently, 1 nm/5 nm $\text{Al}_2\text{O}_3/\text{HfO}_2$ is deposited by ALD and Ti/Pd/Au by thermal evaporation, forming the gate stack. The regrown 100 nm InP is selectively etched by an HCl solution leaving a T-gate. S/D and pad metallization of Ti/Pd/Au completes the process (Fig. 1b).

Results: Fig. 2a shows transfer characteristics of a device with $L_G = 20$ nm measured at DC with a Keithley 4200 semiconductor characterization system. All data is normalized to the total gated periphery of the NWs (7 μm). At $V_{\text{DS}} = 0.5$ V, peak g_m is 2.1 $\text{mS}/\mu\text{m}$. Fig. 2b shows the scaling behaviour of peak g_m and on-resistance R_{on} versus L_G . R_{on} reaches 220 $\Omega\mu\text{m}$ at $L_G = 20$ nm. The total access resistance is estimated to 130 $\Omega\mu\text{m}$ from transmission line measurements.

RF-measurements were performed at 40 MHz to 67 GHz with an Agilent E8361A vector network analyser. On-chip pad de-embedding as well as off-chip two-port load-reflect-match calibration was performed. The total pad capacitances were approximately 20 fF.

Fig. 2 Device characteristics at DC.

a Transfer characteristics of a $L_G = 20$ nm device.

b Scaling behaviour of peak g_m and R_{on} versus L_G .

A small-signal model was determined from the measured S-parameters, with a good fit to the measurement data [8]. Fig. 3 shows measured and modelled (dashed traces) unilateral power gain $|U|$, current gain $|h_{21}|^2$ and maximum available/stable gain ($|MAG|$ and $|MSG|$) for a device with $L_G = 20$ nm. Extrapolated cut-off frequency f_i is 275 GHz and maximum oscillation frequency f_{max} is 400 GHz.

Fig. 3 Measured and modelled (dashed traces) gain of an $L_G = 20$ nm device at $V_{\text{DS}} = 0.5$ V.

The small-signal model, which is similar to that in [6], includes both the effect of border traps in the oxide, and impact ionization. Border traps are modelled using the distributed border trap model in [9]. Border traps introduce a frequency-dependency to g_m and g_d , as well as a frequency-dependent oxide loss, and explain the -10 dB slope of $|U|$ versus f [10]. Fig. 4a shows $g_{m,\text{peak}}$ for an $L_G = 20$ nm device extracted from the small-signal model at DC and 67 GHz (RF). $g_{m,\text{peak}}$ increases by approximately 13% in the latter case, to a maximum of 2.9 $\text{mS}/\mu\text{m}$ at $V_{\text{DS}} = 1.25$ V, which is attributable to that trap responses are partially disabled at high frequency.

The effective gate resistance is $\sim 5 \Omega$, and the source and drain resistances are $\sim 2 \Omega$. The gate-to-source and gate-to-drain capacitances, C_{GS} and C_{GD} , are shown in Fig. 4b. At $V_{\text{DS}} = 0.5$ V, the total gate capacitance $C_{\text{GS}} + C_{\text{GD}}$ is 15 fF at peak g_m . This includes both the parasitic capacitance from the source and drain gate overlaps, and the intrinsic gate capacitance. The latter is estimated as $C_{\text{gg,int}} = (2/3)WLC_{\text{ox}}/(C_q + C_{\text{ox}})$, with the quantum capacitance $C_q = q^2 m^*/\pi \hbar^2$, which is ~ 2 fF with $m^* = 0.04m_0$. Thus, RF-performance is primarily limited by the parasitic overlap capacitance, which can be lowered by implementation of source and drain spacers.

Fig. 4 Peak g_m and capacitances

a Peak g_m measured at both 40 MHz (DC) and 67 GHz (RF), for an $L_G = 20$ nm device.

b Gate-to-source, C_{GS} , and gate-to-drain, C_{GD} , capacitances measured at different V_{DS} .

Fig. 5 shows a benchmark of f_t , f_{max} and the geometric mean $\sqrt{f_t \times f_{max}}$ (dashed traces) for state-of-the-art III-V MOSFETs [11–18]. The geometric mean is 330 GHz for these devices, which is the highest reported value for a III-V MOSFET. Squares show planar devices, and triangles show non-planar devices.

Fig. 5 Benchmark of RF-performance for III-V MOSFETs

Squares show planar devices, triangles show non-planar devices. V_{DS} and L_G varies between devices, but is 0.5 V and 20 nm, respectively, for this work. Dashed traces show the geometric mean.

Conclusion: We have demonstrated $L_G = 20$ nm $\text{In}_{0.85}\text{Ga}_{0.15}\text{As}$ tri-gate MOSFETs with record high-frequency performance, $f_t = 275$ GHz and $f_{max} = 400$ GHz at $V_{DS} = 0.5$ V.

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C. B. Zota, F. Lindelöw, L.-E. Wernersson and E. Lind (Department of Electrical and Information Technology, Lund University, Box 118 S-221 00, Lund, Sweden)

E-mail: cesar.zota@eit.lth.se

References

- [1] H. Riel, L.-E. Wernersson, M. Hong, and J. a. del Alamo, “III-V compound semiconductor transistors—from planar to nanowire structures,” *MRS Bull.*, 2014, **39**(08), pp. 668–677, DOI: 10.1557/mrs.2014.137
- [2] D.-H. Kim, B. Brar, and J. A. del Alamo, “ $f_t = 688$ GHz and $f_{max} = 800$ GHz in $L_g = 40$ nm $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ MHEMTs with $g_{m,max} > 2.7$ $\text{mS}/\mu\text{m}$,” *Proc. IEEE Int. Electron Device Meeting (IEDM)*, Dec. 2011, pp. 13.6.1–13.6.4, 2011, DOI: 10.1109/IEDM.2011.6131548
- [3] C. B. Zota, L. E. Wernersson, and E. Lind, “Single suspended

InGaAs nanowire MOSFETs,” *Proc. IEEE Int. Electron Device Meeting (IEDM)*, Washington, D.C., Dec. 2015, pp. 31.4.1–31.4.4, DOI: 10.1109/IEDM.2015.7409808

[4] J. Lin, X. Cai, Y. Wu, D. A. Antoniadis, and J. A. Del Alamo, “Record maximum transconductance of 3.45 $\text{mS}/\mu\text{m}$ for III-V FETs,” *IEEE Electron Device Lett.*, 2016, **37**(4), pp. 381–384, DOI: 10.1109/LED.2016.2529653

[5] S. Lee, V. Chobpattana, C.-Y. Huang, B. J. Thibeault, W. Mitchell, S. Stemmer, A. C. Gossard, and M. J. W. Rodwell, “Record I_{on} (0.50 $\text{mA}/\mu\text{m}$ at $V_{DD} = 0.5$ V and $I_{off} = 100$ $\text{nA}/\mu\text{m}$) 25 nm-gate-length $\text{ZrO}_2/\text{InAs}/\text{InAlAs}$ MOSFETs,” 2014 Symp. VLSI Technol. Dig. Tech. Pap., June 2014, pp. 1–2, DOI: 10.1109/VLSIT.2014.6894363

[6] C. B. Zota, G. Roll, L.-E. Wernersson, and E. Lind, “Radio-Frequency Characterization of Selectively Regrown InGaAs Lateral Nanowire MOSFETs,” *IEEE Trans. Electron Devices*, 2014, **61**(12), pp. 4078–4083, DOI: 10.1109/TED.2014.2363732

[7] C. B. Zota, D. Lindgren, L. E. Wernersson, and E. Lind, “Quantized Conduction and High Mobility in Selectively Grown $\text{InxGa}_{1-x}\text{As}$ Nanowires,” *ACS Nano*, 2015, **9**(10), pp. 9892–9897, DOI: 10.1021/acsnano.5b03318

[8] I. Kwon, M. Je, K. Lee, and H. Shin, “A simple and analytical parameter-extraction method of a microwave MOSFET,” *IEEE Trans. Microw. Theory Tech.*, 2002, **50**(6), pp. 1503–1509, DOI: 10.1109/TMTT.2002.1006411

[9] Y. Yuan, L. Wang, B. Yu, B. Shin, J. Ahn, P. C. McIntyre, P. M. Asbeck, M. J. W. Rodwell, and Y. Taur, “A Distributed Model for Border Traps in $\text{Al}_2\text{O}_3/\text{InGaAs}$ MOS devices,” 2011, **32**(4), pp. 485–487, DOI: 10.1109/LED.2011.2105241

[10] S. Johansson, M. Berg, K.-M. Persson, and E. Lind, “A High-Frequency Transconductance Method for Characterization of High-k Border Traps in III-V MOSFETs,” *IEEE Trans. Electron Devices*, 2013, **60**(2), pp. 776–781, DOI: 10.1109/TED.2012.2231867

[11] J. Mo, E. Lind, and L.-E. Wernersson, “Asymmetric InGaAs/InP MOSFETs With Source/Drain Engineering,” *IEEE Electron Device Lett.*, 2014, **35**(5), pp. 515–517, DOI: 10.1109/LED.2014.2308925

[12] T. Kim, R. J. W. Hill, C. D. Young, D. Veksler, L. Morassi, S. Oktyabrshky, J. Oh, C. Y. Kang, D. Kim, J. A. Alamo, C. Hobbs, P. D. Kirsch, and R. Jammy, “ InAs Quantum-Well MOSFET ($L_g = 100$ nm) with Record High g_m , f_r and f_{max} ,” 2012 Symp. VLSI Technol. Dig. Tech. Pap., June 2012, pp. 179–180, DOI: 10.1109/VLSIT.2012.6242520

[13] K. D. Chabak, X. Miao, C. Zhang, S. Member, D. E. Walker, P. K. Mohseni, X. Li, and S. Member, “RF Performance of Planar III – V Nanowire-Array Transistors Grown by Vapor – Liquid – Solid Epitaxy,” 2015, **36**(5), pp. 445–447, DOI: 10.1109/LED.2015.2416978

[14] S. Johansson, E. Memisevic, L.-E. Wernersson, and E. Lind, “High-Frequency Gate-All-Around Vertical InAs Nanowire MOSFETs on Si Substrates,” *IEEE Electron Device Lett.*, 2014, **35**(5), pp. 518–520, DOI: 10.1109/LED.2014.2310119

[15] D.-H. Kim, J. A. del Alamo, D. A. Antoniadis, J. Li, J.-M. Kuo, P. Pinsukanjana, Y.-C. Kao, P. Chen, A. Papavasiliou, C. King, E. Regan, M. Urteaga, B. Brar, and T.-W. Kim, “ $L_g = 60$ nm recessed $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ metal-oxide-semiconductor field-effect transistors with Al_2O_3 insulator,” *Appl. Phys. Lett.*, 2012, **101**(22), p. 223507, DOI: 10.1063/1.4769230

[16] M. Berg, O. Kilpi, K. Persson, J. Svensson, M. Hellenbrand, E. Lind, and L.-E. Wernersson, “Electrical Characterization and Modeling of Gate-Last Vertical InAs Nanowire MOSFETs on Si,” 2016, **37**(8), pp. 966–969, DOI: 10.1109/LED.2016.2581918

[17] K. Dae-Hyun, K. Tae-Woo, R. J. W. Hill, C. D. Young, K. Chang Yong, C. Hobbs, P. Kirsch, J. A. del Alamo, and R. Jammy, “High-Speed E-Mode InAs QW MOSFETs With Al_2O_3 Insulator for Future RF Applications,” *Electron Device Lett. IEEE*, 2013, **34**(2), pp. 196–198, DOI: 10.1109/LED.2012.2229107

[18] M. Egard, L. Ohlsson, M. Årlelid, K. Persson, B. M. Borg, F. Lenrick, R. Wallenberg, E. Lind, and L. Wernersson, “High-Frequency Performance of Self-Aligned,” *IEEE Electron Device Lett.*, 2012, **33**(3), pp. 369–371, DOI: 10.1109/LED.2011.2181323