Continuous-Time Delta-Sigma Modulators for Ultra-Low-Power Radios

Radjen, Dejan

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Continuous-Time $\Delta\Sigma$ Modulators for Ultra-Low-Power Radios

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Abstract

The modern small devices of today require cheap low power radio frequency (RF) transceivers that can provide reliable connectivity at all times. In an RF transceiver, the analog-to-digital converter (ADC) is one of the most important parts and it is also one of the main power consumers. There are several architectures for implementing an ADC, but in the last decade, continuous-time $\Delta\Sigma$ modulators (CT DSMs) have become popular due to their potential of achieving low power consumption and the inherent anti-alias filtering.

This thesis investigates different implementations of CT DSMs intended for an ultra-low-power (ULP) receiver operating in the 2.45 GHz ISM band. The main focus is on power saving techniques and jitter insensitive solutions. Papers I and II present a CT DSM with dual switched-capacitor-resistor (DSCR) feedback used in the first DAC. This technique has been developed for the purpose of reducing the jitter sensitivity of the CT DSM while keeping the DAC peak current lower than for conventional SCR feedback. A lower peak current translates into more relaxed slew-rate requirements on the first operational amplifier and thereby less power consumption. Papers III and IV present a low power 2nd-order CT DSM with one operational amplifier. The main objective was to reduce the power consumption of the usually more critical analog part while still achieving a 2nd-order noise shaping. The thesis also examines the possibility of using a successive approximation register (SAR) quantizer instead of the commonly used flash quantizer to reduce the power consumption of the digital part as well.

Populärvetenskaplig sammanfattning

Små, trådlösa och portabla apparater utgör idag en stor del av vår uppkopplade värld. Under det senaste decenniet har dock flera teknologiska framsteg lett mot en utveckling där allt från maskiner till kläder kommunicerar med varandra. Detta brukar kallas för "sakernas internet" och uppskattas involvera 50 miljarder enheter år 2020. Genom att förse dessa enheter med små och smarta sensorer är det möjligt att känna av omgivningen och samla in olika former av data. Det finns många potentiella applikationer där detta är av intresse t.ex. medicinska implantat, spelkontroller, smarta hus och industriell övervakning. Inom medicinska tillämpningar har sensornätverk redan använts för att hålla reda på patientens tillstånd och olika kroppsvärden.

En av de största utmaningarna med sensornätverk är effektförbrukningen som bestämmer hur länge batteriet för en sensor kommer att räcka. Det är viktigt att batteritiden är så lång som möjligt eftersom sensorerna kan vara placerade på ställen som är svåra och farliga att komma åt. Energin från batteriet som sensorn har är det enda energin som den kommer få under dess livslängd. Eftersom batteritekniken går sakta framåt, är det viktigt att utveckla effektiva elektroniska kretsar och algoritmer som minimerar effekten som dras från batteriet.

En sensor kräver i slutändan digitala signaler för att uppnå den funktionalitet som anses viktig idag. Eftersom alla signaler i naturen är analoga, måste de omvandlas till digitala signaler. Detta är en uppgift för Analog-till-digital (A/D) omvandlaren som är en viktig del i det radiochip som sänder och tar emot signalerna i sensornätverket. Det kostar energi att omvandla analoga till digitala signaler vilket innebär att A/D omvandlaren är en kritisk komponent och ansvarar för en stor del av energiförbrukningen i ett radiochip. Det finns många typer av A/D omvandlare men under senare tid har $\Delta\Sigma$ modulatorn blivit populär inom många applikationer.

Den här avhandlingen undersöker flera kretslösningar med syftet att minska känsligheten för tidsfel, så kallad klockjitter, och sänka effektförbrukningen i $\Delta\Sigma$ modulatorn för en lågeffektsradio. Den första $\Delta\Sigma$ modulatorn som konstruerades använde en speciell lösning med dubbla exponentiella pulser för att minska känsligheten för klockjitter. Dessa pulser håller den maximala återkopplingsströmmen på en rimlig nivå och sänker därför strömkravet för den första förstärkaren. Den här tekniken har verifierats med simuleringar och mätningar på ett tillverkat chip. I den andra $\Delta\Sigma$ modulatorn undersöktes ett andra ordningens filter med bara en förstärkare för att minska effektförbrukningen i den analoga delen. Detta resulterade i en låg effektförbrukning medan den övriga prestandan uppfyllde kraven för lågeffektsradion. Den här tekniken har verifierats med simuleringar och mätningar på ett tillverkat chip. Slutligen användes en annan typ av A/D omvandlare s.k. successiv approximation A/D omvandlare som en del i den sistnämnda $\Delta\Sigma$ modulatorn för att ytterligare sänka effekten i den digitala delen. Konceptet har hittills verifierats med simuleringar.

Det här arbetet har varit en del av ett större projekt som går ut på att konstruera en mottagarkedja för en lågeffektsradio. Kravet för den totala chipstorleken är 1 mm^2 och den maximala effektförbrukningen ska vara 1 mW. Projektet sponsrades av Swedish Foundation for Strategic Research (SSF).

Contents

Preface

This dissertation summarizes my research performed at the Department of Electrical and Information Technology at the Lund University for a Ph.D degree in circuit design. The following papers are considered to be a part of this thesis [1–4]:

- D. Radjen, P. Andreani, M. Anderson, and L. Sundström, "A Continuous Time ΔΣ Modulator with Reduced Clock Jitter Sensitivity through DSCR Feedback", in *Proc. of 29th NORCHIP Conference*, Lund, Sweden, Nov. 14-15 2011, pp. 1-4.
- D. Radjen, P. Andreani, M. Anderson, and L. Sundström, "A Continuous Time ΔΣ Modulator with Reduced Clock Jitter Sensitivity through DSCR Feedback", *Analog Integrated Circuits and Signal Processing*, vol. 74, pp. 21-31, Jan. 2013.
- D. Radjen, P. Andreani, M. Anderson, and L. Sundström, "A Low-Power 2nd-order CT ΔΣ Modulator with a Single Operational Amplifier", in *Proc. of 31th NORCHIP Conference*, Vilnius, Lithuania, Nov. 11-12 2013, pp. 1-4.
- D. Radjen, M. Anderson, L. Sundström and P. Andreani, "A Low-Power 2nd-order CT ΔΣ Modulator with a Single Operational Amplifier", *Analog Integrated Circuits and Signal Processing*, Accepted for publication.

I have also co-authored the following papers which are not considered as a part of this dissertation:

- H. Sjöland, J. B. Anderson, C. Bryant, R. Chandra, O. Edfors, A. J. Johansson, N. S. Mazloum, R. Meraji, P. Nilsson, D. Radjen, J. N. Rodrigues, S. M. Y. Sherazi and V. Öwall, "A Receiver Architecture for Devices in Wireless Body Area Networks", *IEEE J. Emerging and Selected Topics in Circuits and Systems*, vol. 2, no. 1, pp. 82-95, Mar 2012.

- Y. Wu, X. Liu, D. Ye, V. Viswam, L. Zhu, P. Lu, D. Radjen and H. Sjöland, "A 0.13μm CMOS $\Delta\Sigma$ PLL FM transmitter", in *Proc. of 29th NORCHIP Conference*, Lund, Sweden, Nov. 14-15 2011, pp. 1-4.
- J. Lindstrand, D. Radjen, R. Fitzgerald, A. Axholt and H. Sjöland, "An Integrated 3-Level Fully Adjustable PWM Class-D Audio Amplifier in 0.35μm CMOS", in *Proc. of 26th NORCHIP Conference*, Tallinn, Estonia, Nov. 16-17 2008, pp. 168-171.

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Thanks to Professor Henrik Sjöland for supervising the UPD project which I was a part of. I am also thankful to Carl Bryant, Nafiseh Seyed Mazloum, Reza Meraji, Rohit Chandra and Yasser Sherazi for being great project members and friends.

Already during my master studies, I was fortunate to get to know Carl and Jonas Lindstrand with whom I have discussed many topics and learned much about circuit design from. Thank you both for being great friends and for all the lunches and dinners that we had.

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Lastly, I would like to thank my family and my friends for constant support and great times outside the office.

Dejan Radjen
Lund, August 2014

List of acronyms

AA	Anti-alias
ADC	Analog-to-digital converter
CIFB	Cascaded integrator feedback
CIFF	Cascaded integrator feedforward
CT	Continuous-time
DAC	Digital-to-analog converter
DEM	Dynamic-element matching
DLL	Delay-locked loop
DSCR	Dual switched-capacitor-resistor
DSM	$\Delta\Sigma$ modulator
DT	Discrete-time
DWA	Data weighted averaging
FSCR	Full clock period switched-capacitor-resistor
WFSK	Wide-band frequency shift keying

GBW	Gain bandwidth
IBN	In-band noise
IID	Independent and identically distributed
LSB	Least significant bit
NRZ	Nonreturn-to-zero
NTF	Noise transfer function
OBG	Out-of-band gain
OSR	Oversampling ratio
PLL	Phase-locked loop
PP	Pulse-position
PW	Pulse-width
RF	Radio frequency
RZ	Return-to-zero
SAR	Successive approximation register
SC	Switched-capacitor
SCR	Switched-capacitor-resistor
SCSR	Switched-capacitor switched-resistor
SCVR	Switched-capacitor variable-resistor
SNR	Signal-to-noise ratio
SNDR	Signal-to-noise-and-distortion ratio
SOA	Single operational amplifier
SQNR	Signal-to-quantization noise ratio

SSF	Swedish Foundation for Strategic Research
STF	Signal transfer function
ULP	Ultra-low-power
UPD	Ultra-portable devices

List of symbols

A_f	Activity factor
α	Starting time instant of a DAC pulse
β	Ending time instant of a DAC pulse
dQ	Charge error
Δ	Quantization step
e_a	amplitude error sequence
e_q	Jitter charge error sequence
f_{bw}	Signal bandwidth
f_s	Sampling frequency
H_{CT}	Continuous-time feedback transfer function
H_{DT}	Discrete-time feedback transfer function
G_{CT}	Continuous-time forward transfer function
G_{DT}	Discrete-time forward transfer function
$IBN_{j,exp}$	In-band noise due to jittered exponential pulses

$IBN_{j,rec}$	In-band noise due to jittered rectangular pulses
L	Loop filter order
N	Number of bits in the quantizer
N_q	Quantization noise
NTF	Noise transfer function
η_a	Amplitude efficiency
η_j	Jitter suppression efficiency
OSR	Oversampling ratio
Q	Charge
STF	Signal transfer function
σ_j	Standard deviation of the jitter timing error
t_d	Loop delay
t_d	Jitter timing error
T_s	Sampling period
τ	Time constant
τ_d	Normalized loop delay
τ_n	Normalized time constant

1 Introduction

1.1 MOTIVATION

In today's modern world, the use of wireless communication has expanded into many areas of our life. This development stimulates the innovation of new technologies to meet the ever increasing demands on the communication systems. As the wireless revolution now takes its first steps into a future scenario where all things communicate with everything and everywhere, also referred to as Internet of Things, new challenges arise and the old ones are getting more prominent. One of the most critical of these challenges is the power consumption. Especially in ultra-low-power (ULP) wireless applications such as smart sensors and medical implants, it is important to minimize the power consumption and achieve battery lifetimes of several years. The next step is the use of scavenged energy from the surroundings which would eventually eliminate the need for batteries. This level of portability can only be realised by addressing the design issues of the radio frequency (RF) transceiver which is the most critical component in ULP wireless applications. To achieve a truly low power operation, the transceiver should only be activated when sending/receiving data. Furthermore, it should consume minimum amount of power when active and provide sufficiently reliable connectivity at all times.

The analog-to-digital converter (ADC) is a mandatory component in an RF transceiver and cannot be avoided due to the required interface between analog and digital domains. Conversion of analog to digital signals is a power hungry operation which makes the ADC one of the highest power consumers in an ULP RF transceiver. The $\Delta\Sigma$ modulator (DSM) is a type of ADC that has increased in popularity and also found its way in ULP applications. Its operation is based on a negative feedback system which combines two important concepts: oversampling and noise shaping. This enables the use of quantizers with only a few bits while still achieving a high resolution. Due to negative feedback and a low number of

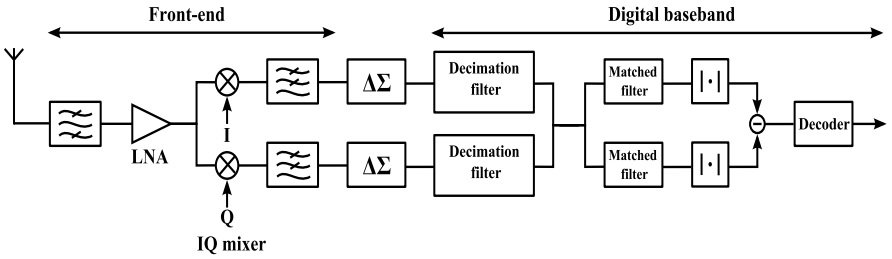

Fig. 1.1: UPD project, receiver chain.

bits, the matching requirements in the quantizer are relaxed.

Traditionally DSMs have been implemented with discrete-time (DT) circuits. These types of modulators are referred to as DT DSMs. In recent years, DSMs using continuous-time (CT) circuits i.e. CT DSMs have received increasing attention due to the following reasons: 1) Relaxed amplifier requirements compared to DT DSMs resulting in lower power consumption. 2) Implicit anti-alias (AA) filtering which is especially beneficial in radio applications. The loop filter is usually the largest power consumer in a CT DSM due to the use of operational amplifiers. This dissertation addresses the issue with power consumption by using alternative loop filter implementations with fewer operational amplifiers while still maintaining the desired resolution. An attempt has also been made to decrease the power consumption in the quantizer. Furthermore, the high clock jitter sensitivity usually associated with CT DSMs has also been considered.

1.2 THE UPD PROJECT

This work has been a part of the ultra-portable devices (UPD) project which was sponsored by Swedish Foundation for Strategic Research (SSF). The objective was to design a receiver chain intended for ULP short range wireless applications. Some of the specifications are as follows:

- Power consumption (active mode): 1 mW.
- Data rate: 250 kb/s.
- Frequency band: 2.45 GHz.
- Chip area: 1 mm^2.

The architecture of the receiver chain is shown in Fig. 1.1. It consist of a direct conversion front-end followed by the $\Delta\Sigma$ ADCs and the digital baseband. The chosen modulation was wideband frequency shift keying (WFSK). This is a constant envelope modulation that is easy to demodulate and it supports the use of

non-linear but efficient power amplifiers. The power budget for one ADC was allocated to 100 μW and the minimum required signal-to-noise-and-distortion ratio (SNDR) found from simulations was 50 dB. More details about the receiver can be found in [5].

1.3 RESEARCH CONTRIBUTIONS

The following are the research contributions from the dissertation:

- A new technique termed dual switched-capacitor-resistor (DSCR) feedback which reduces the peak current of the feedback digital-to-analog converter (DAC) while still maintaining a low sensitivity to clock jitter. Reduced peak current relaxes the slew-rate requirements on the operational amplifiers.
- Analysis and calculation of thermal noise contribution from the DSCR DAC and design procedure for DSCR feedback in CT DSMs.
- A fabricated and measured chip which implements a CT DSM with DSCR feedback.
- Reduction of power consumption in CT DSMs using a 2nd-order single operational amplifier (SOA) loop filter.
- A method for extending the range of realizable feedback coefficients in the chosen 2nd-order SOA loop filter compared to prior work.
- Simulation results including amplifier non-idealities which can be used to assist the design of CT DSMs with the chosen SOA loop filter.
- A fabricated and measured chip which implements a CT DSM with the SOA loop filter. This circuit meets the required specifications of the receiver chain used in the UPD project.
- Reduction of power consumption in CT DSMs by replacing the commonly used flash quantizer with an asynchronous successive approximation (SAR) quantizer.

1.4 OUTLINE

The outline of the dissertation is as follows:

Chapter 1 presents the motivation behind the research topic and gives a short introduction to the UPD-project which this work was a part of. The main research contributions of this dissertation are also outlined.

Chapter 2 gives a basic introduction to DSMs. The concepts that are relevant for the following content are covered.

Chapter 3 discusses the non-idealities typically present in CT DSMs such as excess loop delay, clock jitter and mismatch errors. Different techniques to handle the non-idealities are also covered.

Chapter 4 introduces passive, active-passive and SOA loop filters and how they can be used to reduce the power consumption of CT DSMs. Different circuit implementations are analysed and compared.

Chapter 5 introduces asynchronous SAR quantizers and how they can be used to reduce the power consumption of CT DSMs.

Chapter 6 gives conclusions and future work.

Papers I - IV

2

$\Delta\Sigma$ modulators

This chapter gives a brief introduction to the basic principles of $\Delta\Sigma$ modulators (DSMs) and then focuses on CT DSMs. Important design aspects of CT DSMs such as discrete to continuous-time conversion, selection of the feedback pulses and anti-alias (AA) filtering are covered as well.

2.1 PRINCIPLES OF $\Delta\Sigma$ MODULATION

DSMs employ a combination two important concepts: oversampling and noise shaping. Both of these are discussed in this section.

2.1.1 OVERSAMPLING

Analog-to-digital converters (ADCs) can be divided into two types: Nyquist-rate ADCs and oversampling ADCs. The type of ADC is determined by the oversampling ratio (OSR) which is the ratio between the Nyquist frequency and the signal bandwidth i.e.

$$OSR = \frac{f_s}{2f_{bw}} \tag{2.1}$$

where f_s is the sampling frequency and f_{bw} is the signal bandwidth. A strict definition of a Nyquist ADC would be $OSR = 1$ as the sampling frequency is twice the signal bandwidth, just enough to fulfil the Nyquist sampling criterion. However, in practice, Nyquist ADCs use slightly higher OSR, typically less than 8, to relax the AA filtering [6]. The OSR for oversampling ADCs is usually significantly larger than for Nyquist ADCs and could be several hundreds for certain cases.

Assuming that the quantization noise from an N-bit ADC can be approximated as white noise [7] [8], the power spectral density is spread uniformly in the Nyquist interval as shown in Fig. 2.1. It is obvious that an increased OSR will reduce the IBN since the signal band occupies a smaller portion of the Nyquist in-

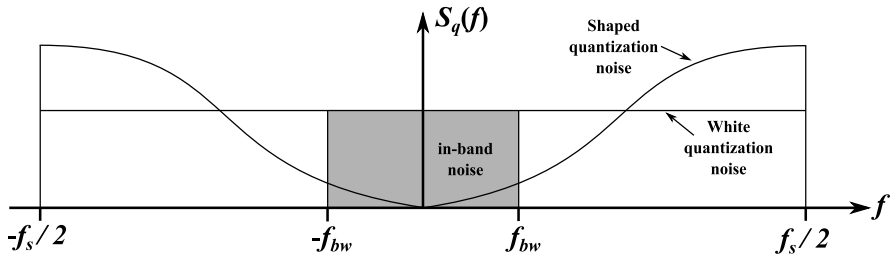

Fig. 2.1: Quantization noise spectra with oversampling and noise shaping.

terval. Every doubling of the OSR improves the signal-to-quantization-noise ratio (SQNR) by 3 dB [9]. However, this improvement is not always sufficient and very high OSRs are often required to significantly increase the SQNR.

2.1.2 NOISE SHAPING

Oversampling can become more effective if the IBN is further reduced by noise shaping. The noise shaped spectrum is also shown in Fig. 2.1 where the quantization noise is shaped by an appropriate high-pass filter function. If a 1st-order high-pass filter is used, every doubling of the OSR results in an SQNR improvement of 9 dB [9]. Consequently, the combination of oversampling and noise shaping is more effective compared to oversampling alone. The performance can be further improved by using a higher order filter. It should be noted that noise shaping does not reduce the total noise power in the Nyquist interval. Integrating the noise from 0 to $f_s/2$ would still yield the same power as for oversampling alone. However, the IBN is reduced and more noise is pushed towards higher frequencies. To fully exploit the benefit provided by oversampling and noise shaping, a sharp low-pass digital filter is required after the ADC to filter out the noise outside the band of interest. Furthermore, the sampling rate at the output of the ADC must be reduced to the Nyquist rate by discarding (i.e. decimating) the unnecessary samples. Usually, filtering and decimation are combined into one filter called decimation filter [10].

2.2 ΔΣ MODULATOR TOPOLOGIES

The simplest approach to achieve noise shaping is by placing a high-pass filter after the quantizer. The problem with this approach is that the signal will be filtered as well. This is undesirable since ideally the input signal should remain unaffected. To avoid filtering of the input signal, while still achieving high-pass filtering of the quantization noise, a loop filter can be placed in a feedback loop together with the quantizer. This is the basic architecture of a DSM. The loop filter

can be implemented either in the DT or CT domain and the resulting modulators are referred to as DT respectively CT DSMs. Both types of DSMs are covered in this section.

2.2.1 DISCRETE-TIME ΔΣ MODULATORS

The block diagram of a general DT DSM is shown in Fig. 2.2. It is a feedback configuration consisting of a DT loop filter, a quantizer with arbitrary number of bits and a feedback digital-to-analog converter (DAC). The DAC is required to convert the digital signal after the quantizer to a DT signal that is fed back to the loop filter. The CT signal at the input is sampled, i.e. converted to a DT signal, before entering the loop filter. The forward transfer function $G_{DT}(z)$ and the feedback transfer function $H_{DT}(z)$ are usually realized as a two-input loop filter.

DT LINEAR MODEL

The system in Fig. 2.2 is difficult to analyze mathematically due to the non-linear transfer characteristics of the quantizer. However, an intuitive understanding of its operation can be obtained by replacing the quantizer with its linear model consisting of additive quantization noise N_q and a unity gain block. Furthermore, if the feedback DAC is ideal, it can be omitted since only operation at sampling instants is of interest. The resulting linearised model is shown in Fig. 2.3. By performing linear analysis, it can be shown that the output Y can be written as a linear combination of the input signal X and the quantization noise N_q:

$$Y(z) = STF(z)X(z) + NTF(z)N_q(z) \tag{2.2}$$

where

$$NTF(z) = \frac{1}{1 + H_{DT}(z)} \tag{2.3}$$

is the noise transfer function (NTF), and

$$STF(z) = \frac{G_{DT}(z)}{1 + H_{DT}(z)} = G_{DT}(z)NTF(z) \tag{2.4}$$

is the signal transfer function (STF). From (2.3) it can be concluded that the feedback transfer function $H_{DT}(z)$ must be large in the band of interest to reduce the NTF there and implement high-pass filtering of the quantization noise. According to (2.4), the forward transfer function $G_{DT}(z)$ must also be large in the same range to force the STF to equal unity. Consequently, both $G_{DT}(z)$ and $H_{DT}(z)$ must be low-pass transfer functions.

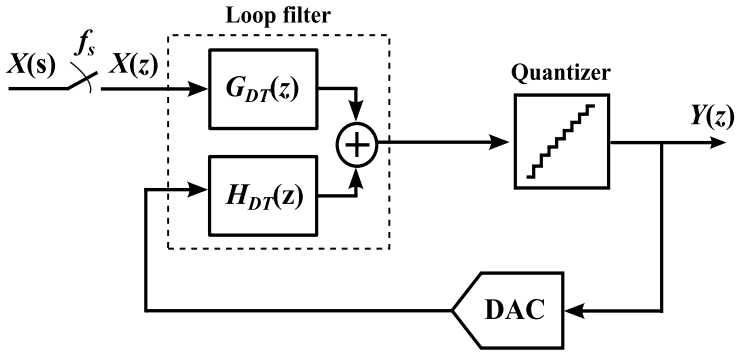

Fig. 2.2: General DT DSM.

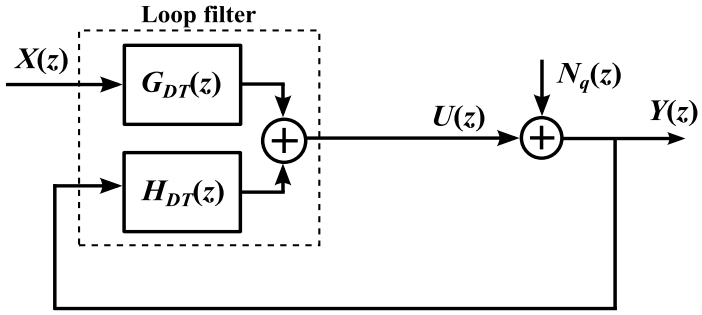

Fig. 2.3: DT linear model.

STABILITY

The DSM in Fig. 2.2 is a non-linear feedback system and hence stability is of great importance. Although the linear model is simple and intuitive, it fails to predict the stability behaviour of DSMs in many cases. This is due to the fact that the gain of the quantizer is signal dependent, an effect that is not captured by the linear model. More sophisticated models that change the quantizer gain in accordance with the input signal do exist [11] [12]. However, to predict stability without any doubt, extensive simulations should always be performed.

The stability requirement also restricts the possible choices of the NTF [13]. This becomes more important for higher order loop filters as less aggressive NTFs are required to guarantee stability. Assuming a loop filter with order L, the simplest NTFs are Lth order differentiators:

$$NTF(z) = (1 - z^{-1})^L \tag{2.5}$$

A high order differentiator yields a more effective noise shaping but it also results in a large out-of-band gain (OBG). For $L > 2$, the large OBGs can lead to

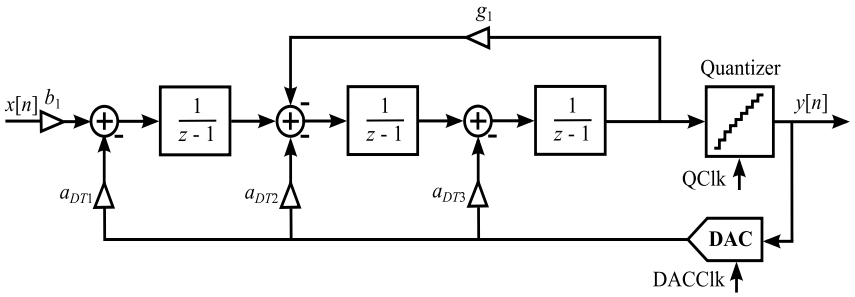

Fig. 2.4: A 3rd-order DT CIFB DSM.

instability, especially if single-bit quantizers are used [13]. To ensure stable operation, the NTFs in (2.5) can be modified by shifting the poles from the origin. The pole locations can then be controlled to reduce the OBG and thereby enable the implementation of high order NTFs. This procedure is implemented in the commonly used Schreier's toolbox in Matlab [14]. The toolbox takes into account the trade-off between OBG and maximal achievable SQNR and optimizes the NTF accordingly. The resulting NTF yields a realistic SQNR that differs significantly from the one predicted by the linear model.

IMPLEMENTATION OF DT LOOP FILTERS

There are many different ways of implementing loop filters for DSMs. The two most common architectures for low pass DSMs are: cascaded integrator feedback (CIFB) and feedforward (CIFF) [15]. The former has been used in [1–4]. As an example, a DSM employing a CIFB loop filter of order 3, which achieves a unity STF in-band, is shown in Fig. 2.4. The feedback coefficients $a_{DT1} - a_{DT3}$ can be obtained from [14] when a suitable NTF has been determined. By introducing the coefficient g_1, zero-optimized NTFs can be achieved which further increases the SQNR.

The DT integrators $I(z) = 1/(z-1)$ are implemented using switched-capacitor (SC) circuits. The summing operations can be realized with summing SC integrators while the coefficients are given by capacitance ratios. The latter is beneficial regarding process variations as capacitor ratios can be implemented accurately in CMOS processes [16].

2.2.2 CONTINUOUS-TIME ΔΣ MODULATORS

The first DSM modulator was actually implemented with a CT loop filter [17]. When SC circuits were introduced, DT DSMs became popular due to their low sensitivity to process variations. However, recently CT DSMs have received increasing attention due to lower power consumption and AA filtering. Furthermore, for low-voltage applications, the resistance of the switches in DT DSMs is

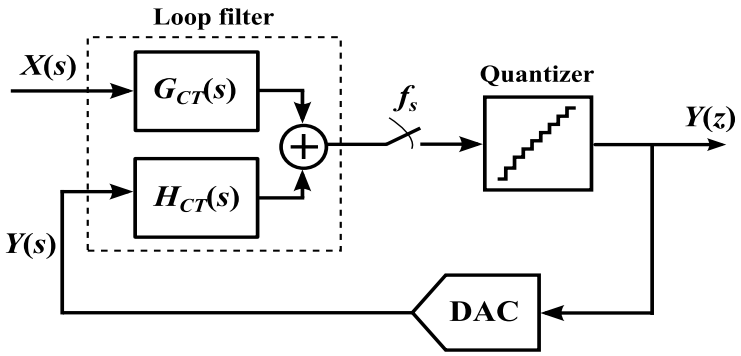

Fig. 2.5: General CT DSM.

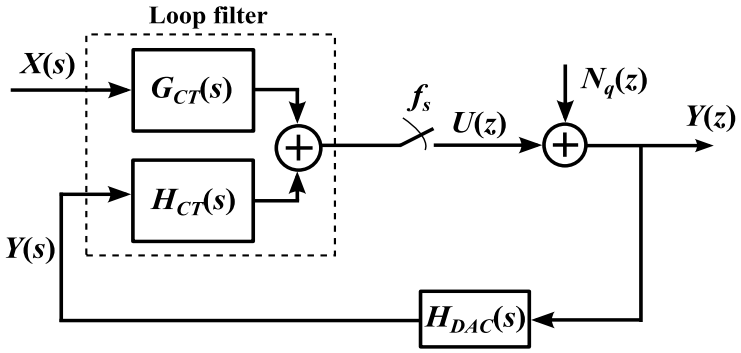

Fig. 2.6: CT linear model.

increased due to the lower overdrive voltage [18]. This issue is avoided in CT DSMs since the loop filter does not require any switches. Several low-voltage (below 1V) CT DSMs have been demonstrated in [19–21].

The block diagram of a general CT DSM is shown in Fig. 2.5. Compared to the DT DSM in Fig. 2.2, the loop filter is CT and the sampling operation is moved inside the loop. In practical implementations, sampling is performed by the quantizer.

CT LINEAR MODEL

If the quantizer is replaced by additive noise and a unity gain block as in 2.2.1, a linear model of the CT DSM in Fig. 2.5 is obtained and shown in Fig. 2.6. An important distinction to the DT linear model is that the the transfer function of the feedback DAC, $H_{DAC}(s)$, needs to be taken into account. This is since the loop filter processes CT signals and the behaviour between sampling instants cannot be ignored. However, the transfer function from output Y to the input of the

quantizer U is still DT, due to the sampling operation inside the loop.

The processing of the input signal also requires special attention since the definition of the STF for a CT DSM is not as straight forward as for the DT DSM. From Fig. 2.6 it is obvious that the CT input signal is pre-filtered by the forward transfer function $G_{CT}(s)$ before it is sampled. This action improves the AA filtering present in CT DSMs. The shorthand expression for the signal after filtering and sampling is $[G_{CT}(s)X(s)]^*$ where * is the star operator [22] and refers to the periodic spectrum repetition after sampling. Since the input signal is in the CT domain and the output signal is in the DT-domain, it is not possible to define a DT STF [23]. However, it is possible to define a CT STF. After direct analysis of the block diagram in Fig. 2.6, it can be shown that the output signal can be written as

$$\begin{aligned} Y(z) &= NTF(z)[G_{CT}(s)X(s)]^* + NTF(z)N_q(z) \\ &= [G_{CT}(s)NTF(e^{sT_s})X(s)]^* + NTF(z)N_q(z) \end{aligned} \tag{2.6}$$

where $NTF(z)$ is the same as for the DT DSM and is given by (2.3) and $z = e^{sT_s}$ with a sampling period of T_s. The input signal is multiplied by $G_{CT}(s)NTF(e^{sT_s})$ before the star operator is applied and therefore the CT STF is defined as

$$STF(s) = G_{CT}(s)NTF(e^{sT_s}). \tag{2.7}$$

Just as for DT DSMs, the STF depends on the NTF. This effect further improves the AA filtering in CT DSMs.

DISCRETE TO CONTINUOUS TIME CONVERSION

The design of CT DSMs usually starts by transforming a DT system to its CT equivalent. This approach is preferred since the theory of optimizing a desired DT loop filter to meet certain specifications is well established. Furthermore, there is software available for efficient design and fast simulation of DT systems [14].

The equivalence between CT and DT DSMs is achieved by using the impulse invariant transformation [9] [23]. This method is based on the observation that the transfer function from the output to the input of the quantizer in both DT and CT DSMs is in the DT domain, compare Fig. 2.3 and Fig. 2.6. Then by simply equating the impulse responses from the output to the input of the quantizer, as shown in Fig. 2.7, the equivalence is achieved. In other words, the following equation is solved:

$$\mathcal{Z}^{-1}\{H_{DT}(z)\} = \mathcal{L}^{-1}\{H_{CT}(s)H_{DAC}(s)\}|_{t=nT_s}. \tag{2.8}$$

For simple DAC feedback pulses, $H_{DAC}(s)$, (2.8) can be solved analytically [23–25]. More complicated pulses can be handled by using numerical methods [26] [27].

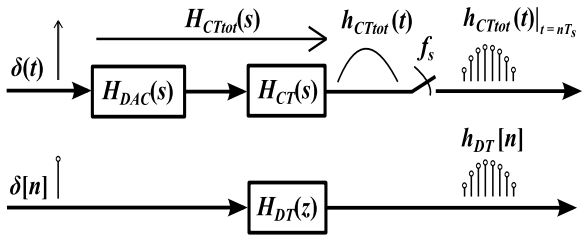

Fig. 2.7: Impulse invariant transformation.

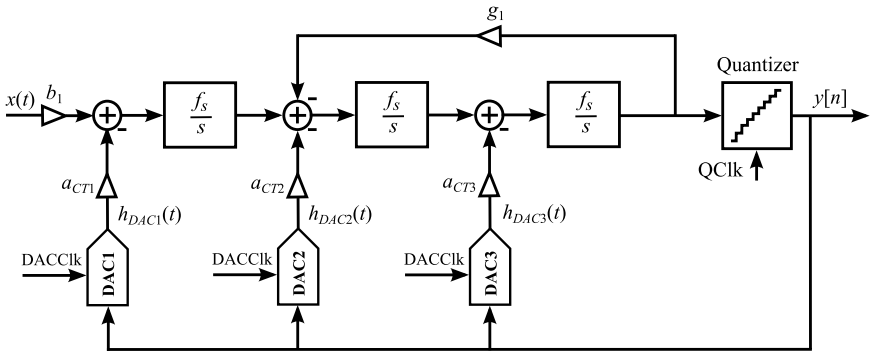

Fig. 2.8: A 3rd-order CT CIFB DSM.

IMPLEMENTATION OF CT LOOP FILTERS

Fig. 2.8 shows a DSM employing a CT version of the CIFB loop filter in Fig. 2.4. The basic architecture is the same as for the DT loop filter. However, the integrators are of CT type with the transfer function $I(s) = f_s/s$. In practice, active-RC and/or gmC-integrators can be used to realize $I(s)$ and the loop filter coefficients. Starting with a DT loop filter with DT feedback coefficients $a_{DT1} - a_{DT3}$, the CT feedback coefficients $a_{CT1} - a_{CT3}$ can be obtained by solving (2.8) for DAC pulses $h_{DAC1}(t) - h_{DAC3}(t)$.

2.3 DAC FEEDBACK PULSES

Theoretically, there is an endless number of possible DAC pulses that can be used in CT DSMs. The choice is usually restricted by practical considerations such as ease of implementation and timing errors which include clock jitter and loop delay. The effect of timing errors in CT DSMs will be discussed in the chapter 3.

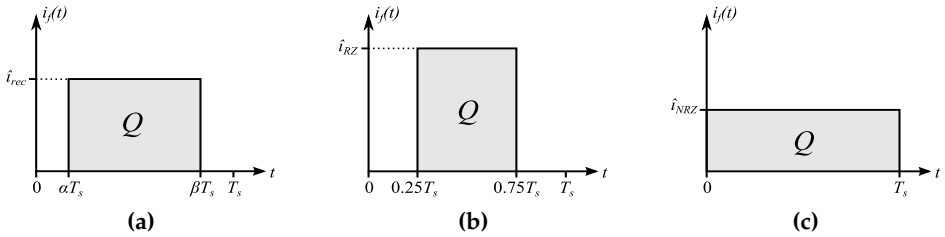

Figure 2.9: Rectangular DAC pulses. (a) General rectangular pulse, (b) RZ-pulse with duty cycle of 0.5, (c) NRZ-pulse.

2.3.1 RECTANGULAR PULSES

The most commonly used feedback pulses are rectangular pulses [24] [28]. These pulses are simple to generate by switching either current or voltage sources with control signals derived from the main clock. A general rectangular pulse of the DAC at the input of the corresponding integrator is shown in Fig. 2.9a where $\hat{i}_{rec}$ is the DAC peak current and Q is the amount of charge transferred during one sampling period. The pulse is contained within one sampling period T_s. The transfer function of a DAC generating rectangular pulses is found by taking the Laplace transform of the pulse in Fig. 2.9a

$$H_{rec}(s) = \hat{i}_{rec}\frac{e^{-\alpha T_s s} - e^{-\beta T_s s}}{s}. \tag{2.9}$$

This transfer function can be used in (2.8) to analytically obtain the feedback coefficients for general rectangular feedback pulses.

RETURN-TO-ZERO FEEDBACK

If $\beta - \alpha < 1$ for the pulse in Fig. 2.9a, the feedback is referred to as return-to-zero (RZ) as the DAC current returns to zero at βT_s. It is common to use RZ pulses with $\beta - \alpha = 0.5$, as shown in Fig. 2.9b, since this results in a duty cycle of 0.5 which is easy to implement. In chapter 3, it will become clear that RZ feedback is most sensitive to clock jitter and can be critical if used in the outermost DAC in a DSM. However, it can be used in the subsequent DACs with benefit to avoid additional circuit complexity due to loop delay compensation.

NONRETURN-TO-ZERO FEEDBACK

Another special case of the rectangular pulses, shown in Fig. 2.9c, is obtained if $\alpha = 0$ and $\beta = 1$. The DAC current is high during the entire sampling period and therefore the feedback is referred to as nonreturn-to-zero (NRZ). For two equivalent DSMs employing NRZ and RZ feedback, respectively in the first feedback

branch, the peak current for the NRZ modulator is reduced by half compared to the RZ modulator. The reason is that the transferred charge Q for two equivalent modulators is the same and the current must be doubled for RZ feedback to transfer the same charge during $T_s/2$. This translates into a larger CT feedback coefficient for the RZ modulator i.e. $a_{CT1,RZ} = 2a_{CT1,NRZ}$.

The reduced peak current of the NRZ pulses is beneficial since it relaxes the integrator amplifier slew-rate requirements. As will become clear in chapter 3, NRZ feedback is less sensitive to clock jitter than RZ feedback. However, excess loop delay prevents the use of NRZ feedback in all DACs as the delay can easily shift the NRZ pulses into the next sampling period which in turn can lead to an unstable DSM.

2.3.2 EXPONENTIAL PULSES

In the recent decade, there have been several works that have used shaped feedback pulses to further reduce the jitter sensitivity of CT DSMs. The most widely used shaped feedback pulses are exponentially decaying pulses [2] [25] [26] [29] [30] since they are fairly easy to generate. In its most simplest form, exponential decay can be achieved by letting a capacitor discharge through a resistor.

SWITCHED-CAPACITOR-RESISTOR FEEDBACK

Switched-capacitor-resistor (SCR) feedback, shown in Fig. 2.10a together with the circuit implementation, was first introduced in [29]. The basic idea is to charge a capacitor C during the first half of the sampling period and discharge it through a resistor R during the second half of the sampling period. The jitter sensitivity is determined by the time constant $\tau = RC$. Compared to rectangular pulses for the same charge transferred during one sampling period, the peak current of exponential pulses is larger since more charge is transferred in the beginning. This requires again a larger feedback coefficient than for an equivalent NRZ or RZ feedback path. The peak current required to transfer a charge Q using SCR feedback is also dependent on τ.

SWITCHED-CAPACITOR VARIABLE-RESISTOR FEEDBACK

One method of reducing the peak current while still maintaining a low jitter sensitivity was presented in [26]. The feedback pulse and the circuit implementation are shown in Fig. 2.10b. Since the capacitor is discharged through a variable resistor, the technique is called switched-capacitor variable-resistor (SCVR) feedback. The capacitor is first charged for $0 < t < \alpha T_s$ and then discharged through the variable resistor for $\alpha T_s < t < \kappa T_s$. The resistance must vary in a linear fashion to keep the current constant during discharge. Finally, for $\kappa T_s < t < \beta T_s$, the resistance is held constant and the current decreases exponentially. In this way a

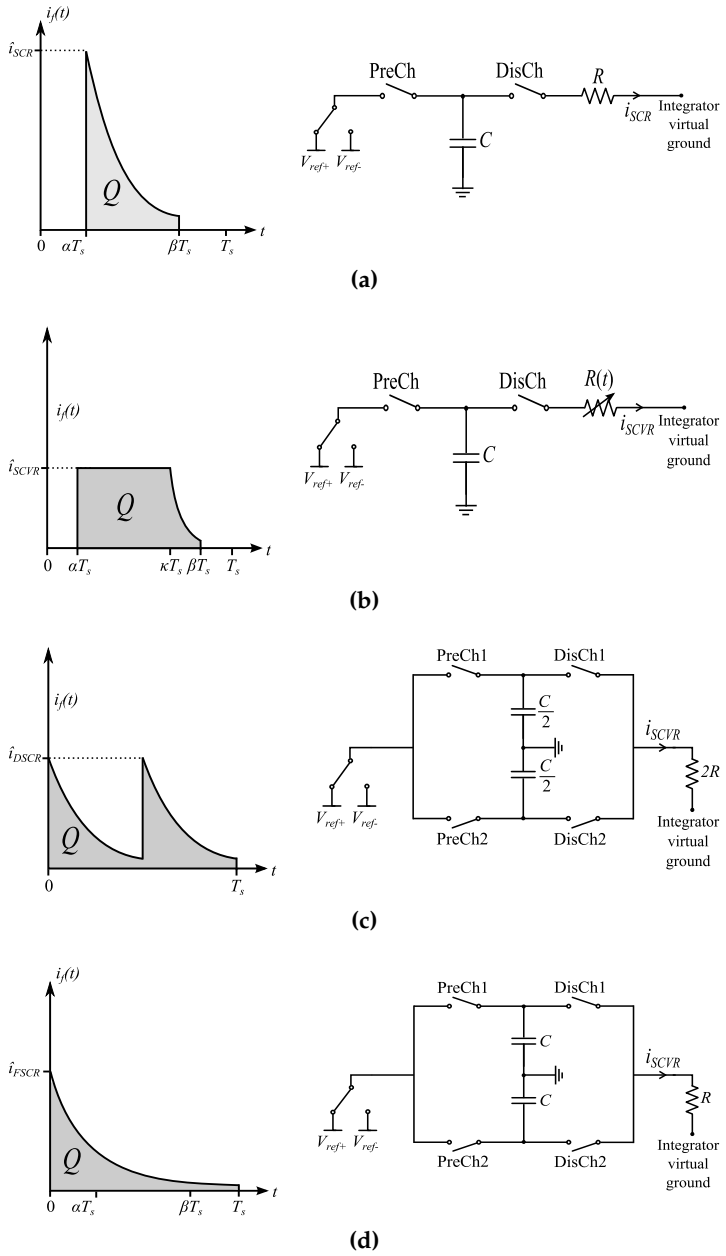

Figure 2.10: Exponential pulses and circuit implementations. (a) SCR pulse, (b) SCVR pulse, (c) DSCR pulse, (d) FSCR pulse.

combination of an RZ and SCR pulses is created with a reduced peak current and low jitter sensitivity.

Implementation of a continuously varying resistance is not trivial and can only be approximated by switching in several resistors in discrete steps. The feedback is then called switched-capacitor switched-resistor (SCSR) feedback. Although SCSR feedback manages to lower the peak current, the circuit complexity increases significantly compared to SCR feedback.

DUAL SWITCHED-CAPACITOR-RESISTOR FEEDBACK

Another technique with intention of reducing the peak current of exponential feedback pulses was presented in [1] [2]. The main idea is to divide the exponential pulse into two identical units. This is shown in Fig. 2.10c together with the circuit implementation. The feedback is referred to as dual switched-capacitor-resistor (DSCR) feedback. The operation is based on two capacitors that are alternately charged and discharged through a common resistor. Each discharge process lasts for $T_s/2$. Compared to SCR feedback, for the same time constant $\tau = RC$ and charge Q, each capacitor must be $C/2$ as it stores a charge of $Q/2$. In order to keep the same time constant, the resistor of the DSCR implementation must be doubled which reduces the peak current by half. Furthermore, compared to SCSR feedback, the circuit implementation is simple as there is no need to implement a varying resistance.

FULL CLOCK PERIOD SWITCHED-CAPACITOR-RESISTOR FEEDBACK

During the course of this work, another SCR-technique has been presented in [30]. The feedback pulses together with the corresponding circuit implementation are shown in Fig. 2.10d. The technique is called full clock period switched-capacitor-resistor (FSCR) feedback because the charge is transferred during the entire clock period. This leads to both reduced peak current and improved immunity to clock jitter compared to SCR feedback. Similar to DSCR feedback, the operation is based on two capacitors that are alternately charged and discharged through a common resistor. The difference is that each of these processes lasts during the entire clock period.

2.3.3 AMPLITUDE EFFICIENCY

In 2.3.2, it became clear that exponential feedback pulses require larger peak currents than their rectangular counterparts. This also results in larger feedback coefficients compared to rectangular feedback. To more easily compare the different feedback pulses in terms of peak current, the amplitude efficiency η_a was defined in [26]. It is given as $\eta_a = a_{CT1,RZ}/a_{CT1,exp}$ where $a_{CT1,RZ}$ is the CT feedback coefficient of an RZ DAC in the first feedback branch with $\alpha = 0.5$ and $\beta = 1$

and $a_{CT1,exp}$ is the CT feedback coefficient of an exponential DAC in the first feedback branch. Thus, a high peak current translates into a low amplitude efficiency. For NRZ feedback, which has the lowest peak current and feedback coefficient, $\eta_a = 2$ and it is the highest amplitude efficiency that can be achieved. For all the exponential pulses covered in 2.3.2, the expression for η_a can be generalized as

$$\eta_a = 2R\left(\gamma + \tau_n\left(1 - e^{-\frac{\beta-\kappa}{\tau_n}}\right)\right) \tag{2.10}$$

where R is the repetition factor ($R = 2$ for DSCR feedback and $R = 1$ for the other feedbacks), γ is the normalized length of the constant current phase for SCVR feedback, $\tau_n = \tau/T_s$ is the normalized time constant, κ is the normalized time instant which indicates when exponential decay begins and β is the normalized time instant which indicates when exponential decay ends. This expression is used later in chapter 3 for comparison of different pulses.

3

DAC non-idealities in CT ΔΣ modulators

This chapter discusses the impact of feedback DAC non-idealities on the performance of CT DSMs. Since the DAC waveforms in a CT DSM are integrated over time, any errors perturbing these waveforms will affect the integrated output. There are mainly two types of DAC errors: timing errors, which include loop delay and clock jitter, and mismatch errors which affect the DAC levels and are critical when multi-bit DACs are used.

3.1 EXCESS LOOP DELAY

Considering again the CT DSM in Fig. 2.8. Ideally the DACs should react immediately after the quantizer clock edge. However, in practical implementations, the finite transistor switching times causes a delay between the quantizer clock and the DAC waveforms. This delay is called excess loop delay or just loop delay. The effect of loop delay on DAC pulses is shown in Fig. 3.1 for RZ and NRZ feedback. Both pulses are shifted by $t_d < T_s$ compared to the ideal pulse positions. The RZ pulse stays inside the sampling period and is integrated between 0 and T_s without any error. The NRZ pulse, on the other hand, is shifted into the next sampling period and the part after T_s is missed by the integrator resulting in an error. Obviously, a large loop delay is required to push the RZ pulses into the next sampling period which makes the RZ feedback less sensitive to loop delay compared to NRZ feedback.

The detrimental effect of loop delay on the performance of CT DSMs has been studied in [24] [28] [31]. It can be shown that loop delay results in coefficient mismatch which affects the NTF and increases the quantization noise. Furthermore, if the pulse is pushed into the next sampling period, the order of the modulator increases eventually leading to instability. It is also of importance to understand which of the feedback paths in a CT DSM is most sensitive to loop delay. In [32], it was shown that the first feedback path is the least sensitive to loop delay while

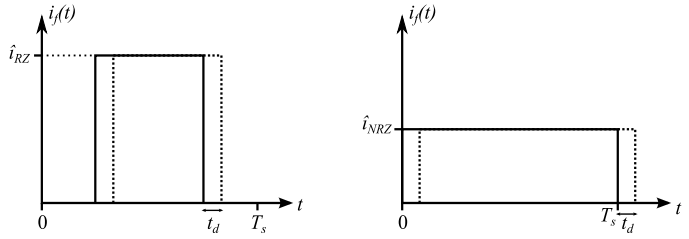

Fig. 3.1: RZ and NRZ pulses affected by loop delay.

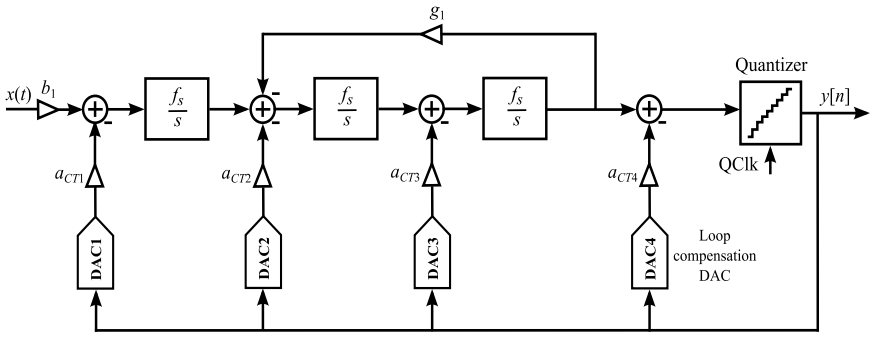

Fig. 3.2: Addition of an extra feedback path for loop delay compensation.

the following feedback paths are successively more sensitive. The last feedback path is, however, most critical which must be considered during design.

3.1.1 LOOP DELAY COMPENSATION

In practical implementations, a certain amount of loop delay is required to ensure proper operation. There are two main reasons for this: First the DACs should be updated only after the quantizer has finished the conversion of the current sample, hence, there must be a delay between the quantizer and the DACs. Second, loop delay is not well controlled as it is both dependent on signal and process variations. By introducing a deliberate loop delay, which is significantly larger than the worst case delay, all the variations can be incorporated. Unfortunately, the introduced loop delay can shift the DAC pulses into the next sampling period, especially if NRZ feedback is used, increasing the order of the modulator from L to $L+1$. Since there are still only L feedback coefficients, it is intuitive to add an additional coefficient to restore full controllability of the system [31] [33] [34]. This method is shown in Fig. 3.2 where a fourth feedback path has been added around the quantizer. By readjusting the rest of the coefficients, loop delays up to one sampling period can be compensated by this method and full performance

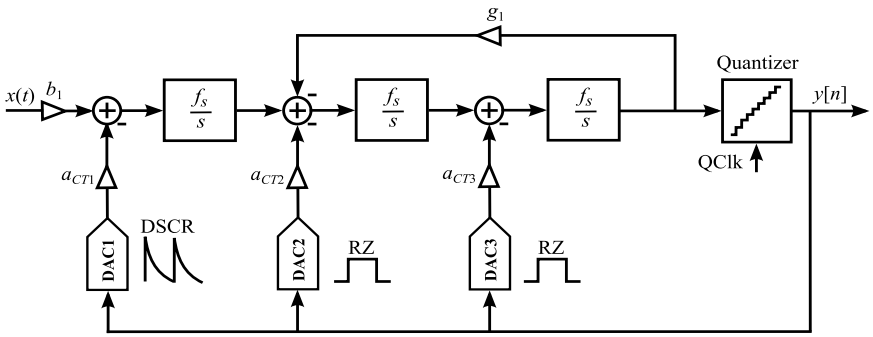

Fig. 3.3: Loop delay insensitive DSM architecture.

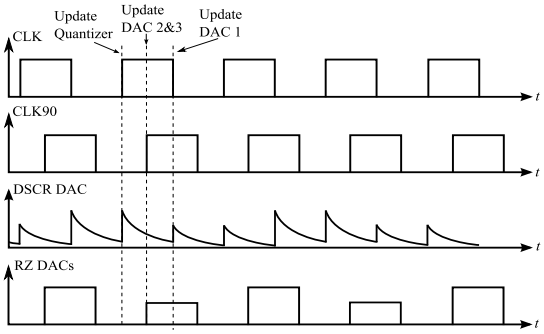

Fig. 3.4: Timing diagram of the loop delay insensitive DSM.

restored. The disadvantage is that an additional DAC and a summing operation is required where the latter is more critical as it is usually implemented using a summing amplifier. In [35], two other promising compensation techniques that address the above issues have been reviewed with some disadvantages regarding the integrator gain bandwidth (GBW) requirements and STF peaking.

3.1.2 LOOP DELAY AND RZ FEEDBACK

In Fig. 3.1, it was shown that RZ feedback is less sensitive to loop delay than NRZ feedback. The RZ pulse was centred in the middle of the sampling period which has two advantages: There is a $T_s/4$ delay between the quantizer and the DAC which ensures proper operation; There is a $T_s/4$ delay margin until the next sampling period. The above advantages suggest the use of RZ pulses in later feedback paths which are most sensitive to loop delay [32]. This has been adopted in [1][2], as shown in Fig. 3.3, where RZ pulses are used in the two last feedback paths while the first feedback path employs DSCR pulses to reduce the sensitivity to clock jitter. The overall timing diagram of the DSM is shown in Fig. 3.4. All

DACs are updated well after the beginning of the clock period which ensures that the quantizer has processed the samples before they are converted to analog form. The extension of the DSCR pulses into the next clock period is not an issue since the first feedback path is highly insensitive to loop delay.

The advantage of RZ feedback is that no additional circuit complexity is required to reduce the sensitivity to loop delay. However, the loop delays in high frequency applications can occupy significant portions of the sampling period and shift even RZ pulses into the next sampling period. In this case, the compensation techniques in 3.1.1 cannot be avoided.

3.2 CLOCK JITTER

Clock jitter is caused by statistical variations of the clock edges and depends on the purity of the clock source. There are mainly two types of jitter: Independent (white) jitter and the more realistic accumulated jitter [36] [37]. If a clock waveform is affected by independent jitter, the sampling instants are given as

$$t_n = nT_s + t_{jn}, \quad n = 0, 1, 2, ..., N-1 \tag{3.1}$$

where t_{jn} are independent and identically distributed variables (IID) which represent the random variations from the ideal sampling instants, and N is the length of the sequence t_n. In practical implementations, the clock reference is generated in a phase-locked loop (PLL) and the jittered sampling instants due to phase noise can be approximated by

$$t_n = nT_s + \sum_{i=0}^{n} t_{ji}, \quad n = 0, 1, 2, ..., N-1. \tag{3.2}$$

Although t_{ji} are still IID, the actual timing deviations from ideal sampling instant are accumulated due to the summation and depend on previous values.

3.2.1 JITTER ERROR SOURCES IN ΔΣ MODULATORS

Fig 3.5 shows block diagrams of general DT and CT DSMs. The most critical errors resulting from clock jitter are generated either at the input or in the feedback DAC. These errors are as follows:

1. Sampling jitter errors: A jittered clock will cause the CT signal at the input of the DT DSM to be sampled at wrong time instants. This results in amplitude errors that are injected directly at the input. Sampling jitter errors also affect the CT DSM before the quantizer. However, all errors at this point are suppressed by the NTF and can usually be neglected.

2. DAC jitter errors: Any timing variations affecting the clock that controls the DAC will modify the starting and ending points of the feedback pulses.

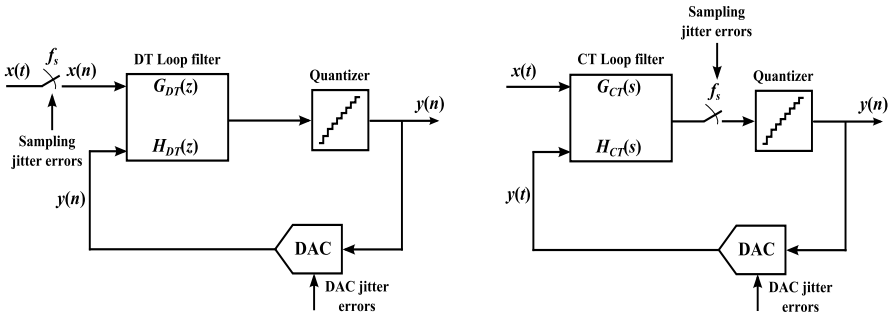

Fig. 3.5: Jitter error sources in DT and CT DSMs.

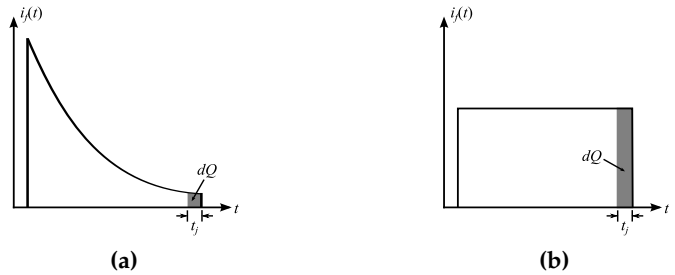

Figure 3.6: DAC pulses under jitter influence. (a) Jittered DT DAC pulse, (b) Jittered CT DAC pulse.

A typical feedback pulse in a DT DSM affected by clock jitter is shown in Fig. 3.6a. The shape is exponential since the capacitors in SC circuits are discharged through switches with finite on-resistances. Most of the charge is transferred during the beginning of the sampling period and therefore the charge lost due to an error is small. This is not the case for CT DSMs as shown in Fig.3.6b for the commonly used rectangular pulses. More charge is lost due to the rectangular shape which results in high sensitivity to clock jitter.

The sampling jitter errors at the input only affect the signal while the DAC jitter errors affect the sum of the signal and the quantization noise. Since the latter contains a significantly larger power, CT DSMs are more sensitive to clock jitter than DT DSMs.

PROPAGATION OF DAC JITTER ERRORS

To understand the effect of DAC jitter errors in more detail, the 3rd order CT DSM in Fig. 3.7 is considered. It has been shown in several publications that jitter

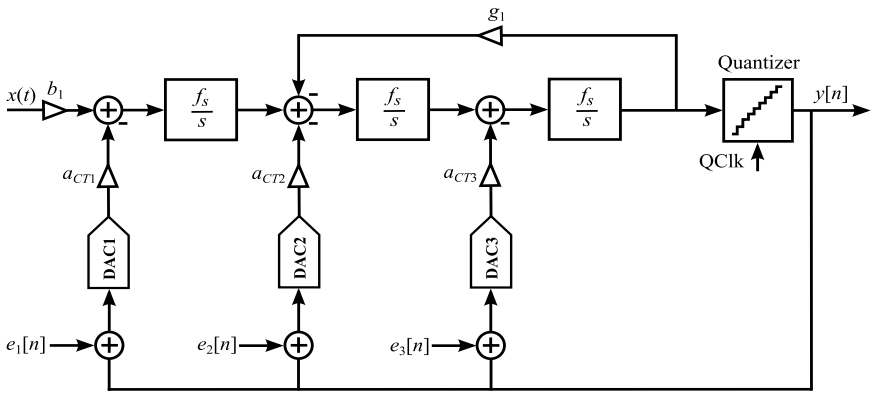

Fig. 3.7: Modeling clock jitter as additive amplitude errors.

in the feedback DAC can be modelled as an additive amplitude error sequence that produces the same charge error as the timing variations due to clock jitter [38–40]. This is the purpose of the error sequences $e_1[n] - e_3[n]$ in Fig. 3.7. The effect of these errors can be studied by referring them back to the input and then multiplying by the STF which is ideally unity in band. The following conclusions can be reached from this approach:

1. The DAC errors $e_2[n]$ and $e_3[n]$ are at least 1st-order noise shaped when referred back to the input since they are preceded by at least one integrator.

2. The error $e_1[n]$, on the other hand, is unaffected and directly injected at the input. Due to this reason, the first DAC is most critical and measures have to be taken to keep its errors from significantly affecting the performance.

These conclusions can be generalized for a loop filter of order L.

PULSE-WIDTH AND PULSE-POSITION ERRORS

There are two possible pulse errors that result from DAC jitter errors: pulse-width (PW) and pulse-position (PP) errors. These are shown in Fig. 3.8 for an arbitrary rectangular pulse. The timing error due to clock jitter t_j affects the pulse edges but it also changes the pulse-width and shifts the center of the pulse. The effect of PW and PP errors on the performance of CT DSMs has been modelled in [41] [42] and can be explained with the help of the conclusions above and Fig. 3.7. PW errors from the first DAC are most critical as they are directly injected at the output without any suppression. PW errors from the rest of the DACs are not as problematic since they are at least first order noise shaped. The performance is not affected by PP errors in the first DAC since only the position of the pulse is changed and not the pulse-width. Since the integral of the pulse is not dependent

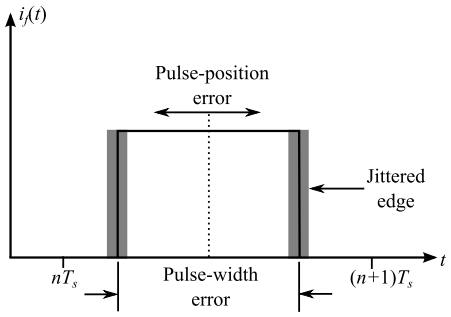

Fig. 3.8: Pulse-width and pulse-position errors.

on the position, the impulse response remains the same. However, it can be shown that PP errors from the rest of the DACs affect both the impulse response and the remaining feedback coefficients [24] [42]. Fortunately these errors are at least first order noise shaped.

In conclusion, PW errors from the first DAC are most dominant but the errors from the other DACs should be included when modelling clock jitter since they cannot always be neglected [26].

3.2.2 JITTER SENSITIVITY OF RECTANGULAR PULSES

The charge errors $e_q[n]$ due to clock jitter affecting the RZ and NRZ pulses are shown in Fig. 3.9 for single-bit feedback. The peak values of the DAC outputs are determined by the feedback coefficient $a_{CT,RZ}$ or $a_{CT,NRZ}$ and the quantization step Δ which equals the DAC reference voltage in this case. It is obvious that the charge errors due to clock jitter are generated only during the transitions of the DAC output signal. The NRZ DAC output always transitions between $a_{CT,NRZ}\Delta$ and $-a_{CT,NRZ}\Delta$ while the RZ DAC output only transitions between $\pm a_{CT,RZ}\Delta$ and 0. However, as discussed in 2.3.1, $a_{CT,RZ} = 2a_{CT,NRZ}$, assuming a duty cycle of 0.5, and therefore the height of the transitions is the same in both cases. Consequently, the charge error affecting one edge of both the RZ and NRZ pulses is also the same and is given by:

$$dQ = 2a_{CT,NRZ}\Delta t_j. \tag{3.3}$$

The difference between NRZ and RZ is the number of transitions. The RZ DAC is forced to always transition two times during every clock period even when the input data does not change. Obviously, this increases the power of the charge error compared to the NRZ DAC which transitions only when the input data changes. Due to this reason, RZ feedback is more sensitive to clock jitter than NRZ feedback.

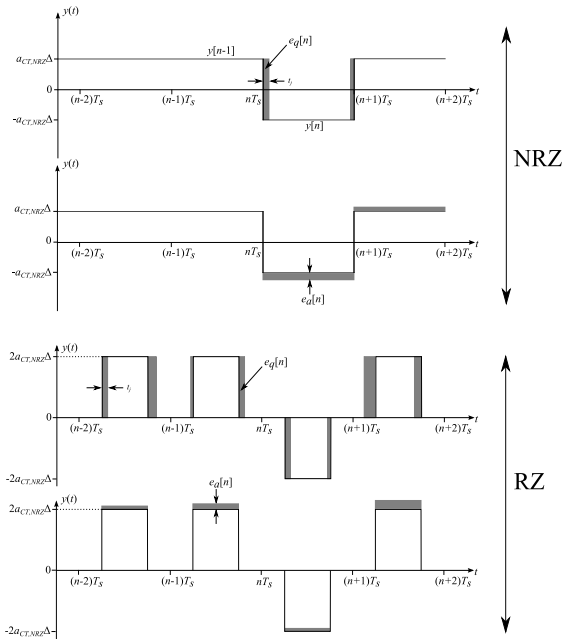

Fig. 3.9: NRZ and RZ pulses affected by clock jitter.

3.2.3 EFFECT ON THE PERFORMANCE

The equivalent additive amplitude errors $e_a[n]$ of the charge errors $e_q[n]$ are also shown in Fig. 3.9. These are obtained by normalizing $e_q[n]$ with the sampling time T_s which yields for NRZ [36] [39] [43]

$$e_a[n] = (y[n] - y[n-1])\frac{t_j}{T_s}. \tag{3.4}$$

It is obvious from (3.4) that the jitter timing error t_j interacts with the output $y[n]$ which contains both the signal and the quantization noise. The multiplication between t_j and the signal transition $dy[n] = y[n] - y[n-1]$ translates into convolution in the frequency domain. This implies that clock jitter modulates with both the signal and the quantization noise [40] [44]. Assuming that the clock is affected by accumulated jitter given by (3.2), the impact on the spectrum of a CT DSM is shown in Fig. 3.10. The error $e_a[n]$ consists of two main components:

1. The side-bands around the signal which are caused by modulation between jitter close to the sampling frequency and the signal. A similar effect can be observed in DT DSMs if the sampler at the input is affected by accumulated clock jitter [37] [44].

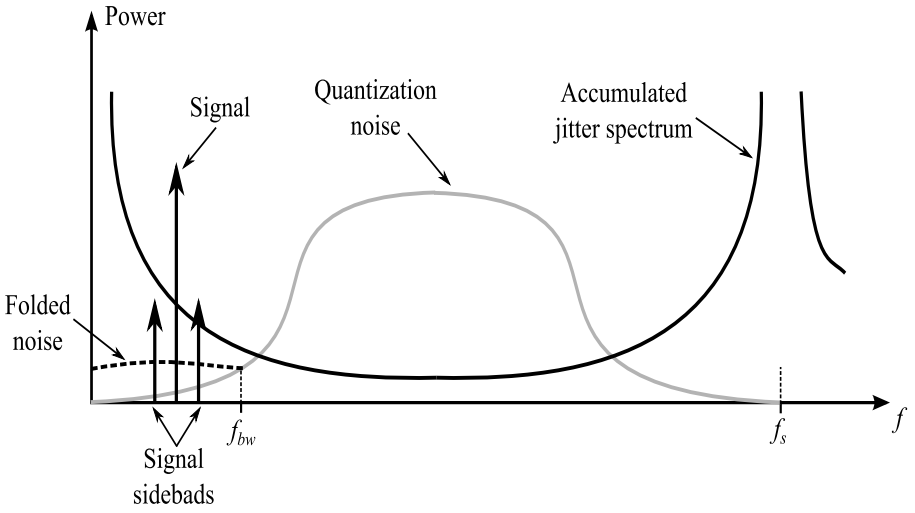

Fig. 3.10: Effect of clock jitter in the frequency domain.

2. White noise which is a result of the modulation between wideband jitter and the quantization noise. Since the noise at high frequencies is folded down, it fills the signal band and degrades the SNR.

It has been shown in [41] that the sidebands are caused by PP errors while the white noise is caused by PW errors.

In many publications, the independent or white jitter modelled by (3.1) is also used to study the impact on the performance. The reason is that the white noise component resulting from the modulation between wideband jitter and quantization noise accounts for the increased sensitivity to clock jitter in CT DSMs. Therefore the white jitter model can be used to obtain a measure of jitter sensitivity and also results in simple expressions. It can be shown that the IBN resulting from the white jitter affecting the first DAC in a CT DSM employing single-bit rectangular pulses is given by [24]

$$IBN_{j,rec} = \frac{A_f}{OSR}\left(\frac{a_{CT1,NRZ}}{b_1}\frac{\Delta\sigma_j}{T_s}\right)^2 \tag{3.5}$$

where $a_{CT1,NRZ}$ and b_1 are the first NRZ-feedback coefficient and forward coefficient (see Fig. 3.7), σ_j is the standard deviation of the white jitter and A_f is the activity factor which models the number of transitions for every clock cycle. It is obvious that for RZ pulses, $A_{f,RZ} = 2$ since there are always two transitions every clock cycle. For NRZ pulses, $A_{f,NRZ} < 1$ since a transition does not necessarily occur every clock cycle. In [28] it was found that $A_{f,NRZ} \approx 0.7$ for single-bit NRZ feedback and a large input signal.

To easily compare the different feedback pulses, the jitter suppression efficiency η_j was defined in [26] as a measure of how efficiently the white jitter is suppressed in an arbitrary DAC compared to a RZ DAC. Using (3.5) to calculate the IBN due to jitter for RZ and NRZ pulses, the jitter suppression efficiency of NRZ feedback is found as

$$\eta_j = 10\log_{10}\frac{IBN_{j,NRZ}}{IBN_{j,RZ}} = 10\log_{10}\frac{A_{f,NRZ}}{A_{f,RZ}} \approx -4.6\text{dB}. \tag{3.6}$$

Consequently, NRZ feedback shows somewhat better jitter performance and is usually preferred in the first DAC.

3.2.4 REDUCING THE EFFECT OF CLOCK JITTER

This section presents several existing methods that reduce the effect of clock jitter in CT DSMs.

MULTI-BIT FEEDBACK

The simplest way to improve the jitter performance in CT DSMs is to use multi-bit feedback. Jittered NRZ and RZ multi-bit waveforms are shown in Fig. 3.11. The NRZ waveform transitions only by one least significant bit (LSB) at most which reduces the charge errors compared to the single-bit case. This benefit is further enhanced for increased number of bits where every bit yields approximately 6 dB of jitter suppression [45]. The RZ pulses also benefit from multi-bit feedback but less than NRZ pulses. This is since the transitions are signal dependent and are usually larger than 1 LSB.

The problem with multi-bit feedback is the degraded linearity of the DACs due to mismatch. This has to be addressed in a practical implementation and will be discussed later in this chapter.

MODIFICATION OF THE NTF

In 3.2.3 it was discussed that modulation between the jitter and the quantization noise increases the IBN. Since the NTF shapes the quantization noise, the IBN due to jitter depends on the NTF. Thus a CT DSM can be made less sensitive to jitter by designing an appropriate NTF. This was examined in [39] and the analysis was further extended in [43]. The IBN due to jitter is primarily determined by the behaviour of the NTF outside the signal band since the NTF is small within the signal band. For the commonly used maximally flat NTFs, the OBG is used to fully characterize the out of band behaviour. Although an increased OBG would reduce the in-band quantization noise, the opposite is true for the out of band quantization noise which modulates with the jitter and degrades the IBN. This suggests that there is a trade-off between the in-band quantization noise and jitter and an optimum OBG exists that results in an NTF with least jitter sensitivity.

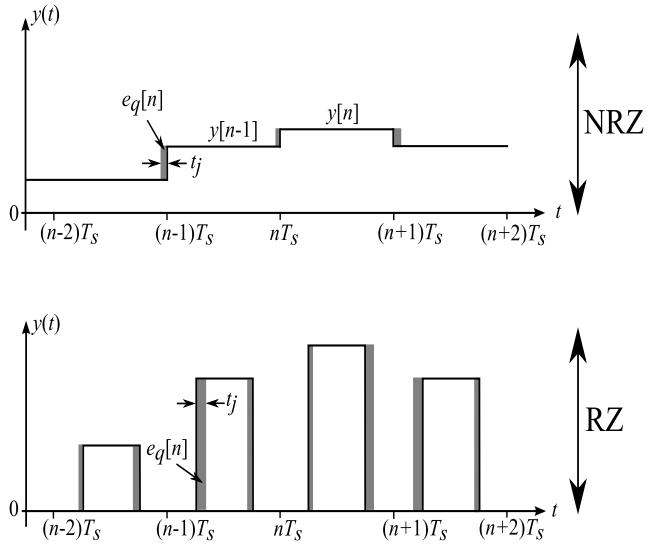

Fig. 3.11: NRZ and RZ multi-bit pulses affected by clock jitter.

Another option is to use other NTFs than the maximally flat. These can be designed with the same in-band behaviour as the maximally-flat NTFs but different out of band behaviour which can improve the jitter sensitivity.

EXPONENTIALY DECAYING FEEDBACK PULSES

The idea behind exponential feedback in CT DSMs is to mimic the exponential discharge that takes place in DT DSMs as shown earlier in Fig. 3.6a. The charge errors due to clock jitter are significantly reduced by the shape of the pulse which accounts for the low jitter sensitivity of DT DSMs. By using the technique in at least the first DAC in CT DSMs, the white PW jitter is suppressed and the same jitter performance as in DT DSMs can be achieved [37]. Thus if the DACs are affected by accumulated jitter, the suppression of the usually dominating white jitter component would reveal the noise skirts due to PP jitter which resembles the sampling jitter in DT DSMs.

CT DSMs employing exponential pulses also inherit the high amplifier slew-rate requirements present in DT DSMs due to large peak currents. This was discussed in 2.3.2 and the amplitude efficiency was introduced for easier comparison between different feedback pulses.

In Fig. 3.12, all the exponential pulses covered in 2.3.2 are compared for the same τ and transferred charge Q in terms of peak current and jitter sensitivity. It can be noted here that $\kappa = 0.5$ for SCR and SCVR and $\kappa = 0$ for FSCR and DSCR. Furthermore, $\alpha = 0.25$ for SCVR and $\beta = 0.5$ for DSCR. By looking at the charge

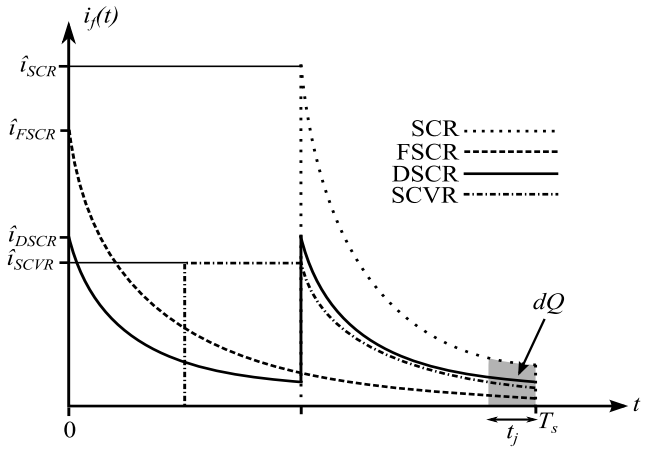

Fig. 3.12: Comparison of all exponential pulses.

errors, it is obvious that the FSCR pulse is least sensitive to clock jitter. However, the peak current is still larger than for the DSCR pulse. By decreasing τ, the jitter suppression of all pulses is improved further since even more charge is transferred during the beginning of the clock period. However, this also results in increased peak current which suggests that there is a trade-off between jitter sensitivity and peak current.

Using the same method as in [24], a generalized expression of the IBN due to white clock jitter for all the exponential DACs can be found as

$$IBN_{j,exp} = \frac{A_{f,exp}}{OSR}\left(\frac{a_{CT1,exp}}{b_1}\frac{\Delta\sigma_j}{T_s}e^{-\frac{\beta-\kappa}{\tau_n}}\right) \tag{3.7}$$

where $A_{f,exp} = 2$ for all the exponential DACs and $a_{CT1,exp}$ is the first feedback coefficient of the exponential DAC. Compared to the expression in (3.5) for rectangular pulses, the exponential factor is present which accounts for the attenuation of clock jitter. Similar to the calculation in (3.6), the jitter suppression for all the exponential DACs can be found as

$$\eta_j = 10\log_{10}\frac{IBN_{j,exp}}{IBN_{j,RZ}} = 10\log_{10}\left(\frac{e^{-\frac{\beta-\kappa}{\tau_n}}}{2\eta_a}\right)^2 \tag{3.8}$$

where the amplitude efficiency η_a was given by (2.10). The amplitude efficiency and jitter suppression efficiency for the pulses in Fig. 3.12 are plotted in Fig. 3.13 and Fig. 3.14 for different and normalized values of ($\tau_n = \tau/T_s$). It is again obvious that FSCR feedback results in best jitter suppression but the amplitude efficiency is worse than for DSCR and SCVR.

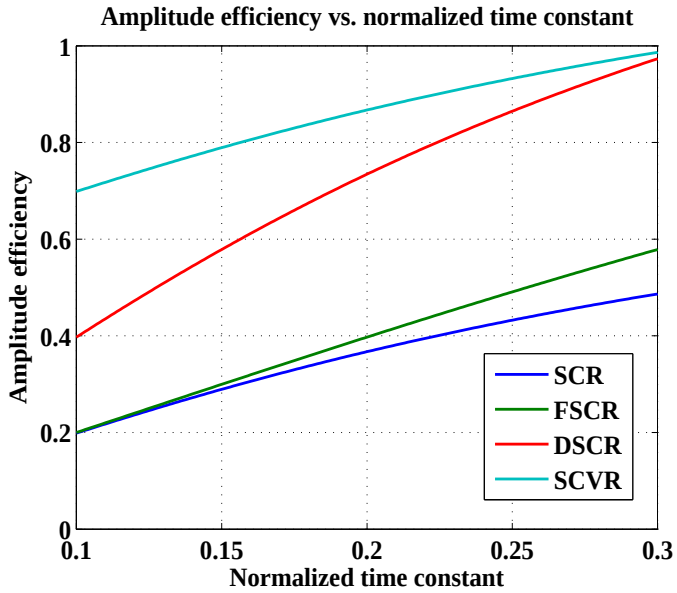

Fig. 3.13: Amplitude efficiency vs. normalized time constant.

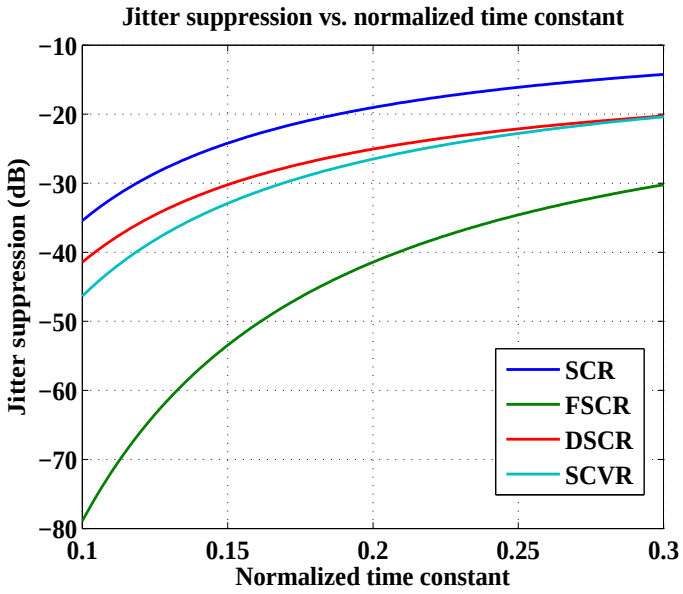

Fig. 3.14: Jitter suppression efficiency vs. normalized time constant.

3.3 MISMATCH ERRORS

One important advantage of single-bit DSMs is the fact that the feedback DAC is inherently linear and does not require precision matching. This is due to the fact that only two levels are used, and even if they are affected by errors due to component mismatch, the DAC characteristics will still remain linear. However, the achieved resolution of single-bit DSMs is limited by the stability criterion which restricts the use of aggressive NTFs. According to Lee's rule, the OBG of the NTF in a single-bit modulator is typically limited to 1.5 [46]. By employing multi-bit quantizers, this problem is alleviated and NTFs with higher OBGs are allowed which also result in less quantization noise in-band. Furthermore, in 3.2.3 it was argued that multi-bit feedback in CT DSMs is beneficial for reducing clock jitter. Unfortunately, multi-bit DACs lack the ability of achieving adequate linearity without high-precision matching. Contrary to single-bit DACs, more than two levels are used, and any mismatch errors affecting at least one of the levels will cause the transfer characteristics to deviate from a straight line. Again, the first DAC is the most critical as its errors are directly injected at the input. The non-linear characteristics of the DACs will cause harmonic distortion and noise. Harmonic distortion, in particular, might not be tolerable in the application of interest. To achieve the desired performance, the DACs must be as linear as the overall DSM [13] which can only be achieved by high-precision matching. Resistive DACs relieve matching requirements somewhat, compared to current steering DACs, since resistors show better matching accuracy than transistors [47]. However, to significantly relieve the matching requirements, some form of dynamic-element matching (DEM) can be used [6] [15]. The main principle behind DEM is the conversion of the static DAC non-linearity into pseudo-random noise. This is achieved by randomly choosing the different DAC unit elements. Then, noise shaping can be used, just as for the DSM, to push the noise to higher frequency which is then removed by the decimation filter. There are several implementations of DEM algorithms but the most efficient is data weighted averaging (DWA) [48]. DWA has been used to enhance the linearity of the multi-bit DSMs in [1–4].

4

Power saving techniques

The loop filter in a DSM is usually designed by using CIFB or CIFF structures where the number of integrators is determined by the order of the loop filter. Both architectures require power hungry operational amplifiers (opamps) to implement the integrators. Due to this reason, the loop filter is the the largest power consumer in a DSM. The key to minimizing the power consumption is therefore to use just the sufficient amount of power in the operational amplifiers to fulfil the requirements of every integrator. Another interesting option, described in this chapter, is to exploit other DSM architectures that can be realized with less operational amplifiers than the order of the loop filter.

4.1 REDUCING THE NUMBER OF OPAMPS

In DT DSMs, the switching nature of SC circuits enables the reuse of one opamp for several integrations. Thus, higher order DT loop filters with only one opamp can be realized resulting in significant power savings as demonstrated in [49]. Another method of reducing the number of opamps in DT DSMs is to use double sampling integrators [50][51]. By employing several SC structures around one opamp operating with time-interleaved signals, a second order integrator can be realized. These techniques cannot be employed in CT DSMs and therefore different approaches are required. This section will cover power reduction techniques for CT DSMs.

4.1.1 PASSIVE LOOP FILTERS

Passive networks are linear and have the ability to operate at low supply voltages without consuming any power from the supply. Thus they can be used in CT DSMs to completely avoid operational amplifiers [52–55]. In such a design, the comparator is the only active element. Fig. 4.1 shows a block diagram of a simple

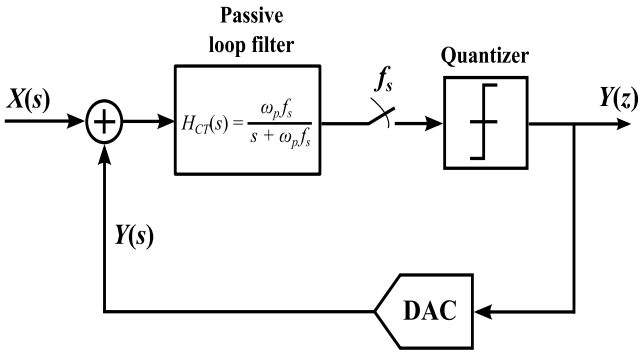

Fig. 4.1: Block diagram of a 1st-order single-bit passive CT DSM.

1st-order single-bit passive CT DSM. The loop filter is realized with a RC network with transfer function

$$H_{CT}(s) = \frac{\omega_p f_s}{s + \omega_p f_s} \tag{4.1}$$

where $\omega_p = 1/(RCf_s)$ is the normalized 3 dB cut-off frequency. The NTF depends on ω_p which should be less than 1 to achieve efficient quantization noise suppression. Thus, compared to a 1st-order CT DSM realized with an active integrator i.e. $H_{CT}(s) = f_s/s$, the output of the loop filter is attenuated by ω_p. To compensate for this, the quantizer gain of the passive DSM must be $1/\omega_p$ times higher. Since there is no gain in the passive network, the thermal noise resulting from the resistors is not suppressed. It can be shown that thermal noise is actually amplified and the effect is worse for lower ω_p. The quantization noise suppression on the other hand is improved for lower ω_p as the NTF approaches the ideal 1st-order noise shaping. Consequently, there is a trade-off between quantization noise and thermal noise and an optimal ω_p should be chosen to minimize the combination of both. This trade-off limits the maximum achievable SNR.

One important issue with passive CT DSMs is the small signal swing as the difference between the input signal and quantization noise is attenuated by the passive network. This also makes the design of the quantizer (especially the multi-bit quantizer) quite challenging since a large signal swing is required to avoid metastability. Therefore, the most appropriate way to increase the SNR of passive DSMs is to increase the OSR. For example, to achieve 10 to 12 bits of resolution, the OSR can be up to 1000 [53] [55].

4.1.2 ACTIVE-PASSIVE LOOPFILTERS

The design issues in 4.1.1 have been addressed in [54] by combining both passive and active networks. Using this strategy, a 5th-order CT DSM was implemented as shown in Fig. 4.2. The 2nd and 4th integrators are implemented as passive

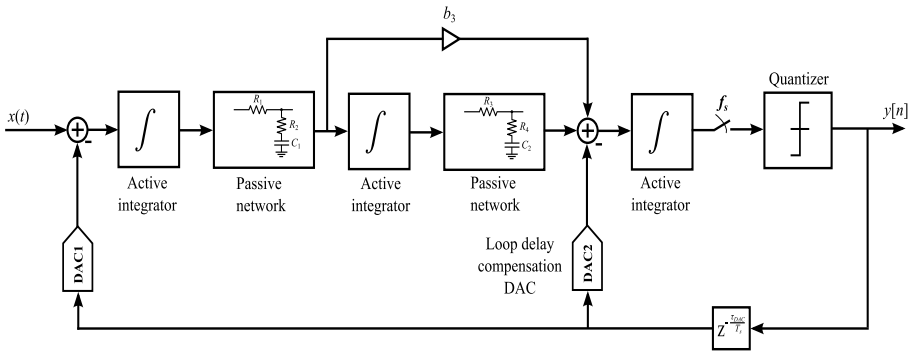

Fig. 4.2: Block diagram of a 5th-order single-bit active-passive CT DSM.

networks to reduce the number of opamps. The noise of the passive networks is suppressed by the gain of the active integrators. At least a 1st-order suppression of the noise from the second integrator is achieved. The reduced signal swing from the passive networks is compensated by the gain of the active integrators which simplifies the design of the quantizer. Similar to the passive DSM, the normalized cut-off frequency ω_p of the passive networks will affect the efficiency of the noise shaping. By optimizing both the gain of the first active integrator and ω_p of the second passive integrator, the desired noise shaping and proper signal scaling can be achieved.

4.1.3 SINGLE OPAMP LOOP FILTERS

Another way to reduce the power consumption of CT DSMs is to implement the loop filter with single opamp (SOA) networks [3] [4] [56–60]. A SOA network can be regarded as a combination of active and passive networks and therefore inherits the benefits of both. Since the opamp provides gain, just as in a conventional active RC integrator, there is no signal attenuation and the thermal noise is not amplified as in passive or active-passive DSMs. The use of higher order passive networks enables a more aggressive noise shaping than one active RC integrator but with only one opamp. Compared to the conventional CIFB or CIFF architectures, a loop filter based on SOA networks uses less opamps and therefore accumulates less phase delay caused by finite GBW of the opamps [58]. This results in better stability. In general, a SOA network consists of an arbitrary 4-terminal passive RC network and an opamp as shown in Fig. 4.3. The passive network can be fully characterized by its short circuit admittaces. The input signal to the network in general is the difference between the input signal V_{in} and the DAC feedback signal V_{fb}. If an ideal opamp with infinite gain is assumed, it can be shown that the transfer function of the SOA network is [61]

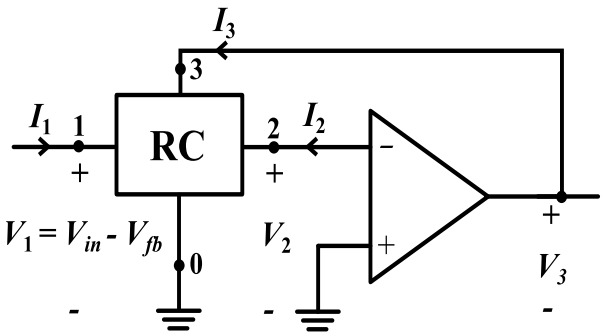

Fig. 4.3: General SOA network.

$$H_{CT}(s) = \frac{V_3}{V_1} = -\frac{y_{12}(s)}{y_{32}(s)} \tag{4.2}$$

where $y_{12}(s)$ and $y_{32}(s)$ are the short circuit admittances defined as

$$y_{12}(s) = \left.\frac{I_1}{V_2}\right|_{V_1,V_3=0}, \qquad y_{32}(s) = \left.\frac{I_3}{V_2}\right|_{V_1,V_3=0}. \tag{4.3}$$

To ensure proper operation of the DSM, the SOA based loop filter should implement the same feedback transfer function $H_{CT}(s)$ as an equivalent CIFB or CIFF loop filter. It can be shown that this transfer function of order L can also be implemented as a cascade of 2nd-order sections as demonstrated in Fig. 4.4 for the CIFF loop filter [57] [58]. In general, the transfer function of a 2nd-order section is given by

$$H_{si}(s) = k_1 \frac{s^2 + b_{1i}s + b_{0i}}{s^2 + \omega_{0i}^2}. \tag{4.4}$$

The form of the denominator indicates that the two poles are situated on the imaginary axis which results in a resonant transfer function. This enables the realization of zero-optimized NTFs. By setting $b_{1i} = 0$, the resulting transfer function is suitable for implementation of the lower architecture in Fig 4.4. Furthermore, $\omega_i = 0$ moves the two poles to the origin in both cases. Next, several SOA networks that implement the transfer function of the same form as (4.4) will be discussed.

SOA NETWORK 1

The first SOA network able to implement the transfer function in (4.4) is shown in Fig. 4.5. It has been developed in [58] and used as a part of a 5th-order DSM to reduce the number of opamps. The transfer function is of 3rd-order in general but

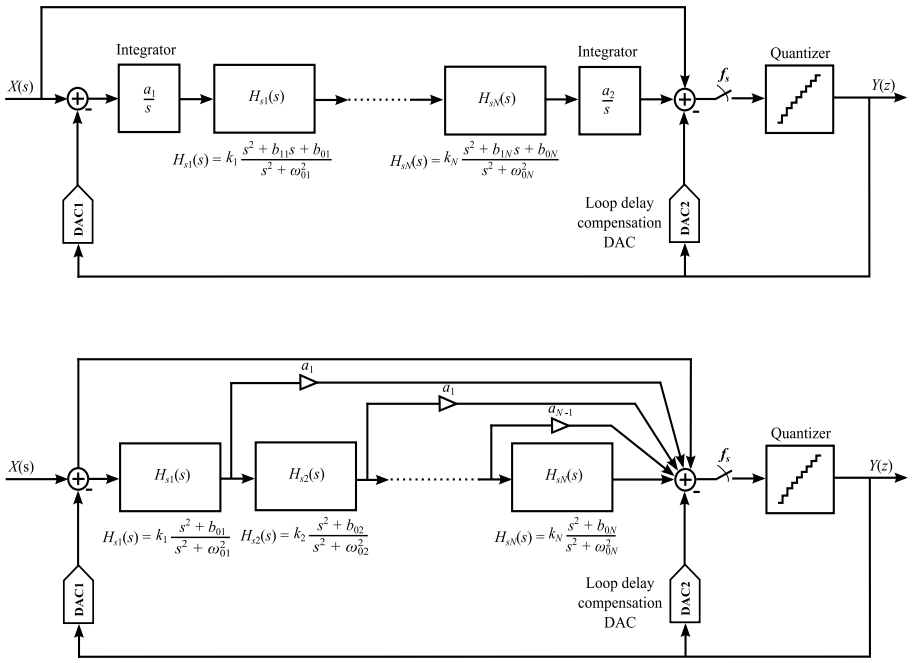

Fig. 4.4: Examples of the CIFF architecture implemented with 2nd-order SOA sections.

if the following resonating conditions are fulfilled, $R_3^{'}||R_{in2} = R_1||R_2||R_{in2}||R_{in1}$ and $C_3 = C_1 + C_2 + C_{in}$, the transfer function is of 2nd-order and is given by

$$H(s) = -\frac{\frac{C_{in}}{C_2}s^2 + \frac{1}{R_{in2}C_2}s + \frac{1}{R_1R_{in1}C_1C_2}}{s^2 + \frac{1}{R_1R_2C_1C_2}}. \tag{4.5}$$

The form of the denominator indicates that the two poles are situated on the imaginary axis which results in a resonant transfer function. Thus the SOA network can be used to implement zero-optimized NTFs. The disadvantage is that it cannot be placed in the front-end of the DSM. Since the input signal is not applied at virtual ground, its summation with the feedback signal from the DAC cannot be implemented as required in a DSM. Therefore, the SOA network must be preceded by one RC integrator which implies that implementation of a 2nd-order, or in general even order DSMs, cannot be implemented with these networks alone. This does not however prevent the use of the SOA network to reduce the number of opamps in later stages of a high odd order DSM.

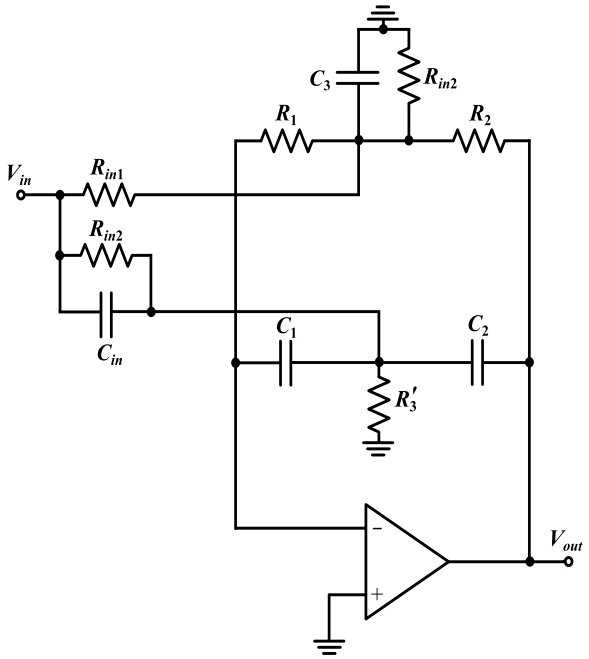

Fig. 4.5: SOA network 1.

SOA NETWORK 2

The next SOA network is shown in Fig. 4.6a and has been described in [3] [4] [56]. It consists of fewer passive components than the previous SOA network and it can be placed at the front-end of the DSM as the input signal is applied at virtual ground. The transfer function is given by

$$H(s) = -\frac{\frac{1}{n_2^2}\left(1+\frac{n_2}{n_1}\right)+\frac{3}{n_2}sRC}{(sRC)^2}. \tag{4.6}$$

where n_1 and n_2 are the sizing factors. The two poles are situated at the origin which implies that the implementation of zero-optimized NTFs is not possible. In Fig 4.6a it is assumed that the difference between the input signal and the DAC feedback has already been generated. In practice, these signals have to be applied separately and summed at a common point. This is achieved by transforming the network in Fig 4.6a to the one in Fig 4.6b. It can be shown that both networks have the same transfer function given by (4.6) [4].

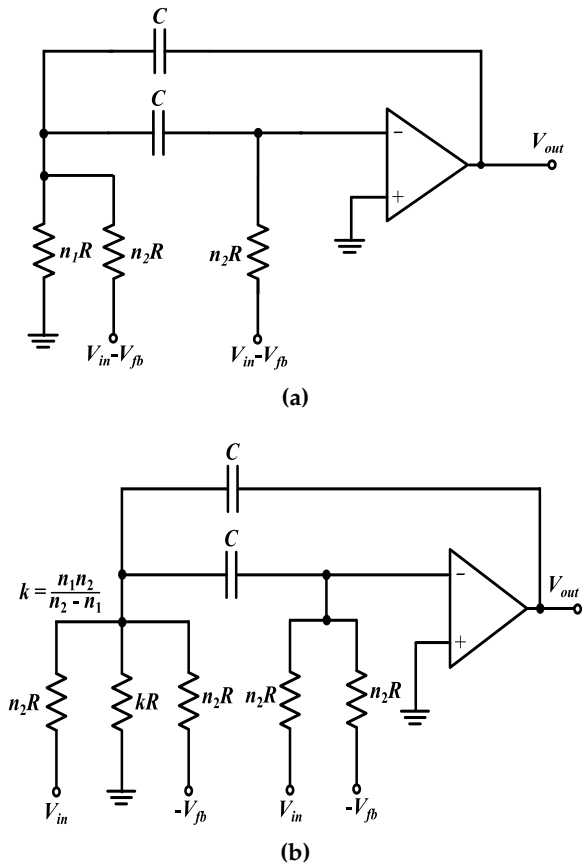

Figure 4.6: SOA network 2. (a) Basic network, (b) More practical implementation.

SOA NETWORK 3

During the course of this work, the SOA network in Fig. 4.7 has emerged [57]. Similar to the SOA network in Fig. 4.6, the injection of the difference between the input and the DAC signal at virtual ground permits the use in the DSM front-end. However, the design is simpler since the difference is only injected at virtual ground and nowhere else. The positive feedback path through R_4 results in the following resonating transfer function if the resonating condition $R_3C_1 = R_4(C_1 +$

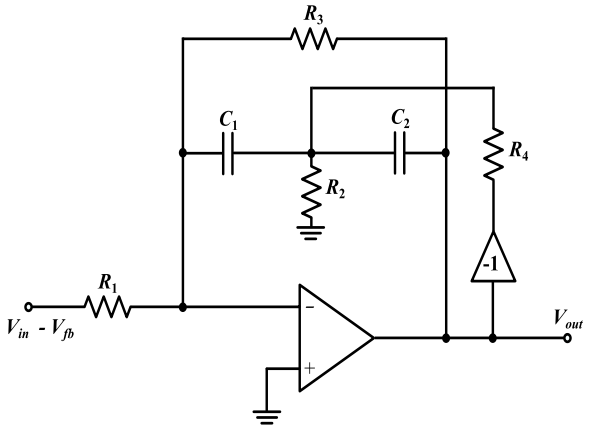

Fig. 4.7: SOA network 3.

C_2) is fulfilled:

$$H(s) = -\frac{1}{R_1C_1C_2}\frac{(C_1+C_2)s + \left(\frac{1}{R_2}+\frac{1}{R_4}\right)}{s^2 + \frac{1}{R_3C_1C_2}\left(\frac{1}{R_2}+\frac{1}{R_4}\right)}. \tag{4.7}$$

Alternatively, the poles at the origin can be implemented by removing R_3 and R_4. This version of the SOA network was used in the front-end of the DSM in [57] A similar network was used in [59] where it was also extended to 3rd-order.

4.1.4 ANTI-ALIASING

The SOA-based DSMs are architecturally different from conventional DSMs and thus it is of interest to examine how this affects the STF and the AA performance. To gain a better understanding, the block diagrams of the 2nd-order CIFB and SOA loop filters are compared in Fig. 4.8. The CIFB loop filter employs a distributed architecture with two integrators while the SOA loop filter can be regarded as a direct implementation of the desired feedback transfer function. In both cases, the feedback transfer function $H_{CT}(s)$ is the same and is given by:

$$H_{CT}(s) = -\frac{a_{CT1} + a_{CT2}T_s s}{(T_s s)^2}. \tag{4.8}$$

Both poles are at the origin as in [3] [4].

The forward transfer function $G_{CT}(s)$ affects the STF and is different in the two cases. For the CIFB loop filter it is a double integrating transfer function given by:

$$G_{CT}(s) = \frac{b_1}{(T_s s)^2}. \tag{4.9}$$

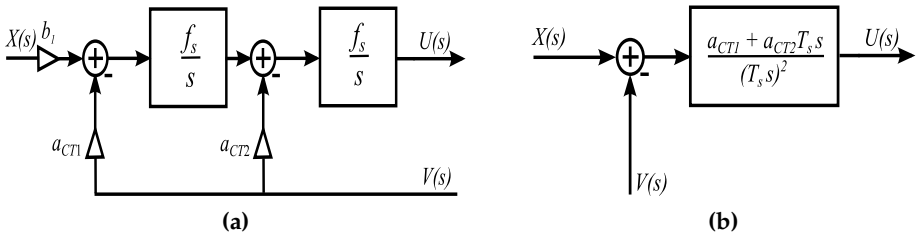

Figure 4.8: Block diagrams of: (a) A 2nd-order CIFB loop filter, (b) A 2nd-order SOA loop filter.

For the SOA loop filter however, $G_{CT}(s) = H_{CT}(s)$ which is a double integrating transfer function with one zero in the denominator. The magnitude response of $G_{CT}(s)$ is plotted in Fig. 4.9 for the 2nd-order CIFB and SOA loop filters. Due to the zero in the numerator, the slope of $|G_{CT}(j2\pi f)|$ for the SOA loop filter decreases after the break frequency leading to a reduced attenuation. The effect on the STF in the first aliasing zone is shown in Fig. 4.10. It has been shown that the AA suppression for CIFB DSMs is significantly better than for its CIFF counterparts [62] [63]. The plots in Fig. 4.10 suggest that the AA suppression of the SOA DSM is degraded compared to the CIFB DSM but is still better than for the CIFF DSM.

4.1.5 AMPLIFIER NON-IDEALITIES

The amplifier non-idealities, such as finite gain and GBW, alter the loop filter transfer function and result in an NTF with degraded quantization noise suppression [64]. In [4], a small signal model of the SOA network 2 was developed to study the effect of amplifier non-idealities. In this section, the SOA network 3 is compared to SOA network 2 in terms of amplifier requirements as it is relevant for the work in [4]. Both networks were adjusted to implement the same transfer function which is of the same form as in (4.8) with its both poles at the origin. For the SOA network 3, the poles are moved to the origin by removing the resistors R_4 and R_3, see Fig. 4.7.

The loop gain of the loop filter is an important quantity which determines how accurately the ideal loop filter transfer function is approximated. The small signal models for both networks were used to calculate the loop gain [65] under the influence of amplifier non-idealities. This procedure resulted in the plots shown in Fig. 4.11 and 4.12. In the first case, only a DC-gain of 62 dB is included while the GBW is infinite. In the second case, both finite DC gain and a GBW = 16 MHz are included where GBW was equal to the sampling frequency of the DSM. The loop gain of the SOA network 3 is somewhat higher due to less resistive loading on the amplifier by the feedback network. This leads to lower DC-gain

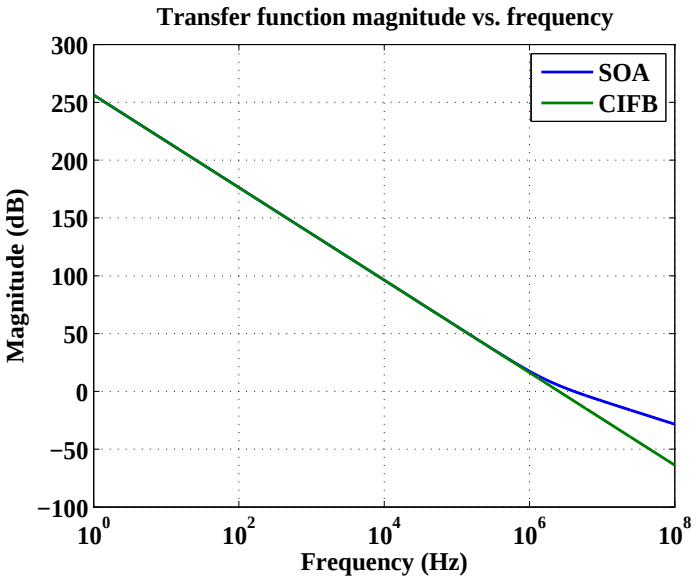

Fig. 4.9: Forward transfer functions of 2nd-order CIFB and SOA loop filters.

and GBW requirements. If $GBW = f_s$, the loop gain of both SOA networks drops significantly and therefore a GBW equal to f_s is not sufficient to achieve an acceptable performance. Thus, compared to a conventional active RC integrator, the DC-gain and GBW requirements of SOA networks are expected to be higher due to higher resistive loading by the feedback network. One way to increase the loop gain is by scaling up the resistors in the SOA networks. However the maximum sizes of the resistors are limited by other design constraints such as thermal noise and area.

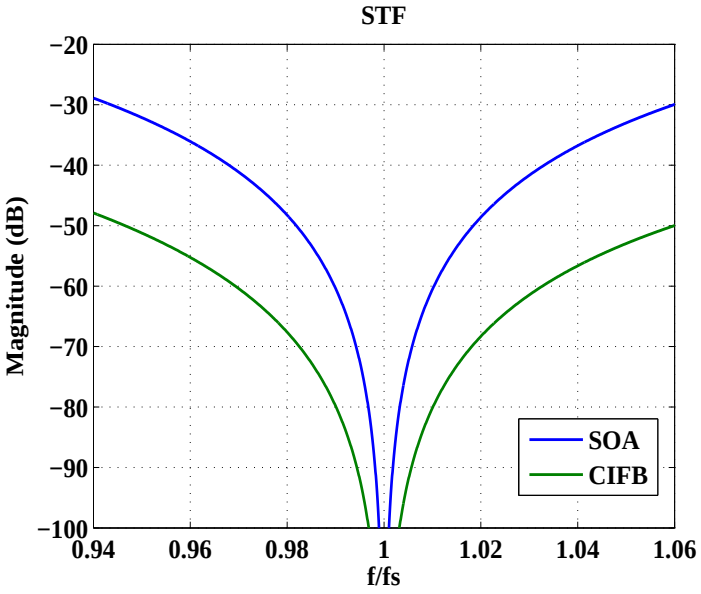

Fig. 4.10: STFs around the 1st aliasing zone of 2nd-order CIFB and SOA loop filters.

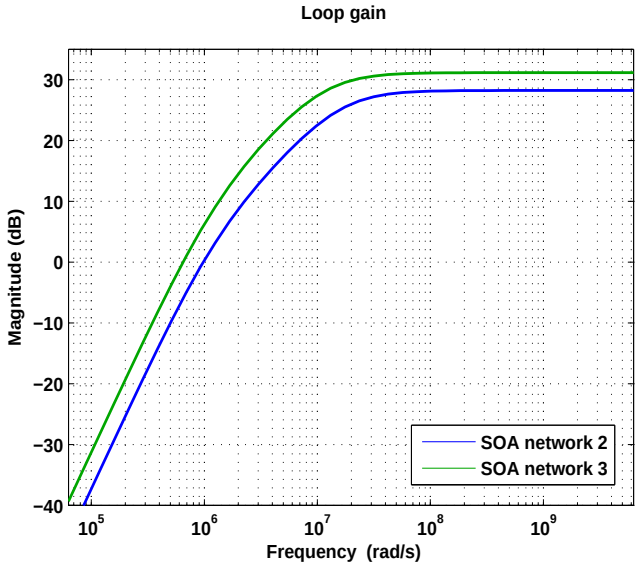

Fig. 4.11: Effect of finite DC gain on the loop gain.

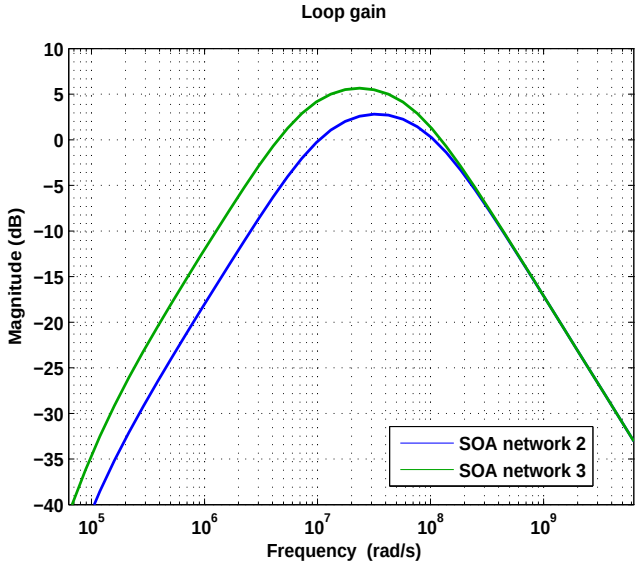

Fig. 4.12: Effect of finite DC gain and GBW on the loop gain.

5

A Low power CT ΔΣ modulator with a SAR quantizer

The use of multi-bit quantization in DSMs is beneficial for reducing the quantization error and relaxing the jitter requirement. It also enables the use of a lower sampling frequency. However, for a large number of bits, the power consumption can become an issue especially if the flash architecture is used to implement the quantizer. This chapter presents a low-power 2nd-order CT DSM with a 4-bit quantizer implemented with the successive approximation register (SAR) architecture which is more power efficient than the flash architecture. Generation of a high frequency clock normally required for proper operation of the SAR quantizer is avoided by using asynchronous control.

5.1 CT ΔΣ MODULATORS WITH SAR QUANTIZERS

The SAR ADC with its simple architecture requires almost no analog circuits and is the most energy efficient ADC. It has been extensively used in low power applications and for implementation of sub stages in other ADCs, for example, pipeline ADCs. Another possibility is to replace the commonly used flash-type quantizer in a DSM with a SAR-type quantizer to save power and area. This is achievable since for an N-bit quantizer, 2^N comparators are replaced by only one comparator clocked with a higher frequency than the sampling frequency.

There are a few publications of DSMs employing SAR quantizers. In [66], a SAR quantizer was used in a DT DSM for audio applications. Furthermore, two CT DSMs with SAR-quantizers were presented in [67] [68]. When used in a CT DSM, the SAR quantizer will introduce a loop delay as it requires several clock cycles to perform the conversion. As discussed in 3.1, the loop delay is detrimental to the performance of CT DSMs but it can be compensated by introducing an additional feedback path and a loop delay compensation DAC around the quantizer as shown in Fig. 5.1. In this work, the loop compensation DAC and the summing operation have been realised using switched capacitor techniques [67]. The delay

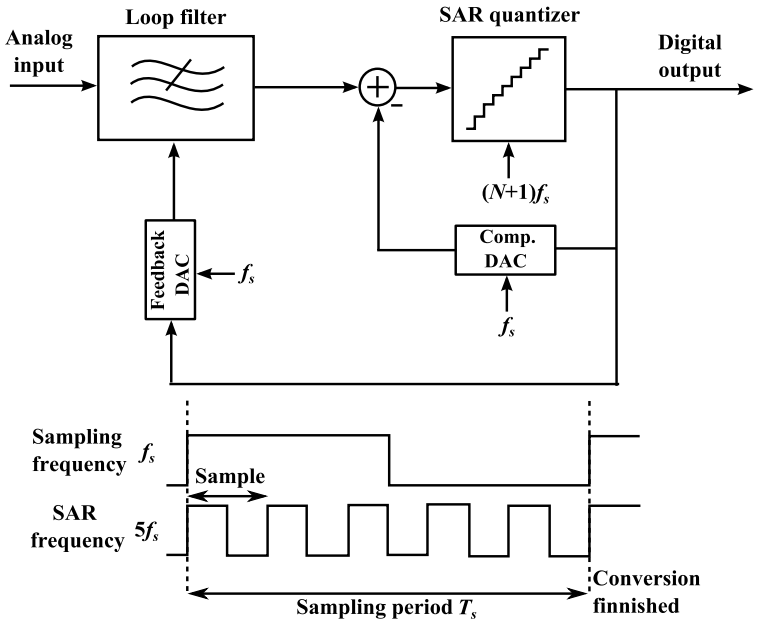

Fig. 5.1: Block diagram of a CT DSM with a SAR quantizer.

of the SAR quantizer has to be contained within one sampling period as it is not possible to fully compensate for larger loop delays. If the clock frequency for the SAR quantizer is chosen to more than $(N+1)f_s$, the loop delay will not exceed one sampling period as shown in the timing diagram in Fig. 5.1 for $N = 4$. Generation of the clock requires additional power and area and a delay-locked loop (DLL) for synchronization [67]. To avoid the generation of the high frequency clock, asynchronous control was adopted in this work [68] [69].

5.2 IMPLEMENTED ΔΣ MODULATOR

The implemented CT DSM had the same specifications as in [3] [4]. The targeted SNR is 60 dB over a 500 kHz bandwidth. In the DT-domain, the DSM was designed for an SQNR of 70 dB to leave a 10 dB margin for thermal noise and distortion. To achieve the targeted SNR, while keeping the sampling frequency as low as possible, a 4-bit quantizer was used. This choice together with a 2nd-order loop filter resulted in a sampling frequency of 16 MHz and an OSR of 16.

The block schematic of the DSM is shown in Fig. 5.2. The SOA network 2 described in 4.1.3 was used to implement the 2nd-order loop filter. Resistive NRZ DACs are used in the feedback while the loop compensation DAC is realized with SC techniques.

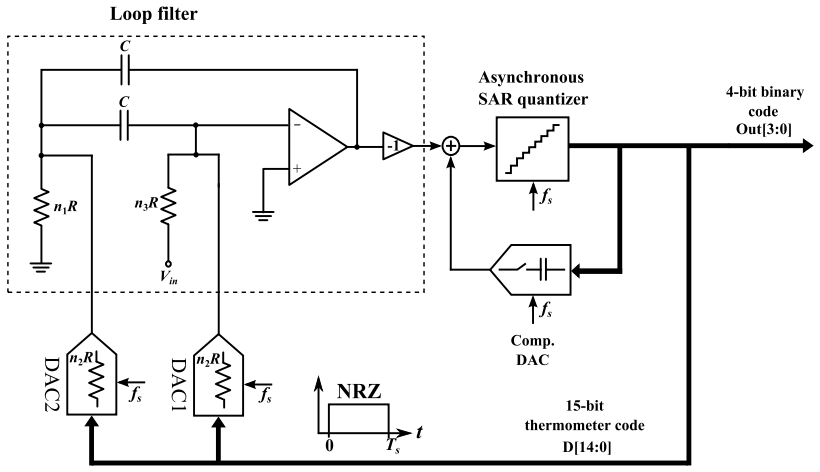

Fig. 5.2: Implemented CT DSM.

5.2.1 LOOP DELAY COMPENSATION

As discussed in 3.1.1, the loop delay t_d in CT DSMs can be compensated by adding an additional feedback path around the quantizer. This is shown in the block diagram in Fig. 5.3 for the equivalent CIFB implementation of the DSM in this work. The classical 2nd-order noise shaping, $NTF(z) = (1 - z^{-1})^2$ was realized by the DSM. The original CT coefficients with zero loop delay obtained after DT to CT conversion with NRZ feedback are $a_{CT1} = 1$, $a_{CT2} = 1.5$ [24] [28]. With loop delay affecting the feedback pulses, these coefficients have to be tuned and the added compensating coefficient a^*_{cmp} has to be determined to achieve full compensation. For a 2nd-order CT DSM with NRZ feedback, it can be shown that after compensation, the new set of coefficients are given by [24]

$$\begin{cases} a^*_{CT1} = a_{CT1} \\ a^*_{CT2} = a_{CT1}\tau_d + a_{CT2} \\ a^*_{cmp} = \dfrac{a_{CT1}\tau_d^2}{2} + a_{CT2}\tau_d \end{cases} \tag{5.1}$$

where τ_d is the normalized loop delay ($\tau_d = t_d/T_s$). Fig 5.4 shows a plot of the compensating coefficient for different values of τ_d. The results can be used to optimize the value of the compensating coefficient and the allocated loop delay for the SAR quantizer. In this design, the determination of the allocated loop delay was based on practical implementation details. Consequently, by choosing $a^*_{cmp} = 1$, the loop compensation DAC realized with SC techniques will be identical to the main DAC in the SAR quantizer. As will be discussed later, this results in a convenient implementation of the loop delay compensating feedback path and avoids the power hungry summing amplifier that would be required otherwise.

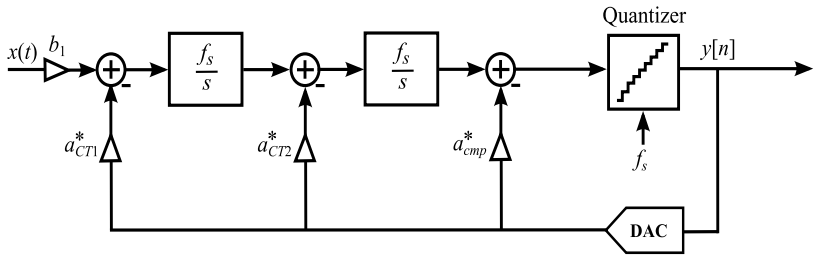

Fig. 5.3: Loop delay compensation of a 2nd-order CIFB CT DSM.

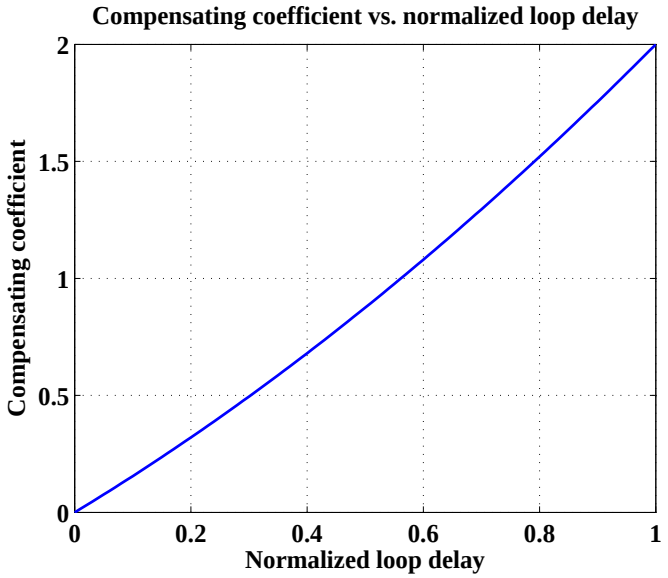

Fig. 5.4: Compensating coefficient vs. normalized loop delay.

From Fig. 5.4, $a^*_{cmp} = 1$ results in a loop delay of $t_d = 0.56T_s$. Using $\tau_d = 0.56$, the other coefficients are obtained from (5.1) which yields $a^*_{CT1} = 1$ and $a^*_{CT2} = 2$.

5.2.2 CONTROLLING THE STF

In 4.1.4 it was discussed that the STF of a 2nd-order SOA DSM depends on the coefficients a_{CT1} and a_{CT2}. Thus a change in these coefficients resulting after loop delay compensation will affect the STF. Later it was discovered that this can be achieved for the SOA network 2 in Fig. 4.6 by only injecting the input signal V_{in} at virtual ground and using an additional parameter n_3, see Fig. 5.5. Besides the gained control over the STF, the loop filter is further simplified. For completeness, the SOA network 3 with STF control is also shown in Fig. 5.5. This is simply

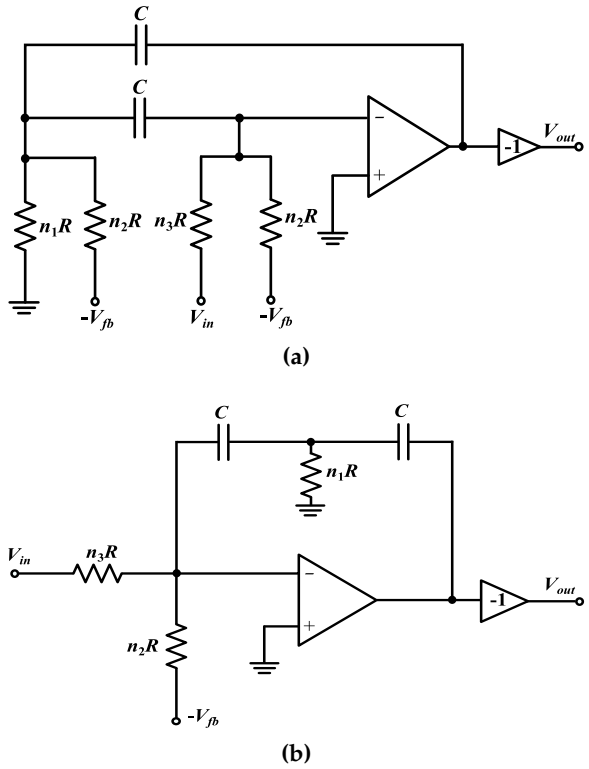

Figure 5.5: STF control for: (a) SOA network 2, (b) SOA network 3.

achieved by adding the input signal and the feedback at virtual ground where the additional parameter n_3 is used for the signal path. Using superposition, the outputs of both networks are found as

$$V_{out} = \frac{\frac{1}{n_3}\left(\frac{1}{n_2}+\frac{1}{n_1}\right)+\frac{2}{n_3}sRC}{(sRC)^2}V_{in} - \frac{\frac{1}{n_2}\left(\frac{1}{n_2}+\frac{1}{n_1}\right)+\frac{3}{n_2}sRC}{(sRC)^2}V_{fb} \tag{5.2}$$

$$V_{out} = \frac{\frac{1}{n_1n_3}+\frac{2}{n_3}sRC}{(sRC)^2}V_{in} - \frac{\frac{1}{n_1n_2}+\frac{2}{n_2}sRC}{(sRC)^2}V_{fb}. \tag{5.3}$$

Thus the input and the feedback signals are passed through different transfer functions. In both cases, the sizing factors n_1 and n_2 can be used to determine the coefficients for the feedback transfer function which realizes the desired NTF and then the parameter n_3 is used to adjust the forward transfer function and thereby the STF. The effect of STF control is demonstrated in Fig. 5.6. The loop delay compensation in 5.2.1 resulted in coefficients $a^*_{CT1} = 1$ and $a^*_{CT2} = 2$ and the STF

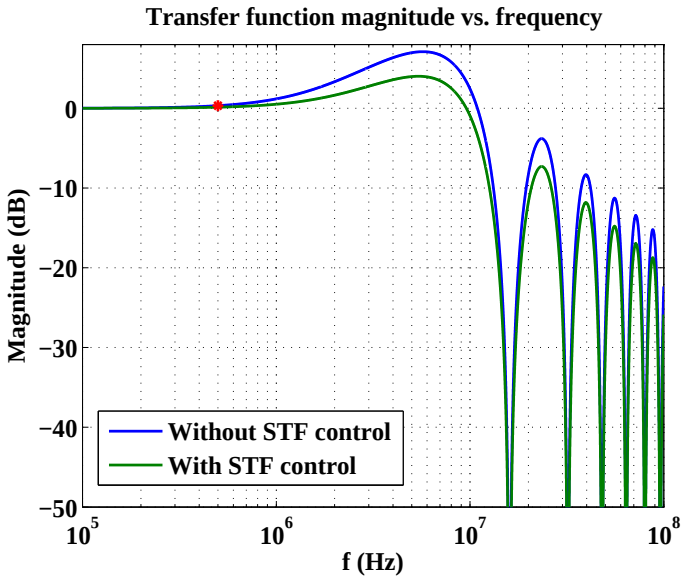

Fig. 5.6: STF Control.

represented by the blue curve. By adjusting the parameter n_3, the AA and out of band peaking was improved as shown by the green curve.

5.3 CIRCUIT IMPLEMENTATION

This section presents additional circuit implementation details of the CT DSM.

5.3.1 SAR QUANTIZER

The schematic of the 4-bit asynchronous SAR quantizer is shown in Fig. 5.7. The loop delay compensation DAC has been realized using the SC technique and embedded together with the main DAC. Since the compensation coefficient was set to 1 in 5.2.1, the compensation DAC can be identical to the main DAC which simplifies the design.

The timing diagram illustrating the operation of the SAR quantizer is also shown in Fig. 5.7. During the sampling phase, the main DAC samples the input signal V_{IN} while the loop compensation DAC holds the previous value $D_C[n-1]$. After the sampling phase, the conversion phase starts and the four bits $B_1 - B_4$ are successively determined. Since the operation is asynchronous, the duration of each bit is determined by the delays in the comparator, SAR-register and the control logic. The first bits are resolved quickly as the comparator handles the largest signal. Naturally, the LSB takes the longest time for the comparator to

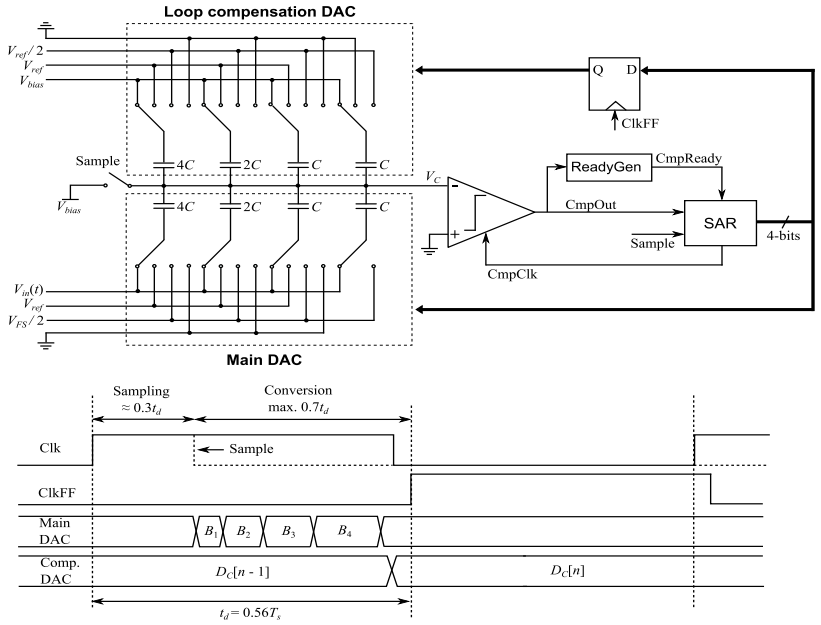

Fig. 5.7: Asynchronous SAR quantizer and timing diagram.

resolve. When the last bit has been determined, the conversion is finished and the compensation DAC is updated. The sampling phase occupies around 30% (10.5ns) of the loop delay while the remaining 70% (24.5ns) are left for the conversion phase. It is important to simulate the SAR quantizer over process variation to ensure that all the timing requirements are met and that the conversion is finished within the allocated time period. One consequence of restricting the implemented loop delay to $0.56T_s$ is that there is not much time left for the DWA after all the time margins. Therefore DWA was omitted in this design. Fortunately, from previous implementations it became evident that the DAC mismatch did not affect the performance significantly.

Both the main and the compensation DAC employ the tri-level charge redistribution technique to reduce the power consumption and improve the settling time [70]. The unit capacitor of each DAC was 50 fF. During the sampling phase, the input signal is sampled on the capacitor array of the main DAC just as for the conventional charge redistribution. However, during the determination of the first bit, the bottom plates of all capacitors are switched to $V_{ref}/2$ instead of V_{ref} which consumes less energy from the reference. The determination of the remaining bits switches the capacitors either to V_{ref} or ground depending on the latest determined bit. Another advantage of the tri-level charge redistribution is the reduction of the total capacitance by half which also results in energy savings compared to the conventional approach assuming the same unit capacitance.

Furthermore, the settling time is also improved since the capacitors are either switched in the same direction or one at the time.

Charge sharing between the capacitors in the main and the compensation DAC implements the required summing operation in the quantizer [67]. During the conversion phase, it can be shown that after charge sharing, the following voltage is present at the input of the comparator

$$V_C = \frac{1}{2}(-(V_{IN} - V_{CDAC}) + V_{MDAC}) \tag{5.4}$$

where V_{MDAC} and V_{CDAC} are the voltages from the main and the compensation DACs. The SAR quantizer determines the output bits by comparing the difference $V_{IN} - V_{CDAC}$ to V_{MDAC}. Charge sharing results in power savings as the implementation of the active summation amplifier is avoided. However, the comparator input signal is attenuated by half as shown in (5.4) which puts higher demands on the comparator.

5.3.2 COMPARATOR AND READY GENERATION

The two-stage dynamic comparator, shown in Fig. 5.8 was used in the SAR quantizer [71]. The first stage is a differential amplifier which suppresses the noise from the second stage. The second stage is a positive feedback latch. Since there is no static biasing, only dynamic power is consumed which makes the comparator energy efficient. To further reduce the power consumption, high-Vt devices have been used.

The CmpReady signal is generated by monitoring the two comparator outputs and deciding which output goes high as shown in Fig. 5.8 [69] [72]. When the comparator has taken a decision, one of the outputs will go high and the NOR gate will detect this by generating an active-low ready indication.

5.3.3 SAR

The asynchronous SAR register together with the timing diagram is shown in Fig. 5.9 [73]. The sampling signal determines when the conversion starts and ends. Control signals Clk1 - Clk4 are generated successively and used by the DAC control logic. The DAC control logic is shown to the right in Fig. 5.9. The flip-flop is used to sample the output of the comparator at the rising edge of Clki. If the comparator output is high, the relevant capacitor is switched from $V_{ref}/2$ to V_{ref} while for a low comparator output, the capacitor is switched to ground. The delay buffer is used to ensure that Clki triggers the AND gate after the output of the flip-flop has stabilized. In this way, unnecessary transitions are avoided.

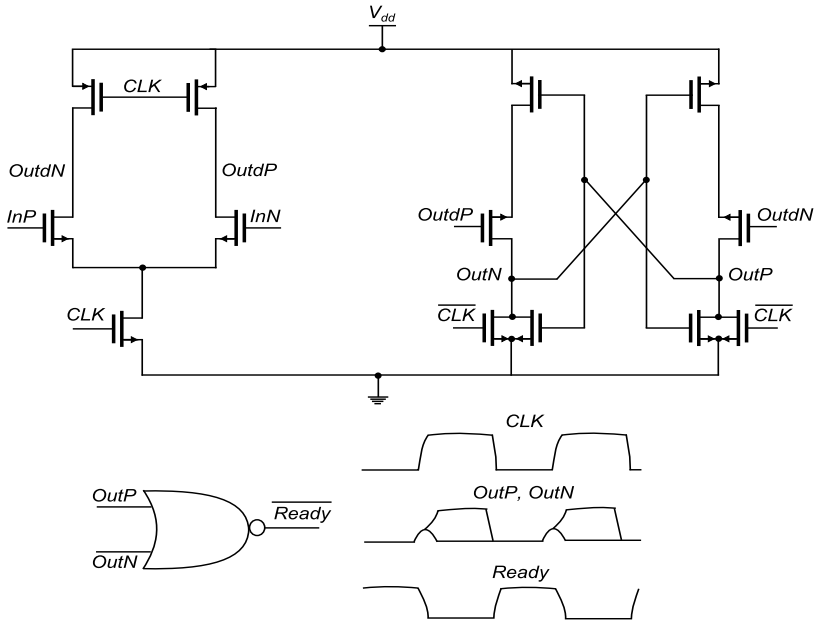

Fig. 5.8: Comparator and ready signal generation.

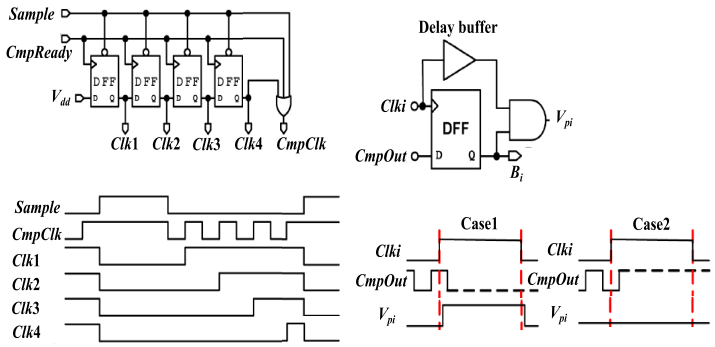

Fig. 5.9: Successive approximation register.

5.4 RESULTS

The DSM has been implemented in a 65 nm CMOS process. The circuit is powered by a 800mV supply and the simulated power consumption is 69 μW. The maximum differential input signal is 200mV. By employing the SAR architecture, the quantizer power consumption was reduced by 40% compared to the flash quan-

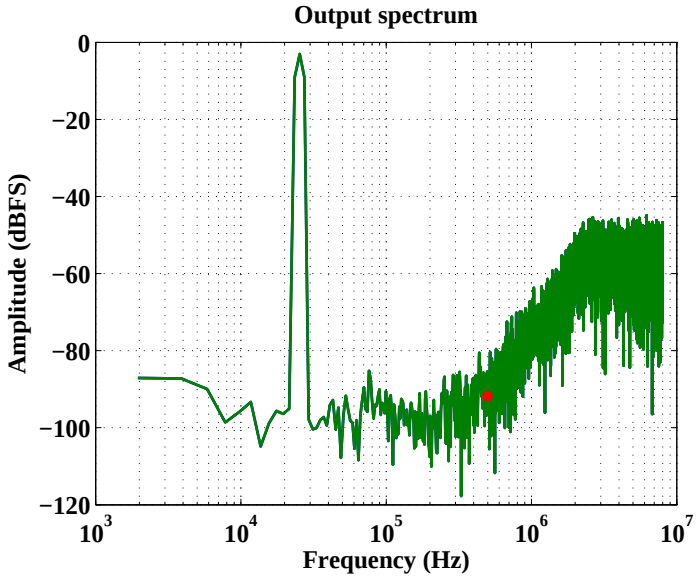

Fig. 5.10: Output spectrum.

tizer in [4]. The simulated output spectrum of the DSM including thermal noise is shown in Fig. 5.10 for an input signal amplitude of -3 dBFS. The simulated SNDR was 65 dB.

The design has been fabricated and tested. Unfortunately, the measurements show stability issues and therefore no results could be obtained. Since the parasitic extraction was not available at the time, the parasitics in the SAR quantizer could not be extracted. When parasitic extraction was performed later, it was discovered from the simulations of the extracted view that the SAR conversion process suddenly stops. Apparently, the parasitics seem to affect the operation of the asynchronous timing loop severely enough to cause malfunction. This issue is under investigation.

6

Conclusions and future work

This dissertation has presented different strategies for reducing power consumption and jitter sensitivity in CT ΔΣ modulators for ULP radios. In this chapter, the conclusions and suggested future work are provided.

The DSCR feedback has proved to be a possible technique for reducing the peak currents of exponential pulses while still maintaining relatively low jitter sensitivity. Compared to SCR feedback the peak current is reduced and the jitter suppression is improved while the circuit complexity is slightly increased. Furthermore, the thermal noise contribution from the DSCR DAC was small and didn't have any significant impact on the SNR of the designed modulator. The DSCR concept has been successfully verified by measurements on a fabricated chip. During the course of this work, another technique called FSCR feedback has emerged. Although it further improves the jitter suppression with a reasonable circuit complexity, the peak current is still larger than for DSCR feedback.

The usage of the single operational amplifier loop filter has resulted in a DSM with a performance that is well within the system requirements of the ULP radio and which achieves a state-of-the-art FOM. This has also been verified by measurements on a fabricated chip. During the course of this work, another single operational amplifier loop filter with signals injected only at virtual ground has been presented [57]. Therefore it is interesting to examine this possibility in more detail. Other amplifier architectures could also be investigated and optimized to further reduce the power consumption.

The reduction of the quantizer power consumption is also of interest and has been accomplished by replacing the commonly used flash quantizer with an asynchronous SAR quantizer. Asynchronous operation avoids the generation of a high frequency clock which would result in additional power consumption. Simulations have shown that the SAR architecture reduces the quantizer power consumption by 40% compared to the flash architecture. It can be interesting to combine this approach together with the single operational loop filter in [57].

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Paper I

Paper I

A Continuous Time $\Delta\Sigma$ Modulator with Reduced Clock Jitter Sensitivity through DSCR Feedback

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A Continuous Time $\Delta\Sigma$ Modulator with Reduced Clock Jitter Sensitivity through DSCR Feedback

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***Abstract*—This paper presents a low-power multi-bit continuous-time $\Delta\Sigma$ modulator with a new approach to clock jitter reduction utilizing switched-capacitor-resistor techniques. The modulator features a 3rd order loop filter, implemented with active RC integrators, and 3-bit quantizer and feedback DACs.**

The $\Delta\Sigma$ modulator has been implemented in a 65nm CMOS process and tested. It achieves a peak SNDR of 70 dB in a 125 kHz signal bandwidth while consuming 380 μW. The combination of a high-order loop filter and multi-bit quantizer allows for a high resolution at a low sampling frequency of 4 MHz, corresponding to an oversampling ratio of 16.

I. Introduction

Continuous-time (CT) $\Delta\Sigma$ modulators have become popular in low power applications due to several advantages compared to their discrete-time counterparts. Bandwidth and slew rate requirements for the operational amplifiers in CT loop filters are relaxed, since they do not suffer from severe settling time-requirements present in switched-capacitor circuits. A sample and hold circuit is not required at the input, as the sampling operation is performed just before quantization. At this stage of the modulator, all errors are significantly suppressed by the feedback loop, and thus sensitivity to sampling errors is a much relaxed issue. Yet another advantage of CT $\Delta\Sigma$ modulators is their inherent anti-alias filtering. This feature simplifies or eliminates the need of any external anti-alias filter at the modulator input. All of the mentioned advantages come at the price of an increased sensitivity to circuit non-idealities, such as loop delay, process variations, and clock jitter. This paper addresses primarily the last of these issues.

Clock jitter in CT $\Delta\Sigma$ modulators has been studied in a number of publications, see e.g. [1]-[3]. The performance of a CT $\Delta\Sigma$ modulator is mostly degraded by the jitter affecting the first feedback DAC, since every non-ideality at this point is directly injected at the modulator input. Several attempts have been made to modify the feedback pulses from the first DAC in such a way as to reduce the errors caused by jitter. One simple and attractive solution is to implement the DAC with switched-capacitor-resistor (SCR) techniques [4]. By periodically switching the capacitor in the RC network, a relatively constant amount of charge is fed back every clock cycle. This charge is little sensitive to the exact clock timing, and therefore the impact of jitter is reduced.

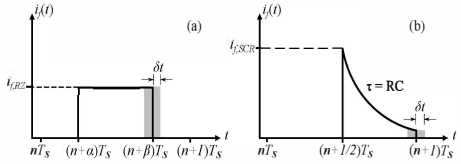

Fig. 1. Normalized DAC current feedback waveforms. (a) Return-to-zero. (b) SCR.

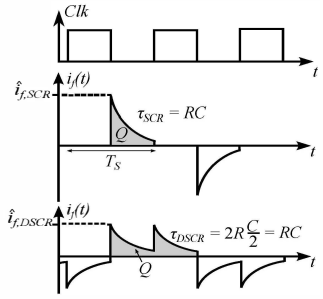

Fig. 2. Timing diagram of SCR and DSCR feedbacks

In this paper, an alternative SCR multi-bit DAC is proposed. It is used to implement a 3rd-order, 3-bit low-power CT $\Delta\Sigma$ modulator. Besides clock jitter reduction, the proposed architecture relaxes the slew-rate requirement of the operational amplifier in the first integrator, with great benefit on power consumption, since this operational amplifier draws the highest current.

II. SCR Feedback Principle

Timing uncertainties due to clock jitter give rise to pulse width variations of the feedback pulses, which result in charge errors. This is shown in Fig. 1(a) for the commonly used return-to-zero (RZ) current pulses. The shaded area represents a charge error which is integrated by the first integrator and transferred to the output. SCR feedback reduces these errors by employing exponential pulse shapes. A comparison between Fig. 1(a) and Fig. 1(b) shows that the error area is (much) smaller for an exponential pulse, i.e. the charge errors are exponentially attenuated. Reduced sensitivity is achieved by increasing the RC constant at the expense of higher peak cur-

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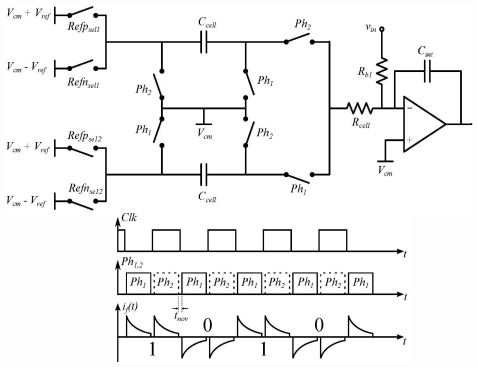

Fig. 3. Schematic and timing diagram of the DAC cell used for generation of DSCR pulses. The cell drives an active RC integrator.

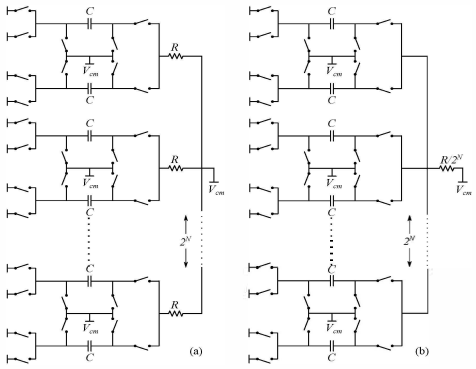

Fig. 4. Two equivalent implementations of the multi-bit DSCR DAC. (a) switched-capacitor cells with one resistor each. (b) switched-capacitor cells with a common resistor.

rents and thereby increased amplifier slew-rate requirements. A possible solution to this problem has been proposed in [5]. In this paper an alternative approach is presented.

A. Proposed SCR Feedback

One possible method to reduce the peak current of an exponential feedback pulse is to divide it into two identical units, while keeping the total charge the same as for a single pulse (Fig. 2). This technique will be called dual SCR (DSCR) feedback. Since the charge Q is distributed over two pulses, two capacitors with half the size are required. For the same time constant the resistor must be doubled and the peak current is halved.

The implementation of a DAC cell generating dual exponential pulses is depicted in Fig. 3, where the single-ended version is shown for simplicity. It consists of parasitic-insensitive switched-capacitor circuits to avoid any switch parasitic capacitances in parallel with the cell capacitance. The control signals $Refp_{sel1,2}$ and $Refn_{sel1,2}$ select either the positive or the negative reference, depending on whether the corresponding output bit from the quantizer is 1 or 0. A logic circuit is used to generate $Refp_{sel1,2}$ and $Refn_{sel1,2}$ from the clock phase signals $Ph_{1,2}$ and the quantizer output. The operation of the circuit is as follows: during Ph_1 the upper capacitor is charged either to V_{ref} or $-V_{ref}$ depending on the digital value from the quantizer. Simultaneously, the lower capacitor is discharged through the resistor, resulting in the first exponential current pulse which enters the virtual ground of the integrator. During Ph_2 the process is reversed as the upper capacitor is now discharged through the resistor, creating the second current pulse, while the lower capacitor is charged either to V_{ref} or $-V_{ref}$. The end result is a sequence of double exponential current pulses as shown in the timing diagram in Fig. 3. A finite non-overlap time t_{nov} between Ph_1 and Ph_2 is required to avoid short circuits through simultaneously closed switches.

The double exponential DAC concept can be extended to the multi-bit case by replicating the DSCR cell together with the resistor R_{cell} and connecting the replicas in parallel, see Fig. 4(a). Another possibility is to discharge all capacitors through a single resistor as shown in Fig. 4(b). In order to keep the same current as in Fig. 4(a), the value of the resistor must be reduced to $R/2^N$ (parallel connection of 2^N resistors with value R) where N is the number of bits in the DAC. Furthermore, since all capacitors are discharged through one resistor, the equivalent capacitance is a factor 2^N times the cell capacitance and the RC time constant is kept the same as in Fig. 4(a). Consequently, area is saved, as only one resistor with value $R/2^N$ is needed, compared to 2^N resistors with value R. Due to this advantage, the single-resistor architecture was used to implement the first DAC in the $\Delta\Sigma$ modulator.

B. Thermal noise

As with all switched-capacitor circuits, thermal noise must be taken into account when designing DSCR multi-bit DACs. The overall thermal noise consists of both direct noise and sampled-and-held noise, i.e. kT/C noise. Referring to Fig. 3, the direct noise spectral density of an SCR cell referred to the input of the first integrator is given by [6]

$$S_{D,SCR}(f) = D\frac{(2\pi f R_{b1} C_{cell})^2 4kTR_{cell}}{(2\pi f R_{cell} C_{cell})^2 + 1} \qquad (1)$$

where D is the duty cycle of the clock that turns the switches on and off, f is the clock frequency, k is Boltzmann constant and T is the absolute temperature. It is assumed here that the switch resistances are included in R_{cell}. Integrating (1) from dc up to the signal bandwidth f_{bw} yields the direct input-referred noise power

$$\overline{v}^2_{D,SCR} = \frac{DR^2_{b1}kT}{R_{cell}}\left(f_{bw} - \frac{arctan(2\pi R_{cell}C_{cell}f_{bw})}{2\pi R_{cell}C_{cell}}\right). \qquad (2)$$

Assuming a high oversampling ratio (OSR), the input-referred sampled-and-held noise power over the signal bandwidth is given by [6]

$$\overline{v}^2_{S,SCR} = (1-D)^2 4kTR^2_{b1}f_s f_{bw}C_{cell} \qquad (3)$$

where f_s is the sampling frequency. Since both half circuits in a DSCR cell generate noise, the contributions in (2) and (3) are doubled. Additionally, in a multi-bit DSCR DAC, the equivalent capacitance is $2^N C_{cell}$, which also has to be substituted into the expressions.

From (2) and (3), it is obvious that the input-referred noise can be reduced by scaling down the capacitor. This is in contrast to plain kT/C noise, where the capacitor needs to be maximized to minimize noise. Furthermore, noise is also dependent on the input resistor of the integrator.

The capacitor size in a DSCR DAC is restricted by different design constraints and cannot be made excessively small. Choosing the minimum practical capacitor value can help making the input-referred noise non-dominant, but it might also jeopardize matching between the unit components in the DACs. Consequently, there is a design trade-off involved between noise and matching. The capacitance value can be minimized by maximizing V_{ref}, which is limited by the supply voltage [7]. For V_{ref} = $V_{dd}/2$, minimum capacitance and thereby minimum input-referred noise is achieved. The feedback resistor is simultaneously maximized and reduces the impact of the non-linear switch resistance during capacitor discharge.

III. System Design and Circuit Implementation

The DSCR multi bit-DAC has been used in a CT $\Delta\Sigma$ modulator intended for wireless ultra-low-power portable devices. System simulations in the discrete-time domain resulted in an adequate SQNR of 81 dB to meet the overall SNR target of 73 dB over a 125 kHz bandwidth. Since it was desirable to keep the oversampling ratio (OSR) at the low value of 16, a 3rd order loop filter with a 3-bit quantizer proved to be a suitable choice for the modulator architecture. The so-called CIFB architecture [8] was chosen for the loop filter and it was implemented with active-RC integrators and additional feedback paths for zero optimization of the NTF. The block schematic of the modulator is shown in Fig. 5.

A. DT-CT conversion and jitter sensitivity

In order to keep the feedback charge of RZ and DSCR pulses equal, the feedback coefficient has to be increased, which results in higher peak currents. It is possible to find an analytical expression for the CT feedback coefficient for the DSCR feedback path in terms of the discrete-time (DT) coefficient by using the DT-to-CT transformation [9]. This expression was verified with a numerical DT-CT mapping method implemented directly in Cadence.

Jitter-suppression efficiency is defined as the amount of suppression that the white Gaussian-distributed pulse-width jitter experiences in the proposed DAC, as compared to the standard RZ DAC [5]. This measure is related to the RC time constant, which was chosen to $\tau \approx 0.16T_s$, and resulted in 20 dB of jitter suppression. The capacitance in the DSCR DAC was set to C_{cell} = 165 fF with V_{ref} set to $V_{dd}/2$. Finally, the input-referred direct and sampled-and-held noise are calculated to $\overline{v}^2_{D,DSCR} = 1.1 \cdot 10^{-13}\ V^2$ and $\overline{v}^2_{S,DSCR} = 2.7 \cdot 10^{-11}\ V^2$.

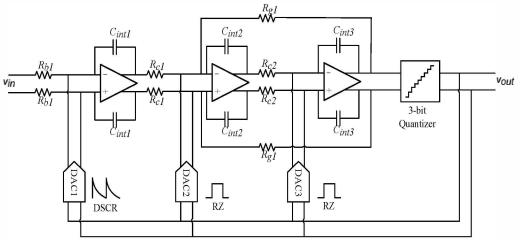

Fig. 5. Block diagram of the $\Delta\Sigma$ modulator.

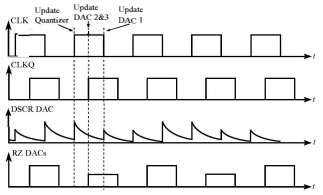

Fig. 6. Overall timing of the $\Delta\Sigma$ modulator.

The maximum total in-band noise for a $\Delta\Sigma$ modulator with 73dB SNR and 200 mVpp input amplitude is $10^{-9}\ V^2$, which shows that our input-referred noise is not dominant and can be neglected. Thermal noise from the input resistors of the first integrator is the most dominant noise source. These resistor values were chosen to achieve the targeted SNR.

RZ DACs were used in the two remaining feedback paths due to simpler implementation compared to the DSCR DAC. The high jitter sensitivity of the RZ DACs is not a primary issue, since any jitter further back in the modulator chain is at least first-order noise shaped. The RZ pulses were delayed a quarter of the clock period (α = 0.25 and β = 0.75), which ensures that the quantizer has fully processed the samples before they are converted by the DACs. RZ feedback is advantageous here over non-return-to-zero (NRZ) feedback since a delayed NRZ pulse would enter into the next clock period. To compensate for this, an extra feedback DAC might be required as well as an adjustment of the loop filter coefficients [8].

B. Circuit implementation

All RC integrators were implemented using a folded-cascode amplifier with 74dB dc gain and a gain bandwidth product of 62 MHz. Both transistors in the input pair operate in weak inversion, and the channel lengths are increased to reduce flicker noise.

Switched-resistor cells were used to realize the two RZ DACs. An additional switch is required in all cells to short both input terminals of the operational amplifier after one half clock period and thereby create the RZ pulse. Since the RZ pulses are delayed by one quarter of clock period, both RZ DACs are clocked by a quadrature clock. The overall timing of the $\Delta\Sigma$ modulator is shown in Fig. 6. All DACs are updated well after the beginning of the clock period, which ensures

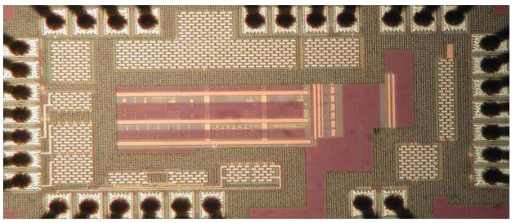

Fig. 7. Chip photo

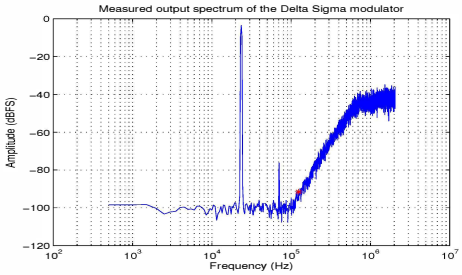

Fig. 8. Measured output spectrum

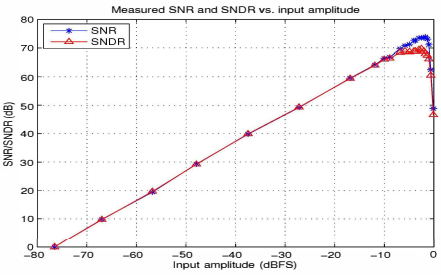

Fig. 9. Measured SNR and SNDR vs. input amplitude

that the quantizer has processed the samples before they are converted to analog form.

The 3-bit flash quantizer was realized with a resistor ladder and regenerative latch comparators without preamplifiers. The overall design also includes a non-overlapping clock generator and a DWA algorithm for dynamic element matching of the DAC components to improve linearity.

IV. Measurement Results

The $\Delta\Sigma$ modulator has been fabricated in a 65 nm CMOS process and tested. Fig. 7 shows the die photo of the modulator, which occupies an active area of 0.17 mm^2. The circuit is powered by a 900 mV supply and the total power consumption is 380 μW. The maximum differential input signal is 200 mV. An audio precision instrument was used to generate a clean input signal during measurements. An I/Q modulation generator was used to generate a clean and stable sinusoidal clock signal which was buffered on chip.

Table I
Results Summary

Parameter	Measured performance
Technology	65nm CMOS
Supply voltage	900 mV
Active area	0.17mm^2
Signal bandwidth	125 kHz
Maximum input amplitude (-3dBFS)	200 mV differential
Clock frequency	4 MHz
Peak SNR	74 dB
Peak SNDR	70 dB
Power consumption	380 μW

The measured output spectrum of the $\Delta\Sigma$ modulator is shown in Fig. 8 for an input signal amplitude of -2.5 dBFS, while SNR/SNDR vs. the input signal amplitude are shown in Fig. 9. The modulator achieves a maximum SNR of 74 dB for an input signal of -1.7 dBFS, and a maximum SNDR of 70 dB for an input signal of -2.5 dBFS. If the DWA algorithm is inactivated, a second order harmonic at -73 dBFS appears in the spectrum. This shows that the DWA algorithm successfully corrects for the mismatch errors in the DAC unit elements. Table I summarizes the modulator performance.

V. Conclusions

This paper has presented a CT $\Delta\Sigma$ modulator with a dual switched-capacitor-resistor multi-bit DAC. By dividing the exponential feedback pulse into several identical unit pulses, the peak current and thereby the operational amplifier slew-rate requirement are reduced, while the DAC is still insensitive to clock jitter. The technique has been tested in a 65nm CMOS 3rd-order 3-bit CT $\Delta\Sigma$ modulator, achieving a peak SNR of 74 dB and a peak SNDR of 70 dB while consuming 380 μW.

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Paper II

Paper II

A Continuous Time Delta-Sigma Modulator with Reduced Clock Jitter Sensitivity through DSCR Feedback

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A continuous time delta-sigma modulator with reduced clock jitter sensitivity through DSCR feedback

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Abstract The performance of continuous time delta-sigma modulators is limited by their large sensitivity to feedback pulse-width variations caused by clock jitter in their feedback DACs. To mitigate that effect, a dual switched-capacitor-resistor feedback DAC technique is proposed. The architecture has the additional benefit of reducing the typically high switched-capacitor-resistor DAC output peak currents, resulting in reduced slew-rate requirements for the loop-filter integrators. The feedback technique has been implemented with a third order, 3-bit delta-sigma modulator for a low power radio receiver, in a 65 nm CMOS process, where it occupies an area of 0.17 mm^2. It achieves an SNDR of 70 dB over a 125 kHz bandwidth with an oversampling ratio of 16. The power consumption is 380 μW from a 900 mV supply.

Keywords Delta-sigma · Clock jitter · Continuous time · Peak current · Switched-capacitor-resistor

1 Introduction

Continuous-time (CT) delta-sigma modulators have become popular in low power applications due to several advantages compared to their discrete-time (DT) counterparts. Bandwidth and slew-rate requirements for the operational amplifiers in CT loop filters are relaxed, since they do not suffer from severe settling time requirements present in switched-capacitor circuits [1]. A sample and hold circuit is not required at the input, as the sampling operation is performed before quantization. At this stage of the modulator, all errors are significantly suppressed by the feedback loop, and thus sensitivity to sampling errors is a much relaxed issue [2]. Yet another advantage of CT delta-sigma modulators is their inherent anti-alias filtering [3, 4]. This feature simplifies or eliminates the need of any external anti-alias filter at the modulator input.

All of the mentioned advantages come at the price of an increased sensitivity to circuit non-idealities, such as loop delay, process variations, and clock jitter [5–7]. This paper addresses primarily the last of these issues.

Clock jitter in CT delta-sigma modulators has been studied in a number of publications, see e.g., [7–9]. The performance of a CT delta-sigma modulator is mostly degraded by the jitter affecting the first feedback DAC, since every non-ideality at this point is directly injected at the modulator input [10]. Several attempts have been made to modify the feedback pulses from the first DAC in such a way as to reduce the errors caused by jitter. In [11] sine shaped feedback pulses are used in the DACs. The generation of sine shaped pulses is, however, not trivial and might require a phase locked loop and additional synchronization blocks. One simple and attractive solution is to implement the DAC with switched-capacitor-resistor (SCR) techniques [12–14]. By periodically switching the capacitor in the RC network, a relatively constant amount of charge is fed back every clock cycle. This charge is insensitive to the exact clock timing, and therefore the impact of jitter is reduced.

In this paper, an alternative SCR multi-bit DAC is proposed. It is used to implement a 3rd-order, 3-bit low-power CT delta-sigma modulator. The implementation of the DAC reduces the peak current of the feedback pulses

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and thereby the slew rate requirements on the operational amplifiers. The main idea is to reduce the peak current and still achieve low sensitivity to clock jitter. Before describing the new SCR technique, existing DAC feedback techniques are reviewed.

1.1 Different DAC feedback waveforms

A simple first order single-bit CT delta-sigma modulator is shown in Fig. 1 for RZ and SCR feedback [12]. The output bit stream from the comparator D_{out} controls the switch which connects the resistor or the capacitor to the positive reference voltage V_{ref+} or the negative reference voltage V_{ref-}. For the modulator with RZ feedback, the RZ switch is opened at a desired time point during the clock period and no feedback current is added to or subtracted from the integrator virtual ground. This action returns the feedback current to zero. For the modulator with SCR-feedback, the PreCh switch is used to pre-charge the capacitor C_a during the first half of the clock period while the DisCh switch discharges the capacitor through the resistor R_a during the second half of the clock period. The resulting feedback current waveforms $i_{f,RZ}(t)$ and $i_{f,SCR}(t)$ are shown in Fig. 2 for a jittered clock. Timing uncertainties due to clock jitter give rise to pulse width variations of the feedback pulses, which result in charge errors. The charge errors are integrated by the integrator and transferred to the output. For a jittered RZ-pulse, the charge errors are directly proportional to the timing errors which explains the high sensitivity to clock jitter. SCR feedback reduces the charge errors by employing exponential pulse shapes. A comparison between both feedback waveforms in Fig. 2 shows that the error area is (much) smaller for an exponential pulse i.e., the charge errors are exponentially attenuated.

Since most of the charge is transferred in the beginning of the discharge phase, the charge lost due to a timing error is relatively small. Similar behavior can be found in discrete DT delta-sigma modulators which explains their low sensitivity to clock jitter.

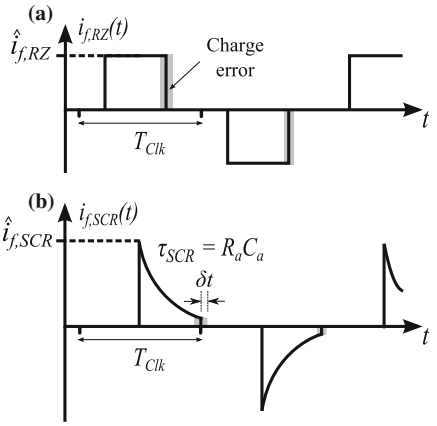

Fig. 2 DAC current feedback waveforms. **a** RZ, **b** SCR

The jitter sensitivity of a CT delta sigma modulator with SCR feedback is dependent on the RC time constant. It decreases with decreased RC time constant since the amount of charge transferred early during the discharge phase increases. On the other hand, this results in higher peak currents and thereby puts a higher demand on the amplifier slew-rate requirements

One possible method to reduce the peak current of an exponential pulse, while still keeping a relatively low jitter sensitivity, has been proposed in [15]. The main idea is to combine the low peak current of an RZ pulse with the reduced jitter sensitivity of an SCR pulse. The resulting feedback current waveform and the corresponding circuit are both shown in Fig. 3(a), (b). The operation is as follows.

1. $0 < t < \alpha\, T_s$, the capacitor is charged to a well defined voltage.
2. $\alpha T_s \leq t < \kappa T_s$, the capacitor is discharged through a variable resistor in such a way that the current through the resistor is held constant. In order to achieve a

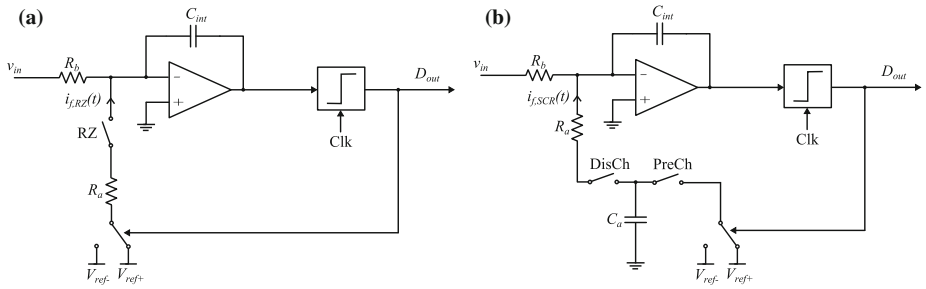

Fig. 1 CT delta-sigma modulators with **a** RZ-feedback, **b** SCR-feedback

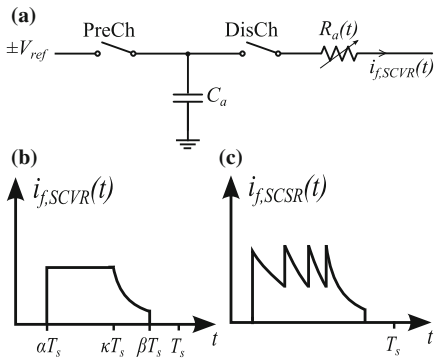

Fig. 3 SCVR and SCSR DAC concept. **a** SCVR circuit concept, **b** SCVR feedback current, **c** SCSR feedback current

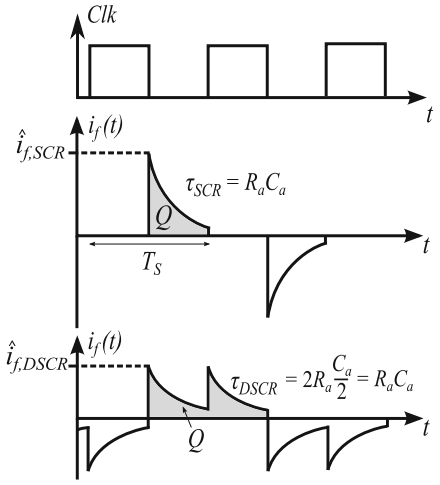

Fig. 4 SCR and DSCR feedbacks compared

constant current, the resistance must decrease in a linear fashion.

3. $\kappa T_s \leq t < \beta T_s$, the resistance is held constant and the discharge current decreases exponentially.

This technique is called switched-capacitor variable-resistor (SCVR) feedback.

A continuously variable resistance is not trivial to implement but it can be approximated by a resistance that changes its value in discrete steps. This is achieved, for example, by switching in and out resistors connected in parallel. If such resistor implementation is used in the DAC, the resulting feedback current can look like in Fig. 3(c). This technique is called switched-capacitor switched-resistor (SCSR) feedback.

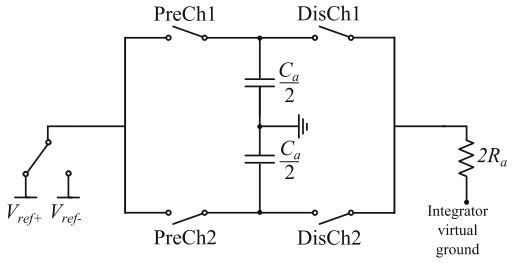

Fig. 5 DSCR circuit concept

Although SCSR feedback reduces the peak current, while still being relatively insensitive to clock jitter, it increases circuit complexity as additional circuits are needed to generate all control signals.

2 Dual-switched-capacitor-resistor (DSCR) feedback

Another method of reducing the peak current of an exponential pulse is to divide it into two identical units, while keeping the total charge the same as for a single pulse, see Fig 4.

This technique is proposed here and is called dual-switched-capacitor-resistor (DSCR) feedback. Compared to the SCR feedback, the same charge Q is distributed over two pulses and half of that charge spills in to the next clock period. The latter is not an issue if the technique is used in the outermost DAC of the feedback loop. If it is used in the succeeding DACs, an additional DAC might be required to compensate for the amount of charge extending into the next clock period.

The DSCR circuit concept is shown in Fig. 5. Two capacitors are required and they are alternately charged and discharged through a common resistor. Compared to SCR feedback, for the same time constant $\tau = R_aC_a$ and charge Q, each capacitor must be $C_a/2$ as it stores a charge of $Q/2$. In order to keep the same time constant, the resistor of the DSCR implementation must be doubled which reduces the peak current by half.

DSCR feedback exploits the clock period more efficiently than SCR feedback since the charge is transferred constantly without gaps. The circuit complexity is slightly increased since one additional capacitor and a couple of extra switches are required.

3 Design of the delta-sigma modulator

The DSCR feedback concept has been extended to the multi-bit case and used to implement the first DAC of a CT delta-sigma modulator. A block schematic of the

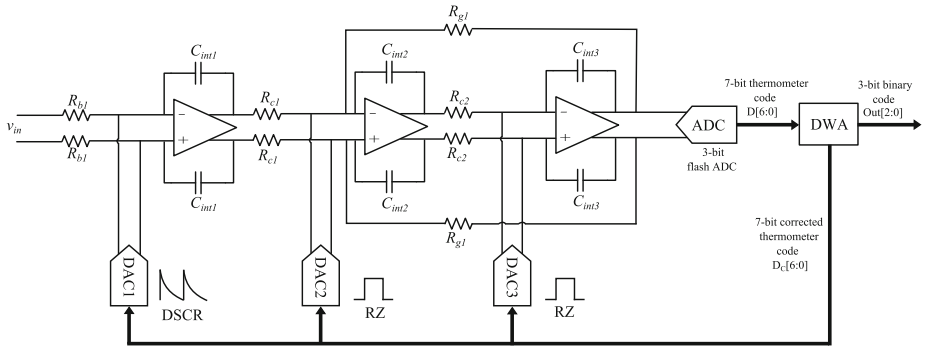

Fig. 6 Block schematic of the delta-sigma modulator

delta-sigma modulator is shown in Fig. 6. The loop filter was implemented with active RC integrators. The delta-sigma modulator also features a 3-bit flash ADC and a data weighted averaging (DWA) algorithm to correct for the mismatch in the DACs. In the following sections the system level design and the implementation of different blocks are described in more detail.

3.1 System level design

System simulations were initially performed in the DT domain using Schreier's toolbox [16]. The SQNR was chosen to 81 dB in order to have some margin and thereby meet the overall SNR target of 73 dB over a 125 kHz bandwidth. Since it was desirable to keep the oversampling ratio (OSR) at the low value of 16, a 3rd order loop filter with a 3-bit quantizer proved to be a suitable choice for the modulator architecture. The so-called CIFB architecture [17] was chosen for the loop filter and an additional feedback path was used to achieve zero optimization of the noise transfer function (NTF).

In order to obtain the CT feedback coefficients, DT-to-CT transformation has to be performed [3]. If the RC time constant of the DSCR pulse is expressed as a fraction of the sampling period, $\tau = \gamma T_s$, the CT coefficient in the outermost feedback path is given by

$$a_{1,DSCR} = \frac{1}{2\gamma(1 - e^{-\frac{1}{2\gamma}})} a_{1,DT} \tag{1}$$

where $a_{1,DT}$ is the DT coefficient. It can be shown that for an equivalent CT delta-sigma modulator with non-return-to-zero (NRZ) feedback, the first coefficient $a_{1,NRZ}$ equals the DT coefficient $a_{1,DT}$ [18]. Since NRZ feedback results in a lowest possible peak current for a CT implementation, (1) can be used to calculate how much $a_{1,DSCR}$ has to be increased compared to $a_{1,NRZ}$. Similarly, the peak current has to be increased by the same amount. The peak current is also dependent on the RC time constant (the parameter γ) and increases when the RC time constant is decreased. Consequently, there is a trade off between peak current and jitter sensitivity. In this design the RC time constant was chosen to $\tau = 0.16T_s$. The ratio between the coefficients, and thereby the peak currents, is $a_{1,DSCR}/a_{1,NRZ} = 3.27$.

RZ DACs were used in the two remaining feedback paths due to simpler implementation compared to the DSCR DAC. The high jitter sensitivity of the RZ DACs is not a primary issue, since any jitter further back in the modulator chain is at least first-order noise shaped. The RZ pulses were delayed a quarter of the clock period ($\alpha = 0.25$ and $\beta = 0.75$) Fig. 3, which ensures that the quantizer has fully processed the samples before they are converted by the DACs. RZ feedback is advantageous here over NRZ feedback since a delayed NRZ pulse would enter into the next clock period. To compensate for this, an extra feedback DAC might be required as well as an adjustment of the loop filter coefficients.

The overall timing of the delta-sigma modulator is shown in Fig. 7. All DACs are updated well after the beginning of the clock period, which ensures that the

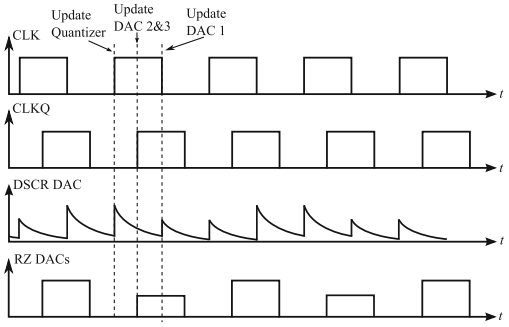

Fig. 7 Overall timing of the delta-sigma modulator

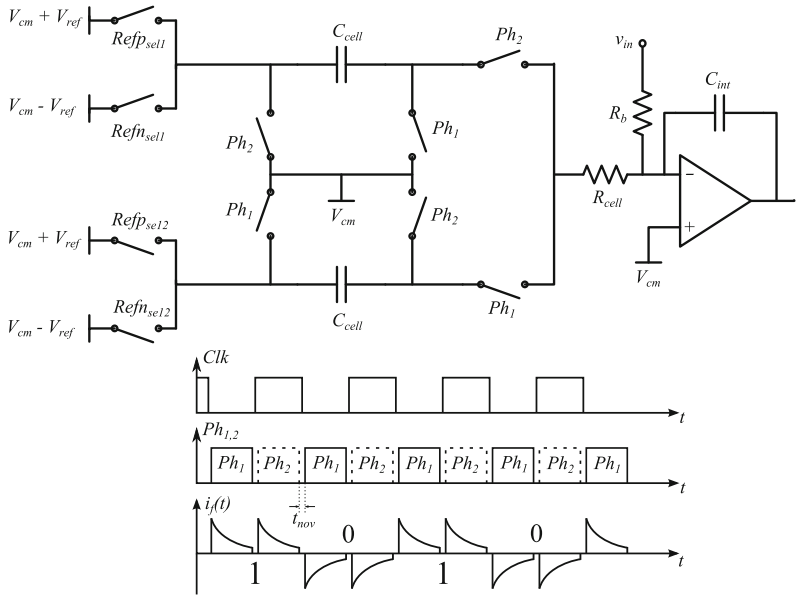

Fig. 8 Schematic and timing diagram of the DAC cell used for generation of DSCR pulses. The cell drives an active RC integrator

quantizer has processed the samples before they are converted to analog form. Since the RZ pulses are delayed by one quarter of clock period, a quadrature clock is required to clock the RZ DACs.

3.2 DACs

The implementation of a DAC cell generating dual exponential pulses is depicted in Fig. 8, where the single-ended version is shown for simplicity. It consists of parasitic insensitive switched-capacitor circuits to avoid any switch parasitic capacitances in parallel with the cell capacitance. The control signals $Refp_{sel1,2}$ and $Refn_{sel1,2}$ select either the positive or the negative reference, depending on whether the corresponding output bit from the quantizer is 1 or 0. A logic circuit is used to generate $Refp_{sel1,2}$ and $Refn_{sel1,2}$ from the clock phase signals $Ph_{1,2}$ and the quantizer output. The operation of the circuit is as follows: during Ph_1 the upper capacitor is charged either to V_{ref} or $-V_{ref}$ depending on the digital value from the quantizer. Simultaneously, the lower capacitor is discharged through the resistor, resulting in the first exponential current pulse which enters the virtual ground of the integrator. During Ph_2 the process is reversed as the upper capacitor is now discharged through the resistor, creating the second current pulse, while the lower capacitor is charged either to V_{ref} or $-V_{ref}$. The end result is a sequence of double exponential current pulses as shown in the timing diagram in Fig. 8. A finite non-overlap time t_{nov} between Ph_1 and Ph_2 is required to avoid short circuits through simultaneously closed switches.

The double exponential DAC concept can be extended to the multi-bit case by replicating the DSCR cell and connecting the replicas in parallel, see Fig. 9(a). Another possibility is to discharge all capacitors through a single resistor as shown in Fig. 9(b). In order to keep the same current as in Fig. 9(a), the value of the resistor must be reduced to $R_a/2^N$ (parallel connection of 2^N resistors with value R_a) where N is the number of bits in the DAC. Furthermore, since all capacitors are discharged through one resistor, the equivalent capacitance is a factor 2^N times the cell capacitance and the RC time constant is kept the same as in Fig. 9(a). Consequently, area is saved, as only one resistor with value $R_a/2^N$ is needed, compared to 2^N resistors with value R_a. Due to this advantage, the single-resistor architecture was used to implement the first DAC in the delta-sigma modulator.

Switched-resistor cells were used to realize the two RZ DACs (Fig. 10). Several switched-resistor cells were connected in parallel to implement a multi bit RZ DAC. Every cell is controlled by one of the thermometer coded output bits from the flash ADC. If the output bit is 1, the switches CP1 are closed and the switches CP2 are open. Positive and negative DAC references are connected to the positive and negative terminals of the operational amplifier in the integrator. If the output bit is 0, the switches CP2 are closed and the switches CP1 are open. The current from the

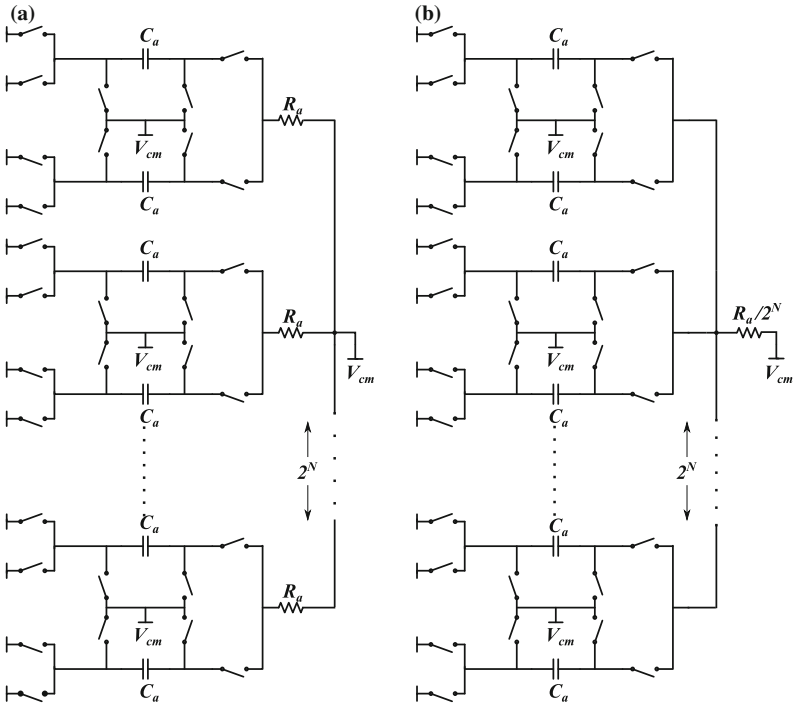

Fig. 9 Two equivalent implementations of the multi-bit DSCR DAC. **a** switched-capacitor cells with one resistor each. **b** switched-capacitor cells with a common resistor

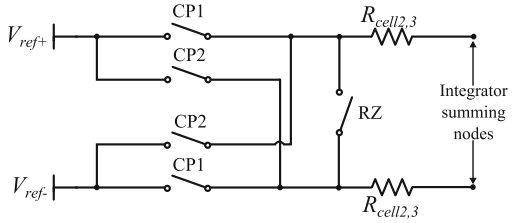

Fig. 10 Implementation of the switched-resistor RZ DAC cell

positive DAC reference is now steered into the negative terminal of the operational amplifier, and vice versa, creating the desired inversion.

An RZ switch is also required to short the input terminals of the operational amplifier after one half of the clock period. The resistors $R_{cell2,3}$ determine the amount of current to be fed back and thereby the feedback coefficient.

3.3 Thermal noise

Input referred thermal noise from the input resistors in the first integrator is the most dominant noise source as it is situated directly at the input. Thermal noise from the other integrators is attenuated by the gain in previous stage/stages when referred back to the input. For a targeted SNR of 73 dB over a 125 kHz bandwidth and a 200 mV input signal, the maximum total in-band noise is 10^{-9} V^2. In order to leave some margin for the less dominant noise sources from the other integrator resistors, integrator amplifiers and the DACs, the noise contribution from the input resistors was slightly less than 10^{-9} V^2.

As with all switched-capacitor circuits, thermal noise must be taken into account when designing DSCR multi-bit DACs. The overall thermal noise in switched capacitor circuits consists of both direct noise and sampled-and-held noise, i.e., kT/C noise. Before considering the noise contribution of a multi-bit DSCR DAC, it is feasible to analyse thermal noise of a simple SCR cell. In Fig. 11 the SCR cell is shown with the integrator during $Ph_1 = 1$ and $Ph_2 = 1$. All switch resistances are assumed to be equal. At the end of Ph_1, when the reference selection switch and the Ph_1 switch open, the sampled-and-held noise from both switches is stored on C_{cell}. The power spectral density (PSD) of the sample-and-held noise is given by [1]

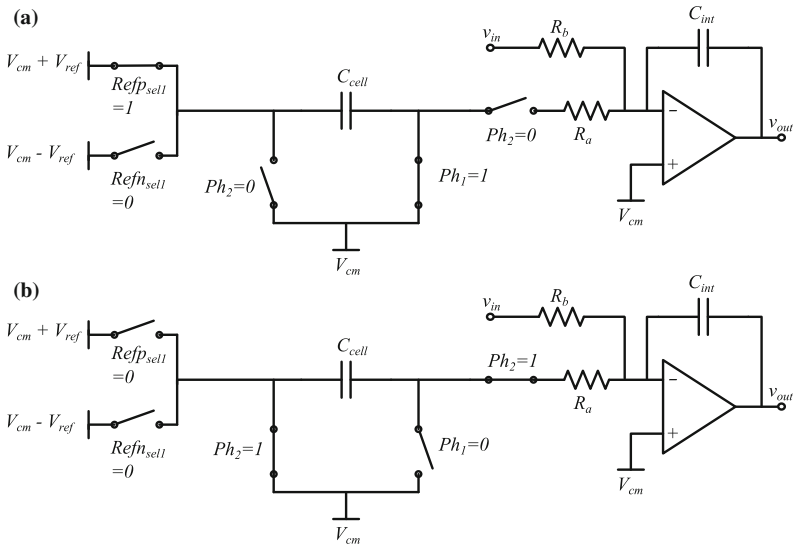

Fig. 11 SCR circuit during different clock phases. **a** Ph_1, **b** Ph_2

$$S_{SH}(f) = \frac{(1-D)^2}{f_s}\frac{2kT}{C_{cell}}\mathrm{sinc}^2\left(\frac{\pi(1-\mathrm{D})\mathrm{f}}{2\mathrm{f_{bw}OSR}}\right) \tag{2}$$

where D is the duty cycle of the control signal that turns the switches on and off, f_s is the sampling frequency, k is Boltzmann constant, T is the absolute temperature, f is the frequency variable, f_{bw} is the bandwidth and OSR is the oversampling ratio. This noise is then integrated during Ph_2.

The squared magnitude of the transfer function of the DT integrator formed by the switches, capacitors and the operational amplifier in Fig. 11 is [1]

$$|H_{DTint}(f)|^2 = \frac{(C_{cell}/C_{int})^2}{4\sin^2\left(\frac{\pi\mathrm{f}}{2\mathrm{f_{bw}OSR}}\right)}. \tag{3}$$

Both (2) and (3) can be simplified if a high OSR is assumed. Then the approximations $\sin(x) \approx x$ and $\mathrm{sinc}(x) \approx 1$ are valid. Using these approximations, the output referred sampled-and-held noise PSD is calculated as

$$\begin{aligned} S_{SHout}(f) &= |H_{DTint}(f)|^2 S_{SH}(f) \\ &= \frac{kT(1-D)^2 C_{cell} f_s}{2(\pi f C_{int})^2}. \end{aligned} \tag{4}$$

The direct noise component is due to the feedback resistor R_a and Ph_2 switches and is present during Ph_2. Fig. 12 shows the simplified circuit during Ph_2 and is used to calculate the direct noise component. The two switch resistances R_{sw} have been included into the total resistance R_{tot} with a noise spectral density $S_{tot}(f) = 4kTR_{tot}$. The

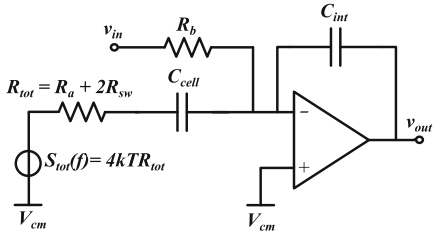

Fig. 12 Simplified SCR circuit during Ph_2

thermal noise of R_{tot} is transferred to the integrator output by the following transfer function

$$H_{CTint1}(f) = -\frac{C_{cell}}{C_{int}}\frac{1}{1+j2\pi f R_{tot} C_{cell}}. \tag{5}$$

The output referred direct noise PSD is obtained as

$$\begin{aligned} S_{Dout}(f) &= |H_{CTint1}(f)|^2 S_{tot}(f) \\ &= \left(\frac{C_{cell}}{C_{int}}\right)^2 \frac{4kTR_{tot}}{1+(2\pi f R_{tot} C_{cell})^2}. \end{aligned} \tag{6}$$

It is of interest to refer both the sampled-and-held noise and the direct noise to the input of the integrator. This is achieved by dividing the PSDs in (4) and (6) by the squared magnitude of the integrator transfer function which is given by

$$H_{CTint2}(f) = -\frac{1}{j2\pi f R_b C_{int}}. \quad (7)$$

After performing the calculations, the following expressions for the input referred sampled-and-held and direct noise PSDs are obtained

$$S_{SHin}(f) = 2kT(1-D)^2 R_b^2 C_{cell} f_s \quad (8)$$

$$S_{Din}(f) = \frac{(2\pi f R_b C_{cell})^2 4kTR_{tot}}{1+(2\pi f R_{tot} C_{cell})^2}. \quad (9)$$

The sampled-and-held noise PSD in (8) is in agreement with the result obtained in [19]. The input referred noise power is obtained by integrating (8) and (9) from dc up to the signal bandwidth f_{bw}

$$\overline{v}_{SHin}^2 = 4kT(1-D)^2 R_b^2 C_{cell} f_s f_{bw} \quad (10)$$

$$\overline{v}_{Din}^2 = \frac{DR_b^2 kT}{R_{cell}}\left(f_{bw} - \frac{\arctan(2\pi R_{tot} C_{cell} f_{bw})}{2\pi R_{tot} C_{cell}}\right). \quad (11)$$

Since both half circuits in a DSCR cell generate noise, the contributions in (10) and (11) are doubled. However, the total noise is the same for equivalent DSCR and SCR cells since the capacitor in a DSCR cell is halved (Figs. 4, 5). Additionally, in a multi-bit DSCR DAC, the equivalent capacitance is $2^N C_{cell}$, which also has to be substituted into the expressions.

From (10) and (11), it is obvious that the input-referred noise can be reduced by scaling down the capacitor. This is in contrast to plain kT/C noise, where the capacitor needs to be maximized to minimize noise. Furthermore, noise is also dependent on the input resistor of the integrator.

The capacitor size in a DSCR DAC is restricted by different design constraints and cannot be made excessively small. Choosing the minimum practical capacitor value can help making the input-referred noise non-dominant, but it might also jeopardize matching between the unit components in the DACs. Consequently, there is a design trade-off involved between noise and matching. The capacitance value can be minimized by maximizing V_{ref}, which is limited by the supply voltage [20]. For $V_{ref} = V_{dd}/2$, minimum capacitance and thereby minimum input-referred noise is achieved. The feedback resistor is simultaneously maximized and reduces the impact of the non-linear switch resistance during capacitor discharge.

The capacitance in the DSCR DAC was set to $C_{cell} = 165$ fF with V_{ref} set to $V_{dd}/2$. Finally, the input-referred direct and sampled-and-held noise are calculated to $\overline{v}_{D,DSCR}^2 = 1.1 \cdot 10^{-13}\, V^2$ and $\overline{v}_{S,DSCR}^2 = 1.35 \cdot 10^{-11}\, V^2$. Compared to the maximum total in-band noise for a 73 dB SNR target, which was calculated to 10^{-9} V^2 before, the input referred noise from the DSCR DAC is not dominant and can be neglected.

3.4 The amplifiers and the quantizer

All RC-integrators were implemented using a folded cascode amplifier as shown in Fig. 13. The amplifier achieves a dc gain of 74 dB and a gain bandwidth product of 62 MHz while consuming 135 μA. Both transistors in the input pair operate in weak inversion. According to the simulations, the transistors in the input pair and in the bottom pair of the cascode are the main contributors of flicker noise. The lengths of these transistors were increased to reduce the flicker noise sufficiently enough to not dominate over the overall thermal noise of the modulator.

The common mode feedback circuit consists of a differential stage with common mode sensing resistors and source followers to buffer the amplifier outputs. The high input impedance of a source follower keeps the output impedance of the amplifier high and the dc gain is relatively unaffected. In order to handle the dc shift introduced

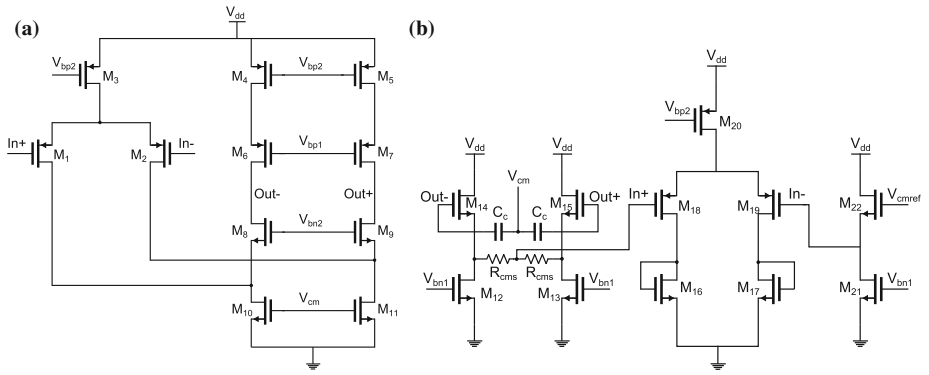

Fig. 13 Integrator amplifier. **a** Main amplifier circuit, **b** common mode feedback

by a source follower, an identical stage is inserted between the common mode reference and the negative input to the differential stage.

The 3-bit flash ADC was realized with a resistor ladder and regenerative latch comparators without pre amplifiers.

4 Measurement results

The delta-sigma modulator has been fabricated in a 65 nm CMOS process and tested. Fig. 14 shows the die photo of the modulator, which occupies an active area of 0.17 mm^2. The circuit is powered by a 900 mV supply and the total power consumption is 380 µW. The maximum differential input signal is 200 mV. An audio precision instrument was used to generate a clean input signal during measurements. An I/Q modulation generator was used to generate a clean and stable sinusoidal clock signal which was buffered on chip.

The measured output spectrum of the delta-sigma modulator is shown in Fig. 15 for an input signal amplitude of −2.5 dBFS. If the DWA algorithm is inactivated, a second order harmonic at −73 dBFS appears in the spectrum, Fig. 16. This shows that the DWA algorithm successfully corrects for the mismatch errors in the DAC unit elements.

A graph of SNR/SNDR vs. the input signal amplitude is shown in Fig. 17. The modulator achieves a maximum SNR of 74 dB for an input signal of −1.7 dBFS, and a maximum SNDR of 70 dB for an input signal of −2.5 dBFS.

The CT modulator provides an inherent anti aliasing filtering which is advantageous for low power radios as the anti aliasing filter can either be removed or simplified. The anti aliasing performance of the delta sigma modulator was measured by applying a large signal around the sampling

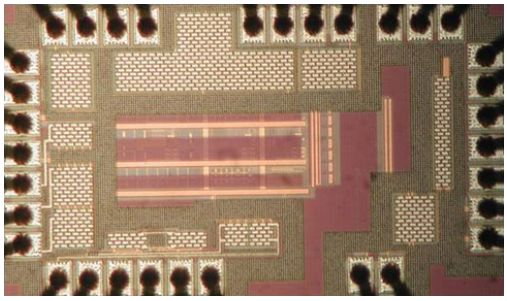

Fig. 14 Chip photo

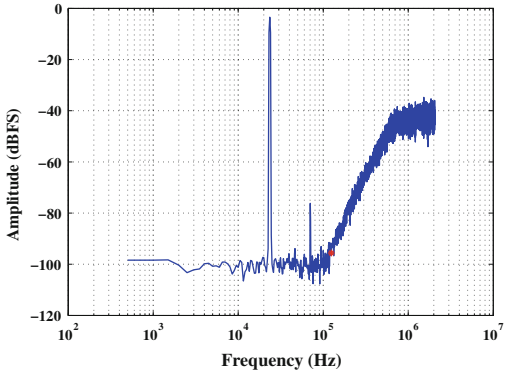

Fig. 15 Measured output spectrum, 8,192 point FFT with a Hann window averaged four times

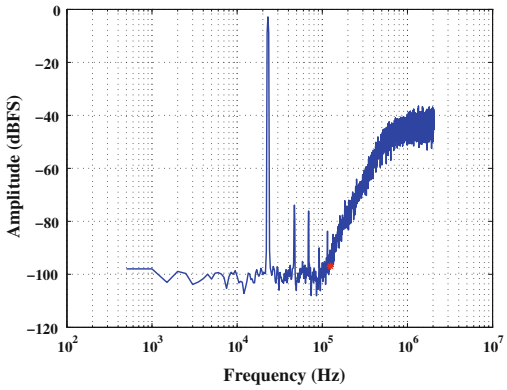

Fig. 16 Measured output spectrum with DWA turned off, 8,192 point FFT with a Hann window averaged four times

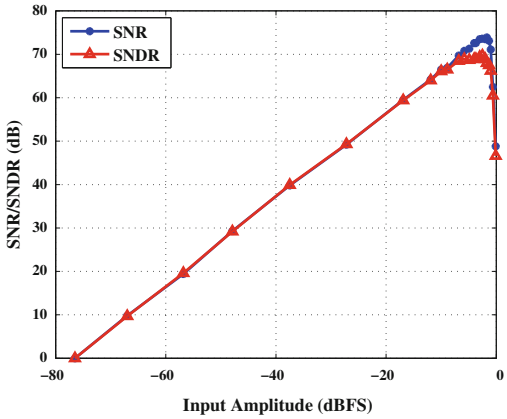

Fig. 17 Measured SNR and SNDR vs. input amplitude

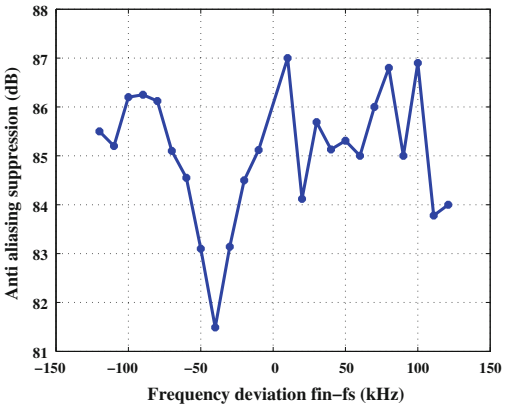

Fig. 18 Measured anti aliasing suppression around the sampling frequency

Table 1 Performance comparison

Reference	Process (μm)	Supply voltage (V)	BW (kHz)	SNDR (dB)	Power (μW)	FOM (pJ/ Conv)
[14]	0.18	1.8	24	89	122	0.2
[21]	0.5	1.5	25	60	250	12.3
[22]	0.5	2.2	3.4	80	200	7.2
[23]	0.5	1.5	25	70	135	2.1
[24]	0.13	1.2	20,000	63.9	58,000	2.3
This work	0.065	0.9	125	70	380	1.2

frequency and observing at which frequency the aliased and filtered version of the signal will appear. The frequency of the input signal was swept from $f_s - f_{bw}$ and $f_s + f_{bw}$ since all frequencies in this range will fold in band. If the amplitude of the input signal is known, the anti aliasing suppression can be calculated which is defined as the ratio between the input signal amplitude and the amplitude of the aliased signal. The measured anti aliasing suppression is shown in Fig. 18. It stays above 80 dB throughout the entire frequency interval.

The performance summary and comparison to previous work is shown in (Table 1).

5 Conclusions

This paper has presented a CT ΔΣ modulator with a DSCR multi-bit DAC. By dividing the exponential feedback pulse into several identical unit pulses, the peak current and thereby the operational amplifier slew-rate requirement are reduced, while the DAC is still insensitive to clock jitter. The technique has been tested in a 65 nm CMOS 3rd-order 3-bit CT ΔΣ modulator, achieving a peak SNR of 74 dB and a peak SNDR of 70 dB while consuming 380 μW.

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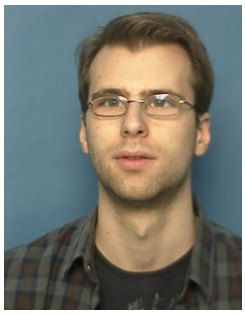

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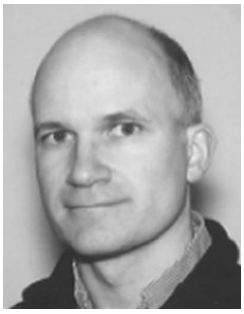

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Paper III

Paper III

A Low-Power 2nd-order CT $\Delta\Sigma$ Modulator with a Single Operational Amplifier

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A Low-Power 2nd-order CT $\Delta\Sigma$ Modulator with a Single Operational Amplifier

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***Abstract*—This paper presents a multi-bit continuous-time $\Delta\Sigma$ modulator intended for ultra low power radios. The modulator features a 2nd order loop filter implemented with a single operational amplifier to reduce the power consumption. Furthermore, a 4-bit quantizer is used to achieve high resolution at a low oversampling ratio of 16.**

The $\Delta\Sigma$ modulator has been implemented in a 65nm CMOS process. Simulation results show a peak SNDR of 65 dB over a 500 kHz signal bandwidth, while consuming 76 μW from a 800 mV power supply.

I. Introduction

In today's rapidly growing market of portable electronic devices, the development of low-power and low-voltage circuit design techniques is of great importance. Low power consumption is necessary in order to extend the battery life as much as possible and to avoid frequent battery replacement. This is especially important in medical implant devices such as pacemakers. Among the different parts of a low power electronic system, the highest power consumers are still analog and mixed signal blocks. An analog-to-digital converter (ADC) is such a block which is unavoidable due to the interface between analog and digital signals.

$\Delta\Sigma$ modulators have been widely used to implement ADCs, since they are highly insensitive to circuit imperfections such as device mismatch. Continuous-time (CT) $\Delta\Sigma$ modulators, in particular, are of interest for low power applications due to their low power consumption and inherent anti aliasing [1]. The loop filter in a CT $\Delta\Sigma$ modulator is usually designed by using feedback (CIFB) or feedforward (CIFF) structures [2]. Both architectures are usually implemented with active-RC integrators, since a high linearity can be achieved due to the use of negative feedback. This makes the loop filter the largest power consumer in a $\Delta\Sigma$ modulator. Since the number of integrators is usually equal to the order of the loop filter, the power consumption can be reduced by decreasing the order at the expense of decreased resolution. Another alternative, which is described in this paper, is to keep the desired order and reduce the number of amplifiers by using alternative implementations of the loop filter. This has been investigated by several authors, e.g. [3]-[5]. In this paper, an approach similar to [5] has been adopted by implementing a CT $\Delta\Sigma$ modulator with a 2nd-order loop filter using a single operational amplifier. The method presented here can implement a broad range of feedback coefficients. Furthermore, additional simulation results are presented which can be used to systematically design $\Delta\Sigma$ modulators with this type of loop filter.

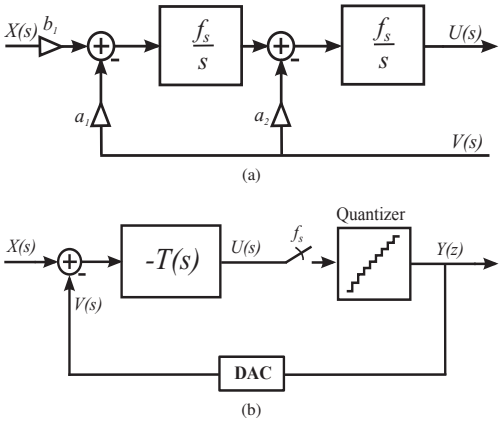

Figure 1: Block diagrams of (a) a 2nd order CIFB loop filter, (b) a CT $\Delta\Sigma$ modulator.

The paper is organized as follows: Section II describes the theory and implementation of the single operational amplifier loop filter. Section III gives details about the overall implementation of the $\Delta\Sigma$ modulator. Section IV presents the simulation results. Section V concludes the paper.

II. Loop filter implementation

The block diagram of a 2nd order loop filter implemented with the CIFB structure is shown in Fig. 1(a). The feedback transfer function from $V(s)$ to $U(s)$ is given by

$$T(s) = -\frac{a_1 + a_2 s T_s}{(sT_s)^2} \tag{1}$$

where T_s is the sampling period and a_1, a_2 are the feedback coefficients. The feedback transfer function determines the noise transfer function (NTF) of the $\Delta\Sigma$ modulator. The main objective of this work is to lump the CIFB architecture into an active network consisting of one active element and a 2nd order passive RC network and implementing the same transfer function as in (1). Furthermore, when the active network is

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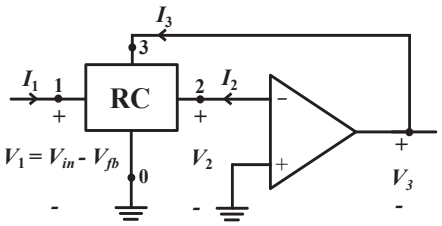

Figure 2: General single operational amplifier network.

used in a CT $\Delta\Sigma$ modulator, Fig. 1(b), it should implement the same NTF as an equivalent CIFB loop filter. This is not achievable with conventional 2nd order single amplifier filters, for example the Sallen-Key filter, since their transfer functions are not of the same form as (1). Instead, the passive RC network needs to be customly designed from the given transfer function.

A general single amplifier active network is shown in Fig. 2. The 4-terminal RC-network can be fully characterized by its short-circuit admittances. Assuming an ideal amplifier with infinite gain, it can be shown that the transfer function of the network is [6]

$$T(s) = \frac{V_3}{V_1} = -\frac{y_{12}(s)}{y_{32}(s)} \tag{2}$$

where $y_{12}(s)$ and $y_{32}(s)$ are the short circuit admittances defined as

$$y_{12}(s) = \left.\frac{I_1}{V_2}\right|_{V_1,V_3=0}, \qquad y_{32}(s) = \left.\frac{I_3}{V_2}\right|_{V_1,V_3=0}. \tag{3}$$

When used in the $\Delta\Sigma$ modulator, Fig. 1(b), the input signal to the network is the difference between the input signal to the modulator and the feedback signal.

The remaining task is to synthesize the RC network which results in the transfer function in (1). Implementation of the addition operator in Fig. 1(b) is also necessary, and will be discussed later.

A. Synthesis of the RC-network

The 4-terminal RC network used to implement the desired transfer function is shown in Fig. 3. All resistors are expressed in terms of a common resistance R and the parameters n_1 and n_2. These parameters are used to size the resistors and thereby implement the desired feedback coefficients. External nodes 1 and 3 have been shorted to find the short circuit admittances $y_{12}(s)$ and $y_{32}(s)$. Using (2) and (3), it can be shown that the transfer function of the loop filter is

$$T(s) = -\frac{\frac{1}{n_2^2}\left(1+\frac{n_2}{n_1}\right)+\frac{3}{n_2}sRC}{(sRC)^2}. \tag{4}$$

This equation is of the same form as (1), where the time constant RC equals the sampling period T_s. The feedback

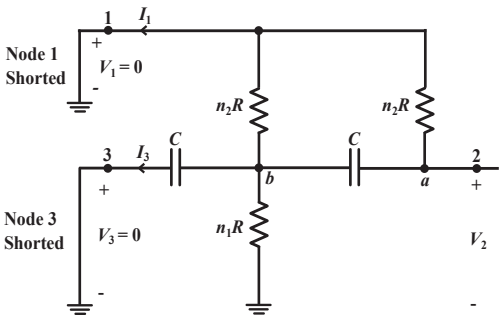

Figure 3: 4-terminal RC-network used in the loop filter.

coefficients a_1 and a_2 can be identified by comparing the numerators in (1) and (4):

$$\begin{cases} a_1 = \dfrac{1}{n_2^2}\left(1+\dfrac{n_2}{n_1}\right) \\ a_2 = \dfrac{3}{n_2} \end{cases} \quad \Longrightarrow \quad \begin{cases} n_1 = \dfrac{3a_2}{9a_1 - a_2^2} \\ n_2 = \dfrac{3}{a_2} \end{cases}. \tag{5}$$

For any given values of the feedback coefficients, the equations in (5) can be used to find the correct parameters n_1 and n_2.

B. Implementation of the addition operator

So far it has been assumed that the difference between the input and the feedback signal has been provided. This situation is shown in Fig. 4(a), where the RC-network in Fig. 3 is excited by the voltage $V_{in} - V_{fb}$ at node 1. Using Thévenin's theorem, the circuit can be transformed to the one shown in Fig. 4(b). The transformation enables the input signal to the modulator and the feedback signal to be applied separately to the network. However, the voltages V_{in} and V_{fb} are multiplied by a factor of 2 which needs to be implemented if the circuits in Fig. 4(a) and Fig. 4(b) are to realize the same transfer function. The first step towards avoiding the multiplication factor is to transform the circuit again according to Fig. 4(c). In this case the voltages are applied to the left sub circuit without any multiplication while the resistor values have been changed. Furthermore, by dividing all the resistor values and voltages in the right sub circuit by 2, the multiplication factor is avoided and two identical feedback DACs can be used as the resistors connected to the feedback paths will be identical. Although this circuit is not equivalent to the ones in Fig. 4(a)-(c), it can still be shown that it will implement the same transfer function as in (4) after the cancellation of the common polynomials in the admittances $y_{12}(s)$ and $y_{32}(s)$.

III. System design and circuit implementation

The single operational amplifier loop filter has been used in a CT $\Delta\Sigma$ modulator intended for wireless ultra-low-power portable devices. System simulations in the discrete-time domain resulted in an adequate SQNR of 70 dB to meet the overall SNR target of 60 dB over a 500 kHz bandwidth. In order to achieve the targeted SNR, while keeping the sampling

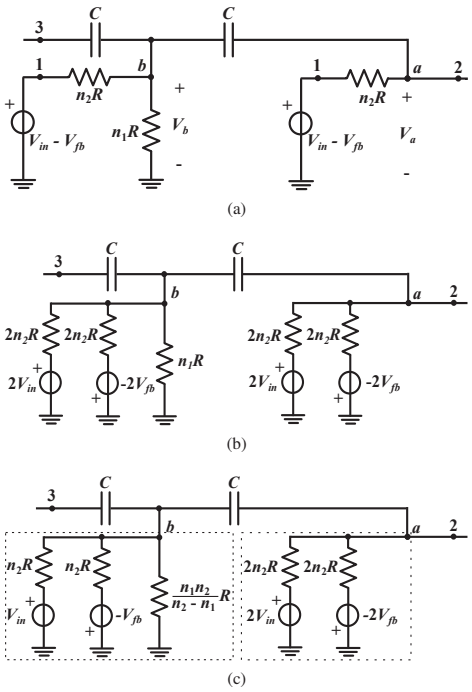

Figure 4: (a) RC-network with voltage $V_{in} - V_{fb}$ provided. (b) First transformation of the circuit in (a). (c) Second transformation of the circuit in (a).

frequency as low as possible, a 4-bit quantizer was used. This choice together with a 2nd order loop filter resulted in a sampling frequency of 16 MHz and an oversampling ratio (OSR) of 16.

The block schematic of the modulator is shown in Fig. 5. A DWA algorithm is used after the 4-bit flash quantizer to improve linearity of the DACs. Resistive DACs are used in the feedback due to better noise performance compared to current steering DACs [7]. Since the output of the DWA is thermometer coded, a 4-bit feedback DAC must use 15 switched resistor unit cells. Delayed return-to-zero (RZ) pulses are used in the feedback in order to ensure that the quantizer has fully processed the samples before they are converted by the DACs. The pulses are delayed by a quarter of the clock period ($\alpha = 0.25$ and $\beta = 0.75$) in Fig. 5. RZ feedback is advantageous here over non-return-to-zero (NRZ) feedback which would require an additional DAC and summing operation to compensate for the excess loop delay [8]. The high jitter sensitivity of RZ pulses is not a serious issue due to the low sampling frequency.

Discrete-to-continuous time (DT-CT) conversion [8], [9] with RZ feedback yields the following values for the feedback coefficients: $a_1 = 2$, $a_2 = 3$. Using the equations in (5), the following sizing factors are obtained: $n_1 = n_2 = 1$. This is a special case, since the expression for the resistor between node b and ground in Fig. 4(c) approaches infinity. This indicates that the resistor is not needed. Since $n_2 = 1$, all the remaining resistors will have a value of R as shown in Fig. 5.

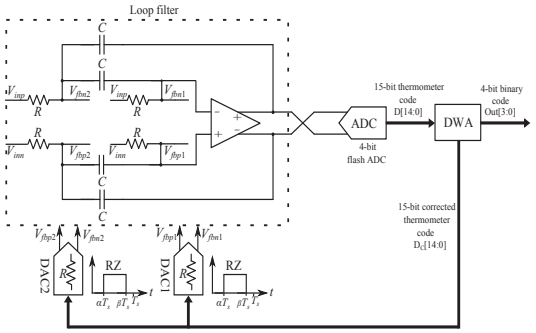

Figure 5: Block schematic of the $\Delta\Sigma$ modulator.

A. System simulations

In order to study the effects of circuit non-idealities such as finite amplifier DC-gain and unity gain bandwidth, a simple amplifier model with a transconductance, output resistance and output capacitance was built in Cadence. The output resistance was set to 130 kΩ which was the typical value that could be obtained from a common source stage when used as the output stage of the operational amplifier. By sweeping the other two parameters, it was possible to study the effects of finite DC-gain and unity gain bandwidth.

Fig. 6 shows SNR vs. DC-gain for different values of the common resistance R in the loop filter. Thermal noise from all resistors was included in the simulations. It is evident from these results that the performance for lower DC-gains deteriorates when R decreases. This is due to the fact that the feedback network loads the amplifier more for smaller values of R, and therefore a larger transconductance is required to compensate for the loading effect. The upper limit of R is determined by thermal noise and resistor area. Since the resistance of a unit cell in a 4-bit resistive DAC must be 15 times larger than the parallel resistance of all cells, the area can become an issue for large values of R.

Based on a trade off between the above mentioned limitations, R was set to 15 kΩ. Substituting the value for R in the expression for the sampling period, $T_s = RC$, and solving for C, yields C = 4.17 pF. According to the graph for $R = 15$ kΩ in Fig. 6, a gain of at least 200 is required to keep the maximum possible SNR.

Fig. 7 shows SNR vs. unity gain bandwidth for $R = 15$ kΩ. These results show that a unity gain bandwidth of at least 70 MHz is required to keep the SNR degradation to 1 dB.

B. Design of the operational amplifier

The operational amplifier was implemented using the two stage Miller architecture. Two stage architectures are more

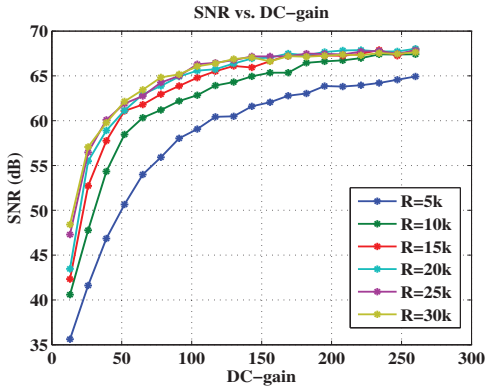

Figure 6: Simulated SNR vs. gain for different values of R.

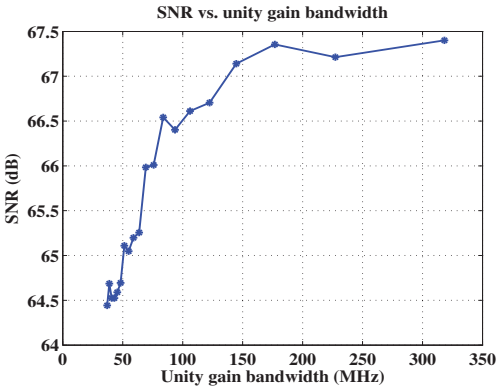

Figure 7: Simulated SNR vs. unity gain bandwidth.

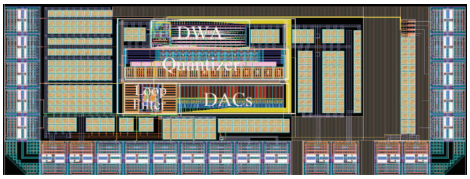

Figure 8: Layout.

suitable for low supply voltages than single stage architectures since the gain is achieved by cascading stages instead of transistor stacking which limits the voltage headroom. The operational amplifier consumes 43 μW with a DC-gain of 62 dB and a unity gain bandwidth of 90 MHz. The latter requirement sets the power consumption.

IV. Simulation Results

The $\Delta\Sigma$ modulator has been implemented in a 65 nm CMOS process and simulated. The chip is currently under fabrication. Fig. 8 shows the layout where the modulator

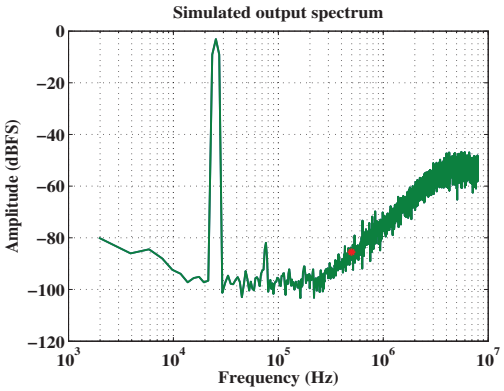

Figure 9: Simulated output spectrum, 8192 point FFT with a Hann window averaged 4 times.

occupies an active area of 0.08 mm^2. The circuit is powered by a 800 mV supply and the total power consumption is 76 μW. The maximum differential input signal is 200 mV. Fig. 9 shows the output spectrum for an input signal amplitude of -3 dBFS including thermal noise. The modulator achieves a maximum SNDR of 65 dB over a 500 kHz bandwidth. This results in a figure of merit of 52 fJ/conv.

V. Conclusions

This paper has presented a CT $\Delta\Sigma$ modulator with a 2nd order single operational amplifier loop filter. The main objective of the loop filter is to reduce the number of active elements while still achieving a 2nd order noise shaping. The concept has been implemented in a 65nm CMOS 2nd-order 4-bit CT $\Delta\Sigma$ modulator, achieving a peak SNDR of 65 dB while consuming only 76 μW.

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Paper IV

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A Low-Power 2nd-order CT Delta-Sigma Modulator with a Single Operational Amplifier

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A low-power 2nd-order CT delta-sigma modulator with a single operational amplifier

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Abstract We present a 2nd-order 4-bit continuous-time (CT) delta-sigma modulator (DSM) employing a 2nd-order loop filter with a single operational amplifier. This choice strongly reduces the power consumption, since operational amplifiers are the most power hungry blocks in the DSM. The DSM has been implemented in a 65 nm CMOS process, where it occupies an area of 0.08 mm^2. It achieves an SNDR of 64 dB over a 500 kHz signal bandwidth with an oversampling ratio of 16. The power consumption is 76 μW from a 800 mV power supply. The DSM figure-of-merit is 59 fJ/conversion. The CT DSM is well suited for the receiver of an ultra-low-power radio.

Keywords Delta-Sigma · Single-operational-amplifier · Low-power · Continuous time · RC loop filter

1 Introduction

In today's rapidly growing market of portable electronic devices, the development of low-power and low-voltage circuit design techniques is of great importance. Low power consumption is necessary to extend the battery life as much as possible and to avoid frequent battery replacement. Among the different parts of a low power electronic system, the highest power consumers are still analog and mixed-signal blocks. An analog-to-digital converter (ADC) is such a block, and one having a fundamental importance due to the required interface between the analog and digital domains.

Delta-sigma modulators (DSMs) have been widely used to implement ADCs, since they are highly insensitive to circuit imperfections such as device mismatch. Continuous-time (CT) DSMs, in particular, are of interest for low-power applications, due to their low power consumption and inherent anti aliasing [1]. The loop filter in a CT DSM is usually designed by using cascaded integrator feedback (CIFB) or feedforward (CIFF) structures [2]. Both architectures are usually implemented with active-RC integrators, since a high linearity can be achieved with the use of negative feedback. This makes the loop filter the largest power consumer in a DSM. Since the number of integrators is usually equal to the order of the loop filter, the power consumption can be reduced by decreasing the order at the expense of a less aggressive noise shaping. Another possibility, which is described in this paper, is to keep the desired filter order and reduce the number of amplifiers by using alternative implementations of the loop filter. This has been investigated in several works, e.g. [3]–[6]. These loop filters are of the feedforward type, which usually cause an amount of peaking in the signal transfer function (STF) of the DSM. Thus, if the DSM is used in a radio receiver, the presence of possible interfering signals at the same frequencies where the STF peaks would result in a deteriorated dynamic range for the receiver. Because of this issue, a CIFB DSM is preferred for such applications [7]. In this paper, an approach similar to [6] has been adopted, by implementing a CT DSM with a 2nd-order loop filter using a single operational amplifier and a feedback architecture.

This paper is organized as follows: Sect. 2 discusses CT DSMs with single-amplifier loop filters in general and gives an overview of previous work. Sect. 3 presents

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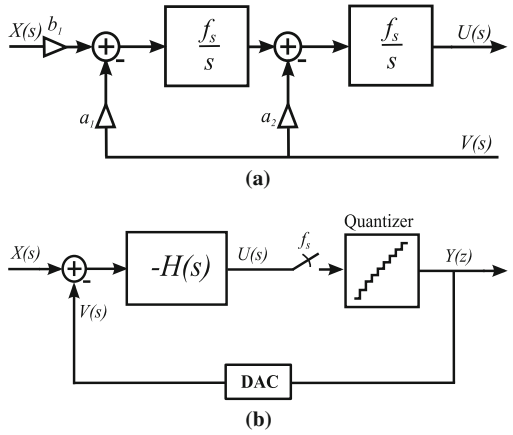

Fig. 1 Block diagrams of **a** a 2nd-order CIFB loop filter, **b** a CT DSM modulator

theory and implementation details of the single-amplifier loop filter in this work. In Sect. 4, the effects of amplifier non-idealities on the loop filter transfer function are discussed. Section 5 describes system level design and circuit implementation of the DSM. Section 6 presents the measurement results of the fabricated chip. The paper is concluded in Sect. 7.

2 CT DSMs with single-amplifier loop filters

The block diagram of a 2nd-order loop filter implemented with the CIFB structure is shown in Fig. 1(a). The feedback transfer function from $V(s)$ to $U(s)$ is given by

$$H(s) = -\frac{a_1 + a_2 T_s s}{(T_s s)^2} \tag{1}$$

where T_s is the sampling period and a_1, a_2 are the feedback coefficients. The feedback transfer function determines the noise transfer function (NTF) of the DSM. The main objective of this work is to lump the CIFB architecture into an active network consisting of one active element and a 2nd-order passive RC network, while implementing the same transfer function as in (1). Furthermore, when the active network is used in a CT DSM, Fig. 1(b), it should implement the same NTF as an equivalent CIFB loop filter. This is not achievable with conventional 2nd-order single-amplifier filters, such as the well-known Sallen-Key filter, since their transfer functions are not of the same form as (1). Instead, the passive RC network needs to be custom-designed starting from the desired transfer function.

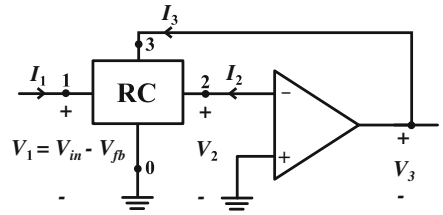

Fig. 2 General single-amplifier network

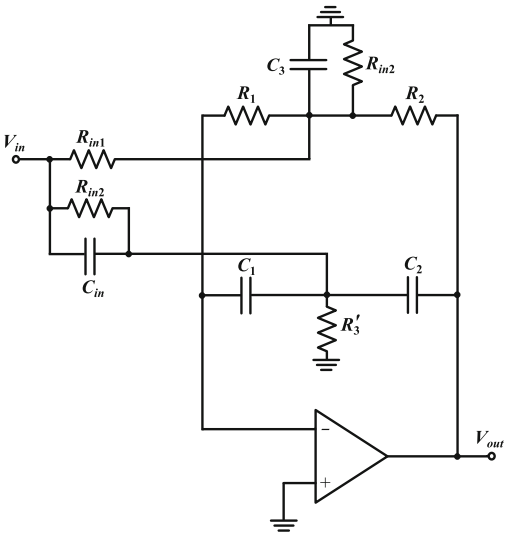

Fig. 3 Single-amplifier resonator proposed in [3]

2.1 General single-amplifier network

A general single-amplifier active network is shown in Fig. 2. The 4-terminal RC network can be fully characterized by its short-circuit admittances. Assuming an ideal amplifier with infinite gain, it can be shown that the transfer function of the network is [8]

$$H(s) = \frac{V_3}{V_1} = -\frac{y_{12}(s)}{y_{32}(s)} \tag{2}$$

where $y_{12}(s)$ and $y_{32}(s)$ are the short circuit admittances defined as

$$y_{12}(s) = \left.\frac{I_1}{V_2}\right|_{V_1, V_3 = 0}, \qquad y_{32}(s) = \left.\frac{I_3}{V_2}\right|_{V_1, V_3 = 0}. \tag{3}$$

When used in the DSM of Fig. 1(b), the input signal to the network is the difference between the input signal to the modulator and the feedback signal.

The task is now to synthesize the RC network which results in the transfer function in (1). Implementation of the addition operator in Fig. 1(b) is also necessary, and will be discussed later. Next subsection presents previously published single-amplifier networks.

2.2 Previous work

The single-amplifier resonator (SAR) shown in Fig. 3 has been developed in [3] and used in a 5th-order DSM. The transfer function is of 3rd-order in general. If the resonating conditions $R_3'||R_{in2} = R_1||R_2||R_{in2}||R_{in1}$ and $C_3 = C_1 + C_2 + C_{in}$ are fulfilled, it reduces to a 2nd-order transfer function given by

$$H(s) = -\frac{\frac{C_{in}}{C_2}s^2 + \frac{1}{R_{in2}C_2}s + \frac{1}{R_1R_{in1}C_1C_2}}{s^2 + \frac{1}{R_1R_2C_1C_2}}. \quad (4)$$

Contrary to (1), which has two poles at the origin, the poles of the SAR transfer function are situated at the imaginary axis resulting in a resonant transfer function which can be used to implement a zero-optimized NTF. Compared to a conventional resonator with two integrators, only one operational amplifier is used, which helps to reduce the power consumption. The disadvantage of this SAR is that it cannot be used at the front-end of the DSM, since the input signal is not applied at virtual ground. Consequently, the feedback signal from the DAC cannot be subtracted from the input, as required to implement the addition operator in Fig. 1(b). However, implementations of loop filters of higher order than two are possible if the SAR is preceded by at least one integrator.

To avoid the above mentioned disadvantage, the SAR in Fig. 4 has been proposed in [4]. The positive feedback path through R_4 results in the following resonating 2nd-order transfer function if the resonating condition $R_3C_1 = R_4(C_1 + C_2)$ is fulfilled:

$$H(s) = -\frac{1}{R_1C_1C_2}\frac{(C_1 + C_2)s + \left(\frac{1}{R_2} + \frac{1}{R_4}\right)}{s^2 + \frac{1}{R_3C_1C_2}\left(\frac{1}{R_2} + \frac{1}{R_4}\right)}. \quad (5)$$

The SAR can also be modified to implement the transfer functions with both poles at the origin. By removing the positive feedback path (R_4 and the inversion) and the resistor R_3, the transfer function will be of the same form as (1). The poles will end up at the origin which can be seen from (5) by letting R_3 approach infinity. This version of the single-amplifier network has been developed in [5], where it was also extended to a 3rd-order transfer function. It was also used at the front-end of the 4th-order DSM in [4].

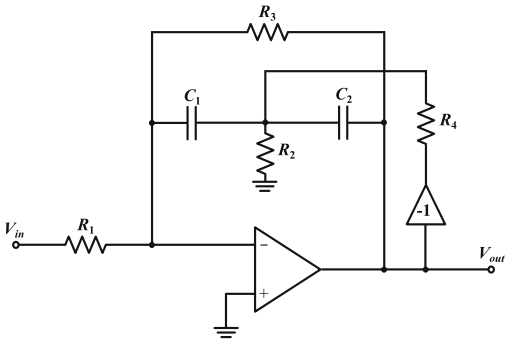

Fig. 4 Single-amplifier resonator proposed in [4]

3 Loop filter implementation

In this work, the approach similar to [6] has been adopted for a 2nd-order single-amplifier loop filter. In [6] a 3rd-order single-amplifier loop filter has been presented. However, the method used in [6] can only implement a limited range of loop filter coefficients, and is not suitable for commonly used values of loop filter coefficients in a 2nd-order DSM. Due to this reason, another method is introduced here to enable the implementation of a broad range of feedback coefficients for 2nd-order DSMs. Furthermore, details about the synthesis of the 2nd-order passive RC network are presented. Contrary to [3] and [4], the loop filter in this work mimics the CIFB architecture as the number of feedback branches is equal to the order of the loop filter.

3.1 Synthesis of the RC network

The denominator in (1) contains the term $(T_s s)^2$, which is the transfer function of a 2nd-order differentiator. This term has to be present in one of the short-circuit admittances $y_{12}(s)$ or $y_{32}(s)$ in (2). One step towards obtaining an admittance that contains a 2nd-order differentiator is to use the simple 1st-order RC network in Fig. 5. By considering the voltage over the resistor, V_R, the RC network contributes a 1st-order differentiator, since we obtain

$$D(s) = \frac{V_R}{V_2} = \frac{R_1Cs}{1 + R_1Cs} \quad (6)$$

where the factor R_1Cs in the numerator represents the differentiator, and a pole is located at $p = -1/(R_1C)$. An additional differentiator is obtained by adding another capacitor according to Fig. 5 and shorting it to ground to obtain the short circuit admittance y_{32}. This is due to the fact that the voltage over the resistor, V_R, is multiplied by the admittance of the capacitor C to obtain the short-circuit

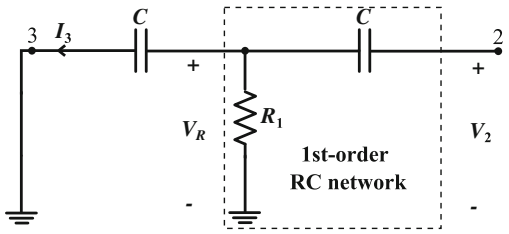

Fig. 5 RC network implementing $y_{32}(s)$ only

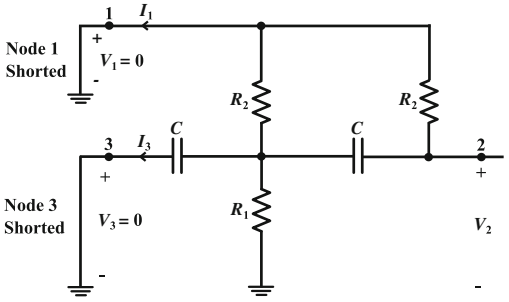

Fig. 6 Modified RC network that implements both $y_{12}(s)$ and $y_{32}(s)$

current I_3. The additional factor Cs contributes a second differentiator. The short-circuit admittance y_{32} of the circuit in Fig. 5 is given by

$$y_{32}(s) = \frac{I_3}{V_2} = -\frac{(R_1Cs)^2}{P(s)} \tag{7}$$

where the factor $(R_1Cs)^2$ in the numerator implements the 2nd-order differentiator and the denominator is given by $P(s) = R_1(1 + 2R_1Cs)$. After division by $y_{32}(s)$ in (2), the factor $(R_1Cs)^2$ ends up in the denominator, just as in the transfer function in (1), while the undesired polynomial $P(s)$ ends up in the numerator and needs to be cancelled by $y_{12}(s)$.

By modifying the RC network according to Fig. 6, the undesired polynomial $P(s)$ will be cancelled and the transfer function will be of the same form as (1). The short-circuit admittance $y_{12}(s)$ of the modified RC network is

$$y_{12}(s) = \frac{I_1}{V_2} = -\frac{\frac{R_1}{R_2^2}(R_1 + R_2 + 3R_1R_2Cs)}{P(s)} \tag{8}$$

where $P(s)$ has changed to

$$P(s) = \frac{R_2}{R_1}(R_1 + R_2 + 2R_1R_2Cs) \tag{9}$$

due to the addition of the resistors R_2. It is obvious that both $y_{12}(s)$ and $y_{32}(s)$ contain $P(s)$. Substituting (8) and (7) into (2) leads to the cancellation of $P(s)$ and yields the final transfer function of the single-amplifier network:

$$H(s) = -\frac{R_1}{R_2^2}\frac{R_1 + R_2 + 3R_1R_2Cs}{(R_1Cs)^2}. \tag{10}$$

Compared to (1), there is a 1st-order polynomial which contains the loop-filter coefficients a_1 and a_2 in the numerator, and a 2nd-order differentiator in the denominator.It is practical to express the resistors R_1 and R_2 in terms of a common resistor value R, i.e $R_1 = n_1R$ and $R_2 = n_2R$. The parameters n_1 and n_2 are used to implement the desired loop filter coefficients, while the value of R is determined according to noise, area, and power consumption requirements. Substituting the expressions for both resistors into (10) yields

$$H(s) = -\frac{\frac{1}{n_2^2}\left(1 + \frac{n_2}{n_1}\right) + \frac{3}{n_2}sRC}{(sRC)^2}. \tag{11}$$

Referring again to (1), the time constant RC equals the sampling period T_s, while the loop filter coefficients can be identified by comparing the numerators:

$$\begin{cases} a_1 = \frac{1}{n_2^2}\left(1 + \frac{n_2}{n_1}\right) \\ a_2 = \frac{3}{n_2} \end{cases} \qquad \begin{cases} n_1 = \frac{3a_2}{9a_1 - a_2^2} \\ n_2 = \frac{3}{a_2} \end{cases}. \tag{12}$$

For any given values of the loop filter coefficients, the equations in (12) can be used to find n_1 and n_2.

3.2 Implementation of the addition operator

So far it has been assumed that the difference between the input and the feedback signal is available. This situation is shown in Fig. 7(a), where the RC network in Fig. 6 is used together with an operational amplifier and is excited by the voltage $V_{in} - V_{fb}$ at node 1. In a practical implementation, V_{in} and V_{fb} are two separate signals and therefore need to be applied to the RC network separately. This can be achieved by transforming both left and right sub-circuits enclosed by dashed shapes in Fig. 7(a). Both transformations are shown in Fig. 7(b). The transformation of the right sub-circuit is straightforward, since the resistor is connected to the virtual ground of the operational amplifier. Therefore, the voltage components V_{in} and V_{fb} can be applied in parallel instead, while the transfer function of the loop filter remains the same.

The left sub-circuit is not connected to a virtual ground, and its transformation is not as straightforward. The first step is to redraw the circuit according to Fig. 7(b). The

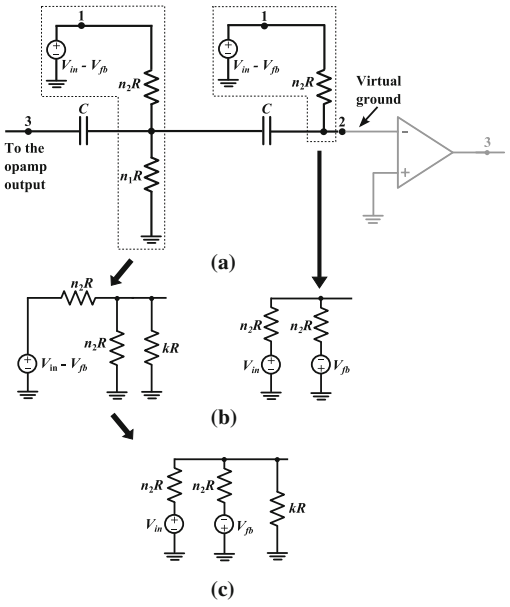

Fig. 7 **a** Loop filter with voltage $V_{in} - V_{fb}$ provided. **b** Transformations of the two sub-circuits. **c** Further transformation of the left sub-circuit

resistor n_1R has been split into a parallel connection of two resistors, n_2R and kR, where the factor k makes the parallel resistance equal to the original n_1R. Solving the equation $n_2R \| kR = n_1R$ yields k as

$$k = \frac{n_1 n_2}{n_2 - n_1}. \tag{13}$$

The reason for dividing up the n_1R resistor into two resistors is the following: the left circuit in Fig. 7(b) has a suitable Thévenin equivalent, as shown in Fig. 7(c), which separates the two voltage signals V_{in} and V_{fb}, as desired.

The final loop filter after all transformations is shown in Fig. 8. The two resistors connected to the feedback signal V_{fb} are split into several parallel unit resistors when multi-bit DACs are used.

4 Effects of amplifier non-idealities

The amplifier non-idealities, such as finite gain and finite bandwidth, alter the loop filter transfer function and result in an NTF with degraded quantization noise suppression [9]. To study the effects of the non-idealities on the loop filter transfer function, an amplifier model consisting of a transconductance g_m, output resistance r_o, output capacitance c_o and input capacitance c_i was used. The output

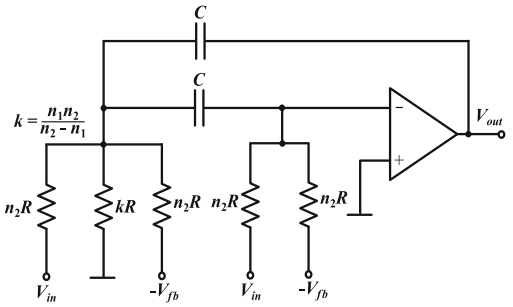

Fig. 8 The final loop filter

capacitance also includes the loading capacitance at the amplifier output. The amplifier model is shown in Fig. 9 together with the rest of the loop filter. The loop gain of the loop filter is $A\beta$, where A is the forward gain and β is the feedback factor. Both A and β can be found from Fig. 9 as

$$A = \frac{i_c}{v_i}, \qquad \beta = \left.\frac{v_i}{i_c}\right|_{v_s=0}. \tag{14}$$

The loop gain can be used to calculate the loop filter transfer function [10].

In Fig. 10, the loop gain of the loop filter is shown for two cases: finite DC gain only and both finite DC gain and finite gain-bandwidth product (GBW). The amplifier DC gain in this example was 62 dB and GBW was 16 MHz, which is equal to the actual DSM sampling frequency. First, the case with finite DC gain only ($c_o = c_i = 0$ in Fig. 9) is considered. For low frequencies, the two capacitors in the feedback network in Fig. 9 act as open circuits and the loop gain is low, since almost no signal is fed back. For high enough frequencies, the two capacitors in the feedback network act as short circuits and the loop gain reaches a maximum value and remains constant. If both capacitors in Fig. 9 are replaced by short circuits and v_s is shorted to calculate β according to (14), the transconductance will see the output resistance r_o in parallel with the three resistors of value n_2R and one of value n_1R. The loop gain for high frequencies is therefore given by

$$T_\infty = -g_m\left(r_o \| n_1R \| \frac{n_2R}{3}\right). \tag{15}$$

It is beneficial if this value is as large as possible, since it determines how accurately the ideal loop filter transfer function is approximated. One way to achieve higher loop gain is to increase the value of R. However, as will be discussed later, R cannot be arbitrary large, since the size is limited by various design constraints. In the second case, the additional pole due to the finite GBW causes the loop gain to deviate already at low frequencies, and the maximum value in (15) is never reached.

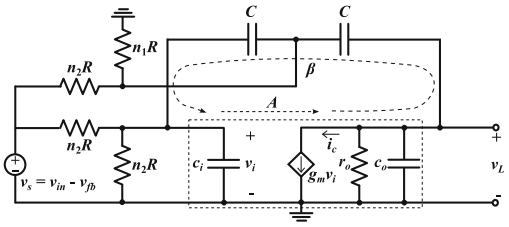

Fig. 9 The small signal model of the loop filter

In Fig. 11, the non-ideal loop filter transfer function is plotted for the two cases and compared to the ideal one in (11). In the first case, finite DC-gain transforms the two poles at the origin into two complex poles. This causes a flat loop filter transfer function and reduced quantization noise suppression at lower frequencies. Furthermore, at high frequencies the actual transfer function deviates from the ideal one due to the right-half-plane zero caused by the direct path from input to output through the feedback network. At intermediate frequencies, the ideal transfer function is, however, well approximated. In the second case, finite GBW causes the actual transfer function to deviate from the ideal one at intermediate frequencies as well, which further degrades the quantization noise suppression. This is also related to the reduction of loop gain at intermediate frequencies, as shown in Fig. 10. For a GBW equal to the sampling frequency, the loop gain is not sufficient and, as will be discussed later, a higher GBW is required to achieve an acceptable performance.

5 Design of the delta-sigma modulator

The single-amplifier loop filter has been used in a CT DSM intended for wireless ultra-low-power portable devices. System simulations in the discrete-time domain performed by using Schreiers's toolbox [11] resulted in an adequate SQNR of 70 dB to meet the overall SNR target of 60 dB over a 500 kHz bandwidth. To achieve the targeted SNR, while keeping the sampling frequency as low as possible, a 4-bit quantizer was chosen. This choice, together with a 2nd-order loop filter, resulted in an oversampling ratio of 16, yielding a sampling frequency of 16 MHz.

The block schematic of the modulator is shown in Fig. 12. Resistive DACs are used in the feedback due to better noise performance compared to current-steering DACs [12]. Due to the use of multi-bit quantization, highly linear multi-bit DACs are required. The DACs must be as linear as the overall modulator to achieve the desired performance [13]. This requires high-precision matching of the unit elements. Resistive DACs relieve matching requirements somewhat, compared to current steering DACs, since resistors show

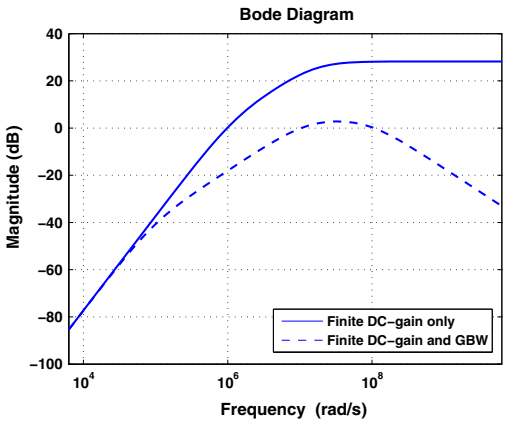

Fig. 10 Effects of finite DC-gain and GBW on the loop gain of the loop filter

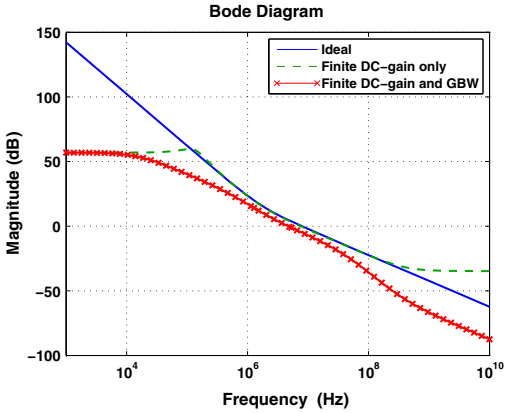

Fig. 11 Effects of finite DC-gain and GBW on the loop filter transfer function

better matching accuracy than transistors [14]. However, to significantly relieve the matching requirements, data weighted averaging (DWA) is used after the 4-bit flash quantizer.

Delayed return-to-zero (RZ) pulses are used in the feedback to ensure that the quantizer has fully reached a decision before its output is converted by the DACs. The RZ pulses are delayed by a quarter of the clock period (i.e., $\alpha = 0.25$ and $\beta = 0.75$ in Fig. 12). RZ feedback is advantageous here over non-return-to-zero (NRZ) feedback, which would require an additional DAC and summing operation to compensate for the excess loop delay [15] [16]. The high jitter sensitivity of RZ pulses is not of concern due to the low sampling frequency.

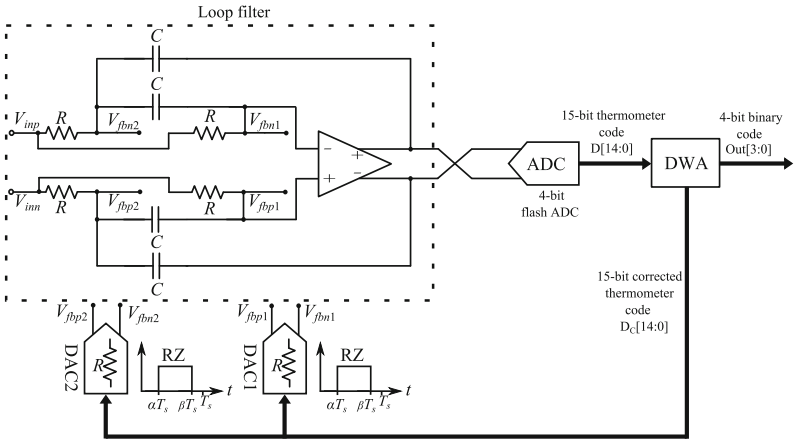

Fig. 12 Block schematic of the DSM

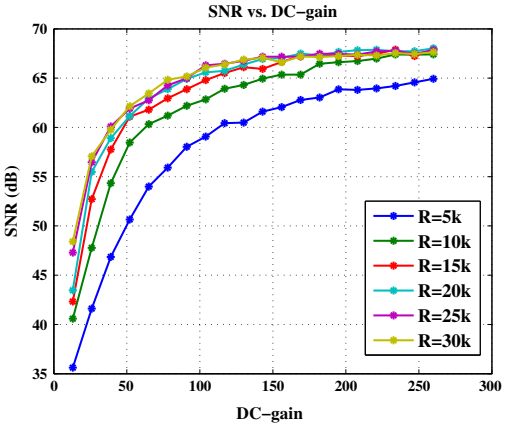

Fig. 13 Simulated SNR vs. DC-gain for different values of R

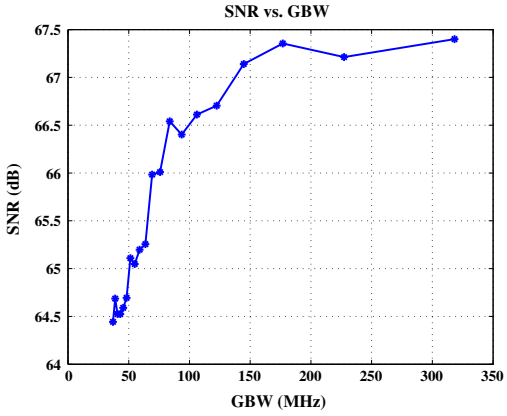

Fig. 14 Simulated SNR vs. GBW for $R = 15$ k

Discrete-to-continuous time conversion [15], [17] with RZ feedback pulses yields the following values for the feedback coefficients: $a_1 = 2, a_2 = 3$. Using the equations in (12), the following factors are obtained: $n_1 = n_2 = 1$. This is a special case, since the expression for k in (13) approaches infinity. This means that the kR resistor can be removed from the circuit. Since $n_2 = 1$, all the remaining resistors will have a value of R, as shown in Fig. 12.

5.1 System simulations

To study the impact of amplifier non-idealities on the overall performance of the modulator, the amplifier model from Fig. 9 was used during system simulations. The output resistance was set to 130 kΩ, which was the typical value that could be obtained from a common source stage when used as the output stage of the operational amplifier. By sweeping the other two parameters, it was possible to study the effects of finite DC-gain and finite GBW. The modulator was designed for a maximum differential input signal of 200 mV, which was used in simulations as well.

Fig. 13 shows SNR vs. DC gain for different values of R in the loop filter. Thermal noise from all resistors was included in the simulations. It is evident from these results that the performance for lower DC gains deteriorates when R decreases. This is due to the fact that the loop gain decreases for smaller values of R, as predicted by (15), as the amplifier output is increasingly loaded by the feedback network. This can only be compensated by a corresponding

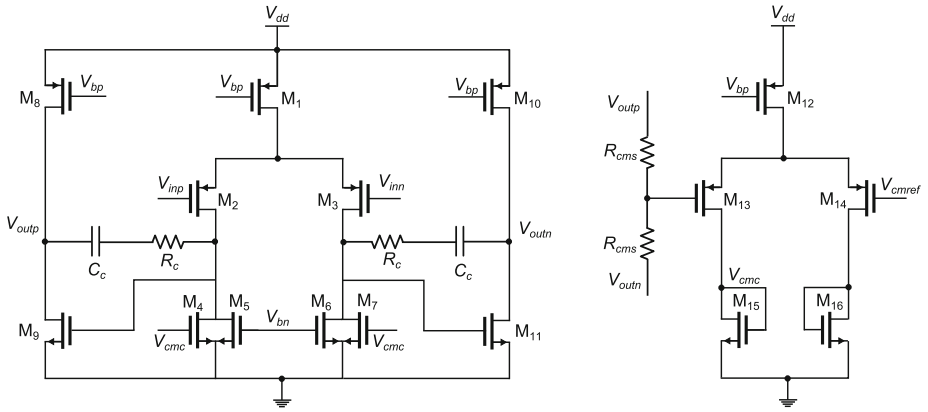

Fig. 15 The operational amplifier with common-mode feedback

increase of the transconductance. The upper limit of R is determined by thermal noise and resistor area. Since the resistance of a unit cell in a 4-bit resistive DAC must be 15 times larger than the parallel resistance of all cells, the area may become an issue for large values of R. Furthermore, the associated parasitic capacitances become large as well, deforming and delaying the feedback pulses.

Based on a trade-off between the above mentioned limitations, R was set to 15 kΩ. Substituting the value for R in the expression for the sampling period, $T_s = RC$, yields $C = 4.17$ pF. According to the graph for $R = 15$ kΩ in Fig. 13, a gain of at least 200 is required to maintain the maximum possible SNR. The SNR is 67.4 dB, and it is easy to show that the thermal noise from the resistors degrades the SNR by 2.6 dB.

Figure 14 shows SNR vs. GBW for $R = 15$ kΩ. These results show that a GBW of at least 70 MHz is required to ensure less than 1 dB of SNR degradation.

5.2 The operational amplifier

The operational amplifier was implemented using the two-stage Miller architecture, see Fig. 15. Two-stage architectures are more suitable for low supply voltages than single-stage architectures, since the gain is achieved by cascading stages instead of transistor stacking, which would otherwise limit the voltage headroom. To obtain realistic stability requirements, the operational amplifier was designed inside the actual loop filter where it is going to be used [18]. The parasitic capacitance at the input of the flash ADC loads the amplifier output and was also included in the test bench. This capacitance was estimated to 100 fF after simulations. The final design resulted in a DC gain of 62 dB and a GBW of 90 MHz while consuming 43 µW from 0.8 V. The GBW requirement sets the power consumption.

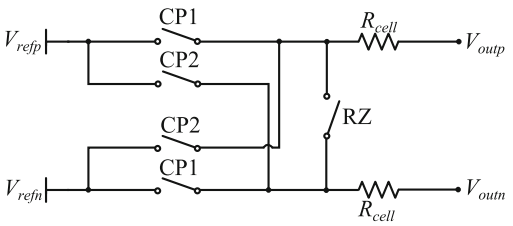

Fig. 16 Resistive DAC cell

5.3 Feedback DACs

Switched-resistor cells were used to realize the two RZ DACs, see Fig. 16. Several switched-resistor cells were connected in parallel to implement a multi-bit RZ DAC. Every cell is controlled by one of the thermometer-coded output bits from the flash ADC. The value of the cell resistance R_{cell} is 225 kΩ.

6 Measurement results

The DSM has been implemented in a 65 nm CMOS process. Fig. 17 shows the chip photograph of the modulator, which occupies an active area of 0.35×0.23 mm. The circuit is powered by a 800 mV supply and consumes 76 µW. The maximum differential input signal is 200 mV. An RF signal generator was used to generate a clean sinusoidal clock signal, which was buffered on-chip. Figure

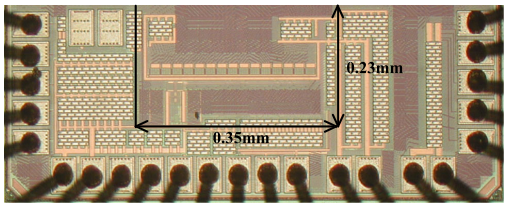

Fig. 17 Chip photo, active area: 0.35 mm × 0.23 mm

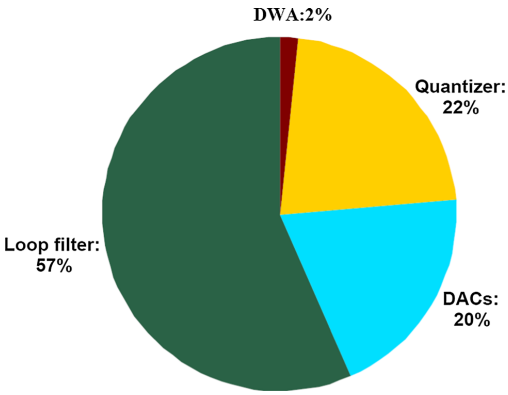

Fig. 18 Power breakdown of the DSM

18 shows the power breakdown of the DSM. The clock generator wasn't implemented in this deign and its power consumption is omitted in the power budget.

The measured output spectrum of the DSM is shown in Fig. 19 for an input signal amplitude of -3 dBFS. If the DWA algorithm is inactivated, a 2nd-order harmonic at -73 dBFS and a 5th-order harmonic at -80 dBFS appear in the spectrum. This shows that the DWA algorithm successfully mitigates for the mismatch errors in the DAC unit elements.

A graph of SNR/SNDR vs. the input signal amplitude is shown in Fig. 20. The modulator achieves a maximum SNR of 65.2 dB for an input signal of -2.5 dBFS, and a maximum SNDR of 64 dB for an input signal of -3 dBFS. This results in a figure-of-merit (FOM) of 59 fJ/conversion. A performance summary and comparison with other relevant DSMs is shown in Table 1.

7 Conclusions

This paper has presented a CT DSM with a 2nd-order loop filter using a single operational amplifier. The main goal of such a loop filter is to reduce the power consumption while

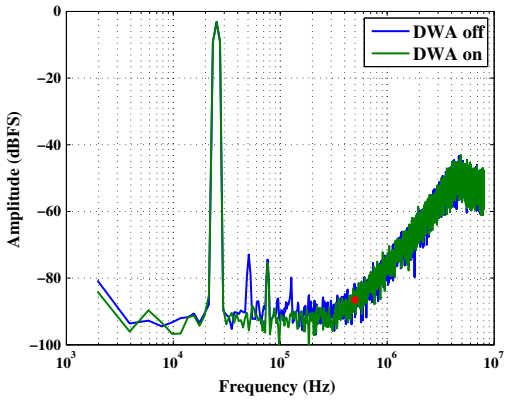

Fig. 19 Output spectrum for a −3 dBFS input signal

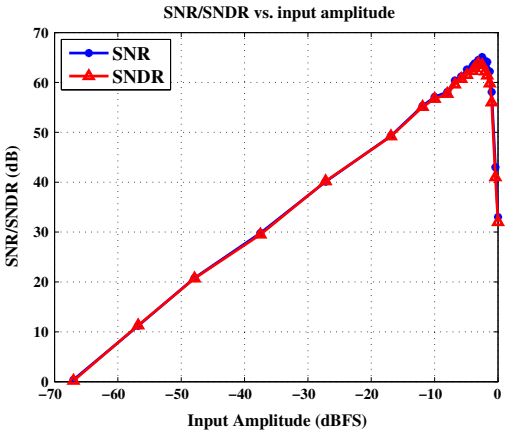

Fig. 20 Measured SNR and SNDR vs. input amplitude

Table 1 Performance comparison

Reference	Process (μm)	Supply voltage (V)	BW (MHz)	SNDR (dB)	Power (mW)	FOM (fJ/Conv)
[4]	0.13	1.2/1.4	7.2	77	13.7	164
[5]	0.04	-	10	70	2.57	50
[12]	0.18	1.8	0.024	91	0.09	65
[19]	0.065	0.8	0.02	91	0.23	198
[20]	0.18	1.8	0.024	89	0.122	110
[21]	0.090	1.2	1	62	0.89	433
[22]	0.13	0.9	1.92	51	1.5	1350
[23]	0.13	1.5	2	71	3	259
This work	0.065	0.8	0.5	64	0.076	59

still achieving a 2nd-order shaping of the DSM quantization noise. The concept has been verified by implementation and measurements of a 65 nm CMOS 2nd-order 4-bit CT DSM, achieving a peak SNR of 65.2 dB and a peak SNDR of 64 dB over a 500 kHz bandwidth, while consuming only 76 μW.

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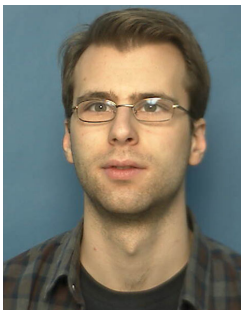

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