Vertical III-V Nanowire Tunnel Field-Effect Transistor

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Elvedin Memisevic

LUND UNIVERSITY

Doctoral Thesis
Electrical Engineering
Lund, September 2017

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Metal-oxide-semiconductor field-effect transistor, Steep slope devices, Tunnel field-effect transisor, Vertical nanowire, III-V semiconductors, Hydrogen silsesquioxane

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Abstract

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Using transmission electron microscopy, the heterojunction was characterized. Furthermore, TCAD modeling was performed to understand what limits the performance of these devices. Also, electrical measurement of the

random telegraph noise allowed us to understand the impact the oxide defects have on highly scaled devices.

Populärvetenskaplig Sammanfattning

Den elektroniska revolutionen som har pågått de senaste 60 åren har haft en stor inverkan på vårt samhälle. Idag när man blickar framåt ser man nya utmaningar såsom elektriska kretsar som härmmar hjärnan (Neuromorphic computing), Kvantdatorer samt Sakernas Internet; teknologier som har potential till att förändra vårt samhälle. Grundstenen i den utvecklingen är transistorn, en elektronisk komponent som kan användas för att förstärka elektriska signaler i analoga kretsar eller fungera som en omkopplare som kan användas för att bygga upp olika logiska grindar i digital kretsar. Genom nedskalning av dimensionerna kan vi idag bygga digital kretsar med flera miljarder transistorer på en yta som motsvarar ett frimärke. Denna stora täthet av transistorer gör att värmeutvecklingen är väldigt högt och kan skada kretsen ifall den inte hanteras rätt. För att åtgärda detta krävs det att transistorerna blir effektivare vilket innebär att lägre drivspänningar används och snabbare växling mellan av och på tillståndet åstadkomms. Den högsta teoretiska hastigheten som traditionella transistorerna kan växla är begränsade till 60 mV/dekad (termiska gränsen vid rums temperatur). Detta innebär; för att ändra strömmen med en dekad krävs det minst en spänningändring på 60 mV.

Tunneltransistor är en annan typ av transistor än de som används idag, då den använder ett kvantmekansik fenomen kallat tunnlig för att operera. Genom att utnyttja en annan operationsmekanism än traditionella transistorn kan tunneltransistorerna mer effektivt slås på och av. Orsaken till bättre effektivitet är att tunneltransistorn inte begränsas av den termiska gränsen på samma sätt som traditionela transistorn gör. I detta arbete tillverkas tunneltransistorer genom att använda vertikala nanotrådar, cylindriska III-V halvledar-kristaller med en diameter mellan 20-40 nm och en längd mellan

400-600 nm. Användandet utav vertikala nanotrådar tillåter oss att kombinera olika III-V halvledare utav högt kristallin kvalite, i samma nanotråd. Den cylindriska formen hos vertikala nanotrådarna erbjuder dessutom bästa möjliga elektrostatiska kontrol. Kombination av optimerad struktur, hög material kvalite samt bästa möjliga elektrostatik tillåter oss att tillverka tunneltransistorer med en prestanda som för första gången någonsin kan jämföras med prestanda hos dagens traditionella transistorer. Det är ett viktigt steg för att tunneltransistor ska gå från att vara den lovande kandiadeten till den trovärdiga ersättaren.

Acknowledgments

During my PhD-studies I have been lucky to meet and work with lots of great people. First, I would like to thank my main supervisor Lars-Erik Wernersson for giving me a opportunity to do my PhD studies in the nanoelectronics group and for his guidance and encouragement. I would also like to thank my supervisor Erik Lind for fruitful discussions and great advices. Furthermore, I would like to thank my supervisor Johannes Svensson for his help with the nanowire growth and contributions to the TFET project.

Lars Ohlsson was one of my supervisors during my master thesis and later colleague during my PhD-studies. It has been a great pleasure to work with Lars. I have known Cezar Zota since 2007, these 10 years have been enjoyable due to his great humor and intelligence. I have spent many hours at the office together with Martin Berg, Kristoffer Jansson, Jun Wu, Sebastian Heunisch, Markus Hellenbrand, Olli-Pekka Kilpi, Štefan Andrić, Fredrik Lindelöw, and Adam Jönsson. Many great things can be said about these men, however only one of them keeps the unofficial record for most sleeping hours in our clean room. I also had the great pleasure to share my time at the nanoelectronics group with Aein Shiri Babadi, Sofia Johansson, Karl-Magnus Persson, Anil Dey, and Mattias Borg. I would like to thank technicians and engineers at Lund Nano Lab for their great professionalism and hard work to keep the lab running. I would like to thank my friends and close ones for their support. Finally, I would like to thank my parents who always have supported me in my decisions and showed me undying and unconditional love.

Elvedin Memisevic

Contents

Preface

This thesis is a summary of the five years of work I have performed within the nanoelectronics group at department of Electrical and Information technology at Lund University. The work has been performed under supervision of Dr. Johannes Svensson, Associate Professor Erik Lind, and Professor Lars-Erik Wernersson.

STRUCTURE OF THE THESIS

This thesis is devided in three main parts: Introduction, Appendix, and Papers.

- **INTRODUCTION**
  The research field is reviewed and summarized, with emphasis on the papers that are included in the thesis.

  1: Background
  Introduction of main aspects of the transistor for the reader. Development of the transistors with emphasis on used material and geometry of the devices. Motivation to why there is a need for steep slope devices.

  2: Fundamentals of Tunnel Field-Effect Transistors
  Short introduction to theory of the TFET, with emphasis on devices with 1D channel.

  3: Fabrication
  Here the manufacturing of the devices is discussed. First an

overview is given followed by a discussion about challenges to work with vertical structures.

4: Vertical InAs/GaSb and InAs/InGaAsSb/GaSb nanowire TFETs
A overview of the current field is given, followed by presentation of the work with vertical InAs/GaSb and InGa/InGaAsSb/GaSb TFETs is presented. In the final sub-chapter devices in this work are benchmarked against published data.

5: Final words and Outlook
Some final words and outlook is given about the results in this thesis.

- **APPENDICES**
  Further details on various aspects of the work can be found in the appendices.

  A: Fabrication of the Vertical Tunnel Field-Effect Transistors

  B: Self-alignment of Hydrogen Silsesquioxane

  C: Fabrication of Vertical Transistors with 20 nm gate length

  D: Vertical InAs/GaSb nanowire TFETs with channel diameter of 11-12 nm

- **PAPERS**
  The included papers are reproduced in the last part of the thesis.

INCLUDED PAPERS

The following papers are included in this thesis and the respective published or draft versions are appended at the back of this thesis.

Paper I: E. Memisevic, M. Hellenbrand, E. Lind, A.R. Persson, S. Sant, A. Schenk, J. Svensson, R. Wallenberg, and L.-E. Wernersson, "Individual defects in InAs/InGaAsSb/GaSb Nanowire Tunnel Field-Effect-Transistors operating below 60 - mV/decade," *in Nano Letters*,vol. 17, no. 7, pp. 4373-4380, Jun. 2017

► *I manufactured the devices, performed DC measurements, wrote introduction, fabrication, and conclusion sections. With support from L.-E. Wernersson was responsible for coordination and overall writing process.*

Paper II: E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind, and L.-E. Wernersson, "Vertical InAs/GaAsSb/GaSb Tunneling Field-Effect Transistor on Si with S = 48 mV/decade and I_{on} = 10 μA/μm for I_{off} = 1 nA/μm at V_{DS} = 0.3 V ," *in 2016 IEEE International Electron Devices Meeting (IEDM)*, pp. 19.1.1-19.1.4, Dec. 2016.

► *I manufactured the devices, performed DC measurements, and wrote the whole manuscript.*

Paper III: E. Memisevic, J. Svensson, E. Lind, and L.-E. Wernersson, "InAs/(In)GaAsSb/GaSb Nanowire Tunnel Field-Effect Transistors," *Submited to IEEE Trans. Electron Dev.*

► *I manufactured the devices, performed all measurements, and wrote the whole manuscript.*

Paper IV: E. Memisevic, E. Lind, M. Hellenbrand, J. Svensson, and L.-E. Wernersson, "Determination of band edge sharpness by comparison of subthreshold and conduction slopes in TFETs," *in IEEE Electron Device Lett.,* Manuscript

► *I manufactured the devices, performed some of the measurements, and wrote the manuscript.*

Paper V: E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind, and L.-E. Wernersson, "Scaling of Vertical InAs-GaSb Nanowire Tunneling Field-Effect Transistors on Si," *in IEEE Electron Device Lett.,* vol. 37, no. 5, pp. 549-552, Mar. 2016.

► *I manufactured the devices, performed most of the measurements, and wrote the whole manuscript.*

Paper VI: E. Lind, E. Memisevic, A.W. Dey, and L.-E. Wernersson, "III-V Heterostructure Nanowire Tunnel FETs," *in IEEE Electron Devices Soc.*, vol. 3, no. 3, pp. 96-102, May 2015.

► *I manufactured the vertical devices, performed all measurements on the vertical devices, and contributed to the section about the vertical devices.*

Paper VII: E. Memisevic, E. Lind, and L.-E. Wernersson, "Thin electron beam defined hydrogen silsesquioxane spacers for vertical nanowire transistors," *in J. Vac. Sci. Technol. B* , vol. 32, no. 5, pp. 051211-1-051211-6, Sep./Oct. 2014.

► *I developed the process for HSQ spacers, manufactured the devices, performed all measurements, and wrote whole manuscript.*

EXTRANEOUS PAPERS

The following papers are not included in the thesis, but summarise related work which I have contributed to.

Paper viii: S. Johansson, E. Memisevic, L.-E. Wernersson, and E. Lind, "High-frequency gate-all-around vertical InAs nanowire MOSFETs on Si substrates," *in IEEE Electron Device Lett.*, vol. 35, no. 5, pp. 518-520, Mar. 2014.

Paper ix: S. Johansson, E. Memisevic, L.-E. Wernersson, and E. Lind, "RF characterization of vertical InAs nanowire MOSFETs with ft above 140 GHz," *Proceeding of the International Conference on Indium Phosphide and Related Materials (IPRM)*, May 2014.

Paper x: E. Memisevic, J. Svensson, E. Lind, and L.-E. Wernersson, "Vertical InAs/GaSb Nanowire Axial TFETs Integrated on Si-substrates (CSW)," *Compound semiconductor week, Jun. 2015*

Paper xi: E. Memisevic, J. Svensson, E. Lind, and L.-E. Wernersson, "InAs/GaSb Vertical Nanowire TFETs on Si for Digital and Analogue Applications," *Silicon Nanoelectronics Workshop (SNW)*, Jun. 2016

Paper xii: E. Memisevic, J. Svensson, E. Lind, and L.-E. Wernersson, "Statistics of InAs/InGaAsSb/GaSb TFETs with sub-50 mV/decade operation at V_{DS} of 0.3V," *Compound semiconductor week (CSW), May 2017*

Paper xiii: M. Hellenbrand, E. Memisevic, J. Svensson, E. Lind, and L.-E. Wernersson, "Random Telegraph Signal Noise in Tunneling Field-Effect Transistors with S below 60 mV/decade," *European Solid-State Device Research Conference (ESSDERC), Sept. 2017*

Paper xiv: J. Zhang, C. Alessandri, P. Fay, A. Seabaugh, T. Ytterdal, E. Memisevic, and L.-E. Wernersson, "Projected Performance of Experimental InAs/GaAsSb/GaSb TFET as Millimeter-Wave Detector," *IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (IEEE S3S), Oct. 2017*

Paper xv: A. Schenk, S. Sant, E. Memisevic, L.-E. Wernersson, K. Moselund, and H. Riel, "The Impact of Hetero-junction and Oxide-interface Traps on the Performance of InAs/Si and InAs/GaAsSb Nanowire Tunnel FETs," *Simulation of Semiconductor Processes and Devices (SISPAD), Sept. 2017*

Paper xvi: M. Hellenbrand, E. Memisevic, M. Berg, O.-P. Kilpi, J. Svensson, and L.-E. Wernersson, "Low-Frequency Noise in III-V Nanowire TFETs and MOSFETs," *Submitted to EDL*

Abbreviations and Symbols

ABBREVIATIONS

2DM two-dimensional material
AFM atomic force microscopy
ALD atomic layer deposition
Al_2O_3 aluminum oxide
Ar argon
As arsenic
AsH_3 arsine
Au gold

BOE buffered oxide etch
BTBT band-to-band tunneling

C carbon
CH_3COOH acetic acid
CMOS complementary metal-oxide-semiconductor

DAT defect assisted tunneling
DC direct current
DIBL drain-induced barrier lowering
DeZn diethylzinc

EBL electron beam lithography
EOT effective oxide thickness

FET field-effect transistor

FOX flowable oxide

Ga gallium
GAA gate-all-around
GaAs gallium arsenide
GaSb gallium antimonide
Ge germanium
GeSn germanium tin

H hydrogen
H_2O water
H_2O_2 hydrogen peroxide
H_3PO_4 phosphoric acid
H_2SO_4 sulfuric acid
HCl hydrochloric acid
Hf hafnium
HF hydrogen fluoride
HfO_2 hafnium dioxide
HNO_3 nitric acid
HP hotplate
HSQ hydrogen silsesquioxane

I_2 iodine
IC integrated circuit
In indium
InAs indium arsenide
InGaAs indium gallium arsenide
InGaAsSb indium gallium arsenide antimonide
InP indium phosphide
IPA isopropyl alcohol (2-propanol)

KI potassium iodide
KOH potassium hydroxide

MIBK methyl isobutyl ketone
MoS_2 molybdenum disulfide
MOSFET metal-oxide-semiconductor field-effect transistor
MOVPE metalorganic vapour phase epitaxy

N_2 nitrogen
NaOH sodium hydroxide

NDR negative differential resistance
Ni nickel

O oxygen

PMMA poly(methyl methacrylate)
PVCR peak-to-valley ratio

RF radio frequency
RIE reactive ion etching
RTP rapid thermal processing
RTS random telegraph noise

Sb antimony
SEM scanning electron microscopy
SF_6 sulfur hexafluoride
Si silicon
SiGe silicon germanium
SiO silicon monoxide
SiO_x silicon oxide
Sn tin

TAT trap assisted tunneling
TCAD technology computer aided design
TDMAHf tetrakis(dimethylamido)hafnium(IV)
TEM transmission electron microscopy
TESn tetraethyltin
TFET tunneling field-effect transistor
Ti titanium
TMA trimethylaluminium
TMAH tetramethylammonium hydroxide
TMD transition metal dichalcogenides
TMGa trimethylgallium
TMIn trimethylindium
TMSb trimethylantimony

ULP ultra low power
UV ultraviolet

W tungsten
WKB Wentzel-Kramers-Brillouin

WZ wurtzite

ZB zincblende
Zn zinc
ZrO_2 zirconium dioxide

GREEK SYMBOLS

ϵ_0 ($A^2s^4kg^{-1}m^{-3}$) Vaccum permittivity: $\approx 8.854 \cdot 10^{-12}$ $A^2s^4kg^{-1}m^{-3}$
ϵ_r (unitless) Relative permittivity
μ_e ($m^2/(Vs)$) Electron mobility
μ_p ($m^2/(Vs)$) Hole mobility
ρ (Ωm^2) Resistivity

LATIN SYMBOLS

E_g (J) Band-gap energy
C_s (F) Semiconductor capacitance
C_{ins} (F) Insulator capacitance
g_d (S) Output conductance
g_m (S) Transconductance
$g_{m,max}$ (S) Peak Transconductance
I_D (A) Drain current
I_{DS} (A) Drain-source current
I_G (A) Gate current
I_{OFF} (A) Off-current
I_{ON} (A) On-current
k ($m^2kgs^{-2}K^{-1}$) Boltzmann constant
L_G (m) Gate length
m^* Relative effective mass
q (As) Elementary charge
r_{ON} (Ω) On-resistance
S (mV/decade) Subthreshold swing
S_{MIN} (mV/decade) Minimum subthreshold swing
T (K) Temperature
v_{inj} (m/s) Electron injection velocity
V_{DD} (V) Supply voltage
V_{DS} (V) Drain-source voltage
V_{GS} (V) Gate-source voltage
V_T (V) Threshold voltage

FUNCTIONS AND OPERATIONS

$\log(\cdot)$ logarithm with the base 10

INTRODUCTION

1

Background

1.0.1 THE TRANSISTOR

The world of today has been shaped by the electronic revolution that has occurred during the last 60 years. The birth year of the modern transistor, which is the main building block for almost all electronics, is generally set to 1947 when researchers John Bardeen, Walter Brattain, and William Shockley demonstrated the first functioning transistor [1]. The next important step was when transistors were integrated on the same wafer in the first integrated circuits (IC). Since the first ICs the number of transistors has roughly been doubled every 18th months reaching todays circuits that contain billions of transistors. The rate of the scaling is said to follow Moores Law, after co-founder of Intel Gordon Moore, who predicted this development [1,2]. During these years many different types of transistors have been developed, although the main type used in this revolution is the metal-oxide-semiconductor field-effect transistor (MOSFET).

An illustration of a MOSFET can be viewed in Figure 1.1a, where the main sections and dimensions are marked. Even if this is a device with four terminals, commonly three of them (source, drain, and gate) are used actively during device operation. Figure 1.1b, shows the band diagram of a n-type MOSFET without any voltage applied at the source and drain terminals. Source and drain regions are n-doped, the region between is p-doped. This difference in doping creates a barrier for the charges. The height of this barrier can be controlled by applying voltage on the gate-terminal, thereby this voltage is used to turn on and off the device. Figure 1.1c illustrates band diagram for two different source to drain voltages, using the same gate-voltage. Usually source to drain voltage is referred to as drive voltage.

To build a CPU requires two types of transistors, p-type and n-type MOS-

FETs [2]. The difference between these two types of devices is the type of charges that are flowing through the channel, for n-type it is electrons and for p-type it is holes. By combing these two type of MOSFETs, complementary logic (CMOS) can be implemented. Figure 1.1d shows an inverter which is the smallest part of this logic. In this thesis all focus will be on n-type of devices.

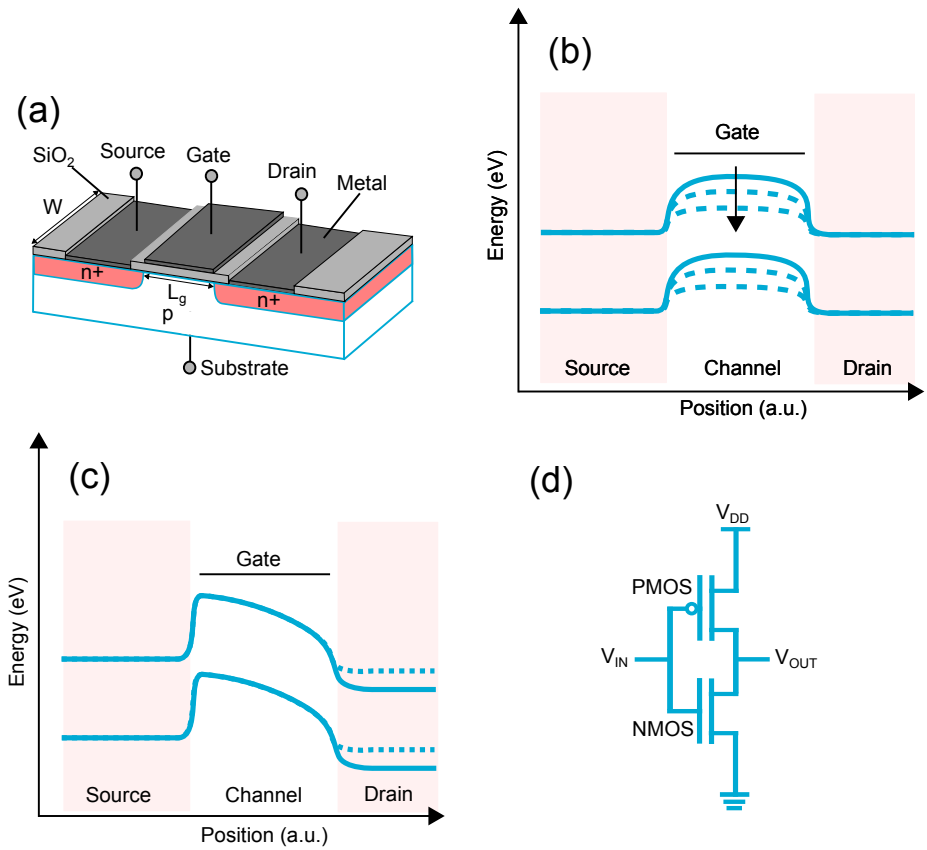

Figure 1.1: Metal-oxide-semiconductor Field-Effect Transistor (MOSFET) (a) Illustration of a planar MOSFET. (b) Band diagram of a MOSFET without any drive voltage applied. Gate-voltage changes the height of the barrier in region between source and drain. (c) Band diagram of the MOSFET when the drive voltage is applied. (d) An inverter circuit which is the smallest CMOS logic gate.

1.0.2 METRICS

In a transistor the current is controlled using gate voltage and drain to source voltage. All data presented in this thesis is measured using common-source configuration, which means that the source is common voltage reference for the gate and drain voltage. Thereby the gate voltage is written as V_{GS} and drain to source voltage as V_{DS}. To make a proper characterization of the transistor there are a number of metrics that are used and these will be described below.

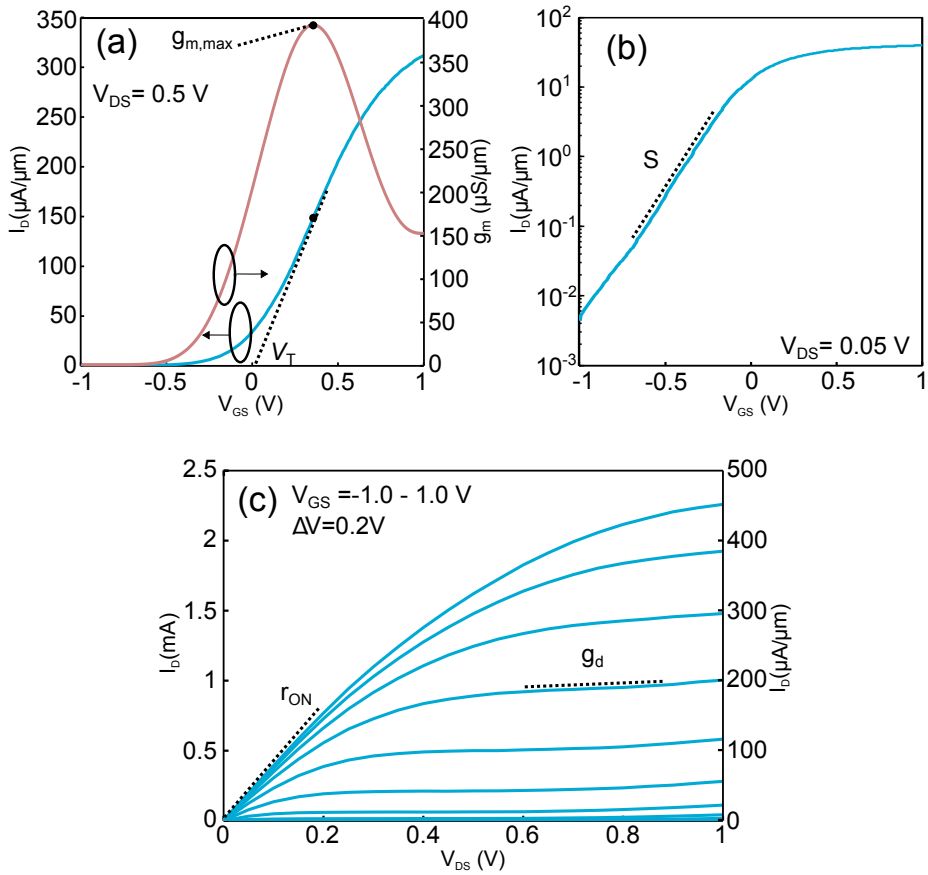

Figure 1.2: Electrical characteristics of a vertical InAs nanowire MOSFET [Paper VII] (a) Transfer curves of the MOSFET in linear scale, where g_m is the transconductance and V_T is the threshold voltage. (b) Transfer curves of the MOSFET with logarithmic scale on Y-axis, where S is subthreshold swing. (c) Output data of a MOSFET, where g_d is the output conductance and r_{ON} is on-resistance.

DRIVE CURRENT

Transfer and output graphs are shown in Figure 1.2a and c, respectively. These two graphs describes dependence of the current, that flows between the source and drain, on the gate and drive voltage. As the transistor switches from off to on state the current will change its magnitude with several orders, thereby to study the off characteristics the current in transfer graph is plotted using a logarithmic scale, Figure 1.2b. Using these graphs, metrics that are important for transistors performance can be determined. For the digital circuits, the ratio between the off- and on-current is of importance, thus it is important to clearly see the difference between the zero and one. In general when discussing currents for digital applications, usage of I_{OFF} and I_{ON} is common. I_{ON} is usually determined with reference to used I_{OFF} according to

$$I_{ON} = I_D(V_{DS} + V_{GS,OFF}), \tag{1.1}$$

where $V_{GS,OFF}$ is gate voltage at I_{OFF}.

The large number of transistors that are integrated on the same chip has increased the importance of off-current. Even if not all transistors operate at the same time, the large number of the transistors that are turned off will impact the total power consumption. Today, the off-current is categorized accordingly: 100 nA/μm (High power), 1 nA/μm (Standard power), 30 pA/μm (Low Power), and 15 pA/μm (Ultra Low Power) [3].

However, the on-current needs also to be large enough to achieve sufficient operation speed and reliability. As equation 1.1 shows, the used drive voltage will determine how much voltage that needs to be applied over the transistor to switch between the off- and on-current. However, the final on-current will also depend on subthreshold swing and transconductance of the device, as these metrics determine how effectively transistor utilize available voltage. All normalized currents, published in this thesis, are normalized using $\pi \cdot d_{InAs} \cdot n_{NW}$, where d_{InAs} is diameter of InAs segment and n_{NW} is number of nanowires in the device.

TRANSCONDUCTANCE

From the transfer curve, the transconductance (g_m) can be extracted. Definition of the transconductance is

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}}, \tag{1.2}$$

which is simply a partial derivate of the drain current with respect to the gate voltage. This metric describes how effectively a transistor amplifies a small voltage on the gate, which is a important metric for analog applications

where the transistor is used to amplify signals. However, also in digital circuits high g_m is beneficial, as high g_m and low subhtreshold swing allows for large on-current.

OUTPUT CONDUCTANCE

The dependence of the output current on a change of the drive voltage (V_{DS}) is described by output conductance which is defined according to

$$g_d \equiv \frac{\partial I_D}{\partial V_{DS}}. \tag{1.3}$$

The output conductance (g_d) is extracted in the saturated region of the output graph as shown in Figure 1.2c. Preferably this value should be as low a possible to ensure linearity and a good gain when the transistors are used as amplifiers. For an ideal MOSFET the value is zero. However, in real devices drain-induced-barrier lowering (DIBL) and channel length modulation will increase the output conductance.

THRESHOLD VOLTAGE

The threshold voltage (V_T) is used as a reference point when the transistor switches between off and on state. The threshold voltage of a device is in one definition extracted by fitting a line to the point at $g_{m,max}$ and extrapolating the line down to the x-axis a shown in Figure 1.2a. Depending if the V_T is positive or negative the transistor is said to be an enhancement or depletion mode device, respectively. If gate voltage is zero a depletion mode device is in the on-state and a enhancement mode device is in the off-state. Enhancement mode transistor is important for digital circuits that requires that the transistor is turned off when no gate voltage is applied.

SUBTHRESHOLD SLOPE

The subthreshold slope is a partial derivate of the drain current on a logarithmic scale with respect to the gate voltage in the subthreshold region of the transistor. In the literature, the numbers that are provided for this metric represents the inverse subthreshold slope

$$S \equiv \frac{\partial log(I_D)}{\partial V_{GS}}^{-1}, \tag{1.4}$$

which is also refereed to as subthreshold swing. This is a central metric in this work, and will be discussed further ahead.

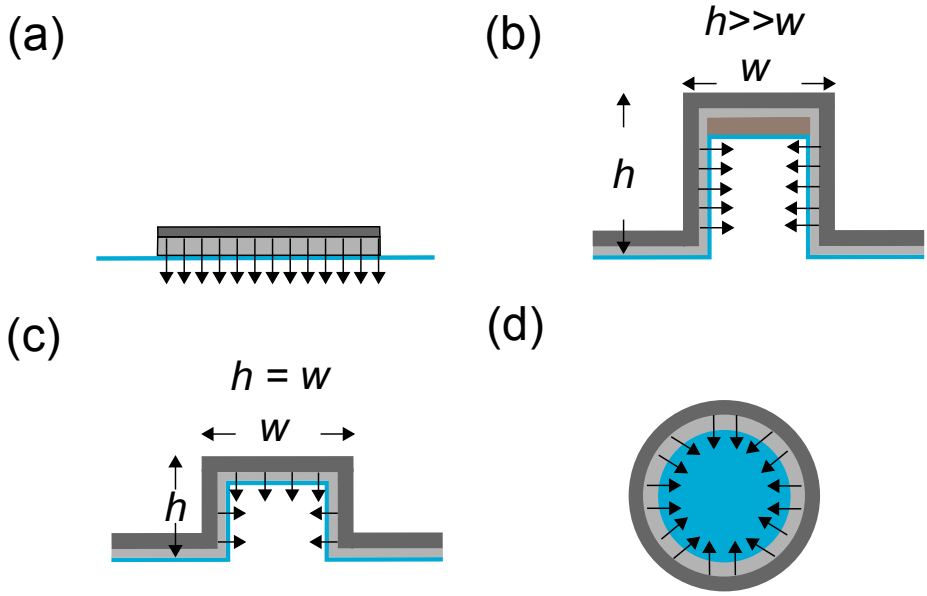

Figure 1.3: Different gate geometries (a) Planar (b) Fin-gate (c) Tri-gate (d) Gate-all-around

1.0.3 III-V SEMICONDUCTORS AND DEVICE GEOMETRIES

Industry have used silicon (Si) and planar gate geometry to fabricate the MOSFETs during most of its existence. The relative simplicity of the planar gate geometry, Figure 1.3a, together with great availability, and low cost of the silicon have been crucial for the development we have witnessed. With the scaling of the transistor, short-channel effects such as drain-induced-barrier lowering (DIBL) have forced the industry to abandon the planar gate geometry. To keep the electrostatic control while the scaling continues, industry has moved to 3D geometry such as Fin-gate (Figure 1.3b) and Tri-gates (Figure 1.3c). To further improve the electrostatics next steep would be to transition to a gate-all-around geometry (Figure 1.3d) [4].

One of the good properties of the Si is its native oxide, which due to its high quality could directly be integrated in the gate-stack [5]. However, scaling of the gate-length has required reduction of the oxide thickness to reduce the impact of short channel effects by improving the electrostatics. To keep the electrical field over the oxide constant also drive voltage was scaled down. However, when the oxide reached a thickness of 1-2 nm, the leakage current through the oxide increased significantly due to quantum mechanical tunneling. This forced industry to replace the silicon dioxide with materials

that exhibit higher dielectric constant (κ) also refereed to as high-κ materials such as aluminum oxide (Al_2O_3) or hafnium oxide (HfO_2). Due to a higher κ value these materials can be thicker, while still allowing to achieve same electrical field.

Although silicon is the material of choice for the industry, there are other semiconductors which can provide some benefits such as better transport properties, direct band-gap, and band-gap engineering when using III-V semiconductors [6]. One of the most crucial properties of any semiconductor is the effective mass, m^*, of the charges and the mobility, μ, which describes how easily charges, electrons or holes, moves in the material when an electrical field is applied. According to the Drude model [7], which relies on classical physics, the relation between these parameters is $\mu \propto (m^*)^{-1}$, where semiconductors with a low effective mass also exhibit a high mobility. As Table 1.1 shows some of the most common III-V semiconductors exhibit a much larger electron mobility than Si. Moreover, the hole mobility is much better for Ge compared to III-V and Si. However, as the devices are scaled down and exhibit more ballistic transport without scattering in the channel, the injection velocity, (v_{inj}), of the charges will be more relevant property for device performance. This parameter describes at which speed the charges enters the channel. Semiconductors with low effective mass exhibit high injection velocity, $v_{inj} \propto (m^*)^{-1/2}$. Combination of the high mobility and injection velocity would result in higher on-current. However, usage of Si has been prolonged by utilizing strain engineering on Si channel [8]. Addition of Ge, into the source and drain of the MOSFET, have led to a tremendous increase of hole mobility due to created uniaxial compresive strain. However, usage of C introduced a tensile strain, which increased the electron mobility instead. Yet, usage of Ge or III-V semiconductors, would allow for much higher mobility and injection velocity.

1.0.4 STEEP SLOPE DEVICES

The scaling of the transistor has resulted in circuits with large device density, reaching a power density of 100 $A/\mu m^2$. A increase in the power density would damage the transistors and for mobile applications with limited cooling this limit is already to high. To reduce the power dissipation, the most effective would be a reduction of the drive voltage which exhibit a quadratic dependence according to the equation

$$P_{disp} = \alpha L_d C V_{DS}^2 f, \tag{1.5}$$

where α is the logic activity factor, f is the operation frequency, L_d is the logic depth, and C is the switched capacitance [10]. However, reduction of the drive voltage will have an impact on either off-current or on-current. This can

Semiconductor	μ_e $[cm^2/(Vs)]$	μ_h $[cm^2/(Vs)]$	$v_{inj,e}$ $[cm/s]$
Si	1400	450	$1.2 * 10^7$
Ge	3900	1900	
GaSb	7000	1000	
GaAs	8500	400	
InAs	40000	500	$3.7 * 10^7$
InSb	70000	1000	

Table 1.1: Mobility of the electrons and holes in different semiconductors, this mobility is acquired in bulk materials [9].

be viewed in Figure 1.4a, to keep on-current at high enough level for a proper circuit operation, off-current will increase with decreasing drive voltage. Explanation for this behavior is due to fixed subthreshold swing of the MOSFET, which is fundamentally limited by the operational temperature of the device. To deal with this issue a device that can reach lower subthreshold swing than a MOSFET needs to be used. These devices are called steep slope devices and compared to the MOSFET, an ideal steep slope device would reach a higher on-current while retaining the off-current, Figure 1.4b. Using Equation 1.4, which describes the subthreshold swing, we can determine what is required of a steep slope device. By rewriting the Equation 1.4 to

$$S = \frac{\partial V_{GS}}{\partial \Psi_S} \frac{\partial \Psi_S}{\partial log(I_D)}, \tag{1.6}$$

where V_{GS} is the gate voltage, and Ψ_S is the surface potential at the interface between the semiconductor and high-κ. The partial derivates $\frac{\partial V_{GS}}{\partial \Psi_S}$ and $\frac{\partial \Psi_S}{\partial log(I_D)}$ reflect the transistor body factor and conduction mechanism in the channel, respectively. By using an equivalent capacitor divider model [11], Figure 1.4c, an approximate solution to the Equation 1.6 can be obtained

$$S \approx \underbrace{(1 + \frac{C_S}{C_{ins}})}_{m} \underbrace{\frac{kT}{q} ln10}_{n}, \tag{1.7}$$

where C_s is the semiconductor capacitance, C_{ins} is the capacitance over the insulator (high-κ), k is Boltzmans constant, T is temperature, and q is elementary charge. For a MOSFET, the minimum value the factor m can achieve is ≈ 1. The value of the n is determined by the operational temperature which is 59.5 mV/decade at 300 K. For a steep slope device, the factors m or n

needs to achieve a lower minimum value. Reduction of m can be achieved by changing the gate-stack of the MOSFET utilized in negative capacitance FET [12, 13]. Reduction of n requires devices that operate with other physical mechanism than thermionic injection such as quantum mechanical band-to-band tunneling a mechanism harvested by the tunnel field-effect transistors (TFETs).

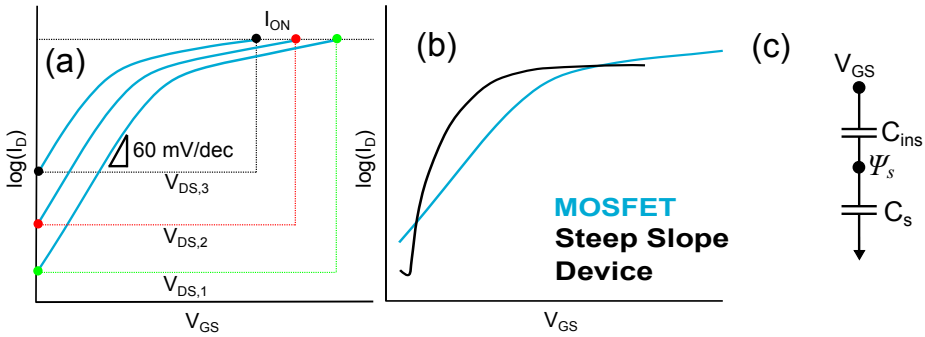

Figure 1.4: (a) Transfer curves showing what happens when the drive voltage (V_{DS}) scales down. Requirement to keep the on-current at same level forces off-current to increase as the drive voltage is decreased. This is due to the fixed subthreshold swing MOSFETs exhibit. (b) Comparison between a MOSFET and steep slope device. Due to a lower subthreshold swing a steep slope device can keep the off-current low and achieve a higher on-current than MOSFET. (c) Illustration of equivalent capacitor divider model of FET, where C_{ins} is the insulator capacitance, C_s is semiconductor capacitance, and Ψ_s is the surface potential.

2

Fundamentals of Tunnel Field-Effect Transistors

This chapter will give a short introduction to TFETs. More detailed information can be found in publications of Seabaugh et. al. [14] and Ionescu et. al. [10].

2.1 PRINCIPLES OF THE TUNNEL FIELD-EFFECT TRANSISTORS

The MOSFET is turned off and on by raising and lowering a potential barrier in the channel region using the gate voltage. The transport over the barrier occurs through thermionic emission where only carriers with an energy higher than the barrier can contribute to the current. Thereby, the distribution of the charges in the Fermi-Tail will determine how quickly a MOSFET can be switched off and on. The efficiency is described by the subhtreshold swing of the device, and the lowest value can be calculated using

$$S = ln(10) * \frac{kT}{q}, \tag{2.1}$$

where k is Boltzmans constant, T is temperature, and q is elementary charge. At room temperature the lower limit for a MOSFET, controlled by thermionic emission, is 58.1 mV/decade, usually rounded up to 60 mV/decade.

Tunnel Field-Effect Transistors are designed to filter out the high-energy carriers in the Fermi-tail, thereby these devices can switch between the off and on-state with a subthreshold swing below 60 mV/decade. The band diagram of the TFET and MOSFET can be viewed in Figure 2.1. Similar to the MOSFET, Figure 2.1a, a TFET is turned off and on by lowering and raising the bands in the channel as illustrated in Figure 2.1b. In the off-state, the channel

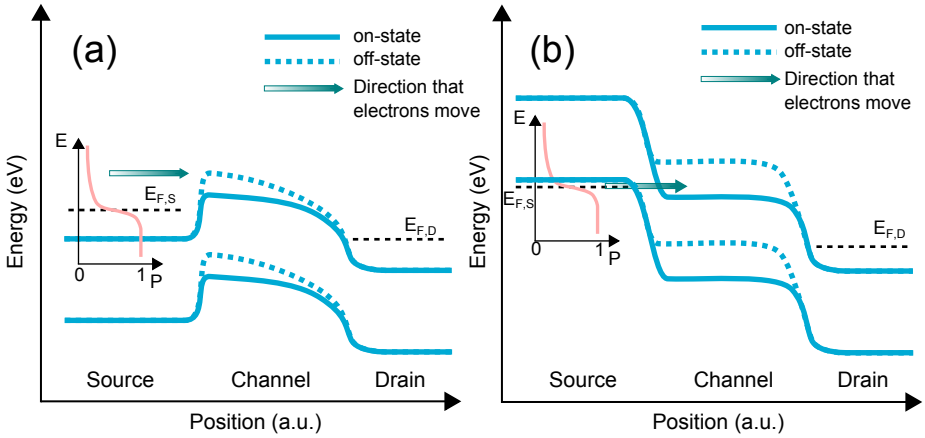

Figure 2.1: Comparison beteen the MOSFET and TFET. (a) Band diagram of a MOSFET in the on and off state. $E_{F,S}$ and $E_{F,D}$ is the Fermi-level at the source and drain, respectively. P is the occupation probability. (b) Band diagram of a TFET in the on and off state.

band-gap is in line with the Fermi-level of the source, thereby electrons in the source have no states to tunnel to in the channel. The device is turned on when the conduction band of the channel is lowered below the Fermi-level in the source.

Since a TFET relies on tunneling it is challenging to reach as high current as in a MOSFET. The influence of this effect can be reduced by usage of III-V materials that provides possibility to design devices with heterojunctions that have thinner barriers. These heterojunctions can either be of type II (staggered) or type III (broken) shown in Figure 2.2b and Figure 2.2c, respectively. As presented in Paper VI the type of the junction between different materials can change with dimensions, since confinement can increase the band-gap. As shown, for example the heterojunction between the InAs and GaSb is broken for bulk, but in nanowires with InAs diameter below 8 nm the heterojunction become staggered.

2.2 MODEL FOR 1-D TUNNEL FIELD-EFFECT TRANSISTOR

A simple model for 1-D TFET with a homojunction will be presented in the following text. More detailed derivation and explanations can be found in Ref. [14]. Using the Landauer-Buttiker formalism the current trough the device can be described using

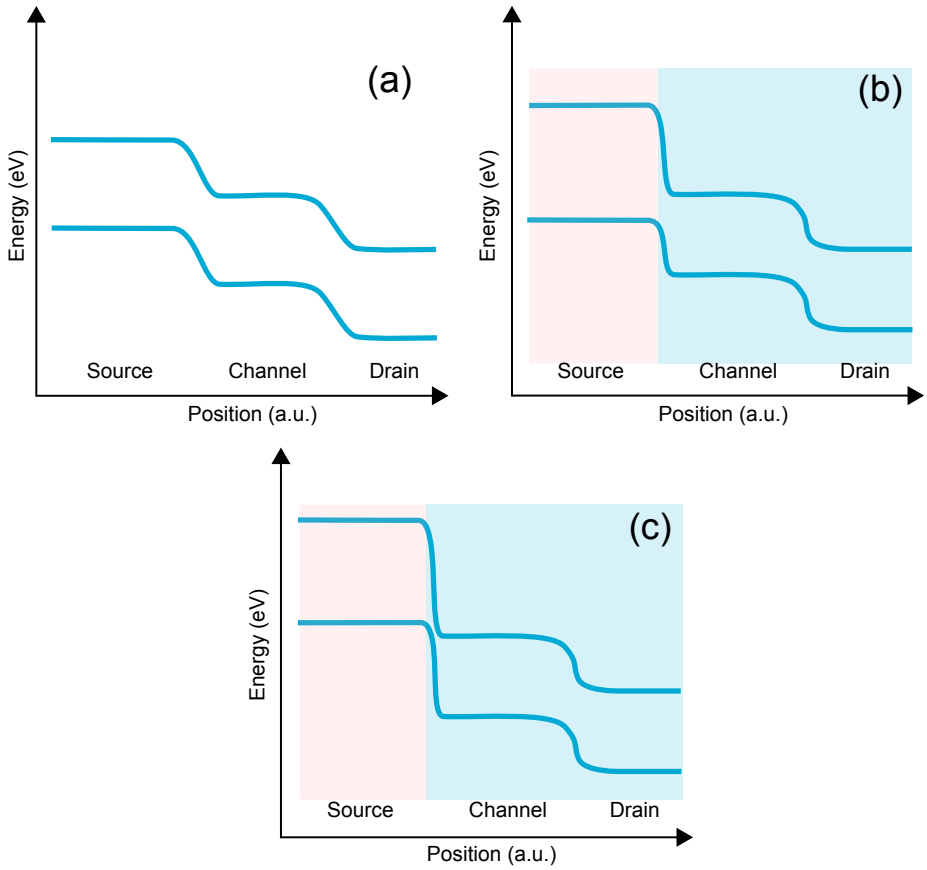

Figure 2.2: TFETs with different band alignments (a) Homojunction (b) Heterojunction with staggered band-gap alignment. (c) Heterojunction with broken band-gap alignment.

$$I_{ON} = \frac{2q}{h} \int_{E_{v,s}}^{E_{c,c}} T(E) f_0(E, E_{F_S}) dE, \tag{2.2}$$

where h is Planck's constant, q is elementary charge, T(E) is transmission probability, f_0 is Fermi-Dirac function, E_{F_S} is the source Fermi energy, $E_{c,c}$ is the channel conduction sub-band edge, and $E_{v,s}$ is the source valence sub-band edge. The small diameter of the channel will result in single sub-band and quantization will increase the band-gap. Furthermore, it is assumed that the doping in the source is degenerate and V_{DS} is large enough to reduce

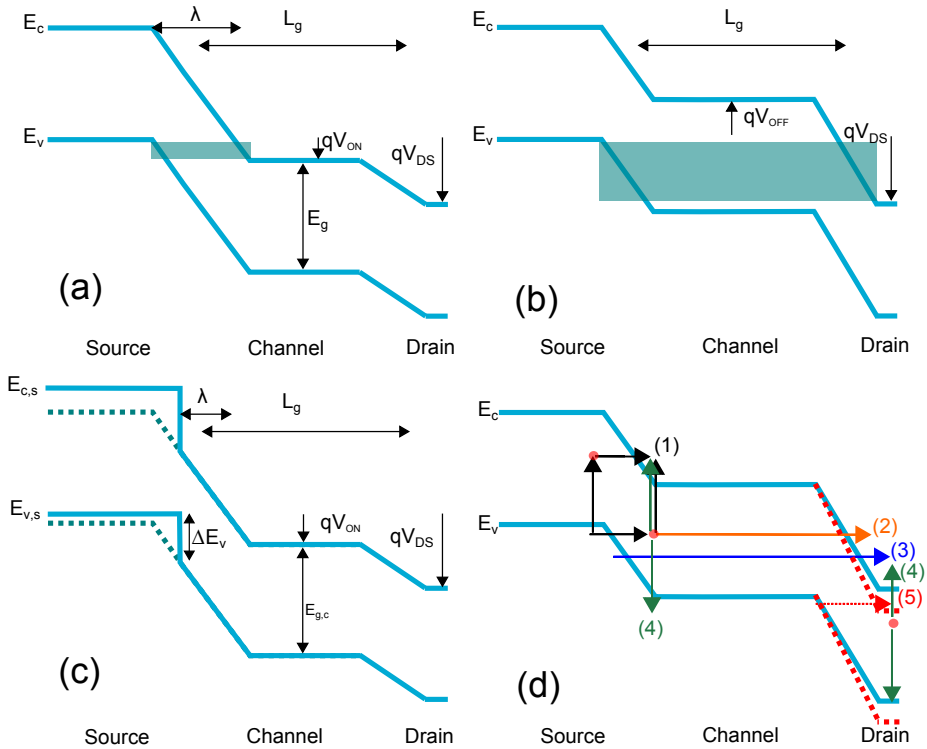

Figure 2.3: TFETs model (a) A TFET with homojunction in on-state, where λ corresponds to geometric length scale calculated using Poison's equation, E_g is the band-gap, qV_{ON} is band-shift due to applied gate voltage, and qV_{DS} band shift due to applied drain voltage. (b) A TFET with homojunction in the off-state. (c) A TFET with a heterojunction, where $E_{g,c}$ is the band-gap in the channel. Dotted line shows how conduction and valence band would be in a TFET with homojunction. (d) Leakage mechanism in real TFETs (1,2) Defect/Trap assisted tunneling (3) Tunneling between source and drain (4) Shockley-Read-Hall (5) Reverse tunneling that can occur if $V_{DS} > E_{g,ch}/q$

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the back injection of the charges from the drain. At temperature of 0 K, the Fermi-Dirac function will be ≈ 1 and Eq. 2.2 can be rewritten to

$$I_{ON} \approx \frac{2q}{h} \int_0^{qV_{ON}} T_{ON}(E)dE, \tag{2.3}$$

where integration over the tunneling window between $E_{v,s}$ (=0) and qV_{ON} gives the current in the on-state. The charges tunnel between the valence

and conduction band through a parabolic barrier, for which transmission probability can be determined using the WKB-approximation

$$T_{ON}(E) = exp\left(-2\int_{x_1}^{x_2} |k_x(E)|\, dx\right), \tag{2.4}$$

where the imaginary k-vector

$$Im(k_x) = \frac{1}{\hbar}\sqrt{\frac{2m^*}{E_g}}\sqrt{\frac{E_g^2}{4} - q^2\varepsilon^2x^2}, \tag{2.5}$$

is obtained from Kane's two-band model [15]. Used constants in the Eq. 2.5 are: $\hbar$ is the reduced Planck's constant, m^* is the effective mass, q is the elementary charge, E_g is the band-gap, and ε is the electrical field. Equation 2.4 is integrated over classical turnings points,

$$x_1 = -\frac{E_g}{2q\varepsilon}, x_2 = \frac{E_g}{2q\varepsilon}, \tag{2.6}$$

where the result can be seen in following equation

$$T_{ON}(E) = exp\left(\frac{\pi\sqrt{m^*}E_g^{3/2}}{2\sqrt{2}q\hbar\varepsilon}\right) \tag{2.7}$$

and the electric field is approximated according the equation

$$\varepsilon \approx \frac{E_g + qV_{ON}}{q\lambda}, \tag{2.8}$$

where λ approximately corresponds to the geometric length scale obtained using Poison's equation. Some of the parameters used in Eqs. 2.3 - 2.8 can be viewed in Figure 2.3a.

The final equation that describes the current in the on-state is

$$I_{ON} = \frac{2q}{h}T_{ON}V_{ON}, \tag{2.9}$$

which is obtained by using Eqs. 2.7 and 2.3.

The current in the off-state will be determined, in ideal case, only by the tunneling between the source and drain as illustrated in Figure 2.3b. The barrier that charges need to pass is modeled as a rectangular barrier using the equation

$$I_{OFF} \approx \frac{2q}{h}\int_{E_{c,d}}^{E_{v,s}} exp\left(-\frac{2\sqrt{2m^*}L_g}{\hbar}\sqrt{E\left(1-\frac{E}{E_g}\right)}\right) dE, \tag{2.10}$$

where $E_{c,d}$ is the conduction band in the drain and $E_{v,s}$ is the valence band in the source. According to equation 2.10, without any material imperfections, the off-current of a TFET is limited by the gate-length and band-gap of the channel material. This will set a limit on how short gate-lengths that can be used in TFETs [16,17]. Combining equations 2.9 and 2.10, the currents through a TFET with 1D channel and homojunction can be described. Interested readers can find the derivation of the equation for TFETs with bulk channel in Ref. [14]. As presented in Paper VI, currents for a TFET with 1D channel and heterojunction can be obtained by modifying some of the previous equations. For TFETs with a heterojunction, the barrier will be thinner as compared to a homojunction as shown in Figure 2.3c. Equation 2.6 for classical turnings points is modified according to

$$x_1 = -\frac{E_g}{2q\varepsilon} + \frac{\Delta E_v - E}{q\varepsilon}, x_2 = \frac{E_g}{2q\varepsilon}. \tag{2.11}$$

Furthermore, equation 2.8 for electrical field is modified to equation

$$\varepsilon \approx \frac{E_g - \Delta E_v + qV_{ON}}{q\lambda}. \tag{2.12}$$

Inserting equations 2.11 and 2.12 into the equation 2.4 we obtain the new equation

$$T_{ON}(E) = exp\left(\frac{\sqrt{m^*}E_{gc}^{3/2}}{2\sqrt{2}q\hbar\varepsilon}g(\theta)\right), \tag{2.13}$$

where

$$g(\theta) = \left[\frac{\pi}{2} - \left(\theta\sqrt{1-\theta^2} + sin^{-1}(\theta)\right)\right], \tag{2.14}$$

and

$$\theta(E) = 2\left(\frac{\Delta E_v - E}{E_{gc}}\right) - 1, \quad 0 < E < \Delta E_v. \tag{2.15}$$

Inserting Eq. 2.13 in to the Eq. 2.2, on-current for a 1D TFET with staggered heterojunction can be calculated. Furthermore, equation 2.13 will also describe 1D TFETs with homojunction and heterojunction with broken band-gap alignment, which will occur when equation 2.15 becomes -1 or 1, respectively.

The model presented in this section is a very simplified view of the TFET. In real devices the performance is limited by material defects that are not considered in the model, Figure 2.3d. Defects in materials, either in bulk or at interfaces, will contribute with leakage paths as they will add energy states in the band-gap to which the electrons/holes can tunnel to and from. This effect is referred to as defect/trap assisted tunneling (DAT/TAT) [18]. Furthermore,

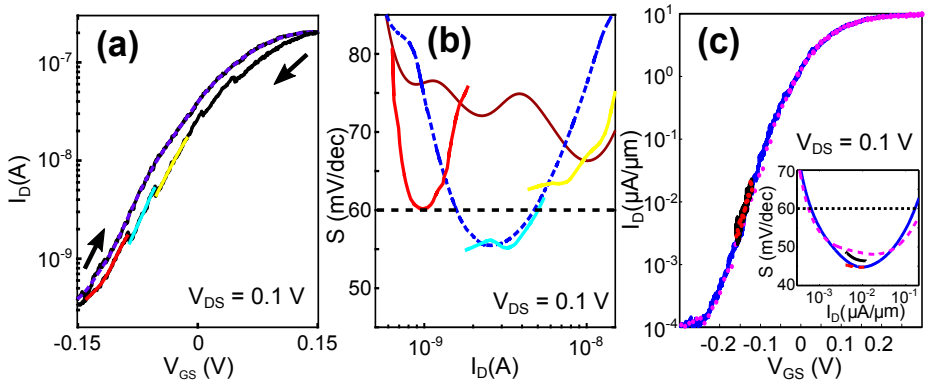


Figure 2.4: Transfer characteristics of vertical InAs/InGaAsSb/GaSb nanowire TFETs from Papers I and II (a) Gate voltage is swept from low to high and back, generating different results due to interaction of charges with defects in the high-κ. [Paper I] (b) I_D vs subthreshold swing extracted from the sweeps in a. (c) By using sweep in different range and directions, the effects of hysteresis and interaction with oxide defects can be studied. [Paper II]

Shockley-Read-Hall generation in depleted source and drain regions will add another leakage path [19]. The reverse tunneling of minority carriers into the channel from drain will occur if used V_{DS} is larger than $E_{g,ch}/q$. Furthermore, leakage through high-κ will add another leakage path, not shown in Figure 2.3d. These leakage paths will have an impact on the off-current and the subthrehold swing of the devices. Impact of these effects will be discussed in the next sub-chapter.

2.3 CHARACTERIZATION OF TUNNEL FILED-EFFECT TRANSISTORS

TFETs exhibit a number of properties in their electrical characteristics that differ from conventional MOSFETs. Three of the main characteristics are the ability to operate below 60 mV/decade, negligible temperature dependence of the subhtreshold swing, and negative differential resistance (NDR) at forward bias. Theoretically, the properties of the TFET are determined by the materials in the heterojunction. However, defects in the bulk of the semiconductor, at the interface or in the high-κ will deteriorate the performance. Figures 2.4a and b, show an example of how defects in the oxide influence the performance of the device. When a highly scaled device operates in the subthreshold region, the number of charges is relatively small thereby effects of charges interacting with defects in oxide will have noticeable impact on the subthreshold swing. As presented in Figure 2.4a, a sweep from low to

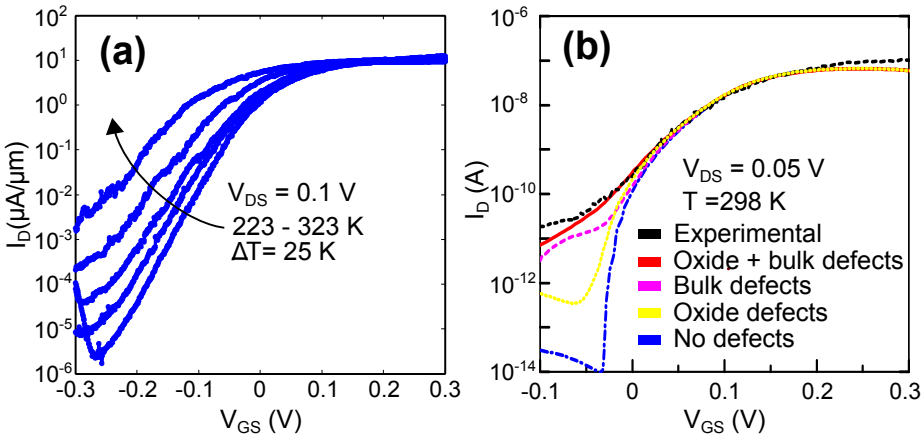


Figure 2.5: Temperature dependence and modeling of the devices in this work. (a) Transfer curves of a device at different temperatures. [Paper I] (b) Modeling of transfer curves at room temperature showing what influence different type of defects have on the performance in the subthreshold region. [Paper II]

high voltage and back show different behavior. In the on-state when there is larger amount of charges in the channel, the defects in the oxide will be charged. On the sweep down, the charges in the oxide will tunnel back to the channel impacting the subthreshold swing as shown in Figure 2.4b. Thereby, when measuring it is necessary to measure in different directions and with different ranges to confirm the operation below subthreshold swing, Figure 2.4c. Influences from the oxide defects can be removed by using pulsed measurements [20, 21]. In this type of measurement the applied signal on the gate is a short pulse whose period is much shorter than the time constant of the capture or emission process.

In an ideal device, the subthreshold swing should not depend on the temperature as the Fermi-Tail is filtered out by the band-gap. However, defects in the band-gap will open additional paths for carrier transport. In the off-state, when there should be no band-to-band tunneling (BTBT), these extra paths will allow the charges to bypass the barrier. This is referred to as Defect-assisted tunneling. As Figure 2.5a shows, devices in this work also exhibit temperature dependence. Modeling of these devices in Paper I, (Figure 2.5b) indicates that bulk defects are the main limitation of the subthreshold swing and off-current.

The negative differential resistance observed in TFETs, Figure 2.6a, have been extensively studied in Esaki diodes [22, 23]. However, compared to the diode, the TFET has a third terminal (V_G) and the channel region is not doped.

Using common drain configuration the bands can be swept with V_{SD} as shown in Figure 2.6b-d. Using the gate terminal, the position of the Fermi-level can be adjusted in similar way as when changing the doping in traditional diodes. It is tempting to use diodes to evaluate the heterojunction of a material system as the fabrication of the diodes is more simple [24–27]. However, this is not trivial, since the heterojunction of a diode is generally heavily doped on both sides. The heavy doping is necessary to obtain high peak currents, which introduces additional defects that are not present in TFETs.

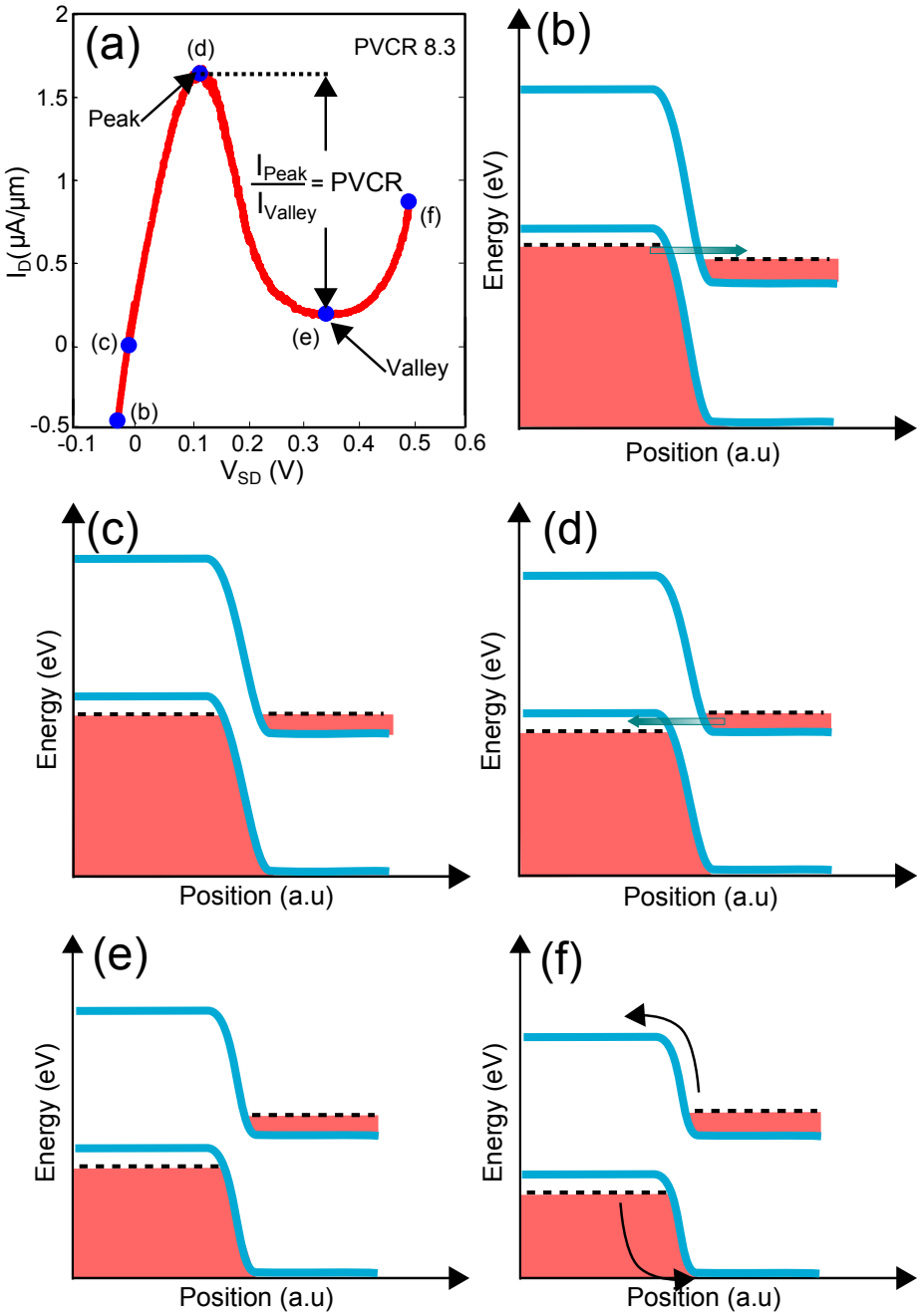


Figure 2.6: Negative differential resistance and the mechanism behind this behavior (a) NDR in output of a TFET at certain V_{GD}. Definition of the peak-to-valley-current ratio (PVCR) is given in the figure. (b-f) As the V_{GD} is swept the net current will be determined by relative positioning of bands.

3

Fabrication

Scaling of transistors has been the main path to improve the performance and has therefore relied on major advancements in fabrication techniques. The vertical geometry provides us with new types of challenges and thereby also requires new solutions. The usage of more than one material in the heterostructure of the TFETs in this work contributes to further increase of the complexity. If these challenges are tackled in a correct manner one can produce devices that benefits from great electrostatics of vertical nanowires and performance enhancement provided by the properties of III-V materials such as direct band-gap and higher injection velocity than Si. This chapter consists of three sub-chapters; growth of the nanowires, a general description of the fabrication process, and challenges to work with vertical nanowire transistors.

3.1 GROWTH OF THE NANOWIRES

Generally, fabrication of semiconductor nanowires can be achieved by using either top-down or bottom-up approach [28]. In the top-down approach, thin-films are grown followed by masking and etching of un-masked regions. The bottom-up approach instead uses seed-particles to catalyze or templates to restrict the growth in selected region. Using these methods nanowires of a numerous different semiconductor materials has been fabricated such as: Si, Ge, InAs, InP, GaAs, GaSb, InGaAs, etc [29, 30]. In this work, a bottom-up method is used with Au-seed particles as catalysts that are positioned on an InAs layer on top of a Si-wafer [31]. These wafers allows for usage of cheap Si-wafers and simple integration of III-V materials. Seed particles are defined using the steps described in Figure 3.1.

The size of the particles is determined by the used electron dose, the resist thickness, and the thickness of evaporated metal layer. This process allows for simple scaling of the numbers of nanowires in every device. The growth of the nanowires is performed using metalorganic vapor phase epitaxy (MOVPE). Group III-precursors (TMGa, TMIn) and group V-precursors (TMSb, AsH_3) are used as the source materials. In theory, the composition and crystal structure of the nanowires are controlled by the growth temperature, and the amount of and ratio between the precursors in the chamber. However, this picture is more complicated in reality since the ratio that matters is ratio between the precursors in the proximity of the seed particles [32, 33]. This ratio is influenced by the surface of the sample, the distance between the seed particles as they are competing against each other for the material. The growth direction for the nanowires is [111]B, and with crystal structure of either zincblende (ZB) or wurtzite (WZ). It should be mentioned that the crystal structure a material exhibits in bulk is not necessarily the same for the nanowires grown with the bottom-up method. InAs have ZB in bulk, but can for certain growth conditions be WZ. Furthermore, some of the regions of the nanowires needs to be doped (Figure 3.2) to reduce influences of resistances, such as access-resistance or contact-resistance. These dopants are introduced during the growth using TESn for n-doping and DEZn for p-doping. Adding these materials can further complicate the growth and influence the morphology of the nanowires. Extensive work in Lund has build up a vast knowledge base and perfected the growth process, which has resulted in nanowires of high material quality as shown in many publications [32, 34–36]. This quality is necessary to fabricate devices with great performance, as these nanowires form the channel through which charges are transported. Schematic images of nanowires used in this thesis can be viewed in Figure 3.2. One mayor challenge in following steps is to fabricate the devices while maintaining the quality.

3.2 FABRICATION PROCESS OF THE VERTICAL NANOWIRE TRANSISTORS

The vast majority of the devices in this work were manufactured by the steps described in this section. For interested readers there is a more detailed description in Appendix A.

1. **Digital etching:** Using ozone and citric acid nanowires are digitally etched, this removes the GaSb-shell that was formed during the growth and reduces the diameter of the InAs channel. Challenges with this step is discussed in section 3.3.1 and effects of diameter reduction will be further discussed in Chapter 4.

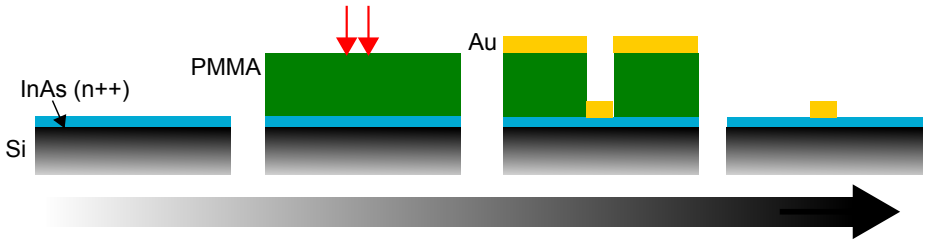


Figure 3.1: Definition of the Au-seed particle. From left to right: Si wafer with integrated InAs layer is spin-coated with PMMA. By using the electron beam lithography, position and size of the seed particles is determined. A gold film is evaporated and lift off is performed to form the particles.

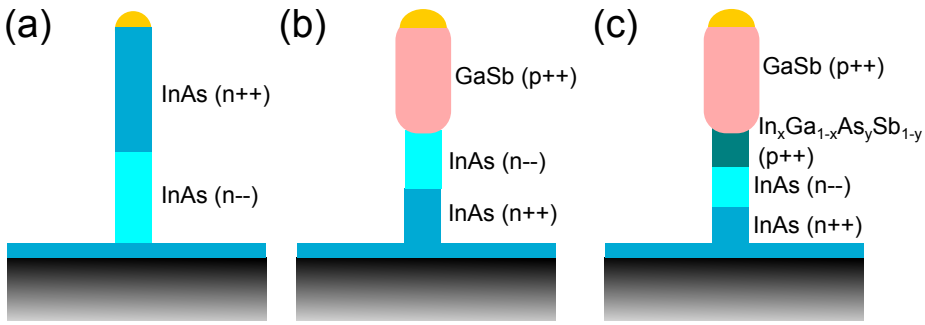


Figure 3.2: (a) InAs nanowire used in paper VII for fabrication of MOSFET. (b) InAs/GaSb nanowires used in paper V and paper VI for fabrication of heterojunction TFETs with broken band-gap alignment. (c) InAs/InGaAsSb/GaSb nanowires used in paper I, II, III, and IV for fabrication of heterojunction TFETs with staggered band-gap alignment.

2. **High-κ:** Directly after digital etching, the surface of the sample is covered with a high-κ bilayer, which together with gate-metal forms the gate-stack of the transistor. Atomic layer deposition (ALD) is used to form the bilayer with 5 cycles of Al_2O_3 at 300 ^{o}C and 36 cycles of HfO_2 at 120 ^{o}C. Prior to the start of the deposition of the Al_2O_3, a couple of Al pulses are used to clean the surface thereby improving the interface between the high-κ and III-V material [37,38].

3. **InAs-mesa:** The InAs-mesa is etched out using UV-lithography and wet-etching to isolate the devices. This step can also be performed after the gate-definition step depending on which spacer technology is used for the bottom spacer.

4. **Bottom-spacer:** A number of different materials (S1800 photo-resist,

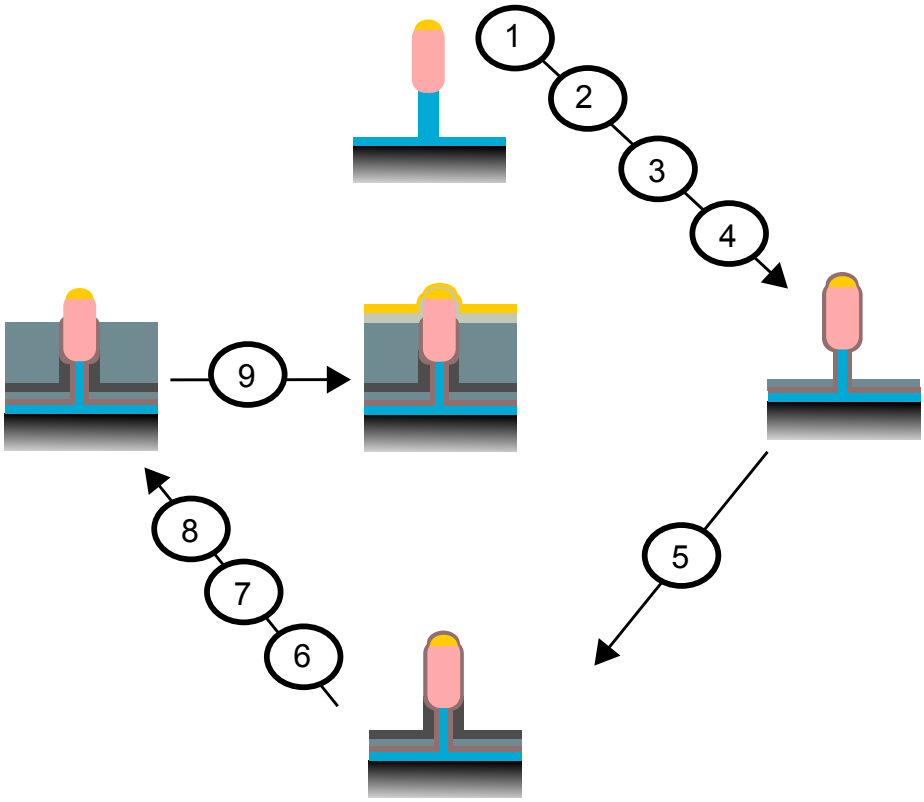


Figure 3.3: Flow chart of the fabrication process of the vertical transistors. 1. Digital etching, 2. Applying high-κ, 3. InAs-mesa etching, 4. Formation of bottom spacer, 5. Definition of the gate-length and gate-pad, 6. Formation of top-spacer, 7. Making the via-holes 8. Removing the high-κ from the top of the nanowire and via-holes 9. Top-metal deposition and patterning

Hydrogen silsesquioxane (HSQ), and Silicon oxide (SiO_x)) and methods have been used to form the bottom-spacer for the transistors in this work. Techniques and challenges to work with these different materials are discussed in section 3.3.2.

5. **Gate:** A 60-nm-thick tungsten (W) film is sputtered on the sample. The physical gate-length is set by spin-coating the sample with organic photo-resist (S1800) which covers the nanowries completely. Using O-plasma, the thickness of the resist is reduced to the desired height. Using reactive ion etching (RIE), the tungsten is removed from the exposed surfaces with a SF_6/Ar mix. More about gate-definition is

discussed in section 3.3.3.

6. **Top-spacer:** Except for the MOSFETs in paper (VII), the top-spacer for all transistors manufactured in this work is produced using organic spacer S1800. Explanation for this can be found in section 3.3.2. The spacer is formed by spin-coating the sample with organic photo-resist covering the nanowires completely followed by etching of the resist using O-plasma to desired thickness.

7. **Via-holes:** Using S1800 and UV-lithography the via holes are defined. The holes through the spacers are made using reactive etching and wet etching.

8. **Removing of the high-κ:** The high-κ on the top of the nanowire and in the drain via-hole is removed using diluted HF.

9. **Top-metal and contact-pads:** The top-metal is made of Ni and Au, applied by either sputtering or evaporation. If evaporation is used, the sample is covered with LOR3A and S1800 resist, which is patterned using UV-lithography prior to the evaporation. After the evaporation, the film is removed from un-patterned surfaces with lift-off. For sputtered metal films, S1800 and UV-lithography is used to mask areas where the pads would be. Metal film in uncovered areas is removed using wet-etching.

3.3 CRITICAL PROCESSING STEPS

In this section, the most crucial steps are discussed in detail. Those steps are digital etching, spacer technologies, gate definition, and contacts formation.

3.3.1 REDUCTION OF NANOWIRE DIAMETER USING DIGITAL ETCHING

Compared to an ordinary wet etching process, the digital wet etching is a self-limiting process. Many commonly used solutions for wet etching contain a mix of one or more oxidizers (H_2O_2, HNO_3, concentrated H_2SO_4) and etchants [39,40]. During etching the surface of semiconductor is continuously oxidized and the oxide is etched keeping the process continuous. If the oxidizer is removed, the etching can continue in some case although at a significantly reduced rate. In this work commonly used mix of citric acid and hydrogen peroxide, [41, 42] , was modified by replacing the oxidizer with ozone, thereby achieving a digital wet etching process. This process fulfilled the requirements of high selectivity towards the GaSb and high reproducibility. As Figure 3.4a and b shows, the diameter of the GaSb has

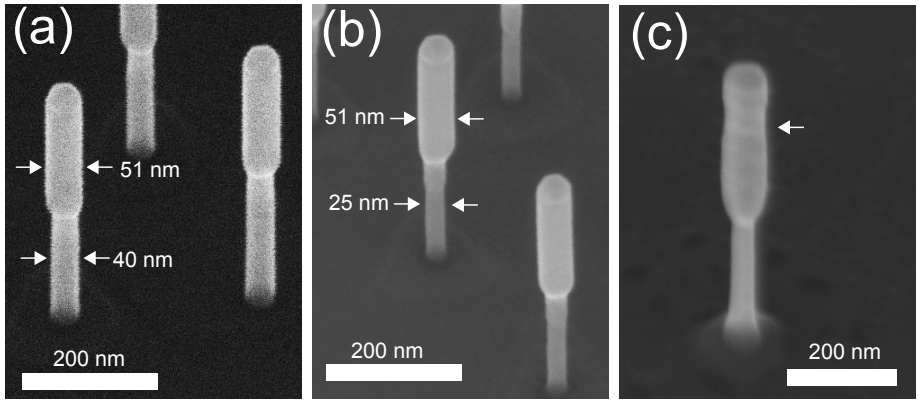


Figure 3.4: (a) InAs/InGaAsSb/GaSb nanowires before digital etching. The thickness of the InAs is 40 nm and of the GaSb is 51 nm. (b) Nanowires from same sample after 5 cycles of digital etching, the diameter of InAs has decreased with 15 nm. Diameter of GaSb has not changed. (c) InAs/GaSb nanowire that was exposed to O-plasma prior to the digital etching shows damage on the GaSb after the digital etching.

not been changed even after 5 cycles, which have reduced the diameter of the InAs from 40 to 25 nm. Furthermore, the process exhibits high reproducibility where the etching rate is approximately 1.5 nm/cycle. Even if this process shows great reproducibility and selectivity, experience also tells us that it is very delicate. Any extensive exposure of the nanowires to processing prior the digital etching can have influence on the selectivity and etching rate. As shown in Fig 3.4c, the top GaSb segment was etched on the nanowires that where exposed to plasma in previous steps. Other limitation is breaking of the nanowires, when cycling between dry oxidation step and wet etching step. The solvent is removed from the sample using dry blowing, which results in destroyed nanowires due to surface tension that bends the nanowires and breaks them [43]. This can be solved using other drying techniques, such as critical point drying [44].

3.3.2 SPACER TECHNOLOGIES USED FOR VERTICAL NANOWIRE TRANSISTORS

The function of the spacer-film is to separate the terminals (Source, Gate, Drain) of the transistor. The spacer-film should be made of low-κ material to reduce the parasitic coupling between the metal-layers and rigid enough to give mechanical stability to the transistor [45]. As presented in section 3.2 we use two spacer layers for the devices in this work, even if their functionality

is the same, there can be different requirements on them. This is because every layer in the process need to be compatible with materials already on the sample and with the steps that follow. For example, the top-spacer needs to withstand HF etching used to remove the high-κ on the top of the nanowires, this requirement is less important for the bottom spacer. However, the bottom spacer should be able to withstand high temperatures during post metal annealing >250 ^{o}C of the gate. Three different materials have been used to fabricate bottom and top spacers: organic photo-resist S1800, hydrogen silsesquioxane (HSQ), and silicon oxide (SiO_x).

ORGANIC SPACER

The steps of how the organic spacer is applied is presented in Figure 3.5a. The sample is first spin-coated with S1800 followed by permanent baking of the resist. Using O-plasma, the resist is thinned down to the desired thickness. The organic resist exhibits a couple of desirable properties when working with novel devices and processes. It is quick to apply without need of high temperature and the thickness is easily trimmed down to the desired thickness utilizing O-plasma. If not permanently baked, it is simple to remove using acetone without damaging the structure, what makes it forgiving for mistakes. Furthermore, it can easily form thick layers >1 um without cracking due to stress as e.g. HSQ. Additionally, it can withstand HF, which makes it suitable as top-spacer. However, the organic spacer can attract moisture and this induce potential barriers due to charging thereby deteriorating the performance of the device. Furthermore, the thickness of a spin coated resist increases close to the edges which makes it difficult to achieve spacer-thickness below 60-70 nm with a good yield. During O-plasma etching the resist is etched more quickly at the edges making it difficult to achieve good enough control, this issue is addressed by use of sacrificial pieces placed around the real sample. Over time, the performance of the devices with organic spacers deteriorate [46]. Usage of O-plasma to thin down the resist can have negative effect on the device performance, this is especially true for devices with organic bottom spacer where the channel region is exposed.

HYDROGEN SILSESQUIOXANE

Historically, hydrogen silsesquioxane (HSQ) was used to planarize uneven surfaces, due to its great gap-filing properties [47]. During this process, the HSQ is spin-coated on the sample, followed by curing at temperatures of 600-800 ^{o}C. During the curing -O-H bonds are broken and replaced by Si-O, thereby the HSQ transforms to SiO_x in the first steps of curing and if temperature is high enough it continues its transformation to SiO_2 [48].

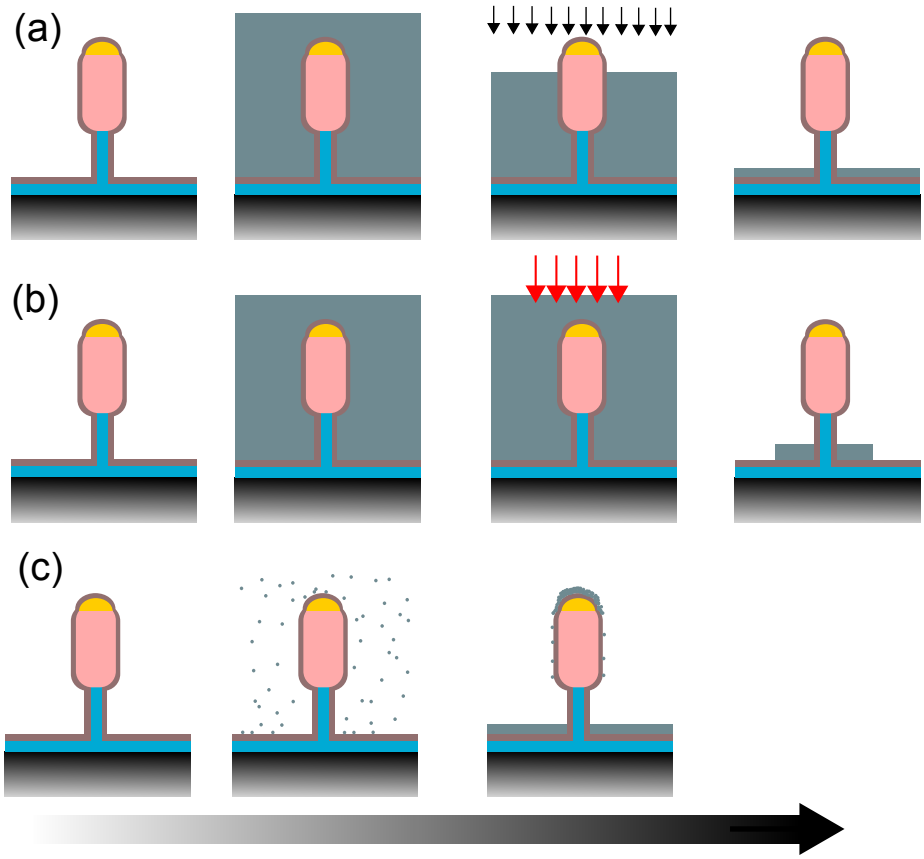


Figure 3.5: (a) Organic spacer (S1800): the sample is spin-coated with organic spacer followed by permanent baking. The spacer is thinned down using reactive ion etching and O-plasma. (b) HSQ spacer: the sample is spin-coated with HSQ, followed by soft-baking to remove the solvent. Selected areas are exposed with certain electron dose using electron beam lithography. HSQ is developed in TMAH and cured using rapid thermal processing (RTP). SEM images of HSQ can be viewed in Figure 3.6. (c) SiO_x spacer: Using thermal evaporation, the sample is covered with SiO_x of a certain thickness. The sample is rotated during evaporation and no tilt is used. After evaporation the sample is etched in HF to remove the flakes on the sidewall of the nanowires.

During 1997-98 the first reports came that the HSQ could be used as a negative resist in electron beam lithography (EBL) [49]. It was demonstrated that the HSQ could be transformed using an electron beam instead of curing and thus it was possible to form patterns. Developer for the HSQ is a base such as potassium hydroxide (KOH), sodium hydroxide (NaOH) or tetramethylam-

monium hydroxide (TMAH) [50, 51]. Since the first demonstration, a large number of publications have reported the usage of HSQ as the negative resist [52–54]. HSQ exhibit a number of good properties for usage as spacer, it has a low κ of 3-3.9, it can withstand high temperatures and is mechanically stable.

Usage of HSQ as spacer material for vertical nanowires was demonstrated with Si-nanowires where the HSQ layer was curred and then etched down to wanted thickness using wet etching with HF [55]. This technique has limited use for III-V nanowires in this work because these structures can not withstand temperature above >400 ^{o}C without decomposing. Some tests, to etch cured HSQ (350 ^{o}C), were conducted with mixed success. Difficulty to achieve a good reproducibility and faster etching along the nanowires, forced us to abandon this approach. To circumvent this issue, the curing at high temperature was replaced by usage of electron beam exposure, see Paper VII. In Figure 3.5b, the steps used to fabricate the HSQ spacer are presented. The process begins with spin coating of the HSQ on the sample followed by soft-baking of the HSQ. Using certain electron dose and voltage, selected areas are exposed. The HSQ is developed using TMAH and cured at 300 ^{o}C in N_2/H_2 ambient atmosphere to remove solvent and neutralize lose O-bonds. The final thickness of the HSQ-spacer in this process relies on a number of parameters such as initial HSQ thickness, baking conditions before the exposure, electron dose, acceleration voltage, developer concentration, development time, and developing temperature [56–58]. The influence of the initial thickness on the final thickness and used electron dose can be viewed in Figure 3.6a. The sensitivity of the HSQ increases with increasing initial thickness, the same effect can be achieved with increasing prebaking temperature or reduction of developer concentration. The opposite effect is achieved using higher developer temperature. Generally, an increase of sensitivity will reduce the contrast of the HSQ. During usage of this process on real devices all parameters except for the used electron dose where kept constant. The final result can be viewed in Figure 3.6b, where a pad was written locally around the nanowires.

Advantages of this process is the possibility to determine the spacer thickness for every individual structure on the sample. Spacers, with thickness of 40-50 nm, can be produced with good control (Figure 3.6c). Furthermore, the HSQ-pad is written locally, thereby the InAs-mesa can be etched after the gate fabrication, which simplify the processing. The fabrication of the HSQ spacer is performed at low temperature (<300^{o}C), however if required the HSQ can withstand post metal deposition annealing. Furthermore, compared to the organic spacer, the channel region of the transistor is not exposed to harmful plasma processing. Observed ability of the HSQ to self-align to the nanowire arrays and surface unevenness is presented in Appendix B.

The HSQ was used for both top and bottom spacers in Paper VII. To achieve this, the high-κ was removed from the top of the nanowires using HF, followed by formation of the top HSQ spacer. This was necessary to do, otherwise the HF would have etched away the HSQ. This method is unfortunately not possible to use with InAs/GaSb nanowires, because the developer TMAH etches GaSb very quickly [59]. Furthermore, cracks can form in the HSQ-pad when the initial thickness of the HSQ reaches above 600 nm, Figure 3.6d [60].

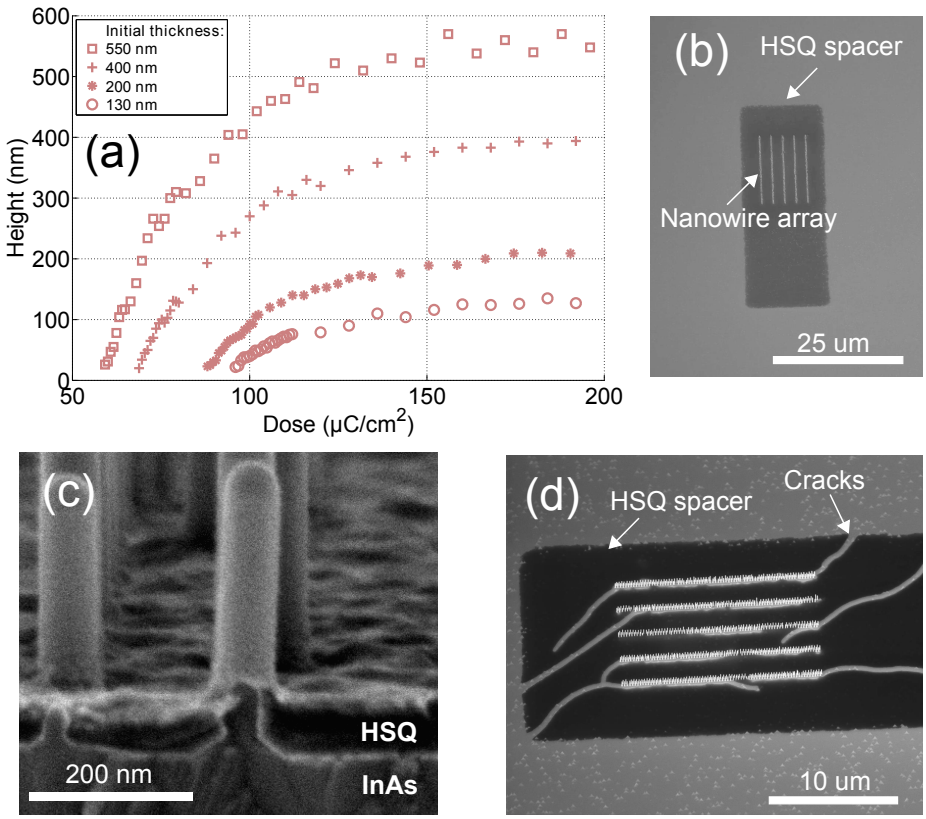


Figure 3.6: (a) Dependence of the final thickness of the HSQ spacer and electron dose. Increasing the initial HSQ thickness increases the sensitivity of the HSQ. (b) Finished HSQ pad surrounding the nanowire array. (c) Cross-section of a HSQ pad with a thickness of 44 nm. The sample was covered with a Ti-film prior to cleaving to enhance the contrast and remove the charging. (d) If the HSQ thickness becomes too large it can start to crack. In this case, the HSQ started to crack along the nanowire arrays.

SILICON OXIDE

The SiO_x has been used as bottom spacer in Papers I-IV in this work and also previously by Thelander et. al. [61]. Compared to the organic spacer and HSQ, the fabrication process of the SiO_x spacer is easier. The final thickness of the spacer is determined during the evaporation. This results in a process with great reproducibility and films with thicknesses of 15-20 nm can be fabricated. For the nanowires used for the TFETs in this work, the thicker GaSb at the top shadows the thinner InAs section which results in no or little deposition of the SiO_x flakes on the channel region of the devices as shown in the Figure 3.5c. The SiO_x spacer can withstand as high temperature as HSQ, it is etched slower by HF but still fast enough to be unusable for the top-spacer. Furthermore, thicker SiO_x can introduce strain in the film that may result in cracking.

3.3.3 FABRICATION OF GATE WITH GATE-ALL-AROUND GEOMETRY

One of the great strengths with vertical nanowire structures is the ability to fabricate gate-all-round, a geometry that provides the best electrostatic control. Furthermore, the smallest achievable gate-length is not limited by the resolution of the lithographic tools, instead the limit is set by the used thin film technology. In this work same process has been utilized for all transistors, the steps of this method are illustrated in Figure 3.7. Using the sputter, the sample was covered with a tungsten film, followed by spin-coating of S1800. Using reactive ion etching, the S1800 was etched to the desired thickness using O-plasma and the exposed tungsten was removed with an SF_6/Ar mix. The limitation of this method is set by the steps after the sputtering. As mentioned earlier in section 3.3.2, the yield deteriorates quickly if resist thickness reaches below 60-70 nm. This effectively limits the possibility to make gates with lengths below 50 nm. This limitation can be addressed by using another technology to apply the second film, such as evaporation. A simple test was performed by replacing the S1800 with evaporated Ni, which resulted in functioning MOSFETs with a physical gate length of 20 nm, see more details and electrical data in Appendix C. Another solution to this issue is usage of the gate-last process that was developed by the group [62] and is successfully used on the MOSFETs [63]. This method has so far not been tested on the TFETs although some of the challenges working with the nanowires that are covered with metal is discussed in section 3.3.4. Another technology for the gate is evaporation, which would results in a non-conformal coverage that dose not require extensive post-deposition processing. Unfortunately, this is not possible for the structures in this work, shadowing from the thicker GaSb stops the metal to reach the junction region.

3.3.4 TOP AND BOTTOM CONTACTS FORMATION

Parasitic resistance that inhibits the performance of transistors comes mainly from:

1. Increasing resistance due to the thinning of InAs segment.
2. Difficulty to make good ohmic-contact due to large band-gap and/or insufficient doping of the GaSb. [64, 65].

Attempts were made to address these issues. To reduce the resistance on the drain side a tungsten socket was introduced using a similar process as for the gate fabrication. The results can be viewed in Figures 3.8a and b. In the following steps, the nanowire diameter was reduced using digital etching. However with the socket added, this process exhibited poor reliability related to the etch-rate of InAs and selectivity towards the GaSb. This change in selectivity and reliability can be due to plasma process used to define the socket and also influence of metal assisted chemical etching (MACE) [66].

To reduce the contact resistance between the top contact and the GaSb segment, attempts were made to use evaporated Ni. The sample was spin-coated with organic resist followed by thinning with O-plasma of the resist until the top of GaSb was visible. Following these steps, a 5-nm-thick Ni layer was evaporated without any tilt and with rotation. The results can be viewed in Figures 3.8c and d. The digital etching was then performed showing less reliability and selectivity similarly to what was observed when the W-socket was made. Reproducibility of this process was shown to be difficult to achieve as the lift-off of the Ni-film failed numerous times. As all of these steps seem to influence the digital etching, attempts where made to apply evaporated Ni after digital etching. This process relied on the shadowing in similar way as for the previously described SiO_x spacer, unfortunately even a very thin Ni film can easily diffuse and stop further etching of the materials thereby hindering the mesa-etching which is needed to isolate the devices.

The solution in the end was to reduce the resistance at the drain side by usage of evaporated SiO_x, on the source side solution has been to simply protect the GaSb with high-κ during most of the process and to remove the high-κ just prior to the applying of top-metal. In the long run, to achieve full benefits from theses devices other processing techniques need to be used such as a gate-last process [62].

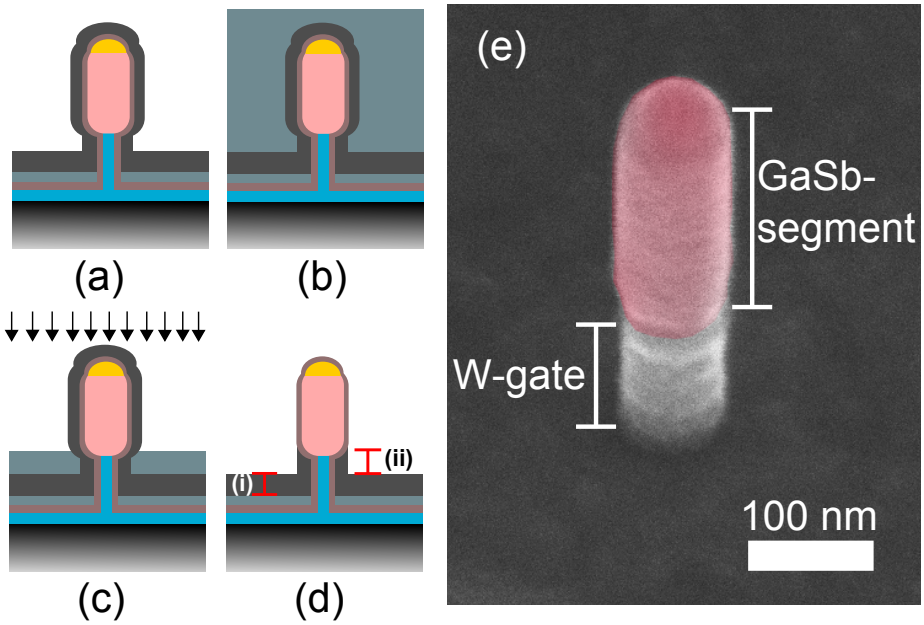


Figure 3.7: Fabrication of the gate (a) A tungsten film is sputtered on the sample (b) Organic resist is spin coated on the sample. (c) Resist is etched down using O-plasma to desirable thickness and exposed tungsten is removed using a mix of SF_6/Ar with RIE. (d) Resist is then removed from the sample. Total gate-length is determined by two process steps, which are: (i) Thickness of the sputtered film (ii) Final resist thickness prior to the etching of tungsten film. Step ii is the limiting step to reach gate-lengths shorter than 50 nm. (e) A SEM image, showing a InAs/GaSb nanowire after the gate fabrication.

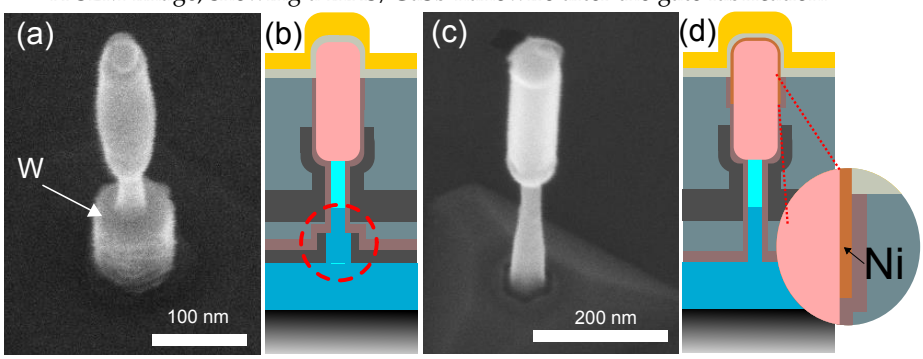


Figure 3.8: (a) A SEM image showing InAs/GaSb nanowire with W-socket manufactured to reduce the access-resistance on the drain. (b) Schematic illustration of a finished device with W-socket marked with dotted circle. (c) A SEM image showing InAs/GaSb with evaporated Ni on top of the GaSb segment to improve the contact resistance. (d) Illustration of a finished device with evaporated Ni on top of the nanowire.

4

Vertical InAs/GaSb and InAs/InGaAsSb/GaSb nanowire TFETs

In this chapter vertical InAs/GaSb and InAs/InGaAsSb nanowire TFETs will be discussed. This chapter is organized in five sub-chapters. Current status of field is given in first sub-chapter. Scaling of the InAs/GaSb TFETs is discussed in the second sub-chapter. The third sub-chapter describes usage of HSQ and SiO_x bottom spacers with InAs/GaSb TFETs. The motivation to switch from InAs/GaSb to InAs/InGaAsSb/GaSb is given in sub-chapter four. In the final sub-chapter, TFETs in this work are benchmarked against some selected TFETs and a Si-FinFET.

4.1 CURRENT STATUS OF TUNNEL FIELD-EFFECT TRANSISTOR

TFETs have been fabricated using a number of different material systems and device geometries. TFETs with a subthreshold swing well below the thermal limit have been manufactured by usage of Group IV semiconductors such as: Si, Ge, SiGe, and GeSn. With exception of GeSn, usage of these materials benefits directly from their dominance in the industry. These materials exhibit well optimized high-κ interfaces, well controlled doping, good contacts, less defects, and no scaling issues. However, despite of these benefits, Si- and Ge-based devices have limitations. These materials exhibit a large indirect band-gap, which results in low tunneling probability and thereby the on-currents are very low. The on-current has been increased by usage of strain engineering, which reduces the band-gap. Furthermore, usage of GeSn alloys allows for fabrication of TFETs with direct band-gap. By using strained Si, Knoll et. al. have demonstrated nTFET and pTFET with minimum subthreshold swing of 30 and 90 mV/decade at V_{DS} = 0.1 V, respectively [67]. Also in the same publication, a complementary inverter was manufactured.

Usage of III-V semiconductors allows for band engineering with direct band-gap, which allows for optimization of the junction to reach higher on-currents than what TFETs made of group IV are able to achieve. Using III-V semiconductors, TFETs with homojunction or heterojunction (staggered or broken band-gap alignment) have been demonstrated. However, due to a higher amount of defects in the bulk and at the interfaces, no device have demonstrated ability to operate well bellow the thermal limit. Both, Ahn et. al. and Alain et. al. have fabricated planar InGaAs TFETs with homojunction, which were able to reach a minimum subthreshold swing of 57 and 54 mV/decade at V_{DS} = 0.1 V, respectively [68, 69]. To achieve this performance, a source junction with a steep impurity profile and without defects was necessary. Reduction of defects is needed to remove the impact of DAT, which otherwise increase the subthreshold swing. The source junction in these devices was formed by usage of solid-phase Zn diffusion. Furthermore, devices fabricated by Alain et. al. also exhibited highly scaled EOT (0.8 nm) which further improved the electrostatic control and subtheshold swing.

To improve the current further, usage of staggered heterojunction is necessary. However, this action also adds one more interface that can contribute with defects. Yet, so far the TFETs with staggered heterojunction have demonstrated the best combination of currents and subthreshold swing. Dewey et. al. used a undoped $In_{0.7}Ga_{0.3}A$ pocket to form a staggered heterojunction in an InGaAs TFET, which resulted in three times higher current levels than comparable TFET with a homojunction [70]. Furthermore, using EOT scaling these devices were able to reach a minimum subhtreshold swing of 58 mV/decade at V_{DS}= 0.3 V. Similar results were achieved by Ahn. et. al., who could demonstrate improved currents when switching to staggered heterojunction, although the subhthreshold swing increased from 57 to 62 mV/decade. Zhao et. al. used a similar approach by adding undoped $InAs/In_{0.7}Ga_{0.3}As$ pocket to form a staggered heterojunction. The combination of vertical nanowires and gate-all-around geometry improved the electrostatics. These devices could achieve minimum subthreshold swing of 54 mV/decade at 0.3 V and operate at similar current levels as devices fabricated by Dewey et. al. [71].

Staggered heterojunction can also be formed by using $In_{0.53}Ga_{0.47}As/GaAs_{0.51}Sb_{0.49}$ as Fujimatsu et. al. have demonstrated [72]. By using 26-nm-thick vertical nanowires and with a EOT of 2.3 nm, a minimum subthreshold swing of 71 mV/decade was achieved. Pandey et. al. demonstrated staggered $In_{0.65}Ga_{0.35}As/GaAs_{0.45}Sb_{0.65}$ TFETs, which exhibited a high quality high-κ/channel interface and highly scaled EOT (0.8 nm). These devices could achieve on-current of 245 μA/μm at V_{DS} = 0.5 V and V_{GS} = 1.5 V. The minimum subthreshold swing from the DC-measurement was 102 mV/decade at V_{DS} = 0.05 V. However, the subthreshold swing could be improved to 55 mV/decade by using pulsed I-V measurements to

suppress the D_{it} in the mid-gap [73]. Also pTFETs were fabricated by using $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ to form the junction. These devices could reach a on-current of 14 $\mu A/\mu m$ at V_{DS} = -0.5 V and V_{GS} = -1.5 V. However, these devices exhibited a minimum subthreshold swing of 171 mV/decade at V_{DS} = 0.05 V. Discrepancy between the subthreshold swings can be explained by the different high-κ/channel interface in these devices. The interface in these nTFET and pTFET, are $In_{0.65}Ga_{0.35}As/ZrO_2$ and $GaAs_{0.35}Sb_{0.65}/HfO_2$, respectively.

The largest currents achieved by any TFET so far have been achieved by using near broken or broken band-gap heterojunction. Zhou et. al. demonstrated vertical TFETs with broken heterojunction implemented using InAs/GaSb. These devices reached 180 $\mu A/\mu m$ at $V_{GS} = V_{DS}$= 0.5 V, with a minimum subthreshold swing of 200 mV/decade [74]. D_{it} could be reduced by using forming gas annealing, which improved the minimum subthreshold swing to 150 mV/decade. Bijesh et. al. used $In_{0.9}Ga_{0.1}As/GaAs_{0.8}Sb_{0.2}$ to manufacture vertical TFETs with near broken band-gap. These devices exhibited large on-current, 740 $\mu A/\mu m$ at V_{DS} = 0.5 V and V_{GS} = 2.5 V, however the subthreshold swing was > 400 mV/decade [75]. By using template-assisted growth, lateral InAs/GaSb nanowire TFETs with gate-all-around were demonstrated by Cutaia et. al. [76]. nTFETs achieved an average subthreshold swing of 140 mV/decade and an on-current of 40 $\mu A/\mu m$ at $V_{DS} = V_{GS}$ = 0.5 V. The on-current and subthreshold swing of these devices were limited by the undoped source, which resulted in source depletion. However, Si/InAs pTFETs, integrated on the same wafer, achieved an average subhthreshold swing of 70 mV/decade and an on-current of 4 $\mu A/\mu m$ at $V_{DS} = V_{GS}$ = -0.5 V, which is one of the best pTFETs. Tomioka et. al. demonstrated vertical nanowire InAs/Si TFETs with minimum subthreshold swing of 21 mV/decade at V_{DS} = 1 V and on-current of 1 $\mu A/\mu m$ at $V_{DS} = V_{GS}$ = 1 V [77]. InAs nanowires, with a diameter of 30 nm, were in these devices grown on a Si-wafer utilizing template-assisted growth.

Materials that have gained more interest in recent years are two-dimensional materials (2DMs) such as transition metals dichalcogenides (TMD), Bi_2Se_2, Bi_2Te_2, and graphen. These materials would provide the possibility to manufacture an atom-thick channel, allowing the best possible electrostatics [78]. Sarkar et. al. demonstrated 2D TFET, which uses a molybdenium disulfide (MoS_2) bilayer as channel material [79]. The source was formed using Ge, which allows for controlled doping something that is so far difficult to achieve with 2DMs otherwise. The heterojunction between Ge and MoS2 is formed with van der Waals bond, which allows for a stress free interface. The gate-stack used in these devices was a solid polymer electrolyte, as there is so far no good technology to form a high-κ on 2DM. These devices achieved a minimum subthreshold swing of 3.9 mV/decade at V_{DS} = 1 V, at

a very low current.

As these presented publications shows there are a number of challenges to overcome when designing TFETs based on group IV or III-V semiconductors. An abrupt tunneling junction is required both for composition and doping. The interface between III-Vs and high-κ needs to exhibit a very low D_{it} to reduce DAT. Furthermore, an ultra-thin geometry is needed for robust electrostatic control. TFETs based on 2DMs show some desirable properties, however these novel materials also require more material research and development to improve the currents.

4.2 IMPROVING OF THE ELECTROSTATICS WITH REDUCED CHANNEL DIAMETER

Using vertical nanowire structures should provide us with best possible electrostatics, which would help to improve the subthreshold swing of the TEFTs. However, devices need to be scaled in a proper way, reducing the diameter only will increase the access resistance which will reduce the currents. Reduction of the diameter requires also reduction of the nanowire lengths and reduction of ungated areas i.e. spacer thickness [45]. For InAs/GaSb nanowire TFETs, an organic resist was used for fabrication of the bottom and top spacers, more information about this technology can be found in chapter 3.3.2. As shown in Figure 4.1a, the diameter of the nanowires was scaled down to 11 nm and the lengths were reduced from 1 μm to 500 nm. Reduction of the nanowire length required thinning of the bottom and top spacer, where the bottom spacers were reduced from 200 to 50 nm. Reduction of the top spacer is less extensive, thus top spacer needs be thick enough to stop the HF during removal of the high-κ on the top of the nanowire. The gate-length was reduced from 500 nm to 100 nm, with reduced overlap of the gate on the GaSb-segment.

Transfer data from devices with InAs diameter of 15 and 40 nm can be seen in Figure 4.1b, where the subthreshold swing was improved from 236 to 78 mV/decade at V_{DS}= 0.05 V [Paper VI], I_{OFF} is reduced, and DIBL is improved confirming improved electrostatic control. Furthermore, scaling of the device dimensions has kept I_{ON} in same range 6 to 9 μA/μm at V_{DS}=V_{GS} = 0.5 V. This trend is confirmed in Figure 4.1c and d where data from a number of devices from each sample are presented. The number of nanowires varies between 1-100 in these devices, where increasing number of used digital cycles reduces the yield of functioning devices and standing nanowires. Reduction of the diameter reduces I_{OFF} by an order of 3 and reduction of the nanowire length and spacer thickness increases the I_{ON} current. This scaling improves device characteristics down to a diameter of 15-20 nm.

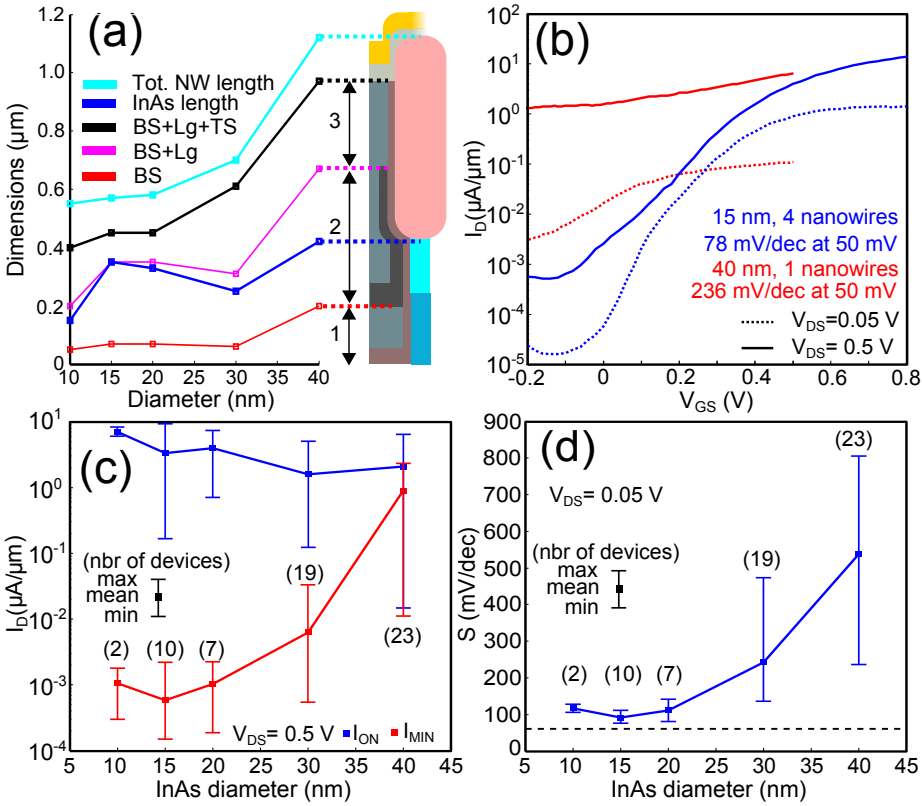


Figure 4.1: (a) Scaling of the vertical InAs/GaSb nanowire TFETs. Numbers at right in the image marks sections: 1) Bottom spacer 2) Gate-length 3) Top-spacer [BS=Bottom spacer, TS=Top spacer] (b) A comparison of transfer data from devices with InAs diameter of 15 and 40 nm, respectively. Reduction of diameter improves the electrostatics and subthreshold swing. (c) I_{ON} and I_{OFF} vs InAs diameter. Data from devices with thinner diameter exhibit lower variation, due to larger portion of the devices with 1-2 nanowires in the batch. (d) General trend of diameter scaling is a reduced subthreshold swing with reduced diameter. [All currents in this figure are normalized using $\pi \cdot d_{InAs} \cdot n_{NW}$, where d_{InAs} is diameter of InAs segment and n_{NW} is number of nanowires in the device.]

Further scaling of the diameter did not continue to improve the performance. The subthreshold swing increased from 78 to 123 mV/decade, as the diameter was scaled from 15 to 11 nm. This can, in part, be described by the transfer data form a device with 11 nm diameter in Figure 4.2a. The transfer data exhibits a large amount of noise, which impacts the subthreshold swing

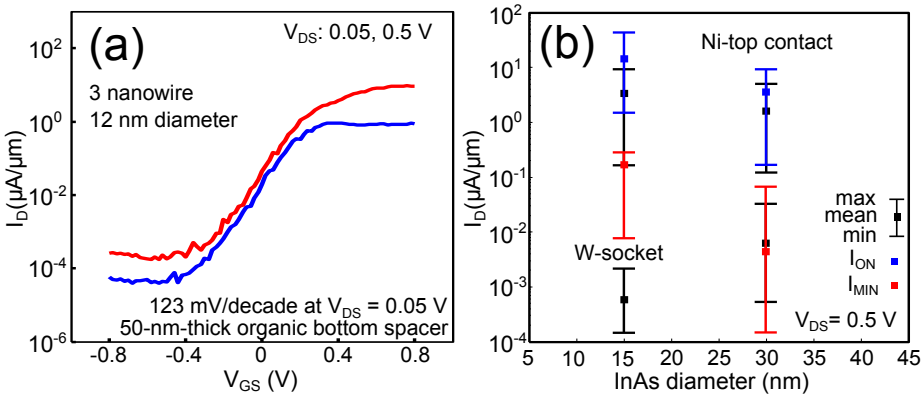


Figure 4.2: (a) Transfer data for a device with InAs diameter of 11 nm. (b) Transistors with improved contacts using with W-socket or Ni-alloying. Also data without improved contact with InAs diameter 15 nm and 30 nm is included as reference. [All currents in this figure are normalized using $\pi \cdot d_{InAs} \cdot n_{NW}$, where d_{InAs} is diameter of InAs segment and n_{NW} is number of nanowires in the device.]

[Paper I].

Scaling the diameter of the InAs segment will result in an increasing resistance on the drain side reducing the currents. Furthermore, making a good contact to GaSb on the source side is challenging due to a number of reasons such as too high Schottky barrier, difficulty to remove oxides, low doping etc. These two effects contribute to parasitic resistance that reduce the currents. The resistance on the source side was reduced using Ni-alloying and resistance on the drain side was reduced using W-socket. More detail about the process can be found in section 3.3.4. In Figure 4.2b, data from devices with improved contacts is compared against values presented in Figure 4.1c. Both approaches resulted in devices with a larger on-current, although the W-socket had larger impact on the on-current. However, devices with W-socket exhibited also a larger off-current. This can be expected as the metal of W-socket and gate-metal are only separated by a high-κ layer.

4.3 NON-ORGANIC BOTTOM SPACER

Using electron beam lithography and HSQ-spacer, the thickness can be adjusted for every individual device on the sample as shown in Figure 4.3a. Detailed information about the HSQ spacer technology can be found in Chapter 3.3.2. This method allowed us to study effects of bottom spacer thickness and gate-placement, on the device characteristics (Paper V). The length of the

nanowires, with an InAs diameter of 20 nm, was approximately 500 nm where InAs-segment is 300 nm and GaSb-segment is 200 nm. Nanowires with InAs diameter of 25 nm exhibited same total length, however with approximately 30 nm shorter InAs segment. Furthermore, the number of nanowires used in the transistors was varied between 1-220 and the thickness of the bottom spacer was varied from 0 to 170 nm. Data from devices with one nanowire and bottom spacer with thicknesses of 0 or 60 nm, is presented in Figure 4.3b. The device with the thinnest diameter exhibit the lowest subthreshold swing, 70 mV/decade at V_{DS} = 0.05 V, and the smallest DIBL. The spacer thickness have an impact on the on-current as larger ungated region increases the access resistance, thereby the device with the thinnest spacer and thickest nanowire diameter exhibit the largest on-current.

In Figure 4.3c, the dependence between the number of nanowires and the off- and on-current is presented. Neither the off-current nor the on-current exhibit any clear dependence on the number of the nanowires. However, as data in Figure 4.3d shows, the subthreshold swing increase with increasing number of the nanowires, from 68 to 96 mV/decade.

The impact of the bottom spacer thickness on I_{OFF} and I_{ON} is presented in 4.4a. Independently of the diameter, the off- and on-current is decreasing with increasing bottom spacer thickness. However, devices with a thicker diameter show a larger drop of the current as the thickness is changed from 140 to 170 nm. Shorter InAs segment, that thicker nanowires have, will result in a longer undoped InAs segment that is ungated. However, the thickness of the bottom spacer does not impact on the subthreshold swing, Figure 4.4b.

Devices using a 15-nm-thick SiO_x-layer as bottom spacer were manufactured, the method is described more in detail in Chapter 3.3.2. The total length of the nanowires used on this sample was 600 nm, where the InAs-segment and the GaSb-segment were 260 nm and 340 nm long, respectively. Transfer and output data is presented in Figure 4.4 for a device with 20-nm-thick InAs diameter and 40 nanowires in the array. Device achieves a subthreshold swing of 75 mV/decade at V_{DS} = 0.05 V, which is degraded to 97 mV/decade at V_{DS} = 0.5 V due to ambipolarity. However, the on-current of this device is larger than what previous devices could achieve with same diameter.

4.4 SWITHCING FROM BROKEN TO STAGGERED BAND-GAP ALIGNMENT

The concept with usage of band-gap in the source to filter out the highest energy carriers in the Fermi-Tail, forces charges to tunnel trough a barrier as they are moving between valence band in the source and conduction band in the channel. From this perspective usage of materials that provide

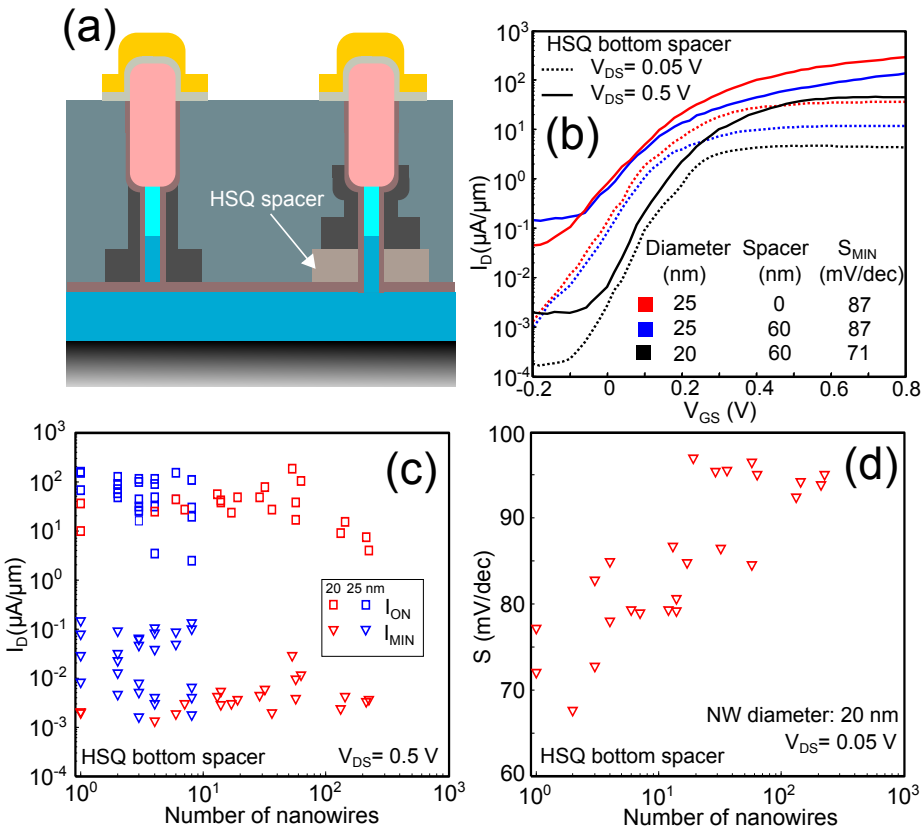


Figure 4.3: TFETs with HSQ bottom spacer (a) Illustration show how HSQ can change the position of the gate. (b) Transfer data for devices with different diameters and spacer thickness. (c) Number of nanowires vs on-current and off-current for devices with a diameter of 20 or 25 nm. (d) Subthreshold swing vs number of nanowires for devices with 20-nm-thick InAs channel. [All currents in this figure are normalized using $\pi \cdot d_{InAs} \cdot n_{NW}$, where d_{InAs} is diameter of InAs segment and n_{NW} is number of nanowires in the device.]

a broken band-gap alignment is really interesting, as this type of junction exhibit the thinest barrier. However, it is not trivial to fabricate devices with subthreshold swing below 60 mV/decade and so far no device with broken band-gap have demonstrated ability to operate below 60 mV/decade [80]. Another approach is to use devices with staggered heterojunction with near broken band-gap alignment. Scaling the diameter of the InAs below 8 nm in InAs/GaSb nanowires would create a heterojunction with near broken band-gap alignment as shown in Figure 4.5a. The technology used to fabricate the

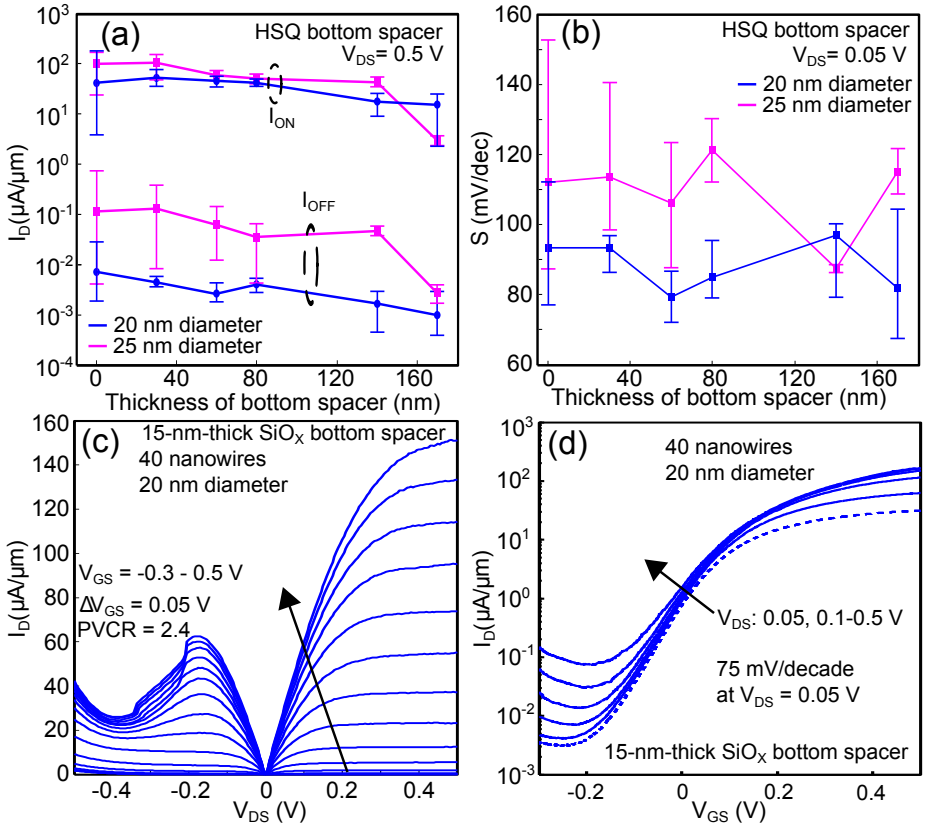


Figure 4.4: (a) HSQ thickness influence on off and on-current. (b) Subthreshold swing vs HSQ thickness. (c) Output data, where V_{GS} is swept from -0.3 to 0.5 V. (d) Transfer data for V_{DS} of 0.05 V, 0.1-0.5 V. [All currents in this figure are normalized using $\pi \cdot d_{InAs} \cdot n_{NW}$, where d_{InAs} is diameter of InAs segment and n_{NW} is number of nanowires in the device.]

transistors in this thesis can be used to fabricate devices with diameter of 11 nm, Figure 4.5b, although with poor yield (see chapter 3.3.1). Furthermore, the scaling of diameter increases the resistance, which will reduce the on-current if the thickness of the bottom spacer can not be scaled down enough. By using the SiO_x spacer instead of the organic spacer, the thickness of the bottom spacer can be reduced enough to improve the current in devices with 11-nm-thick channel (Appendix D). Data from devices with highly scaled diameter does also exhibit more noise in their characteristics, which impacts the subthreshold swing (Paper I). Another alternative to achieve staggered heterojunction with near broken band-gap is to use band-gap engineering by

usage of III-V materials. In the Papers I-IV, (In)GaAsSb segment was added which allows to control the properties of the heterojunction. However, it is not only important to find the right composition, control of the growth conditions is necessary to reduce the defects. The growth conditions of the InAs growth was changed according to the results from Wu et. al. [81]. Usage of these conditions resulted in lower amount of D_{it} close to the conduction band in InAs [81]. This change should improve the interface and reduce the amount of defects close to the conduction band of the InAs in the channel region, which according to the Franco et. al. is critical region for the TFETs [82].

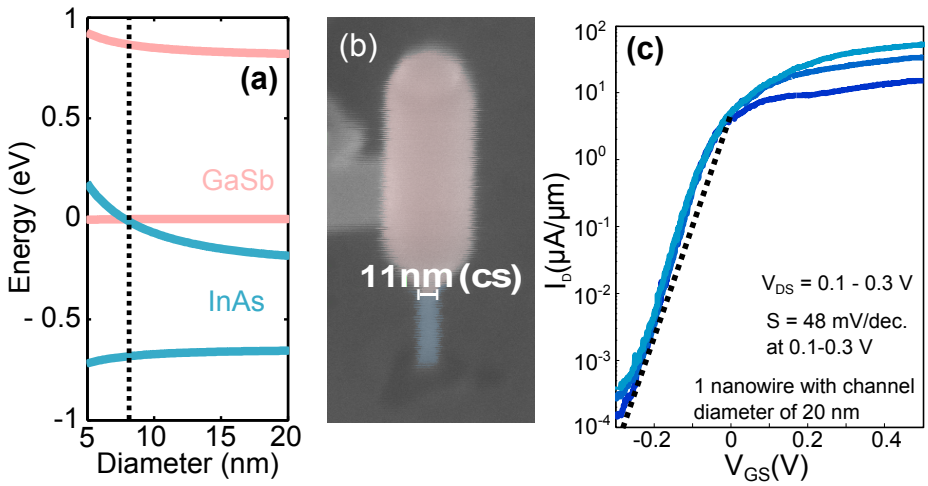
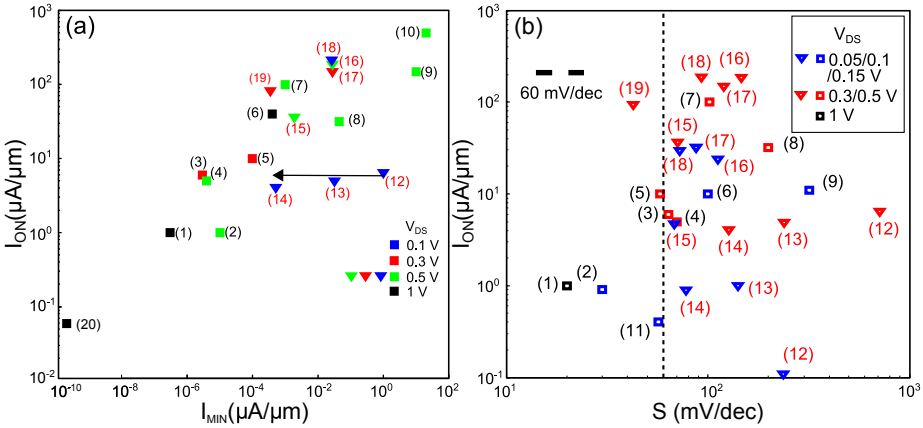


Figure 4.5: (a) As presented in Paper IV scaling of the InAs will increase the band-gap. Doted line marks when diameter is 8 nm. (b) Technology allows for scaling of the InAs diameter down to 11 nm, however the yield is only 1-2 %. (c) Transfer data for a vertical InAs/InGaAsSb/GaSb nanowire TFET from Paper I-IV. Doted line exhibit subthreshold swing of 60 mV/decade. [All currents in this figure are normalized using $\pi \cdot d_{InAs} \cdot n_{NW}$, where d_{InAs} is diameter of InAs segment and n_{NW} is number of nanowires in the device.]

4.5 BENCHMARKING OF DEVICES IN THIS WORK

The general trend in the data shows what would be expected, Si TFETs with homojunction exhibit the widest tunneling barrier and thereby also shows the lowest on-current and off-current. However, these devices operate well below the thermal limit reaching down to 20-30 mV/decade. In contrast, heterostructure TFETs with broken or near broken band-gap alignment exhibit the highest currents due to a thin barrier. In between the devices with the



(1) InAs/Si, Tomioka et. al., (VLSI 2012)
(2) Si/Ge, Knoll et. al., (EDL 2013)
(3) InGaAs, Noguchi et. al., (IEDM 2013)
(4) InAs/Si, Cutaia et. al., (VLSI 2016)
(5) InGaAs, Dewey et. al., (IEDM 2011)
(6) InAs/InGaAs, Ahn et. al., (VLSI 2016)
(7) InGaAs, Pandey et. al., (Trans. on Circ. 2016)
(8) InAs/GaSb, Zhou et. al., (IEDM 2012)
(9) GaSb/InAs(Sb), Dey et. al., (EDL 2013)
(10) InGaAs/GaAsSb, Bijesh et. al., (IEDM 2013)
(11) InGaAs, Ahn et. al., (VLSI 2016)
(12) InAs/GaSb, This work, 40 nm InAs diameter, organic spacer
(13) InAs/GaSb, This work, 30 nm InAs diameter, organic spacer
(14) InAs/GaSb, This work, 15 nm InAs diameter, organic spacer
(15) InAs/GaSb, This work, 20 nm InAs diameter, 60 nm HSQ bottom spacer
(16) InAs/GaSb, This work, 20 nm InAs diameter, 0 nm HSQ bottom spacer
(17) InAs/GaSb, This work, 25 nm InAs diameter, 0 nm HSQ bottom spacer
(18) InAs/GaSb, This work, 20 nm InAs diameter, 15 nm SiOx bottom spacer
(19) InAs/InGaAsSb/GaSb, This work, 20 nm InAs diameter, 15 nm SiOx bottom spacer
(20) 2D TFET, Sarkar et. al. (Nature 2015)

Figure 4.6: Benchmarking of selected TFETs. Squares marks data of devices published from other authors. (a) Ion vs Imin for a number of devices with homojunction, staggered and broken heterojunction. (b) I_{ON} vs point subthreshold swing for same devices as in (a). I_{ON} in both figures is defined as current at V_{ON} which is V_{ON}=V_{MIN}+V_{GS}, where V_{GS} = 1 V.

widest and thinnest tunneling barrier there are devices with a staggered heterojunction. Those devices exhibit higher currents as compared to devices with a homojunction and with a lower subthreshold slope than devices with broken heterojunction.

The data from InAs/GaSb and InAs/InGaAs/GaSb nanowire TFETs in this work is benchmarked against some of the published data presented in subchapter 4.1. In Figure 4.6a and b, on-current, off-current, and subthreshold swing for a number of devices is compared. Devices with only organic spacers (12)-(14) exhibit lower on-currents than other devices with broken band-gap. However, scaling of diameter improves both off-currents and subthreshold swing, moving the performance closer to what is published on TFETs with staggered heterojunction. Devices with HSQ bottom spacer (15) - (17) exhibit improved on-currents due to further reduction of bottom spacer and better subthreshold swing, reaching down to 70 mV/decade which is a clear improvement for devices with broken band-gap. Combining thin

diameter and bottom spacer in devices with 15-nm-thick SiO_x spacer (18), allowed us to manufacture devices that combine a subthreshold swing of 75 mV/decade at 0.05 V and high on-current. However, InAs/InGaAs/GaSb nanowire TFETs (19) exhibit the best combination of current and subthreshold swing.

To augment the MOSFET in the future, TFETs need to operate at higher current levels than those achieved this far with sub-threshold swing well below 60 mV/decade. To be useful, the sub-60 region would need to be in a current range from 15 pA/μm (Ultra Low Power) and reach at least 1 μA/μm [83]. When operating with MOSFETs in digital circuits, the rule of thumb has been to use 1/3 of the V_{DS} in the subthreshold region and rest above the subthreshold voltage. A TFET operated in a similar way with V_{DS} of 0.3 V would only have 0.1 V to switch between 15 pA/μm and 1 μA/μm i.e the average slope needs to be at least as low as 20 mV/decade.

Vertical InAs/(In)GaAsSb/GaSb nanowire TFET in this thesis have shown promising results. Data from two devices with different (In)GaAsSb compositions is presented in Figure 4.7. These devices exhibit a subthreshold swing of 45-48 mV/decade at V_{DS} = 0.1 V, which is lower than what previous III-V TFETs have a demonstrated. Furthermore, operation below 60 mV/decade occurs at higher currents than what previously published devices have demonstrated. The strength of this data is the combination of large currents and operation well below 60 mV/decade, which are required for circuit applications. Furthermore, modeling and material characterization, Paper I, shows that there is room for optimization of the heterojunction to reduce the off-currents and improve the subthreshold swing. Even more optimization can be performed by reducing the length of the nanowire and improve the contacts.

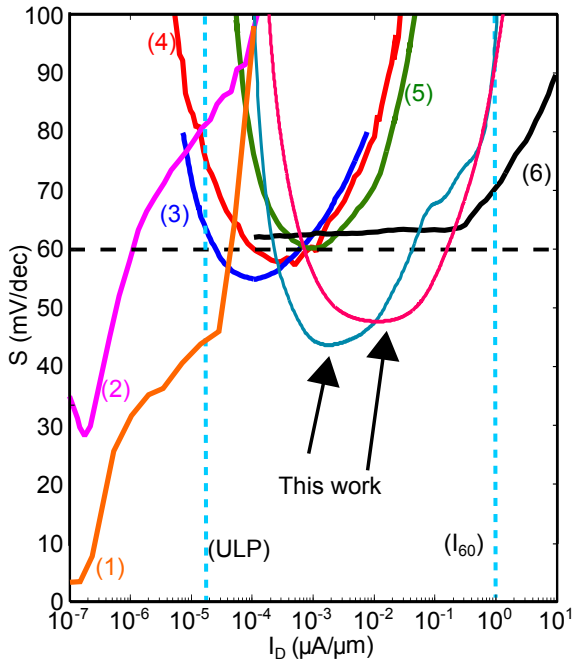


Figure 4.7: Benchmarking of the published TFET data compared to a state of the art Si FinFET with 16 nm gate-length. Vertical InAs/InGaAsSb/GaSb nanowire TFETs in this thesis, exhibit the highest I_{60} and reaches a minimum subthreshold swing well below 60 mV/decade [Paper III]. (1) 2D TFET (Sarkar et. al., [79]), (2) Si-TFET (Knoll et. al., [67]), (3) InGaAs Homojunction TFET (Alain et. al., [69]), (4) InGaAs Homojunction TFET (Ahn et. al., [68]), (5) InGaAs Staggered Heterojunction TFET (Dewey et. al., [70]), (6) 16 nm Si FinFET (TSMC 2013 [84])

5

Final words and Outlook

'Different' and 'new' is relatively easy. Doing something that's genuinely better is very hard.

Jonathan Ive

Since the autumn 2013, when the first samples with vertical TFETs were manufactured at Lund University, to where these TFETs stand today a large leap forward has been taken. Benefit from the groups extensive knowledge about the vertical processing and nanowire growth has made this development possible. The main accomplishment of this work was the demonstration of TFETs with a performance that exceeds the performance of traditional Si MOSFETs at low drive voltages. Even if this behavior was expected according to the theory, it has never been demonstrated experimentally until publication of Paper II.

Even so, there is plenty room for improvements of these devices. The heterojunction, which is the central part of the TFET, could be further optimized by changing the composition and doping. Improvement of the high-κ/channel interface by adding Ga to InAs or use improved high-κ recipe would improve electrostatics and further reduce the off-current due to lower D_{it}. Furthermore, a better approach to contact the top of the nanowire is required, this would help to increase the currents. Development of a gate-last process, similar to the process used for the vertical MOSFETs in the group, would be the best solution.

The general development of the III-V TFETs have taken some important steps during the time-span of this thesis. Three different groups have demonstrated devices with ability to operate below 60 mV/decade during the last two years. Two of the devices were TFETs with homojunction, which

due to a highly scaled EOT and defect-free source junction could achieve operation below the thermal limit. The third device, a TFET with staggered heterojunction, could achieve a subthershold swing below 60 mV/decade due to a well-scaled channel and usage of gate-all-around geometry together with a high quality high-κ/channel interface.

The knowledge to model TFETs general behavior have been available for a long time. Ever since the early studies of Esaki diodes, the tunneling process has been studied. However, the performance of all III-V based TFETs is limited by the defects in the bulk and interfaces. Thereby, more and more efforts are devoted to understand the roll and impact different defects have on the performance. Availability of more good experimental data will be useful to support this effort.

A question that has been around since the beginning: Can a TFET be used to replace or complement the MOSFET? This is a important question, however even today there is no clear answer. There is a number of possible outcomes, from simple yes and no to more complicated. With more knowledge maybe we will be able to make TFETs that are comparable or better than what MOSFETs are. However if the complexity to build these TFETs is too great, the question is then will there be any economical motivation to invest in such device? Another outcome is, as we understand these devices more and more we will be able to keep the complexity at reasonable level, which will allow for large scale fabrication and even be economically motivated. So part of the answer is to be addressed by the scientific community and the other part by industry.

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APPENDICES

A

Fabrication of the Vertical Tunnel Field-Effect Transistors

In this section the recipe used to manufacture device in Papers I-IV will be presented. Furthermore, information about manufacturing of the HSQ spacer will be given in the end of this chapter. The HSQ spacer was used in Papers V and VII.

SUBSTRATE Samples in this work are made using lightly p-doped 4-inch silicon-wafers (111) as starting material. Using metalorganic vapour phase epitaxy (MOVPE) a low-resistive 250-nm-thick InAs layer is grown. The InAs-layer functions as a buffer-layer for nanowire growth and furthermore is used as low resistive interconnecting layer. At the interface between p-doped Si and n-doped InAs a pn-junction is formed, thereby closing a possible leakage path through the substrate. During the fabrication process InAs-layer will be removed between the devices to isolate them. This procedure is necessary to reduce the risk for short circuiting in case the probe tip would penetrate the organic spacer beneath the probing-pads. Buffer layers on samples used in this work are grown by Johannes Svensson.

PREPARATIONS BEFORE THE GROWTH Placement of the nanowires is determined using gold (Au) discs which are positioned and deposited using poly(methyl methacrylate) (PMMA) based lift-off process and electron beam lithography (EBL). Processing described in the following text is performed by using 2×2 cm^2 pieces.

1 Clean the sample

- Use heated acetone (50 ^{o}C, 3 min)

- Rinse in IPA

2 Dehydrate the surface to achieve better adhesion

- Heat the sample on a hotplate (180 ^{o}C, 5 min)
- To reduce the risk of burning the resist, cool the sample before next step by placing it on a cold metal surface.

3 Apply PMMA 200A5:Anisole (1:1) and hardbake the resist

- Spin on the resist (1500 rpm/s, 6000 rpm, 30 s)
- Bake in oven (180 ^{o}C, 45 min)

4 Apply PMMA 950A4 and hardbake the resist

- Spin on the resist (1500 rpm/s, 6000 rpm, 30 s)
- Bake in oven (180 ^{o}C, 45 min)

5 Pattern and develop the resist

- Use electron beam lithography to pattern the resist. Parameters given are for system Raith 150, focusing is achieved by burning contamination spots followed by 3-point adjustment with automatic focus correction enabled.
  (Aperture 7.5 μm, Acceleration: 20 kV, Step size 2 nm, Beam current: 15 pA, Dose for dots in double arrays with 200 nm pitch (6 fC), Dose for single dots (60 fC)).
- Develop the resist using MIBK/IPA 1:3 (90 s)
- Rinse in IPA (30 s)
- Inspect patterns with optic microscope using dark mode

6 Evaporation of metal layer and lift-off

- Clean the sample using O_2-plasma ashing in Plasma Preen, with metal cage deployed (15 s, 5 mbar)
- Remove the native InAs-oxide in patterned holes by wet etching with HCl:H_2O (1:1) or BOE (1:10) (60 s or 30 s)
- Rinse in H_2O (60 s)
- Evaporate the gold film using Pfeiffer Classic 500 system (15 nm, 0.1 nm/s, $>5 \times 10^{-7}$ mbar)
- Place the sample in beaker with heated acetone (50 ^{o}C) and wait until the surface has shifted color. Agitate the solvent with tweezers to remove the film.

- Move the sample to a new beaker with heated acetone (50 ^{o}C, 1 min). Be sure to keep the surface wet during the movement between the beakers, there can still be some metal residues on the sample.
- Move the sample to a new beaker with heated acetone (50 ^{o}C, 5 min). This step is to remove possible resist residues.
- Rinse in IPA (60 s)
- Rinse in IPA (5 min)

7 Cleave the sample

- Spin on S1818 (1: 5 s, 100 rpm/s, 500 rpm 2: 60 s, 1000 rpm/s, 4000 rpm/s)
- Hardbake the resist (120 ^{o}C, 15 min)
- Dice the sample in smaller pieces 1×1 cm^2 using manual scriber.
- Clean the sample in acetone (50 ^{o}C, 15 min)
- Move the sample in new beaker with acetone, and place that beaker in ultrasonic power bath
- Move sample in new beaker (5 min)
- Rinse in IPA

8 Clean the sample before the growth

- Clean the sample using O_2-plasma ashing in Plasma Preen, with metal cage deployed (15 s, 5 mbar)
- Remove the native InAs-oxide in patterned holes by wet etching with HCl:H_2O (1:1) or BOE (1:10) (60 s or 30 s)
- Rinse in H_2O (60 s)

Samples used in Papers V-VII where prepared using steps described above. However, for the samples used in other papers, steps 1-7 were performed at Chalmers University. The dicing of these was performed using automatic scriber, which scribes the whole 4-inch wafer in pieces with dimensions of 1×1 cm^2. The same process is used to clean these samples after the dicing and before the growth.

GROWTH OF THE NANOWIRES By using Au-particles as seed particles, the nanowires were grown using vapour-liquid-solid growth method. All growth was performed using metal organic vapor epitaxy (MOVPE) with following precursors: trimethylindium (TMIn), arsine (AsH3), trimethylgallium (TMGa), and trimethylantimony (TMSb). Doping was added to the source and drain regions using precursors: triethyltin (TESn) and diethylzinc (DEZn).

DEVICE FABRICATION

1 Reduction of the channel region through digital etching

- Oxidize using ozone at elevated temperature (50 ^{o}C, 5 min)
- Etch with citric acid (30 s)
- Rinse in H_2O (60 s)
- Rinse in IPA (60 s)

2 Gate dielectric deposition using atomic layer deposition (Savannah-100)

- Apply Al_2O_3 using trimethylaluminium (TMA) and H_2O precursors (1 nm, 300 ^{o}C)
- Apply HfO_2 using tetrakis(dimethylamino)hafnium (TDMAHf) and H_2O precursors (4 nm, 120 ^{o}C)

3 Deposition of bottom spacer using AVAC

- Evaporate SiO_x without any tilt and rotation turned on (15 nm, 0.1-0.2 nm/s)
- Remove the SiO_x flakes from sidewalls of the nanowire using diluted 1:400 HF:H_2O (2min)
- Rinse in H_2O (60 s)
- Compensate for reduced high-κ thinning, by applying extra HfO_2 using tetrakis(dimethylamino)hafnium (TDMAHf) and H_2O precursors (2 nm, 120 ^{o}C)

4 Gate metal deposition

- Sputter on a 60-nm-thick tungsten (W) using AJA Orion 5 with rotation (DC power 100 W, 9 sccm Ar-flow, 0.09 nm/s))

5 Gate-length definition

- Spin on S1813 resist (1: 5 s, 100 rpm/s, 500 rpm 2: 60 s, 1000 rpm/s, 4000 rpm)
- Hardbake the resist on a hotplate (120 ^{o}C, 15 min)

- Thin down resist in RIE with O-plasma, used time differs from sample to sample depending on nanowire length. (800-1000 s, 15 sccm, 50 W, 300 mTorr)
- Remove the tungsten that is exposed in RIE with SF_6/Ar mix. (45 s, 45/10 sccm, 140 W, 185 mTorr)
- Clean the sample using O_2-plasma ashing in Plasma Preen. (15 s, 5 mbar) This step is to remove the Teflon layer that is fomred during the etching with SF_6.
- Clean the sample in acetone to remove the resist (60 s)
- Rinse in IPA

6 Gate-pad definition

- Spin on S1813 resist (1: 5 s, 100 rpm/s, 500 rpm 2: 60 s, 1000 rpm/s, 4000 rpm)
- Softbake the resist on a hotplate (115 ^{o}C, 90 s)
- Pattern the resist using UV-lithography (365 nm wavelength) (6 s, 20 mW/cm^2)
- Develop the resist in MF319 with continuous stirring. (70 s)
- Rinse in H_2O with continuous stirring.
- Hardbake the resist on a hotplate. (120 ^{o}C, 15 min)
- Remove the tungsten that is exposed in RIE with SF_6/Ar mix. (45 s, 45/10 sccm, 140 W, 185 mTorr)
- Clean the sample using O_2-plasma ashing in Plasma Preen. (15 s, 5 mbar)
- Clean the sample in acetone to remove the resist (60 s)
- Rinse in IPA

7 Isolate the devices by etching out a mesa from the buffer layer.

- Spin on S1813 resist (1: 5 s, 100 rpm/s, 500 rpm 2: 60 s, 1000 rpm/s, 4000 rpm)
- Softbake the resist on a hotplate (115 ^{o}C, 90 s)
- Pattern the resist using UV-lithography (365 nm wavelength) (6 s, 20 mW/cm^2)
- Develop the resist in MF319 with continuous stirring. (70 s)
- Rinse in H_2O with continuous stirring.

- Hardbake the resist on a hotplate. (120 ^{o}C, 15 min)
- Remove the high-κ/SiO_x/high-κ layer 1:400 HF:H_2O (20 min)
- Etch InAs mesa with 1:1:25 H_3PO_4:H_2O_2:H_2O (120 s)
- Rinse in H_2O with continuous stirring.
- Clean the sample in acetone to remove the resist (60 s)
- Rinse in IPA

8 Top-spacer is fabricated to separate gate-pad from top-metal which is source of the device. Organic resist is spin-coated on the sample and thinned down to wanted thickness.

- Spin on S1813 resist. (1: 5 s, 100 rpm/s, 500 rpm 2: 60 s, 1000 rpm/s, 4000 rpm)
- Permanent bake the resist in oven. (200 ^{o}C, 40 min)
- Thin down resist in RIE with O-plasma, used time differs from sample to sample depending on nanowire length. (500-600 s, 15 sccm, 50 W, 300 mTorr)

9 Formation of via-holes through the top-spacer

- Spin on S1813 resist (1: 5 s, 100 rpm/s, 500 rpm 2: 60 s, 1000 rpm/s, 4000 rpm)
- Softbake the resist on a hotplate (115 ^{o}C, 90 s)
- Pattern of gate-via is transfered to the resist using UV-lithography (365 nm wavelength) (6 s, 20 mW/cm^2)
- Develop the resist in MF319 with continuous stirring. (70 s)
- Rinse in H_2O with continuous stirring.
- Hardbake the resist on a hotplate. (120 ^{o}C, 15 min)
- Thin down resist in RIE with O-plasma, used time differs from sample to sample depending on nanowire length. (1000 s, 15 sccm, 50 W, 300 mTorr)
- Clean the sample in acetone to remove the resist (60 s)
- Rinse in IPA
- Spin on S1813 resist (1: 5 s, 100 rpm/s, 500 rpm 2: 60 s, 1000 rpm/s, 4000 rpm)
- Softbake the resist on a hotplate (115 ^{o}C, 90 s)
- Pattern of drain-via is transfered to the resist using UV-lithography (365 nm wavelength) (6 s, 20 mW/cm^2)

- Develop the resist in MF319 with continuous stirring. (70 s)
- Rinse in H_2O with continuous stirring.
- Hardbake the resist on a hotplate. (120 ^oC, 15 min)
- Thin down resist in RIE with O-plasma, used time differs from sample to sample depending on nanowire length.
  (1000 s, 15 sccm, 50 W, 300 mTorr)

10 Fabrication of the top-contact

- Remove the high-κ at top of the nanowires using 1:400 HF:H_2O (7 min)
- Sputter on a 10-nm-thick Ni layer using AJA Orion 5 with rotation (DC power 100 W, 9 sccm Ar-flow, 0.06 nm/s))
- Sputter on a 150-nm-thick Au layer using AJA Orion 5 with rotation (DC Power 100 W, 9 sccm Ar-flow, 0.34 nm/s))
- Spin on S1813 resist (1: 5 s, 100 rpm/s, 500 rpm 2: 60 s, 1000 rpm/s, 4000 rpm)
- Softbake the resist on a hotplate (115 ^oC, 90 s)
- Pattern the resist using UV-lithography (365 nm wavelength) (6 s, 20 mW/cm^2)
- Develop the resist in MF319 with continuous stirring. (70 s)
- Rinse in H_2O with continuous stirring.
- Hardbake the resist on a hotplate. (120 ^oC, 15 min)
- Etch Au using 1:2:17 KI:I_2:H_2O (40 s) with continuous stirring.
- Rinse in H_2O
- Etch Ni using 1:2.5:2.5:5 CH_3COOH:HNO_3:H_2SO_4:H_2O (40 s)
- Rinse in H_2O
- Clean in acetone to remove the resist
- Rinse in IPA

HYDROGEN SILSESQUIOXANE SPACER Deployment of organic spacer and SiO_x is presented in the main recipe, however also hydrogen silsesquioxane (HSQ) was used as spacer in some of the papers (V and VII). Processing of the HSQ was integrated in the main recipe, where special care was required when the HF was used. HSQ is easily etched by HF, so steps that involves usage of HF are performed before HSQ step or when HSQ is well protected with other layers. Following steps describes formation of bottom spacer:

- Spin on HSQ (60 s, 1500 rpm/s, 3000 rpm)
- Soft-bake on a hotplate to remove the solvent (200 ^{o}C, 2min)
- Electron beam lithography is used to pattern the resist. Parameters given are for system Raith 150, compared to PMMA focusing can not be performed by burning a contamination spot instead prepared markers where used.
  (Aperture 10 μm, Acceleration: 20 kV, Step size 10 nm, Beam current: 20 pA, Area dose: 40 μC/cm^2)
- Using 25wt% tetramethylammonium hydroixde (TMAH) to develop the resist (60 s)
- Rinse in H_2O (60 s)
- HSQ is cured using rapid thermal processing (300 ^{o}C, 20 min, N2/H2 ambient)

B

Self-alignment of Hydrogen Silsesquioxane

During the development of the process for fabrication of the HSQ spacers a number of observations were made. Two of the observations are disused in the text below. Both of the observations relies on the correlation between the sensitivity and initial thickness of the HSQ. Where the initial thickness is the thickness of HSQ prior to the exposure with electron beam and development of the HSQ. As presented in Paper VII, thicker HSQ exhibit a higher sensitivity and therefore requires a lower effective electron dose to achieve similar thickness than what a thinner HSQ would require. This allows for self-alignment of the HSQ in following situations: (1) if the nanowires are longer than the initial thickness of the HSQ, will result in a thicker HSQ in the closest proximity of the nanowires as shown in Figure B.1a. After exposure and development self-aligned finger will form around the nanowire arrays as Figure B.1b shows. (2) Using HSQs great gap-filling ability, a unevenness in the underlying layer will be filled by the HSQ and the surface will be flat. The HSQ over the unevenness is thicker for the electrons and thereby the HSQ in this region exhibit a larger sensitivity. As Figure B.1c shows this adjustment could properly level the surface over a unevenness.

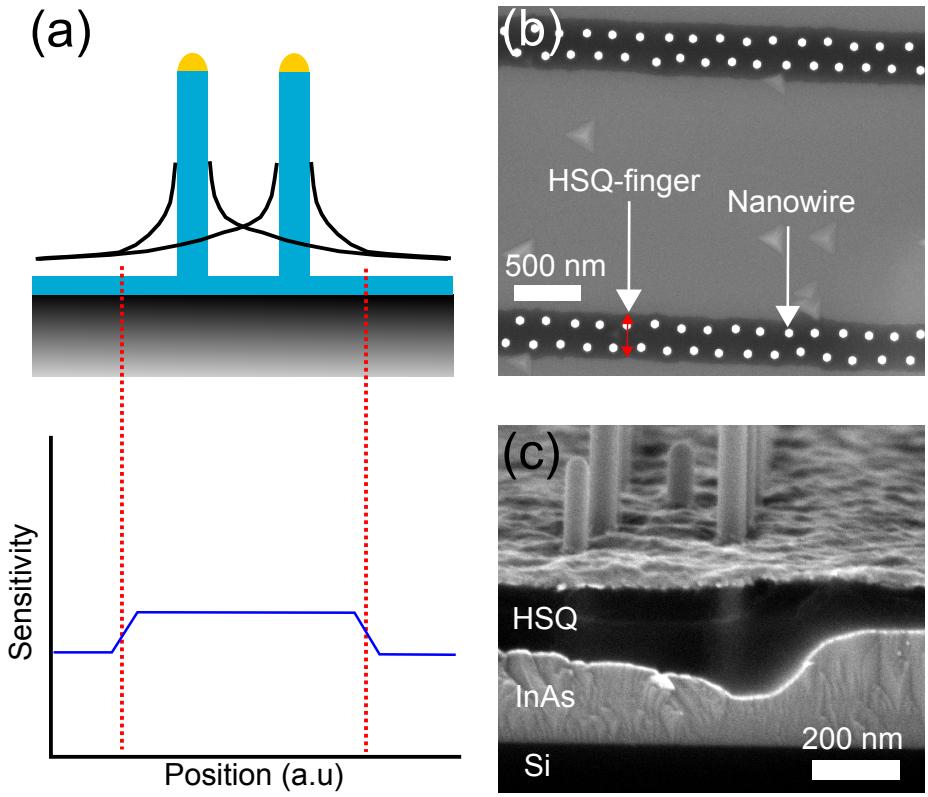

Figure B.1: Self-alignment of the HSQ observed when working with the samples in this thesis. (a) Schematic illustration that shows how HSQ, which is thinner than the length of the nanowires, covers the structure. In the close proximity of the nanowires the HSQ will form a upslope. This effect will be enhanced if the pitch between the nanowires is reduced. During the exposure of the HSQ layer, there will be a difference in sensitivity. This change in sensitivity over the sample is illustrated by the graph showing position vs sensitivity. Thicker HSQ exhibit higher sensitivity. (b) A SEM image that shows self-aligned HSQ fingers around the nanowires arrays. How wide the fingers are depends on a number of factors such as: used electron dose, HSQ thickness, baking temperature, etc. (c) Similar effect, observed in (a), is achieved when the HSQ fills an unevenness on the sample.

C

Fabrication of Vertical Transistors with 20 nm gate length

Fabrication of the gate is described in chapter 3.3.3. In this process the gate-length is defined by spin-coating the sample with a organic resist which is thinned down to the desired thickness in subsequent step. Metal is removed from exposed regions and the sample is cleaned from the resist. All etching in this process is performed using reactive ion etching. Reliability of this method depends on how even the resist can be spin-coated on the sample and how uniformly this resist can be etched down. These two parameters can be controlled well enough to fabricate transistors with a gate length of 50-100 nm. However, achieving shorter gate-lengths with a good yield is difficult. To reach shorter gate-lengths with great yield would require another approach. In this section functioning devices with gate-lengths of 20 nm are demonstrated. Evaporated Ni is used instead of organic resist to define the gate-length. Nanowires used for these devices are undoped InAs nanowires with a diameter of 28 nm in the gate-region. Fabrication process for these device is similar as the process described in paper VII expect for the definition of the gate which is described in following text.

A 15-nm-thick tungsten film was sputtered on using the same parameters as described in Appendix A. Sample was spin coated with S1813 and the resist was soft-baked at 115^{o}C for 90 s on a hot-plate. Using a lift-off mask and soft-UV lithography, a pattern of the gate-pad was exposed. Using MF319 the resist was developed and the resist was hard-baked on hot-plate at 120^{o}C for 15 min. A 5-nm-thick Ni film was applied using thermal evaporation, without any tilt and with rotation. Evaporated Ni film was removed from the areas outside the pads using lift-off and W-film was etched away with SF_6/Ar in reactive ion etching. Sample was cleaned using O_2 ashing, followed by acetone and IPA. Figures C.1a-c illustrates the steps used to fabricate the gate.

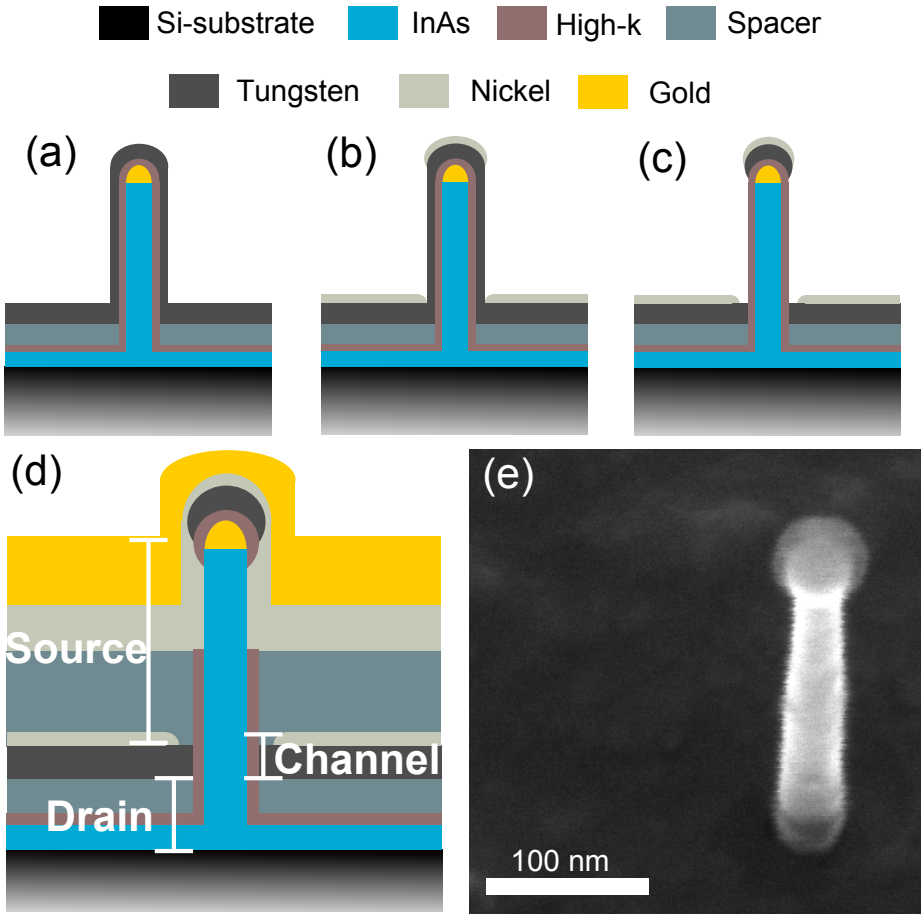

Figure C.1: Fabrication of the gate (a) Sputtering on a 15-nm-thick Tungsten film. (b) Evaporate 5-nm-thick Nickel film without any tilt. (c) Etch away tungsten from the sidewalls of the nanowires using SF_6/Ar in reactive ion etching. (d) Finished device with the drain, channel. and source region marked. (e) A SEM images showing a device with one nanowire after finished gate. Some tungsten and nickel are left on top of the nanowire.

Schematic image of fished device with the drain, channel, and source regions marked out in Figure C.1d. A SEM image of a device after the gate is finished can be viewed in Figure C.1e.

Transfer and output data from one of the devices can be viewed in Figure C.2. The transfer data confirms gate-modulation, where the current can be changed with 3 orders of magnitude. However, as the output data shows, this device is haunted by a large access resistance. Large ungated regions of

undoped nanowire contribute to the large access resistance. However, none of the shortcomings are directly related to used gate-technology. Formation of some alloy was observed on the edges of the gate-pad. Also, on some of the pads the metal was etched, so further optimization of this process if required.

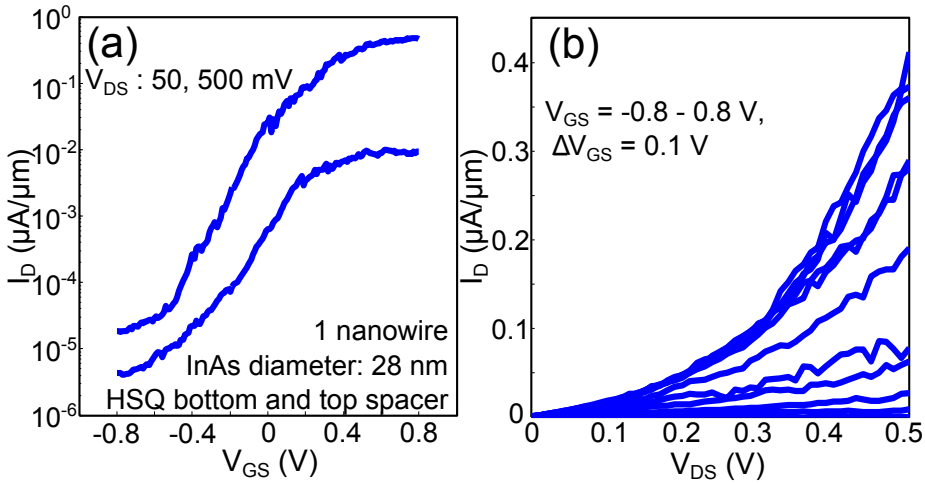

Figure C.2: (a) Transfer data from a device with one nanowire. Diameter of the nanowire is 28 nm and the nanowire is undoped. The data shows that the current in the channel can be modulated which confirms functioning gate. (b) Output data from the device in (a). The current is reduced due to a large access resistance. [All currents in this figure are normalized using $\pi \cdot d_{InAs} \cdot n_{NW}$, where d_{InAs} is diameter of InAs segment and n_{NW} is number of nanowires in the device.]

D

Vertical InAs/GaSb nanowire TFETs with channel diameter of 11-12 nm

TFETs with channel diameter of 10-12 nm were manufactured in this thesis. The first devices were fabricated using organic spacers, which limits the thickness of the bottom spacers to 50 nm (chapter 3.3.2). For the next sample the SiO_x was used to fabricate a 15-nm-thick bottom spacer resulting in improved on-current Figure D.1a. However, devices on both samples exhibit a larger subthreshold swing (123 mV/decade) than devices with 15-20 nm diameter (78 mV/decade) presented in Section 4.1. The transfer data of these highly scaled devices exhibit more random telegraph noise compared to similar devices with thicker diameter. This increased noise have impact on the subthreshold swing of these device, see Paper I. Devices with SiO_x spacer, Figure D.1 c/e, achieved on-current which is 10 times higher.

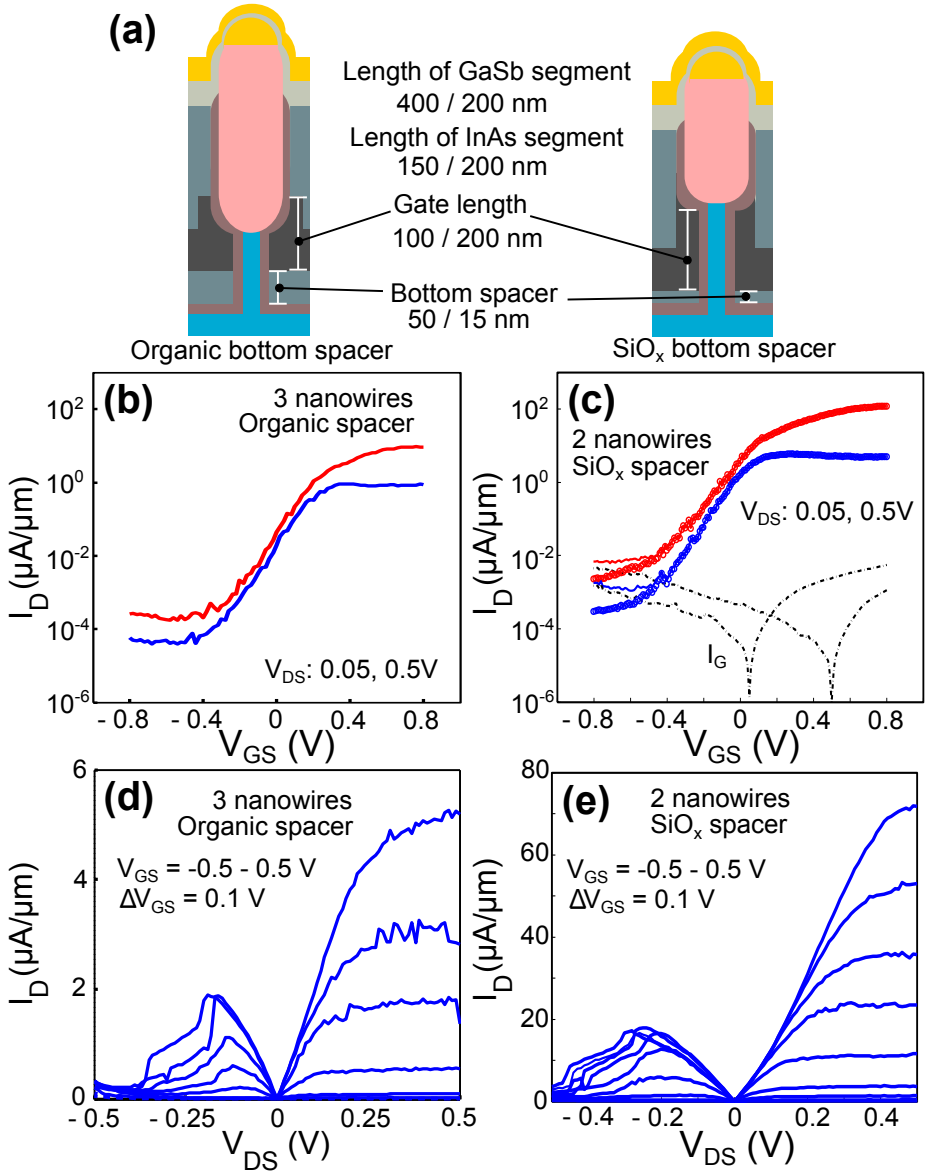

Figure D.1: TFETs with thin channel (a) Schematic illustration of InAs/GaSb nanowire TFETs with channel diameters of 11-12 nm. Bottom spacer was manufactured using organic photo resist (left) or SiO_x spacer (right). (b) Transfer data from one of the devices with organic bottom spacer. The gate-current was two orders of magnitude lower than the current in the channel. (c) Transfer data from one of the devices with SiO_x spacer. (d) Output data from one of the devices with organic bottom spacer. (e) Output data from one of the devices with SiO_x spacer. [All currents in this figure are normalized using $\pi \cdot d_{InAs} \cdot n_{NW}$, where d_{InAs} is diameter of InAs segment and n_{NW} is number of nanowires in the device.]