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Extrinsic and Intrinsic Performance of Vertical InAs Nanowire MOSFETs on Si Substrates

Karl-Magnus Persson, Martin Berg, B. Mattias Borg, Jun Wu, Sofia Johansson, Johannes Svensson, Kristofer Jansson, Erik Lind, and Lars-Erik Wernersson

Abstract— **This paper presents DC and RF characterization as well as modeling of vertical InAs nanowire MOSFETs with L_G = 200 nm and Al_2O_3/HfO_2 high-κ dielectric. Measurements at V_{DS} = 0.5 V show that high transconductance (g_m = 1.37 mS/μm), high drive current (I_{DS} = 1.34 mA/μm), and low on-resistance (R_{ON} = 287 Ωμm) can be realized using vertical InAs nanowires on Si substrates. By measuring the 1/*f*-noise, the gate area normalized gate voltage noise spectral density, $S_{VG} \cdot L_G \cdot W_G$, is determined to be lowered one order of magnitude compared to similar devices with a high-κ film consisting of HfO_2 only. Additionally, with a virtual source model we are able to determine the intrinsic transport properties. These devices (L_G = 200 nm) show a high injection velocity (v_{inj} = $1.7 \cdot 10^7$ cm/s) with a performance degradation for array FETs predominantly due to an increase in series resistance.**

Index Terms— **MOSFET, RF, InAs, Nanowire (NW).**

I. INTRODUCTION

Striving towards ultra-scaled devices, the transistor architecture and the material properties need consideration. The nanowire geometry offers advantageous electrostatic scaling [1] and the use of a high-κ gate dielectric allows reduced EOT without large gate leakage currents. InAs has a high injection velocity, v_{inj}, and allows simple fabrication of low resistance contacts [2][3]. High current densities have been demonstrated for thin InAs transistor channels [4].

In this paper we demonstrate DC characterization, modeling and RF characterization of FETs consisting of arrays of vertical NWs (a-FETs) [5][6][7]. Our data for a-FETs show a threefold improvement on earlier data and we achieve transconductance values above 1 mS/μm for individual nanowires. This is attributed to an improved bi-layer gate dielectric using Al_2O_3/HfO_2, as well as more reliable processing with a thin Si_3N_4 film, reducing the source series resistance [8]. From DC modeling, we identify the main limiting factors in the transistor layout.

II. DEVICE FABRICATION

Devices are fabricated on Si substrates cut from a 4" Si wafer covered by a 300-nm-thick InAs contact layer (ICL).
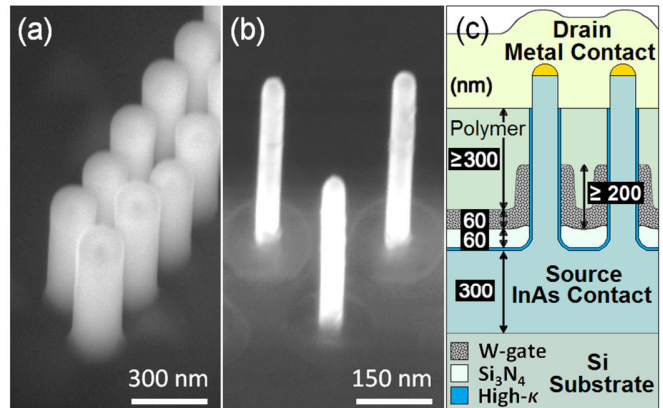
Fig. 1. (a) SEM images at 30° tilt angle of NW array after PECVD of Si_3N_4, and, (b) after side removal etch. (c) Schematic cross-section of the NW FET device. A 60-nm-thick Si_3N_4 film separates the InAs source contact layer from the gate metal while a spin-on resist (≥ 300-nm) separates the gate and drain metals.

The Si is highly resistive and the InAs layer is grown without intentional doping (n = $3 \cdot 10^{18}$ cm^{-3}) demonstrating a sheet resistance of 36 Ω/□. Definition of size and position of gold seed particles is made with electron-beam-lithography and growth of InAs nanowires is performed in an metal-organic-vapor-phase-epitaxy (MOVPE) growth chamber at 420 °C and with a Sn dopant flow corresponding to a doping level of ~$1 \cdot 10^{18}$ cm^{-3} [9]. For a-FETs, NWs are placed in zigzag rows to reduce the parasitic capacitance within the array [10], with 300 nm spacing between each NW (see Fig. 1a and Fig. 1b). Devices are fabricated with 1, 52, 96, and 192 NWs and with two NW diameters; D_{NW} = 45 nm and D_{NW} =28 nm [8]. Besides the difference in size of catalytic gold particles, the rest of the growth conditions are identical. The dielectric is deposited in a Cambridge Savannah ALD process with 10 cycles of Al_2O_3 at 250 °C and 60 cycles of HfO_2 at 100 °C, with a total thickness of 7 nm translating to an estimated EOT of 1.8 nm. The D_{NW} = 28 nm have a thinner HfO_2 layer, yielding an estimated EOT = 1.3 nm. Subsequent to the ALD, the 2×2 cm^2 pieces are cleaved into 4 samples and each sample is thereafter processed individually. Devices are isolated by etching out source-mesas from the ICL in a wet-etch procedure. A 60-nm-thick source-to-gate spacer layer is fabricated in a process where a plasma-enhanced-chemical-vapor-deposited (PECVD) Si_3N_4-film (Fig. 1a) is conformaly formed on the NWs. The film is then selectively removed on the sides of the wires, while keeping the lateral film intact by protecting it with a polymer etch mask in a SF_6 dry-etch
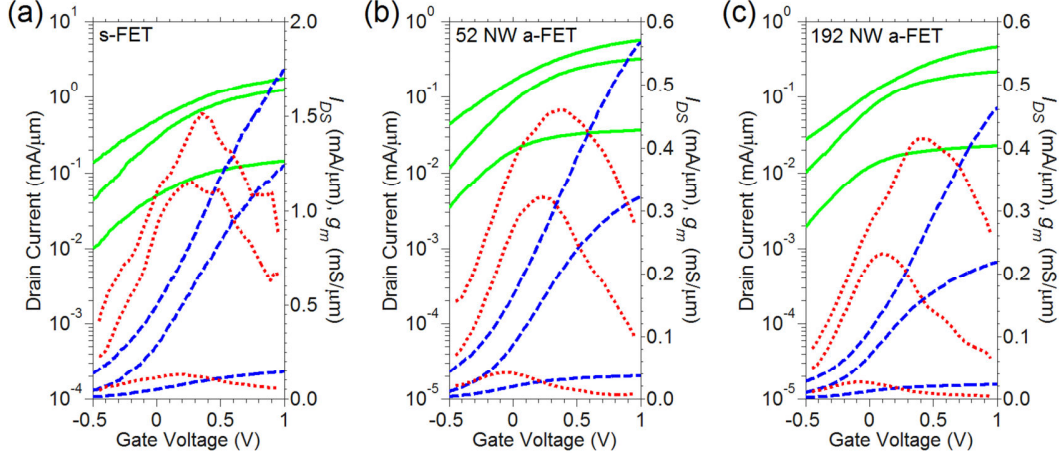
Fig. 2. DC transfer characteristics for V_{DS} = 0.05 V, 0.5 V, and 1.0 V, showing I_{DS} on a logarithmic scale (green, solid line), I_{DS} on a linear scale (blue dashed line), and g_m on a linear scale (red, dotted line), for (a) a s-FET, (b) a 52 NW a-FET, and (c) a 192 NW a-FET.

process (Fig. 1b). The sputtered W-gate is defined to 200 nm length by the thickness of an etched down polymer etch mask, using a SF_6 dry-etch process similar as with the nitride. The gate-drain top spacer is fabricated with a spin-coated polymer resist which is etched-back to around 300 nm. The top contact metal consist of 250 nm sputtered Ti/W/Au. A schematic cross-section of a device is shown in Fig. 1c. The ICL acts as source, and the top metal as the drain contact.

III. MEASUREMENTS AND SMALL-SIGNAL MODEL

DC characterization is performed with a Keithley 4200-SCS. For the D_{NW} = 45 nm devices, transfer characteristics for a single NW FET (s-FET), two a-FETs (52 and 192 NWs, respectively) are shown in Fig. 2a, 2b, and 2c, respectively. The peak transconductance is reduced for a-FETs as compared with the s-FETs, and the data is presented in Table I. Plots of output characteristics are shown in Fig. 3a and 3b for an s-FET and an a-FET (52 NWs), respectively. In Fig. 3c, g_m versus V_{GS} for three s-FETs is shown. At V_{DS} = 0.5 V, the best device show g_m = 1.37 mS/μm. The s-FET device referred to as NW1 is the same in Fig. 3a and 3c. In Fig. 3d, transconductance for several devices have been plotted against

Diameter / # of NWs	L_g (nm)	EOT (nm)	R_{SD} (Ωμm)	g_m (mS/μm)	I_{ON} (mA/μm)	SS (mV/dec)	DIBL (mV/V)
28 nm / 96	~300	1.3	~3000	0.15	0.06	140	110
45 nm / 192	~300	1.8	1630	0.23	0.13	540	240
45 nm / 52	~300	1.8	1240	0.32	0.17	480	320
45 nm / 1 (NW3)[a]	~200	1.8	310	1.09	0.59	420	260
45 nm / 1 (NW1)[a]	~200	1.8	210	1.19	0.67	500	320
45 nm / 1 (NW2)[a]	~200	1.8	190	1.37	0.75	800	600
13 nm / N/A[b]	230	2.4	170	1.72	0.9	180	-
25 nm / 1[c]	170	-	-	1.07	0.5*	260	-
15 nm / 1[d]	100	1.3	150	1.23	0.6	140	60
20x30 nm / 1[e]	20	1.2	~500*	1.65	0.54	88	7

Table I. Peak values listed for 45-nm s-FETs and 45-nm and 28-nm a-FETs with 52, 96, and 192 NWs, respectively. All our measures are normalized to NW circumference. Transconductance characteristics of the tabled s-FETs[a] are shown in Fig. 3c. As reference, data for a XOI FET[b] [14], a radial NW FET[c] [15], a lateral NW FET[d] [4], and a top down GAA FET[e] [16] are added. All values given for V_{GS}-V_T ≤ V_{DS} = 0.5 V, which is also here chosen as the definition for I_{ON}. Some values are estimates made by the authors*.

the on-resistance (R_{ON}) in order to correlate the transconductance with the access resistance. All our performance measures are normalized to circumference ($I_{DS,norm}$ = $I_{DS}/(n·π·D_{NW})$), where n is the number of NWs. For the D_{NW} = 45 nm NWs, the uniform doping coupled with the large diameter causes a substantial band bending inside the NWs, which limits the off performance. This is strongly dependent on the NW doping and radius, as the Fermi level movement is restricted towards the valence band due to the increasing D_{it} towards the valence band of InAs [11]. In Table I, we have as a reference included data for a 28-nm-diameter a-FET that shows a substantially improved subthreshold swing, SS. The fact that the thinner NWs show better off-state performance and lower DIBL is attributed to increased electrostatic control due to its smaller diameter and the thinner EOT. In contrast, a difference in conduction related to confinement effects is only expected for sub 15 nm NWs, as concluded from a simulation study of the band structure as a function of NW diameter scaling [12]. A further interesting point of reference is that reported data for InAs NW FETs with D_{NW} = 40 nm and L_G = 35 nm show SS = 130 mV/decade, a value that is significantly lower than the here reported values. This dissimilarity can be attributed to the three times higher doping used in the present study, preventing full depletion of the channel [13].

Comparing V_T for our D_{NW} = 45 nm s-FETs and a-FETs, devices show similar values (typically between -0.4 – -0.2 V) and there is no relation between V_T and peak transconductance, $g_{m,peak}$. Quantifying $g_{m,peak}$-widths, the values for s-FETs and a-FETs do not differ, suggesting there is not a significant spread in V_T within arrays that would cause a degraded maximum g_m. For reference, we have benchmarked our data with other high performance InAs and InGaAs NW FETs; a 13 nm planar XOI FET, L_G = 230 nm [14], a 25 nm diameter InAs/InP radial nanowire FET (Ω-gate, $I_{DS,norm}$ = $I_{DS}/(n·0.75π·D_{NW})$), L_G = 170 nm [15], a 15 nm in diameter lateral NW, L_G = 100 [4], and a top down rectangular GGA FET (20x30 nm), L_G = 20 nm [16].

Low frequency noise (LFN) characterization is made with a Stanford SR830 lock-in amplifier in series with a Stanford SR570 LNA. The current noise spectral density, S_{ID}, is
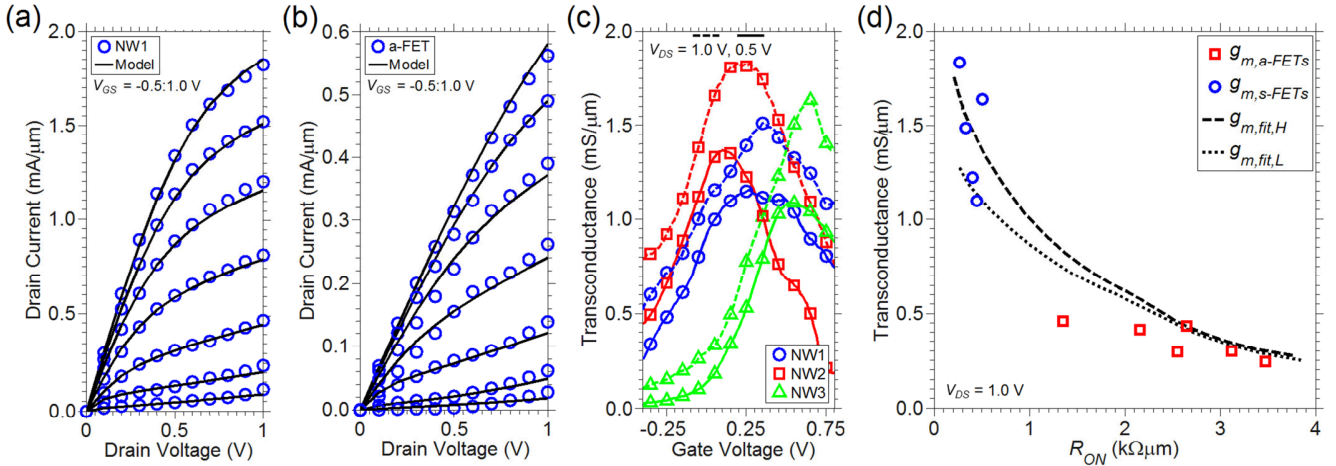
Fig. 3. I_{DS} versus V_{DS} (data normalized to circumference) for (a) a s-FET, and (b) a 52 NW a-FET. (c) g_m normalized to circumference versus V_{GS} for s-FETs. (d) Measured $g_{m,peak}$ normalized to circumference for a-FETs (red squares) and s-FETs (blue circles) plotted against measured R_{ON} at $V_{DS} = 1.0$ V. The black dashed line, $g_{m,fit,H}$, is simulated using the VS model for $v_{inj} = 1.7 \cdot 10^7$ cm/s and $L_G = 200$ nm. The black dotted line, $g_{m,fit,L}$, is simulated using the VS model for $v_{inj} = 1.2 \cdot 10^7$ cm/s and $L_G = 300$ nm.

measured for $V_{DS} = 50$ mV and $f = 10$ Hz. A common measure of comparison is the deduced gate voltage noise spectral density, $S_{VG} = S_{ID}/g_m^2$, normalized to the gate area ($S_{VG} \cdot L_G \cdot W_G$). Data for 2 s-FETs and 2 a-FETs is plotted in Fig. 4. The lowest levels for all the measured devices are determined to range in the interval $S_{VG} \cdot L_G \cdot W_G = 310 - 410$ $\mu m^2 \mu V^2$/Hz. Another common measure of comparison is the S_{ID} normalized to the drain current, S_{ID}/I_{DS}^2. The lowest measured levels are $S_{ID}/I_{DS}^2 = 0.9 \cdot 10^{-10} - 1.5 \cdot 10^{-10}$ Hz^{-1} and $S_{ID}/I_{DS}^2 = 0.9 \cdot 10^{-8} - 2.0 \cdot 10^{-8}$ Hz^{-1}, for two 52 NW a-FETs and two s-FETs, respectively. The measurements indicate that when accounting for the difference in total gate width, the extracted S_{Vg} for s-FETs and a-FETs show undeviating values. Further, comparing the $1/f$-noise to similar devices but fabricated with a higk-κ of HfO$_2$ only [15], the new devices improved the noise performance about one order of magnitude in terms of $S_{VG} \cdot L_G \cdot W_G = 5700$ $\mu m^2 \mu V^2$/Hz and even greater for $S_{ID}/I_{DS}^2 = 7.3 \cdot 10^{-7}$ Hz^{-1}. The decrease in LFN can be related to
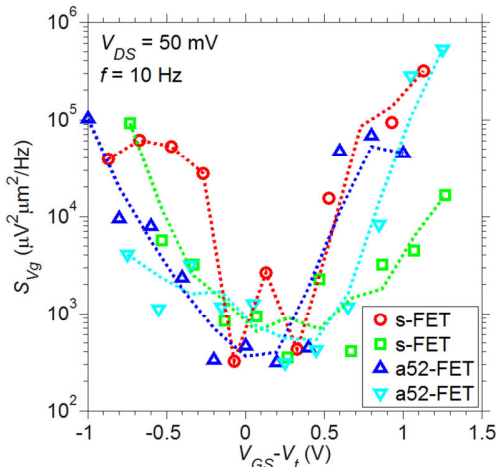

Fig. 4. S_{VG} plotted versus $V_{GS}-V_T$ for 4 different devices, two s-FETs and two 52 NW a-FETs. The data was measured at $V_{DS} = 50$ mV and $f = 10$ Hz and is normalized to total gate area, $L_G \cdot W_G$. The dotted lines are added to indicate the voltage dependence.

the introduction of an Al$_2$O$_3$ film, which more efficiently can reduce the amount of sub-oxides [11]. For comparison, the ITRS roadmap states that for the year 2015, multi-gate MOSFET devices for mm-wave applications should comply with $S_{VG} \cdot L_G \cdot W_G = 10.3$ $\mu m^2 \mu V^2$/Hz [17]. Further work is hence required to reach the target goals within the roadmap.

The RF characterization is performed using an Aglient E8361A network analyzer from 60 MHz to 40 GHz at a RF power of -27 dBm [5]. For measurements, a-FETs with 192 NWs was chosen on the premises of having a higher absolute g_m and a SEM image of the InAs mesa structure of one such device is shown in Fig. 5a. The highlighted areas show the location of where contact vias and pads will be formed in later stages. The deduced current gain, h_{21}, and unilateral power gain, U, for the best device is shown in Fig. 5b, for which $f_t = 14.6$ GHz and $f_{max} = 30.0$ GHz at $V_{DS} = 1.0$ V, and $V_{GS} = -0.45$ V, and -0.60 V, respectively. The RF data are fitted to a standard MOSFET small-signal model [5] where the parasitic elements are included in Fig. 5c. For simplicity, impact ionization was not accounted for as it turned out to have negligible effect in the fitting to the measured data. Statistics over 4 devices show f_t in an interval of 9.7-17.4 GHz and f_{max} of 20.3-30.0 GHz, at $V_{DS} = 1.0$ V.

IV. DC DEVICE MODELING

To describe the transistor characteristics of the $D_{NW} = 45$ nm devices, a virtual source (VS) model is fitted to the measured DC data [18]. The model is based on a channel charge equation and also provides a coherent intrinsic gate capacitance [19]. Modeled devices are chosen on the premises of low R_{ON} in combination with less pronounced impact ionization, thus being able to neglect the later. Since a direct measurement of the NW contact and channel resistivity is difficult, we do a simultaneous fit of the VS-model parameters with estimates of the source/drain resistance. For a s-FET (referred as NW1), assuming a NW resistivity of $1.0 \cdot 10^{-3}$ Ωcm [20] and a first spacer layer thickness of 67 nm (60 nm Si$_3$N$_4$ + 7 nm high-κ), we obtain $R_S = 65$ $\Omega\mu$m. The metal-ICL

(a)

(b)

(c)

$R_g = 5\ \Omega$ $g_m = 14.5\ mS,\ g_{ds} = 0.11\ mS$ $R_D = 33\ \Omega$

V_{gs} v'_{gs} C_{gs} C_{gd} $g_m v'_{gs}$ g_{ds} C_{ds} V_{ds}

$R_S = 34\ \Omega$ $C_{gs} = 110\ fF,\ C_{gd} = 33\ fF,\ C_{ds} = 1\ fF$
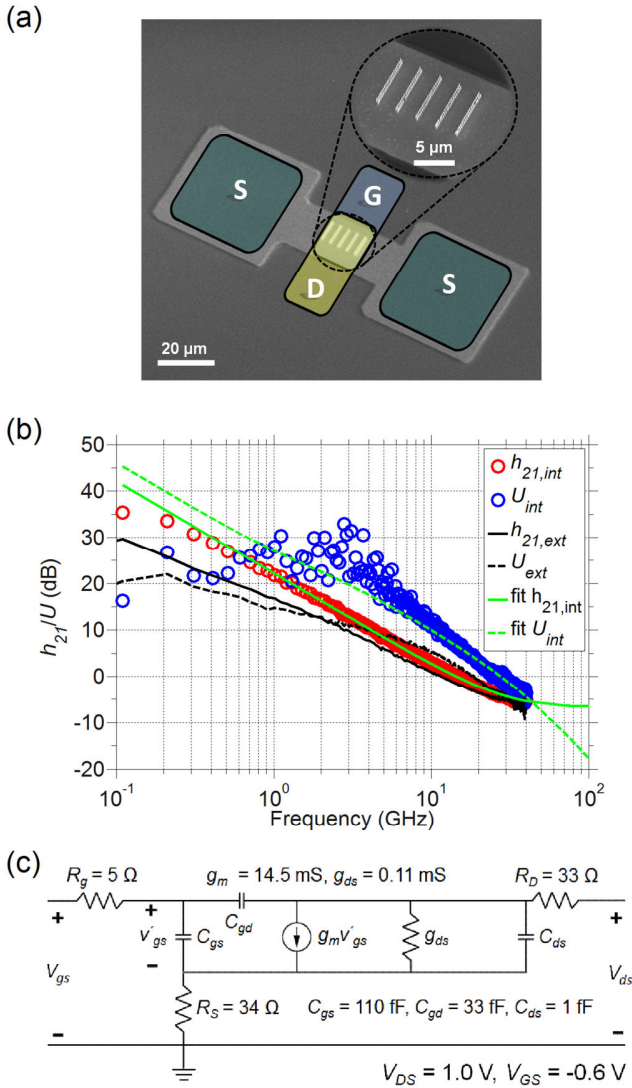
$V_{DS} = 1.0\ V,\ V_{GS} = -0.6\ V$

Fig. 5. (a) SEM image with highlighted areas for the source via contacts, S, the gate pad, G, and the drain pad, D, and where the intrinsic region corresponds to the quadratic area in the center, also shown at higher magnification. (b) The graph is showing intrinsic and extrinsic current gain, $h_{21,int}$ and $h_{21,ext}$, respectively, and intrinsic and extrinsic unilateral power gain, U_{int} and U_{ext}, respectively, for a 192 NW a-FET device. Also, fitting of a small-signal model to the intrinsic data is added (fit $h_{21,int}$ and fit U_{int}). (c) Extracted small-signal parameters for the measured device at $V_{DS} = 1.0$ V and $V_{GS} = -0.6$ V.

contact resistance is measured to be in the order of 2 Ω and is for simplicity counted as a constituent of the ICL. For the s-FET, the 18 Ω series resistance contribution from the ICL, corresponding to 2.5 Ωµm, can be ignored. Fitting the data in Fig. 3a gives $R_D = 141$ Ωµm, equivalent to 300 nm resist top spacer thickness (translating to 160 nm non-gated resistive NW segment length, see Fig. 1c) and in agreement with the experimental implementation. At a gate length of $L_G = 200$ nm, we obtain values of mobility, $\mu_{LOW-FIELD} = 1300$ cm^2/Vs and $v_{inj} = 1.7 \times 10^7$ cm/s. While the rather low mobility can be expected for a highly doped surface channel, the injection velocity is in the same range as is reported for an InAs HEMT of similar gate length [2] ($v_{inj} \sim 2 \times 10^7$ cm/s).

(a)

52 NWs

$R_{d,NW} = 115\ \Omega$

$R_{s,NW} = 36\ \Omega$

$R_{s,ICL} = 18\ \Omega$

(b)

192 NWs

$R_{d,NW} = 33\ \Omega$

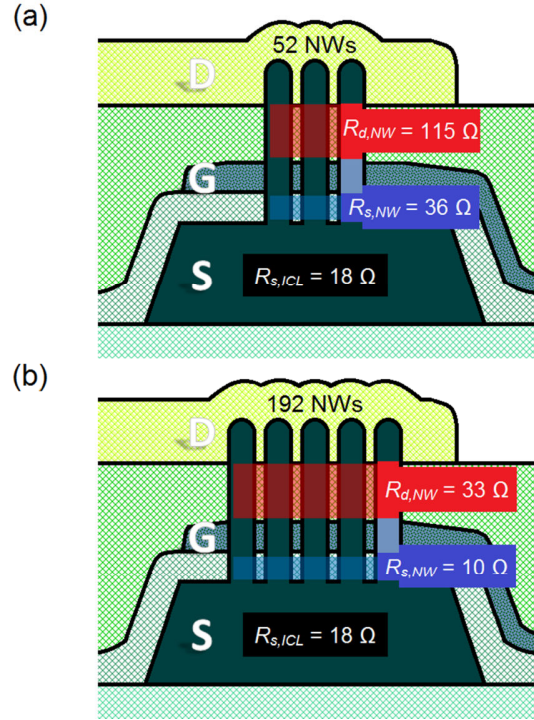$R_{s,NW} = 10\ \Omega$

$R_{s,ICL} = 18\ \Omega$

Fig. 6. Schematic illustration of the distribution of the parasitic series resistance extracted from DC measurements and VS modeling where the subscripts $R_{S,ICL}$ and $R_{S,NW}/R_{D,NW}$ are the series resistances associated with the ICL and the NW, respectively. Values are shown for (a) a 52 NW a-FET and (b) a 192 NW a-FET.

To analyze a-FETs, the fitted model for the s-FET is expanded and fitted to an a-FET with 52 NWs. The significant increase in R_{ON} for a-FETs compared to s-FETs can in part be explained by the undoped ICL that adds 18 Ω source series resistance, see Fig. 6. In order to obtain a good fit, however, it is needed to reduce v_{inj} by around 30% and also increase the resistivity of the NWs by a factor of around 4, and this fitting is shown in Fig. 3b. The decrease in v_{inj} can be explained by longer channels for a-FETs as compared with the s-FET (as well as thicker spacer layers) due to the defining polymer resist, used for the etch-back of the gate, that tends to become thicker around arrays. The steep increase in series resistance can, however, not be explained simply by a thicker gate-drain separation. Instead, it must be considered that the doping incorporation of the surfactant Sn is higher for single NWs as compared to NWs grown in arrays due to the limited collection area for the a-FETs during the vapor liquid solid (VLS) growth. The radial band bending inefficiency for the 45-nm-diameter NW FETs, as described earlier, can effectively be modeled as a parasitic parallel conduction. For the measured s-FET in Fig. 3a, it is in the order of 0.25 mS/µm. For a-FETs, this value is about 4-6 times lower, however, the transfer characteristics are not significantly improved compared to s-FETs as the transconductance is reduced by a similar factor due to series resistance. The variance in characteristics between devices with equal number of NWs is thought to be related to diameter variation (NWs in arrays typically vary between 40 - 45 nm) in combination with variations of separation layer thicknesses over the sample. To compare the effect of the reduced v_{inj} with the effect of

external resistances, we plot in Fig. 3d calculated values for the extrinsic transconductance, $g_{m,ext,}$, as a function of R_{ON}, using the VS model. In the plot there are two lines representing two values of v_{inj} (the fitted s-FET and a-FET) corresponding to $L_G = 200$ nm ($g_{m,fit,H}$) and $L_G = 300$ nm ($g_{m,fit,L}$), respectively. Comparing the simulated data with the experimentally measured $g_{m,ext}$, a good fit can be obtained. This indicates that the external resistances are the major source for device performance degradation for a-FETs as compared with s-FETs. This can essentially be described using the conventional formula relating the extrinsic and intrinsic transconductance $g_{m,ext} = g_{m,int}/ (1 + g_{m,int} \cdot R_S + g_{d,int} \cdot (R_S + R_D))$ [21]. Here g_d is the output conductance. From the average experimental data for the s-FETs shown in Fig. 3c, we deduce a value for the intrinsic transconductance, $g_{mi} = 2.4$ mS/µm. For the a-FETs, this value range between $0.5 – 0.7$ mS/µm.

The total parallel resistance contributions from the un-gated segments of the NWs are shown in Fig. 6a and 6b for a 52 NW a-FET and a 192 NW a-FET, respectively. Comparing the normalized series resistance contributions attributed to the un-gated NW segments (omitting the ICL), $R_S = 265$ Ωµm and $R_D = 845$ Ωµm for the 52 NW a-FET, and $R_S = 270$ Ωµm and $R_D = 900$ Ωµm for the 192 NW a-FET. These values are quite close as expected (2% and 6% in difference for R_S and R_D, respectively). For a 52 NW a-FET, the ICL (18 Ω) adds another 12 % to the total series resistance while for a 192 NW a-FET, the series resistance contribution from the ICL adds another 42 %. This explains why a 52 NW a-FET has better normalized DC performance than a 192 NW a-FET.

V. RF DEVICE MODELING

Performing electrostatic simulations of the capacitances of the de-embedded structure of 12x12 µm² [5], that is the overlapping source-gate and gate-drain areas, as indicated in Fig. 5a with the overlapping rectangles, the parasitic capacitances $C_{gs,p}$ and $C_{gd,p}$ are determined to 131 fF and 16 fF, respectively. The substantially larger $C_{gs,p}$ originates from the thinner source spacer layer and higher permittivity of the Si_3N_4 as compared with the drain spacer. Taking into account the low density of states for InAs, the high frequency intrinsic gate capacitance, $C_{gg,i}$, for 192 NWs is simulated to be in the interval of 6 fF to 23 fF for $V_{GS} – V_T$ varying between -0.5 V to 0.5 V, at $V_{DS} = 1$ V. Considering the low measurement gate bias and assuming that the $C_{gg,i}$ contribution lies in the middle of the given range, the simulated number ($C_{gg,tot} = 5.95$ fF/µm) is 13 % larger than the number extracted from the measurement ($C_{gg,tot} = 5.27$ fF/µm). Actual pad size difference compared to the patterned area as well as uncertainty in the spacer layer thicknesses and dielectric constants are likely the reasons for the deviation between measured and calculated capacitances. The extracted $g_{m,int}$ of 0.53 mS/µm corresponds to a $g_{m,ext}$ of 0.36 mS/µm, which can be related to the maximum $g_{m,ext}$ measured at DC for the same device ($g_{m,ext} = 0.30$ mS/µm, 20 % lower). The low V_{GS} in the measurement for maximum f_t and f_{max} suggest a shift in V_T as compared to DC ($V_T = -0.45$ V for $V_{DS} = 1$ V). Both the shift in V_T and the increase in g_m can be related to slow traps that are not responding at higher frequencies, thus explaining the lowering

of the V_T and a frequency dependent g_m [22]. Comparing the series resistances from the RF model extraction with those from the VS model fitting of the DC measurements, they are found to be fairly similar. The RF extraction gives $R_S = 34$ Ω and $R_D = 33$ Ω while the DC measurements translates into $R_S = 28$ Ω and $R_D = 33$ Ω.

VI. DISCUSSION

Based on the data presented in this paper we draw some general conclusions regarding III-V NWs and their implementation; although high intrinsic performance, that is high transconductance and drive currents, has been demonstrated in various forms of III-V nanowires [4][14][15][16], it is clear that the implementation of RF-compatible devices still is a challenge. Analysis of planar III-V MOSFETs [23] show that the control of the access resistance is one of the key parameters to increase the transconductance and to obtain attractive RF-properties. The method used in the here presented implementation, that is uniform doping of the transistor channel, needs further refinement beyond diameter scaling in order to avoid increase in the access resistance. Increased doping control may be one alternative to reduce the source/drain resistance [9]. Alternatively, the access regions may be regrown, although at the cost of parasitic capacitance [10]. A heterobarrier may also be included into the channel to increase the carrier control [24]. It appears that a combination of these appraoches may be required to fully exploit the potential of the high III-V injection velocity for RF-compatible MOSFETs in either vertical or lateral geometry.

VII. CONCLUSION

The performance of s-FET performance has been evaluated ($g_{m,ext} = 1.37$ mS/µm). Based on a virtual source model we are able to accurately model and determine intrinsic transport properties including $v_{inj} = 1.7 \cdot 10^7$ cm/s. The performance is degraded by series resistance for devices consisting of arrays of NWs. The introduction of a thin Al_2O_3 film combined with an outer HfO_2 film may be responsible for the measured reduction in $1/f$-noise compared to similar devices fabricated with HfO_2 only.

REFERENCES

[1] C. P. Auth, J. D. Plummer , "Scaling theory for cylindrical, fully-depleted, surrounding-gate MOS-FET's," *IEEE Electron Device Letters,* vol.18, no.2, pp.74-76, Feb. 1997.

[2] D.-H. Kim, J. A. del Alamo, D. A. Antoniadis and B. Brar, "Extraction of Virtual-Source Injection Velocity in sub-100 nm III-V HFETs," *IEEE International Electron Devices Meeting (IEDM)*, 2009, vol., no., pp. 35.4.1 - 35.4.4, 7-9 Dec. 2009.

[3] A. M. Crook, E. Lind, Z. Griffith, M. J. W. Rodwell, J. D. Zimmerman, A. C. Gossard, and S. R. Bank, "Low resistance, nonalloyed Ohmic contacts to InGaAs," *Appl. Phys. Lett.*, vol. 91, no.

19, pp. 192114, Nov. 2007..

[4]   [4] A. Dey, C. Thelander, E. Lind, K. D. Thelander, M. Borg, M. Borgström, P. Nilsson, L.-E. Wernersson, "High-Performance InAs Nanowire MOSFETs," *IEEE Electron Device Lett.*, vol. 33, no. 6, pp. 791-793, Jun 2012.

[5]   S. Johansson, M. Egard, S. Gorji Ghalamestani, B. Mattias Borg, M. Berg, L.-E. Wernersson, and E. Lind, "RF Characterization of Vertical InAs Nanowire Wrap-Gate Transistors Integrated on Si Substrates," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no 10, pp. 2733 – 2738, Oct. 2011.

[6]   W. Prost and F. J. Tegude, "Fabrication and RF performance of InAs nanowire FET," *Device Research Conference (DRC), 2010*, vol., no., pp.279-282, 21-23 June 2010.

[7]   T. Takahashi, K. Takei, E. Adabi, Z. Fan, A. M. Niknejad, and A. Javey, "Parallel Array InAs Nanowire Transistors for Mechanically Bendable Ultrahigh Frequency Electronics," *ACS Nano, vol. 4, no. 10*, pp. 5855-5860, Sep. 2010.

[8]   K.-M. Persson, M. Berg, M. Borg, J. Wu, H. Sjoland, E. Lind and L.-E. Wernersson, "Vertical InAs Nanowire MOSFETs with I_{DS} = 1.34 mA/μm and g_m = 1.19 mS/μm at V_{DS} = 0.5 V," *IEEE Device Research Conference (DRC), 2012*, vol., no., pp. 195-196, 18-20 June 2012.

[9]   G. Astromskas, K. Storm, O. Karlström, P. Caroff, M. Borgström, and L.-E. Wernersson, "Doping Incorporation in InAs nanowires characterized by capacitance measurements," *J. Appl. Phys.*, vol. 108, no. 6, pp. 054306, Sep. 2010.

[10]   K. Jansson, E. Lind, and L.-E. Wernersson., "Performance Evaluation of III–V Nanowire Transistors," *IEEE Trans. Electron Devices.*, vol. 59, no. 9, pp. 2375–2382, Sep. 2012.

[11]   J. Wu, E. Lind, R. Timm, M. Hjort, A. Mikkelsen, and L.-E. Wernersson, "Al₂O₃/InAs metal-oxide-semiconductor capacitors on (100) and (111)B substrates," *Appl. Phys. Lett.*, vol. 100, no. 13, pp. 132905, Mar. 2012.

[12]   K.-M. Persson, E. Lind, A. Dey, C. Thelander, H. Sjöland, and L.-E. Wernersson, "Low-Frequency Noise in Vertical InAs Nanowire FETs," *IEEE Electron Dev. Lett.*, vol. 31, no. 5, pp. 428-430, May 2010.

[13]   E. Lind, M. P. Persson, Y.-M. Niquet, and L.-E. Wernersson, "Band Structure Effects on the Scaling Properties of [111] InAs Nanowire MOSFETs," *Electron Devices, IEEE Transactions on* , vol.56, no.2, pp.201,205, Feb. 2009.

[14]   K. Takei, S. Chuang, H. Fang, R. Kapadia, C.-H. Liu, J. Nah, H. S. Kim, E. Plis, S. Krishna, Y.-L. Chueh, and A. Javey, "Benchmarking the performance of ultrathin body InAs-on-insulator transistors as a function of body thickness," *Appl. Phys. Lett.*, vol. 99, no. 10, pp. 103507, Sep. 2011.

[15]   X. Jiang, Q. Xiong, S. Nam, F. Qian, Y. Li, and C. M. Lieber, "InAs/InP radial nanowire heterostructures as high electron mobility devices," *Nano Lett.*, vol. 7, no. 10, pp. 3214–3218, Sep. 2007.

[16]   J. J. Gu, X. W. Wang, H. Wu, J. Shao, A. T. Neal, M. J. Manfra, R. G. Gordon, and P. D. Ye, "20-80 nm Channel Length Gate-all-around Nanowire MOSFETs with EOT=1.2nm and Lowest SS = 63mV/dec," *IEEE International Electron Device Meeting (IEDM)*, 2012, 10-12 Dec 2012.

[17]   International Technology Roadmap for Semiconductors. [Online]. Available: http://public.itrs.net

[18]   A. Khakifirooz, O. M. Nayfeh, and D. Antoniadis, "A Simple Semiempirical Short-Channel MOSFET Current–Voltage Model Continuous Across All Regions of Operation and Employing Only Physical Parameters", *IEEE Trans. Electron Devices,* vol. 56, no. 8, pp 1674-1680, Aug 2009.

[19]   L. Wei, O. Mysore, and D. Antoniadis, "Virtual-Source-Based Self-Consistent Current and Charge FET Models: From Ballistic to Drift-Diffusion Velocity-Saturation Operation," *IEEE Trans. Electron Devices,* vol. 59, no. 5, pp 1263-1271, May 2012.

[20]   C. Thelander, K. A. Dick, M. T. Borgström, L. E. Fröberg, P. Caroff, H. A. Nilsson, and L. Samuelson, "The electrical and structural properties of n-type InAs nanowires grown from metal-organic precursors," *Nanotechnol.*, vol. 21, no. 20, pp. 1-9, Apr. 2010.

[21]   Chou, S.Y.; Antoniadis, D.A., "Relationship between measured and intrinsic transconductances of FET's," *Electron Devices, IEEE Transactions on* , vol.34, no.2, pp.448,450, Feb 1987

[22]   S. Johansson, M. Berg, K.-M. Persson, and E. Lind, "A High-Frequency Transconductance Method for Characterization of High-κ Border Traps in III-V MOSFETs," *IEEE Trans. Electron Devices,* vol.60, no.2, pp.776-781, Feb. 2013.

[23]   M. Egard, et al., "High-Frequency Performance of Self-Aligned Gate-Last Surface Channel In₀.₅₃Ga₀.₄₇As MOSFET," *Electron Device Letters, IEEE* , vol.33, no.3, pp.369-371, March 2012.

[24]   L.E. Froberg, C. Rehnstedt, C. Thelander, E. Lind, L.-E. Wernersson, and L. Samuelson, "Heterostructure Barriers in Wrap Gated Nanowire FETs," *Electron Device Letters, IEEE*, vol.29, no.9, pp.981-983, Sept. 2008.

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