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High Current Density InAsSb/GaSb Tunnel Field Effect Transistors

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Introduction. Steep-slope devices, such as tunnel field-effect transistors (TFETs), have recently gained interest due to their potential for low power operation at room temperature. The devices are based on inter-band tunneling which could limit the on-current since the charge carriers must tunnel through a barrier to traverse the device. The InAs/GaSb heterostructure forms a broken type II band alignment which enables inter-band tunneling without a barrier, allowing high on-currents. We have recently demonstrated high current density ($I_{ON,\ reverse}$ = 17.5 mA/μm^2) nanowire Esaki diodes[1] and in this work we investigate the potential of InAs/GaSb heterostructure nanowires to operate as TFETs. We present device characterization of $InAs_{0.85}Sb_{0.15}$/GaSb nanowire TFETs, which exhibit record-high on-current levels.

Device fabrication. The nanowires were grown from Au aerosols on a GaAs substrate using metal organic vapor phase epitaxy[2]. For the nucleation of the GaSb segment, a short stem of GaAs was first grown. Zn doping was introduced to reduce the series resistance in the GaSb segment, which was followed by growth of an unintentionally doped InAsSb top segment as well as a thin shell of InAsSb covering the GaSb segment. This shell facilitates the contact formation to GaSb and also allows for single-step source and drain contact process. At the final stage of the growth, the nanowires were annealed to form a neck region at the InAsSb/GaSb heterointerface, which reduces the conducting area and suppresses potential shell leakage currents[3]. The nanowires were transferred onto a prepatterned Si chip where source, drain and gate electrodes were defined by electron beam lithography and thermal evaporation of Ni/Au. An Al_2O_3/HfO_2, 3/70 cycles (0.3/8 nm), bilayer deposited at 100 ^oC with atomic layer deposition was used as a gate dielectric.

Electrical characterization. A record high on-current of 110 μA/μm (I_{DS} = 19 μA, circumference = 0.17 μm) was measured for $V_{DS} = V_{GS}-V_T$ = 0.5 V, with R_{ON} = 20 kΩ = 3.5 Ω·mm. Furthermore, the devices show a distinct negative differential resistance characteristic with a peak to valley ratio of 3. The maximum peak current density, with V_{DS} applied on the GaSb side, was measured to 1.2 mA/μm^2, with a peak position that moves to slightly higher V_{DS} with increasing positive V_{GS}. A fixed peak position with varying peak current suggests that the gate is indeed affecting the bands at the heterojunction and that the device is not a tunnel junction in series with a field effect transistor. The limited off-characteristics found for these devices are here likely affected by inter-band tunneling in the gate-drain region and/or hole accumulation under the gate. A conservative evaluation of the subthreshold swing (SS), at the slope on the gentle side of the hysteresis loop, representing an upper bound value, would be 300 mV/decade at V_{DS} = 0.3 V. Furthermore, the devices also show an I_{ON}/I_{OFF} ratio of 275 at V_{DS} = 0.3 V. Extraction of the SS is made difficult because of hysteresis in the transfer characteristics, possibly caused by trapped charges in the gate dielectric.

1. High Current Density Esaki Tunnel Diodes Based on GaSb-InAsSb Heterostructure Nanowires. B. Ganjipour, A.W. Dey, B. M. Borg, M. Ek, M.-E. Pistol, K. A. Dick, L.-E. Wernersson, and C. Thelander. *Nano Letters* 2011 *11* (10), 4222-4226
2. Formation of the Axial Heterojunction in GaSb/InAs(Sb) Nanowires with High Crystal Quality. M. Ek, B. M. Borg, A. W. Dey, B.Ganjipour, C.Thelander, L.-E.Wernersson, and K. A. Dick. *Crystal Growth & Design* 2011 *11* (10), 4588-4593
3. Diameter reduction of nanowire tunnel heterojunctions using in situ annealing. B. M. Borg, M. Ek, K. A. Dick, B. Ganjipour, A. W. Dey, C. Thelander, and L.-E. Wernersson, *Appl. Phys. Lett.* 99, 203101, 2011

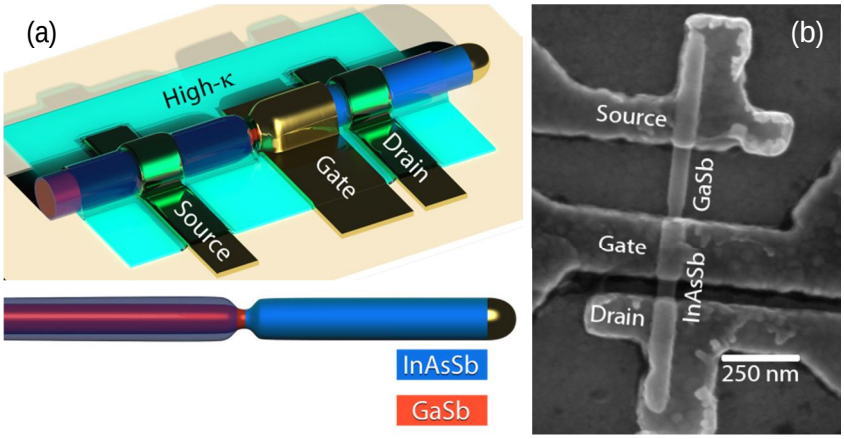

Fig. 1. (a) Schematic layout of an InAsSb/GaSb TFET. (b) SEM image of an InAsSb/GaSb TFET device. Electrode configuration for reverse biased operation.

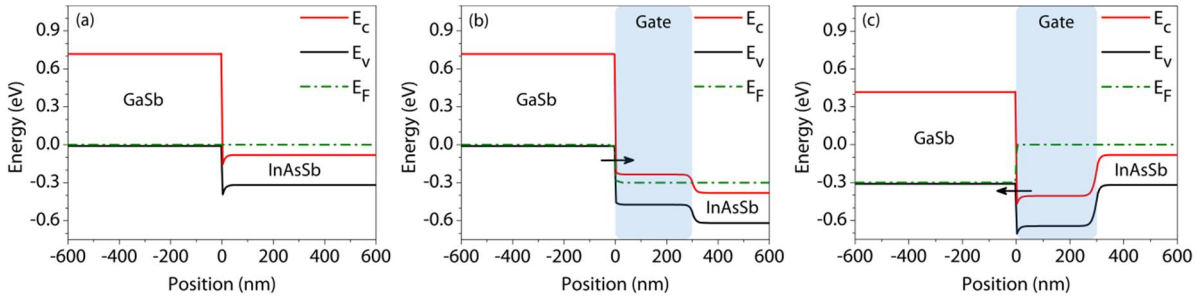

Fig. 2. Simulated band structure of an ideal InAsSb/GaSb heterointerface. (a) The band structure at equilibrium. (b) Reverse biased (positive drain bias on the InAsSb segment and GaSb grounded) with a positive gate voltage applied. (c) Forward biased (positive drain bias on the GaSb segment and InAsSb grounded) with a positive gate voltage applied.

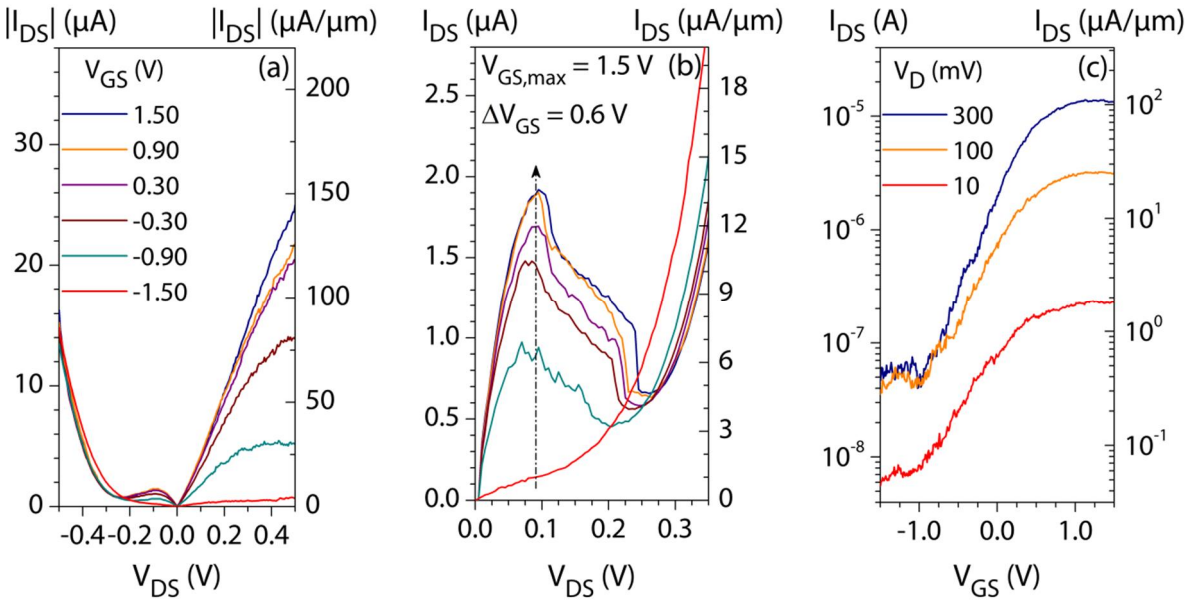

Fig. 3. Output and transfer characteristics of an InAsSb/GaSb TFET at room temperature. (a) Reverse biased with GaSb grounded. (b) Forward biased with InAsSb grounded. (c) Reverse biased with GaSb grounded.