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Digital Phase Locked Loops for Radio Frequency Synthesis

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LUND UNIVERSITY

Doctoral Thesis
Electrical Engineering
Lund, December 2017

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Popular Science

The demand of handsets with high data rate capability, more complex features and long battery life at an affordable cost has been the driving force behind most innovations in wireless communication systems for consumer electronics. These innovations have made radio communication smooth and efficient, thereby maximizing its impact worldwide and reshaping the way data is shared between people.

Central to wireless communication systems are the radio transmitter and receiver, which are responsible for transmitting and receiving data between wireless devices. A key function in both is *frequency generation*, which is needed to place the transmitted data in a very well controlled region of the frequency spectrum (typically, at radio-frequency, RF), and, conversely, to transfer the received data from RF to the original low frequency. Frequency generation is usually accomplished by means of a *phase-locked loop* (PLL), where, starting from a very stable reference frequency of a few tens of MHz, very precise frequencies up to several GHz are synthesized.

The wireless communication environment is very hostile, with many interference sources potentially able to contaminate the often tiny desired signal. This poses tough requirements on the purity of the RF signal generated by the PLL, since the PLL must coexist with a number of other radio blocks integrated on the same silicon die. In particular, the ever larger digital signal processing units in the typical radio fabricated in a modern CMOS process generate a large amount of switching noise, caused by all commutations between logic 0 and logic 1 occurring there, which may easily affect the integrity of the PLL.

At the same time, the conventional circuit design of analog functions, of which the PLL is an example, is becoming increasingly problematic, as ultra-scaled CMOS technologies mandate the use of very low power supply voltages, as a consequence of the extremely reduced dimensions of the CMOS devices.

Furthermore, the effort associated to bring about such a technology scaling has turned once cheap CMOS processes into very expensive ones, and the relatively large area occupied by analog circuits is weighing heavily on the total cost of the radio transceiver.

Because of the above reasons, we are witnessing an unrelenting migration of analog functions towards the digital domain, and the foremost example of this is the digital PLL, which can exploit all the advantages, in terms of programmability, reconfigurability, adaptivity, and compactness, that are beyond the reach of the traditional PLL

In this dissertation, several techniques are demonstrated, that improve the design of the digital PLL, in terms of both overall architecture and individual PLL sub-blocks, obtaining excellent performances.

Contents

Preface

This thesis summarizes my academic work carried out in the mixed-signal group at the department of Electrical and Information Technology, Lund University, Sweden, from November 2012 to August 2017. In the following, I will describe my contributions to the published papers I have co-authored.

I L. Fanori, **A. Mahmoud**, T. Mattsson, P. Caputa, S. Ramo, and P. Andreani,"A 2.8-to-5.8 GHz harmonic VCO in a 28 nm UTBB FD-SOI CMOS process," in Radio Frequency Integrated Circuits Symposium (RFIC), 2015 IEEE, 2015, pp. 195-198.

Contributions. I helped the first author with circuit simulations and measurements on the designed oscillator.

II **A. Mahmoud**, L. Fanori, T. Mattsson, P. Caputa, and P. Andreani, "A 2.8-to-5.8 GHz harmonic VCO based on an 8-shaped inductor in a 28 nm UTBB FD-SOI CMOS process," Analog Integrated Circuits and Signal Processing, vol. 88, no. 3, pp. 391-399, 2016.

Contributions. I performed all of the analysis and simulations of the magnetic coupling of the 8-shaped inductor. I helped the first author with circuit simulations and measurements on the designed oscillator. I wrote the section about the magnetic coupling, and re-wrote the rest.

III **A. Mahmoud**, P. Andreani, and P. Lu, "A 65nm CMOS fraction-N digital PLL with shaped in-band phase noise," in Nordic Circuits and Systems Conference (NORCAS): NORCHIP & International Symposium on System-on-Chip (SoC), 2015. IEEE, 2015, pp. 1-4.

Contributions. I performed a large part of the PLL modeling, simulation, implementation, and layout design. I wrote most of the manuscript.

IV **A. Mahmoud**, P. Andreani, and P. Lu, "A wide band fractional-N digital PLL with a noise shaping 2-D time to digital converter for LTE-A applications,"Analog Integrated Circuits and Signal Processing, vol. 89, no. 2, pp. 337-345, 2016.

Contributions. I performed a large part of the PLL modeling, simulation, implementation, and layout design. I performed all the analysis and simulation of the $\Delta\Sigma$ quantization noise cancellation scheme. I wrote the manuscript.

V **A. Mahmoud**, P. Andreani and F. Pepe, "A 2.8-3.8-GHz Low-Spur DTC-Based DPLL With a Class-D DCO in 65-nm CMOS," in IEEE Microwave and Wireless Components Letters, vol. PP, no. 99, pp. 1-3.

Contribution I performed most of the modeling, simulation, implementation, and layout design; I took the measurements, and wrote the manuscript.

Valuable help and guidance have been received from my co-authors during different stages of each work. My supervisor' contributions from the idea, design development, simulations up to manuscript production significantly enhanced the quality of work.

Acknowledgments

As I am approaching the final stage of my graduate career at EIT, I realize I have been blessed by God to collaborate with several people that were very supportive in my research. I believe I would not have been able to accomplish so much without the help from so many.

First and foremost, I would like to express my deepest gratitude to my supervisor Associate Professor Pietro Andreani. His support is always there whenever I need it. His guidance helped me to overcome numerous difficulties encountered during my research.

I also would like to thank my co-supervisors, Dr. Luca Fanori, Dr. Ping Lu and Dr. Federico Pepe. I am greatly indebted to them, and respectful for the encouragements and support they have given me all throughout my graduate studies. I have learnt a great deal from them. Thank you for always having time for me and for all the valuable suggestions and discussions over the years.

I want to thank, too, the many colleagues and friends who have directly or indirectly contributed to my work and have made this experience all themore valuable: Mohammed, Rakesh, Yang, Mojtaba, Dimitar, Farrokh, Breeta, Babak, Oskar, Xiaodong, Siyu, Hemanth, Steffen, Jesús, Muris, Anders, Waqas, Jonas, Mattias, Dejan, and Therese, for the many discussions and the generous help they provided.

I would like to sincerely thank the seniors at the department of EIT. Professor Viktor Öwall, Professor Henrik Sjöland, Associate Professor Markus Törmänen, Associate Professor Joachim Rodrigues, Associate Professor Erik Larsson and Associate Professor Liang Liu. I also thank them for giving me the opportunity to work with many talented researchers.

I would like to thank Göran Jönsson for his great help in the measurement lab, and the people providing various kind of technical support, foremost Andreas Johansson, Erik Jonsson, Stefan Molund and Martin Nilsson. I also ex-

press my gratitude to all the people involved in administrative support, especially Pia Bruhn and Anne Andersson.

Last but not the least, I am deeply indebted to my family. Words cannot express how grateful I am to my parents, my wife, my daughter and my siblings for always been supportive to my work, studies, and research. Although I spent nights and weekends at work, my wife, my better half, always supported me, gave me courage, and made our life full of happiness and love. Finally, I thank all my friends in Sweden and Egypt for their trust and support.

Ahmed Mahmoud

List of Abbreviations

ADC	Analog to Digital Converter
BB	Bang-Bang
BBPD	Bang-Bang Phase Detector
BPF	Band Pass Filter
CAD	Computer-Aided Design
CMOS	Complementary Metal Oxide Semiconductor
CP	Charge Pump
CSI	Current-Starved Inverter
CT	Continuous-Time
DAC	Digital to Analog Converter
DAFS	Direct Analog Frequency Synthesizer
DCO	Digitally Controlled Oscillator
DDFS	Direct Digital Frequency Synthesizer
DLF	Digital Loop Filter
DNL	Differential Non-Linearity
DPLL	Digital Phase Locked Loop
DR	Dynamic Range
DSP	Digital Signal Processor
DT	Discrete-Time
DTC	Digital-to-Time Converter
EM	Electromagnetic
FAC	Frequency Acquisition Controller

FCW	Frequency Control Word
FDD	Frequency Division Duplex
FGRO	Fast-Delay GRO
FM	Frequency Modulation
FOM	Figure-of-Merit
GRO	Gated Ring Oscillator
GVTDC	Gated-Vernier TDC
HB	High-Band
HPF	High Pass Filter
IC	Integrated Circuit
IF	Intermediate Frequency
IIR	Infinite Impulse Register
IMD	Intermodulation Distortion
INL	Integral Non-Linearity
ISF	Impulse Sensitivity Function
LB	Low-Band
LBR	Loop Bandwidth Regulation
LC	Inductor-Capacitor
LDO	Low-Drop-Output Regulator
LF	Loop Filter
LFSR	Linear Feedback Shift Register
LMS	Least Mean Square
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
LSB	Least Significant Bit
LTE-A	Long Term Evolution-Advanced
LTV	Linear Time Variant
MASH	Multi-stAge noise SHaping
MIM	Metal-Insulator-Metal
MMD	Multi-Modulus Divider
MOM	Metal-Oxide-Metal
MUX	Multiplexer
NCO	Numerically Controlled Oscillator
NTF	Noise Transfer Function

PA	Power Amplifier
PD	Phase Detector
PFD	Phase Frequency Detector
PI	Proportional-Integral
PLL	Phase Locked Loop
PSD	Power Spectral Density
PSS	Periodic Steady State
PVT	Process, Voltage and Temperature
RF	Radio Frequency
Rx	Receiver
SCI	Shunt-Capacitor Inverter
SGRO	Slow-Delay GRO
STF	Signal Transfer Function
TA	Time Amplifier
TDC	Time to Digital Converter
TDD	Time Division Duplex
TR	Tuning Range
Tx	Transmitter
UTBB FD-SOI	Ultra-Thin Body and Buried Oxide Fully Depleted Silicon on Insulator
VCO	Voltage Controlled Oscillator

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1 Introduction

1.1 MOTIVATION

Over the last few decades, wireless communication has become increasingly essential in everyday life. The tremendous growth of wireless systems can be traced back to the prodigious development in semiconductor technology, where the aggressive scaling of Complementary Metal Oxide Semiconductor (CMOS) processes makes it possible to integrate hugely complex systems on a single silicon chip of minuscule dimensions (often much smaller than 1 cm^2). This unrelenting CMOS scaling has led to numerous innovations in both digital and analog Integrated Circuit (IC) design, which are largely responsible for the unprecedented market growth of wireless communication. However, for an improved design robustness, the digital approach is preferred, while analog IC design is becoming increasingly difficult, as the available voltage headroom is constantly shrinking. Therefore, digital intensive solutions of traditionally analog components are needed. Moreover, a digital intensive approach provides additional benefits in terms of improved reconfigurability and programmability, better testability, lower variability, optimized power consumption and area, higher degree of integration, and straightforward use of automated Computer-Aided Design (CAD) tools. The above reasons are of imperative importance for mobile wireless communication, where especially low cost, small area and low power designs are mandatory.

Traditionally, the Radio Frequency (RF) functions for wireless communication systems have been realized with analog intensive circuitry. Porting such analog functions to the digital domain, however, is not a simple operation. While the functionality of the system must be improved (or, at least, remain the same), novel problems may arise; nevertheless, some digital intensive RF solutions have already been demonstrated. An important and acclaimed exam-

ple is the Digital Phase Locked Loop (DPLL) [31] [32]. The DPLL approach has become very attractive in recent years, as it is capable of drawing much benefit from the downscaling of CMOS processes, which is not the case for the traditional analog Phase Locked Loop (PLL). In a DPLL, analog building blocks are either replaced by purely digital counterparts, such as the Digital Loop Filter (DLF), or by digitally controlled subsystems, such as the Digitally Controlled Oscillator (DCO). These replacements enable the designer to evade major analog design issues, including the non-linearity of the Charge Pump (CP), large passive components in analog Low Pass Filter (LPF) in the PLL loop, current leakage in the LPF capacitor, and the various problems deriving from a low supply voltage, while, on the other side, they bring forth the typical digital IC advantages in terms of high integration level, programmability, and flexibility, as already mentioned.

Although several DPLLs have displayed a superb performance [27] [33–39], there is still a number of aspects where better techniques and design enhancements are required. Two main issues are phase noise and spurious tones (spurs) in the spectrum of the DPLL output, where a high phase noise may cause reciprocal mixing in the receiver side, which occurs when the noise on the Local Oscillator (LO) (itself derived from the DPLL output) in the radio receiver joins forces with an incoming strong disturbing signal, effectively swamping a much lower desired signal. High spurs, on the other hand, may cause Intermodulation Distortion (IMD). Furthermore, both phase noise and close-in spurs corrupt the signal-to-noise ratio of both received and transmitted signals. A third aspect is that DPLL architectures still require high levels of power consumption and large design areas, which should be both reduced to achieve long operation times and low cost. Finally, DPLLs have, to a large extent, been employed in narrowband wireless systems. With the expected requirements of wideband systems as wireless communication evolves, wideband DPLLs (and, therefore, wideband DCOs) are badly needed.

The goal of this research work has been to find and test techniques for improving different properties of the DPLL at both the architectural and the building-block level.

1.2 RESEARCH CONTRIBUTION

In the course of the research work presented in this thesis, three circuits have been designed in two different CMOS processes, achieving the following results:

1. A DCO characterized by a reconfigurable active core with a wide tuning range, targeted for 2.8-5.8 GHz applications. In this work:
    - We demonstrate that a 28 nm Ultra-Thin Body and Buried Oxide

Fully Depleted Silicon on Insulator (UTBB FD-SOI) CMOS process makes it possible to realize a compact one-octave DCO based on a reconfigurable class-B active core and a single 8-shaped tank inductor, with a very good phase noise and Figure-of-Merit (FOM) performance, even though the UTBB FD-SOI process is optimized for purely low-power digital applications.

- We demonstrate that the UTBB FD-SOI CMOS process is instrumental to achieve a tuning range in excess of one octave at low power consumption
- Compared to ultra wide Tuning Range (TR) DCOs based on transformers or multiple inductors, this DCO is preferred for its comparatively easy and area-efficient design.
- The DCO adopts a re-configurable active core to save power at the lower oscillation frequencies, and to enable a trade-off between power consumption and phase noise at all frequencies.
- Interference caused by the magnetic coupling to and from the DCO inductor is greatly attenuated by resorting to an inductor in the shape of an 8. Simulations of the magnetic coupling between an 8-shaped inductor and a reference inductor show a magnetic coupling reduction as high as 44 dB, depending also on size, orientation, and shape of the interacting inductors.
- The DCO has a FOM of 186–189 dBc/Hz, depending on the oscillation frequency and the configuration of the oscillator core.

2. A DPLL based on a Time to Digital Converter (TDC), targeted for Long Term Evolution-Advanced (LTE-A) applications. The DPLL has a wide tuning range and uses a noise shaping 2D Gated-Vernier TDC (GVTDC) with 5.2 ps of resolution. This contribution presents:

   - A wide bandwidth DPLL for LTE-A bands 33–38 that leverages a 2D GVTDC, which greatly improves the DPLL in-band phase noise by both Vernier and noise shaping techniques, while having a full period capture range. The quantization noise shaping of the TDC greatly improves the in-band phase noise. At the same time, the 2D TDC makes the DPLL able to process large phase errors almost without any deterioration on latency time.
   - A high FOM class-D DCO with a fine tuning step of ~ 4 kHz, which pushes the quantization of discrete tuning well below the oscillator phase noise, is used.

- A quantization noise cancellation based on a Least Mean Square (LMS) algorithm to cancel the $\Delta\Sigma$ quantization noise is implemented.
- The DPLL achieves a very good simulated phase noise of -110 dBc/Hz in-band, and of -140 dBc/Hz at 10 MHz offset, with carrier frequency of 3.5 GHz and 1 MHz DPLL bandwidth.

3. A wideband Digital-to-Time Converter (DTC) based DPLL operating from 2.8 GHz to 3.8 GHz, with an on-chip 40 MHz reference crystal oscillator is presented. In this work:
   - We find the first published measurements on a DPLL employing a class-D DCO.
   - The DPLL displays an excellent behavior in terms of in-band fractional spurs, which are consistently below -65 dBc across the tuning range, thanks to a number of digital correction algorithms running in the background.
   - The simplified Frequency Acquisition Controller (FAC) proposed is wholly digital, requiring no additional analog blocks (e.g., coarse TDCs and RF counters) used in other DPLL designs. A fast and reliable frequency acquisition (lasting 160 μs at most) is achieved, despite the limited capture range of the Bang-Bang Phase Detector (BBPD) used.
   - The measured DPLL has a very good in-band phase noise of -102 dBc/Hz at 100 kHz offset.

Simulation and measurement results have been successfully published by the author in three journal articles and two conference papers. He is the first author in four of these publications.

1.3 THESIS OUTLINE

This thesis is organized into seven chapters as follows:

Chapter 1 presents the motivation and the outline of this work.

Chapter 2 provides an overview of the general aspects and different architectures for wireless frequency synthesis techniques.

Chapter 3 introduces basic background concepts for the DPLL architectures employed in this thesis.

Chapter 4 gives the fundamental design principles of the DCO, focusing on different ways of implementing fine tuning. Digital frequency quantization and oscillator pulling are also analyzed.

Chapter 5 focuses on the design principles for TDCs and DTCs, exploring several popular architectures.

Chapter 6 discusses the fabricated circuit prototypes, with simulations and experimental results.

Chapter 7 includes a brief conclusion.

2

Frequency Synthesizer Overview

2.1 INTRODUCTION

The term frequency synthesizer refers to a category of systems whose objective is to generate a set of stable frequencies. From communication systems to digital circuit applications, from clock and data recovery to modulation and waveform generation, frequency synthesizer is an indispensable item in almost every IC, either wireless or wireline. In general, frequency synthesizers are devices that take one reference frequency (f_{ref}), and generate a multiple of output frequencies ($f_{out,min} - f_{out,max}$). Mostly, a crystal oscillator is employed for the reference frequency, due to its high stability and high spectral purity at a precise frequency.

In wireless communication systems, the frequency synthesizer is commonly serving as an LO source, where it is used as a reference oscillator for frequency translation and channel selection in a variety of up-conversion and down-conversion schemes for different transceiver architectures. Hence, it is one of the most critical modules, as it has a direct critical impact on the performance of the whole transceiver. Therefore, new designs and techniques are usually developed in order to meet the stringent requirements outlined in wireless communication standards in terms of spectral purity, frequency range, etc. along with the stringent specifications of low power consumption and low cost.

This chapter presents a brief discussion of frequency synthesis applications and highlights the high importance of frequency synthesizers for wireless communication systems. Meanwhile, some background into the types and performance metrics of frequency synthesis techniques are introduced, with emphasis on critical performance parameters.

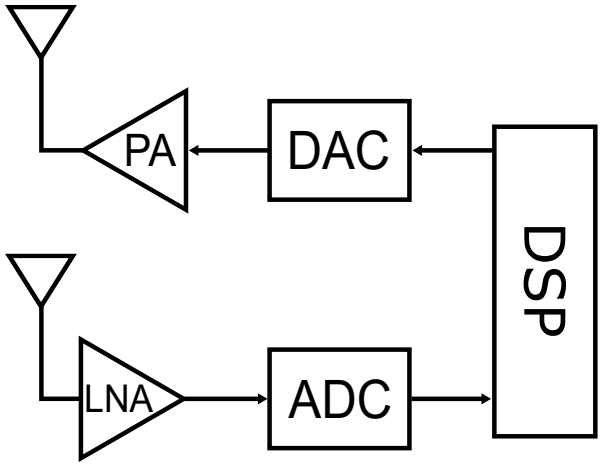


Figure 2.1 Ideal transceiver architecture envisioned in [1].

2.2 FREQUENCY SYNTHESIZERS IN TRANSCEIVERS

A key device in any wireless communication system is the radio transceiver (amalgamation of Transmitter (Tx) and Receiver (Rx)). It is a building block that is responsible for transmitting and receiving data. Figure 2.1 shows the ideal transceiver concept envisioned in [1]. In this configuration, no frequency conversion is needed, as the Analog to Digital Converter (ADC) and Digital to Analog Converter (DAC) already operate at RF. It is a massively digitized transceiver concept that introduces a very high degree of re-configurability and programmability, since most of the work is accomplished in the digital domain. Therefore, this architecture allows for a maximum degree of flexibility through an increase in software capability. Unfortunately, this architecture is not practical in high frequency applications, as it requires unrealistic requirements for ADC and DAC in terms of very high sampling rate and dynamic range, with higher power consumption and higher cost. Furthermore, it also needs a high speed Digital Signal Processor (DSP) to have the ability to process high sampling rate signals, which comes with larger power consumption and higher cost. Thus, this type of transceiver approach is not suitable for high frequency applications.

To alleviate the previous issues, two well-known transceiver architectures are employed, which typically are classified according to the location of the Intermediate Frequency (IF) involved between the baseband and RF, whether it is a direct-conversion (zero-IF) from the baseband to the RF and vice versa (homodyne transceiver), or it is inserted between the baseband and the RF (superheterodyne transceiver).

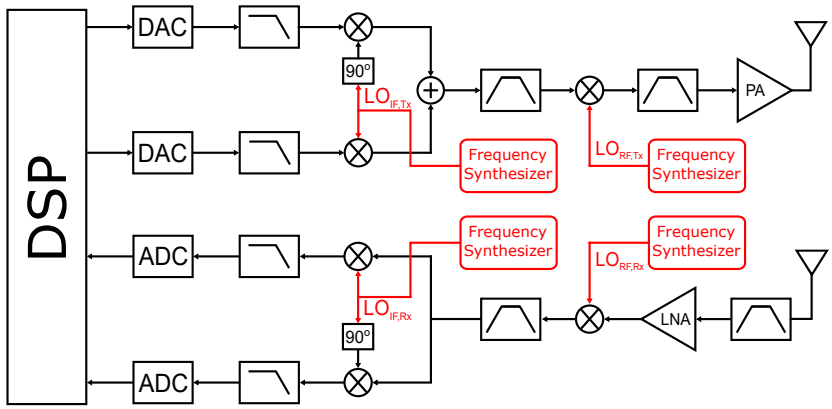


Figure 2.2 Superheterodyne transceiver architecture.

2.2.1 SUPERHETERODYNE TRANSCEIVER

Figure 2.2 shows the superheterodyne transceiver architecture. It is characterized by two steps frequency conversion: down-conversion from RF to IF and then to baseband, and the contrary in up-conversion, from baseband to IF then to RF. In the transmitter side, the digital baseband signal is passed through DACs to generate the appropriate analog baseband signals. These signals are then passed through LPFs to reject any high frequency aliasing components caused by the DACs. Thereafter, these signals are mixed up with $LO_{IF,Tx}$ and up-converted to the IF region, where they are passed through a Band Pass Filter (BPF) to further suppress any unwanted signals. The filtered IF signals are combined together and up-converted to the RF region by $LO_{RF,Tx}$, where it is filtered again and then amplified by a Power Amplifier (PA) and fed to the antenna.

Likewise, in the receiver side, the RF signal from the antenna is first filtered by an RF BPF to attenuate any undesired out-of-band blockers. The signal is then amplified by a Low Noise Amplifier (LNA), which amplifies the signal with relatively low noise contribution. The amplified signal is down-converted firstly to IF by $LO_{RF,Rx}$, then to baseband by $LO_{IF,Rx}$, where it is converted again to the digital domain through ADCs, where additional signal processing is performed. In general, four frequency synthesizers are required: two for the Tx and the other two for the Rx if Frequency Division Duplex (FDD) scheme is adopted, while two frequency synthesizers can be used for both Tx and Rx in case of Time Division Duplex (TDD) scheme.

Superheterodyne transceiver, especially the receiver side, is a very popular architecture in wireless communication systems for its ability to deliver very good performance, and it was the main choice in wireless systems for decades.

Two main advantages single out superheterodyne architectures over other architectures. The first advantage is the low impact of LO leakage, as a result of using two-step frequency conversion. The second one is the high capability of the receiver to suppress undesired signals, which increases the receiver dynamic range, sensitivity and selectivity. However, superheterodyne receivers also exhibit significant drawbacks. One of the biggest cons is the need of high selectivity BPFs to adequately filter out unwanted image and interference signals, which makes these filters hard to be integrated. Discrete components are used instead. Consequently, more discrete components are directly translated to higher cost, higher power consumption, larger area and higher architecture complexity.

2.2.2 HOMODYNE TRANSCEIVER

The homodyne transceiver architecture is shown in Figure 2.3. This architecture is characterized by a one-step frequency translation: either up-conversion directly from baseband to RF on the Tx side, or down-conversion from RF to baseband on the Rx side. Hence, this architecture is also termed as a direct-conversion or a zero-IF transceiver. The homodyne architecture offers a higher degree of integrability, where high cost IF filters are eliminated, since no image problem exists, and then the cost and size of the overall transceiver are consequently reduced. Moreover, it consumes less power than the superheterodyne transceiver, due to only one frequency conversion is needed.

On the other hand, the performance of a homodyne transceiver is limited

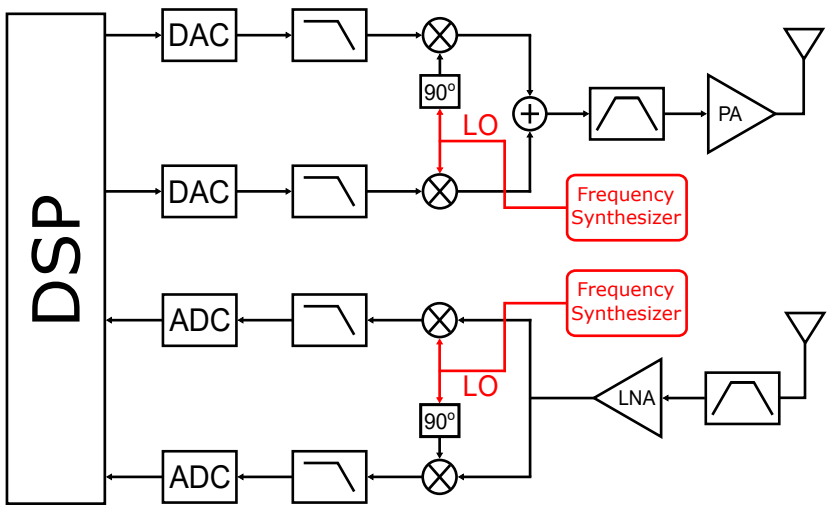


Figure 2.3 Homodyne transceiver architecture.

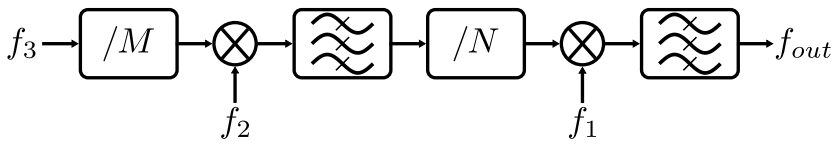


Figure 2.4 Direct analog frequency synthesizer [2].

by two main aspects. Firstly, it requires very high degree of matching between the quadrature paths, as any small mismatch in gain or phase could critically corrupt the performance. Secondly, LO leakage to the mixer has a significant impact and could result in self-mixing problems, which causes a time-varying DC offset at the output of the mixer.

2.3 FREQUENCY SYNTHESIZER ARCHITECTURES

There are many different approaches for implementing a frequency synthesizer [40–42]. Commonly, a frequency synthesizer can be categorized into four main flavors: Direct Analog Frequency Synthesizer (DAFS), Direct Digital Frequency Synthesizer (DDFS), indirect or PLL-based frequency synthesizer, and hybrid frequency synthesizer. The synthesizer performance depends heavily on each particular scheme. Typically, among all the previous schemes, the indirect frequency synthesizer is the most commonly used approach in wireless communication systems because of its high performance, as it has the possibility to achieve high frequency generation, high spectral purity and low power consumption. In the following sub-sections, the above frequency synthesis techniques are explored and their advantages and disadvantages are investigated.

2.3.1 DIRECT ANALOG FREQUENCY SYNTHESIZER

The DAFS approach is shown in Figure 2.4. As indicated by its name, the signal is generated directly employing a frequency multiplication, mixing and division, from a single fixed reference frequency [2]. As explained in the figure, the number of mixing and division stages depends on the target output frequency and the required fine resolution. The generated output frequency can be expressed as

$$f_{out} = f_1 + \frac{f_2}{N} + \frac{f_3}{MN} \tag{2.1}$$

The key advantages of the DAFS approach are the extremely fast switching speed and excellent phase noise performance, as the latter depends mainly on the reference source and can potentially be very low. Unfortunately, seri-

ous problems associated with DAFS limit its use in wireless communication systems. The first major disadvantage is the cross coupling between cascaded stages, which degrades spectral purity. Careful layout with perfect isolation between individual components would be needed to alleviate this problem. Also, DAFS is characterized as a hardware intensive topology. Therefore, for stringent specifications in terms of small frequency step and wide coverage, DAFS becomes very expensive and power hungry topology, and ultimately unfeasible.

2.3.2 DIRECT DIGITAL FREQUENCY SYNTHESIZER

The DDFS approach is very attractive for the reasons of fast frequency generation and very fine frequency resolution. Moreover, it can also be easily integrated, as no external components are needed. Figure 2.5 shows the block diagram of a DDFS. A DDFS utilizes a digital phase accumulator and a sine wave look-up-table to digitally create the desired output waveform in digital domain. Thereafter, a DAC is used to convert the digital waveform from the digital domain to the analog domain. High frequency spurious tones at the DAC output are filtered out by a LPF. As a result of using a lock-up-table, this synthesizer is also known as a table-look-up synthesizer. Furthermore, the combination of digital phase accumulator and sine wave look-up-table is termed Numerically Controlled Oscillator (NCO) [40].

In this approach, the minimum achievable frequency step is determined by the capacity of the digital phase accumulator employed. Therefore, for an L bit accumulator and a certain *Frequency Control Word (FCW)*, the output frequency of the DDFS in terms of the clock frequency f_{clk} can be calculated as [40]

$$f_{out} = \frac{FCW}{2^L} f_{clk} \tag{2.2}$$

Therefore, the range of the output frequency is from $f_{clk}/2^L$ to f_{clk}, since FCW can take any integer value between 1 and 2^L.

However, the following major drawbacks limit the use of this topology in

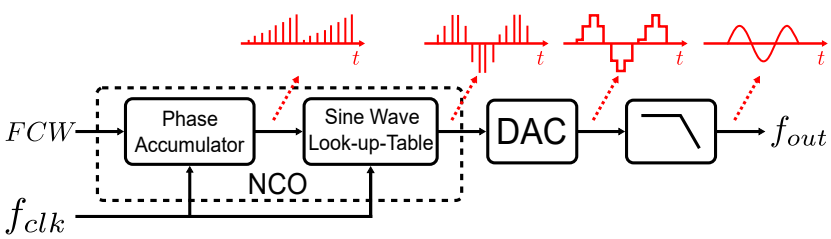


Figure 2.5 Direct digital frequency synthesizer [3].

wireless communication systems, especially for mobile communications. The first reason is the excessive power consumption at high frequencies, as the system has to be clocked with a frequency at least twice the output frequency. In addition, implementing a DAC and a LPF at high frequencies adds a significant amount of power consumption to the total power. Secondly, due to DAC limited resolution and non-linearity issues, the DDFS output spectrum usually suffers from high spurious tones, which are not completely removed by the LPF. These spurious tones degrade the spectral purity performance.

2.3.3 INDIRECT FREQUENCY SYNTHESIZER

The indirect frequency synthesizer, also called PLL-based frequency synthesizer, is the most common, popular and widely used approach in communication systems. Basically, a PLL is a control system with negative feedback producing an output frequency with a certain relation to a reference frequency. Depending on the possible ratios between the output frequency and the reference frequency, PLLs are categorized into two groups: integer-N and fractional-N PLLs. Essentially, fractional-N PLLs are a generalized version of integer-N PLLs. In most wireless applications, an integer-N PLL is not capable of meeting the targeted overall performance; hence, a fractional-N PLL is typically employed for frequency synthesis.

Analog PLL-based frequency synthesizers typically adopt CP architectures. A block diagram of a conventional CP-PLL is depicted in Figure 2.6. The out-

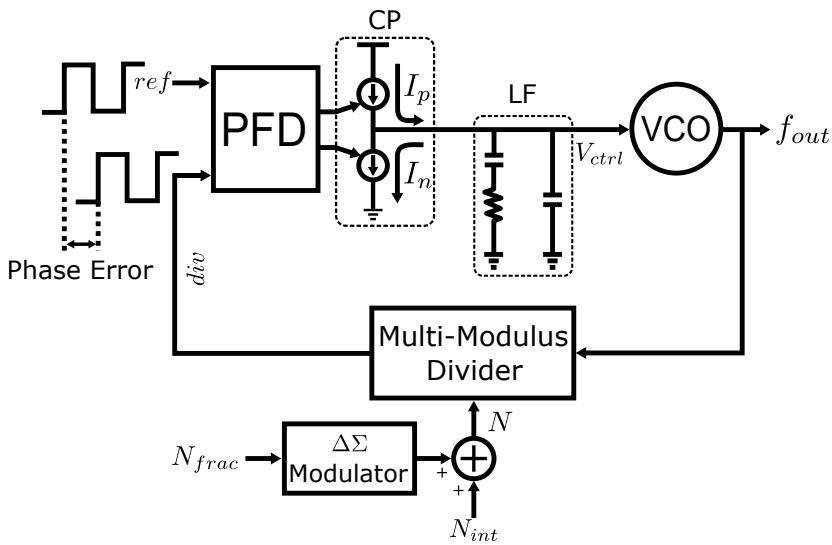


Figure 2.6 Fractional-N CP-PLL.

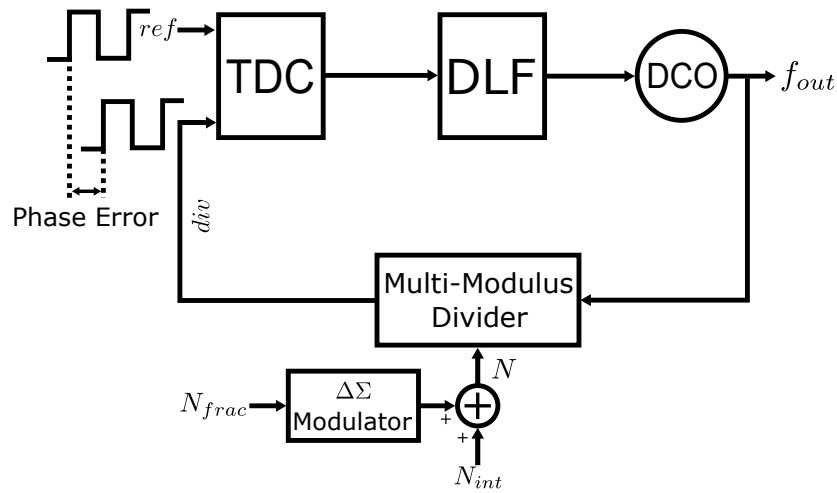


Figure 2.7 Fractional-N DPLL.

put frequency, f_{out}, is generated by the Voltage Controlled Oscillator (VCO), while the reference frequency f_{ref}, is generated by a low-phase-noise crystal oscillator. In the feedback path, the VCO output is divided by a Multi-Modulus Divider (MMD) to produce the frequency-divided signal div. A $\Delta\Sigma$ modulator is used to dynamically vary the division ratio to achieve an effective fractional division ratio. The Phase Frequency Detector (PFD) detects the difference in phase between the reference signal ref, and the div signal in terms of the time difference between their respective closest rising edges. The PFD, thereafter, generates a series of pulses: either "up" or "down" pulses, with a width proportional to the measured time difference. The CP scales the signal generated from the PFD and pumps a current with a proportional duty cycle either into (I_p) or out (I_n) of the Loop Filter (LF). The LF is typically a LPF which converts this current into a tuning voltage for the VCO, while at the same time suppressing noise and glitches produced by the CP non-ideal behavior in order to prevent them from modulating the VCO, causing excessive noise and spurious tones in the VCO output spectrum. The VCO tuning voltage V_{ctrl} increases or decreases the VCO output frequency. As a result, the VCO steady-state output frequency is equal to

$$f_{out} = (N_{int} + N_{frac}) f_{ref} \tag{2.3}$$

where N_{int} and N_{frac} are the integer and fractional parts of the division ratio, respectively.

Fractional-N DPLL-based frequency synthesizers often employ a similar architecture as conventional fractional-N analog PLL-based frequency synthe-

sizers. Such architectures can be realized in several variations to meet the specific requirement of different applications, which differ in performance and complexity [27][31][33][36][37][39][43]. In general, however, the architecture of fractional-N analog PLLs are moved to the digital domain by replacing the PFD with a TDC, the analog LF with a DLF, and the VCO with a DCO, as illustrated in Figure 2.7.

2.3.4 HYBRID FREQUENCY SYNTHESIZER

A Hybrid frequency synthesizer is constructed by combining two or more structures together, in order to take advantage of the special features that distinguish each technique and minimize the drawbacks. Typically, it is a combination between DDFS and PLL [41], as shown in Figure 2.8. In the DDFS-PLL hybrid structure, the DDFS generates a narrow-band instantaneously tunable low frequency signal, used as the PLL reference signal. The PLL up-converts that reference signal to the targeted frequency.

The DDFS-PLL hybrid structure takes the advantages of the very fine frequency step and the fast switching time introduced by the DDFS to enhance the tunability of the whole system, which is difficult to achieve using the PLL structure alone.

2.4 PERFORMANCE METRICS OF THE FREQUENCY SYNTHESIZER

The frequency synthesizer is a key building block in every transceiver. It needs to provide high quality LO signals with stringent requirements to perform frequency translation, either down-conversion or up-conversion, where the performance of the LO frequency generation system directly affects the performance of the whole transceiver.

In general, the frequency synthesizer is characterized by some main characteristics. Therefore the frequency synthesizers are usually selected and ranked according to the following set of performance metrics.

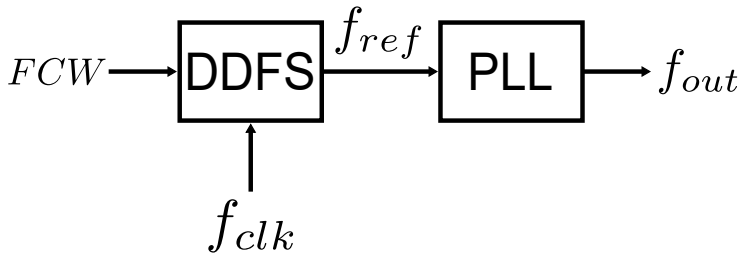


Figure 2.8 The DDFS-PLL hybrid structure.

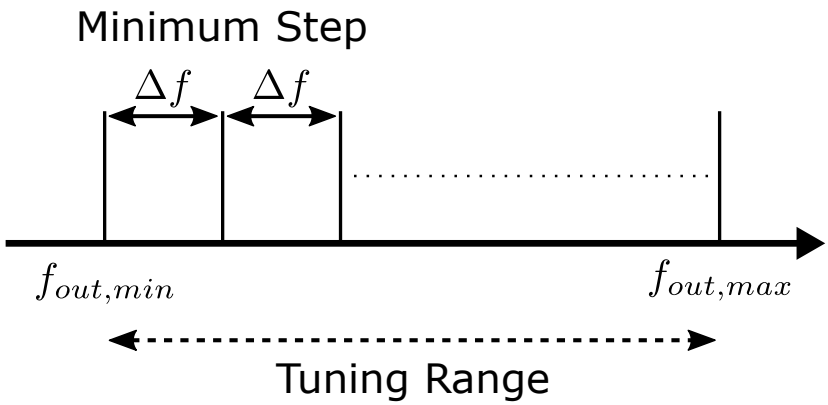


Figure 2.9 Frequency tuning range and frequency resolution.

2.4.1 FREQUENCY TUNING RANGE AND FREQUENCY RESOLUTION

The frequency synthesizer should be capable of producing an accurate carrier frequency that can be well tuned within a specified range, to cover all of the frequency bands specified for a given standard. This specified range is termed as a frequency synthesizer tuning range, as shown in Figure 2.9. In order to ease up frequency planning in presence of an unprecedented band proliferation, it is desirable that as many frequencies as possible are synthesized by a single frequency synthesizer. Such tuning is typically determined by the tuning range of its employed oscillator, and by the frequency multiplication ratio.

Besides tuning range, the synthesizer must be capable of producing a carrier frequency with high frequency resolution, or minimum frequency tuning step. Resolution, which is defined as the minimum possible value achieved via tuning, is usually specified according to the channel spacing for a given standard (see Figure 2.9).

2.4.2 SPECTRAL PURITY

Practical frequency synthesizers are not able to deliver ideal LO signals due to devices noise and external interferences. The quality of their output is typically evaluated depending on two critical performance metrics, i.e. phase noise and spurious tones. Therefore, it is crucial to investigate the impact of these on communication systems performance.

2.4.2.1 PHASE NOISE

An ideal oscillator generates a perfectly periodic output in the time domain, which corresponds to a single tone in the frequency domain at the desired

oscillation frequency ω_c. In reality, however, due to noise, the oscillation signal is phase and amplitude modulated by random or periodic fluctuations. The random fluctuations result in phase noise and amplitude noise, and the output spectrum exhibits sidebands close to ω_c rather than a single tone, as shown in Figure 2.10. Amplitude noise, on the other hand, is rejected by the oscillator itself close to ω_c. The output signal for an ideal and noisy oscillator can be respectively expressed as

$$V_{out,ideal}(t) = A\sin(\omega_c t) \tag{2.4}$$

$$V_{out}(t) = A\sin[\omega_c t + \phi(t)] \tag{2.5}$$

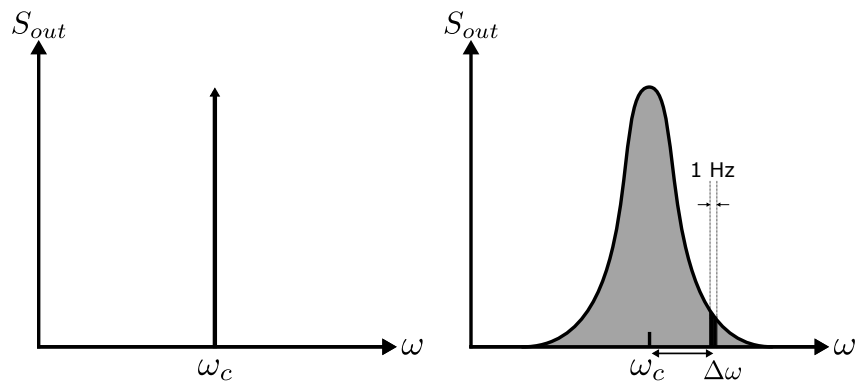
where A is the amplitude of the signal, while $\phi(t)$ represents the random phase fluctuation. Supposing that the random phase fluctuation in (2.5) takes the form of $\phi(t) = \Delta\phi\sin(\Delta\omega t)$, where $\Delta\phi$ is the maximum phase deviation, (2.5) can be rewritten as

$$V_{out}(t) = A\sin[\omega_c t + \Delta\phi\sin(\Delta\omega t)] \tag{2.6}$$

Typically, $\Delta\phi << 1$, hence the final form of (2.6) becomes

$$V_{out}(t) = A\sin(\omega_c t) + \frac{A\Delta\phi}{2}\{\sin[(\omega_c + \Delta\omega)t] - \sin[(\omega_c - \Delta\omega)t]\} \tag{2.7}$$

Equation (2.7) shows that the output spectrum of the oscillator is a combination of a strong tone at ω_c plus a narrow-band Frequency Modulation (FM)



(a) Ideal Output Spectrum. (b) Real output spectrum.

Figure 2.10 Output Spectrum of both an ideal and noisy oscillator.

signal with a modulation index $\Delta\phi$. This FM modulation generates two small tones at $\omega_c + \Delta\omega$ and $\omega_c - \Delta\omega$. Therefore, the output Power Spectral Density (PSD) is

$$S_{out}(\omega) = \frac{A^2}{2}[\delta(\omega-\omega_c) + \frac{1}{2}S_\phi(\omega-\omega_c) + \frac{1}{2}S_\phi(\omega_c-\omega)] \tag{2.8}$$

where

$$S_\phi(\omega) = \frac{\Delta\phi^2}{2}\delta(\omega-\Delta\omega) \tag{2.9}$$

Equation 2.8 illustrates the skirt shape of the oscillator spectrum, where the phase noise spectrum can be seen as a sum of sines.

The phase noise is quantified by normalizing the noise power in a unit bandwidth at a certain offset frequency $\Delta\omega$ from ω_c with respect to the total carrier power. It can be expressed as a single sided PSD with units of dBc/Hz, i.e. decibels relative to the carrier per Hertz

$$L(\Delta\omega) = 10\log(\frac{\text{Noise Power in a 1 Hz bandwidth at } \omega_c + \Delta\omega}{\text{Total Carier Power}}) \tag{2.10}$$

Figure 2.11 shows a typical oscillator phase noise spectrum. Three slope regions can be recognized: $1/\omega^3$, $1/\omega^2$, and a flat region. The $1/f$ flicker noise generated from electronic devices is up-converted to the $1/\omega^3$ region, while the $1/\omega^2$ region is caused by white noise affecting the oscillation period, and

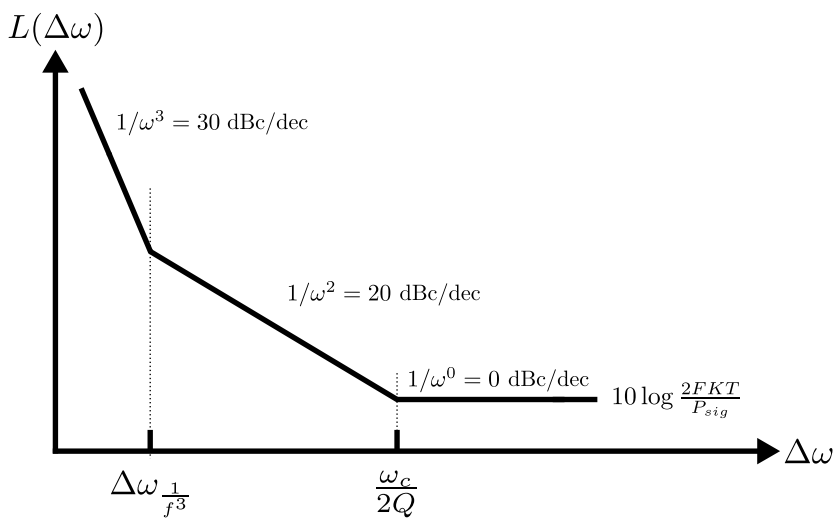


Figure 2.11 Typical oscillator phase noise.

it is also known as the thermal noise region [41]. The flat region is caused by thermal noise from outside the oscillator itself, such as output buffers. Lesson's formula [44] can be used to calculate the phase noise at a certain frequency offset as

$$L(\Delta\omega) = 10\log[\frac{2FKT}{P_{sig}}\{1+(\frac{\omega_c}{2Q\Delta\omega})^2\}(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|})] \tag{2.11}$$

where F, k, T, P_{sig}, Q and $\Delta\omega_{1/f^3}$ are the noise figure, Boltzmann constant, temperature, quality factor of the oscillator tank, and corner frequency of the $1/\omega^3$ phase noise region, respectively.

In addition, by integrating the phase noise over a certain range of offset frequencies, the integrated phase noise can be obtained, expressed as

$$L_{int} = 2\int_{\Delta\omega_1}^{\Delta\omega_2} L(\Delta\omega)\, d\omega \tag{2.12}$$

in units of dBc. The factor 2 in (2.12) takes into account the double sideband of the phase noise. Another way used to measure the impact of phase noise is

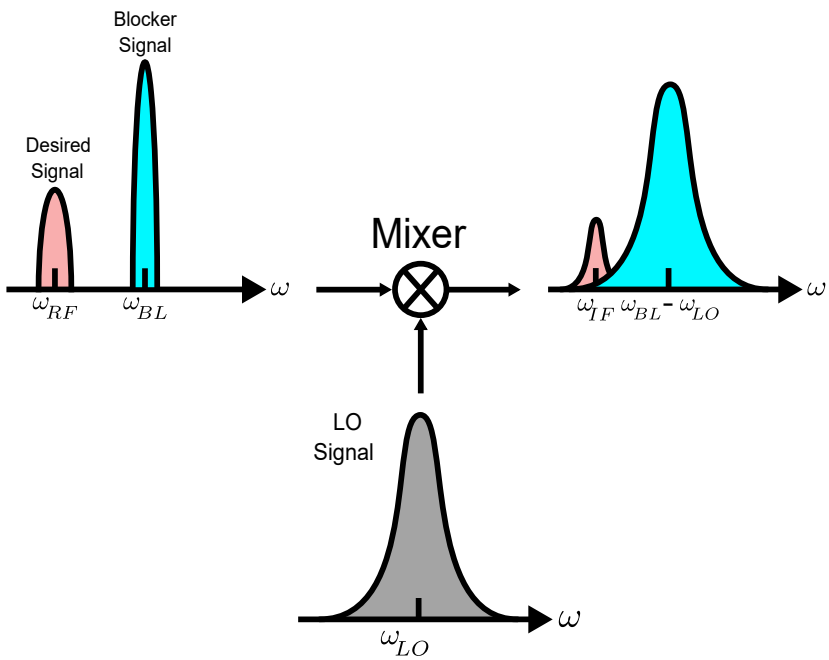


Figure 2.12 Effect of LO phase noise on RF receiver.

the rms phase error, given by [3] [45]

$$\sigma_{\phi} = \frac{180}{\pi}\sqrt{L_{int}} \tag{2.13}$$

in units of degree. From 2.13, the rms jitter in seconds can be expressed as [3]

$$\sigma_{jitter} = \frac{T_c \sigma_{\phi}}{360} \tag{2.14}$$

where T_c is the carrier period. The integrated phase noise, rms phase error and rms jitter take into account both phase noise and spurious tones.

Low phase noise is very important for high quality reception and transmission. Figure 2.12 explains the phase noise influence on RF transceivers. On the receiver side, when the RF signal is down-converted to the desired IF channel, and a large nearby blocker is also present, the frequency translation results in a down-converted blocker with a noise skirt that corrupts the desired IF signal. This phenomenon is called "reciprocal mixing" [46].

2.4.2.2 SPURIOUS TONES

Apart from phase noise, the spectrum of an oscillator may also suffer from discrete spurious tones or spurs. Spurs are undesired frequency components in

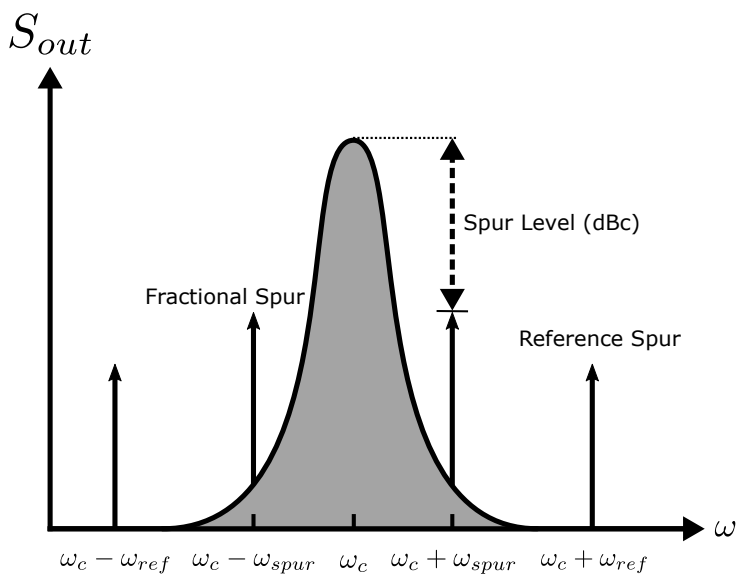


Figure 2.13 LO spectrum with spurs.

the synthesizer output spectrum, which appear at certain discrete offset frequencies from the carrier. They are caused by deterministic periodic fluctuations in phase that modulates the oscillator, causing sideband tones around the carrier. Spurs are characterized in a way similar to the phase noise by normalizing their power level with respect to the carrier, in units of dBc [45]

$$\text{Spur level} = 10\log(\frac{\text{Spur power}}{\text{Carier Power}}) \tag{2.15}$$

There are two types of spurs:

- **Reference Spurs:** They typically appear at frequency offsets from the carrier equal to the reference frequency used, due for example to mismatch in the CP in CP-PLLs.

- **Fractional Spurs:** If a fractional-N frequency synthesizer is used, another type of spurs, called fractional spurs, arise. This type of spurs comes as a result of the quantization noise from the dithering action of the $\Delta\Sigma$ modulator used in the frequency divider. This quantization noise modulates the oscillator generating fractional spurs. Fractional spurs are more critical than reference spurs, as they may appear very close to the carrier, where the LF can not suppress them.

Figure 2.13 illustrates the reference and fractional spurs.

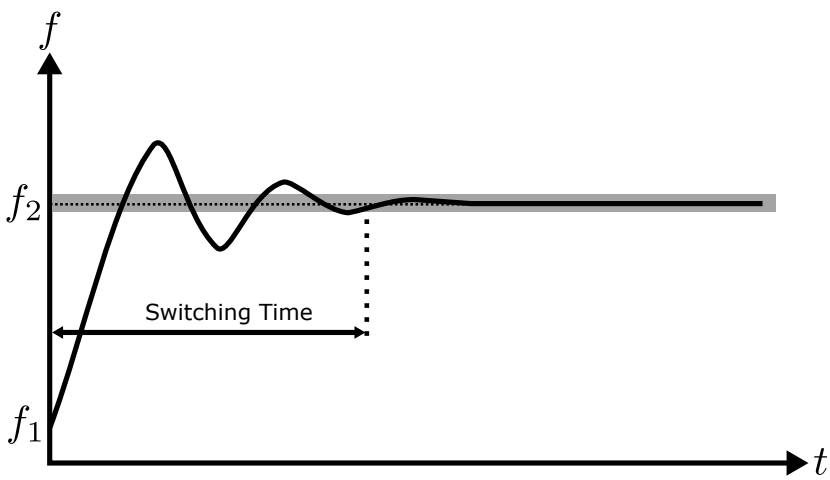


Figure 2.14 Settling time example of a frequency synthesizer [3].

2.4.3 SWITCHING TIME

Switching time, also called "locking time" or "settling time", refers the settling time after channel switch. In other words, it is the time needed for a frequency synthesizer to settle to a new output frequency after the frequency multiplication ratio is changed. This can be crucial for some applications requiring fast switching, such as frequency-hopping spread spectrum. This is illustrated in Figure 2.14, where f_1 and f_2 represent the starting frequency and the new target frequency, respectively. The gray region around the target frequency f_2, specifies the required frequency accuracy, commonly stated in the targeted wireless standard.

2.4.4 POWER CONSUMPTION, SIZE AND PORTABILITY

- **Power Consumption:** It is always an important aspect, especially for portable devices, since it determines the battery life.
- **Size:** It is an important parameter for a successful mass production of the whole transceiver.
- **Portability:** It is very desirable to be able to easily transfer a design from a technology node to the next one.

3

DPLL Fundamentals

While the PLL-based frequency synthesizer approach is a key building block in almost all wireless and wireline transceivers, the design of analog PLLs is facing difficulties due to the downscaling trend in CMOS technology. In recent years, DPLLs have gained a huge popularity, replacing critical analog PLL functions, such as PFD, CP and analog LF, with their digital counterparts. This enables the deployment of extremely powerful digital algorithms implemented in modern nm CMOS processes at low cost.

This chapter contains an overview of DPLL-based frequency synthesizers, which illustrates the principal behavior, system-level properties, and design challenges of representative architectures that are adopted as the base architectures throughout the author's design work. It starts by categorizing the different types of the DPLL, after which fundamental concepts are investigated using *z*-domain and *s*-domain models. The forthcoming analysis has partially been presented in [4][35][41][47–56], but the overall analysis and simulations are the author's own work.

3.1 DPLL ARCHITECTURES

Essentially, DPLLs can be classified into three different classes:

- The first type is the original DPLL (often referred to as "phase-domain" or divider-less DPLL [57]), where the TDC is driven directly by the DCO output signal.

- The second type is the TDC-based DPLL [33]. In this type, the TDC works as a phase frequency detector, where it essentially replaces the PFD and CP of the traditional CP-PLL. Thus, the TDC measures directly

the phase error between the DCO divided signal and the reference signal.

- The third type is the Bang-Bang (BB)-based DPLL. It is considered as a special case of the above type, where a BBPD aided by a DTC is employed, instead of the TDC [35].

In this thesis, only the latter two types have been considered, therefore the forthcoming analysis focuses only on these.

3.2 TDC-BASED DPLL

The TDC-based DPLL contains four main building blocks: a TDC, a DLF, an MMD and a DCO, as shown in Figure 3.1. The feedback mechanism guaranties that the output phase of the divided signal $div[k]$ is in phase-lock with a periodic reference signal $ref[k]$, which is the input of the DPLL. Thus, the phase error between $div[k]$ and $ref[k]$ is measured and digitized by the TDC. A DLF attenuates the TDC output noise and distortion and generates the DCO tuning word $tw[k]$. The resulting $tw[k]$ from the DLF controls the output frequency of the DCO. In steady state, i.e., when phase-lock is achieved, the frequency of $div[k]$ matches the frequency of $ref[k]$, and the output frequency of the DCO settles to the target frequency with a certain accuracy and noise level. In case of fractional operations, the division ratio N is dithered, such that its average matches the required fractional number. Typically, a Multi-stAge noise SHaping (MASH) $\Delta\Sigma$ modulator is used to perform the dithering operation.

Two sources of quantization errors arise as a result of the conversion from

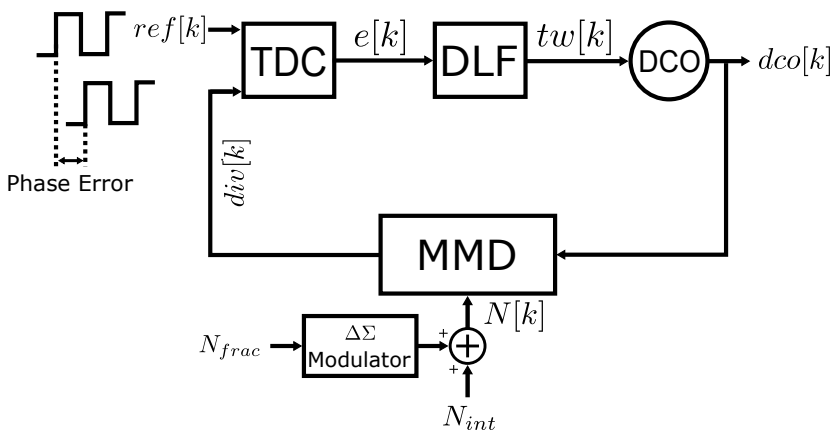
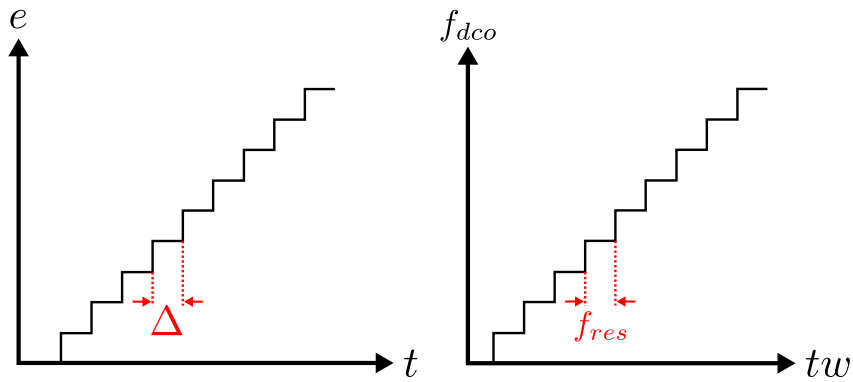


Figure 3.1 TDC-based DPLL basic block diagram.



(a) TDC ideal characteristic curve. (b) DCO ideal characteristic curve.

Figure 3.2 TDC and DCO ideal characteristic curves.

the analog to the digital domain and vice versa. The first one is related to the phase error conversion into a digital form by the TDC block, while the second source of quantization is coming from the DCO, as a result of its finite frequency resolution. The ideal conversion characteristics of both TDC and DCO are shown in Figure 3.2(a) and 3.2(b), respectively. Δ and f_{res} represent the resolution of the TDC and DCO, respectively.

Next, different circuit blocks of the TDC-based DPLL architecture are examined and modeled. After that, the overall transfer function for the TDC-based DPLL system is derived, followed by investigating the noise sources of the different parts, in order to evaluate the noise contribution of each part, and how they can be optimized.

3.2.1 DISCRETE AND CONTINUOUS-TIME MODELS

The DPLL is a discrete-time sampled system implemented with digital components, hence it can be described in the discrete-time domain using difference equations. Therefore, the z-transform is the most convenient method to evaluate and analyze the DPLL system. Next, difference equations and z-domain transfer functions for different circuit blocks of the DPLL are derived, followed by an evaluation of the overall transfer function in z-domain. Furthermore, the s-domain approximation is also derived.

3.2.1.1 DIGITALLY CONTROLLED OSCILLATOR

A DCO works as a digital-to-frequency converter, converting a digital input word $tw[k]$ into an oscillating signal with frequency $f_{dco}[k]$. The DCO can

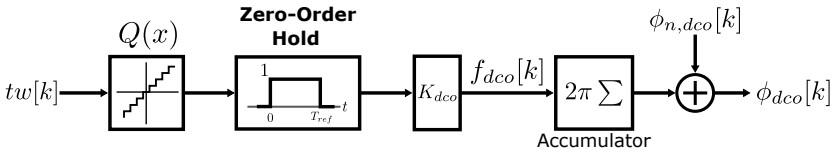


Figure 3.3 DCO discrete-time model.

be modeled as depicted in Figure 3.3. The discrete tuning is modeled by the staircase function $Q(x)$ with a unitary average gain, under the assumption that $tw[k]$ changes only in steps of one [55]. The minimum frequency change achieved by changing one Least Significant Bit (LSB) of $tw[k]$ is called DCO gain, K_{dco}, and has units of Hz/LSB. Therefore, the frequency granularity of the DCO is limited by K_{dco}. Neglecting noise and non-linearities, the ideal digital-to-frequency conversion of the DCO can be described as

$$f_{dco}[k] = f_r + K_{dco} tw[k] \tag{3.1}$$

where f_r is the DCO free running frequency. The phase of the DCO output can be expressed as the integral of the frequency, such that

$$\phi_{dco}(t) = \int_0^t \omega_{dco}(t)\, dt = 2\pi \int_0^t f_{dco}(t)\, dt \tag{3.2}$$

The DCO phase at a certain sampled time $t = kT_{ref}$ (where T_{ref} is the period of the reference signal used), corresponding to the k^{th} sampled value, can be derived in terms of its previous sampled value together with (3.2) [3], as

$$\phi_{dco}[k] = \phi_{dco}[k-1] + 2\pi \int_{(k-1)T_{ref}}^{kT_{ref}} f_{dco}(t)\, dt \tag{3.3}$$

At the sampling instants, the DCO is allowed to update its frequency, otherwise the frequency is kept constant between two consecutive sampling instants; in other words, a zero-order hold operation is performed, as shown in Figure 3.3. By applying the zero-order hold to (3.3), the finite integral on

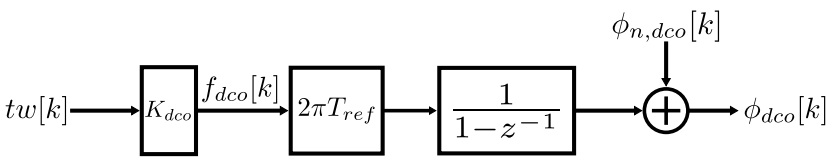


Figure 3.4 DCO z-domain simplified model.

the right-hand side of that equation becomes constant, equal to $2\pi T_{ref} f_{dco}[k]$. Hence, (3.3) becomes

$$\phi_{dco}[k] = \phi_{dco}[k-1] + 2\pi T_{ref} f_{dco}[k] \tag{3.4}$$

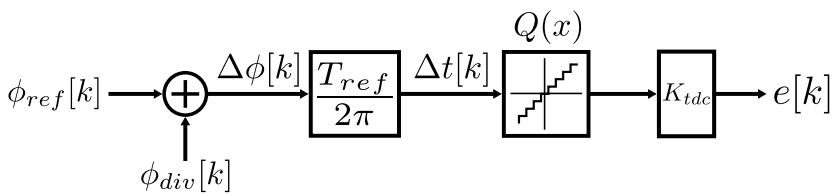
Finally, the corresponding z-transform is

$$\frac{\phi_{dco}(z)}{f_{dco}(z)} = 2\pi T_{ref} \frac{1}{1-z^{-1}} \tag{3.5}$$

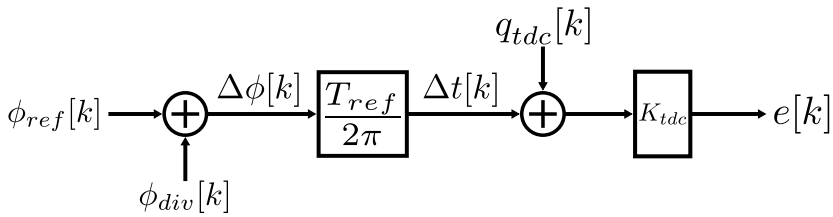
The function $Q(x)$ makes the DCO model in Figure 3.3 non-linear. To simplify the analysis, the $Q(x)$ quantization error is assumed to be a random sequences independent of its input [55]. Also, by assuming that the DCO is designed such that the quantization noise is well below the DCO inherent phase noise, which is possible to achieve in realistic implementations, the noise impact of the DCO quantization noise would be negligible, and the simplified linear model of Figure 3.4 results, where $\phi_{n,dco}[k]$ represents the DCO phase noise.

3.2.1.2 TIME TO DIGITAL CONVERTER

A TDC is modeled by a subtractor detecting the time error $\Delta t[k]$ between $ref[k]$ and $div[k]$, $\Delta t[k] = t_{ref}[k] - t_{div}[k]$, and multiplying it by a gain $K_{tdc} = 1/\Delta$. As in the DCO case, the TDC output also suffers from a quantization error, which



(a) TDC model.



(b) TDC simplified model.

Figure 3.5 TDC models.

is represented by the same function $Q(x)$ [55], as shown in Figure 3.5(a). This function also has a unitary average gain, with the assumption that $e[k]$ changes in steps of one.

In order to make the TDC model linear, the quantizer is replaced by an additive, white and uniformly distributed noise source with a variance of $\Delta^2/12$, and consequently a linear model can be achieved (see Figure 3.5(b)). Neglecting noise sources and non-linearities except the quantization noise $q_{tdc}[k]$, the relationship between the input and output of the TDC can be described as

$$e[k] = (\phi_{ref}[k] - \phi_{div}[k])\frac{K_{tdc}T_{ref}}{2\pi} = \Delta\phi[k]\frac{K_{tdc}T_{ref}}{2\pi} \tag{3.6}$$

Consequently, the corresponding z-transform transfer function is

$$\frac{e(z)}{\Delta\phi(z)} = \frac{K_{tdc}T_{ref}}{2\pi} \tag{3.7}$$

3.2.1.3 DIGITAL LOOP FILTER

The DLF is generally implemented as a LPF. The main role of the DLF is to suppress high-frequency noise components and prevent them from propagating from TDC output to DCO input. It can be implemented in many forms, depending on the performance requirements. Two examples are explained: type-I 1st-order DPLL and type-II 2nd-order DPLL, which can be used as a basis for the study of more advanced implementations.

- Type-I 1st-order DPLL employs only a proportional factor β as a DLF. Hence, there is no additional integrator in the loop except the oscillator. The difference equation of the DLF is simply

$$tw[k] = \beta e[k-D] \tag{3.8}$$

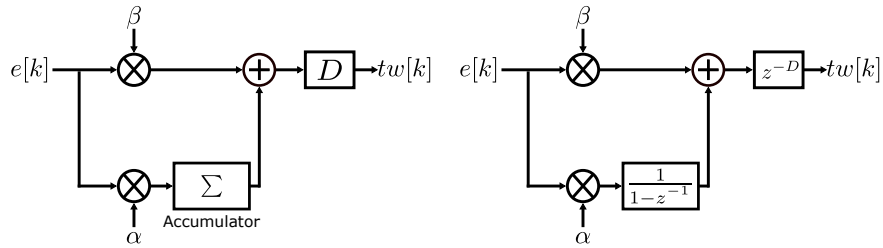
  where D is the latency (it can be 0,1,...). The corresponding z-transform is

$$tw(z) = \beta e(z)z^{-D} \tag{3.9}$$

  Although the above DPLL realization is remarkable in terms of lock time, it has the least noise attenuation among DPLL realizations.

- In a type-II 2nd-order DPLL, a Proportional-Integral (PI) realization can be adopted for the DLF. This is done by adding an integral path with an integrator and a multiplication factor α in parallel with the proportional path, as illustrated in Figure 3.6(a). The difference equations for the integral and proportional paths, respectively are

$$tw_i[k] = \alpha e[k-D] + tw_i[k-1] \tag{3.10}$$



(a) DLF time domain model. (b) DLF z-transform model.

Figure 3.6 DLF models.

$$tw_p[k] = \beta e[k-D] \tag{3.11}$$

The z-transforms of the proportional and integral branches are, respectively (see Figure 3.6(b))

$$tw_i(z) = \alpha e(z) z^{-D} + z^{-1} tw_i(z) \tag{3.12}$$

$$tw_p(z) = \beta e(z) z^{-D} \tag{3.13}$$

The overall difference equation is the summation of both the integral and proportional paths, such that

$$tw[k] = tw_i[k] + tw_p[k] \tag{3.14}$$

which yields to a corresponding z-transform transfer function as follows

$$H_{DLF}(z) = \frac{tw(z)}{e(z)} = [\beta + \frac{\alpha}{1-z^{-1}}]z^{-D} \tag{3.15}$$

In order to improve noise suppression, more integrators can be employed, but at the price of stability issues. Therefore, the vast majority of DPLLs are type-II 2^{nd}-order DPLL and therefore all the upcoming analysis target only type-II 2^{nd}-order DPLL.

3.2.1.4 MMD AND $\Delta\Sigma$ MODULATOR

A Digital MASH $\Delta\Sigma$ modulator can be realized by cascading accumulators and summing their weighted outputs [41]. Figure 3.7 shows a MASH 1.1.1 $\Delta\Sigma$ modulator. The combiner is responsible for combining the three single-bit

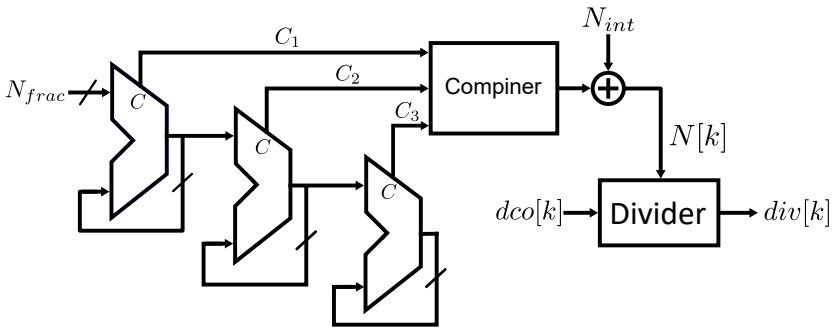


Figure 3.7 Digital MASH 1.1.1 ΔΣ modulator.

carry-out, satisfying a 3rd-order ΔΣ quantization noise shaping. Hence, the output can be expressed as [41]

$$out_{\Delta\Sigma} = C_1 z^{-3} + C_2(z^{-2} - z^{-3}) + C_3(z^{-1} - 2z^{-2} + z^{-3}) \tag{3.16}$$

In general, the process of modeling a ΔΣ modulator starts by firstly assuming its quantization noise is independent of its input [47]. Thereafter, a linear time-invariant model that defines the relationship from the input and quantization noise to the output can be constructed [47]. A MASH ΔΣ modulator of order m, input $x(k)$ and output $y(k)$ is described in z-domain by [47]

$$y(z) = x(z) - (1 - z^{-1})^m q_{\Delta\Sigma}(z) \tag{3.17}$$

where $q_{\Delta\Sigma}[k]$ is the ΔΣ modulator quantization noise, equal to

$$q_{\Delta\Sigma}[k] = N[k] - N_{nom} \tag{3.18}$$

$$N_{nom} = N_{int} + N_{frac} \tag{3.19}$$

A MASH structure of order m can be defined with two terms [47]: Signal Transfer Function (STF) and Noise Transfer Function (NTF), which in this case, are

$$STF: \;\; H_s(z) = 1 \tag{3.20}$$

$$NTF: \;\; H_n(z) = (1 - z^{-1})^m \tag{3.21}$$

Figure 3.8 and 3.9 show both the time and z-domain models for the divider combined with a ΔΣ modulator.

A conclusion can be derived from the above equations, i.e., that the ΔΣ modulator output both its input and its quantization noise $q_{\Delta\Sigma}[k]$ high-pass shaped; by a filter $(1 - z^{-1})^m$. Ideally, $q_{\Delta\Sigma}$ is white and uniformly distributed between 0 and 1, therefore its spectrum is flat with a magnitude of $1/12$ [47].

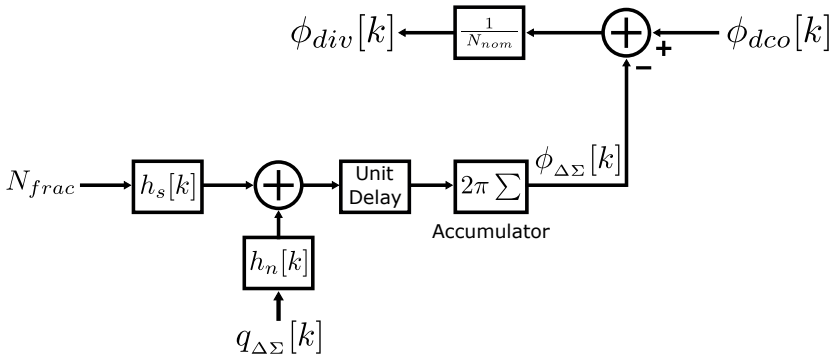


Figure 3.8 Divider and ΔΣ modulator time domain model.

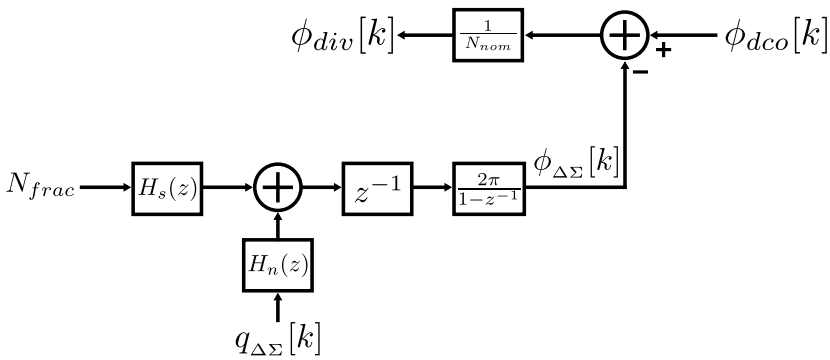


Figure 3.9 Divider and ΔΣ modulator z-domain model.

3.2.1.5 OVERALL TRANSFER FUNCTIONS

Figure 3.10 shows the overall z-domain model of a TDC-based DPLL. Based on the above transfer functions of all the loop blocks, the overall transfer function of the system can be derived. Furthermore, from the z-domain transfer function a simplified approximation in s-domain is also derived.

3.2.1.5.1 z-domain Transfer Function

From Figure 3.10, where another scale factors of T_{ref} and $1/T_{ref}$ account for the Discrete-Time (DT)-Continuous-Time (CT) and CT-DT conversions are added [50], the open-loop transfer function in z-domain can be expressed as

$$H_{ol}(z) = T_{ref}^2 K_{tdc} K_{dco} H_{DLF}(z) \frac{1}{N_{nom}} \frac{1}{1-z^{-1}} \tag{3.22}$$

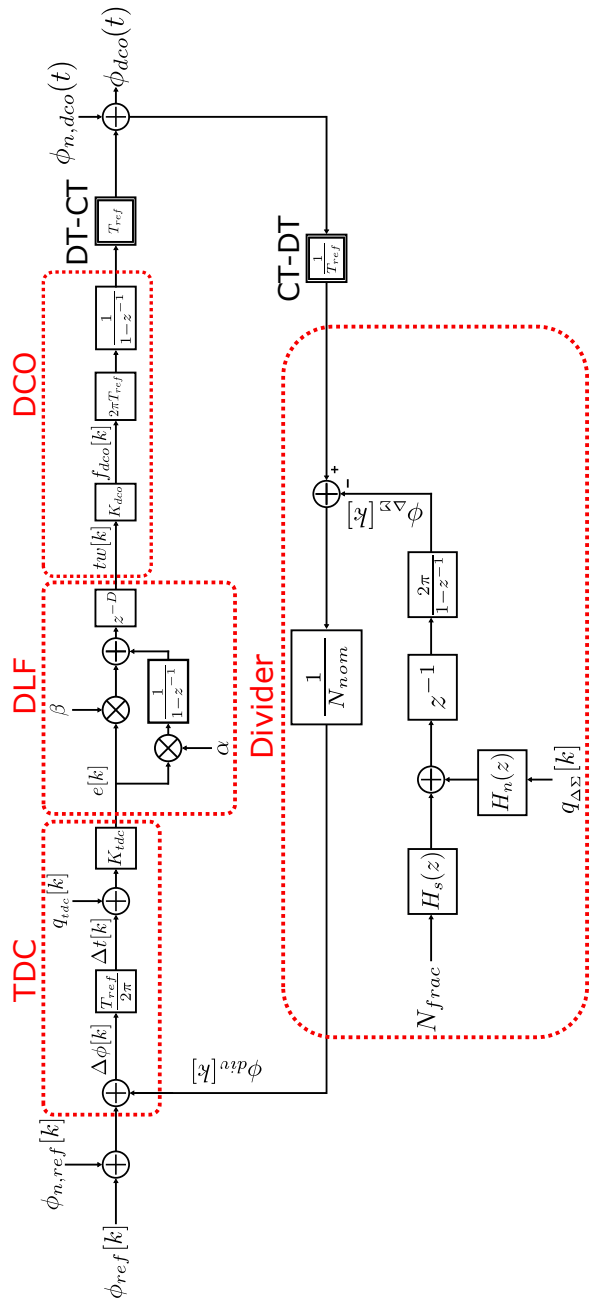


Figure 3.10 TDC-based DPLL z-domain model.

The overall closed-loop transfer function can be written as

$$H_{cl}(z) = \frac{\phi_{dco}}{\phi_{ref}} = \frac{H_{ol}(z)}{1 + H_{ol}(z)} \tag{3.23}$$

$$H_{cl}(z) = \frac{T_{ref}^2 K_{tdc} K_{dco} H_{DLF}(z)/(1 - z^{-1}) N_{nom}}{1 + T_{ref}^2 K_{tdc} K_{dco} H_{DLF}(z)/(1 - z^{-1}) N_{nom}} \tag{3.24}$$

3.2.1.5.2 *s*-domain Transfer Function

Although the *z*-transform is the natural description of any DT system, it is common also to approximate DPLLs with a linear CT system in *s*-domain. The conversion can be performed relying on the following approximation [47]:

$$z^{-1} = e^{-sT_{ref}} \approx 1 - sT_{ref} \tag{3.25}$$

where $s = j2\pi f$. The above approximation is valid under the assumption that T_{ref} is much longer than the loop time constants, where the accuracy of the approximation depends on the DPLL bandwidth. Substituting (3.25) into (3.22), the open-loop *s*-domain transfer function can be derived, i.e.,

$$H_{ol}(s) = T_{ref} K_{tdc} K_{dco} H_{DLF}(s) \frac{1}{s} \frac{1}{N_{nom}} \tag{3.26}$$

The overall closed-loop transfer function in *s*-domain can thus be written as

$$H_{cl}(s) = \frac{\phi_{dco}}{\phi_{ref}} = \frac{H_{ol}(s)}{1 + H_{ol}(s)} = \frac{T_{ref} K_{tdc} K_{dco} H_{DLF}(s)/sN_{nom}}{1 + T_{ref} K_{tdc} K_{dco} H_{DLF}(s)/sN_{nom}} \tag{3.27}$$

The unity gain frequency is equal to

$$f_u \approx \frac{\beta T_{ref} K_{tdc} K_{dco}}{2\pi N_{nom}} \tag{3.28}$$

The above approximation is only valid if $f_u \gg f_z$, where f_z is the stabilizing zero and is equal to

$$f_z = \frac{\alpha}{2\pi\beta T_{ref}} \tag{3.29}$$

In this case, f_u can be used as a good approximation of the closed-loop bandwidth.

Figure 3.11 shows the magnitude responses of the transfer function $H_{cl}(z)$ and its *s*-domain approximation $H_{cl}(s)$ for three different values of α and β. The reference frequency is chosen to be 40 MHz, and the output frequency is equal to 3 GHz.

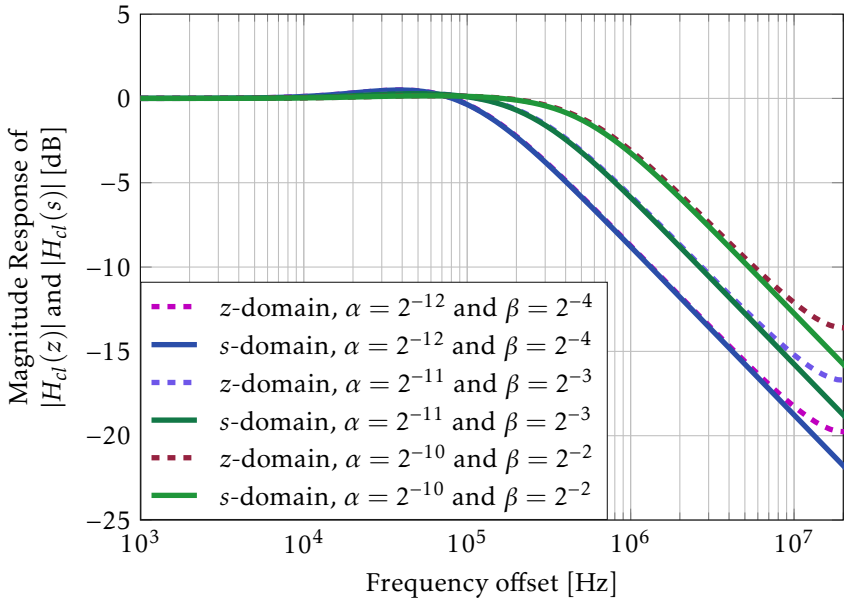


Figure 3.11 Matlab simulations showing the magnitude responses of the closed-loop transfer function in z-domain $|H_{cl}(z)|$ and also in s-domain $|H_{cl}(s)|$ for three different values of α and β.

3.2.2 NOISE SOURCES ANALYSIS

The analysis of different noise blocks of the TDC-based DPLL, and their contributions to the overall noise performance, is introduced in this section. Four dominant sources of noise are discussed in details, as shown in Figure 3.10: a) Reference signal noise, b) TDC quantization noise, c) DCO signal noise and d) $\Delta\Sigma$ modulator quantization noise. They are labeled as $\phi_{n,ref}$, q_{tdc}, $\phi_{n,dco}$ and $q_{\Delta\Sigma}$, respectively. The analysis is done in both z-domain and s-domain. For the forthcoming simulations, the reference frequency is chosen to be 40 MHz and the output frequency is equal 3 GHz, with $N_{int} = 75$ and $N_{frac} = 0$.

3.2.2.1 REFERENCE NOISE TRANSFER FUNCTION

In order to study the effect of the reference noise, a reference noise transfer function is needed to be derived from Figure 3.10, as follows:

$$H_{\phi_{n,ref}}(z) = \frac{\phi_{dco}}{\phi_{n,ref}} = \frac{T_{ref}^2 K_{tdc} K_{dco} H_{DLF}(z)/(1-z^{-1})N_{nom}}{1 + T_{ref}^2 K_{tdc} K_{dco} H_{DLF}(z)/(1-z^{-1})N_{nom}} \tag{3.30}$$

The right hand side of (3.30) is the closed-loop transfer function of the system, therefore

$$H_{\phi_{n,ref}}(z) = H_{cl}(z) \tag{3.31}$$

Consequently, the noise transfer function of the reference in s-domain is

$$H_{\phi_{n,ref}}(s) = \frac{\phi_{dco}}{\phi_{n,ref}} = \frac{T_{ref}K_{tdc}K_{dco}H_{DLF}(s)/sN_{nom}}{1 + T_{ref}K_{tdc}K_{dco}H_{DLF}(s)/sN_{nom}} \tag{3.32}$$

$$H_{\phi_{n,ref}}(s) = H_{cl}(s) \tag{3.33}$$

The reference noise transfer function $H_{\phi_{n,ref}}$ has a low-pass nature, as it is equal the closed-loop function. Hence, the more bandwidth reduction, the better reference noise suppression.

3.2.2.2 TDC NOISE TRANSFER FUNCTION

The TDC noise transfer function can be calculated as

$$\phi_{dco} = [-\frac{1}{2\pi N_{nom}}\phi_{dco} + q_{_{tdc}}]2\pi T_{ref}^2 K_{tdc}K_{dco}H_{DLF}(z)\frac{1}{1-z^{-1}} \tag{3.34}$$

$$\phi_{dco} = [-\phi_{dco} + 2\pi N_{nom}q_{_{tdc}}]T_{ref}^2 K_{tdc}K_{dco}H_{DLF}\frac{1}{(1-z^{-1})N_{nom}} \tag{3.35}$$

$$\phi_{dco} = [-\phi_{dco} + 2\pi N_{nom}q_{_{tdc}}]H_{ol}(z) \tag{3.36}$$

Thereafter, the TDC noise transfer function in z-domain can be expressed as

$$H_{q_{tdc}}(z) = \frac{\phi_{dco}}{q_{_{tdc}}} = 2\pi N_{nom}\frac{H_{ol}(z)}{1 + H_{ol}(z)} = 2\pi N_{nom}H_{cl}(z) \tag{3.37}$$

The TDC noise transfer function in s-domain is

$$H_{q_{tdc}}(s) = \frac{\phi_{dco}}{q_{_{tdc}}} = 2\pi N_{nom}H_{cl}(s) \tag{3.38}$$

Figure 3.12 shows the magnitude responses of the TDC noise transfer function for three different values of α and β. As shown in the figure, the TDC noise transfer function behaves as a LPF with a DC gain of $2\pi N_{nom}$. As the reference noise, the TDC noise is better attenuated with decreasing the DPLL bandwidth.

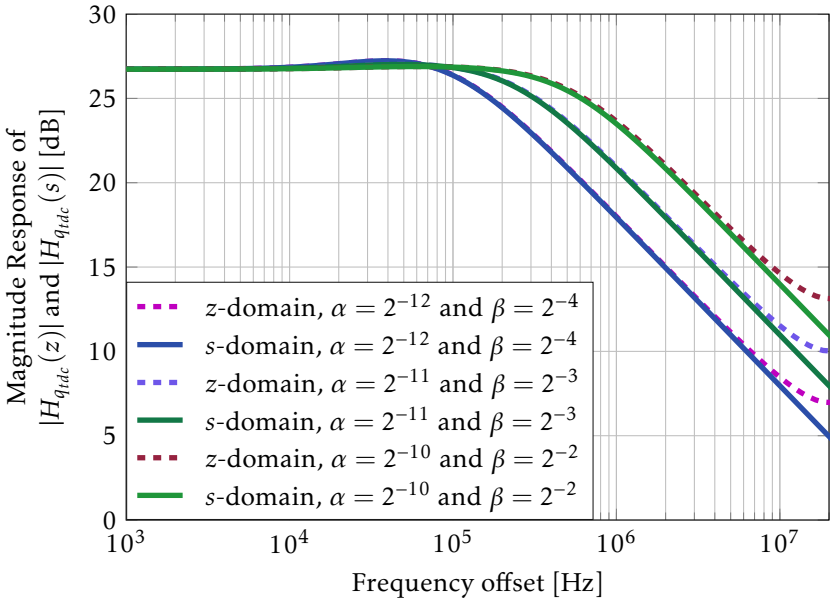


Figure 3.12 Matlab simulations showing the magnitude responses of the TDC noise transfer function $|H_{q_{tdc}}(z)|$ in z-domain and $|H_{q_{tdc}}(s)|$ in s-domain for three different values of α and β.

3.2.2.3 DCO NOISE TRANSFER FUNCTION

From the presented model, the DCO noise transfer function can be found as

$$\phi_{dco} = -T_{ref}^2 K_{tdc} K_{dco} H_{DLF}(z) \frac{1}{(1-z^{-1})N_{nom}} \phi_{dco} + \phi_{n,dco} \tag{3.39}$$

$$\phi_{dco} = -H_{ol}(z)\phi_{dco} + \phi_{n,dco} \tag{3.40}$$

Consequently, the DCO noise transfer function in z-domain is

$$H_{\phi_{n,dco}}(z) = \frac{\phi_{dco}}{\phi_{n,dco}} = \frac{1}{1+H_{ol}(z)} \tag{3.41}$$

$$H_{\phi_{n,dco}}(z) = \frac{1+H_{ol}(z)-H_{ol}(z)}{1+H_{ol}(z)} = 1 - H_{cl}(z) \tag{3.42}$$

The DCO noise transfer function in s-domain is

$$H_{\phi_{n,dco}}(s) = \frac{\phi_{dco}}{\phi_{n,dco}} = 1 - H_{cl}(s) \tag{3.43}$$

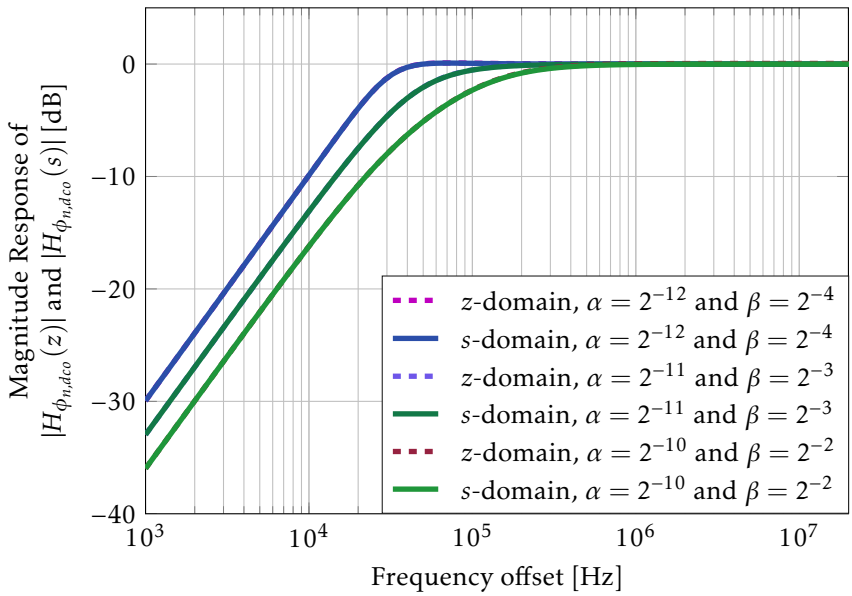


Figure 3.13 Matlab simulations showing the magnitude responses of the DCO noise transfer function $|H_{\phi_{n,dco}}(z)|$ in z-domain and $|H_{\phi_{n,dco}}(s)|$ in s-domain for three different values of α and β.

Figure 3.13 shows the magnitude responses of the DCO noise transfer function for three different values of α and β. The transfer function behaves as a High Pass Filter (HPF) with a high frequency gain of 1. As a result, from a design perspective, the DCO noise is better suppressed by increasing the bandwidth of the DPLL.

3.2.2.4 $\Delta\Sigma$ MODULATOR NOISE TRANSFER FUNCTION

The $\Delta\Sigma$ modulator noise transfer function can be derived from Figure 3.10 by firstly deriving an expression for $\phi_{_{\Delta\Sigma}}$ with respect to ϕ_{dco}, as follows:

$$\phi_{dco} = [-\frac{1}{T_{ref}}\phi_{dco} + \phi_{_{\Delta\Sigma}}]T_{ref}^3 K_{tdc} K_{dco} H_{DLF}(z) \frac{1}{(1-z^{-1})N_{nom}} \tag{3.44}$$

$$\phi_{dco} = [-\phi_{dco} + T_{ref}\phi_{_{\Delta\Sigma}}]H_{ol}(z) \tag{3.45}$$

$$\frac{\phi_{dco}}{\phi_{_{\Delta\Sigma}}} = T_{ref}\frac{H_{ol}(z)}{1+H_{ol}(z)} = T_{ref}H_{cl}(z) \tag{3.46}$$

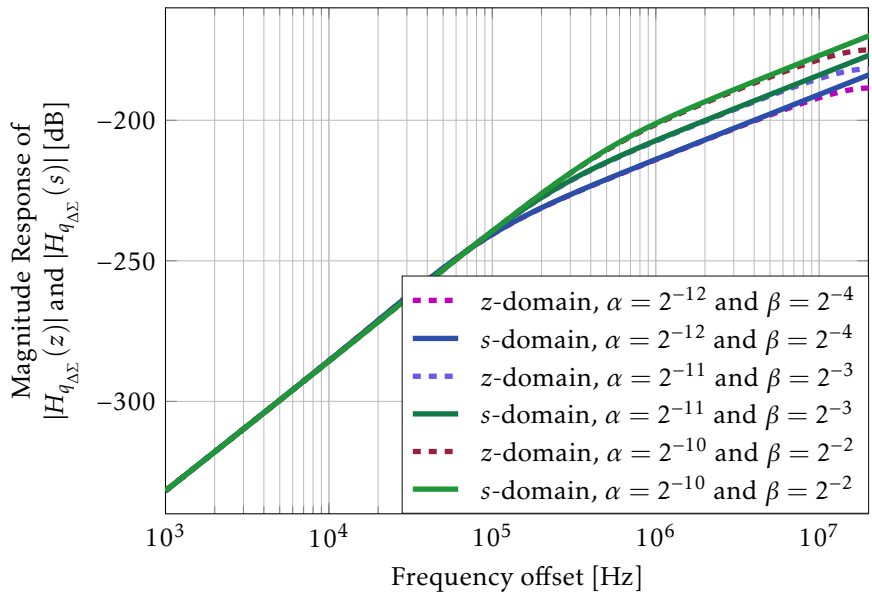


Figure 3.14 Matlab simulations showing the magnitude responses of the ΔΣ modulator noise transfer function $|H_{q_{\Delta\Sigma}}(z)|$ in z-domain and $|H_{q_{\Delta\Sigma}}(s)|$ in s-domain for three different values of α and β.

Consequently, the ΔΣ modulator noise transfer function is

$$H_{q_{\Delta\Sigma}}(z) = \frac{\phi_{dco}}{q_{\Delta\Sigma}} = \frac{\phi_{dco}}{\phi_{\Delta\Sigma}} \frac{\phi_{\Delta\Sigma}}{q_{\Delta\Sigma}} = 2\pi T_{ref} \frac{z^{-1}}{(1-z^{-1})} H_n(z) H_{cl}(z) \tag{3.47}$$

And the noise transfer function in s-domain is

$$H_{q_{\Delta\Sigma}}(s) = \frac{\phi_{dco}}{q_{\Delta\Sigma}} = 2\pi \frac{1 - sT_{ref}}{s} H_n(s) H_{cl}(s) \tag{3.48}$$

Figure 3.14 shows the magnitude responses of the ΔΣ modulator noise transfer function for three different values of α and β. The same consideration for the ΔΣ modulator quantization noise can be made as for TDC and reference noise: the lower the bandwidth, the higher the noise suppression.

3.2.3 PHASE NOISE PERFORMANCE

In the investigated DPLL architecture, the phase information is basically extracted from the zero crossing of the periodic signals. Therefore, to evaluate the PSD of the phase noise, only the zero crossings are considered. For this reason, in order to model the system, it is enough to calculate the zero-crossings

[47], which accordingly decreases the number of computations. Hence, the TDC-based DPLL is modeled such that only the time instances of the rising and falling edge events of the DCO signal are captured. Accordingly, the phase information of the DCO output is extracted and used to estimate the overall PSD $S_{\phi,tot}(f)$. Then the simulation results are compared with the results coming from the model shown in Figure 3.15, which shows the PSD of each contributed noise with its corresponding noise transfer function. Because reference noise, TDC quantization noise, DCO noise and $\Delta\Sigma$ modulator quantization noise are uncorrelated to each other, the overall noise spectral density $S_{\phi,tot}$ at the DPLL output can be obtained by summing the noise PSD of each contributing, as shown in the figure. One important note is that the calculation of the noise PSD requires both DT and CT signals. Therefore, the following three equations need to be accurately evaluated [50]:

1. If a CT input $x(t)$ is fed to CT filter $H(f)$ to produce a CT output $y(t)$

$$S_y(f) = |H(f)|^2 S_x(f) \tag{3.49}$$

where S_x and S_y are the PSD for the x and y signals, respectively.

2. If a DT input $x[k]$ is fed to CT filter $H(f)$ to produce a CT output $y(t)$

$$S_y(f) = \frac{1}{T}|H(f)|^2 S_x(e^{j2\pi fT}) \tag{3.50}$$

where T is the sampling time.

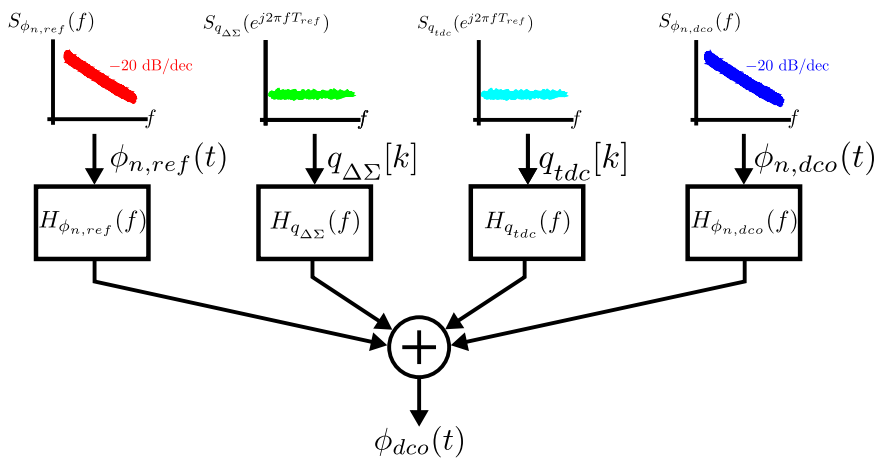


Figure 3.15 Phase noise calculation model.

3. If a DT input $x[k]$ is fed to DT filter $H(e^{j2\pi fT})$ to produce a DT output $y[k]$

$$S_y(e^{j2\pi fT}) = |H(e^{j2\pi fT})|^2 S_x(e^{j2\pi fT}) \tag{3.51}$$

Two cases are tested:

1. **Integer-N Operation:** In case of integer-N channel, the simulation is done at 3.0 GHz with a 40 MHz reference clock and 5 ns TDC resolution, with a DPLL bandwidth equal to 500 kHz. Figure 3.16(a) shows the results from simulations compared with the model of Figure 3.15. The figure also illustrates the contribution of each block to the total phase noise. The simulated phase noise agrees very well with the model.

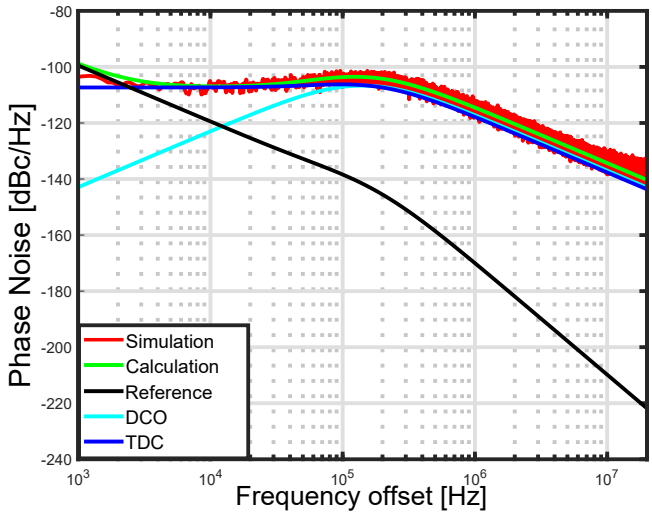
2. **Fractional-N Operation:** For fractional-N operation, the performance is limited by the noise folding due to the quantization noise produced as a consequence of the dithering action of the $\Delta\Sigma$ modulator. This dithering produces high-pass shaped noise similar to the $\Delta\Sigma$-ADC quantization noise, which degrades the output phase noise performance and modulates the oscillator output causing fractional spurs, as shown in Figure 3.16(b). Cancellation schemes using adaptive LMS algorithms can be adopted to alleviate the fractional spurs problem (see Chapter 6).

3.3 BANG-BANG-BASED DPLL

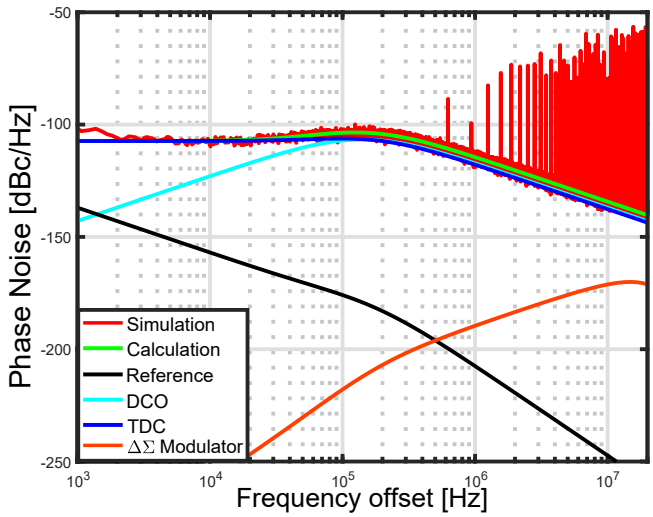
In a TDC-based DPLL, a high TDC resolution plays a very important role in achieving a low-noise wide-bandwidth DPLL. If the TDC quantization noise is assumed to be white, then the in-band phase noise floor of a DPLL for a TDC resolution of Δ is [33]

$$\text{PN} = 10\log[\frac{(2\pi N_{nom})^2}{T_{ref}}\frac{\Delta^2}{12}] \tag{3.52}$$

To provide an intuitive view for the high demand of high TDC resolution when a low phase noise with high DPLL bandwidth is desired, two examples are explored. The examples illustrate the phase noise performance under the same circumstances of 3 GHz output frequency, 40 MHz reference frequency and 75 division ratio, but with different TDC resolutions and bandwidths. According to (3.52), the TDC contributes an in-band phase noise of -95 dBc/Hz for a 20 ps TDC resolution. The bandwidth in this case is 100 kHz (low bandwidth), as shown by the red line plotted in Figure 3.17. However, in order to lower the in-band phase noise, while enlarging the bandwidth beyond 100 kHz, the TDC resolution has to be improved, as shown by the blue



(a) Simulated TDC-based DPLL phase noise at 3.0 GHz with a 40 MHz reference clock and 5 ns TDC resolution with a bandwidth of 500 kHz, for integer channel.



(b) Simulated TDC-based DPLL phase noise at 3.0 GHz with a 40 MHz reference clock and 5 ns TDC resolution with a bandwidth of 500 kHz, for fractional channel.

Figure 3.16 Simulated TDC-based DPLL phase noise for integer and fractional channels.

line plotted in the same figure. In this example, a TDC with 5 ps is used. Accordingly, the TDC contributes an in-band phase noise of -107 dBc/Hz, which demonstrates that the only applicable way to achieve low phase noise performance with larger bandwidth is to improve the TDC resolution.

As the TDC resolution is one of the key limitations in the TDC-based DPLL, much effort has been dedicated to enhancing its resolution, at the cost of higher complexity and power consumption. In this sense, architectures based on a BBPD, are very attractive, as shown in Figure 3.18. The BBPD is basically a D-Flip flop that samples the reference signal by means of the divided signal, and is commonly used in clock and data recovery circuitry [58–62]. Next, the operation of the BB-based DPLL is explained, thereafter its transfer function is derived.

3.3.1 DISCRETE AND CONTINUOUS-TIME MODELS

The BBPD has the ability to detect only sign information of phase difference between two signals; in other words, it generates an output in the form of a lead/lag pulse of fixed width and amplitude. The width and amplitude of the

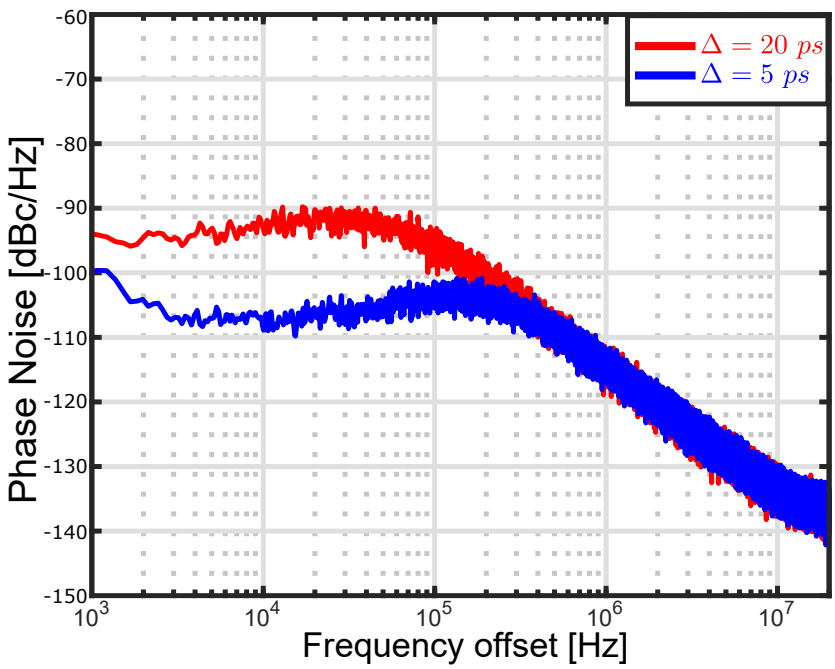


Figure 3.17 Phase noise performance for different TDC resolution and bandwidths.

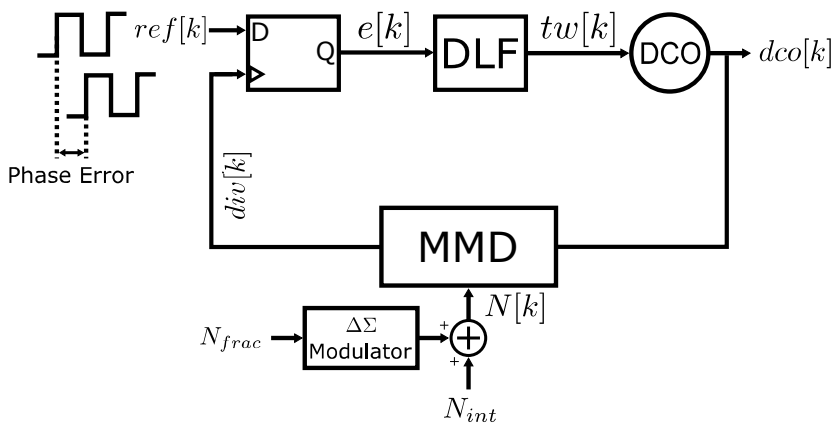


Figure 3.18 DPLL employing a BBPD.

output pulses are, however, insensitive to the magnitude of the input phase difference. Even when the loop is locked, the output of the BBPD dithers between lead and lag decisions. Therefore, the BBPD characteristic is highly non-linear and causes strong dithering jitter at the DPLL output. The non-linear transfer characteristic of the BBPD needs a non-linear technique to analyze the DPLL behavior. However, in various literature, it is shown that the BBPD can be linearized in the presence of both reference and DCO noise [48] [49] [51–56].

Following the same procedure as in the TDC-based DPLL, with the same block modeling except for the BBPD, a z-domain model of the BB-based DPLL is constructed in Figure 3.19, where the BBPD is replaced by a gain K_{bbpd}. Therefore, the open-loop transfer function of the DPLL can be written as

$$H_{ol}(z) = T_{ref}^2 K_{bbpd} K_{dco} H_{DLF}(z) \frac{1}{N_{nom}} \frac{1}{1-z^{-1}} \tag{3.53}$$

The overall closed-loop transfer function can be written as

$$H_{cl}(z) = \frac{\phi_{dco}}{\phi_{ref}} = \frac{H_{ol}(z)}{1+H_{ol}(z)} \tag{3.54}$$

$$H_{cl}(z) = \frac{T_{ref}^2 K_{bbpd} K_{dco} H_{DLF}(z)/(1-z^{-1}) N_{nom}}{1+T_{ref}^2 K_{bbpd} K_{dco} H_{DLF}(z)/(1-z^{-1}) N_{nom}} \tag{3.55}$$

Consequently, the open-loop transfer function of the system in s-domain is

$$H_{ol}(s) = T_{ref} K_{bbpd} K_{dco} H_{DLF}(s) \frac{1}{s} \frac{1}{N_{nom}} \tag{3.56}$$

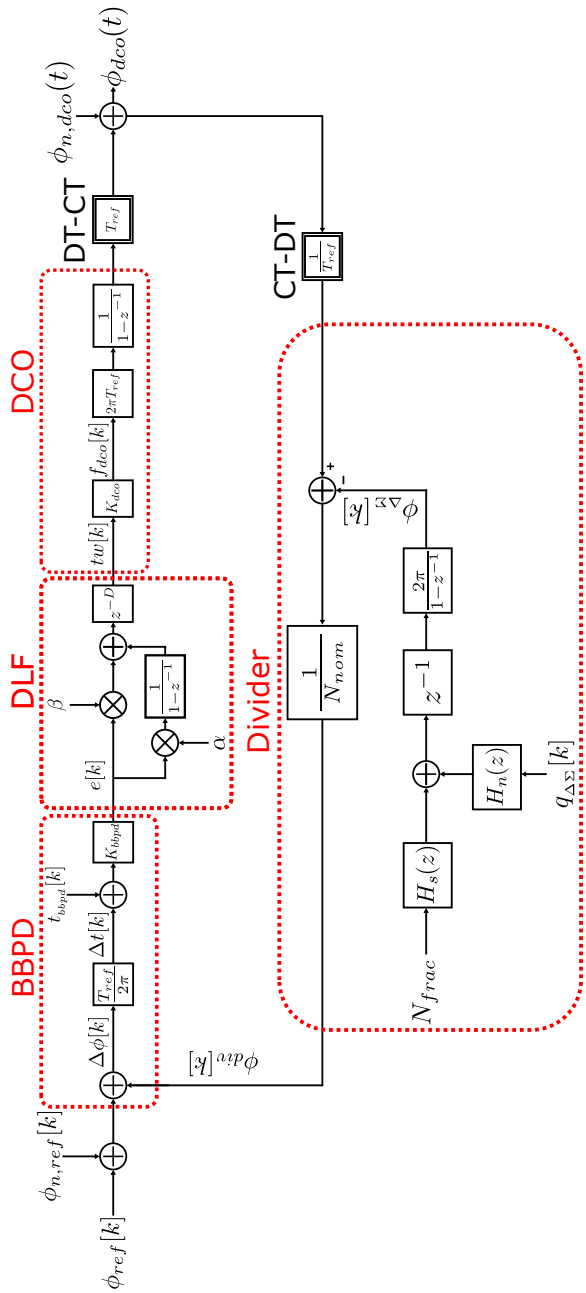


Figure 3.19 BB-based DPLL z-domain model.

The corresponding overall closed-loop transfer function in s-domain can be written as

$$H_{cl}(s) = \frac{\phi_{dco}}{\phi_{ref}} = \frac{H_{ol}(s)}{1 + H_{ol}(s)} \tag{3.57}$$

$$H_{cl}(s) = \frac{T_{ref} K_{bbpd} K_{dco} H_{DLF}(s)/sN_{nom}}{1 + T_{ref} K_{bbpd} K_{dco} H_{DLF}(s)/sN_{nom}} \tag{3.58}$$

The gain K_{bbpd} is set by [51]

$$K_{bbpd} = \sqrt{\frac{2}{\pi}} \frac{1}{\sigma_{\Delta t}} \tag{3.59}$$

where $\sigma_{\Delta t}$ is the standard deviation of the time difference $\Delta t[k] = t_{ref}[k] - t_{div}[k]$ and can be calculated as [51]

$$\sigma^2_{\Delta t} \approx \frac{N}{4\pi}[1 - \frac{2}{\pi} tan^{-1} \frac{f_z}{f_u}] \frac{f_{ref}}{f_u} \sigma^2_{T_{dco}} \tag{3.60}$$

where $\sigma_{T_{dco}}$ is the standard deviation of the white Gaussian noise which is superimposed to the DCO period T_{dco}, while f_z and f_u are the unity gain and stabilizing zero of the BB system, respectively. In this case, f_u is equal to

$$f_u \approx \frac{\beta T_{ref} K_{bbpd} K_{dco}}{2\pi N_{nom}} \tag{3.61}$$

Accordingly, two operation regions for the BB-based DPLL can be classified:

1. **Random Noise Regime:** If the noise sources within the loop are strong enough to scramble the BBPD quantization error, the mode of operation is referred to as random noise regime [49]. In this regime, and under the assumption of $f_u / f_z > 5$, (3.60) is simplified to

$$\sigma_{\Delta t} \approx \sqrt{\frac{\pi}{8}} \frac{\sigma^2_{T_{dco}}}{\beta K_{dco} T^2_{dco}} \tag{3.62}$$

2. **Limit Cycle Regime:** In the absence of enough random noise to scramble the BBPD quantization error, the BBPD quantization error will modulate the DCO, giving rise to large fractional spurs. This mode of operation is called limit cycle regime [49]. In the limit cycle regime, $\sigma_{\Delta t}$ can be calculated as [49]

$$\sigma_{\Delta t} \approx \frac{1 + D}{\sqrt{3}} N \beta K_{dco} T^2_{dco} \tag{3.63}$$

Finally, $\sigma_{\Delta t}$ is the sum of (3.62) and (3.63), given by

$$\sigma_{\Delta t} \approx \sqrt{\frac{\pi}{8}} \frac{\sigma_{T_{dco}}^2}{\beta K_{dco} T_{dco}^2} + \frac{1+D}{\sqrt{3}} N \beta K_{dco} T_{dco}^2 \tag{3.64}$$

The optimum β can be calculated as [51]

$$\beta|_{opt} \approx \frac{\sqrt[4]{3\pi/8}}{K_{dco} T_{dco}^2 \sqrt{(1+D)N}} \sigma_{T_{dco}} \tag{3.65}$$

To be able to synthesize fractional channels through BB operation, a $\Delta\Sigma$ modulator is used to dither the MMD, as shown in Figure 3.18. As a result, this dithering operation introduces a phase modulation into the $div[k]$ signal, whose amplitude is proportional to the accumulated quantization error $n_{div}[k]$ of the $\Delta\Sigma$ modulator, which in turn depends on the order of the $\Delta\Sigma$ modulator. The sequence $n_{div}[k]$, in steady-state operation, makes $\Delta t[k]$ periodic, which experience a large step of one T_{dco}, if a 1st-order $\Delta\Sigma$ modulator is used, and larger than one T_{dco} if higher orders are used. This step is much larger than

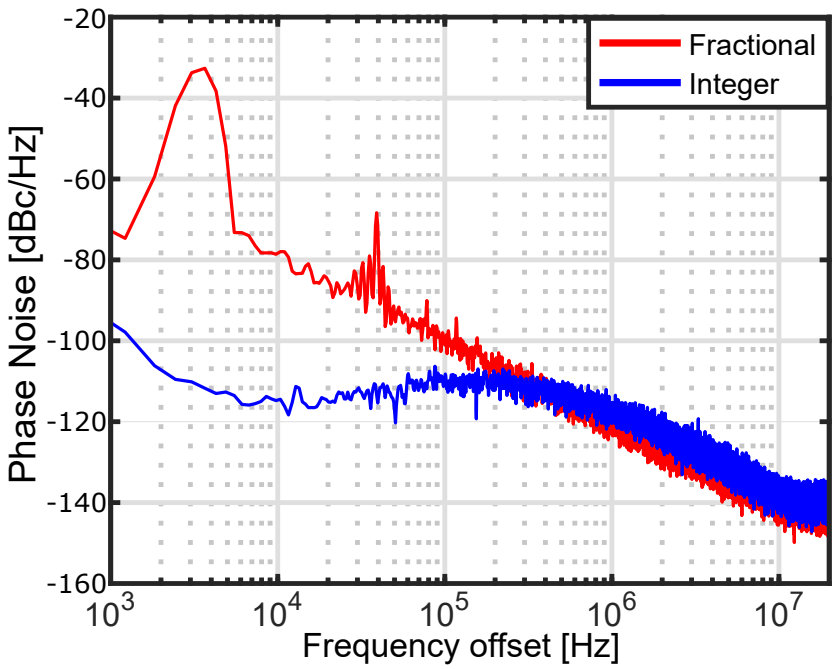


Figure 3.20 Matlab simulation of a BB-based DPLL when an integer channel and a fractional channel are synthesized.

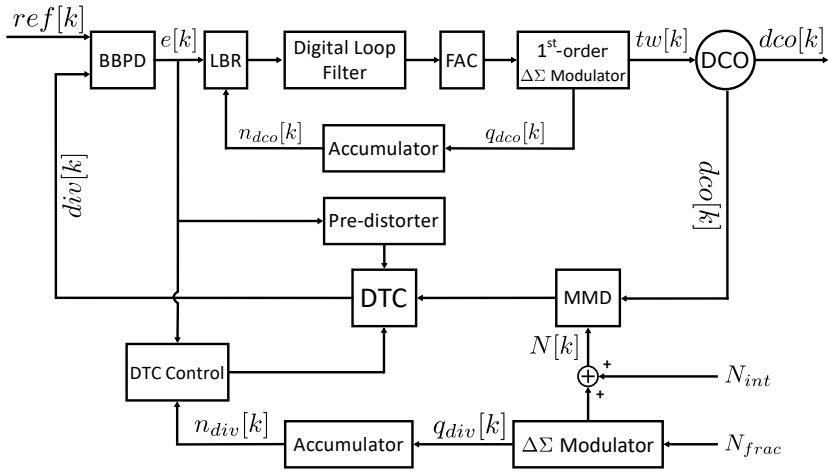


Figure 3.21 BB-based DPLL complete block diagram.

$\sigma_{\Delta t}$, leading to a complete loss of the random noise regime, and making the DPLL converging to the limit cycle region. Consequently, the $\Delta t[k]$ periodic signal in turn makes the DCO tuning word periodic. Thereafter, the periodic sequence $tw[k]$ modulates the DCO output signal, generating large fractional spurs that may fall within the DPLL bandwidth [35].

Figure 3.20 shows a phase noise simulation comparison between two division ratios when an integer channel and a fractional channel are synthesized, employing a 1st-order $\Delta\Sigma$ modulator. The figure explicitly shows the large difference in phase noise performance between the two cases, where the spectrum in the fractional case has much larger noise and spurs than the one in the integer case.

So, to exploit the BBPD in fractional operations, the random noise regime has to be recovered. This means that the $\Delta\Sigma$ quantization step has to be reduced below the random noise level before it arrives to the BBPD input. This operation recovers the random noise regime and as a result breaks the fractional periodicity, leading to elimination of fractional spurs. This is done by inserting a DTC into the feedback loop after the MMD. The DTC adds a controllable time shift on $div[k]$, reducing the time error $\Delta t[k]$. By doing that, $\Delta t[k]$ in this case will be as large as fractions of T_{dco}, instead of one or more T_{dco} [35]. Although the stringent requirements of the TDC, in terms of resolution and linearity, are now moved from the TDC side to the DTC side, it is nevertheless true that designing a high-resolution DTC is easier than designing a high-resolution TDC. Nonetheless, as is the case with the TDC, DTC non-linearity causes imperfect cancellation of quantization noise. However,

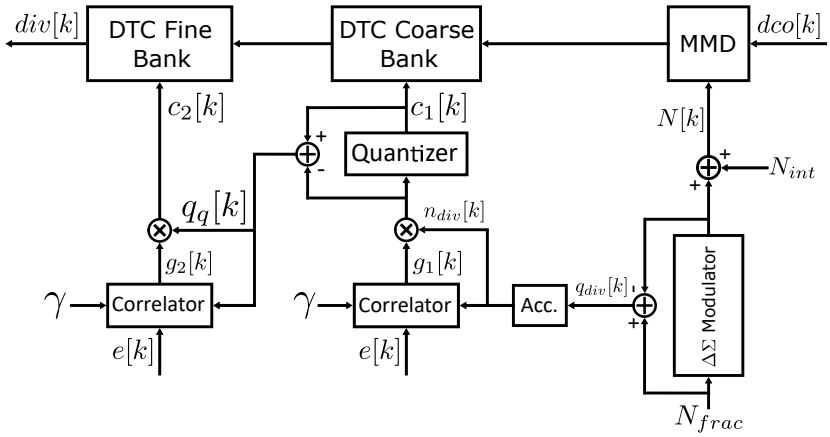


Figure 3.22 Block schematic view of the DTC control.

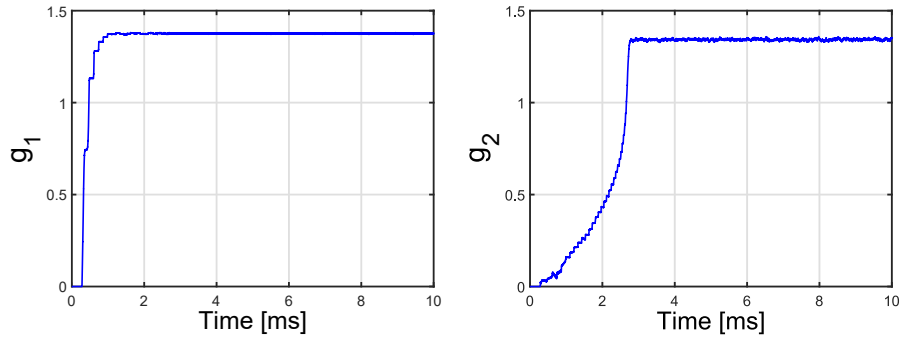
its non-linearity can be handled by implementing a background pre-distortion technique [4], which efficiently solve the DTC non-linearity problems.

Figure 3.21 shows the complete block diagram of a BB-based DPLL. As shown in the figure, the main loop is assisted by: a) DTC control b) Predistorter c) Loop Bandwidth Regulation (LBR) d) Frequency Acquisition Controller (FAC) and finally e) a 1^{st}-order digital $\Delta\Sigma$ modulator dithering the control bits of the DCO. In the next sub-sections, the details of each block are illustrated.

3.3.1.1 DTC CONTROL

The DTC is adaptively controlled by means of algorithms based on the LMS concept [35]. Figure 3.22 shows the control process, where two DTC banks are used: coarse and fine banks. Control is achieved in two steps. The first step starts by firstly extracting the quantization error from the $\Delta\Sigma$ modulator $q_{div}[k]$, then accumulating it to generate the accumulated quantization noise $n_{div}[k]$. The output from the accumulator is then correlated with the BBPD output $e[k]$ to generate the first estimated gain $g_1[k]$. The signal $n_{div}[k]$ is then corrected by $g_1[k]$ generating $c_1[k]$, which is finally converted into a time delay by the DTC coarse bank. The process continues to compensate for the quantization noise occurring in the first step. The process starts in the same way by extracting the quantization error $q_q[k]$ from the quantizer and correlating it with $e[k]$. The correlation result represents the second estimated gain $g_2[k]$. This gain is multiplied by $q_q[k]$ to generate the second control word $c_2[k]$ that controls the DTC fine bank (see Figure 3.22). The need for automatically adjustable gains is due to the desire to compensate for any Process, Voltage and

Temperature (PVT) variations that can affect the DTC gain. The convergence speed of g_1 and g_2 is controlled by changing the LMS coefficient γ. Unfortunately, speeding up the settling time of the algorithm comes with the price of



(a) Simulated transient of the LMS coefficient g_1.

(b) Simulated transient of the LMS coefficient g_2.

Figure 3.23 Simulated transients of the LMS coefficients.

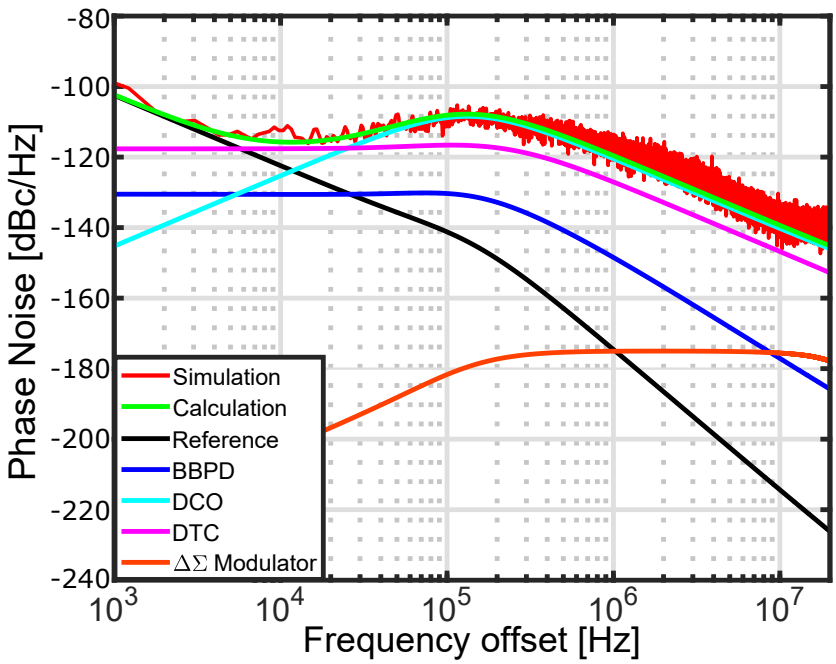


Figure 3.24 Simulated phase noise for the worst case fractional division ratio.

larger fluctuations of the estimated gains, which makes the cancellation process imperfect, resulting in a degradation in spurious tones levels. Figure 3.23 shows the simulated transient gains (g_1 and g_2) with γ equal 2^{-10} from start-up to the final value.

A 1st-order $\Delta\Sigma$ modulator is not sufficient to make the LMS loop works properly in the case of a near-integer fractional channel, as the streaming output of a 1st-order $\Delta\Sigma$ modulator is almost constant. Furthermore, the LMS loop must be much slower than the period of the signal n_{div}, in order to work properly, which is not achieved with a 1st-order $\Delta\Sigma$ modulator [63], as it displays very low-frequency idle tones. The streaming output of a 2nd-order $\Delta\Sigma$ modulator, on the other hand, generates a much faster output that makes the LMS loop works properly [35]. Figure 3.24 shows the simulated BB-based DPLL phase noise at 3.0 GHz with a 40 MHz reference clock. The simulation is done for the worst case fractional division ratio $N_{frac} = 1/2^n$, where n is the number of bits of the $\Delta\Sigma$ modulator used ($n = 10$ in this simulation). The figure also indicates the phase noise contribution of each block to the total phase noise.

3.3.1.2 PRE-DISTORTER

The DTC non-linearity causes a significant degradation in phase noise and spur level performance, as a result of imperfect cancellation of the quantization noise induced by the $\Delta\Sigma$ modulator. In addition, it also changes the shape of the quantization noise spectrum, an effect known as spectral regrowth [64]. The effects of the DTC non-linearities can be greatly alleviated with the aid of an adaptive pre-distortion technique implemented in the digital domain [4].

The relationship between DTC control word and the corresponding delay can be modeled by the function $f(x)$, shown in Figure 3.25. $f(x)$ represents the set of all integer values that can be taken by the variable x between $-M$ and M in the domain $X = \{-M,...,M\}$. The pre-distortion technique is based on mapping the domain X into a new domain $Y = \{\hat{y}_{-M},...,\hat{y}_M\}$ by a new function $\hat{y}(x)$. The new composition $f[\hat{y}(x)]$ has to guarantee the linear relationship $\xi x + \delta$, where ξ is the gain and δ is the intercept point for $x = 0$ [4]. The function $\hat{y}(x)$ can be formed under two conditions: a) f is monotonic b) $\hat{y}(x)$ is given by $f^{-1}(\xi x + \delta)$ where f^{-1} is the inverse of f [4] (see Figure 3.25).

The previous explanation is known as ideal pre-distortion, where $2M$ coefficients of the function $\hat{y}(x)$ have to be estimated. However, estimating this large number of coefficients is impractical, where a large number of digital accumulators and mixers has to be used [4]. Therefore, a piece-wise-linear operation can be adopted to approximate the inverse function, by considering only a finite number of points and using linear interpolation to estimate the remaining points. To do this, the DTC control word (as mentioned before) is split into two controlling words, x_1 for the coarse control word and x_2 for the

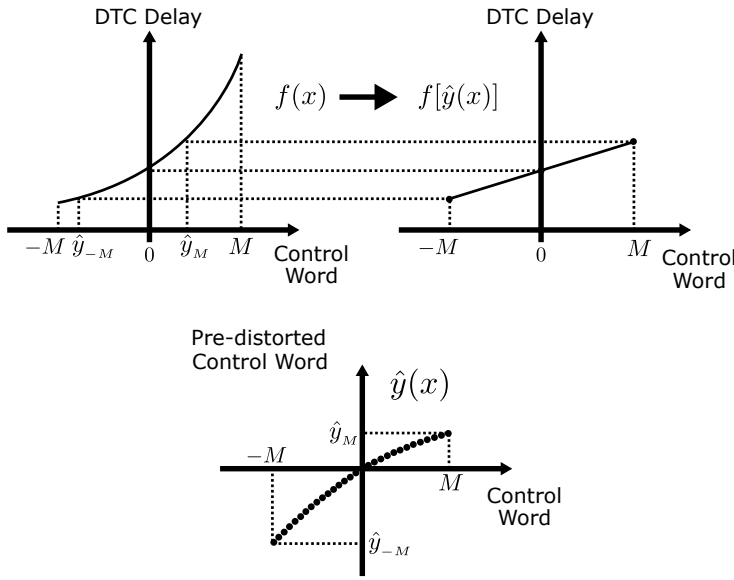


Figure 3.25 Ideal pre-distortion concept [4].

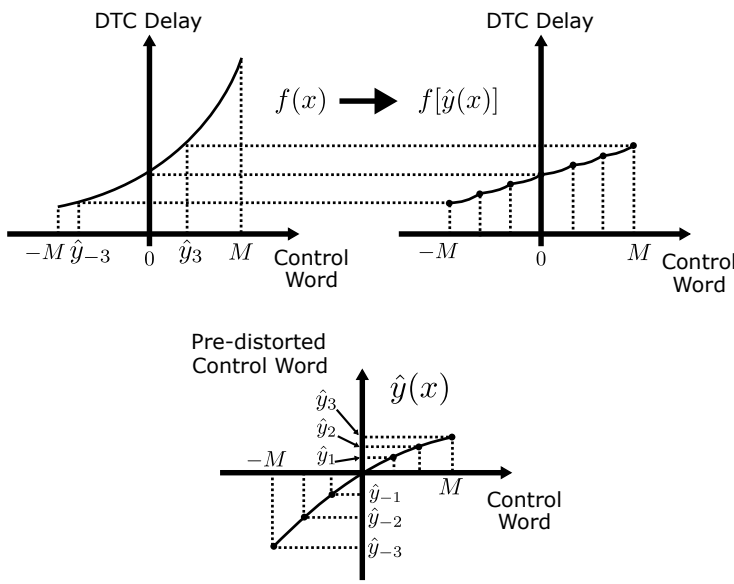


Figure 3.26 Pre-distortion based piece-wise-linear concept [4].

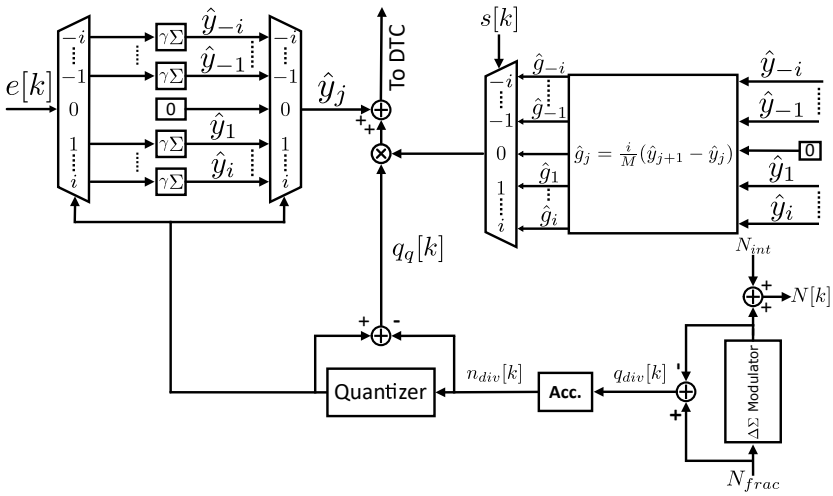


Figure 3.27 Block schematic view of the pre-distorter [4].

fine control word. The coarse control word is calculated as [4]

$$x_1 = \lfloor \frac{i}{M} x \rfloor \tag{3.66}$$

where $\lfloor\ \rfloor$ represents a floor operation. x_1 can take any integer value between $-i$ and i, with $i < M$. Therefore, only $2i$ coefficients have to be calculated for the estimation of the coarse function $\hat{y}_{x_1}$ and consequently the number of coefficients to be estimated is decreased from $2M$, as in the ideal case, to $2i$. Then, the function $\hat{y}(x)$ can be expressed as [4]

$$\hat{y}(x) = \hat{y}_{x_1} + \hat{g}_{y_{x_1}} x_2 \tag{3.67}$$

where the gains $\hat{g}_{y_{x_1}}$ are calculated from $\hat{y}_{x_1}$ by the following relationship [4]

$$\hat{g}_{y_{x_1}} = \frac{i}{M}(\hat{y}_{x_1+1} - \hat{y}_{x_1}) \tag{3.68}$$

Figure 3.26 shows the pre-distortion-based piece-wise-linear operation for the case of $i = 3$.

Figure 3.27 shows the pre-distorter schematic. The inverse characteristics of the DTC is estimated by firstly generating $n_{div}[k]$ from $q_{div}[k]$, then $n_{div}[k]$ is quantized to generate $s[k]$, which selects only one accumulator to generate $\hat{y}_j[k]$. On the other hand, the quantization error from the quantizer, $q_q[k]$, is corrected by the gain $\hat{g}_j[k]$, generated by the subtraction of two consecutive coefficients (chosen also depending on the value of $s[k]$) and the result is added

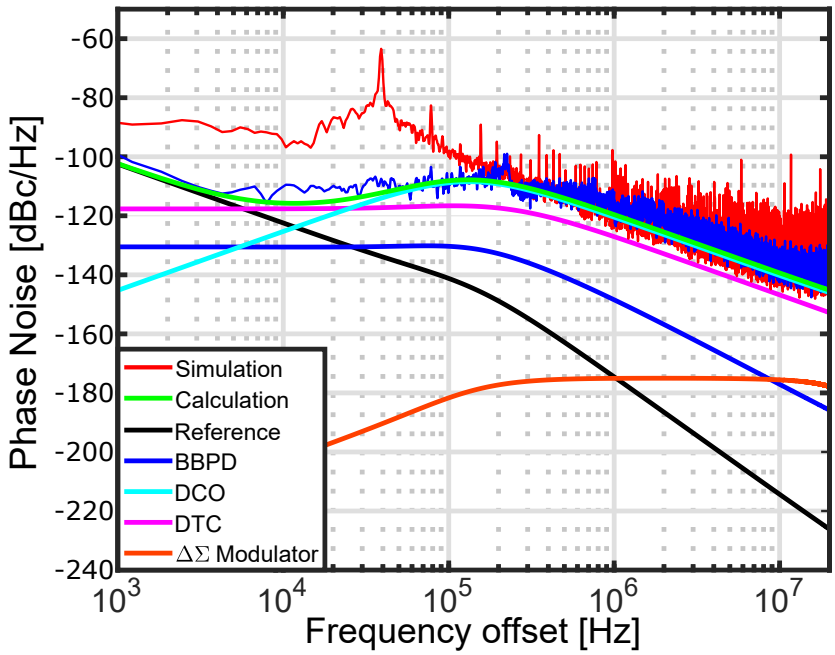
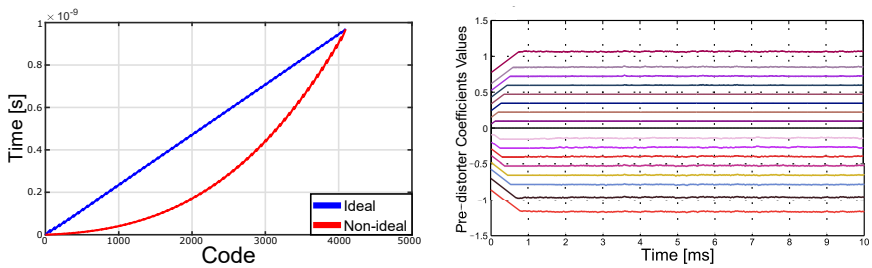


Figure 3.28 Matlab simulation of phase noise spectrum with enabling (blue line) and disabling (red line) the pre-distorter.



(a) (b)

Figure 3.29 (a) Ideal (blue line) and non-ideal (red line) DTC characteristic (b) Simulated transient of the pr-distorter coefficients.

to $\hat{y}_j[k]$ to generate the digital input code for the DTC coarse and fine control words.

The convergence speed of the estimated coefficients is also controlled by γ. Figure 3.28 shows the simulated phase noise at 3.0 GHz with a 40 MHz reference clock and a 10-bit pre-distorter with a third order non-linearity in the DTC characteristic curve (see Figure 3.29(a)). The simulation shows the huge difference in phase noise performance enabling (blue line) and disabling

(red line) the pre-distorter. The settling of some coefficients from start-up to final values is reported in Figure 3.29(b).

3.3.1.3 LOOP BANDWIDTH REGULATION

The BBPD gain in the random noise regime depends on the time jitter $\sigma_{\Delta t}$ at its input. Accordingly, this dependency makes the DPLL bandwidth also dependent on the amount of DPLL noise, which is not desirable. This problem is added to other causes of uncertainty in the bandwidth, such as DCO gain and PVT variations. Therefore, an adaptive background LBR, which makes the loop independent of the above mentioned factors, is needed [5].

A digital circuit, performing the automatic loop bandwidth regulation, can be implemented as shown in Figure 3.30. It uses the quantization noise of the 1st-order $\Delta\Sigma$ modulator driving the DCO to estimate the gain of the path from the DCO to the BBPD including the MMD, then dividing the BBPD output by that gain, to normalize the loop gain of the DPLL [5]. Estimating this gain starts by calculating the $\Delta\Sigma$ modulator quantization noise $q_{dco}[k]$, which is then fed to a digital integrator to provide the integrated quantization noise $n_{dco}[k]$. After the integration, the process continues to generate $g_{lbr}[k]$, which is the required estimated gain of the DCO-BBPD path. The estimated gain $g_{lbr}[k]$ is inverted by a digital divider to get $g_{lbr}^{-1}[k]$. Finally, $g_{lbr}^{-1}[k]$ is multiplied by $e[k]$ to normalize the loop gain and remove the dependency of the bandwidth on the above mentioned factors.

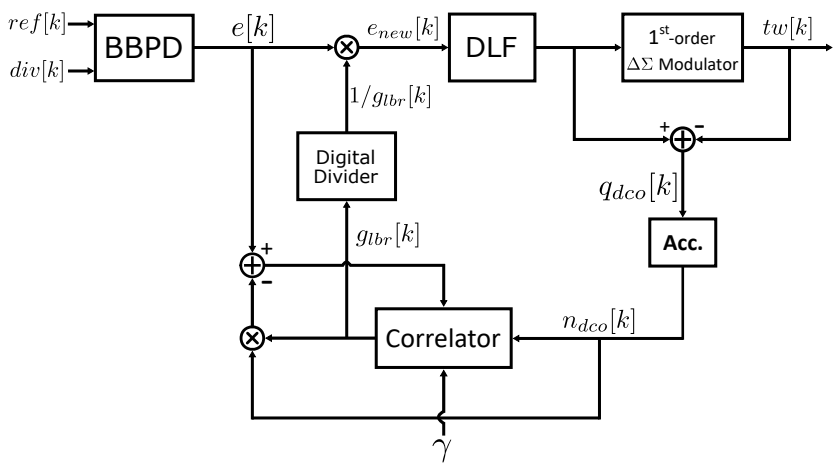


Figure 3.30 LBR schematic [5].

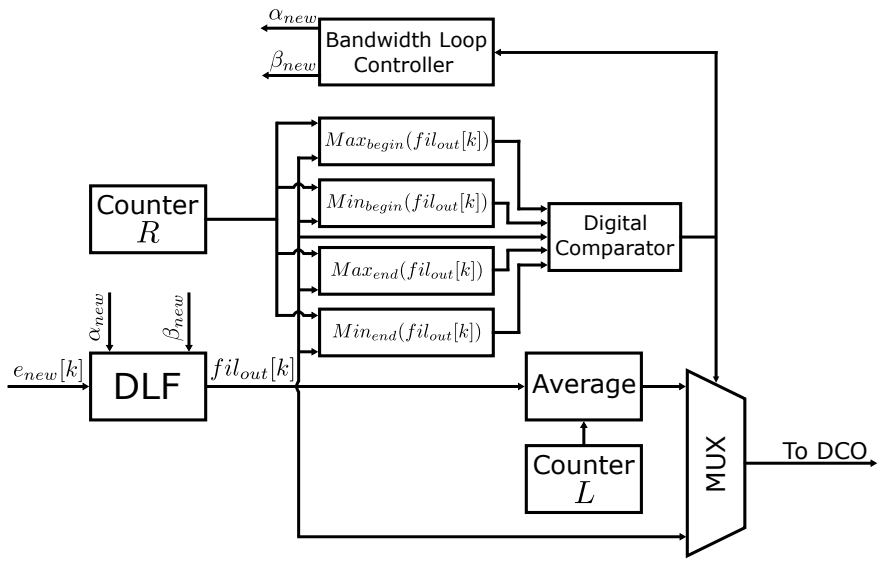


Figure 3.31 Proposed FAC scheme.

3.3.1.4 FREQUENCY ACQUISITION CONTROLLER

Since the BBPD has a very small detection range [35], an automatic FAC is needed. Figure 3.31 depicts the block diagram of the proposed automatic FAC architecture. The operation starts by increasing the loop bandwidth even at the expense of degraded phase noise and spurs performance, which are quite unimportant at this time. This operation is known as gear-shifting. The basic idea behind gear-shifting is to use a larger loop bandwidth during frequency acquisition, shifting the loop bandwidth to the normal value after the DPLL is locked. The maximum and minimum of the first and final R samples of the filter output $fil_{out}[k]$ during a certain measurement window L are saved. The following two conditions are tested

$$Min_{begin}(fil_{out}[k]) < fil_{out}[k] < Max_{begin}(fil_{out}[k]) \tag{3.69}$$

$$Min_{end}(fil_{out}[k]) < fil_{out}[k] < Max_{end}(fil_{out}[k]) \tag{3.70}$$

If these conditions are true, the digital comparator opens the Multiplexer (MUX) for the average of the filter output word to the DCO and at the same time the bandwidth loop controller generates new values α_{new} and β_{new} for the DLF to decrease the loop bandwidth. On the other hand, if one of these conditions is false, the process continues until the two conditions become true. The

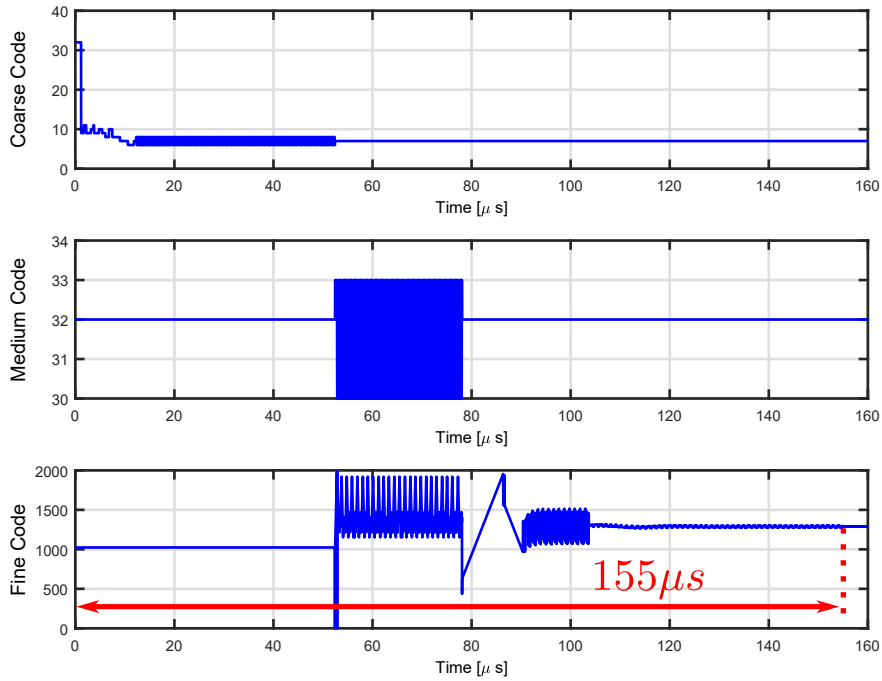


Figure 3.32 Simulation plots demonstrating the acquisition behavior of three DCO banks.

process continues by decreasing α_{new} and β_{new} until lock is achieved. Thereafter, the coefficients return back to their nominal values.

Figure 3.32 shows a simulation of the FAC behavior for a DCO with three banks: coarse, medium and fine. Coarse and medium banks are controlled by 6 bits each, while the fine bank is controlled by 11 bits. Lock is achieved after 160 μs at most.

4

Digitally Controlled Oscillator

An oscillator is an electronic circuit that produces a periodic output signal from a DC power at a desired frequency. Oscillators can be realized in many forms: ring oscillators, Inductor-Capacitor (LC)-tank oscillators, crystal oscillators, relaxation oscillators, etc.; however, for a typical RF wireless communication system, the differential cross-coupled LC-tank CMOS oscillator is often used, due to its excellent performance. A well designed oscillator must meet very stringent requirements, such as phase noise, power consumption, and tuning range, since its performance affects to a large extent the overall performance of the PLL. Therefore, the implementation of the cross-coupled LC oscillator has received a lot of attention in recent years, as illustrated by the large number of high quality publications reporting improved performance [8–11] [29] [65–72].

The core part of a PLL-based frequency synthesizer is a VCO. The frequency of the output signal of the VCO is determined by the control voltage that is continuously applied to it. Thereafter, the concept of a DCO was proposed as the digital counterpart of a VCO, where an interface with digital inputs is used to change the output frequency of the DCO. Therefore, DCOs deliberately avoid any analog tuning voltage, allowing the loop control circuitry to be implemented in a fully digital manner. However, except for the interface, the DCO core is essentially the same as that of a VCO. Therefore, both share the same key design consideration.

This chapter focuses on the fundamental theory of LC-tank oscillators and analyzes the advantages of this structure. Furthermore, commonly used design parameters are explained, with focus on those affecting the performance of PLLs in general and DPLLs in particular.

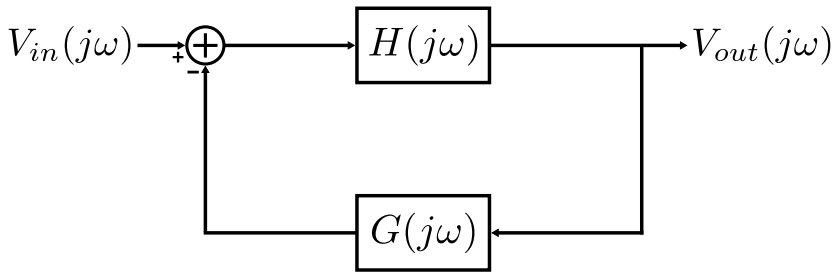


Figure 4.1 Feedback network.

4.1 OSCILLATOR FUNDAMENTALS

An oscillator can be described as a linear feedback network, as demonstrated in Figure 4.1, where $H(j\omega)$ and $G(j\omega)$ are the gains of the feed-forward and feedback network, respectively. This feedback viewpoint is very useful for the analysis of oscillators, and has been widely used to predict their behavior. Obviously, the overall transfer function of the complete network is

$$\frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{H(j\omega)}{1 + H(j\omega)G(j\omega)} \tag{4.1}$$

where $H(j\omega)G(j\omega)$ is the open loop gain. The open loop gain must fulfill the following necessary conditions, known as "Barkhausen criteria", in order to oscillate:

- **Gain condition:**

$$|H(j\omega_0)||G(j\omega_0)| = 1 \tag{4.2}$$

- **Phase condition:**

$$\angle H(j\omega_0)G(j\omega_0) = 180° \tag{4.3}$$

The gain and phase equations (4.2 and 4.3) pose the necessary conditions for steady-state oscillation. In a real-life oscillator, we need

$$|H(j\omega_0)||G(j\omega_0)| > 1 \tag{4.4}$$

Under this condition, the oscillator circuit amplifies its own noise at ω_0 and the oscillation can start. As a result, the oscillation amplitude increases. Due to saturation effects and non-linearities of the active devices used in the oscillator, the open loop gain falls back to unity, and the oscillation amplitude comes to a steady-state value. However, in reality, gain is a concept of linear circuits, but oscillators are very non-linear.

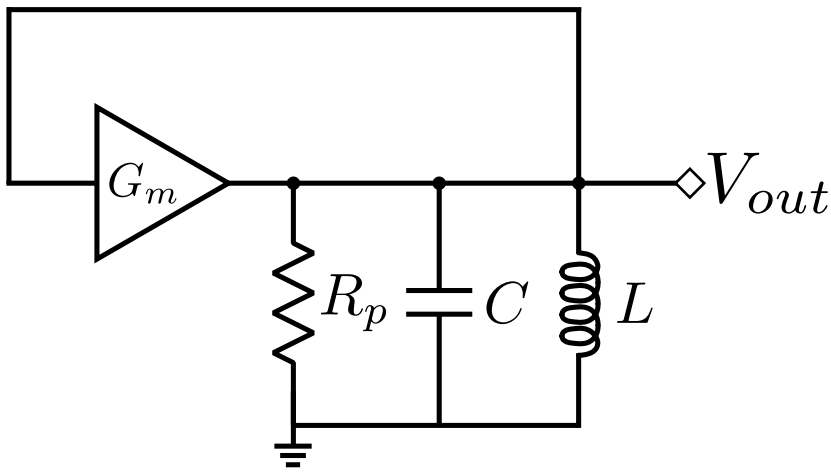


Figure 4.2 LC oscillator negative resistance model.

4.2 LC-TANK OSCILLATOR

In order to obtain stringent phase noise performance for cellular and wireless communication devices, LC oscillators are preferred. An LC oscillator generally consists of an inductor and a capacitor, in series or in parallel. LC oscillators exhibit a very good phase noise performance, compared to ring oscillators. Thus, this work focuses on LC oscillators. The following sections introduce the basic concept of the LC oscillator in general, and cross-coupled differential pair architecture in particular.

4.2.1 PRINCIPLES OF LC-TANK OSCILLATOR

To describe the fundamental operation of LC oscillators, we may use the concept of negative resistance, illustrated in Figure 4.2. This model can be regarded as a special case of the feedback model, where the feedback transfer function $G(j\omega)$ is replaced by an LC network, while the feed-forward transfer function $H(j\omega)$ is replaced by an active circuit with a transconductance G_m. The LC network forms a resonator that selects the frequency of oscillation. The LC resonator circuit essentially amplifies the noise in the circuit, feeds back this amplified noise, and then adds it back to the input, while the energy is transferred back and forth between the inductor and capacitor. This periodic exchange of energy between inductor and capacitor continues forever, generating a continuous oscillating signal. However, this happens only when both components are lossless. In practice, ideal inductors and capacitors are not physically attainable because they have losses; therefore, when energy is

transfered between inductor and capacitor, there is some loss. The total losses in the LC-tank can be modeled by a resistor, R_p, in parallel with the tank, which dissipates some energy every cycle, causing a decay in the amplitude of the resonant signal. To achieve steady-state oscillation, the active element should be designed such that it has enough gain to replenish the energy lost from R_p. In other words, the active circuit performs, in average, as a negative resistor $-R_p$ to cancel out R_p.

The oscillation frequency of the LC oscillator can be derived from Barkhausen criteria as

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{4.5}$$

4.2.2 CROSS-COUPLED DIFFERENTIAL PAIR

LC oscillators can be categorized depending on how the active circuit is implemented. Therefore, it is possible to implement an oscillator using single active devices in traditional topologies such as Hartley, Colpitts and Pierce. Nonetheless, most realizations of LC oscillators utilize differential realizations. Although they double the power consumption, they have attractive properties, such as their ability to provide a higher degree of common-mode noise rejection in terms of power supply and substrate noises that are often presented in on-chip power rails. Added to that, many integrated RF systems benefit from employing a differential oscillator, since typical integrated mixers utilize differential topologies. Therefore, differential oscillator topologies eliminate the need for a single-ended to differential conversion circuit. The most common differential oscillator topologies are the ones that utilize the cross-coupled differential pair, which uses two cross-coupled transconductors to generate the negative resistance of Figure 4.2. In CMOS technology, depending on the transistor type used to build the cross-coupled pair, three architectures are recognized: NMOS-only, PMOS-only and CMOS oscillator, as shown in Figure 4.3.

In an NMOS-only topology, the cross-coupled pair is formed by NMOS transistors only, while in a PMOS-only topology, only PMOS transistors are used to form the cross-coupled pair. The CMOS topology uses a combination of both NMOS and PMOS transistors to form the cross-coupled pair. Each topology has its own trade offs, and it depends on the designer to select the appropriate topology for the system. The NMOS-only topology requires less area compared to the PMOS-only architecture, as to produce the same transconductance, larger PMOS transistors are needed, since the electron mobility for NMOS transistors are higher than for PMOS transistors. Consequently, the parasitic capacitances in NMOS-only oscillators are smaller than those using PMOS differential pair. Hence, the NMOS-only architecture provides larger achievable TR and higher oscillation frequency. The NMOS-only and PMOS-

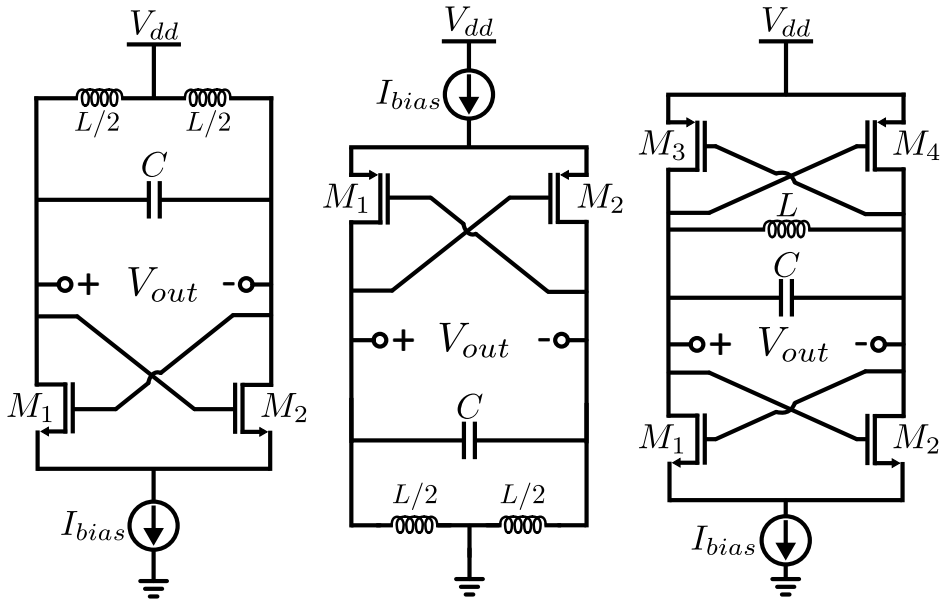


Figure 4.3 Simplified circuits schematic of cross-coupled differential pair architectures for a) The NMOS-only architecture b) The PMOS-only architecture and c) The CMOS architecture.

only architectures produce the higher output voltage swing between cross-coupled topologies, which theoretically is up to twice the supply level, since the utilized inductor is either tied to the supply voltage, as in the NMOS-only topology, or to the ground, as in the PMOS-only topology. This property is very important for minimizing the phase noise by maximizing the output signal [73]. However, NMOS transistors have higher flicker noise compared to PMOS ones [74] and thus they are contributing a considerable amount of up-converted $1/f$ noise to the phase noise. On the other hand, CMOS oscillators have the lowest current consumption in comparison to the other two types, to generate the same transconductance value. Nonetheless, this architecture suffers from headroom issues, as the PMOS differential pair has to be stacked.

4.3 REVIEW OF EXISTING PHASE NOISE MODELS

Besides Leeson's model, described in Chapter 2, various models have been developed to explain and describe phase noise in oscillators. In this section, two

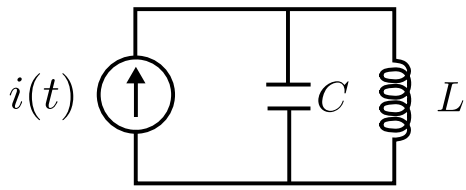
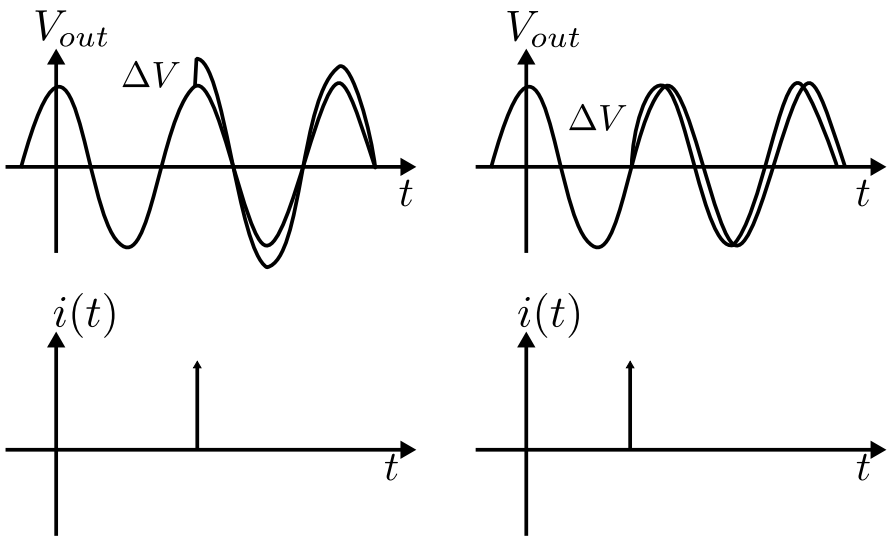


Figure 4.4 Current noise impulse model [6].



(a) Impulse injected at the peak. (b) Impulse injected at the zero crossing.

Figure 4.5 impulse injected at different times [6].

models proposed in [6] [7] are briefly explained, and their fundamental phase noise equations are shown.

4.3.1 HAJIMIRI AND LEE'S PHASE NOISE MODEL

This theory has been presented by Ali Hajimiri and Thomas Lee [6], where they attempt to give a quantitative explanation of the phase noise in oscillators. The main idea is that a current noise source injecting charges into the oscillator has a different impact on the oscillator phase over the oscillator period. Suppose an injected noise source can be modeled as current impulses in the time domain, as shown in Figure 4.4. If the current noise impulse occurs at the top of the voltage waveform, the amplitude will increase suddenly. Accordingly, the

instantaneous voltage change ΔV is given by

$$\Delta V = \frac{\Delta q}{C_{tot}} \tag{4.6}$$

where Δq is the total charge from the injection due to the current impulse and C_{tot} is the total capacitance at that node. If the impulse is injected at the oscillation peak, the only change in the oscillation waveform will occur on the amplitude, not the phase, as shown in Figure 4.5(a). However, suppose now that this impulse is injected at the zero crossing of the oscillation waveform. In this case, a change in both amplitude and phase occur, but with maximum effect on phase and zero (ideally) effect on amplitude, as shown in Figure 4.5(b). As can be seen, the assumption of time, invariance in the conversion of noise into phase noise, does not hold. Therefore, Hajimiri and Lee introduced a Linear Time Variant (LTV) phase noise model.

A so-called time-domain Impulse Sensitivity Function (ISF), Γ, is introduced to characterize the noise impact over the period. The ISF is a dimensionless, frequency-and amplitude-independent periodic function with period 2π, which describes how much phase shift results from applying a unit impulse at time $t = \tau$. The ISF can be expressed as a Fourier series as

$$\Gamma(\omega_0\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n cos(n\omega_0\tau + \theta_n) \tag{4.7}$$

where c_n and θ_n are real-valued coefficients, and n is the th harmonic index. If $i(t)$ is a (cyclo)stationary white current noise source, it can be shown that the phase noise is given by

$$L(\Delta\omega) = 10\log[\frac{1}{2}\frac{KT}{V_{max}^2}\frac{1}{R_p(C\omega_0)^2}(\frac{\omega_0}{\Delta\omega})^2] \tag{4.8}$$

where V_{max} is the maximum voltage swing across the tank.

4.3.2 PEPE AND ANDREANI'S PHASE NOISE MODEL

This model is based on a small-signal noise analysis performed around the Periodic Steady State (PSS) of the oscillator, where the time-variant transconductance of the active core is expressed as a Fourier series [7]. The model is shown in Figure 4.6. The phase noise can be derived in terms of the resonator impedance and the large-signal PSS, and independently of transconductance terms, if the resonator voltage-to-current ratio is expressed directly through the resonator admittance.

The phase noise calculation relies on a matrix formulation of the oscillator PSS, where the basic concepts of matrix algebra in terms of eigenvalues

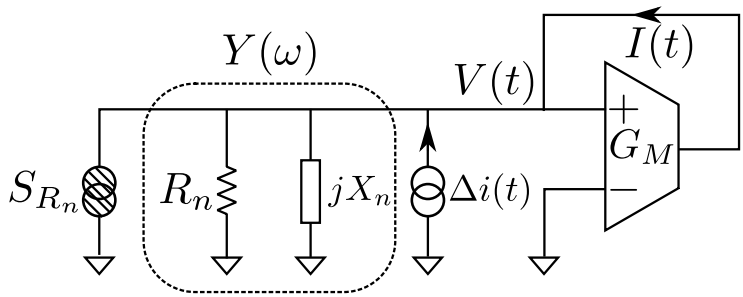


Figure 4.6 Basic schematic view of the transconductor-based oscillator [7].

and eigenvectors are used. An important note is that the oscillator PSS owns one eigenvalue equal to zero. This eigenvalue dominates the behavior of the whole system. Accordingly, the phase noise superimposed onto the PSS is estimated by applying the theory of perturbed eigenvalues to that zero eigenvalue. Thereafter, the phase noise caused by the resonator, the transconductance, and the total phase noise can be expressed, respectively, as

$$L_{res} = 10\log[2k_BT\frac{\omega_o^2}{\|\overrightarrow{DV}\|^2}|\frac{1}{\delta\lambda_1}|^2\overrightarrow{LV}_1^T.Re(\boldsymbol{Y}).\overrightarrow{LV}_1^*] \tag{4.9}$$

$$L_{gm} = 10\log[2k_BT\gamma\frac{\omega_o^2}{\|\overrightarrow{DV}\|^2}|\frac{1}{\delta\lambda_1}|^2\overrightarrow{LV}_1^T.\tilde{\boldsymbol{G}}.\overrightarrow{LV}_1^*] \tag{4.10}$$

$$L_{tot} = 10\log[2k_BT\frac{(1+\gamma)\omega_o^2}{\|\overrightarrow{DV}\|^2}|\frac{1}{\delta\lambda_1}|^2\overrightarrow{LV}_1^T.Re(\boldsymbol{Y}).\overrightarrow{LV}_1^*] \tag{4.11}$$

where $\boldsymbol{Y}$ stores the admittances of the resonator at the different harmonics, $\tilde{\boldsymbol{G}}$ performs the convolution between the harmonic terms of instanteneous transconductance $g(t)$ and $\Delta v(t)$ ($\Delta v(t)$ is the small-signal voltage arising in response to $\Delta i(t)$), and the vector $\overrightarrow{DV}$ stores the harmonics of $dV(t)/dt$, while $\overrightarrow{LV}_1$ is

$$\overrightarrow{LV}_1 = \frac{\overrightarrow{DV}^*}{\|\overrightarrow{DV}\|.} \tag{4.12}$$

4.4 OSCILLATOR PERFORMANCE PARAMETERS

Oscillators have several important performance characteristics beside phase noise that are typically described by the following parameters:

- **Center Frequency:** The center frequency is the mid-range value in the characteristic curve of the oscillator and is specified by the targeted application. Usually, the center frequency is influenced by PVT variations, thus a wide enough TR is desirable.
- **Tuning Range:** It is the range of frequencies generated by the oscillator. It is defined by the difference between the maximum and the minimum frequency that the oscillator can achieve and is usually measured in percentage of the center frequency.
- **Power Consumption:** It is a critical issue for most battery operated systems, where low power consumption is very important for long battery life. Hence, the less power consumed for a certain performance, the more efficient the oscillator.
- **Frequency Resolution:** It is a performance characteristic specified only for DCOs. It is defined as the minimum possible frequency step at the DCO output.
- **Frequency Tuning Non-Linearity:** The output frequency is expected to be linearly proportional to the input control value; however, the tuning characteristics usually exhibit non-linearity behavior. The non-linear tuning characteristics of the oscillator can cause a performance degradation in the PLL using that oscillator [75]. Therefore, the frequency tuning non-linearity should be minimized as much as possible.
- **Frequency Pulling:** It is another challenging problem for LC oscillators, caused by the magnetic coupling between different inductors, causing a frequency modulation on the oscillator signal, especially when integrated on the same chip.
- **Size and Integrability:** They are important for high density integration to bring the cost down, therefore oscillator area has to be designed as small as possible.

In the upcoming sub-sections, frequency tuning range, frequency resolution and frequency pulling are illustrated in more details.

4.5 FREQUENCY TUNING OVERVIEW

Most oscillators are designed such that their frequency can be tuned over a certain frequency range. This is important not only to cover the whole application bandwidth, but also to compensate for frequency variations that are caused by the PVT variations. Moreover, a wide frequency tuning is often

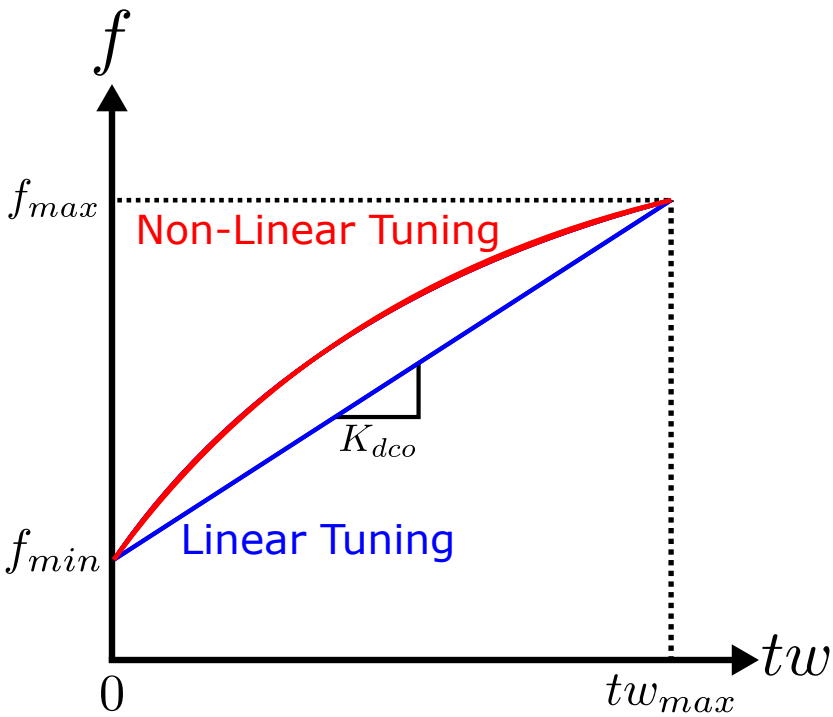


Figure 4.7 DCO tuning curves.

needed to support different cellular communications standards with more and more frequency bands.

Ideally, the DCO output frequency is linear vs its tuning digital control input tw. The relationship between the output frequency f_{out} and tw can be expressed as

$$f_{out} = f_r + K_{dco}.tw \tag{4.13}$$

where f_r is the DCO free running frequency and K_{dco} is the DCO gain. Nonetheless, for realistic designs of DCOs, designers have to deal with non-ideal factors that make the above relationship not linear any more. One main factor that causes non-linear DCOs is the mismatch between the components. The tuning curves of linear and non-linear DCO are shown in Figure 4.7.

Another important issue due to the DCO's natural discrete tuning is the quantization noise, which degrades the noise performance. A reduced frequency step improves the phase noise, but makes the frequency range too narrow. Alternatively, a large number of steps can be used, but with more and more circuit complexity. To solve this issue, the DCO tuning is usually divided at least into three levels of tuning: coarse, medium and fine. The coarse and

medium tuning ensure a wide frequency range, while the fine tuning provides high frequency resolution.

In the next two sub-sections, wide frequency tuning range and frequency resolution techniques are explored and summarized, showing the advantages and drawbacks of each technique.

4.5.1 WIDE FREQUENCY TUNING RANGE TECHNIQUES

As mentioned in (4.5), the resonance frequency ω_0 can be controlled by changing either the inductance value L or the capacitance value C. Using multiple oscillators to achieve an ultra-wide overall TR via overlapping TRs is one possible solution, but at the same time it increases the area by a large amount. Another method is to use switched capacitors and MOS switches. In this case, there is a trade-off between phase noise and TR. To achieve a good phase noise, wide MOS switches should be used to decrease the on-resistance and maintaining a good quality factor. On the other hand, the larger the MOS switches, the larger the off-state parasitic capacitances, which limits the maximum oscillation frequency. This can be counteracted by scaling down the tank inductance value, increasing however the power consumption at the lower oscillation frequencies; at the same time, it is also impractical to scale down the inductor size [9]. In the next sub-sections some wide-band DCO architectures are reviewed.

4.5.1.1 DUAL-CORE DCO

A wide TR can be achieved by using a double-core oscillator with two concentric 8-shaped inductors occupying the same area [8]. Figure 4.8 shows a hybrid schematic/layout view of the dual-core DCO. The architecture employs two 8-shaped inductors. As illustrated in the figure, the smaller 8-shaped coil is rotated by 90° and placed inside the larger 8-shaped coil in a concentric, symmetric way. This architecture uses two cross-coupled transistor pairs and two capacitor banks to perform two modes of operation: High-Band (HB) and Low-Band (LB). Each mode uses its own cross-coupled pair and capacitor bank. 8-shaped inductors are used, since they do not interfere with each other, as they reject any common-mode magnetic field because of geometric symmetry, while they also generate a magnetic field that vanishes far from the coils due to their twisted nature [10] [76–79].

Measurement results shows an oscillation between 2.4 GHz and 3.6 GHz with TR = 40% in LB mode, while an oscillation between 3.4 GHz and 5.3 GHz with TR = 43% in HB mode, for a total TR of 75%. This architecture uses less area, compared to two independent oscillators with overlapping TRs, but damages somewhat the Q of the inductors.

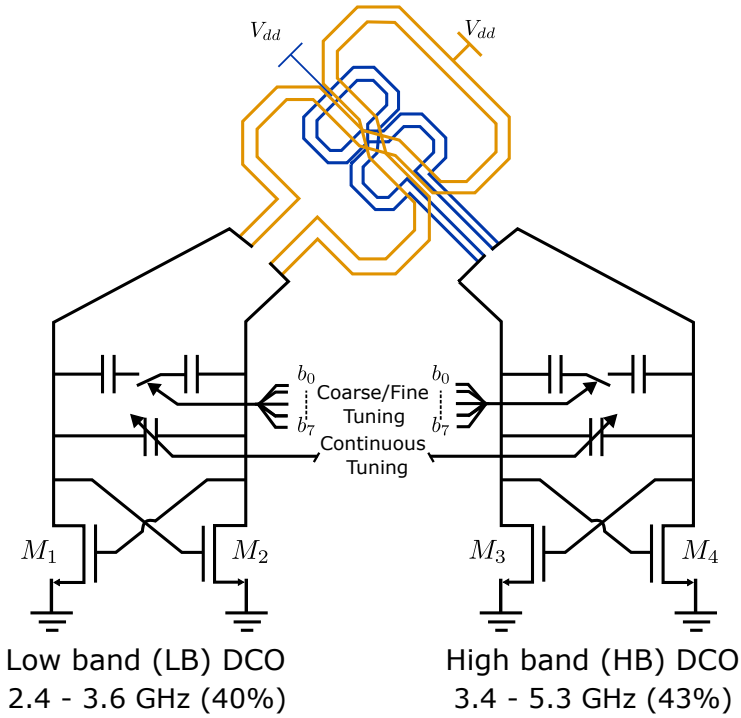


Figure 4.8 Hybrid schematic view of the dual-core DCO [8].

4.5.1.2 TRANSFORMER-BASED DCO

Another possibility is the transformer-based oscillators [9] [65–67] [80], which uses two LC tanks connected by a transformer. An example of this type is proposed in [9] and shown in Figure 4.9. This architecture uses an LC resonator with two identical LC tanks coupled through the magnetic coupling M and the capacitive coupling C_c. Two resonant operation modes arise:

- **Even-mode:** in this mode, the LC voltages and currents in the two coils have the same amplitude and are in phase. Figure 4.10(a) illustrates the even-mode operation, where the capacitors C_c have a zero voltage drop and therefore there is no current flow through them. Consequently, they have no effect on the operation. Since, the currents in the two coils are in phase, the effective inductance in this mode is equal to $L+M$ for both LC tanks. Hence, the even-mode resonant frequency is

$$\omega_{even} = \frac{1}{\sqrt{(L+M)C}} \tag{4.14}$$

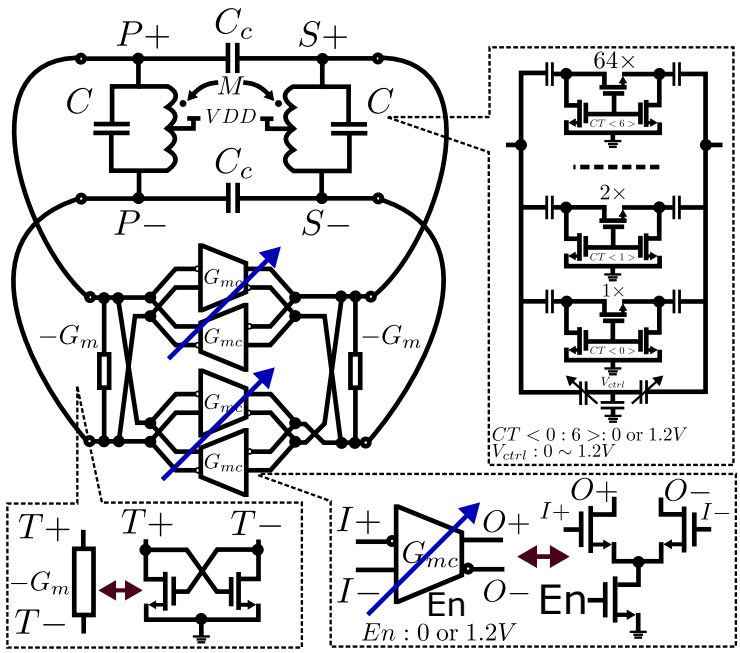
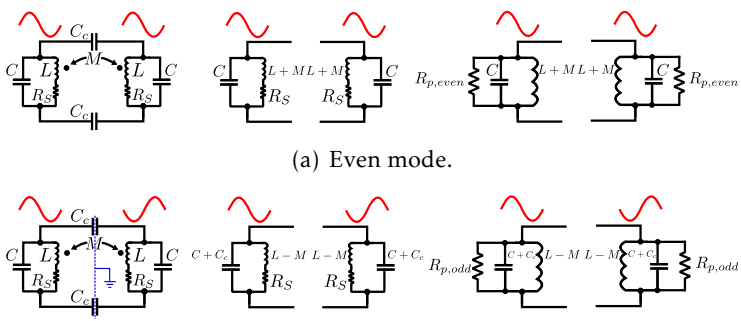


Figure 4.9 The transformer-based DCO architecture proposed in [9].



(a) Even mode.

(b) Odd mode.

Figure 4.10 The two resonant modes of the LC resonator [9].

- **Odd mode:** in this mode, the LC voltages and currents in the two coils, have the same amplitude but are 180° out of phase. Hence, in this case the capacitors C_c see differential voltage and accordingly each LC tank sees a series of two C_c. Therefore, the effective capacitance becomes $C+C_c$, as shown in Figure 4.10(b). The effective inductance is translated

to be $L-M$. Consequently, the odd-mode resonant frequency is

$$\omega_{odd} = \frac{1}{\sqrt{(L-M)(C+C_c)}} \tag{4.15}$$

By assuming that the series resistance R_s of the two coils dominates in the resonator's energy loss, the equivalent parallel resistance $R_{p,even}$ in the even mode can be calculated as

$$R_{p,even} \approx \frac{[\omega_{even}(L+M)]^2}{R_s} = \frac{L+M}{CR_s} \tag{4.16}$$

While the equivalent parallel resistance $R_{p,odd}$ in the odd mode can be calculated as

$$R_{p,odd} \approx \frac{[\omega_{odd}(L-M)]^2}{R_s} = \frac{L-M}{(C+C_c)R_s} \tag{4.17}$$

where C_c is always positive, but M can take positive or negative values. However, negative M is preferred for two reasons:

1. As illustrated in (4.14) and (4.15), negative values of M decrease ω_{odd} and increase ω_{even}, which improves the C_c's effect in increasing the separation of the two frequencies.

2. As explored in (4.16) and (4.17), negative values of M can be used to make $R_{p,even} = R_{p,odd}$ in order to achieve a balanced performance in the two modes.

Measurement results show that a TR between 2.48 GHz to 5.62 GHz can be achieved with this architecture. Using transformer-based DCO techniques results in a good phase noise and a wide TR, but unfortunately it uses two LC tanks instead of a single one, and also it is difficult to design an 8-shaped transformer.

4.5.1.3 SWITCHED INDUCTORS DCO

It is also possible to use switched inductors instead of switched capacitors [10]. Switched-inductors operation can be achieved, as proposed in [10], through using two coils: primary and secondary. The secondary has two states: open or short-circuited. The tank coil reduces to the primary circuit when the secondary is open, while when the secondary is short-circuited, the tank coil has a value of $L_p(1-k^2)$, where L_p and k are the inductance of the primary and coupling coefficient between primary and secondary, respectively.

Figure 4.11 shows the coils implementing the variable inductor, whereas Figure 4.12 shows the secondary coil. The figure also shows the wide NMOS

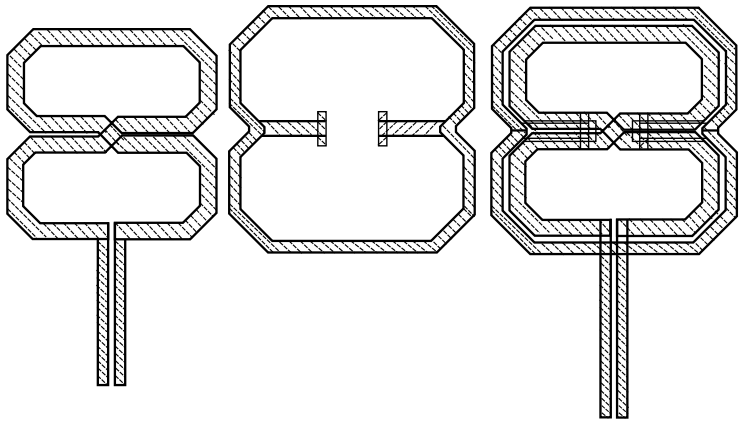


Figure 4.11 (left) primary circuits; (middle) secondary circuit; (right) transformer implementing the two-step variable inductance [10].

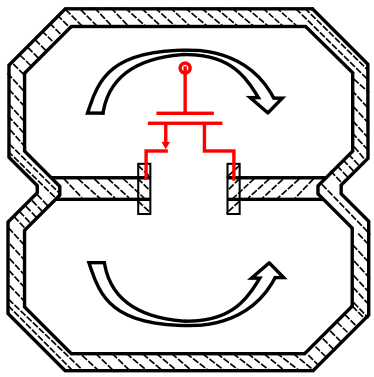


Figure 4.12 When the switch is open, no current is flowing across the secondary circuit [10].

switch used to open or short-circuit the secondary coil. When the switch is open, the secondary works as a single short-circuited loop, but with no current flowing through it, where the 8-shaped primary induces opposite fields in the two halves of the secondary loop. On the other hand, when the switch is closed, the secondary is translated to two identical independent loops, and the equivalent inductance in this case, as mentioned before, is $L_p(1-k^2)$ instead of L_p in the first case. Measurements show that a TR of 2.62 GHz to 3.93 GHz is achieved, when the secondary is open, while a TR of 4.90 GHz to 5.75 GHz is achieved, when the secondary is short-circuited.

By using this architecture, large TR becomes possible, but unfortunately it

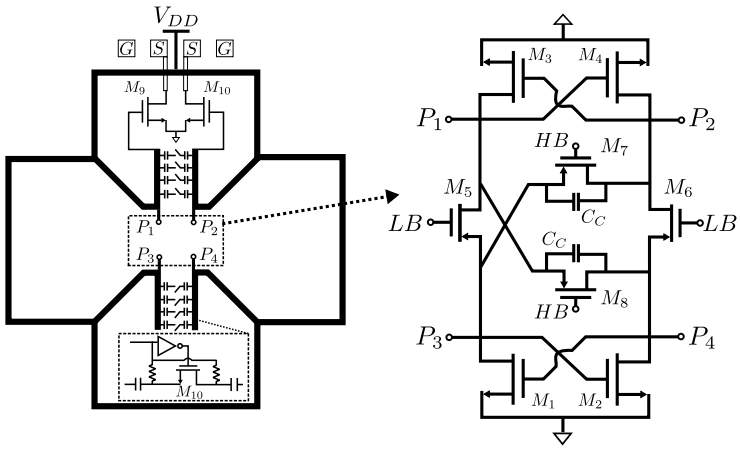


Figure 4.13 Circuit schematic of a mode-switching DCO [11].

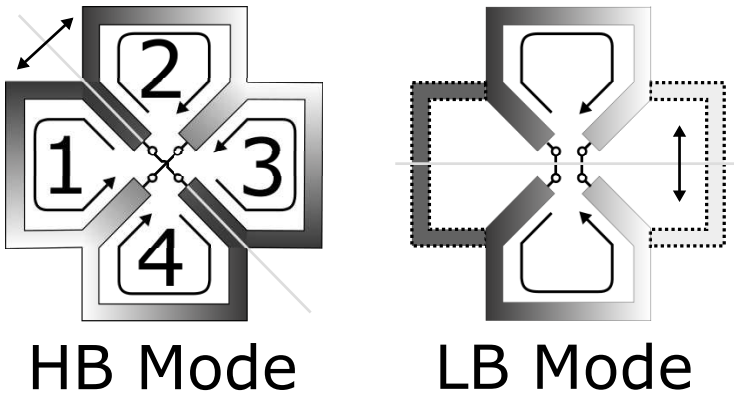


Figure 4.14 The two modes of the mode-switching DCO [11].

is difficult to achieve a low phase noise at reasonable power consumption (i.e., a high FOM) and a degradation performance occurs due to the Q degradation as a result of inductor switch ohmic losses.

4.5.1.4 MODE-SWITCHING DCO

Figure 4.13 shows the architecture of the mode-switching DCO [11]. It consists of a clover-shaped inductor with four identical lobes, two pairs of cross-coupled NMOS transistors $M_{1,2,3,4}$ to provide negative resistance, a mode-switching network consisting of PMOS transistors $M_{5,6,7,8}$, two coupling capacitors C_C, and a coarse capacitor bank. Also the oscillator has two modes,

namely, LB and HB. LB mode is chosen, when the gates of M_5 and M_6 are grounded and M_7 and M_8 are connected to V_{DD}. By doing that, the terminal P_1 is short-circuited to P_3 and P_2 is short-circuited to P_4. Therefore, the inductor in lobes 1 and 3 have no oscillation, as shown in Figure 4.14, where the oscillation exists in lobes 2 and 4. The LB resonant frequency is equal $1/2\pi\sqrt{L_{LB}(C+C_C)}$ where C is the total capacitance of all the blocks in the oscillator.

The contrary happens in HB mode, where to select this mode the gates of M_5 and M_6 are connected to V_{DD}, while M_7 and M_8 are grounded. Therefore, the terminal P_1 is short-circuited to P_4 and P_2 to P_3. In this mode, all the four lobes of the inductor contribute to the overall inductance. Figure 4.14 shows the direction of AC current in the four lobes. In HB mode, each loop inductor is coupled to its two adjacent neighboring loops. Hence, the total inductance seen between terminals $P_{1,4}$ and $P_{2,3}$, namely L_{HB}, is larger than $1/4$ of a single loop inductor by a factor of $(1+k)$, where k is the effective coupling coefficient of the system of 4 coupled loops. The HB resonant frequency is equal $1/2\pi\sqrt{L_{HB}C}$.

Measurement results shows the TR of the LB mode is from 3.24 GHz to 4.9 GHz, while it is from 4.5 GHz to 8.45 GHz in HB mode. Therefore, the total TR is between 3.24 GHz to 8.45 GHz. Unfortunately, this technique requires a very large area.

4.5.2 FINE TUNING TECHNIQUES

Due to the natural discrete tuning of the DCO, like any discrete system, it suffers from quantization noise, which degrades the total phase noise performance, as mentioned before. Therefore, it is mandatory to study the impact of the DCO quantization noise, due to the finite DCO frequency resolution Δf_{res}. The DCO can be modeled as shown in Figure 4.15(a). The infinite precision control word tw is quantized to a finite precision control word depending on Δf_{res}. Thereafter, a simplified model can be achieved, shown in Figure 4.15(b), by replacing the quantization noise coming from the quantizer by an additive uniformly distributed random variable $\Delta f_{n,0}$ with white noise spectral characteristics [12]. The phase noise resulting from the DCO finite resolution at offset Δf is given by [12]

$$L(\Delta f) = \frac{1}{12}\left(\frac{\Delta f_{res}}{\Delta f}\right)^2 . \frac{1}{f_{ref}} . \left(\operatorname{sinc}\frac{\Delta f}{f_{ref}}\right)^2 \tag{4.18}$$

where f_{ref} is the reference frequency of the DPLL. The DCO should be designed such that the quantization-induced phase noise is well below the DCO inherent phase noise. This can be achieved in two ways, according to (4.18):

- **Increasing the reference frequency:** In this way a reduction of 3 dB in

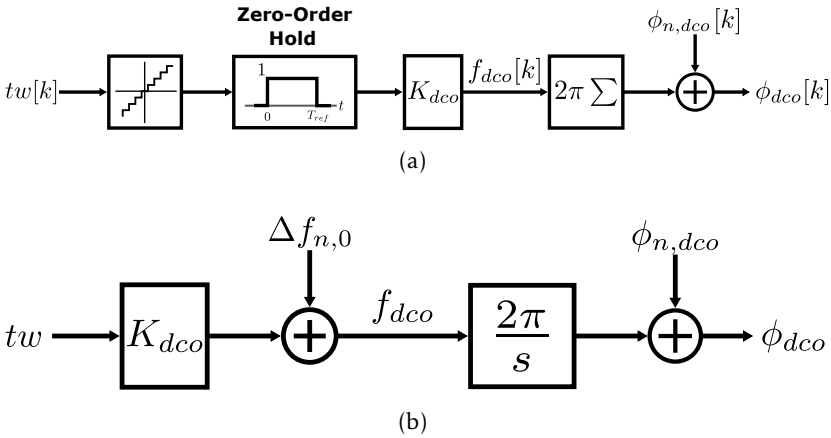


Figure 4.15 DCO quantization noise model [12].

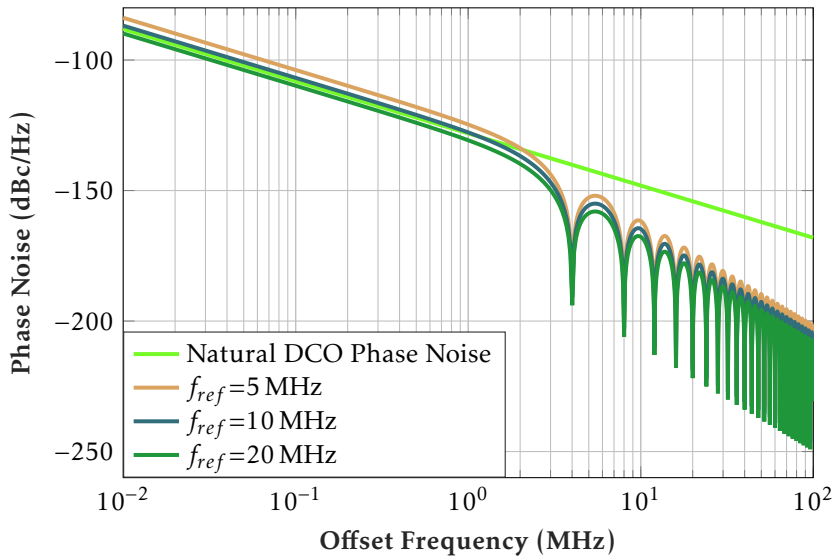
quantization-induced phase noise can be achieved by doubling the reference frequency. However, the choice of the reference frequency is usually restricted by various system requirements. Figure 4.16(a) shows a simulation explaining the impact of increasing f_{ref} on the quantization-induced phase noise. The figure shows also the simulated phase spectrum taking into account only the -20 dB/dec phase noise component.

- **Increasing the DCO frequency resolution:** In this way a reduction of 6 dB in quantization-induced phase noise can be attained by increasing the frequency resolution by two, as illustrated by the reduction achieved in Figure 4.16(b). In this example Δf_{res} is decreased until the DCO phase noise becomes dominant. After reaching that, no more reduction in Δf_{res} is needed.

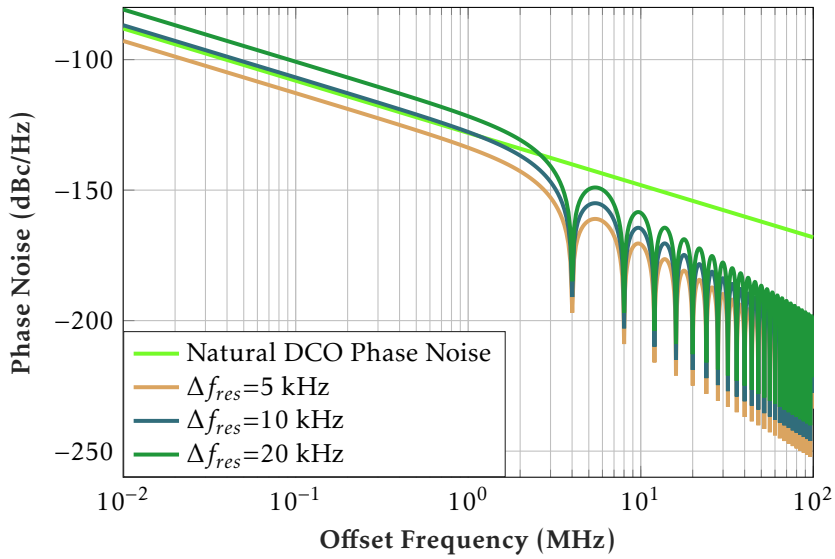
Obviously, a higher frequency resolution is the best choice to avoid the DCO quantization noise problem. Hence, several topologies have been introduced to increase the frequency resolution, and each technique has its own advantages and disadvantages that the designer should be aware of. Next, some methods for higher frequency resolution are discussed, illustrating the strongest and weakness properties for each technique.

4.5.2.1 $\Delta\Sigma$ MODULATOR DITHERING

A widely used method for improving the DCO frequency resolution is $\Delta\Sigma$ modulator dithering [12]. Dithering involves placing a high speed $\Delta\Sigma$ modulator between the DLF and the DCO to switch the capacitors on and off to reduce the effective DCO quantization step. Therefore, on average, the effective



(a) Phase noise spectrum due to changing f_{ref} with fixed Δf_{res}=5 kHz.



(b) Phase noise spectrum due to changing Δf_{res} with fixed f_{ref}=40 MHz.

Figure 4.16 Matlab simulations showing the effect of changing f_{ref} and Δf_{res} on the DCO quantization-induced phase noise.

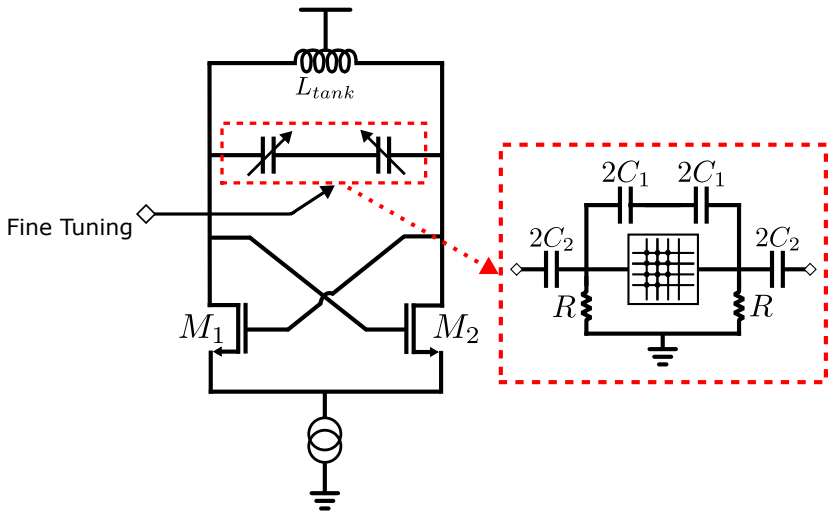


Figure 4.17 Capacitive divider scheme [13].

value achieved would seem to be a fractional number between the two capacitors value being involved, resulting in better resolution. The high speed clock for the $\Delta\Sigma$ modulator is derived from the divided DCO signal. This technique in principle is similar to adding the fractional functionality in PLLs through a $\Delta\Sigma$ modulator.

Dithering, however, requires a high speed $\Delta\Sigma$ modulator, leading to a higher degree of power consumption and complexity. Furthermore, depending on the dithering frequency, the out-of-band phase noise would increase due to the high-pass noise transfer function of the $\Delta\Sigma$ modulator, and it is difficult to keep it below the thermal phase noise.

4.5.2.2 CAPACITIVE DIVIDER TECHNIQUE

Another possible solution is the use of a capacitive divider technique [13], which is used to obtain a reduction of the minimum effective tunable unit capacitance through parallel and series combinations of fixed capacitors with digital tuning varactors, as shown in Figure 4.17. Three devices are needed to implement this technique: fine tuning varactor bank, capacitors C_1 in parallel to the varactor bank and series coupling capacitors C_2. The equivalent capacitance ΔC_{eq} that can be achieved becomes [13]

$$\Delta C_{eq} \approx \left(\frac{C_2}{C_1 + C_2}\right)^2 \Delta C \tag{4.19}$$

where ΔC is the capacitance step when a unit varactor is switched.

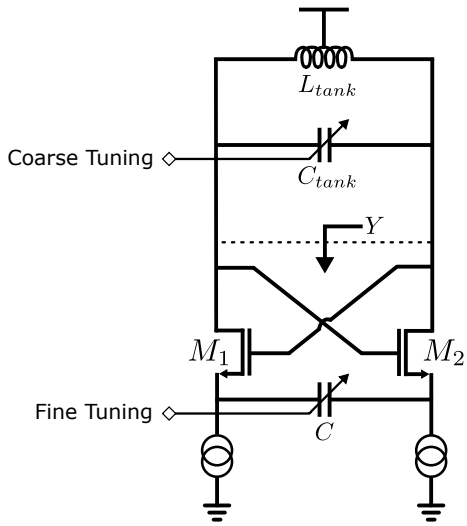


Figure 4.18 Capacitively degenerated DCO scheme [14].

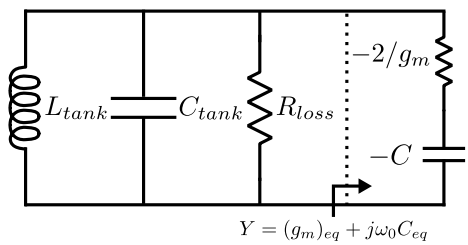


Figure 4.19 Capacitively degenerated DCO equivalent circuit [14].

The biasing resistor R in the figure should be large enough so as not to have a critical effect on the equivalent capacitance. If, for example, $C_1 = 1$ pF and $C_2 = 100$ fF the reduction factor achieved is 121, which shows the effectiveness of the technique. However, this technique is limited by parasitic capacitances and mismatches.

4.5.2.3 CAPACITIVE DEGENERATION METHOD

In order to obtain higher frequency resolution, another method depending on switching very small values of capacitance can be employed [14]. This is can be done by moving the fine tuning bank from the drains to the sources of the cross-coupled pair that implements the negative resistance of the LC oscillator, as shown in Figure 4.18. If the value of the capacitance C is much greater than the ratio $g_m/(2\omega_0)$, where g_m is the transconductance of the cross-coupled

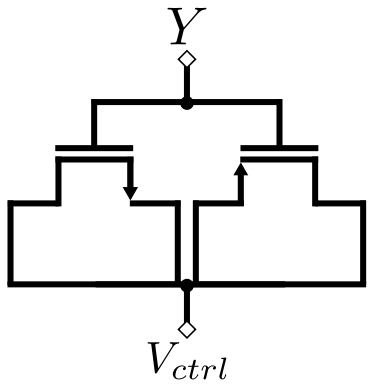


Figure 4.20 Simplified model of the varactor composed of NMOS and PMOS pair [15].

pair, the admittance Y seen by the tank, shown in Figure 4.19, is

$$Y = \frac{-g_m}{2} - j\omega_0 C Q_f^2 \tag{4.20}$$

where $Q_f = g_m/(2\omega_0 C)$.

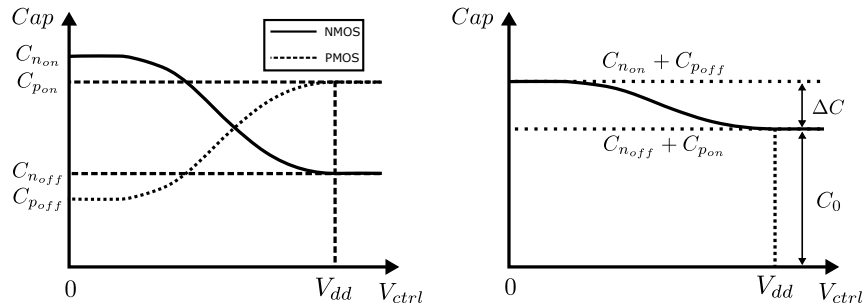
The real part of Y still represents the negative conductance for tank losses compensation, while the imaginary part presents the equivalent negative capacitance shrunken by a factor $g_m^2/(2\omega_0 C)^2$. Simulation results suggest, for example, that a capacitor of value 3 pF can effectively be reflected into an equivalent capacitance of 15 fF with a reduction factor of about 200 at an oscillation frequency of 3.6 GHz.

This technique eliminates the need for $\Delta\Sigma$ dithering, which, we have seen, increases complexity and out-of-band phase noise. However, it is deeply sensitive to PVT variations, because its resolution depends on the transconductance of transistors and must be calibrated.

4.5.2.4 MOS VARACTORS TECHNIQUES

Another method to enhance the frequency resolution is by minimizing the unit switchable capacitor by using complementary MOS varactors: NMOS and PMOS [15]. This method relies on the small differences in capacitance values between PMOS and NMOS varactors. In this method, a varactor consists of an NMOS varactor in parallel with a PMOS varactor is formed, as illustrated in Figure 4.20.

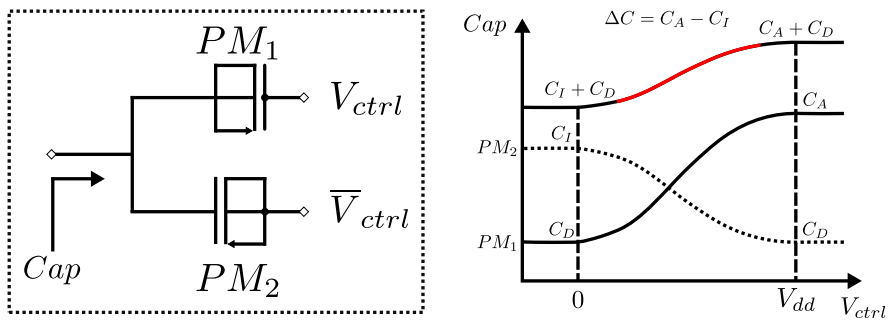
The individual C-V characteristic curves of both PMOS and NMOS varactors are displayed in Figure 4.21(a). If both varactors are connected in parallel with the same control voltage applied to them, a new C-V characteristics can be



(a) C-V characteristics of NMOS and PMOS varactor.

(b) C-V characteristics of the formed varactor.

Figure 4.21 C-V characteristics [15].



(a) Simplified model of varactor composed of PMOS pair.

(b) C–V characteristic of the constructed pair.

Figure 4.22 Simplified model with C-V characteristics [16].

obtained, as illustrated in Figure 4.21(b), and the equivalent capacitance ΔC achieved by using this topology is equal to

$$\Delta C = C_{n_{on}} + C_{p_{off}} - C_{n_{off}} - C_{p_{on}} \tag{4.21}$$

where $C_{n_{on}}$ and $C_{n_{off}}$ are the capacitances of the NMOS on and off regions, respectively, while $C_{p_{on}}$ and $C_{p_{off}}$ are the capacitances of the PMOS on and off regions, respectively.

Another method is suggested in [16] by using two PMOS varactor pair oppositely coupled in parallel (see Figure 4.22(a)), and controlled by a control voltage V_{ctrl} and inverted $\overline{V}_{ctrl}$, respectively. This method exploits the differences between the accumulation and inversion region capacitances of the PMOS varactor. Changing the value of V_{ctrl} between 0 and V_{dd}, the capaci-

tance of each varactor then swings oppositely to each other between different regions, as illustrated in Figure 4.22(b). The small difference in varactor value between different modes of the opposite varactors gives the required small capacitance change, as shown in Figure 4.22(b).

4.6 OSCILLATOR PULLING

As a result of continued scaling in CMOS technologies, more designs are integrated together. The inductor is the most critical component in an LC oscillator, since its Q affects the phase noise performance and determines the power dissipation. Aside from a large area occupied by inductors, reducing the distance between inductors results in a stronger magnetic coupling between them, which causes interference between different circuits, especially at high frequencies. For example, the existence of power amplifiers with a large output power at frequencies near a multiple of those generated by the oscillators can cause a frequency modulation on the oscillator signal, a phenomena referred to as pulling.

Reducing the magnetic coupling between different inductors by separating them by a large distance conflicts with the integration principle, and instead of minimizing the area it increases it, increasing costs. An effective way to reduce the magnetic coupling between nearby inductors is to use 8-shaped inductors instead of standard shapes like octagonal one (O-shaped). The 8-shaped inductor [76–79] reduces the magnetic coupling between nearby inductors, as it rejects any common-mode magnetic field because of geometric symmetry, while it also generates a magnetic field that vanishes far from the coil itself.

An Electromagnetic (EM) simulation study of the magnetic coupling between 8-shaped inductor and O-shaped inductor is presented in the rest of this chapter.

4.6.1 EM SIMULATION SETUP

With an O-shaped inductor, shown in Figure 4.23(b) and Figure 4.23(c), a strong magnetic field radiates to nearby inductors, causing interference. On the other hand, the 8-shaped inductor illustrated in Figure 4.23(a) consists of two loops, where the currents flowing in the two loops are equal but in opposite directions, producing magnetic fields that are equal in magnitude but with opposite polarities. This means that the two magnetic fields cancel each other, and the overall magnetic field generated by the 8-shaped inductor almost vanishes far from the inductor itself, reducing the magnetic coupling to nearby inductors. In the same way, the 8-shaped inductor rejects any common-mode magnetic field impinging on it. Unfortunately, the Q of the O-shaped inductor is larger than the Q of the 8-shaped inductor for the same inductance value.

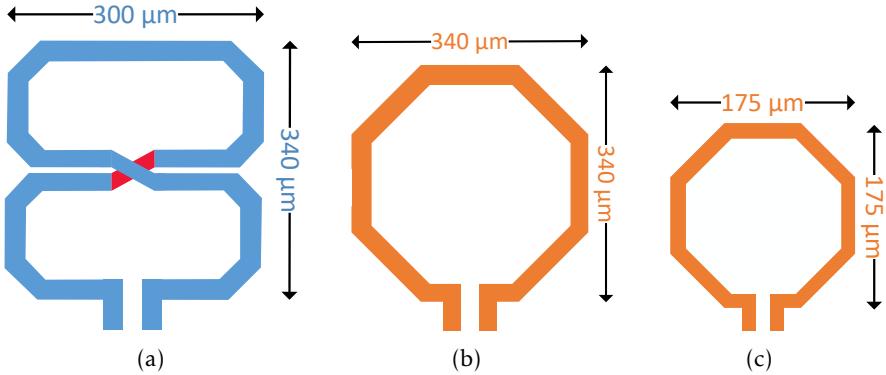


Figure 4.23 Top view a) 0.73 nH 8-shaped inductor, b) 3 nH O-shaped inductor and c) 0.73 nH O-shaped inductor.

This difference is due to the longer trace of the 8-shaped inductor in comparison with O-shaped inductor, which means more series resistance [77].

Three different inductors are designed to be used in simulations:

- A 300×340 μm 8-shaped inductor with inductance value of 0.73 nH [76], as in Figure 4.23(a).
- A 340×340 μm O-shaped inductor with inductance value equal to 3 nH, as in Figure 4.23(b).
- A 175×175 μm O-shaped inductor with inductance value of 0.73 nH, as in Figure 4.23(c).

All inductors are designed in a 28 nm UTBB FD-SOI CMOS process.

ADS momentum is used to perform the EM simulations. As in Figure 4.24, each inductor has two ports. Mixed-mode S-parameter simulation is used.

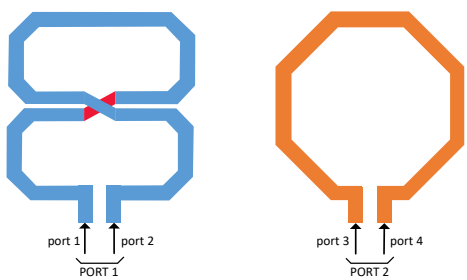
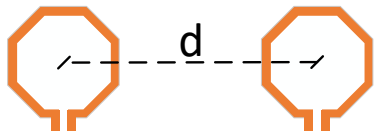
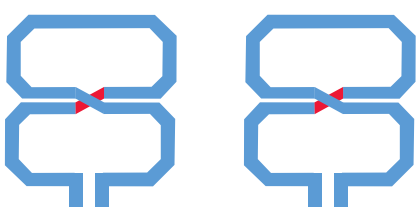


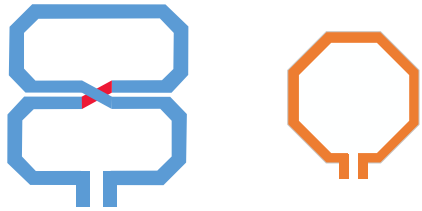
Figure 4.24 Ports in ADS momentum simulation.



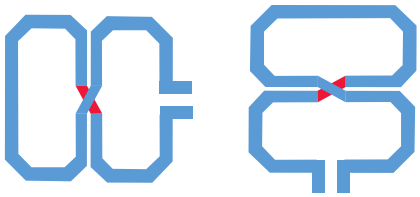
(a) Two 0.73 nH O-shaped inductors.



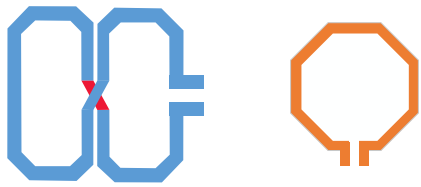
(b) Two 0.73 nH 8-shaped inductors.



(c) 0.73 nH 8-shaped inductor with 0.73 nH O-shaped inductor.



(d) 0.73 nH 8-shaped inductor rotated by 90° with 0.73 nH 8-shaped inductor.



(e) 0.73 nH 8-shaped inductor rotated by 90° with 0.73 nH O-shaped inductor.

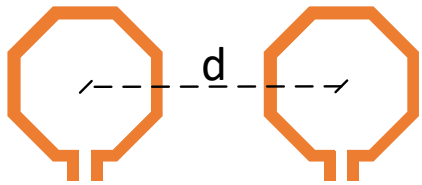
Figure 4.25 First configuration.

Port1 and port2 are combined as PORT1 and port3 and port4 are combined as PORT2. In order to compare the magnetic coupling between 8-shaped inductor and O-shaped inductor, four test configurations, which will be denoted as A, B, C, and D, were examined:

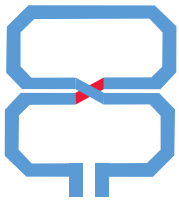
(A) **Test configuration A (Figure 4.25)** uses a 0.73 nH 8-shaped inductor and a 0.73 nH O-shaped inductor with 0.5 mm separation distance (d = 0.5 mm)

(B) **Test configuration B (Figure 4.25)** also uses a 0.73 nH 8-shaped inductor and a 0.73 nH O-shaped inductor, but the separation distance now becomes 1 mm (d = 1 mm).

(C) **Test configuration C (Figure 4.26)** the comparison is done between a 0.73 nH 8-shaped inductor and a 3 nH O-shaped inductor, with separation distance equal to 0.5 mm (d = 0.5 mm).

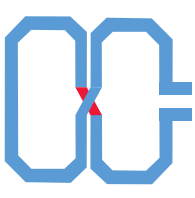


(a) a Two 3 nH O-shaped inductors.

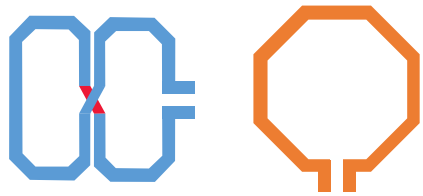


(b) Two 0.73 nH 8-shaped inductors.

(c) 0.73 nH 8-shaped inductor with 3 nH O-shaped inductor.



(d) 0.73 nH 8-shaped inductor rotated by 90° with 0.73 nH 8-shaped inductor.



(e) 0.73 nH 8-shaped inductor rotated by 90° with 3 nH O-shaped inductor.

Figure 4.26 Second configuration.

(D) **Finally, test configuration D (Figure 4.26)** is also between a 0.73 nH 8-shaped inductor and a 3 nH O-shaped inductor, but with separation distance equal to 1 mm (d = 1 mm).

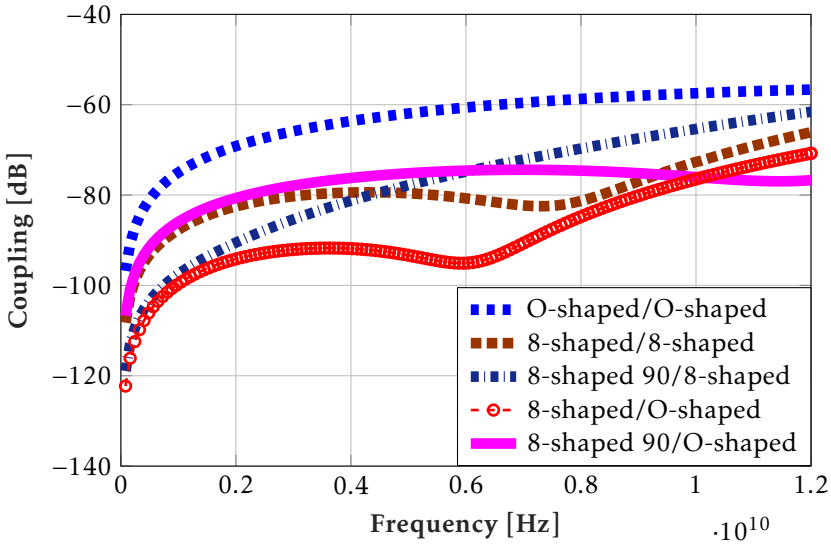
For each configuration, there are five test cases, investigated as follow. The first case is between two O-shaped inductors, which will serve as reference, as shown in Figure 4.25(a). This is followed by the two 8-shaped inductors in Figure 4.25(b), by one 8-shaped inductor and one O-shaped inductor, as shown in Figure 4.25(c), by one 8-shaped inductor rotated by 90° and one 8-shaped inductor, as illustrated in Figure 4.25(d), and finally by one 8-shaped inductor rotated by 90° and an O-shaped inductor, as illustrated in Figure 4.25(e). The magnetic coupling between the inductors, characterized by the magnitude of S_{21}, is examined, for the five test cases in each configuration for the frequency region between 80 MHz and 12 GHz.

Table 4.1 Coupling comparison of configurations (A), (B), (C) and (D) at 6 GHz.

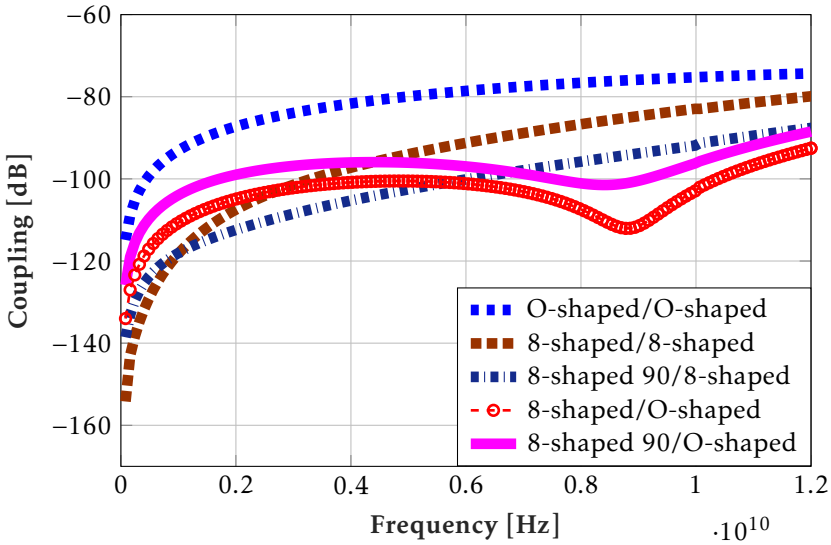
Config	Test Case	Absolute S_{21}	$\Delta(dB)$
A	O-Shaped/O-shaped	-60.6	Ref
	8-Shaped/8-shaped	-80.8	20.2
	8-Shaped 90°/8-shaped	-74.7	14.1
	8-Shaped/O-shaped	-95.0	34.4
	8-Shaped 90°/O-shaped	-74.6	14.0
B	O-Shaped/O-shaped	-78.5	Ref
	8-Shaped/8-shaped	-91.1	12.6
	8-Shaped 90°/8-shaped	-100.0	21.5
	8-Shaped/O-shaped	-101.2	22.7
	8-Shaped 90°/O-shaped	-97.0	18.5
C	O-Shaped/O-shaped	-36.7	Ref
	8-Shaped/8-shaped	-80.8	44.1
	8-Shaped 90°/8-shaped	-74.7	38
	8-Shaped/O-shaped	-80.7	44
	8-Shaped 90°/O-shaped	-58.7	22
D	O-Shaped/O-shaped	-55.9	Ref
	8-Shaped/8-shaped	-91.1	35.2
	8-Shaped 90°/8-shaped	-100.0	44.1
	8-Shaped/O-shaped	-98.7	42.8
	8-Shaped 90°/O-shaped	-82.3	26.4

4.6.2 EM SIMULATION RESULTS

Table 6.1 summarizes the simulation results of each configuration at 6 GHz, while Figures 4.27 and 4.28 shows the simulated magnitude of S_{21} for each configuration. From Figure 4.27(a), which shows the simulation results for test configuration A, it is clear that there is a significant reduction in the magnetic coupling, which reaches a 34 dB improvement at 6 GHz for the 8-shaped/O-shaped test case, compared to the reference case. Figure 4.27(b) displays the test configuration B simulation results. While a reduction in magnetic coupling might be expected with an increasing separation between the inductors, these simulations show a different behavior in some cases, where isolation in fact decreases with an increasing separation. The previous behavior can be explained with the fact that the overall coupling is a combination of magnetic (inductive) and substrate (capacitive) coupling. Therefore, the inductive and capacitive components depend on the frequency, and in some frequency region they may partially cancel each other, resulting in a reduction in the total coupling in that region [81]. The behavior depends on the distance between

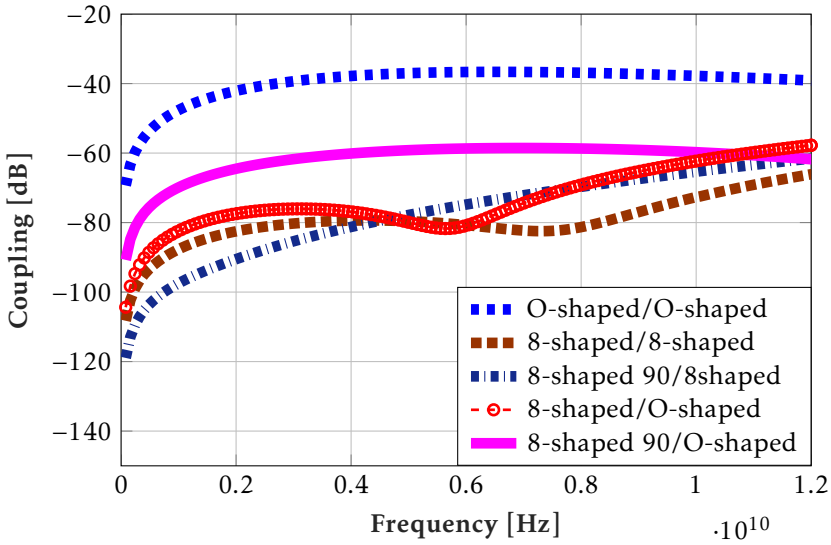


(a) Simulation results of coupling versus frequency for configuration (A).

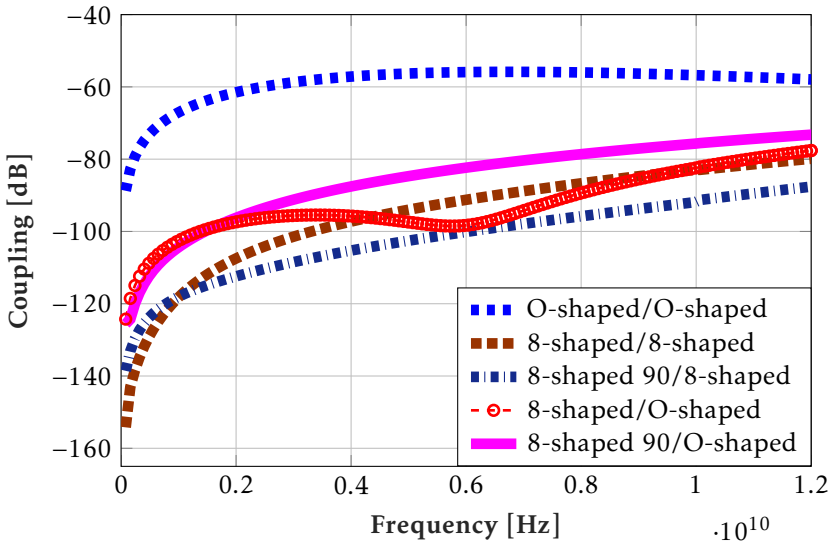


(b) Simulation results of coupling versus frequency for configuration (B).

Figure 4.27 Simulation results of coupling versus frequency for configuration (A) and (B).

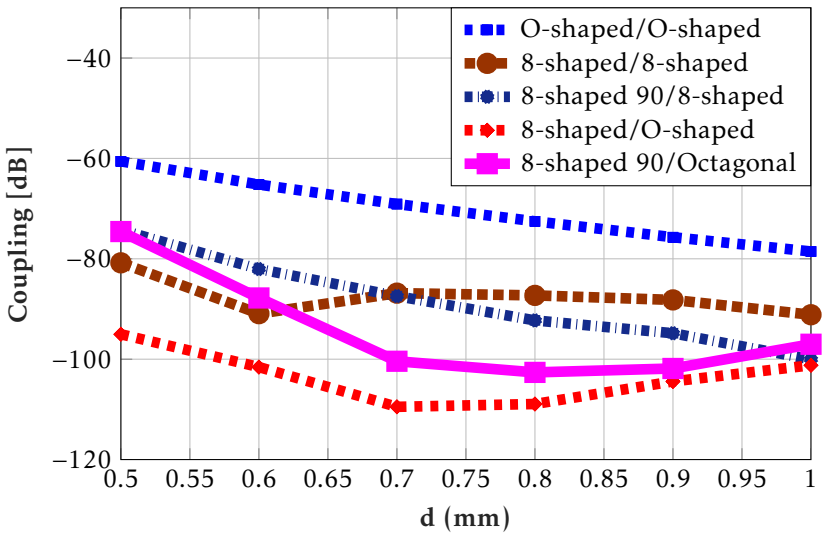


(a) Simulation results of coupling versus frequency for configuration (C).

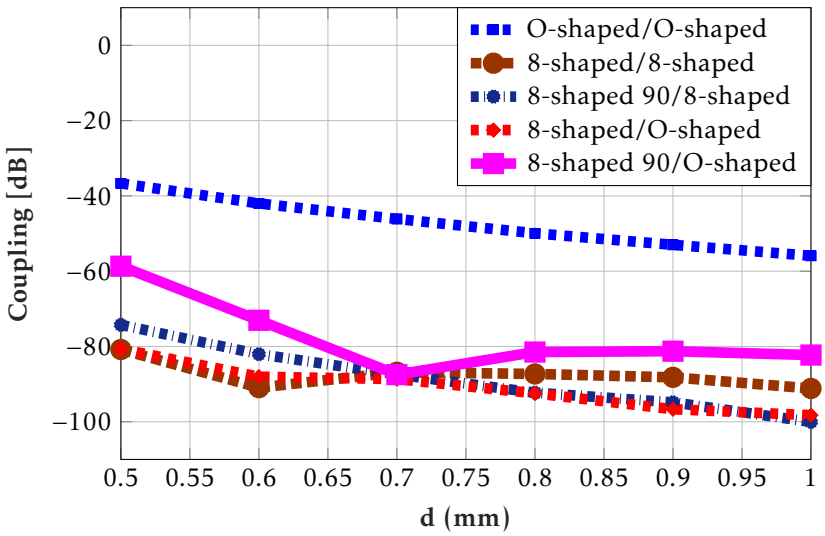


(b) Simulation results of coupling versus frequency for configuration (D).

Figure 4.28 Simulation results of coupling versus frequency for configuration (C) and (D).



(a) Simulation results of coupling versus separation distance (d) for configuration (A).



(b) Simulation results of coupling versus separation distance (d) for configuration (C).

Figure 4.29 Simulation results of coupling versus separation distance (d) for configurations (A) and (C).

coils and on the frequency of operation.

Test configurations C and D represent the case of an 8-shaped inductor and an O-shaped inductor with the same area of the 8-shaped inductor, but with different separations. Also here there are significant isolation improvements, reaching 44 dB at 6 GHz in configuration C for the 8-shaped/8-shaped test case, and the same in configuration D for the 90°–rotated-8-shaped/8-shaped test case. Also here, we notice that in some cases the coupling between coils increases with increasing separation, instead of diminishing (Figure 4.28(a) and 4.28(b)).

Figure 4.29(a) and 4.29(b) shows the simulation results of the magnitude of S_{21} versus separation distance for configurations A and C (respectively) at 6 GHz and separation distance between 0.5 mm to 1 mm. The value of S_{21} drops as the distance increases as indicated, but in some cases it decreases. This can also be explained as in the previous cases.

From all the above simulations we can conclude that the 8-shaped inductor affords a considerable coupling reduction, enabling an enhanced isolation between inductors integrated on a single chip. However, it is important to note that this reduction is also dependent on the orientation of the inductors, so by carefully considering the placement of all sensitive inductors, further coupling reduction can be achieved, as shown by the simulations results.

5

TDC and DTC

TDCs and DTCs nowadays are linked mainly to DPLLs, where a TDC acts as phase detector, but interestingly the potential applications of TDCs vary widely with applications in analog-to-digital conversion for mixed signal interfaces, impedance spectroscopy, time-of-flight measurements for ranging, and also in imaging systems and high energy instrumentation applications, such as digital scopes and logic analyzers. They are also widely used in high-energy particle physics experiments. Also, DTCs can be used in a variety of applications such as in clock and data recovery circuits, (sub-)sampling oscilloscopes, radar, and automatic test equipments.

TDC and DTC are two of the most crucial blocks in a DPLL system. Their performance, combined with the DCO performance, determines to a large extent the overall performance of the TDC-based DPLL and BB-based DPLL systems. Most of the DPLL challenges are associated with the TDC and DTC design. As a result, it has been the subject of intensive research efforts in recent years [18–21] [25–27] [34] [43] [82–92].

This chapter focuses on the fundamentals of TDC and DTC. Furthermore, commonly used design parameters are explained, and some of the most popular TDC and DTC architectures are reviewed.

5.1 TDC

The TDC is a mixed-signal block working as an interface between time domain and digital domain. Therefore, it is inevitable to avoid that the TDC induces quantization errors when converting time to digital signals, due to its finite resolution. This quantization could dominate the in-band phase noise at the output of the DPLL, while it also limits the loop bandwidth. The limitation on the loop bandwidth, in turn, reduces the suppression of the DCO phase

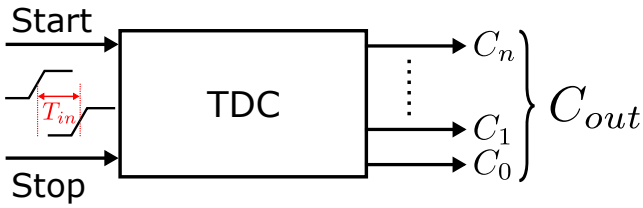


Figure 5.1 Basis of time to digital conversion.

noise, causing poor overall phase noise performance. The key to reduce the quantization error is to improve the resolution of the TDC. Thus, design and implementation of high-resolution TDC become the ultimate goal for the designers. Besides high-resolution, low dead time and large dynamic range are also required for a high quality TDC.

A TDC is a device that quantizes time intervals between two or more consecutive timing events and converts them to digital output values. Figure 5.1 illustrates the basic idea of the TDC, where a time interval T_{in} between two signals is digitized to a digital output code C_{out} through the TDC.

With the aid of Figure 5.2, which is describing the basic operating principles of the TDC, the TDC idea can be clarified and used as an entry point into the discussion of the TDC performance parameters and architectures. The idea behind the TDC is to be able to divide the time interval to be measured ($T_{in} = T_{stop} - T_{start}$) into a number of smaller time intervals of nominal length Δ, where Δ is corresponding to the minimum reference time interval, i.e. the TDC resolution. Thereafter, an approximate value of T_{in} can be directly calculated by counting the number of intermediate reference pulses (i.e. $T_{out} = C_{out}\Delta$).

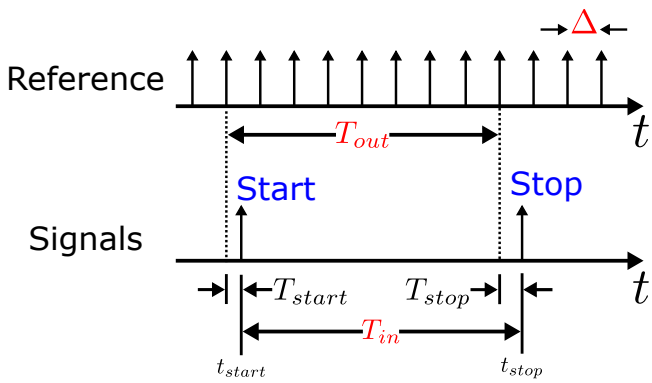


Figure 5.2 TDC conceptual idea [17].

However, the previous relationship can be applied only if the start and stop instants coincide exactly on the intermediate reference pulses, which is not the case in real life, where there is always a quantization error q at both the beginning and end of the measurement. This quantization error is coming as a result of using a finite number of intermediate reference pulses, or, in other words, a finite resolution. Thus, the actual value of T_{out} can be given by

$$T_{out} = C_{out}\Delta + q \tag{5.1}$$

5.1.1 PERFORMANCE PARAMETERS

The TDC draws many parallels with the ADC in terms of its performance characteristics. Therefore, most TDC performance metrics are based on those used for the conventional ADC. The main parameters of the TDC that characterize its performance are: time resolution, dynamic range, linearity, dead time, conversion time, latency, area, and power consumption.

In the next sub-sections, the main TDC performance metrics are presented. Their meaning and significance are explained, as well as the way they can be measured, if relevant.

5.1.1.1 RESOLUTION

As a tool to measure time intervals, resolution or LSB is considered as the most fundamental parameter in designing a TDC. The resolution refers to the minimum input time interval that can be resolved by a TDC. It is also the step width in input–output transfer curve that characterizes the TDC. Ideally, the step widths in the TDC transfer curve are constant, as shown in Figure 5.3(a).

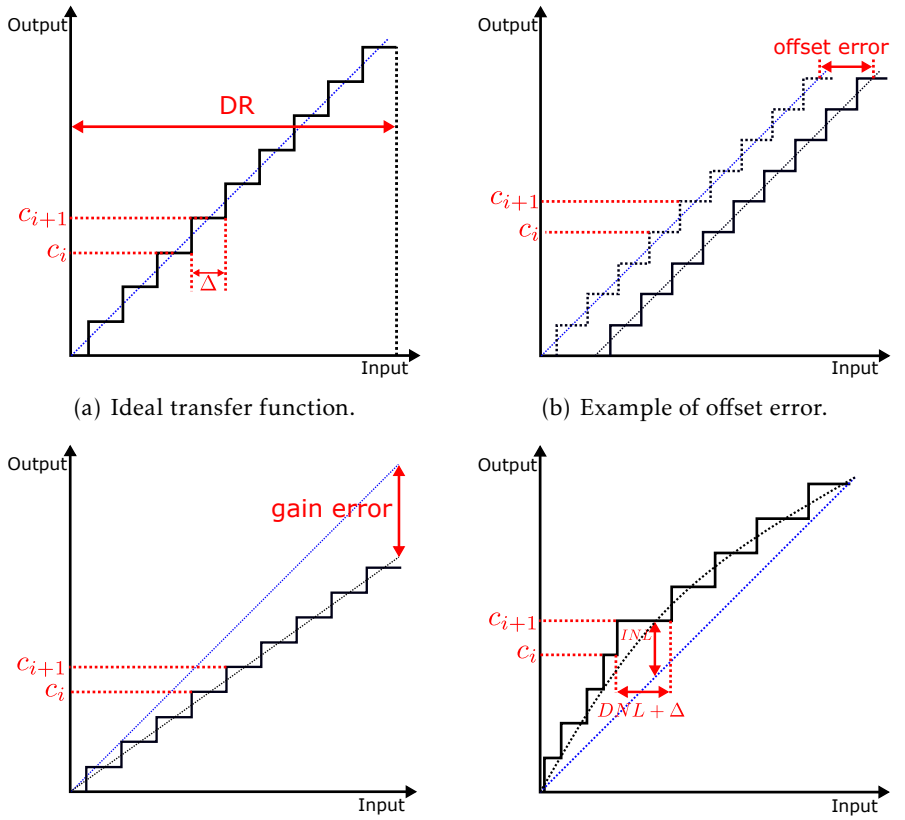
The resolution of the TDC has a direct impact on the performance of a DPLL, where it contributes to the in-band phase noise as described in [41]. This demonstrates that with lower resolution, the performance of the DPLL in terms of its in-band phase noise is improved as expressed by [33]

$$\mathrm{PN} = 10\log[\frac{(2\pi N)^2}{T_{ref}}\frac{\Delta^2}{12}] \tag{5.2}$$

where T_{ref} and N are the reference period and the nominal divide value of the DPLL system, respectively.

5.1.1.2 DYNAMIC RANGE

The Dynamic Range (DR) is the largest time interval that can be measured and correctly quantized without saturation, as shown in Figure 5.3(a). This property is architecture dependent and has a direct impact on the area and power consumption.



(a) Ideal transfer function.

(b) Example of offset error.

(c) Example of gain error.

(d) Example of DNL and INL.

Figure 5.3 TDC ideal and non-ideal curves with gain error, offset error, DNL and INL examples.

5.1.1.3 LINEAR AND NON-LINEAR NON-IDEALITIES

Imperfections or non-idealities lead a TDC to deviate from its ideal curve. Sources of non-idealities include: delay errors, signal crosstalk, layout mismatch, and PVT variations. Therefore, circuit architecture and layout implementations play an important role in increasing or decreasing the impact of non-idealities. The non-idealities of the TDC can be classified into two classes: linear or non-linear. Linear imperfections include gain and offset errors, while INL and DNL are both non-linear blemishes. Linear imperfections usually demand less complications to be corrected and also they are readily or easily seen in the TDC characteristic curve. On the other hand, non-linear imperfections require more rigorous calibration schemes, and usually cannot be totally cor-

rected. Both linear and non-linear terms identify the deviation of the TDCs characteristics in the same manner as for ADCs.

- **Offset Error:** It is defined as the deviation of the TDC characteristic from the ideal characteristic at input equal to zero. It can also be defined as the deviation of the TDC characteristic line from the one of the ideal TDC (the characteristic line is defined by a straight line drawn either as best fit or from the converter's beginning to its end-point, and it is shown with blue color in all curves) [93]. Offset error affects similarly all the digital output codes, therefore it can be eliminated by calibration. It is usually expressed as number of LSBs. Figure 5.3(b) shows an example of a TDC with an offset error.

- **Gain Error:** After correcting the offset error, the gain error is defined as the deviation in the slope of the TDC characteristic line from the ideal one. Figure 5.3(c) shows an example of a TDC with a gain error. Usually the gain error is expressed as a percentage value.

- **DNL:** It is used to refer to the difference between the actual and ideal step widths in the TDC transfer curve [93]. For a given two consecutive digital output codes, DNL_i is given by the following equation

$$DNL_i = \frac{d_{i+1} - d_i - \Delta}{\Delta} \tag{5.3}$$

  where d_i is the measured cumulative delay from the origin to the code c_i, as indicated in Figure 5.3(d).

- **INL:** It describes the deviation of the actual transfer curve from its ideal one. By definition, INL for a particular code is the integral of DNL along the delay stages up to that code, as shown in Figure 5.3(d) and as expressed by [93]

$$INL_i = \sum_{n=0}^{i-1} DNL_n \tag{5.4}$$

5.1.1.4 DEAD TIME, CONVERSION TIME AND LATENCY

Dead time is defined as the time needed after a measurement before a new one can be started [93]. Another performance metric is the conversion time, which is the time duration between the start event and the availability of a valid output [93], while latency is defined as the time duration between the arrival of the stop event and the occurrence of a valid output [93]. Basically, it is how long it takes the TDC to send out a valid output word for a given time input.

Dead time, conversion time and latency describe the speed of the TDC. They are very important especially for high-speed applications. Based on different architectures and application requirements, some TDCs can perform measurements very quickly in real-time, whereas in some cases, there exists a need to exercise the full-scale DR. There is always a trade-off between dead time, conversion time and latency with power consumption.

5.1.2 TDC ARCHITECTURES REVIEW

Generally, according to the operating principles, TDCs can be classified into two categories: analog and digital [94]. In the analog approach, the time interval is firstly converted into a voltage, then this voltage is translated into a digital form by an ADC. These architectures achieve a good performance in terms of resolution and linearity at the expense of high power dissipation, large size, low scalability with CMOS technology, and high noise susceptibility [94]. In contrast with the analog approach, TDCs designed with the digital approach using CMOS processes have gained greatly from process scaling, since reducing gate delays improves the resolution and also leads to compact implementations.

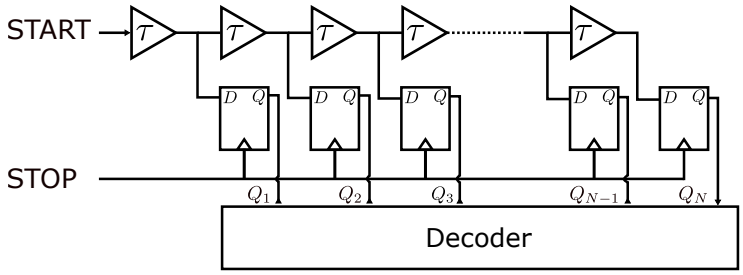
While the delay has continued to decrease, the accuracy of the delay also needs to be improved for the traditional TDC architectures to benefit from scaling. However, with future CMOS scaling, transistor and parasitic mismatch increase, and consequently the delay mismatch also increases, which becomes the bottleneck for many TDC architectures [17]. This has necessitated the exploration of different architectures based on different methods, resulting from extensive research efforts, which are described in the following sub-sections. Their strengths and weaknesses are highlighted accordingly.

5.1.2.1 DELAY-LINE TDC

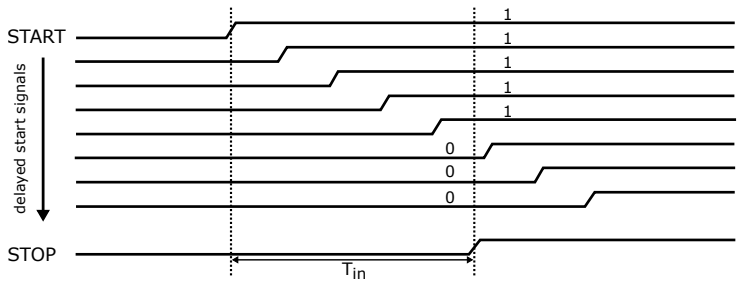
The simplest TDC is based on a delay line composed of delay elements combined with sampling elements (usually D flip-flops) [95]. In Figure 5.4(a) an example of such a TDC architecture is shown. The START signal propagates through a tapped delay line, whose state is sampled by the STOP signal. When the STOP signal arrives, the outputs of all the delay elements are stored into a register resulting in a thermometer code. The position of '1'/'0' transfer in the thermometer code represents the time difference T_{in} between the START and STOP signals, as shown in Figure 5.4(b) and calculated as follows

$$T_{in} = M\tau + q \tag{5.5}$$

where M is the number of all delay stages that have been passed by the START signal, τ represents the time delay of the delay element used, and q is the



(a) Delay-line TDC scheme.



(b) Delay-line TDC waveforms.

Figure 5.4 Delay-line TDC scheme and waveforms.

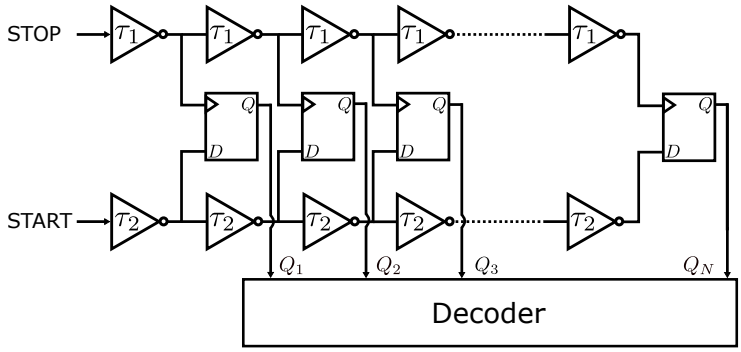
quantization error that arises, as the delay element has only two states, either passed or not passed by the START signal .

One of the obvious advantages of this topology is that it can be fully digital, elegant and simple to be implemented. However, it suffers from poor resolution, since Δ is limited by the minimum delay of the delay element in the chain that can be built in the technology used, or, in other words, $\Delta = \tau$.

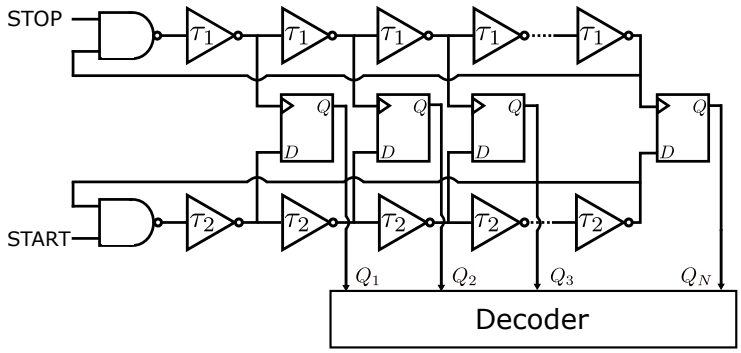
5.1.2.2 VERNIER TDC

The resolution of the TDC can be further improved by adopting the Vernier architecture [84]. A Vernier TDC provides a structure to overcome the process limitation, i.e. capable of measuring time intervals with sub-gate resolution. The Vernier delay line structure consists of a pair of tapped delay chains with a flip-flop at each corresponding pair of taps, as shown in Figure 5.5(a). The idea is to delay both the START and STOP signals with each delay chain; one chain with a slow delay of τ_1 and the other with fast delay of τ_2 per element, so that the Vernier TDC has an effective resolution equal to

$$\Delta = \tau_1 - \tau_2 \tag{5.6}$$



(a) Vernier TDC [84].

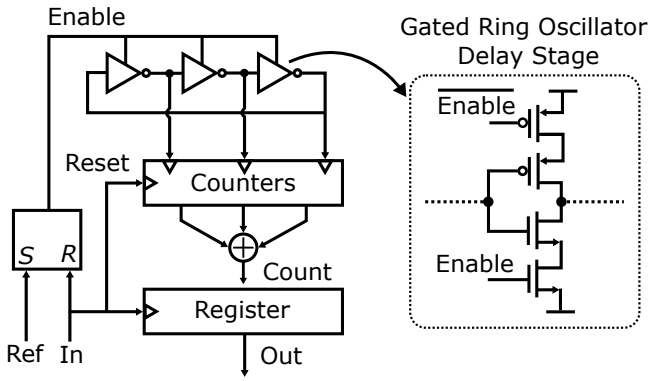


(b) Vernier TDC using ring oscillators [86].

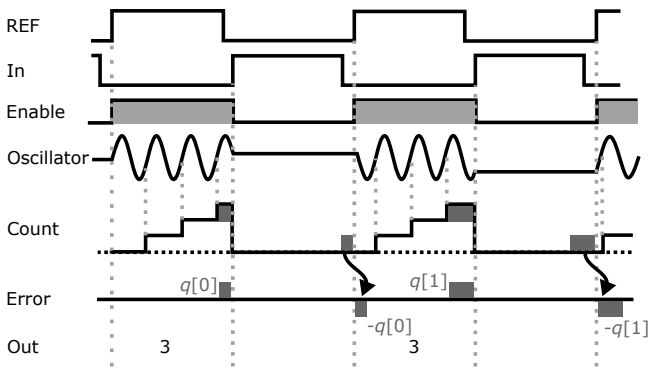
Figure 5.5 TDC-based Vernier method.

The Vernier TDC provides a high resolution beyond process limitation by using delay differences rather than a single delay, and by setting τ_1 close to τ_2, a very fine resolution can be obtained. However, its DR is limited by the total number of delay elements, which would increase dramatically in order to cover a large DR. In addition, latency, area and power consumption would also dramatically increase. Therefore, Vernier TDCs are suitable for applications that do not require a large DR. They also suffer from mismatch problems.

To reduce the size issue, a cyclic architecture of Vernier chains is presented in [86]. This solution is able to extend the Vernier TDC DR by arranging the delay lines as a ring oscillator, similar to the one shown in Figure 5.5(b). For a ring oscillator TDC architecture, the DR is determined by the loop counter which tracks the number of complete cycles the input signal (either edges or pulses) has made across the loop. Since a loop theoretically has infinite length, the number of bits of the counter then places a bound on the range. Although



(a) GRO-TDC scheme.



(b) Associated signals in GRO-TDC structure.

Figure 5.6 GRO-TDC scheme and associated signals [18].

a ring oscillator TDC architecture leads to an increase in the DR, it comes at the cost of complicated decoding logic and calibration.

5.1.2.3 GRO-TDC

Fig 5.6 shows the conceptual implementation of a TDC using a Gated Ring Oscillator (GRO) [18] [33]. A GRO-TDC consists of a ring oscillator structure, but the delay cells in the ring oscillator are gated. As the figure illustrates, to measure the phase difference between two signals, a GRO-TDC operation starts by enabling the ring oscillator during the measurement window and counting the number of resulting transitions that occur in the oscillator. At the end of the measurement window, the ring oscillator is disabled, freezing its current state. Hence, the quantization error from the end of the current measurement

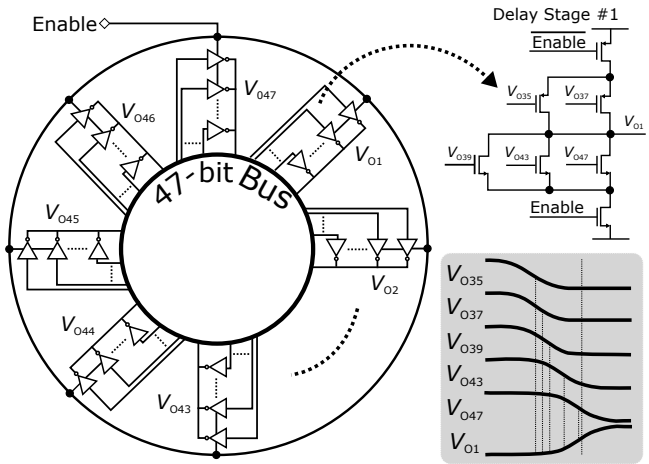


Figure 5.7 Multipath GRO-TDC [19].

window is stored and added to the start of the next measurement interval. Therefore, it provides a first-order noise shaping of the quantization noise, as evidenced by the following first-order difference equation, which expresses the overall quantization noise $e[k]$ as

$$e[k] = q[k] - q[k-1] \tag{5.7}$$

where $q[k]$ denotes the k^{th} quantization error at the end of each measurement window.

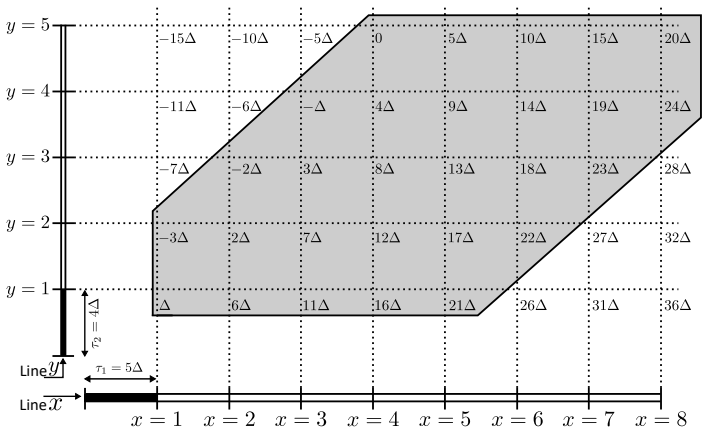
With this first-order noise shaping effect, the quantization noise is moved to a high frequency region, thus a lower in-band noise is achieved, increasing the effective resolution below an inverter delay by virtue of the noise shaping that it offers. Apart from the quantization noise, according to the well-known barrel-shift algorithm for dynamic element matching [96], GRO-TDC structure realizes a first-order shaping of mismatch errors as well. Thus, this architecture ideally achieves high resolution without calibration even in the presence of mismatch [17]. Nevertheless, the native resolution of the GRO-TDC is still set by the inverter delay, i.e., it is relatively poor.

To further improve the limited resolution achieved, a multipath technique can be applied [97], to speed up the transition time of each delay element. By doing that, a resolution enhancement is attained, equal to the same speed up factor. One example of this is the multipath GRO-TDC that has been proposed in [19], and illustrated in Figure 5.7. In this example, three NMOS and two PMOS transistors (in addition to one NMOS and PMOS pair for gating function) are used to realize one inverter, in order to implement this multipath

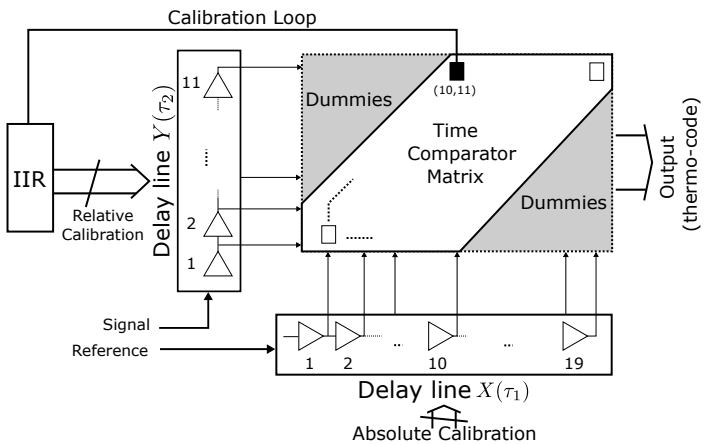
technique. This technique, allows an earlier arrival of the input transition to the slower PMOS transistors. Furthermore, instead of being only tapped from its previous stage, multiple connections to the NMOS transistors are made. Therefore, their speed is not limited any more by the slow PMOS transistors, but only by the transition time of the multipath inverter [19].

5.1.2.4 2D VERNIER TDC

The classic Vernier TDC only computes the time difference between elements located in the same position of the two delay lines, hence it realizes a lin-



(a) Vernier plane expansion.



(b) 2D Vernier TDC implementation.

Figure 5.8 Vernier plane expansion with 2D Vernier TDC implementation [20].

ear delay scheme. However, if the time difference measurements between all different possible taps were granted, the number of possible measurements would increase dramatically. This defines a new plane, Vernier plane, which combines all these time differences [20], as shown in Figure 5.8(a). In this way, having two lines with N and M elements each, NM quantization levels are defined. In reality, only a portion of this plane, highlighted in gray, has a linear and uniform succession of time differences that can be used. The intersection points in the figure are replaced by latches to detect the point where the two signals meet, where each latch produces a "1" or a "0" resulting in a readout in thermometer code format. This approach can significantly decrease the number of stages of the delay lines needed to achieve a given number of quantization steps with the same resolution Δ.

There are plane points which do not contribute to the DR, thereby they are not used and can be neglected. However, to enforce a simpler and more homogeneous design in the delay elements, these points are also connected to the delay line, thus acting as dummy load capacitances. In this sense, SR latches are preferred over D-flip flops, since they have a symmetric structure, which also helps the delay homogeneity in both paths.

The schematic diagram of the 2D Vernier TDC is reported in Figure 5.8(b). The two delay lines define the Vernier plane that is completely covered by a matrix of SR latches used as time comparators (see Figure 5.9). However, as in other Vernier TDCs, the long latency limits the detection range. Also, this architecture needs a calibration procedure during its operation in order to set the correct ratio between the delays τ_1 and τ_2, so adding more complexity to the system.

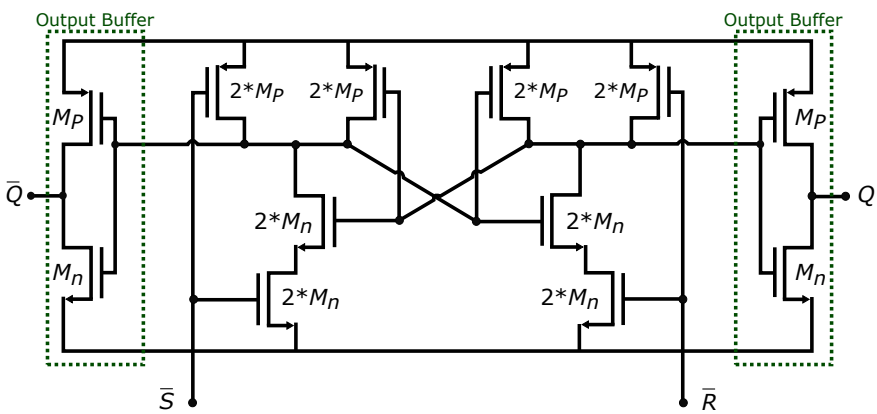


Figure 5.9 Time comparator schematic [20].

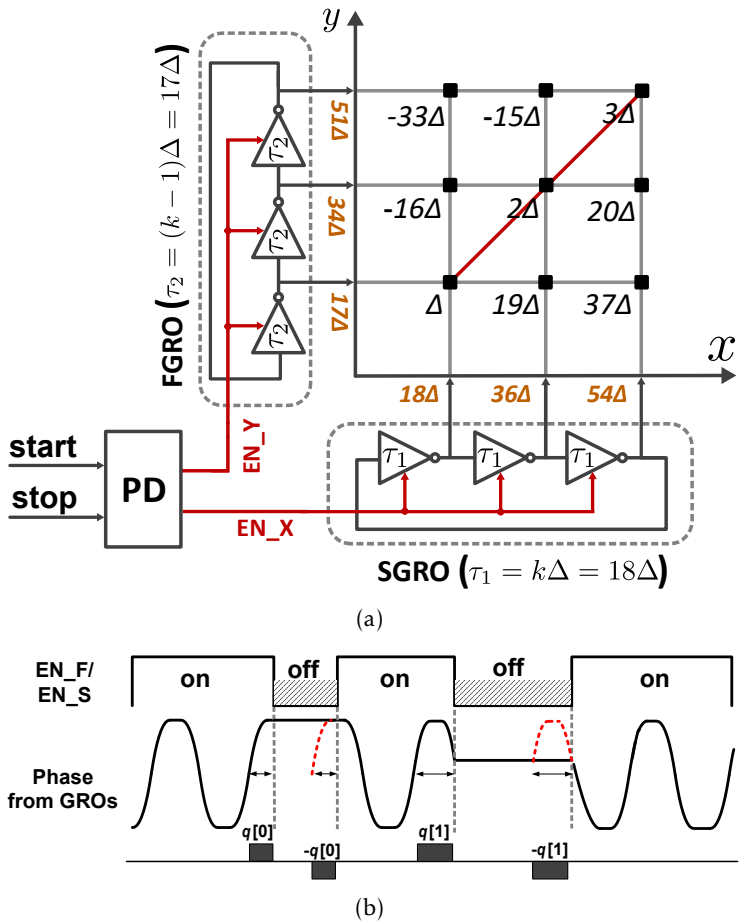


Figure 5.10 a) The simplified 2-D GVTDC and b) GRO operation

5.1.2.5 2D GVTDC

The 2D Gated-Vernier TDC (GVTDC), combining the Vernier approach with a GRO, can achieve both a high raw (Vernier) resolution and a first-order frequency shaping of the quantization noise [90]. As shown in Figure 5.10(a), it is seen that the Vernier line is extended to a Vernier plane by utilizing all delay differences between Slow-Delay GRO (SGRO) and Fast-Delay GRO (FGRO). Here, for convenience, only the positive half plane is used. This requires the Phase Detector (PD) to be able to convert all negative inputs to positive ones, producing a sign indicator.

Two GROs are used to implement the delay lines in the Vernier plane. Dur-

ing the current measurement window, when FGRO catches up with SGRO, the state of both GROs are frozen by falling EN_X/EN_Y. Therefore, the quantization error from the end of the current measurement window for both SGRO/FGRO are stored and added to the start of the next measurement window, as shown in Figure 5.10(b). Accordingly, each GRO starts from this state. In this way, the quantization error is accumulated across all measurement windows, resulting in a first-order quantization noise shaping. The TDC output can be obtained by counting the delay numbers of SGRO and FGRO, respectively. Thereafter, the quantized delay generated by the both SGRO/FGRO is read out by a decoder.

An important issue is the matching between τ_1 and τ_2: if the absolute delays of τ_1 and τ_2 are large, the absolute mismatch is also bound to be large, compared to the Vernier resolution, and this causes a performance degradation.

5.1.2.6 TIME-AMPLIFIER-BASED TDC

Another technique to realize high resolution TDCs is to use time amplification [21][85][88]. In ADCs, voltage amplifiers are considered to be one of the most fundamental building blocks. Their importance comes from the ability to magnify small voltage differences to alleviate some of the stringent requirements necessary for high resolution voltage-based ADC architectures. Similarly, this concept can be borrowed and applied in time-domain applications by introducing the Time Amplifier (TA). The TA plays the same role as the voltage amplifier, but instead of enlarging small voltage differences, it enlarges small time differences introduced by two time events, generally in the form of two rising edge signals. This type of architecture uses a combination of TA

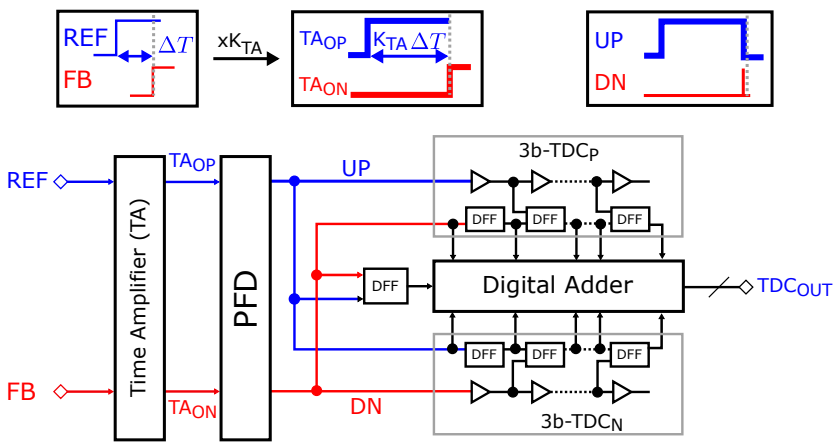


Figure 5.11 TA-based TDC [21].

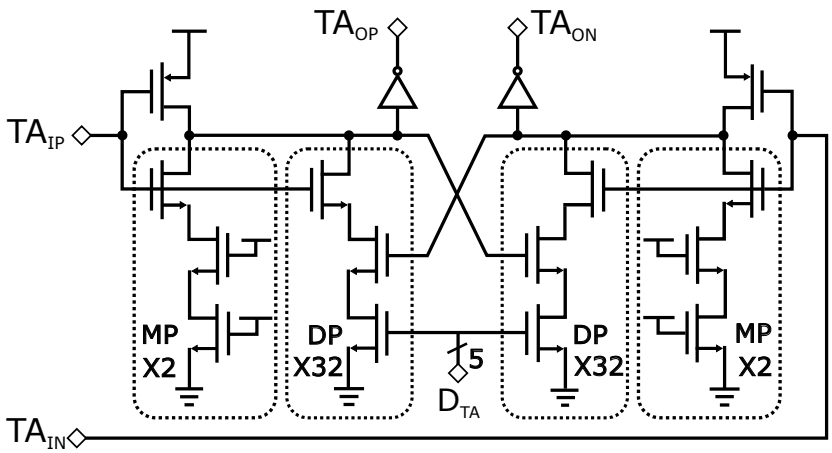


Figure 5.12 Schematic of the fully-symmetric TA [21].

and a low resolution TDC or coarse TDC, for high-resolution measurements, where in [85] a TA is employed in a two-step TDC and a sub-exponent TDC in [88].

In [21], a one-step TA-based TDC has been proposed, and illustrated by the block diagram shown in Figure 5.11. It consists of TA combined with a conventional delay line based TDC. The TA amplifies the input time difference by a gain of K_{TA} , while the delay line based TDC digitizes the TA output. The delay line based TDC quantizes the phase difference between the UP and DN outputs of the PFD with a resolution of one inverter delay. The TA implementation is shown in Figure 5.12. This architecture, however, requires a calibration scheme to accurately determine the TA gain, which adds complexity to the system.

5.2 DTC

The DTC can be formally defined as a device which takes a digital input and converts it into a time instant, i.e., it produces an output signal with a variable delay controlled by a digital word. DTCs come in different architectures. Each architecture is associated with how a controlled delay is generated. Figure 5.13 shows the transfer function of a DTC. The x-axis represents the equivalent decimal of a targeted delay value while the y-axis shows the corresponding output time delay value [22].

The DTC shares most performance parameters with the TDC in terms of time resolution, DR, linearity, area, and power consumption. Therefore, the rest of this chapter focuses only on some DTC architectures.

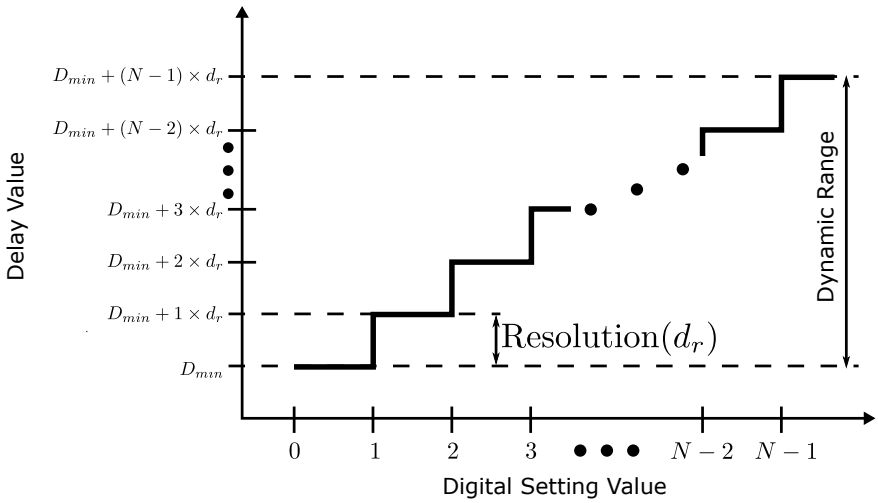


Figure 5.13 DTC transfer function [22].

5.2.1 DTC ARCHITECTURES REVIEW

5.2.1.1 SHUNT-CAPACITOR INVERTER-BASED DTC

Figure 5.14 shows a Shunt-Capacitor Inverter (SCI) schematic. In this topology, N capacitors are employed (NMOS capacitors are used in the figure) as the load to the input inverter via MOS switches. The capacitors can be switched in and out of the circuit by a set of control pins A_1 through A_N. Consequently, the capacitor load can be changed, varying the rise and fall times of the signal. Thereafter, the inverted signal with added delay is inverted back again by

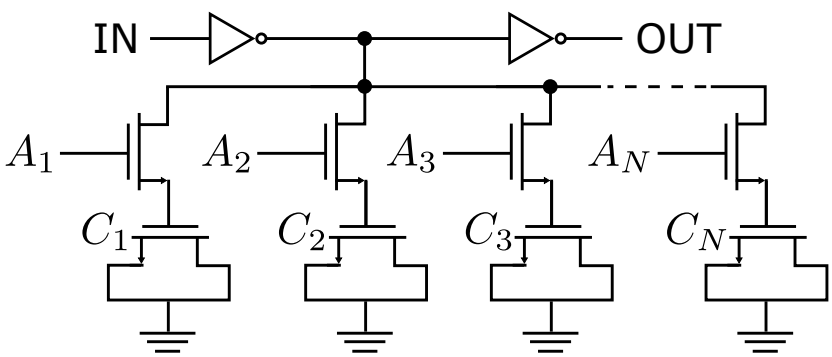


Figure 5.14 An SCI schematic [23].

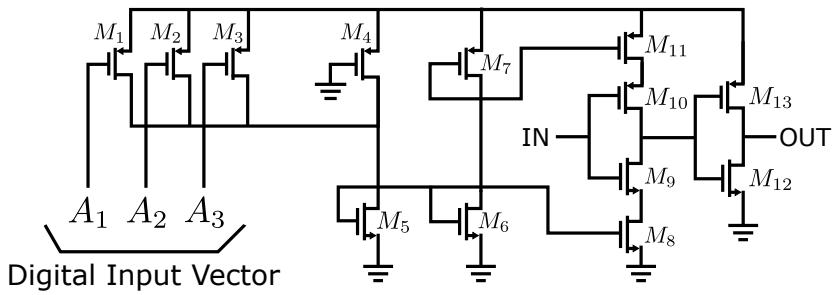


Figure 5.15 An example of CSI architecture [24].

another inverter to resemble the input [23] [82] [87] [98–100]. Accordingly, the total delay is calculated depending on how many capacitors are connected at the same time. This technique is rather power hungry, where its power consumption increases with higher resolution.

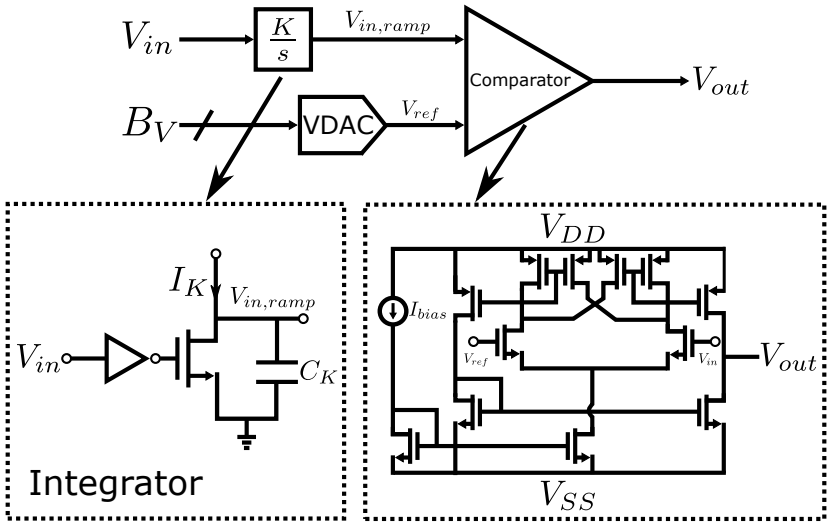
5.2.1.2 CURRENT-STARVED INVERTER-BASED DTC

The Current-Starved Inverter (CSI) structure is shown in Figure 5.15 [24] [101]. The delay of a CSI inverter, constructed by $M_8 - M_{11}$, is controlled by the current I and transistors (M_5–M_7). Meanwhile, the current I is controlled by the PMOS transistors $M_1 - M_3$. The applied digital input through the pins $A_1 - A_3$ turn these transistors on or off. In this way, the current I is determined by the applied digital input. Thereafter, the current I is mirrored to transistors M_8 and M_{11}, where M_8 controls the fall time of the output while M_{11} controls the rise time, resulting in a change in the speed and response of the first inverter. Consequently, a controllable delay is achieved.

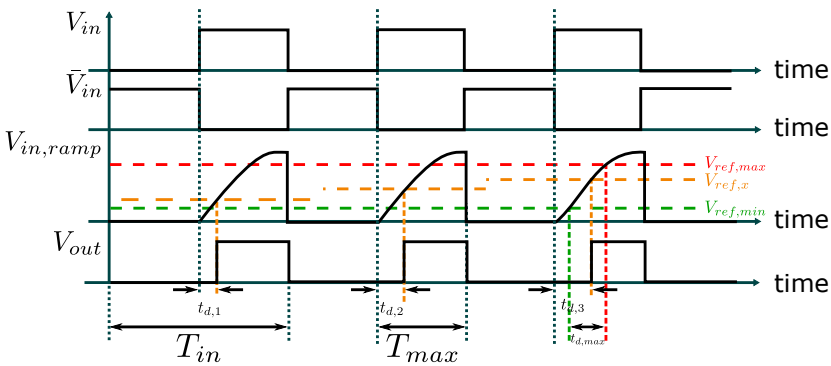
This architecture can be expanded to realize 2^N different delays where N represents the number of PMOS controlling transistors. One important note is that M_9 and M_{10} see the same parasitic capacitances at the source for all the digital input combinations. Hence, a monotonic delay behavior is guaranteed [24] [101]. However, parasitic capacitance of transistors M_1 through M_3 causes non-linear delay steps.

5.2.1.3 VOLTAGE-COMPARATOR-BASED DTC

The architecture consists of a voltage comparator, an integrator, and a DAC, as illustrated in Figure 5.16(a) [25]. The DTC associated waveforms are shown in Figure 5.16(b). The operation starts by inverting the input signal V_{in} to get $\overline{V}_{in}$. Thereafter, it is integrated by the integrator, to produce a ramping signal $V_{in,ramp}$. A comparison is done by the voltage comparator between $V_{in,ramp}$ and a reference voltage V_{ref} that corresponds to a digital word A. Accordingly, by



(a) Voltage-comparator based DTC with schematics of the comparator and the integrator.



(b) Timing diagram showing the operation of the DTC.

Figure 5.16 Voltage-comparator based DTC and associated waveforms [25].

changing the value of A, different delay values can be produced. As an example, Figure 5.16(b) shows different delay values ($t_{d,1}$, $t_{d,2}$, $t_{d,3}$) for different V_{ref} values ($V_{ref,1}$, $V_{ref,2}$, $V_{ref,3}$) , respectively. However, the maximum achievable delay is limited by the input period T_{IN} and the integration constant K, where K can be expressed as

$$K = \frac{I_K}{C_K} = \frac{\Delta V}{\Delta t} \tag{5.8}$$

In reality, enough time margin has to be taken in account for the integrator

to discharge the integration capacitor C_K. This discharge time depends on C_K and the on-resistance of the integrator switch used. The maximum achievable delay depends on the minimum reference voltage $V_{ref,min}$ and the maximum reference voltage $V_{ref,max}$ produced by the DAC. Consequently, this maximum delay can be calculated as

$$t_{delay,max} = \frac{V_{ref,max} - V_{ref,min}}{K} \tag{5.9}$$

The time resolution is

$$t_{delay,LSB} = \frac{V_{ref,max} - V_{ref,min}}{2^{B_V} K} = \frac{V_{ref,LSB}}{K} \tag{5.10}$$

where B_V is the number of bits of the DAC.

5.2.1.4 PHASE INTERPOLATION-BASED DTC

Another way to realize a DTC is by phase interpolation, which can be realized using current sources [102][103], resistors [104][105], or delay lines [27]. The phase interpolation idea is illustrated in Figure 5.17.

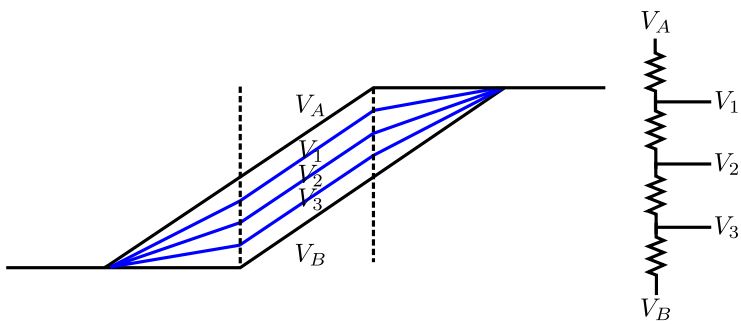


Figure 5.17 Phase interpolation concept starting from two equal-slope signals V_A and V_B, where the interpolated phases ($V_1 - V_3$) have the same slope for the part within the two dashed lines [26].

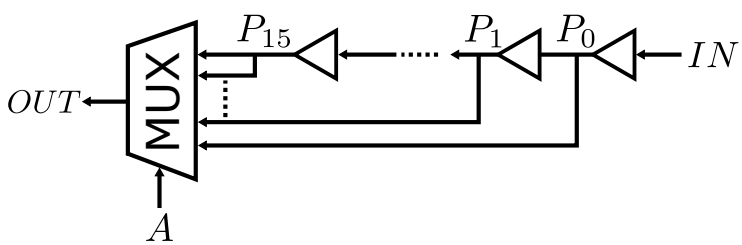
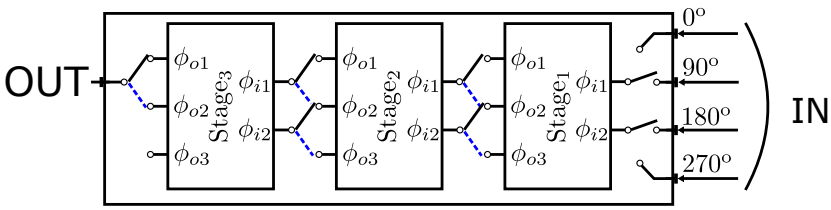
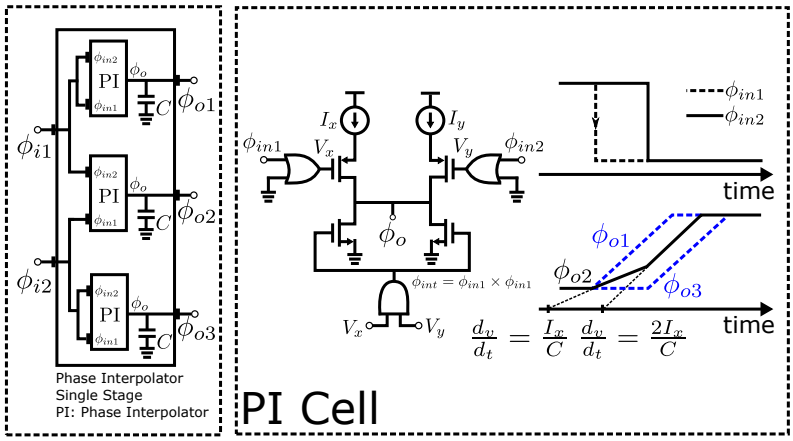


Figure 5.18 Phase interpolator architecture [27].



(a) Block diagram of a 3-bits pipelined phase interpolator.



(b) Circuit schematic of the pipelined phase interpolator.

Figure 5.19 Block diagram and circuit schematic of the pipelined phase interpolator [28].

One possible realization of phase interpolator is shown in Figure 5.18 [27]. The delay line in this example produces 16 phases of the input signal and the multiplexer chooses one of those phases, depending on the value of the digital word A. The delay line consists of a cascade of variable delay stages. However, this architecture is not suitable for wide range applications [35].

Another possible realization of phase interpolator is shown in Figure 5.19(a) [28], which is termed as a pipelined phase interpolator. A circuit schematic of the pipelined phase interpolator is shown in Figure 5.19(b). The figure shows an interpolation between two phases ϕ_{i1} and ϕ_{i2}. The result is three phases ϕ_{o1}, ϕ_{o3} (the inverted version of the original phases) and ϕ_{o2}, the intermediate phase between the two signals. The operation starts by turning on the PMOS transistors when the input ϕ_{in1} goes from HIGH to LOW. At the same time, the NMOS transistors are turned OFF. Accordingly, a current equal to $2I_x$ flows in the load capacitor C, generating the intermediate phase ϕ_{o2} with a slope of $2I_X/C$.

6

Experimental Results

In this chapter, prototypes and experimental results are presented. The first prototype is a 2.8-to-5.8 GHz harmonic VCO based on an 8-shaped inductor in a 28 nm UTBB FD-SOI CMOS process [106] [107]. The second one is a wide band fractional-N DPLL with a noise shaping 2D TDC for LTE-A applications [108] [109]. The third prototype is a 2.8-3.8 GHz Low-Spur DTC-Based DPLL with a Class-D DCO in 65 nm CMOS [110].

6.1 A 2.8-TO-5.8 GHZ HARMONIC VCO BASED ON AN 8-SHAPED INDUCTOR IN A 28 NM UTBB FD-SOI CMOS PROCESS

This section presents a one-octave VCO based on an 8-shaped inductor [76] and a reconfigurable class-B active core design [29] [70]. This VCO has the possibility to switch between two modes, namely single NMOS cross-coupled pair (SP mode) and complementary NMOS-PMOS cross-coupled pair (CP mode) to achieve an efficient power-scalable VCO, where the SP topology reaches a minimum phase noise that is 6 dB lower than what is achievable with the CP topology, but at the cost of a four times higher current consumption. Therefore, SP mode can be used in situations where the phase noise requirement is critical, and CP mode when a more relaxed phase noise performance is allowed. Figure 6.1 shows the simplified schematic view of the VCO. The SP and CP modes share the same tank. The switching between SP and CP modes is achieved by turning on and off the SP and CP switches.

The circuit employed to switch between the SP and CP is an *RC* network, tunable by a PMOS switch M_5, as illustrated in Figure 6.2 and 6.3. The *RC* network is used to decrease the oscillation swing at the gates of M_3 and M_4, when the oscillator switches from CP mode to SP mode. When operating in CP

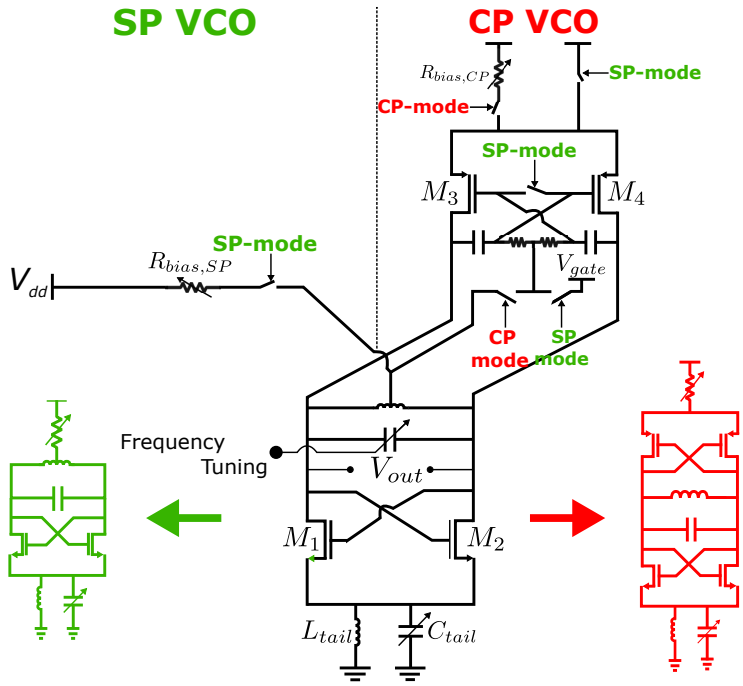


Figure 6.1 Simplified schematic of the VCO, whose active core can be configured either as a single cross-coupled pair (SP, on the left), or as a complementary cross-coupled pair (CP, on the right).

mode (Figure 6.2), the M_3 and M_4 common source is connected to V_{dd} through a switched resistor $R_{bias,CP}$. Meanwhile, the DC voltages at the gates of both transistors are forced to be equal to the common-mode voltage at the VCO output. Concurrently, switch M_5 is turned off. In this case, the AC-coupling circuit between drain and gate has a cut-off frequency of $1/C_bR_b$. The resistor R_b is selected to have a large value, in order to put the cut-off frequency well below ω_{LO}. Consequently, the oscillation at the gates of M_3 and M_4 displays the same swing as the tank oscillation. As a result, transistors M_3 and M_4 contribute the same phase noise as in the case of a standard complementary oscillator.

In the SP mode, M_5 is turned on and both source and gate of M_3 and M_4 are biased to V_{dd}, as shown in Figure 6.3. By doing this, the Ac-coupling network has a high-pass cut-off frequency equal to $2/(C_bR_{on,M_5})$, where R_{on,M_5} represents the M_5 on-resistance. In this case, R_{on,M_5} is chosen to be small enough such that the oscillation swing at the gates of M_3 and M_4 is small, to keep M_3 and M_4 in the off-state and also to maximize the Q of the circuit constructed

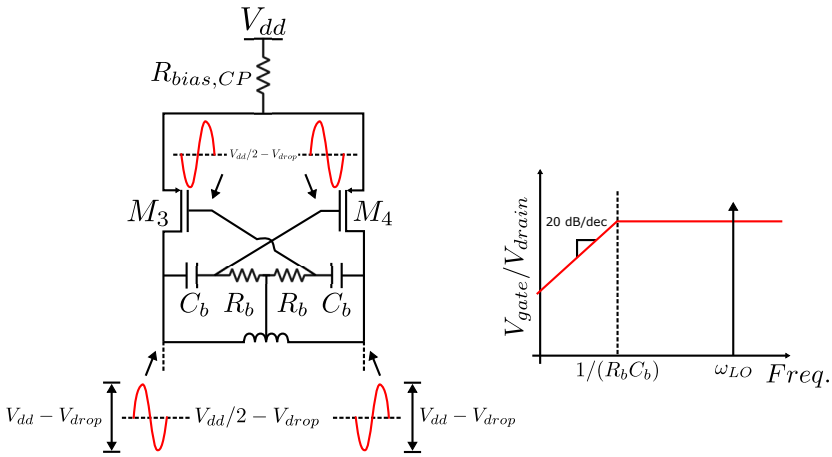


Figure 6.2 Bias circuit in CP mode [29].

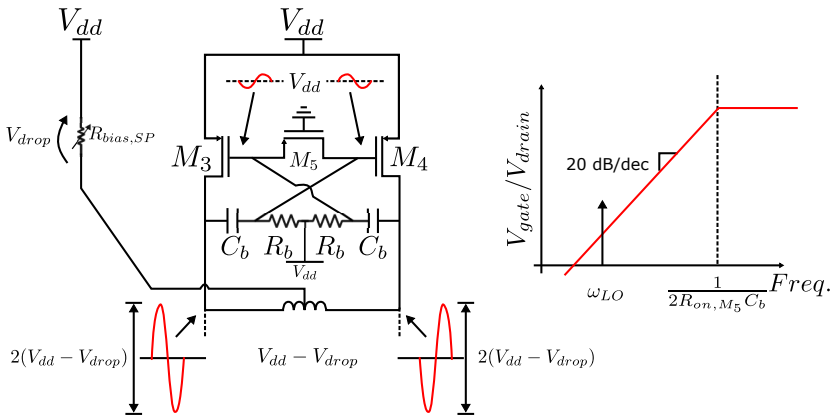


Figure 6.3 Bias circuit in SP mode [29].

by R_{on,M_5} and C_b, to guarantee a negligible impact on the overall Q of the tank.

6.1.1 VCO PROTOTYPE

The VCO prototype has been fabricated in a 28 nm UTBB FD-SOI CMOS process. The VCO has a core area of 380 μm by 700 μm, which includes abundant decoupling capacitance. Figure 6.4 shows the die photo of the VCO. The 28 nm UTBB FD-SOI CMOS process provides two major advantages, compared to the more traditional bulk process, which highly enhance the VCO design:

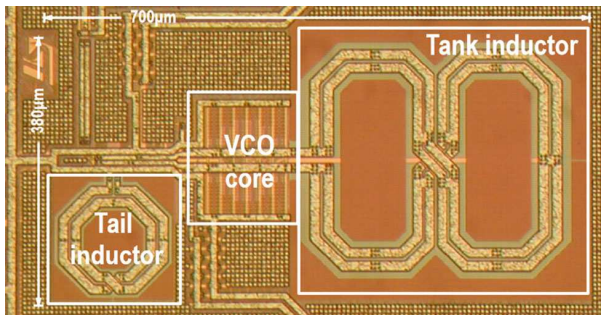


Figure 6.4 Die photograph of the VCO.

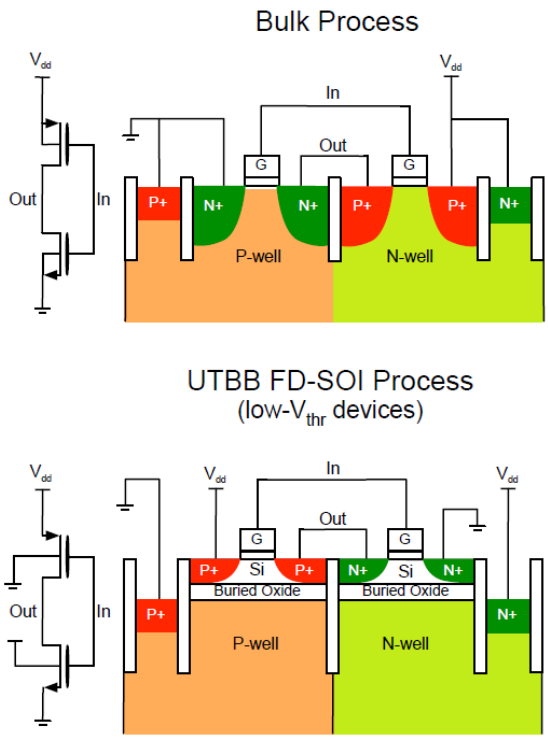


Figure 6.5 In the 28 nm UTBB FD-SOI CMOS process used, it is possible to forward-bias the NMOS/PMOS body to obtain low-V_T devices. Notice that in this case the well types are flipped, compared to a Bulk process or to the normal-V_T devices in the same 28 nm UTBB FD-SOI process, to avoid forward-biasing of the P-well/N-well diode [30].

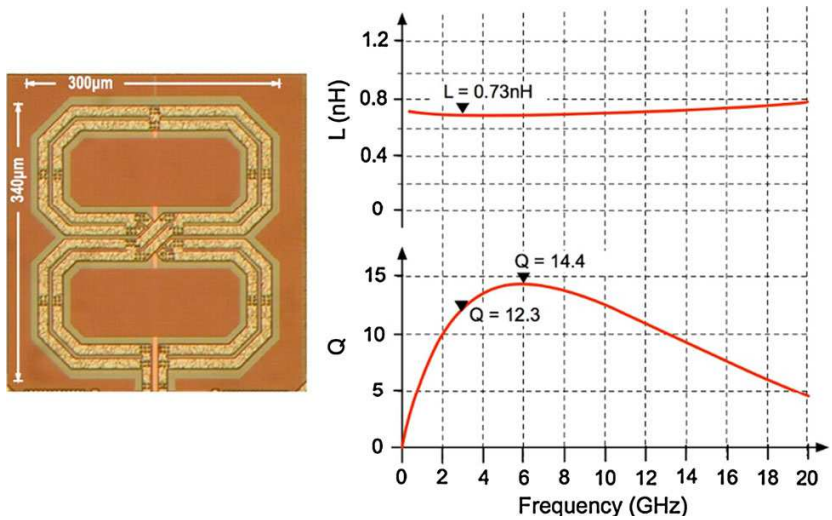


Figure 6.6 The 8-shaped inductor, built with metal layers of standard thickness.

1. The use of ultra-shallow junctions and a total dielectric isolation of the MOS device lead to lower parasitic capacitances (capacitive coupling between source and drain, fringing gate-to-source and gate-to-drain coupling) [30].

2. Furthermore, it is possible to increase the speed of the MOS device by shifting its threshold voltage (V_T) to lower absolute values by biasing its back-gate to the power supply V_{dd} in NMOS devices, and to ground in PMOS devices (instead of the opposite, as in a bulk process, as shown in Figure 6.5).

These two advantages greatly improve frequency tuning via capacitance switching, yielding a higher ratio of on- to off-capacitance, C_{on}/C_{off} [111], for a given quality factor Q_{on} of C_{on}. In our case, for a Metal-Insulator-Metal (MIM) capacitor with C_{on} = 60 fF, we obtain C_{on}/C_{off} = 7 (after post-layout simulations, since interconnect parasitic capacitance dominates over MOS capacitance) together with a Q_{on} of 30 at 6 GHz.

The VCO employs a 0.73 nH 8-shaped inductor to reduce its magnetic coupling, as already discussed (see Section 4.6). Such a relatively high inductance value (in the context of a one-octave VCO design) is allowed by the very low overall parasitic capacitance in parallel to it. A coil-Q of 14.4 is obtained at 6 GHz, despite the lack of thick metal layers (as no process options were used beyond the standard digital flavor), while fully complying with the very se-

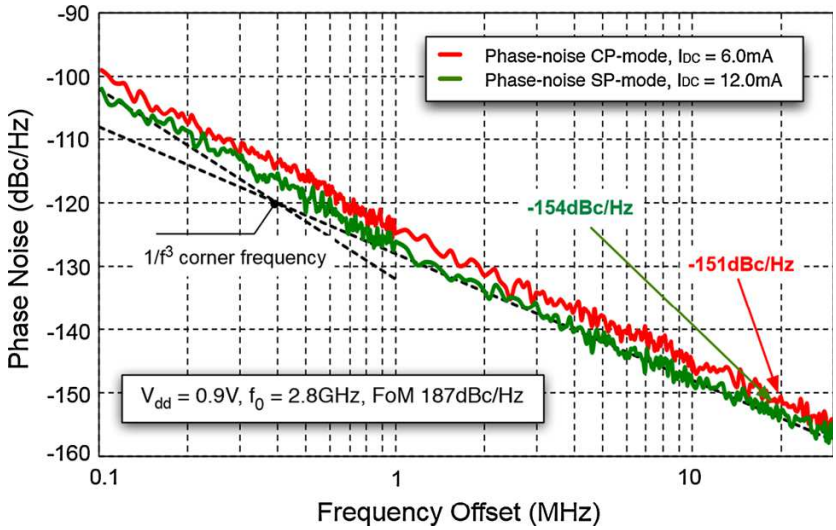


Figure 6.7 Phase noise measurements at the lowest oscillation frequency.

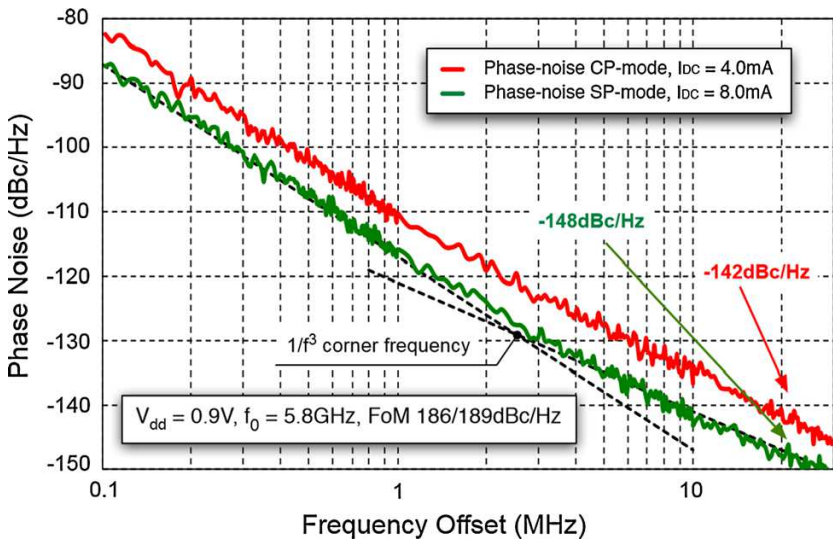


Figure 6.8 Phase noise measurements at the highest oscillation frequency.

vere dummy metal filling rules of the 28 nm back-end lithography. Figure 6.6 shows inductance, Q and layout of the 8-shaped inductor.

Frequency tuning is performed with a 6-bit coarse MIM capacitor bank with the mentioned unit capacitance C_{on} = 60 fF (where the two MSBs are thermo-

Table 6.1 Comparison with state of the art VCOs having a tuning range larger than one octave.

	This work	[9]	[8]	[11]	[69]
TR (GHz)	**2.8–5.8 (70 %)**	2.5-3.9 3.3–5.6 (76 %)	2.4–3.6 3.4-5.3 (75 %)	3.2-8.5 (89 %)	3.3-6.0 5.6–8.3 (86 %)
Type	**Single band**	Mode switching	Core switching	Inductor with cold switch	Inductor switching
Rejection of external magnetic field	**Yes**	No	Yes	Yes	No
Supply voltage (V)	**0.9**	0.6	0.4	0.8	1.6
Current (mA)	**SP: 12–8 CP: 6–4**	16-23	15-11 15-11	25	9.5-4.0 9.5-4.0
Power (mW)	**10.8–3.6**	9.5-14.0	6.0–4.4	20	15.5–6.5
Phase noise (dBc/Hz)	**SP:-154/-148 CP:-151/-142**	-157/-152	-149/-139	-150/-144	-122/-117
Offset (MHz)	**20**	20	10	10	1
Carrier (GHz)	**2.8/5.8**	3.7/5.5	2.4/5.3	3.7/7.8	3.3/7.8
FOM (dBc/Hz)	**186/189**	188/192	187/189	188/189	181/187
Area (mm^2)	**0.27**	0.29	0.34	0.43	0.87 (with pads)
Technology	**28 nm UTBB FD-SOI CMOS**	65 nm CMOS	65 nm CMOS	40 nm CMOS	130 nm CMOS

metric to enhance linearity) and a 6-bit fine Metal-Oxide-Metal (MOM) capacitor bank covering 3 coarse-tuning steps. The same circuitry as in [10] was used to speed-up the frequency response of the VCO, which is crucial to enable wideband frequency modulation. As shown in Figure 6.1, a tail coil resonating at twice the oscillation frequency [112] is used to improve the phase noise performance, particularly in the $1/f^3$ region. Since the TR is very wide, the tail resonance is tuned by a 2-bit capacitor array, controlled by the two MSBs of the coarse frequency tuning. As the tail coil is small and does not belong to the VCO tank, it does not need to be 8-shaped. The current drawn by the VCO is controlled by a 4-bit switched resistor, and the oscillation amplitude is monitored by a linear 4-bit amplitude detector similar to the one described in [113]. Under test, it produces all binary codes up to 1100, corresponding to a simulated peak oscillation of 700–750 mV.

6.1.2 MEASUREMENT RESULTS

All measurements were performed with a V_{dd} of 0.9 V. The TR is between 2.8 GHz and 5.8 GHz, approaching 70 %. Figures 6.7 and 6.8 plot the phase noise at the lowest and highest frequencies, both in SP and CP modes. The lowest phase noise at 2.8 GHz is obtained in SP mode, with -154 dBc/Hz at 20 MHz frequency offset from the carrier and a current of 12 mA, while CP mode delivers -151 dBc/Hz at 6 mA; in both cases, the FOM is 187 dBc/Hz. At 5.8 GHz, SP mode yields -148 dBc/Hz at 8 mA, with a FOM of 189 dBc/Hz, while CP mode yields -142 dBc/Hz at 4 mA, for a FOM of 186 dBc/Hz. The

$1/f^3$ phase noise corner varies between 300 kHz and 3 MHz. Table 6.1 shows the comparison between this VCO with the state-of-the art VCOs with a TR in excess of one octave. The presented VCO has a competitive core area together with a very good phase noise and FOM performance, while also ensuring the rejection of external magnetic fields and producing itself a vanishing magnetic field.

6.2 A WIDE BAND FRACTIONAL-N DPLL WITH A NOISE SHAPING 2D TDC FOR LTE-A APPLICATIONS

The proposed fractional-N DPLL is shown in Figure 6.9. In this type of DPLL, the TDC detects the phase and frequency errors between the reference clock (REF) and feedback clock (CKV), then it converts this phase error to a digital word to control the DCO after filtering by a low-pass DLF, as explained in Section 3.2. The TDC works like a charge pump whose input phase error may vary in the whole reference clock period; therefore, a TDC with large detection range is needed. As described in Section 5.1.1.1, the TDC resolution is a key parameter for achieving high performance. The proposed 2D GVTDC of Section 5.1.2.5 meets this requirement with a super fine resolution and noise shaping to achieve low phase noise performance, while, at the same time, its small latency guarantees a fast phase capturing for fast frequency locking.

The class-D DCO makes it is possible to combine low phase noise, low supply voltage and high power efficiency. The class-D DCO has three tuning banks: coarse, medium and fine. It operates as follows: in the beginning of the operation the coarse bank is activated, until the coarse control word becomes stable, then the medium bank is activated and it operates in the same way as the coarse bank. Finally, the fine bank is activated, which determines

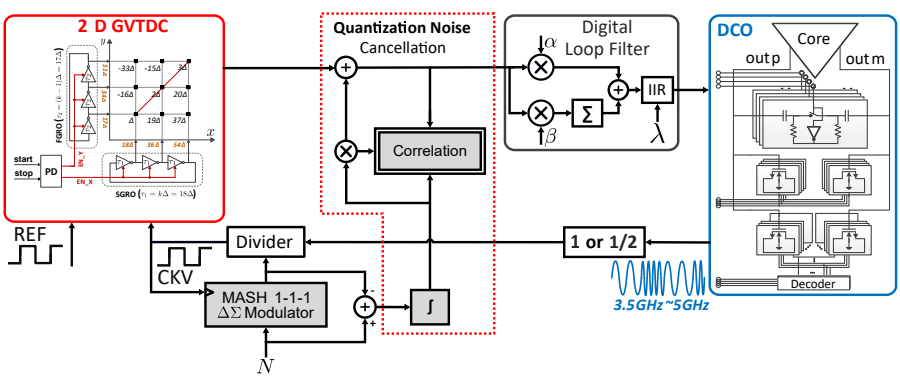


Figure 6.9 Block diagram of the DPLL.

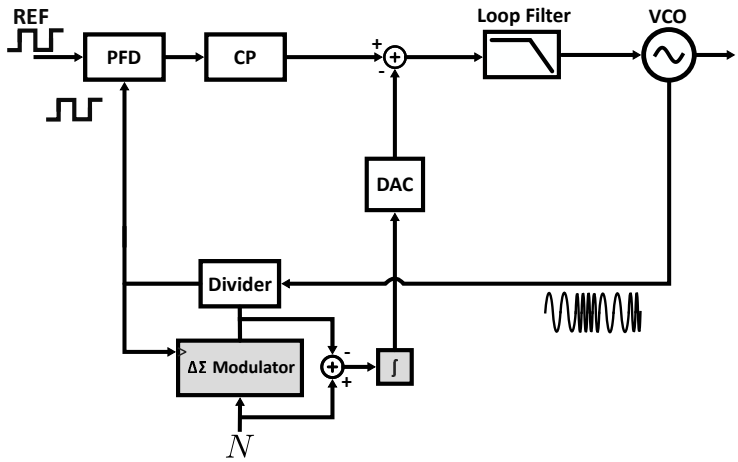


Figure 6.10 Conventional fractional-N analog PLL with ΔΣ quantization noise cancellation scheme.

the resolution of the DCO in the locked state.

The DLF, similar to an analog loop filter, consists of a proportional path scaled by α and an integrated path scaled by β. A zero and a pole (locate at the origin) are generated, with the same effect as a simple series connection of R and C in an analog PLL. A 7-bit MASH 1-1-1 ΔΣ modulator with a 1-bit pseudo-random dithering generates the dynamic division values with the frequency jump step of $f_{ref}/128$, where f_{ref} is the frequency of the reference clock. Because of the use of MASH 1-1-1 ΔΣ modulator, a higher-order loop filter is necessary to get at least -20 dB/dec attenuation for fractional division quantization noise. In this work, a changeable-order Infinite Impulse Register (IIR) filter is inserted after the regular DLF filter.

This work targets LTE-A bands 33-38 where the frequency range is from 1900 to 2620 MHz. The DCO tuning range is from 3.5 to 5 GHz, and a divide-by-2 prescaler is placed after the DCO.

6.2.1 LMS BASED QUANTIZATION NOISE CANCELLATION

Another major source that limits higher bandwidths is the noise folding due to the quantization noise of the ΔΣ modulator, used to dither the divider to achieve fractional operation. This dithering produces high-pass shaped noise, which degrades the output phase noise performance and modulates the oscillator output, causing fractional spurs (see Section 3.2.3).

In order to alleviate the impact of the ΔΣ modulator and achieve low phase noise and low spurs with high bandwidth in a conventional fractional-N ana-

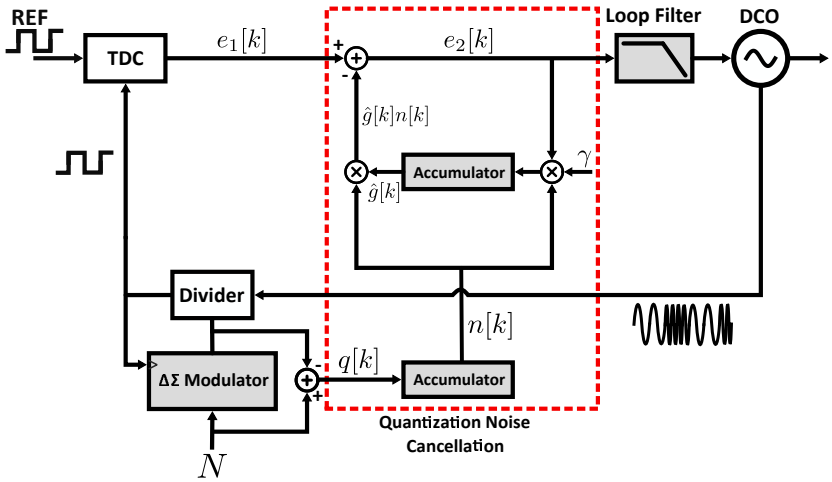


Figure 6.11 DPLL with ΔΣ quantization noise cancellation scheme.

log PLL, a quantization noise cancellation path composed of a current DAC is introduced. The cancellation is achieved by first integrating the quantization noise error obtained by subtracting the output of the ΔΣ modulator from its input, then subtracting the output of the integrator from the output of the charge pump by using a current DAC (Figure 6.10). Unfortunately, because of components mismatches, the gain of the DAC is never perfectly matched to that of the signal path, and there is always a residue that modulates the output of the VCO causing spurs. So, to improve the cancellation, a very complicated analog calibration circuits with high power consumption and large area are needed [114–116].

On the other hand, a DPLL can avoid using a DAC with a complex calibration scheme and matching limitations of analog components. This can be done by employing two techniques. Firstly, by using a DTC in the feedback path with a single bit phase detector, to cancel the quantization noise at the output of the fractional divider [35]. However, the non-linearity of the DTC as a result of the mismatch between delay cells degrades the spurious tones and in-band phase noise of the PLL (see Section 3.3.1.2). Also, the gain of the phase detector in this type of PLLs depends on the noise at its input, which has two important consequences. Firstly, the loop dynamics is difficult to control. Secondly, the PLL bandwidth is sensitive to the amount of noise injected at the input of the phase detector, as explained in details in Section 3.3.1.

The second quantization noise cancellation uses digital algorithms that are able to extract the quantization error, then using digital LMS algorithms that are able to estimate the same gain of the signal path through the TDC in

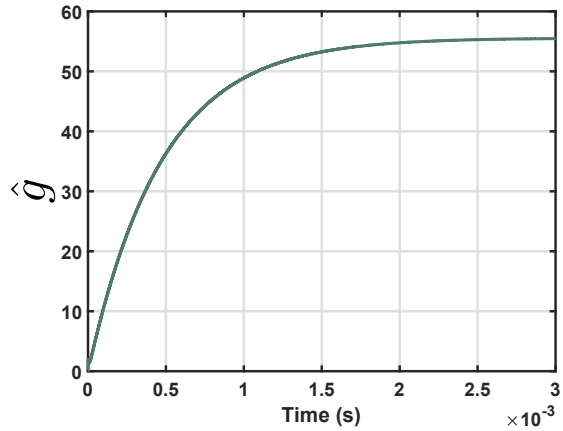


Figure 6.12 Simulated LMS coefficient.

the digital domain and finally subtract the scaled quantization noise at the output of the TDC (Figure 6.11). This cancellation scheme requires a high-performance wide-range TDC, such as the 2D GVTDC used in this work.

The operation of the digital cancellation algorithm starts in a similar way as in the analog fractional-N PLL, by first extracting the quantization error of the $\Delta\Sigma$ modulator $q[k]$, then accumulating it as $n[k]$, then using an LMS algorithm to correlate between the output of the accumulator and the output error from the TDC. The output from the correlator is accumulated to get the proper gain

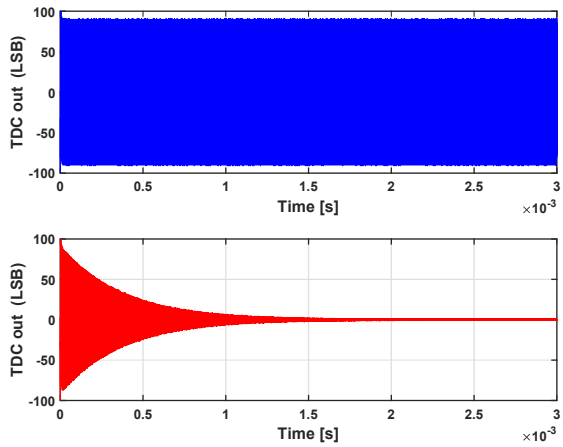


Figure 6.13 The output of TDC with and without enabling $\Delta\Sigma$ quantization noise cancellation circuit.

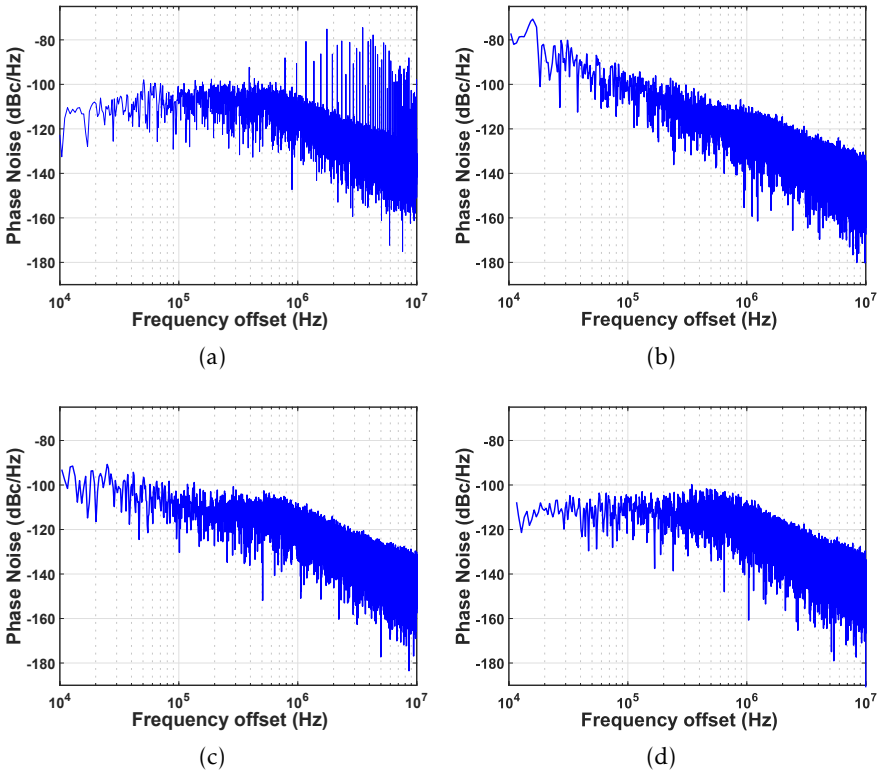


Figure 6.14 a) Simulated phase noise of DPLL without enabling $\Delta\Sigma$ quantization noise cancellation, b) Simulated phase noise of DPLL with enabling $\Delta\Sigma$ quantization noise cancellation and $\gamma = 10^{-2}$, c) Simulated phase noise of DPLL with enabling $\Delta\Sigma$ quantization noise cancellation and $\gamma = 10^{-3}$, and d) Simulated phase noise of DPLL with enabling $\Delta\Sigma$ quantization noise cancellation and $\gamma = 10^{-4}$.

$\hat{g}[k]$. This estimated gain converges to the same value of the gain of the signal path through the TDC (Figure 6.12). This gain is multiplied by $n[k]$, and finally is subtracted from the output of the TDC. Figure 6.13 shows the output of the TDC before and after enabling the quantization noise cancellation circuit.

The convergence speed of the quantization noise cancellation can be controlled by changing the LMS coefficient γ. Unfortunately, speeding up the settling time of the algorithm comes with the price of larger fluctuations of the estimated gain, which make the cancellation of the quantization noise imperfect, causing a degradation in phase noise performance and spurs level at the output of the DCO [33][117]. Matlab simulations have been performed for a

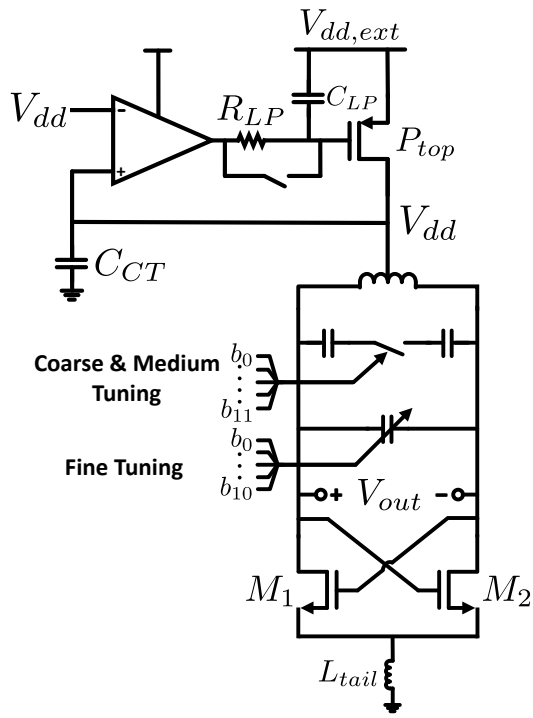


Figure 6.15 Schematic view of the class-D DCO.

1-MHz bandwidth with a 50-MHz reference clock using different values of γ (10^{-2}, 10^{-3} and 10^{-4}). The settling time decreases with increasing γ, but at the same time a degradation in phase noise is observed, as the estimated gain suffers from larger fluctuations, which have a large impact on the phase noise performance, as mentioned (shown in Figure 6.14(a)–(d)). Therefore, the value of γ should be carefully chosen, depending on the application, through simulations, in order to achieve the required settling time and the required phase noise.

6.2.2 SUBBLOCKS

6.2.2.1 CLASS-D DCO

To improve the overall DPLL performance, we have targeted the class-D architecture [118] [119] for the DCO design, for this DPLL design and the next design as well, as shown in Figure 6.15. The reason is the excellent phase noise performance of the class-D oscillator, combined with a superior voltage and power efficiency (in excess of 90%). In fact, it will be remembered that the

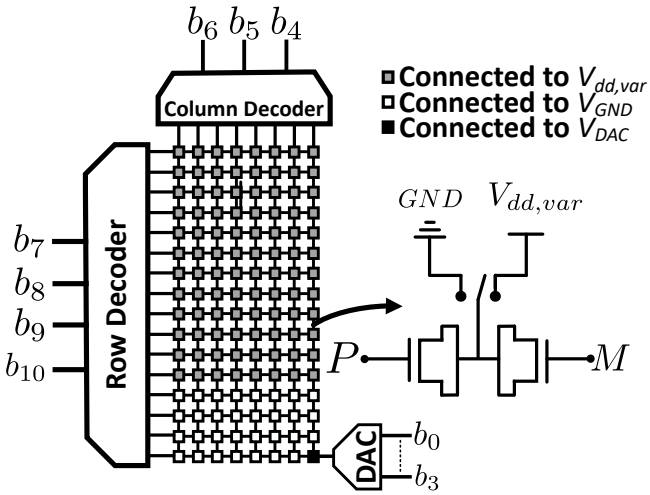


Figure 6.16 Fine tuning bank of the DCO.

class-D oscillator operates in voltage mode, avoiding the voltage drop (with attending efficiency deterioration) on the current-bias circuitry typical of e.g. class-B/class-C topologies. A correctly designed class-D oscillator (i.e., with very wide cross-coupled MOS devices) shows a single-ended oscillation peak close to $3V_{dd}$, rather than the (unreachable) maximum of $2V_{dd}$ of class-B/class-C implementations.

A drawback of the class-D topology is the high supply pushing, which can turn disturbances on the power supply into a relatively high phase noise. This is all the more relevant when the DCO is embedded in a DPLL, where the large digital core generates a substantial amount of digital noise. To obviate this problem, we have co-designed the class-D DCO together with a fully integrated Low-Drop-Output Regulator (LDO), which generates a clean power supply for the DCO [119]. From a $V_{dd,ext}$ of 0.8 V, we obtain a clean V_{dd} of 0.4-0.5 V, which leaves an ample margin for the LDO power device P_{top}. A tail inductor which provides a high resistance at high frequencies to the ground is also added to improve the phase noise performance, especially in the $1/f^3$ region [112].

In the DCO core, there are three capacitor banks for coarse, medium and fine frequency tuning. For coarse and medium tuning, 6-bit low-loss MOM capacitor arrays are used. Fine tuning uses a compact 7-bit MOS varactor array, with 4 additional ultra-fine LSBs obtained by biasing one MOS varactor via a resistive DAC [14] (Figure 6.16).

In this design, the DCO oscillates between 3.5 GHz and 5.0 GHz. The fine tuning uses the capacitive division method [13], which greatly reduces the fre-

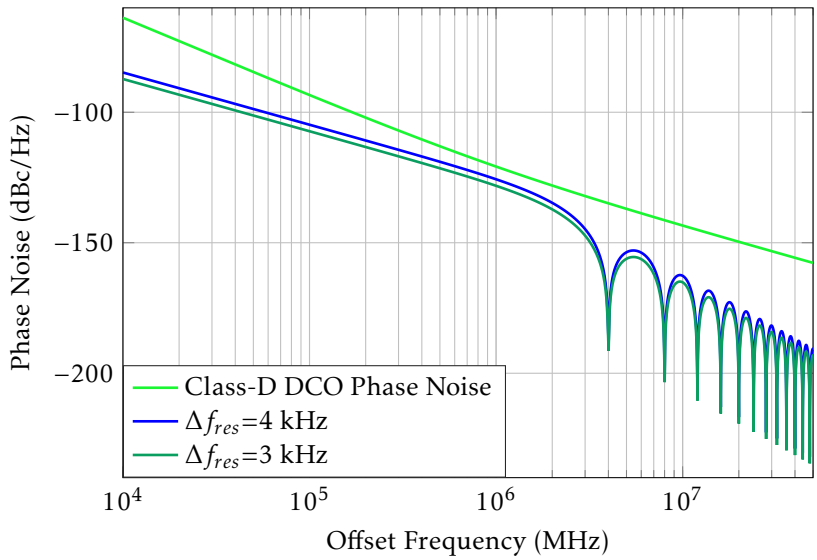


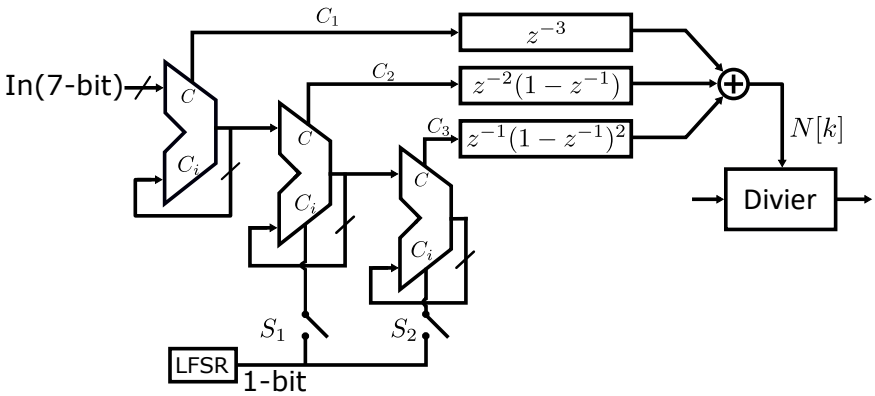
Figure 6.17 Matlab simulations showing the phase noise of the class-D DCO with the DCO quantization-induced phase noise when Δf_{res}=4 kHz and 3 kHz.

quency tuning step of the DCO (see Section 4.5.2.2). The DCO frequency step reaches 4 kHz without any dithering, which translates into an utterly negligible contribution of the DCO quantization-induced phase noise to the overall DPLL phase noise, as shown in Figure 6.17.

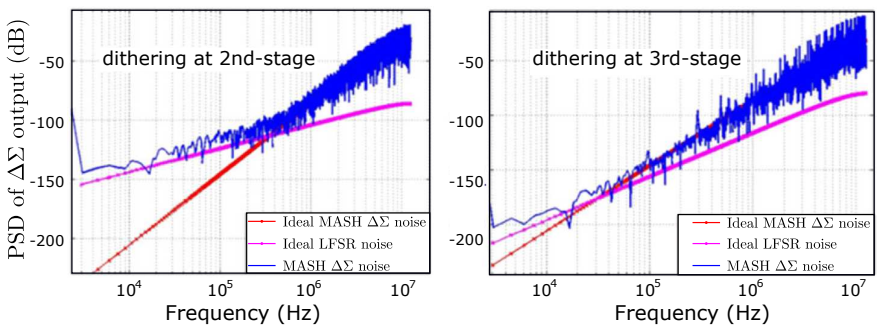
In the second design, the DCO oscillates between 2.8 GHz and 4.1 GHz. Also, the capacitive division method [13] is not used. The implemented DCO has a very fine (average) measured resolution of 3 kHz, which also translates into an utterly negligible contribution of the DCO quantization-induced phase noise to the overall DPLL phase noise (see Figure 6.17).

6.2.2.2 DIVIDER AND MASH 1-1-1 ΔΣ MODULATOR

A multiple-mode frequency divider is used to generate a fractional frequency resolution with respect to f_{ref} by averaging no less than two division values. To avoid the periodical repeat pattern and the subsequent fractional spurious tones, a MASH 1-1-1 ΔΣ modulator is preferred to randomize the output and push most of ΔΣ quantization noise out of the loop bandwidth. Digital MASH ΔΣ modulator can be realized by cascading accumulators and summing their weighted outputs, as shown in Figure 6.18(a), and explained in Section 3.2.1.4. Unfortunately, the randomization is often insufficient, so spurs still appear in



(a) MASH 1-1-1 ΔΣ modulator diagram.



(b) MASH 1-1-1 ΔΣ modulator simulated PSD.

Figure 6.18 MASH 1-1-1 ΔΣ modulator diagram and simulated PSD.

its spectrum, as well as at the DPLL output. A 16-bit Linear Feedback Shift Register (LFSR) is therefore employed to further dither the division value, but inevitably introduces extra noise floor. Figure 6.18(b) shows the simulated output PSD of the MASH ΔΣ modulator. Injecting a pseudo-random bit to the second stage gives a better dithering, compared to injecting it into the third stage, but with the penalty of worse low-frequency noise floor.

The MASH 1-1-1 ΔΣ modulator produces the frequency control word (division value) which varies within 8 values (having a constant average) to the divider. The divider is required to process multiple division values for a fixed fractional N. Such a multiple-mode frequency divider is usually implemented using cascaded 2–3 dividers, as shown in Figure 6.19. The division value is given by the binary number "$p6$-$p0$", generated by the MASH 1-1-1 ΔΣ modulator.

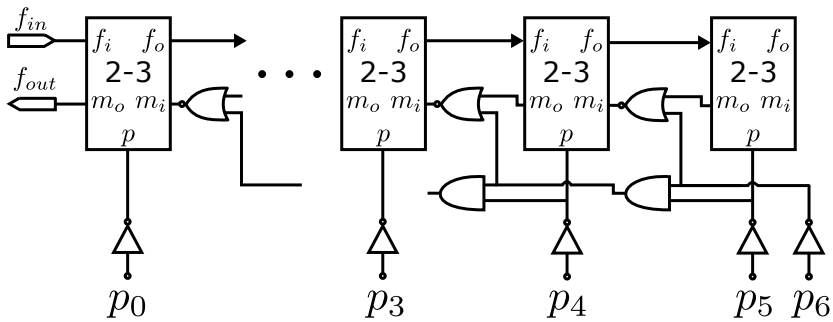


Figure 6.19 Multiple-mode frequency divider.

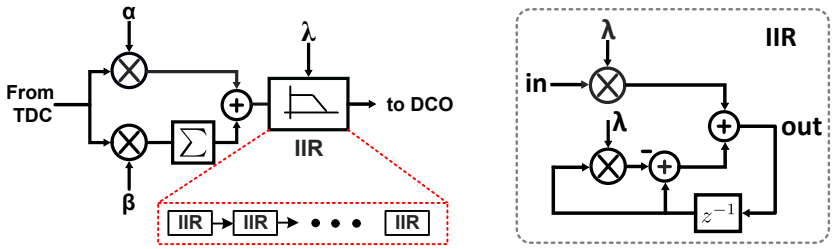


Figure 6.20 DLF and IIR details.

6.2.2.3 DIGITAL LOOP FILTER

The DLF includes two parts: a regular digital filter consisting of a proportional path scaled by α and an integral path scaled by β (see Section 3.2.1.3), and an IIR filter, as detailed in Figure 6.20. The complete transfer function of the DLF is

$$H_{DLF} = (\alpha + \frac{\beta}{1-z^{-1}})(\frac{\lambda}{1-z^{-1}(1-\lambda)})^n \tag{6.1}$$

By replacing z by $1 - sT_{ref}$ to get the s-domain expression

$$H_{DLF} = (\alpha + \frac{\beta}{sT_{ref}})(\frac{1}{1-sT_{ref}(1-1/\lambda)})^n \tag{6.2}$$

where n is the IIR stage number. Five series IIRs stages are used in this design, where the number of stages are selected depending on the bandwidth and the noise requirement. The more the stages involved, the worse the open-loop phase margin, but the better the far-out noise suppression.

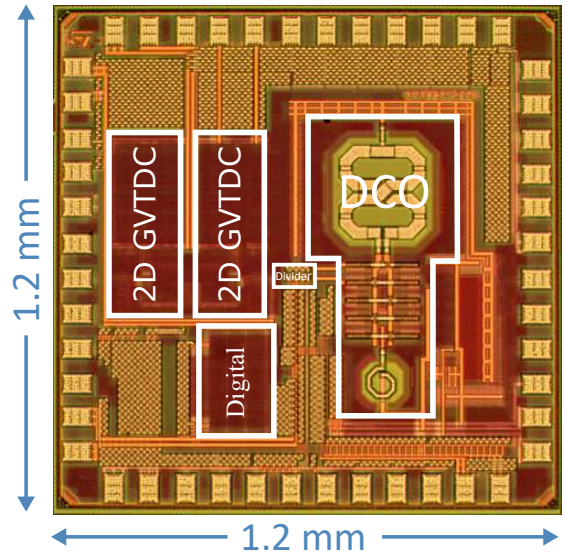


Figure 6.21 DPLL chip layout.

6.2.3 SIMULATION RESULTS

The DPLL is designed and fabricated in a 65-nm CMOS process. However, it did not work properly, as the output was too small and we did not able to measure it. Figure 6.21 shows the whole chip photo, where a replica of the TDC is included for the aim of standalone TDC measurement. The chip occupies 1.2 mm × 1.2 mm (including all pads and decoupling capacitors for power supplies) and consumes 11.2 mW under 1.0 V power supply.

AMS is used to run analog behavioral-level and digital post-layout mixed-signal simulations. The TDC resolution is set to 5.2 ps by an automatic digital calibration. The DCO is also coded at the RTL level with the phase noise obtained from post-layout simulation in Cadence. Transient simulations were done in Modelsim and Matlab, and continuous DCO periods (or zero-crossing time) are collected for the phase noise analysis. A 50-MHz reference clock is used and the worst case division value of 71.9921875 is simulated (near integer division value) with 1-MHz bandwidth. The total noise estimation based on the TDC quantization noise and DCO phase noise can therefore be given in Figure 6.22. As illustrated in Figure 6.22, simulated worst case phase noise at 900 kHz and 10 MHz offsets frequency are -110 and -140 dBc/Hz, respectively, with an overall jitter equal to 204 fs. Considering thermal noise and flicker noise of the devices, the in-band noise should have a flat noise floor, as illustrated by the red line in Figure 6.22. Figure 6.22 shows also the two spec-

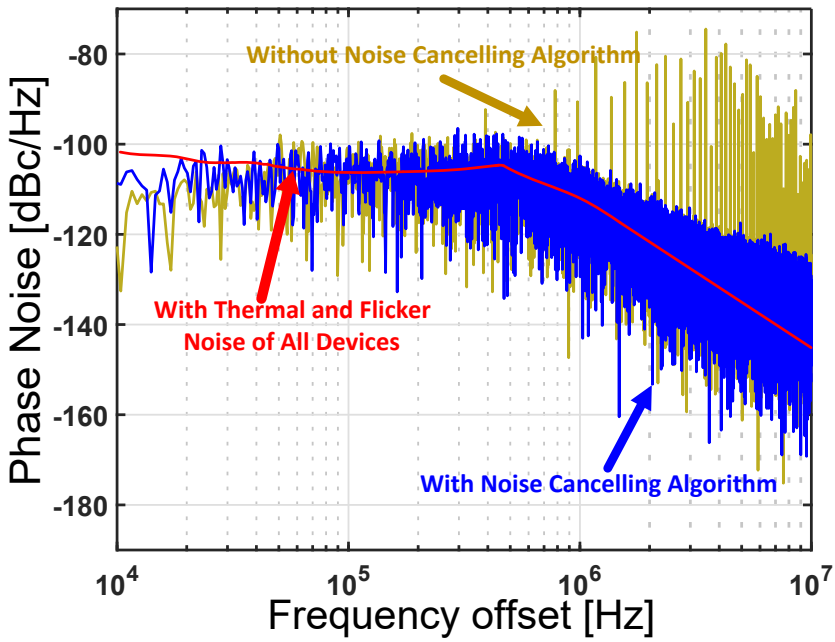


Figure 6.22 Simulated DPLL phase noise at 3.5 GHz with a 50-MHz reference clock with and without enabling ΔΣ quantization noise cancellation.

Table 6.2 Comparison with state of the art DPLLs.

	[35]	[13]	[34]	[38]	**This work[a]**
Output carrier frequency (GHz)	3.7	3.2	5.3	3.5	**3.5**
TR (GHz)	–	2.9–4	4.9–6.9	–	**3.5–5**
Phase noise (dBc/Hz)	-150@ 20 MHz	-118@ 3 MHz	-114@ 1 MHz	-151@ 20 MHz	**-140@ 10 MHz**
Normalized phase noise (dBc/Hz)	-222	-215	-215	-210	**-224**
Feature Size	65-nm CMOS	65-nm CMOS	65-nm CMOS	65-nm CMOS	**65-nm CMOS**
Reference (MHz)	50	40	48	26	**50**
Power consumption (mW)	39	4.5	20	15.6	**11.2**
Max PLL bandwidth (MHz)	0.5	0.3	0.8	0.14	**1**

[a]Simulation results

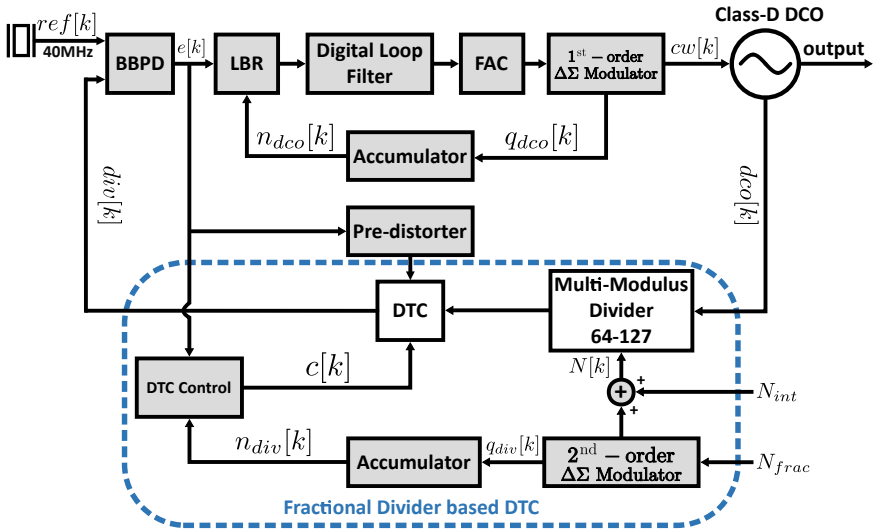


Figure 6.23 Overall DPLL architecture.

tra obtained with and without enabling the ΔΣ quantization noise cancellation algorithm.

Table 6.2 provides a performance comparison between this work with the state-of-the art DPLLs. For fair comparison of this work and previous works with different reference and carrier frequencies, normalized phase noises using Banerjee's figure of merit (BFM) [120] is presented. It should be noticed that simulation results in this work are compared with measurement results for works stated in the table. The normalized phase noise in this work is lower than other designs (-224 dBc/Hz) with low power consumption 11.2 mW and wide bandwidth (up to 1 MHz).

6.3 A 2.8-3.8 GHZ LOW-SPUR DTC-BASED DPLL WITH A CLASS-D DCO IN 65 NM CMOS

Figure 6.23 shows the system architecture of the second designed DPLL, where the blocks in gray have been implemented with standard digital cells. The forward path in the main loop includes a BBPD, a DLF, and a 1^{st}-order ΔΣ modulator dithering the finest control of the class-D DCO, while the main blocks on the feedback path are an integer MMD and a DTC. The 40 MHz reference signal is generated by an on-chip Pierce oscillator with an external crystal resonator. The main DPLL loop is assisted by 1) DTC control, 2) an FAC to speed up frequency acquisition, 3) an LBR, and 4) a digital pre-distorter to

improve DTC linearity.

As shown in Figure 6.23, the BBPD compares the phase of the reference signal (ref) with that of the frequency-divided DCO output (div), delivering a single-bit signal to the DLF, which in turn generates the digital tuning word for the DCO. The fractional frequency divider uses a DTC cascaded to an MMD controlled by a 2^{nd}-order $\Delta\Sigma$ modulator, which modulates the 10-bit fractional frequency division factor.

The FAC is wholly digital, requiring no additional analog blocks (e.g., coarse TDCs [35] and RF counters [121]), as explained in Section 3.3.1.4. Our approach relies instead on a gear-shifting algorithm in the DLF [122], which amplifies the loop filter coefficients by a programmable factor at the beginning of the coarse frequency acquisition and progressively scales them down to their nominal values at fixed time intervals. A fast and reliable frequency acquisition (lasting 160 μs at most) is achieved, despite the limited capture range of the BBPD (Figure 3.31 and 3.32).

6.3.1 CIRCUIT IMPLEMENTATION

6.3.1.1 DTC AND FRACTIONAL FREQUENCY DIVIDER

The fractional frequency division factor $N[k]$ generated by the 2^{nd}-order $\Delta\Sigma$ modulator toggles between the integer factors $N_{int}-1$, N_{int}, $N_{int}+1$ and $N_{int}+2$. At the same time, a quantization error (QE) is also generated and injected into the loop, giving rise to a limit cycle and, hence, to fractional spurs in the DCO spectrum. Fortunately, QE suppression can be implemented very effectively via the DTC, whose task is to produce a delay matching QE. The absolute value of the DTC delay is set according to the output of an LMS algorithm continuously running in the background [35]. By enforcing that the surviving QE at the BBPD input is below the level of thermal noise there, the latter is able to destroys any cyclic QE pattern, eliminating fractional spurs from the DPLL spectrum [35], as explained in details in Section 3.3.1.

The DTC consists of a current-mode inverter loaded by a parallel RC network with a digitally-controlled capacitor, implemented with a 6-bit thermometric coarse MOM capacitor array and a 6-bit thermometric fine inversion-mode-NMOS varactor array, for a fine resolution of 340 fs, (see Figure 6.24). The fine array covers 1.5 steps of the coarse array, which ensures a continuous DTC input-output characteristic in the presence of PVT variations. Finally, to accommodate again PVT variations, the DTC delay spans three times the maximum DCO period, corresponding to the lowest frequency of 2.8 GHz (a DTC range of 2 DCO periods is required by the dynamic range of the accumulated $\Delta\Sigma$ modulator QE n_{div}, see Figure 6.23).

The signal controlling the DTC delay is obtained in two steps, one for coarse and one for fine tuning, as shown in Figure 6.25. In the first step, QE is ex-

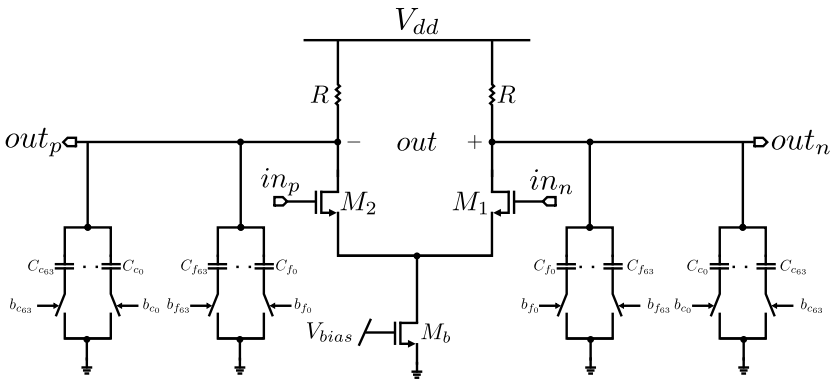


Figure 6.24 DTC implementation.

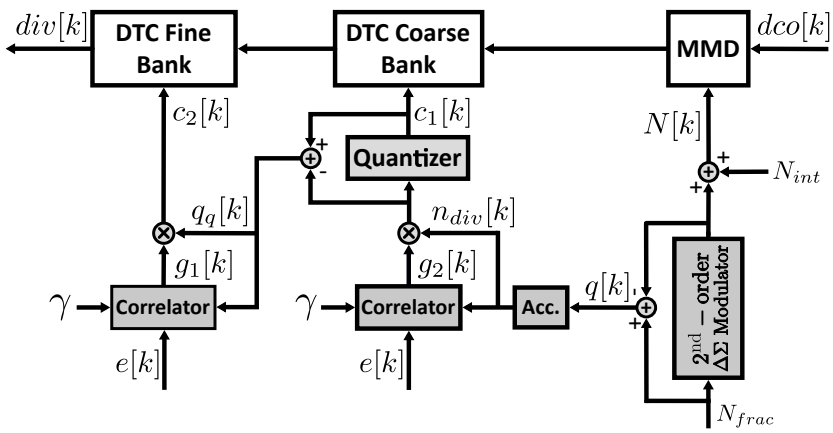


Figure 6.25 Block schematic view of DTC and fractional divider.

tracted from the $\Delta\Sigma$ modulator as $q_{div}[k]$, after which QE is accumulated as $n_{div}[k]$. This signal is correlated with the BBPD output $e[k]$ to generate the estimated gain $g_1[k]$ for coarse tuning; $g_1[k]$ is subsequently multiplied by $n_{div}[k]$ and quantized to generate the coarse tuning word $c_1[k]$. The algorithm is then repeated, extracting $q_q[k]$ from the quantizer and correlating it with $e[k]$, obtaining the estimated gain $g_2[k]$ for fine tuning; finally, $g_2[k]$ is multiplied by $q_q[k]$ to generate the fine tuning word $c_2[k]$ (see Section 3.3.1.1).

The accuracy and speed of the correlation process is controlled via the value of the LMS parameter γ (see Figure 6.25), which is equal to 2^{-10} in this design.

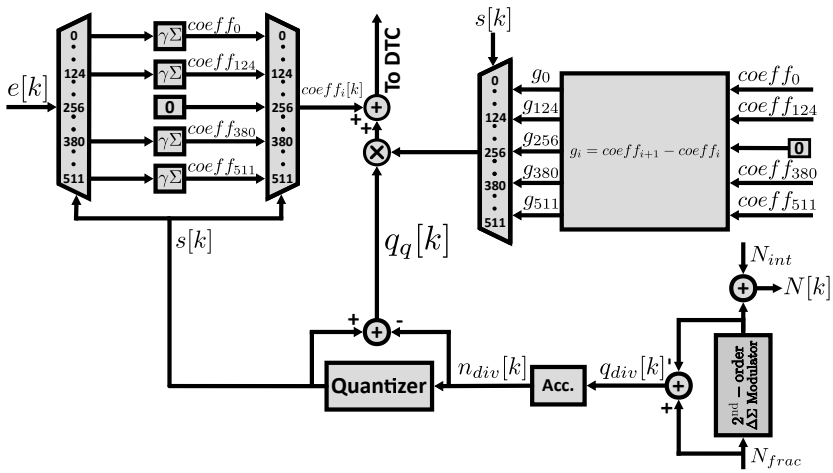


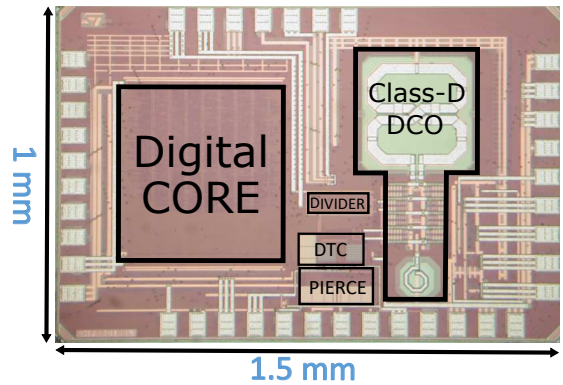
Figure 6.26 Block schematic view of the pre-distorter.

6.3.1.2 DTC LINEARIZATION

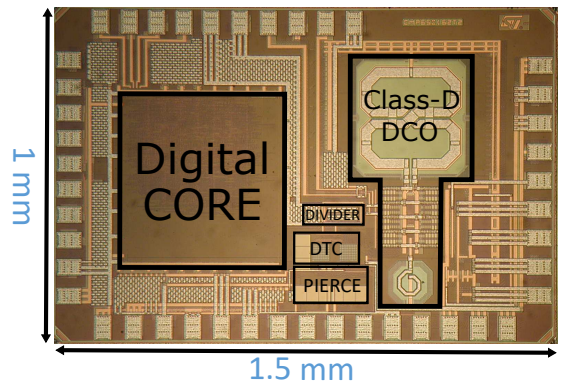
Compared to a TDC with equal resolution, the DTC offers a superior power efficiency. However, even though our DTC is based on a relatively linear *RC*-loaded current-mode inverter, its transfer function still displays a certain amount of non-linearity. DTC linearization, on the other hand, may be conveniently accomplished in the digital domain by means of an adaptive pre-distortion algorithm [4]. The algorithm runs in the background to continuously compensate for any source of non-linearity, including that induced by PVT variations. Specifically, linearization is achieved by measuring the DTC transfer function and subsequently filtering $n_{div}[k]$ with a non-linear block implementing the inverse of the DTC transfer function. In this way, $n_{div}[k]$ is properly pre-distorted before being fed to the control input of the DTC (see Section 3.3.1.2).

Figure 6.26 shows the pre-distorter architecture. In this case, the LMS algorithm does not just generate a simple gain (g_1 in Figure 6.25), but rather a 2^n-point piecewise characteristic, where n is the number of bits in the pre-distorter ($n = 9$ in this design). The algorithm first quantizes $n_{div}[k]$ into $s[k]$, where $s[k]$ enables the s-th path on the left side of Figure 6.26; here, $e[k]$ is accumulated in order to derive the s-th point of the piecewise characteristic of the pre-distorter ($coeff_i$ in Figure 6.26).

The quantization error on n_{div}, i.e. $q_q[k]$, is a small signal that also needs to be filtered by the pre-distorter. This is achieved by amplifying $q_q[k]$ by the discrete derivative of the piecewise characteristic, i.e. $g_i = coeff_{i+1} - coeff_i$ on the right side of Figure 6.26.



(a)



(b)

Figure 6.27 The fabricated two prototypes die photographs.

6.3.2 MEASUREMENT RESULTS

This DPLL has been designed in a 65 nm CMOS process, with an active area of 0.75 mm^2. Two prototypes have been designed. The first one, shown in Figure 6.27(a), did not work properly, as the fine bank was not estimated correctly, and was found to cover less than one LSB of the medium bank, and consequently the DPLL was not able to enter to the final lock.

This issue was solved and a second prototype was fabricated, as shown in Figure 6.27(b). The DPLL has a tuning range between 2.8 GHz and 3.8 GHz. The DPLL consumes 18.2 mW (excluding output buffers) and is powered by different supply domains: a 0.8 V supply for the LDO-DCO, while several distinct 1.2 V supplies power the remaining analog, digital and I/O circuits. The

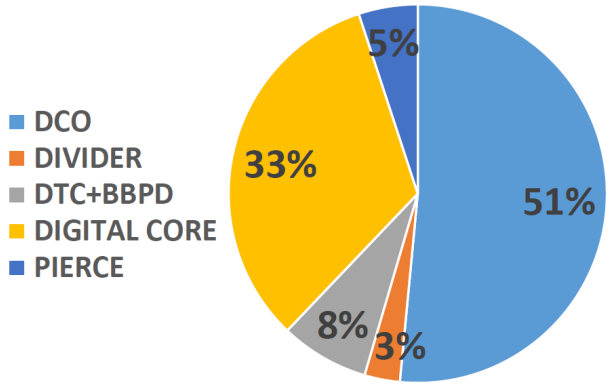


Figure 6.28 Power consumption in the DPLL.

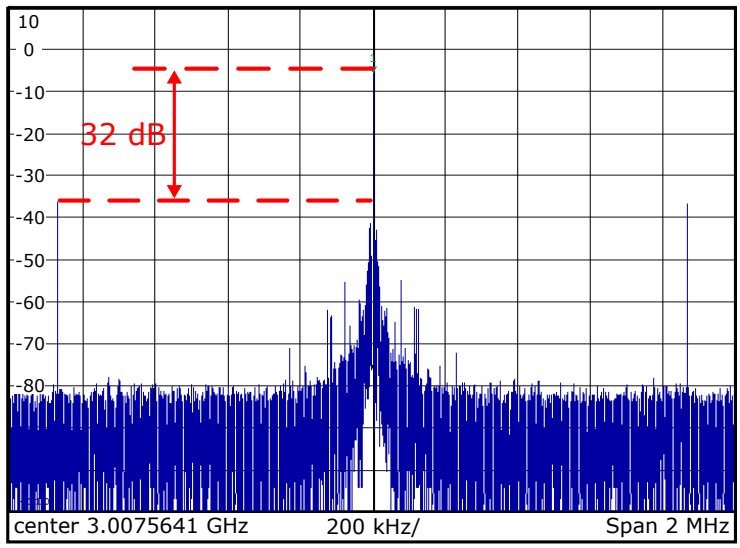


Figure 6.29 DPLL spectrum (2-MHz span) for a 3.0-GHz carrier when spur cancellation is disabled.

power consumption of the main DPLL functions is shown in Figure 6.28.

As shown in Figure 6.29, the measured fractional spur for a 3.0 GHz carrier has a level of about -32 dBc when spur cancellation is disabled. This spur drops to -54 dBc when the same channel is synthesized and spur cancellation is enabled, but DTC pre-distortion is disabled (Figure 6.30). When the DTC pre-distortion is enabled too a very low in-band spur level of -66 dBc is achieved (Figure 6.31). To show the effectiveness of the spur cancellation

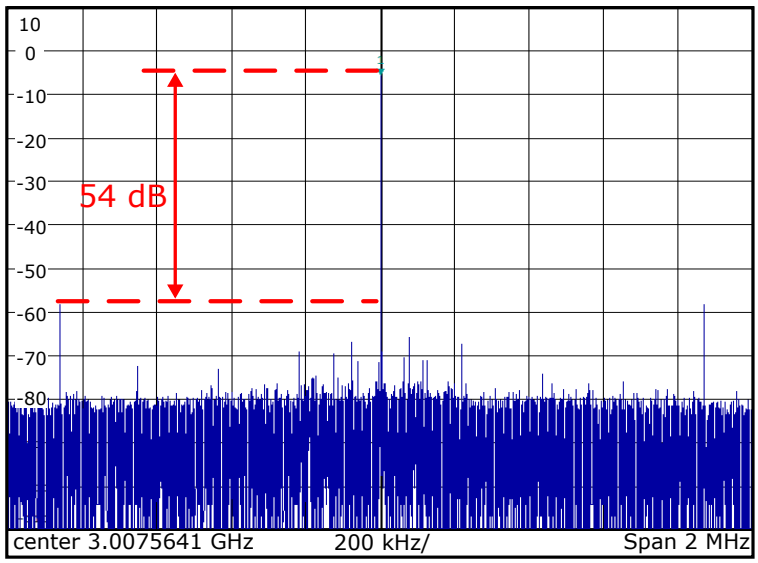


Figure 6.30 DPLL spectrum (2-MHz span) for a 3.0-GHz carrier when DTC pre-distortion is disabled.

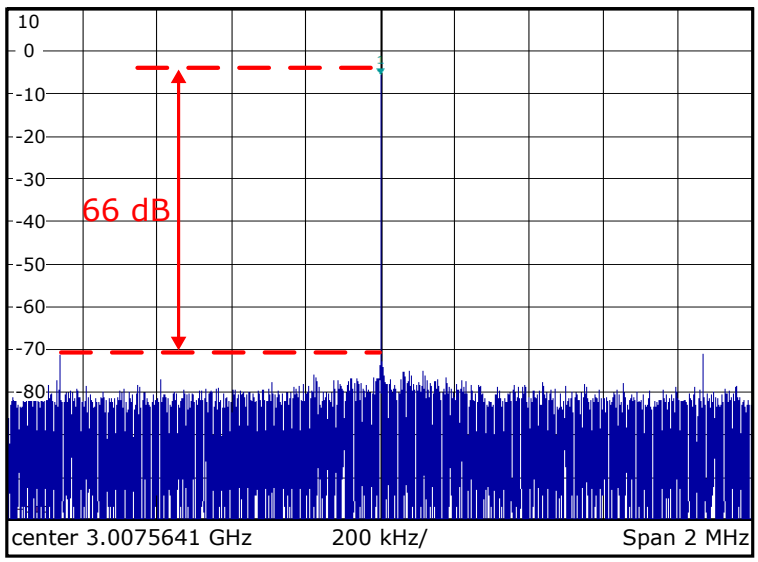


Figure 6.31 DPLL spectrum (2-MHz span) for a 3.0-GHz carrier when nominal operation is enabled.

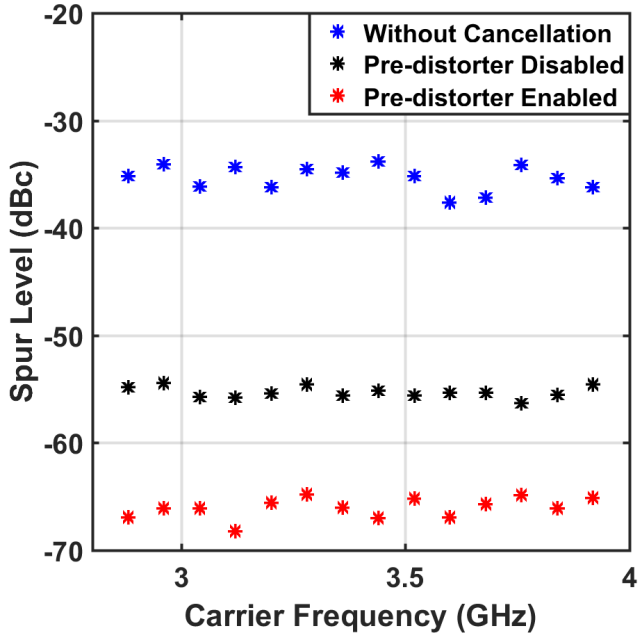


Figure 6.32 In-band fractional spur level across the DPLL tuning range.

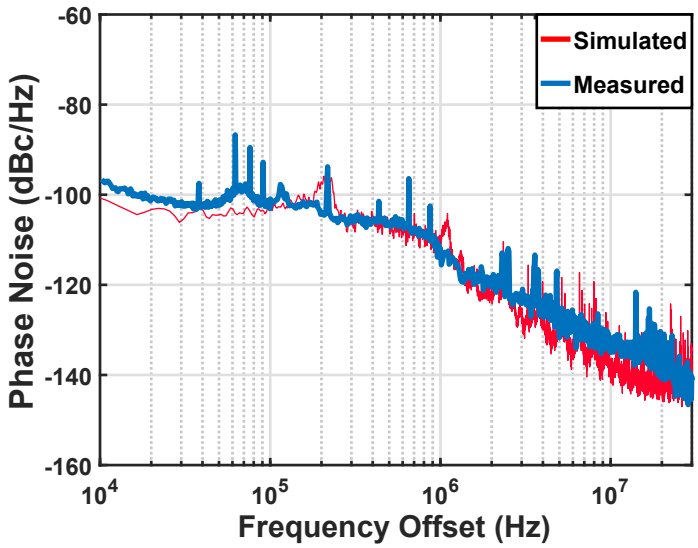


Figure 6.33 Phase noise plot at 3.0 GHz.

Table 6.3 Performance summary and comparison.

Parameter	[43]	[92]	[35]	[91]	[123]	**This work**
Architecture	TDC	TDC	BBPD	TDC	TDC	**BBPD**
f_{ref} (MHz)	50	80	40	50	40	40
f_o (GHz)	3.625	2	3.2	5.36	2.442	**3**
Tuning range (%)	14	38	32	8	22	**31**
Out-Band PN@10MHz (dBc/Hz)	-126	-132	-132	-131	-137	**-134**
In-Band PN@100kHz (dBc/Hz)	-107	-107	-101	-96	-101	**-102**
Bandwidth (MHz)	1	1	0.3	NA	0.2	**1**
Fractional Spur (dBc)	-41	-55	-42	-42	-60	**-66**
Area (mm^2)	0.38	0.56	0.22	0.228	NA	**0.75**
Power (mW)	9.7	9.9	4.5	9.5	1.4	**18.2**
RMS Jitter (ps)	0.39	0.55	0.56	0.7	1.19	**0.497**
FOM (dB)*	-238	-235	-238	-233	-239	**-234**
Process (nm)	65	55	65	65	28	**65**

*$FOM = 10 \times log_{10}[(\frac{\sigma_t}{1sec})^2(\frac{P}{1mW})]$

and DTC linearization techniques, Figure 6.32 reports the in-band spur level across the DPLL tuning range, when 1) spur cancellation is disabled, 2) DTC pre-distortion is disabled, and 3) nominal operation is enabled. While it is expected that disabling spur cancellation should result in huge fractional spurs, the simple LMS algorithm without any DTC linearization is already able to reduce the spur level to well below -50 dBc. Nominal operation, on the other hand, is consistently excellent, with spur levels between -68 dBc and -65 dBc (we acknowledge, however, that frequency division is not functional for very small division ratios, from $1/2^{10}$ to $21/2^{10}$. Thereafter, the DPLL is fully functional, with the performance of Figure 6.32).

Finally, Figure 6.33 shows both simulated and measured phase noise of the DPLL, again for a 3.0 GHz carrier. The phase noise is -102 dBc/Hz at 100 kHz and -134 dBc/Hz at 10 MHz offset frequencies from the carrier. The *rms* jitter, integrated from 10 kHz to 30 MHz, is 497 fs. Table 6.3 highlights the DPLL performance, with a comparison with the state-of-the-art.

7

Conclusions

Frequency synthesis is an important technique in the field of wireless communication. The quality of the produced signal has a great impact on circuit performance and power consumption. A DPLL based frequency synthesizer features a digital intensive implementation and thus has better compatibility with today's nano-scale CMOS technologies as compared to traditional analog intensive designs

In this thesis, the design of DPLL based frequency synthesizers is studied. Efforts have been put on DPLL subblocks level and architecture level in order to achieve high performance results. Consequently, several approaches for performance enhancement have been implemented and verified with prototypes designs, which makes it is possible to achieve high performance DPLL in terms of spurs, phase noise, frequency acquisition, wide TR and power consumption, which are covered in the implemented circuits.

The implemented circuit techniques and architectures are verified , respectively, with three prototype designs. An ultra wide TR VCO has been addressed in the first design. It is implemented in a 28 nm UTBB FD-SOI CMOS process. The VCO makes use of an 8-shaped inductor, since extensive simulations have shown that such a layout is very efficient in improving the robustness of the VCO towards external magnetic fields, while itself generating a much reduced magnetic field. The VCO has a tuning range larger than one octave, while the use of a reconfigurable active core in the VCO allows power saving at the lowest oscillation frequencies, as well as an improved trade-off between power consumption and phase noise at all frequencies. The VCO displays a very good phase noise and FOM performance across its ultra-wide tuning range, and it has very completive active area. In the second design a DPLL based on a 2D GVTDC and a class-D DCO with a $\Delta\Sigma$ quantization noise cancellation based LMS algorithm, has been implemented. The 2D GVTDC is

improving the in-band noise by a first-order noise shaping, while, in the same time, the 2D structure makes the DPLL be able to process large phase errors almost without the influence of latency time. Combined with a high FOM class-D DCO, which achieves the required frequency resolution without any $\Delta\Sigma$ modulator dithering. At the same time, the $\Delta\Sigma$ quantization noise cancellation algorithm allows higher bandwidths without affecting the in-band phase noise performance. In the third prototype, a very low fractional-spurs DPLL is targeted. Consequently, a 65 nm CMOS DTC- and BBPD-based DPLL with a class-D DCO is implemented. This DPLL achieves low phase noise and low fractional-spur levels. The level of in-band fractional spurs is consistently below -65 dBc, demonstrating the effectiveness of the digital algorithms for spur cancellation and DTC linearization. The simplified FAC proposed is wholly digital, requiring no additional analog blocks. Consequently, a fast and reliable frequency acquisition is achieved, despite the limited capture range of the BBPD used.

The techniques covered in this thesis have profitably targeted most of the design challenges.

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