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A High-Frequency Transconductance Method for Characterization of High-κ Border Traps in III-V MOSFETs

Sofia Johansson, Martin Berg, Karl-Magnus Persson and Erik Lind

***Abstract* – A novel method that reveals the spatial distribution of border traps in III-V MOSFETs is presented. The increase in transconductance with frequency is explored in a very wide frequency range (1Hz to 70 GHz) and a distributed *RC* network is used to model the oxide and trap capacitances. An evaluation of vertical InAs nanowire MOSFETs and surface-channel InGaAs MOSFETs with Al_2O_3/HfO_2 high-κ gate dielectric shows a deep border trap density of about 10^{20} $cm^{-3}eV^{-1}$ and a near-interfacial trap density of about 10^{21} $cm^{-3}eV^{-1}$. The latter, cause an almost step-like increase in transconductance at 1-10 GHz. This demonstrates the importance of high frequency characterization of high-κ dielectrics in III-V MOSFETs.**

***Index Terms*—Border traps, high-*k*, transconductance, MOSFET, nanowire, frequency, HfO_2, Al_2O_3, InAs, InGaAs, interface traps**

I. INTRODUCTION

III-V SEMICONDUCTORS, such as InAs and InGaAs, are attractive as channel material in metal-oxide-semiconductor field-effect transistors (MOSFETs) [1, 2] due to their high electron mobilities and injection velocities [3]. The use of atomic layer deposition (ALD) high-κ dielectric in the gate stack has gained a lot of attention as it enables scaling of the equivalent oxide thickness (EOT) below 1 nm, while maintaining low gate leakage currents [4]. It is, however, recognized that large densities of traps in the gate oxide and at the oxide-semiconductor interface may severely degrade the performance of III-V MOSFETs. To facilitate optimized high-κ integration and accurate device modeling, it is not only the interface trap densities, D_{it}, that needs to be characterized, but also the number of border traps, N_{bt}, and their spatial distribution.

The charge pumping method (CP) [5], used for characterizing N_{bt} in Si CMOS, is often not applicable for III-V MOSFETs or nanowire FETs as no body contact is available. Commonly, N_{bt} is instead deduced indirectly by the conductance (*G-V*) or capacitance *(C-V)* [6] methods by measurements on capacitor test structures, which follow a somewhat different processing scheme. Furthermore, it is often only the interface traps that are considered when using these methods. Recently, Sun *et al* reported on a method with frequency dependent transconductance, $g_m(\omega)$, measurements in the 10^1-10^4 Hz frequency range for characterization of very deep border traps [7]. By extending the frequency range of the transconductance measurements to much higher frequencies, *e.g.* 10^{10} Hz, the entire border trap depth profile may be characterized, including the region adjoining the oxide-semiconductor interface. Furthermore, radio frequency (RF) measurements can be used to reveal the intrinsic transconductance, g_{mi}, as no traps respond at sufficiently high frequencies.

This paper reports on a method for characterizing the distribution of border traps in III-V MOSFETs using frequency dependent g_m measurements in the 10^0-$7 \cdot 10^{10}$ Hz frequency range. To deduce the $N_{bt}(x_m)$ depth profile, a transistor model is used where the oxide capacitance, C_{ox}, is replaced by a distributed *RC* network. Measurements are performed in the 10^0-10^5 Hz frequency range by a lock-in amplifier and, in the 10^5-$7 \cdot 10^{10}$ Hz frequency range by network analyzers. Experimental results are reported for two different device geometries: vertical InAs nanowire (NW) wrap-gate MOSFETs and planar InGaAs MOSFETs. In the latter, a high cut-off frequency (f_t = 100 GHz) allows for extension of the characterization method to very high frequencies. A significant increase in g_m is obtained for frequencies above 1 GHz, implying a large number of traps very close to the oxide-semiconductor interface. The model that we propose does not distinguished border traps very close to the semiconductor-oxide interface from interface traps with similar capture cross-section. Hence, one interpretation of these results is that the depth profile includes both border traps and interface traps.

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II. DEVICES UNDER TEST

Fig. 1 schematically depicts the two device geometries evaluated in this work: a surface channel $In_{0.53}Ga_{0.47}As$ MOSFET on an InP substrate and a vertical InAs NW wrap-gate MOSFET on a Si substrate. For the planar device, a 10 nm undoped $In_{0.53}Ga_{0.47}As$ layer was grown by molecular beam epitaxy (MBE) on a p-type ($5\cdot10^{16}$ cm^{-3}) $In_{0.52}Al_{0.48}As$ buffer layer with n-type delta doping of $4\cdot10^{12}$ cm^{-3}. ALD was used for depositing a gate dielectric of 0.5 nm Al_2O_3 and 6.5 nm HfO_2 where Al_2O_3 is deposited at 300°C using TMA and water as precursors, and HfO_2 was deposited at 100°C using TDMA-Hf and water as precursors. Prior to the ALD deposition, the sample was treated with a 21% $(NH_4)S_x$ solution for 20 min at room temperature. Moreover, the device has a gate length of L_g = 200 nm and a gate width of z = 16 µm. Low access resistance was realized by source/drain re-growth and a self-aligned gate-last process. More details on the device fabrication are found elsewhere [8].

In the vertical NW devices, Sn-doped nanowires with 45 nm diameter were grown from Au seed particles by metal-organic vapor phase epitaxy (MOVPE) on a 250–nm-thick InAs layer. From the InAs layer, isolated mesa source contacts were formed by etching. Furthermore, the NW FETs have a 0.5/6.5 nm Al_2O_3/HfO_2 gate dielectric, which was deposited by ALD after nanowire growth using the same precursor as for the surface-channel MOSFETs. Wrap-gates with a gate length of about L_g = 250 nm were formed on arrays of vertical nanowires by back-etching of a sputtered W film and drain contacts were formed at the upper part of the nanowires. The array of nanowires in each device consists of nominally 192 nanowires. A detailed description of the device fabrication may be found elsewhere [9], [10].

The Al_2O_3/HfO_2 gate dielectric used in both devices was chosen as previous studies have shown that a thin Al_2O_3 interface layer gives less interface traps compared to HfO_2 [4]. However, HfO_2 is preferred for the bulk part of the oxide due to its higher permittivity ($\kappa(HfO_2) = 25$, $\kappa(Al_2O_3) = 9$) [11].

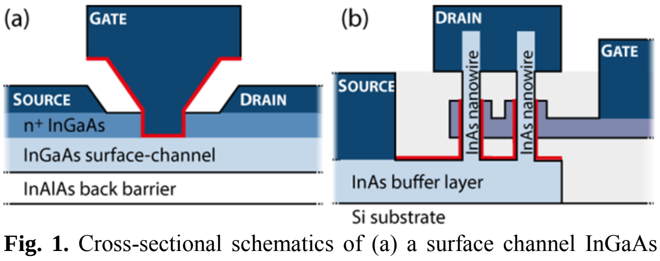

Fig. 1. Cross-sectional schematics of (a) a surface channel InGaAs MOSFET and, (b) a vertical InAs NW MOSFET.

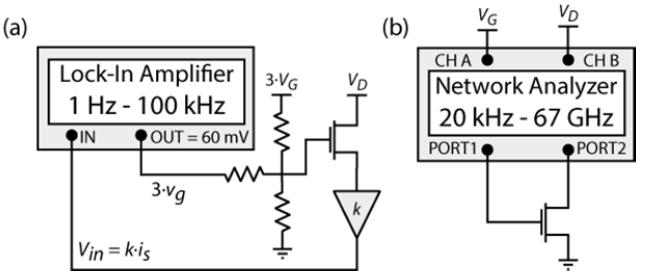

Fig. 2. Schematics of the measurements set-ups used in (a) the low frequency range and, (b) high frequency range.

III. MEASUREMENT SET-UPS

Two different set-ups were used depending on which part of the frequency range that was considered. For low frequencies (1 Hz - 100 kHz), g_m was directly measured as the AC source, i_s, over the AC gate voltage, v_g. The set-up consisted of a lock-in amplifier with a current amplifier at the input and a resistive bias network at the output. The device under test (DUT) was also DC biased as illustrated in Fig. 2a. By connecting the source to the current amplifier, i_s is the input of the lock-in amplifier divided by the multiplication factor of the current amplifier. The resistive network, in Fig. 2a, with three equally large resistances was used for superimposing v_g on a DC gate voltage, V_G. Furthermore, the DUTs were measured by on-chip probing and the DC gate and drain voltages, V_G and V_D, were applied by a Keithley voltage source.

For high frequencies (20 kHz – 60 GHz), g_m was deduced from the admittance (y) parameters (as further described in Sec. IV). For this, scattering (s) parameters were measured by a network analyzer, where V_D and V_G were applied through a bias tee internal to the network analyzer, as illustrated in Fig. 2b. Two different network analyzers were used: an R&S ZVC PNA (20 kHz – 8 GHz) and an Agilent PNA (40 MHz – 67 GHz). The measurements were calibrated off-chip using load-reflect-reflect-match calibration and the impedance of the probing pads was subtracted from the y parameters using dedicated on-chip de-embedding short and open structures. Both DUTs described in Sec. II use 50 Ω co-planar pad layouts.

IV. TRANSISTOR BORDER TRAP MODEL

The spatial distribution of border traps was evaluated from the border trap capacitance, ΔC_{bt}, and the time constant of trapping, $\tau(x)$ [7, 12]. The latter increases exponentially with tunneling depth, x, see (1), and provides the upper frequency limit for which a trap at depth x is able to respond [12].

$$\tau(x) = \tau_0 e^{x/\lambda} \tag{1}$$

Here, x is defined as zero at the semiconductor-oxide interface, see Fig 3a; $\tau_0 = (n\sigma_0 v_{th})^{-1}$ is the trap time constant at the interface, where n is the carrier density at the semiconductor surface, σ_0 is the cross-sectional area of a trap and v_{th} is the thermal velocity; $\lambda = \hbar / \sqrt{8m_{ox}^{*} \cdot \left(E_C^{ox} - E\right)}$ is the attenuation coefficient of the electron wave function where m_{ox}* is the effective mass in the oxide and E_C^{ox} is the conduction band edge in the oxide.

The border trap capacitance, ΔC_{bt}, reflects the amount of border traps in a slice of the oxide with thickness Δx.

$$\Delta C_{bt} = q^2 \cdot N_{bt}(x) \cdot \Delta x\,. \tag{2}$$

Here, $N_{bt}(x)$ is the density of border traps at depth x. In terms of circuit modeling, the incremental capacitance, ΔC_{bt}, may be connected in series with an incremental conductance, ΔG_{bt}, which value is tuned to give the correct time constant $\tau(x)$.

$$\tau(x) = \Delta C_{bt}(x) / \Delta G_{bt}(x)\,. \tag{3}$$

To describe the distribution of traps at different depths in the oxide, the oxide is divided in to incremental steps, ΔC_{ox}, corresponding to slices of the oxide with the width Δx. At each depth an *RC* leg that express $\tau(x)$ at that particular oxide depth [12] is connected, see Fig. 3b.

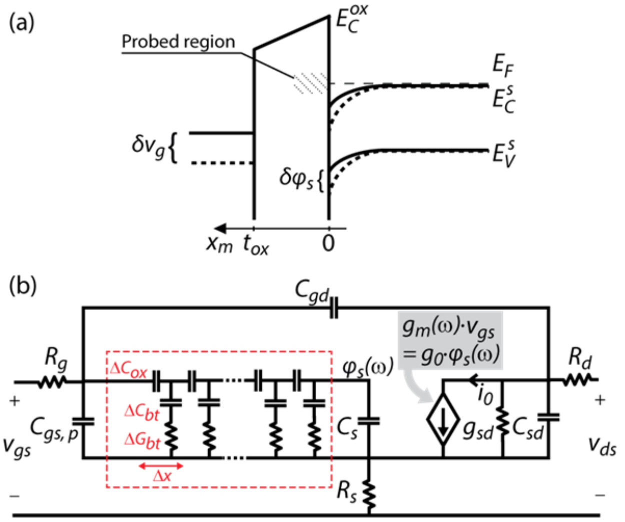

Fig. 3. (a) Illustration of the probed regions induced by an ac gate voltage. (b) A distributed *RC* network representation of the gate dielectric (marked in pink) inserted in a standard FET small signal model. For an FET without traps this *RC* network reduces to C_{ox}. Each leg of the RC network represents a slice of C_{ox} at a certain depth, x_m, with the width Δx and the capacitance ΔC_{ox}.

Using the expressions in (2) and (3), the change in voltage and current caused over one incremental step, Δx, may be expressed in the continuous limit by the following differential equations:

$$\begin{cases} \dfrac{\partial v}{\partial x} = -\dfrac{i(x)}{j\omega\varepsilon_{ox}} \\ \dfrac{\partial i}{\partial x} = -\dfrac{v(x) \cdot j\omega q^2 N_{bt}(x)}{1 + j\omega\tau(x)} \end{cases} \tag{4}$$

The approach for deriving the above equations is the same as for standard transmission line models. The equations were then used to deduce the *y* parameters of the distributed *RC* network. The *y* parameters of the complete transistor small signal model were obtained by inserting the *y* parameters of the distributed *RC* network in a standard FET model as shown in Fig. 3. To extract the various small signal parameters, the source and drain resistances (extracted from DC measurements) were first subtracted from the *y* parameters. Values for gate resistance, R_g, gate-drain capacitance, C_{gd}, and parasitic gate-source capacitance, $C_{gs,p}$ were deduced from the *y* parameters of the DUT, under the assumption that the input conductance is much smaller than 1, and that $\omega^2 \cdot R_g \cdot C_\Sigma^2 << 1$ [13]. Here, $C_\Sigma = C_{gd} + C_{gs,p} + C_{gs}$ is the total input gate capacitance.

According to the small signal model, $g_m(\omega)$ can be deduced from the *y* parameters of the DUT as the real part of y_{21} with a small modification for high frequencies [13],

$$\operatorname{Re}(y_{21}) = \operatorname{Re}(g_m(\omega)) - \omega^2 R_g C_{gd} C_\Sigma\,. \tag{5}$$

The effects of border traps on the transconductance can thus be captured from $\operatorname{Re}(y_{21})$ as long as $\omega^2 \cdot R_g \cdot C_{gd} \cdot C_\Sigma << g_m$ and $\operatorname{Im}(g_m) << \operatorname{Re}(g_m)$. The imaginary part of g_m is due to the phase lag from the distributed *RC* network and was found to be small compared to the real part for all samples and measurement frequencies used in this work.

To find the intrinsic, high-frequency transconductance, g_{mi}, we considered the voltage drop over the oxide, *i.e.* how well δv_{gs} translates into a surface potential, $\delta\varphi_s$, see Fig. 3a. For most frequencies, the relationship between δv_{gs} and $\delta\varphi_s$ is complicated as charge is induced not only in the channel, but also in the traps. This is also the origin of the frequency dependence of the extrinsic transconductance, $g_m(\omega)$. However, for sufficiently high frequencies, no charge traps respond due to the time constant of the trap capturing process. At these frequencies, the distributed *RC* network reduces to the ordinary trap-less C_{ox} and the expression for g_{mi} simplifies to

$$g_{mi} = \left.\frac{\partial i_0}{\partial v_{gs}}\right|_{\omega\to\infty} = v_{inj} \cdot z \cdot C_s \frac{C_{ox}}{C_{ox} + C_s} = g_0 \cdot \frac{C_{ox}}{C_{ox} + C_s}\,. \tag{6}$$

This expression also relates g_0 to $g_m(\omega)$, as shown in Fig. 3b. v_{inj} is the injection velocity, z is the gate width, and C_s is the semiconductor (or quantum) capacitance of the channel.

An analytical expression is deduced for simple calculations of $N_{bt}(x_m)$. Here, it is assumed that for an incremental change in frequency between ω and ω-$\delta\omega$, all traps at a thickness δx around a point x_m charge and discharge during one cycle [7]. Equation (1) gives the following expressions for δx and x_m:

$$\delta x = -\lambda\delta\ln(\omega) \tag{7}$$

$$x_m = \lambda\ln(\omega_0/\omega) \tag{8}$$

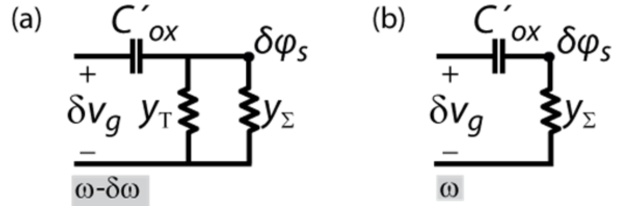

Fig. 4. Admittance models of the oxide at ω-$\delta\omega$ in (a) and at ω in (b).

Admittance models of the oxide at the two frequencies, ω and ω-$\delta\omega$, are shown in Fig. 4. The part of the oxide located beyond x_m can be treated as an ordinary capacitance, $C'_{ox} = C_{ox}/(1 - x_m/t_{ox})$, as no traps respond in this part of the oxide at this frequency. The admittance at a distance x_m into the oxide, within the thickness δx and is given by

$$y_T = \frac{j\omega q^2 N_{bt}(x_m)\delta x}{1 + j\omega\tau(x_m)}. \tag{9}$$

The admittance corresponding to the remainder of the oxide and semiconductor capacitance is described by y_Σ. This admittance also gives a relationship between the frequency dependent transconductance, $g_m(\omega)$ and the intrinsic transconductance, g_{mi}.

$$g_m(\omega) = \frac{j\omega C'_{ox}}{(y_\Sigma + j\omega C'_{ox})} \cdot \frac{C_{ox} + C_s}{C_{ox}} \cdot g_{mi} = \\ = \frac{j\omega C'_{ox}}{(y_\Sigma + j\omega C'_{ox})} \cdot g_0 \tag{10}$$

To account for the derivative of $g_m(\omega)$ in the expression for $N_{bt}(x_m)$, the variation in φ_s at the frequencies ω and ω-$\delta\omega$ is considered. From Fig. 4 we obtain

$$\delta\varphi_s^{\omega} = \frac{j\omega C'_{ox}}{y_\Sigma + j\omega C'_{ox}}\delta v_g \tag{11}$$

$$\delta\varphi_s^{\omega-\delta\omega} = \frac{j\omega C'_{ox}}{y_\Sigma + y_T + j\omega C'_{ox}}\delta v_g \approx \\ j\omega C'_{ox}\delta v_g\left(\frac{1}{j\omega C'_{ox} + y_\Sigma} - \frac{j\omega q^2 N_{bt}\delta x}{(1 + j\omega\tau)(j\omega C'_{ox} + y_\Sigma)^2}\right) \tag{12}$$

In (12) a first order Taylor expansion in δx is assumed. The change is channel potential with frequency is subsequently given by

$$\delta(\delta\varphi_s) = \delta\varphi_s^{\omega-\delta w} - \delta\varphi_s^{\omega}. \tag{13}$$

Using (7), (11)-(13), we obtain

$$\frac{\delta g_m(\omega)}{\delta\ln(\omega)} = \frac{\delta(\delta\varphi_s)g_0}{\delta\ln(\omega)\delta v_g} = \frac{j\omega C'_{ox} j\omega q^2 N_{bt}\lambda g_0 g_m^2(\omega)}{(1 + j\omega\tau)(j\omega C'_{ox})^2 g_0^2}. \tag{14}$$

Solving for $N_{bt}(x_m)$ and taking the real part, we finally obtain the approximate analytical expression

$$N_{bt}(x_m) \approx \frac{(C_s + C_{ox})\cdot g_{mi}}{q^2\lambda\cdot\left(1 - \frac{x_m}{t_{ox}}\right)\cdot g_m^2(\omega)} \cdot \frac{\partial g_m(\omega)}{\partial\ln(\omega)}. \tag{15}$$

Note that, for a III-V quantum well FET, $C_s \approx \frac{q^2 \cdot m*}{\pi\cdot\hbar^2}$ .The analytical expression in (15) is especially suitable for materials, such as InAs, where C_s is comparable to or smaller than C_{ox}. For these materials the variation in surface potential with gate voltage is larger, resulting in larger $\delta g_m(\omega)/\delta ln(\omega)$. Note also that for very deep border traps, the oxide band bending is more pronounced and is likely to be responsible for $\delta g_m(\omega)/\delta ln(\omega)$ rather than $\delta\varphi_s$. Furthermore, equation (15) requires knowledge of g_{mi}, which is found using RF measurements at high enough frequencies where no traps respond.

V. RESULTS AND DISCUSSION

Transfer characteristics for an InGaAs surface-channel MOSFET are shown in Fig. 5. Here, the transconductance is deduced both from DC and RF measurements (20 GHz). The curves have similar shape and show a peak transconductance close to $V_G = 0.1$ V; however, g_m is about 3 times higher at RF.

Also, it should be noted that all measurements on the surface-channel MOSFET presented in this work were conducted about 6 months after device fabrication. During this time the peak DC transconductance has degraded by a factor of three and the threshold voltage has shift more than 0.5 V, indicating creation of excess defects in the oxide. Aging is particularly pronounced for these devices as no passivation is used and the gate oxide is directly exposed to air, which could cause damages such as an increased number of traps in the oxide.

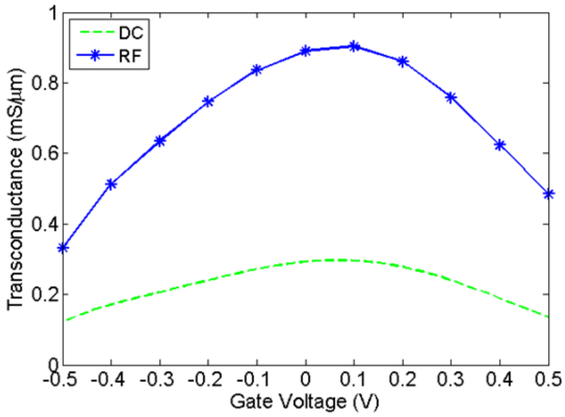

Fig. 5. Transconductance as a function of gate voltage for two different measurements on an InGaAs surface-channel MOSFET is plotted. The green dotted line shows g_m deduced from DC measurements and the blue stared line shows g_m deduced from RF measurements. A drain voltage of V_D = 0.55 V was used. The threshold voltage is V_t = -0.5 V.

Fig. 6 presents the frequency dependence of g_m for the vertical InAs NW MOSFET and InGaAs surface-channel MOSFET measured in the 1Hz - 67 GHz frequency range. For low frequencies (below 100 MHz), g_m increase at a rate of about 0.009 mS/µm per decade and 0.006 mS/µm per decade for the NW device and the surface-channel device respectively, which result in roughly a doubling of g_m from DC up to 100 MHz. These high rates in the two DUTs distinctly indicate high densities of deep border traps in both devices.

In the frequency interval between 1GHz and 10 GHz, a dramatic increase in g_m is seen for the surface-channel device with an increase of roughly 0.30 mS/µm per decade. The largest effect is seen for the bias conditions that gives the highest g_m; still, the same trend was observed for all measured gate voltages (-0.5 V to 0.5 V) and for low drain voltage (V_D = 50 mV). This steep slope in the $g_m(\omega)$ graph implies that the trap profile is dominated by traps very close to the oxide-semiconductor interface. For frequencies above 10 GHz a plateau is observed, which corresponds to an intrinsic transconductance of about g_{mi} = 0.66 mS/µm. Similar transconductance behavior has been observed also in other MOSFETs on the same chip, in MOSFETs on other chips, and using two different network analyzers. For the NW MOSFET, the moderate f_t of a few GHz and the large parasitic capacitances unfortunately veil any similar effects as described in (5). The deduced $g_m(\omega)$ is only valid up to about 1 GHz for the NW device. It should be noted that when calculating $N_{bt}(x_m)$, the intrinsic transconductance is set to g_{mi} = 0.16 mS/µm for the NW device, which is an underestimation if the slope of $g_m(\omega)$ at high frequencies is similar to the surface-channel MOSFET. However, the accuracy is still sufficient to give a good indication of $N_{bt}(x_m)$ also for the NW MOSFET.

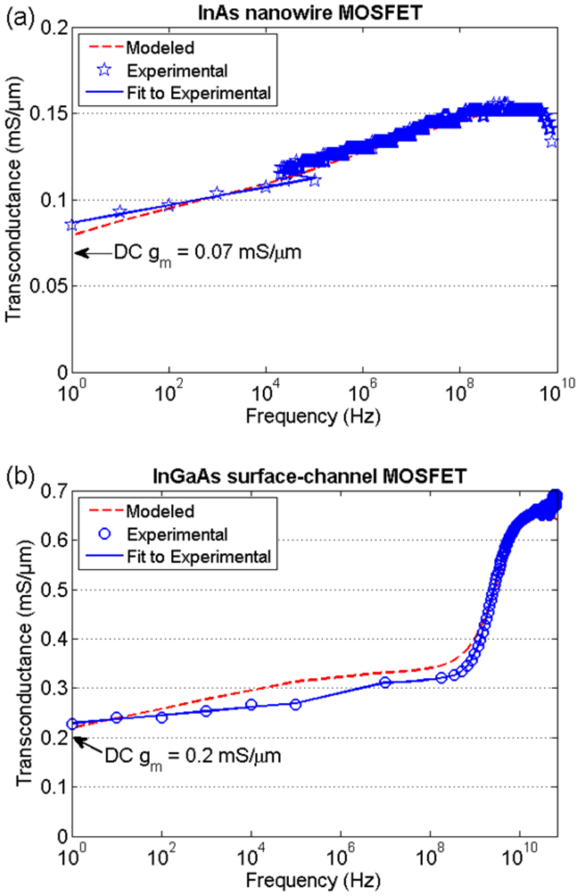

Fig. 6. Transconductance as a function of frequency for (a) a vertical InAs NW MOSFET at DC V_D = 0.55 V and DC V_G = -0.4 V; and, (b) an InGaAs surface-channel MOSFET at DC V_D = 0.55 V and DC V_G = -0.3 V. g_m is here represented by Re(y_{21}) for the de-embedded s parameters in the case of measurements from the network analyzers. The measured g_m is shown by blue stars; a fit to the measured data is shown by a dashed blue line; and g_m of the model using (15) is shown by a solid red line. For comparison, the DC g_m is also shown in the two graphs. The threshold voltage is V_t = -0.5 V for both MOSFETs.

Fig. 7 shows the quantitative border trap depth profiles of the vertical InAs NW MOSFET and the InGaAs surface-channel MOSFET, which are deduced from the measured $g_m(\omega)$ using (15) with $\lambda = 1.1\cdot10^{-8}$ cm. For the InGaAs surface-channel device, N_{bt} is dominated by a large peak situated within a few Å from the oxide-semiconductor interface. The magnitude of the peak provides a large density of near-interfacial traps of $N_{bt}(x_m) = 10^{21}$ cm^{-3}eV^{-1}. It is possible that the interface between the Al_2O_3 and HfO_2 in the gate dielectric, located at about 0.5 nm depth, contributes to the increased $N_{bt}(x_m)$ [14]. And, it could even be argued that this is why a peak is observed. However, preliminary evaluation of MOSFETs with pure HfO_2 gate dielectric have shown similar $g_m(\omega)$ behavior, indicating that the Al_2O_3/HfO_2 interface is not the culprit.

Another possibility is that the peak is partially or fully caused by interface traps. As the capture/emission mechanism suggested for trapping inside the semiconductor conduction band is also associated with a characteristic frequency, $\omega_{0,it}$, and as all traps located at the interface, the $g_m(\omega)$ dependence is expected to show an abrupt increase at $\omega_{0,it}$. This means that Fig. 6b could be interpreted as the $g_m(\omega)$ dependence of the interface traps superimposed on the $g_m(\omega)$ dependence of the border traps. However, it is a delicate issue to judiciously distinguish between different trapping mechanisms. In addition, it may not be possible to describe the interface between InGaAs and Al_2O_3 as atomically abrupt, but instead it is associated with a more complex transition region. Furthermore, the *x*-axis is dependent on τ_0 for which a large variation is found in the reported values [12]. A value of $\tau_0 = 4\cdot10^{-11}$ s was chosen as it corresponds well to the frequency where g_m ceases to increase and gives the smallest error when comparing modeled and measured g_m. It should be noted that, the uncertainty of τ_0 limits the spatial resolution of this method.

A smaller density of *deep* border traps of about $N_{bt}(x_m) = 10^{20}$ cm^{-3}eV^{-1} are observed for both DUTs. The similar values for the two DUTs suggest that the density of deep border traps is not greatly affected by the device geometry or choice of semiconductor. These values are also similar to what has been observed from *C-V* measurements on InGaAs/Al_2O_3 capacitors (N_{bt} ~$4.5\cdot10^{19}$ eV^{-1}cm^{-3}) [12]. Moreover, $N_{bt}(x_m)$ appears to increase somewhat with depth; however, we suggest that this is due to measurement errors.

A projected density of traps of $N_{bt,int} = 5\cdot10^{13}$ cm^{-2}eV^{-1} is calculated for the surface-channel MOSFET by integrating over the measured depths. Fig. 8 shows the total N_{bt} calculated from measurements at different gate voltages. Here, it is observed that the total N_{bt} increases with increasing voltage. In the presented voltage interval, *e.g* $V_G = -0.5$ V to $V_G = 0.5$ V, the Fermi level is understood to be above the conduction band edge as the device is in its on-state. Hence, Fig. 8 shows that the total N_{bt} increases as the Fermi level is moved up in the conduction band, which is consistent with extractions of density of interface traps for InGaAs *C-V* structures [15].

To verify the model, the analytically extracted border trap density is used as input to the full device model in Fig. 3b giving a modeled extrinsic g_m as shown in Fig. 6. The analytically extracted border trap density is thus seen to give a good reproduction of the measured g_m.

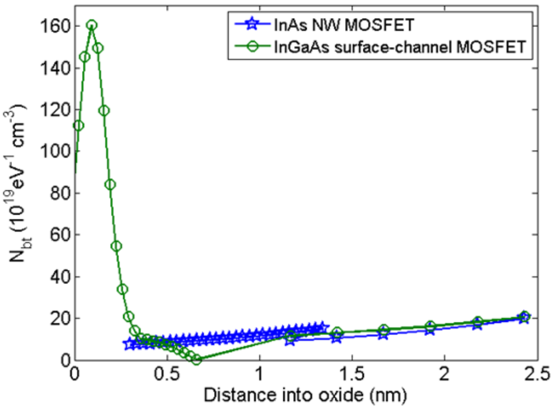

Fig. 7. The number of border traps at different oxide depth deduced from the $g_m(\omega)$ in Fig. 6 for a vertical InAs NW MOSFET (blue curve) and a surface-channel InGaAs MOSFET (green curve).

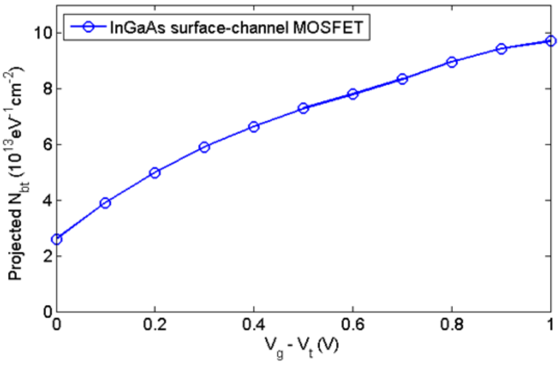

Fig. 8. The voltage dependence of the projected number of border traps is presented. Here, the peak in $N_{bt}(x_m)$ is integrated for frequencies down to 40 MHz, however, the deep border traps are neglected. $V_t = -0.5$ V is substracted from V_G.

VI. Conclusion

We have reported a novel method for characterization of border traps in III-V MOSFETs. The method combines $g_m(\omega)$ measurements with *y* parameter modeling of the oxide and trap capacitances using a distributed *RC* network. From this, an analytical expression is deduced giving the density of border traps as a function of oxide depth. The method was demonstrated for an InGaAs surface-channel MOSFET and a vertical InAs NW MOSFET. For both DUTs, $g_m(\omega)$ steadily increased throughout the 1 Hz -100 MHz frequency range. For the surface-channel MOSFET, a steep increase in $g_m(\omega)$ was observed at about 1-10 GHz. For even higher frequencies a plateau was observed corresponding to the intrinsic transconductance. The method, hence, revealed that the spatial distribution of border traps is dominated by trap states very close to the oxide-semiconductor interface with $N_{bt} = 10^{21}$ cm^{-3}eV^{-1}, whereas the density of deep border traps is about $N_{bt} = 10^{20}$ cm^{-3}eV^{-1}. The high N_{bt} is reasonable when considering the performance degradation of III-V MOSFETs compared to other III-V FETs, such as HEMTs and buried-channel MOSFETs, and it further emphasizes the importance of optimizing the high-κ integration in III-V MOSFETs.

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REFERENCES

[1] M. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M. K. Hudait, J. M. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, W. Rachmady, U. Shah, and R. Chau, "Advanced high-K gate dielectric for high-performance short-channel In$_{0.7}$Ga$_{0.3}$As quantum well field effect transistors on silicon substrate for low power logic applications," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, 2009, pp. 1-4.

[2] Q. Li, X. Zhou, C. W. Tang, and K. M. Lau, "High-Performance Inverted In$_{0.53}$Ga$_{0.47}$As MOSHEMTs on a GaAs Substrate With Regrown Source/Drain by MOCVD," *Electron Device Letters, IEEE,* vol. 33, pp. 1246-1248, 2012.

[3] J. A. del Alamo, "Nanometre-scale electronics with III-V compound semiconductors," *Nature,* vol. 479, pp. 317-323, 2011.

[4] R. Suzuki, N. Taoka, M. Yokoyama, S. Lee, S. H. Kim, T. Hoshii, T. Yasuda, W. Jevasuwan, T. Maeda, O. Ichikawa, N. Fukuhara, M. Hata, M. Takenaka, and S. Takagi, "1-nm-capacitance-equivalent-thickness HfO2/Al2O3/InGaAs metal-oxide-semiconductor structure with low interface trap density and low gate leakage current density," *Applied Physics Letters,* vol. 100, pp. 132906-1-132906-3, Mar 2012.

[5] W. Wang, J. Deng, J. C. M. Hwang, Y. Xuan, Y. Wu, and P. D. Ye, "Charge-pumping characterization of interface traps in Al$_2$O$_3$/In$_{0.75}$Ga$_{0.25}$As metal-oxide-semiconductor field-effect transistors," *Applied Physics Letters,* vol. 96, pp. 072102-1-072102-3, Feb 15 2010.

[6] G. Brammertz, A. Alian, D. H. C. Lin, M. Meuris, M. Caymax, and W. E. Wang, "A Combined Interface and Border Trap Model for High-Mobility Substrate Metal-Oxide-Semiconductor Devices Applied to In$_{0.53}$Ga$_{0.47}$As and InP Capacitors," *IEEE Transactions on Electron Devices,* vol. 58, pp. 3890-3897, Nov 2011.

[7] X. Sun, S. R. Cui, A. Alian, G. Brammertz, C. Merckling, D. Lin, and T. P. Ma, "AC Transconductance Dispersion (ACGD): A Method to Profile Oxide Traps in MOSFETs Without Body Contact," *IEEE Electron Device Letters,* vol. 33, pp. 438-440, Mar 2012.

[8] M. Egard, L. Ohlsson, M. Arlelid, K. M. Persson, B. M. Borg, F. Lenrick, R. Wallenberg, E. Lind, and L. E. Wernersson, "High-Frequency Performance of Self-Aligned Gate-Last Surface Channel In$_{0.53}$Ga$_{0.47}$As MOSFET," *IEEE Electron Device Letters,* vol. 33, pp. 369-371, Mar 2012.

[9] K. M. Persson, M. Berg, J. Wu, S. Johansson, J. Svensson, K. Jansson, E. Lind, and L. E. Wernersson, "Extrinsic and intrinsic performance of vertical InAs nanowire MOSFETs on Si substrates," *Submitted to Electron Device Letters, IEEE,* 2012.

[10] S. Johansson, M. Egard, S. G. Ghalamestani, B. M. Borg, M. Berg, L. E. Wernersson, and E. Lind, "RF Characterization of Vertical InAs Nanowire Wrap-Gate Transistors Integrated on Si Substrates," *IEEE Transactions on Microwave Theory and Techniques,* vol. 59, pp. 2733-2738, Oct 2011.

[11] J. Robertson, "High dielectric constant oxides," *European Physical Journal-Applied Physics,* vol. 28, pp. 265-291, Dec 2004.

[12] Y. Yuan, L. Q. Wang, B. Yu, B. H. Shin, J. Ahn, P. C. McIntyre, P. M. Asbeck, M. J. W. Rodwell, and Y. Taur, "A Distributed Model for Border Traps in Al2O3 - InGaAs MOS Devices," *IEEE Electron Device Letters,* vol. 32, pp. 485-487, Apr 2011.

[13] K. Ickjin, J. Minkyu, L. Kwyro, and S. Hyungcheol, "A simple and analytical parameter-extraction method of a microwave MOSFET," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 50, pp. 1503-1509, 2002.

[14] X. L. Wang, K. Han, W. W. Wang, S. J. Chen, X. L. Ma, D. P. Chen, J. Zhang, J. Du, Y. H. Xiong, and A. P. Huang, "Physical origin of dipole formation at high-k/SiO$_2$ interface in metal-oxide-semiconductor device with high-k/metal gate structure," *Applied Physics Letters,* vol. 96, pp. 152907-1-152907-3, Apr 12 2010.

[15] G. Brammertz, H. C. Lin, M. Caymax, M. Meuris, M. Heyns, and M. Passlack, "On the interface state density at In0.53Ga0.47As/oxide interfaces," *Applied Physics Letters,* vol. 95, pp. 202109-1-202109-3, Nov 16 2009.

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