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Published in:
IEEE Electron Device Letters

DOI:
10.1109/LED.2012.2190132

2012

Link to publication

Citation for published version (APA):
Dey, A., Thelander, C., Lind, E., Dick Thelander, K., Borg, M., Borgström, M., Nilsson, P., & Wernersson, L.-E. (2012). High-Performance InAs Nanowire MOSFETs. *IEEE Electron Device Letters*, *33*(6), 791-793. https://doi.org/10.1109/LED.2012.2190132

Total number of authors:
8

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High-performance InAs Nanowire MOSFETs

Anil W. Dey, Claes Thelander, Erik Lind, Kimberly A. Dick, B. Mattias Borg, Magnus Borgström, Peter Nilsson and Lars-Erik Wernersson

***Abstract*—In this letter we present a 15 nm diameter InAs nanowire MOSFET with excellent on and off characteristics. A *n-i-n* doping profile was used to reduce the source and drain resistances and an Al_2O_3/HfO_2 bi-layer was introduced in the high-κ process. The nanowires exhibit high drive currents, up to 1.25 A/mm, normalized to the nanowire circumference, and current densities up to 34 MA/cm^2 (V_D = 0.5 V). For a nominal L_G = 100 nm we observe an extrinsic transconductance (g_m) of 1.23 S/mm and a subthreshold swing (*SS*) of 93 mV/dec at V_D = 10 mV.**

***Index Terms*—InAs, nanowire, scaling, MOSFET, transconductance (g_m), subthreshold swing (*SS*), on-current (I_{ON}), current density (J_e), high-κ integration, atomic layer deposition (ALD).**

I. Introduction

THE EXCEPTIONAL carrier transport properties of III-V semiconductors combined with advancements in semiconductor fabrication technology have allowed for III-V devices with outstanding properties [1]–[5]. One particularly interesting material system is InAs, which shows great promise for high-performance low-power electronics [2], [3]. To suppress short channel effects, a gate-all-around device geometry, realized around a thin nanowire channel, has been proposed due to the favorable electrostatics. However, at this point it is not clear to what extent scaling of the nanowire diameter will deteriorate the transport properties due to increased surface scattering and quantum confinement effects [6]–[8]. These effects would be particularly adverse in III-Vs due to the low effective masses and the low density of states, factors which need to be compared to the advantage of the high injection velocities of III-Vs [9].

In this work, we present experimental results for a 15 nm diameter InAs MOSFET, demonstrating that high performance InAs nanowire devices may be achieved down to this diameter in spite of surface scattering and quantum confinement effects. We show excellent on and off characteristics, which were achieved by careful nanowire design and the introduction of an Al_2O_3/HfO_2 bi-layer gate dielectric.

II. Process Technology

Nanowires were grown by metal organic vapour phase epitaxy at 420 °C from Au aerosols deposited onto an InAs (111)B wafer [10]. The precursors used were trimethylindium (TMI) and arsine (AsH_3). To form doped source and drain segments (*n-i-n*), tetraethyltin (TESn) and ditertiarybutylselenium (DTBSe) were introduced in the beginning and the end of the growth, respectively. The Se doping gives a very low resistivity in InAs nanowires; however, Se has shown to suffer from a strong memory effect which limits its use to the final stage of the growth process. The doping resulted in hourglass-shaped nanowires, as shown in Fig. 1. This geometry provides a low access resistance in the source and drain segments as well as allowing us to identify the intrinsic segment. The increased diameter in the InAs:Sn and InAs:Se sections is attributed to preferential overgrowth due to the modified surface properties of the doped nanowire segments.

Transmission electron microscopy (TEM) characterization shows that the introduction of the Se precursor gives an abrupt change in the InAs crystal structure from pure wurtzite (WZ) to twinned zinc blende (ZB). Fig. 1d shows a TEM image of such an i-n junction, where it is clearly seen that the diameter increases right at the onset of the change in crystal structure. The effect of the Se precursor to induce such an abrupt change in crystal structure has been reported in [10], where it was also found that the Se-rich ZB segments had resistivities down to 4 x 10^{-3} Ω·cm. The lower n-i junction shows no change in crystal structure and we here speculate that Sn incorporates primarily at the nanowire surface [11], and affects the nanowire surface properties such that Se-rich InAs overgrowth is promoted during epitaxial growth.

Following the growth, the nanowires were transferred onto a pre-patterned Si chip with 100 nm of thermally grown SiO_2. Source and drain electrodes were defined by electron beam lithography (EBL) in polymethyl methacrylate (PMMA), followed by thermal evaporation of Ni/Au. A window for the high-κ dielectric was defined by EBL, followed by an atomic layer deposition (ALD) of 5 cycles (0.5 nm) of Al_2O_3 and 50 cycles (4.5 nm) of HfO_2, both deposited at 100 °C. The thin Al_2O_3 layer improves the InAs/high-κ interface and is more likely to reduce native oxides than pure HfO_2 [12], [13]. Lastly, Ni and Au were used to form a top gate by similar means as for the source and drain electrodes. Fig. 1b shows the schematic of a completed device. The active area of the devices is fully encapsulated within a high-κ film and a top gate metal overlapping both the source and drain electrodes. The devices were not annealed other than during the PMMA baking (180 °C) and ALD (100 °C) stages of the processing.

All measurements were carried out in a vacuum environ-

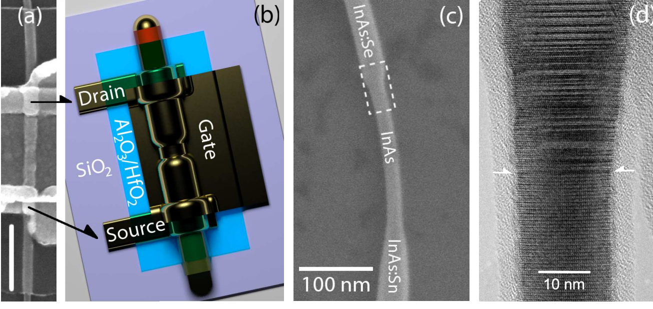

Fig. 1. Top view schematic of a completed device and SEM/TEM micrographs of typical InAs nanowires. (a) SEM image of a completed device. The scalebar is 250 nm. (b) Schematic of an InAs nanowire MOSFET with an overlapping topgate. (c) Scanning electron microscopy (SEM) image of an InAs nanowire with the thin neck region clearly visible, which is the nominally intrinsic segment. The boxed area is studied in greater detail on a similar nanowire in (d). (d) Transmission electron microscopy (TEM) image of an InAs nanowire showing the upper i-n segment (InAs-InAs:Se) of the neck region in detail. The arrows indicate the onset of a twinned zinc blende structure and a diameter increase upon introduction of the Se precursor. The nanowires have an InAs diameter down to 15 nm, with a native oxide thickness of around 1 nm.

ment under dark conditions.

III. Results and Discussion

Fig. 2a shows the electrical output characteristics of a 15 nm diameter (± 2 nm, measured by SEM in the nominally intrinsic segment) InAs nanowire MOSFET. The nominal gate length, L_G = 100 nm, is defined by the length of the intrinsic segment while the source-drain contact separation is 285 nm. The transistors function as n-type MOSFET depletion mode devices with an extracted threshold voltage (V_T) of -0.3 V (Fig. 2b). The negative V_T, extracted by a linear extrapolation from the maximum transconductance, points to some impurity incorporation also in the nominally undoped segment. At V_G = 2 V and V_D = 0.5 V, the nanowires carry 1.25 A/mm of current (normalized to the circumference = $\pi \cdot d_{nw}$) or J_e = 34 MA/cm^2, which is comparable to modern HEMT devices, although HEMTs are operated at a lower gate overdrive [1]. The I_{DS}-V_{DS} characteristics are symmetric when interchanging the source/drain bias, indicating that the two contacts have similar resistance. The maximum voltage gain g_m/g_0 = 50, which highlights the importance of the device geometry. The good output conductance characteristic is a result of the hourglass shape of the device which reduces the series resistances due to the selective overgrowth of the InAs:Sn and InAs:Se n^+ regions. The stacking defects seen in Fig. 1d could be a problem; however, since we measure a low R_{ON} = 5.3 kΩ, we believe that the stacking defects are not a major issue in the device. The on-resistance corresponds to 0.26 Ω·mm, which is again comparable to modern HEMTs, where R_{ON} = 0.5 Ω·mm [1]. In order to estimate the source and drain resistances, the experimental data was compared to simulated data of a 15 nm InAs nanowire MOSFET with 5 nm of HfO$_2$ operating at the ballistic limit [6]. To fit the low bias data from the ballistic model to our experimental data, we added R_S = R_D = 1.6 kΩ to the model (the dotted traces in Fig. 2a), giving a rough estimate of the extrinsic source and drain resistances.

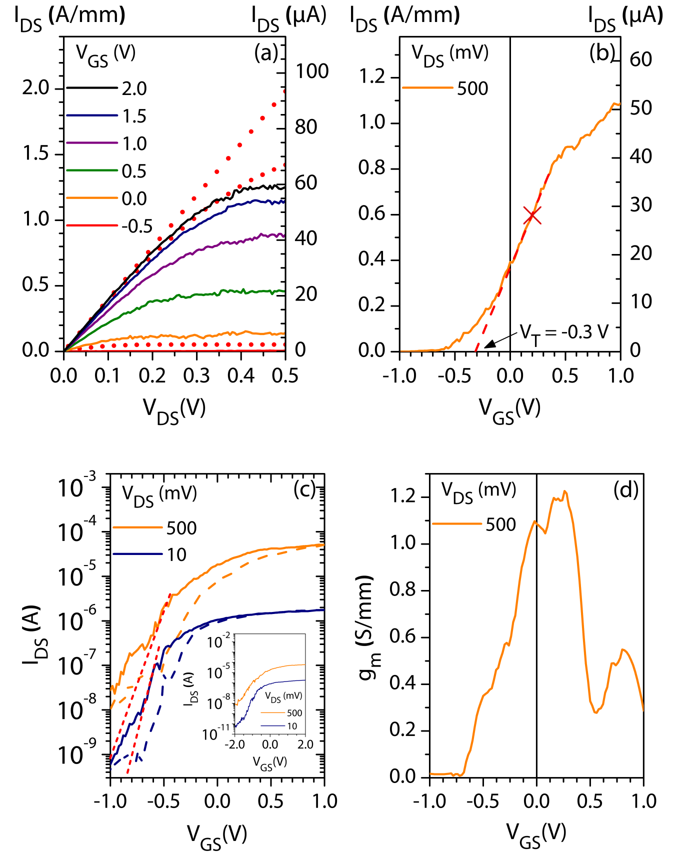

Fig. 2. Electrical data for a 15 nm diameter InAs nanowire MOSFET with L_G = 100 nm (the data in (a) and (d) is normalized to the nanowire circumference). (a) Output characteristics for a measured device. The dotted traces are simulated data for a 15 nm InAs nanowire MOSFET with 5 nm of HfO$_2$ operating in the ballistic limit ($V_{G,max}$ = 1 V and ΔV_G = 0.5 V). (b) The nanowire MOSFET shows n-type depletion mode operation with a threshold voltage of -0.3 V. The cross indicates V_{OV} = V_{DS} = 0.5 V. (c) Logarithmic plot of the current at different drain bias conditions. The solid line is the trace from low to high gate voltage and the dashed trace is from high to low. The inset shows the characteristics for a wider gate sweep, from -2 V to 2 V (d) Transconductance for a device at V_D = 0.5 V. $g_{m,max}$ = 1.23 S/mm.

We extract a maximum normalized transconductance g_m = 1.23 S/mm for V_D = 0.5 V (Fig. 2d). Comparing this to previous work on InAs nanowire MOSFETs, we note an improvement by a factor of 2 to 10 [2], [3], [14]. We attribute this improvement in extrinsic transconductance to the reduced series resistance, the use of a bi-layer high-κ process, as well as to the further scaling of the gate oxide thickness. Using the estimated source and drain resistance, we determined the intrinsic transconductance to be g_{mi} = 1.3 S/mm [15].

Using a non-parabolic model, the flatband gate capacitance of a 15 nm InAs nanowire with 5 nm of HfO$_2$ was calculated, C_g = 8.7 x 10^{-3} F/m^2 [16]. This was used to estimate the extrinsic peak field-effect mobility in the linear region of the device (V_D = 10 mV), L_G = 100 nm, which was found to be μ_e = 1510 cm^2/V·s. The lower values presented here compared to previous reports on similar devices [7], [8], [17], could be explained by the extraction method. A non-parabolic model for a gate-all-around device was utilized as compared to a charge

TABLE I
DATA TABLE FOR A LIST OF DEVICES (*THIS WORK) WITH VARYING DIMENSIONS (D, DIAMETER/THICKNESS) AND GATE LENGTHS (L_G). THE VALUES FOR I_{ON} AND g_m OF NANOWIRE DEVICES ARE NORMALIZED TO THE CIRCUMFERENCE. THE VALUES ARE GIVEN FOR V_{DS} = 0.5 V AND I_{ON} IS PRESENTED FOR V_{OV} = 0.5 V (OR THE NEAREST VALUE).

D (nm)	L_G (nm)	I_{ON} (A/mm)	$g_{m,max}$ (S/mm)	SS (mV/dec)	Ref.	Tech.
15	100	0.6	1.23	140	*	NW
10	30	0.7	1.9	80	[1]	HEMT
30	250	0.12	0.56	120	[4]	FinFET
10	75	0.55	1.75	95	[5]	QWFET
25	170	0.4	0.8	260	[17]	radial NW
13	230	0.9	1.72	180	[19]	XOI

control model or a 2D self-consistent Poisson/Schrödinger solver [7], [17]. A non-parabolic model gives a larger gate capacitance, mainly in accumulation but also slightly higher at flat band conditions, which in turn gives a lower mobility value. Moreover, the device could be quasi-ballistic, which would also yield an underestimation of the mobility [18].

From Fig. 2c we calculated the inverse subthreshold slope *SS* = 140 mV/decade at V_D = 0.5 V and 93 mV/decade at V_D = 10 mV (the dashed red lines). In addition, sweeping the gate from -1 V to 1 V shows little hysteresis in comparison to devices with only HfO_2. The I_{ON}/I_{OFF} ratio, for V_G = -1 V to 1V, was 2 x 10^3 at V_D = 0.5 V (for V_G = -2 V to 2 V, I_{ON}/I_{OFF} = 10^4, where the minimum current $I_{OFF,min}$ = 6 nA). The drain induced barrier lowering (DIBL) was calculated between V_D = 0.25 V and 0.50 V to be 60 mV/V.

Device metrics for a range of competing technologies are included in Table 1. The device presented in this paper is comparable in performance to modern high performance devices in other technologies.

IV. CONCLUSIONS

We present experimental data for 15 nm diameter InAs nanowire MOSFET with I_{ON} = 1.25 A/mm (J_{ON} = 34 MA/cm^2) and an extrinsic transconductance g_m = 1.23 S/mm, normalized to the circumference. We believe that the excellent on-performance is a result of the combination of an optimized device structure and the introduction of an Al_2O_3/HfO_2 bilayer in the high-κ process. We observe a very low on-resistance of 0.26 Ω·mm and also a subthreshold swing of 140 mV/decade at V_D = 0.5 V (93 mV/decade at V_D = 10 mV). The data also shows an I_{ON}/I_{OFF} ratio of 10^4 and a DIBL of 60 mV/V. Our results show that the scaling of nanowire devices does not necessarily have to be limited by surface scattering and quantum confinement effects down to 15 nm diameter.

ACKNOWLEDGEMENTS

The authors would like to thank colleagues within the Department of Electrical and Information Technology and the Department of Solid State Physics at Lund University for support and rewarding discussions. This work was supported by the Swedish Foundation for Strategic Research (SSF), the Swedish Research Council (VR), VINNOVA, the Nanometer Structure Consortium and Lund University (nmC@LU) and the Knut and Alice Wallenberg Foundation.

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