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# Low-Frequency Noise in III-V Nanowire TFETs and MOSFETs

Markus Hellenbrand, Elvedin Memišević, Martin Berg, Olli-Pekka Kilpi, Johannes Svensson, and Lars-Erik Wernersson

**Abstract**—We present a detailed analysis of low-frequency noise (LFN) measurements in vertical III-V nanowire tunnel field-effect transistors (TFETs), which helps to understand the limiting factors of TFET operation. A comparison with LFN in vertical metal-oxide semiconductor field-effect transistors with the same channel material and gate oxide shows that the LFN in these TFETs is dominated by the gate oxide properties, which allowed us to optimize the TFET tunnel junction without deteriorating the noise performance. By carefully selecting the TFET heterostructure materials, we reduced the inverse subthreshold slope well below 60 mV/decade for a constant LFN level.

**Index Terms**—Vertical Nanowires, III-V, MOSFET, TFET, Low-Frequency Noise

## I. INTRODUCTION

LOW-frequency noise (LFN) is known to have a detrimental effect on both transistor and circuit performance [1]. At the same time, however, LFN can be used to gain insight into the material and transport properties of transistors and may be regarded as a technology quality metric. From a comparison of vertical nanowire metal-oxide semiconductor field-effect transistors (MOSFETs) with vertical nanowire tunnel field-effect transistors (TFETs) of a similar structure and the same channel material and gate oxide, we can deduce that the LFN properties in both device types are dominated by the gate oxide. This is further supported by comparison of TFETs with different tunnel junctions. LFN in TFETs was studied experimentally before in Si-based devices [2], [3], but knowledge about full III-V implementations is still limited [4]. Here, we use InAs MOSFETs as reference for the LFN analysis and show how the same LFN model can be applied to TFETs, even when the inverse subthreshold slope  $S$  is reduced below 60 mV/decade. This model and the experimental study of LFN in TFETs will help to better understand the limiting factors of TFET operation.

## II. DEVICE STRUCTURES AND DC CHARACTERIZATION

The processing and final device structure (Fig. 1) for the studied MOSFETs and TFETs are very similar, and especially the resulting gate stack is the same. All nanowires were grown by metalorganic vapor phase epitaxy, using Au seed particles electron-beam-lithography-defined on a highly

n-doped InAs buffer layer integrated on Si. For MOSFETs, the nanowires consisted of a 200-nm-long not intentionally doped InAs bottom segment, followed by a 400-nm-long highly n-doped top segment, the growth of which also resulted in a highly doped shell overgrown around the bottom segment. The TFET nanowires consisted of a highly n-doped InAs bottom segment and a not intentionally doped InAs channel segment, followed by a highly p-doped segment to form the tunnel junction. In the first generation, the junction was realized by switching to GaSb ( $S > 60$  mV/decade) and in the second generation to  $\text{In}_{0.1}\text{Ga}_{0.9}\text{As}_{0.88}\text{Sb}_{0.12}$ , which resulted in  $S$  below 60 mV/decade. To maintain good top contacts, the InGaAsSb segment was followed by an additional GaSb segment and for the MOSFETs, a W/TiN top contact was applied immediately after growth. For all devices, the InAs channel region was digitally etched to reach final diameters of 28 nm for MOSFETs and 20 nm for TFETs. After etching, identical high- $\kappa$  gate oxides (1 nm/4 nm  $\text{Al}_2\text{O}_3/\text{HfO}_2$  atomic layer deposition, effective oxide thickness  $\approx 1.4$  nm) and sputtered W metal gates were applied for all devices. Source, gate, and drain were separated by spacers, details on the processing schemes can be found in [5] for MOSFETs, and in [6] (GaSb) and [7] (InGaAsSb) for TFETs. Fig. 1(c) compares representative transfer characteristics of a MOSFET with both types of TFETs, where these TFET examples exhibit values of  $S = 72$  mV/decade (GaSb) and  $S = 52$  mV/decade (InGaAsSb). Other InGaAsSb devices on the same sample reached values of  $S$  below 50 mV/decade.

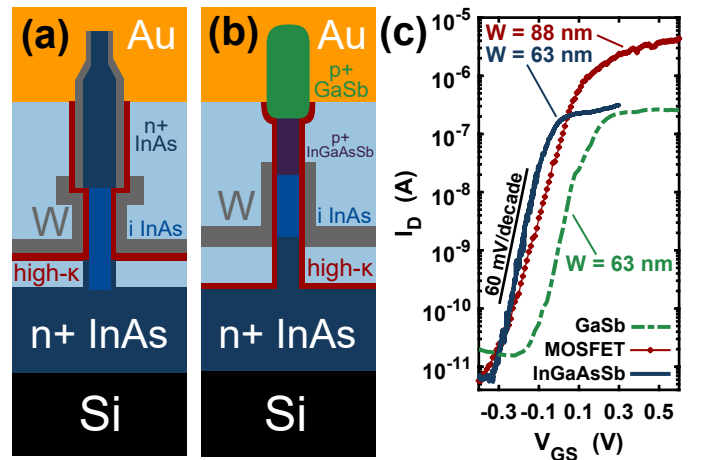


Fig. 1. (a) Schematic illustration of a MOSFET. (b) Schematic illustration of an InGaAsSb TFET. The GaSb structure looks the same, only without the InGaAsSb segment. (c) Transfer characteristics of a MOSFET and both types of TFET at room temperature with  $V_{DS} = 50$  mV. All transistors consisted of a single nanowire.  $W$  in (c) corresponds to the gate width, which for gate all-around transistors is the circumference of the nanowire.

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### III. MEASUREMENT AND ANALYSIS

Each measurement consisted of a logarithmic frequency sweep between 10 Hz and 1 kHz and a more detailed measurement at 10 Hz, and all measurements were carried out for gate voltages  $V_{GS}$  covering the whole range from the off- to the on-state. A lock-in amplifier measured the current noise power spectral density (PSD) of the transistor current for a constant source-drain bias  $V_{DS} = 50$  mV, which was supplied by a low-noise current preamplifier that was used to increase the measurement sensitivity. Fig. 2(a) and (b) show measurements of the noise current PSD representative for InAs MOSFETs, Fig. 2(c) and (d) show the same measurements for InGaAsSb TFETs, and the GaSb TFET measurements showed the same behavior as well. With the exception of the noise for the lowest currents in Fig. 2(d), the complete noise behavior of these devices can be described by the so-called McWhorter model [8]. According to this model, electrons tunneling into and out of gate oxide defects cause fluctuations in the channel potential energy, which appears in the drain current as noise. This noise origin is commonly referred to as number fluctuations. For a long channel MOSFET, starting from the PSD of a single gate oxide defect and integrating over a spatial and energetic defect distribution  $N_{bt}$  [9] results in the expression

$$\frac{S_{I_D}}{I_S^2} = \frac{q^2 k T \lambda N_{bt}}{f \gamma L_G W_G C_{ox}^2} \frac{g_m^2}{I_S^2} = S_{V_{fb}} \frac{g_m^2}{I_S^2}, \quad (1)$$

where  $I_S$  is the source current,  $q$  the elemental charge,  $k$  the Boltzmann constant,  $T$  the temperature,  $\lambda = 0.13$  nm the tunneling attenuation length according to the Wentzel-Kramers-Brillouin approximation,  $f$  the frequency,  $L_G$  and  $W_G$  the effective gate length and width, respectively,  $C_{ox} = 0.033$  F/m<sup>2</sup> is the gate area normalized gate oxide capacitance calculated as a cylindrical capacitor, and  $g_m$  the transconductance.  $S_{V_{fb}}$ , summarizing everything except for the transconductance, is called the flatband voltage noise PSD and was a fitting parameter in Fig. 2, whereas measured values were used for  $I_S$  and  $g_m$ . The frequency exponent  $\gamma$  empirically takes into account spatial nonuniformities in the defect density, where  $\gamma = 1$  corresponds to a spatially uniform defect distribution.

Although the derivation of (1) in [9] was carried out for long channel MOSFETs, it holds for TFETs just as well. With the expression

$$I_{1D} = a (V_R - V_{th}) \exp(-b/\xi) \quad (2)$$

from [10] for an ideal 1D TFET, electrons tunneling into and out of gate oxide defects will change both  $V_R$ , the reverse bias applied to the tunnel junction by the gate, and, since it depends on  $V_R$ , also  $\xi$ , the electric field across the junction. In (2),  $a$  and  $b$  summarize constants and material parameters, and  $V_{th}$  is  $\ln(4)$  times the thermal voltage  $kT/q$ .  $V_R$  is related to the gate bias  $V_{GS}$  as  $V_R = V_{GS} C_{ox} / (C_{ox} + C_q + C_{it})$  with the gate, the semiconductor, and the interface state capacitances  $C_{ox}$ ,  $C_q$ , and  $C_{it}$ , respectively. Since all TFETs featured gate lengths of at least 260 nm,  $V_{DS}$ , in first order approximation, does not affect  $V_R$  anywhere close to the junction. The resulting fluctuation  $I_N$  in the current at each frequency (so that  $I_N = \sqrt{S_{I_D}}$ ) due to a charge fluctuation  $\partial q_{ox}$  in the oxide can be calculated in a straightforward manner as

$$I_N = \frac{\partial I_{1D}}{\partial q_{ox}} \Delta q_{ox} = \frac{\partial I_{1D}}{\partial V_R} \frac{\partial V_R}{\partial q_{ox}} \Delta q_{ox} = g_m \frac{\partial V_R}{\partial q_{ox}} \Delta q_{ox}, \quad (3)$$

which also holds for a 3D expression of (2). Since the noise both in MOSFETs and in TFETs is caused by the same local flatband fluctuations due to charges in the oxide, it is justified to identify  $(\Delta q_{ox} \partial V_R / \partial q_{ox})^2$  in (3) with  $S_{V_{fb}}$  in (1), so that the same noise analysis can be applied both for MOSFETs and for TFETs. And indeed, the proportionalities in (1) fit very well with the results of both InGaAsSb TFETs (Fig. 2(d)) and GaSb TFETs (not shown). Furthermore, the application of the same model is supported by the unnormalized noise in Fig. 3(a), since all measurements follow the same trend. For some MOSFETs, as e.g. in Fig. 2(b), measurement and model do not agree as well, which we attribute to so-called correlated mobility fluctuations. This additional contribution in the intermediate current region results from increased Coulomb scattering from electrons trapped in gate oxide defects and can be modelled by including a factor  $(1 + \beta \mu_{eff} C_{ox} I_S / g_m)^2$  in the right side terms of (1) [9]. Here, the scattering parameter  $\beta$  and the effective channel mobility  $\mu_{eff}$  together were a fitting parameter, determined

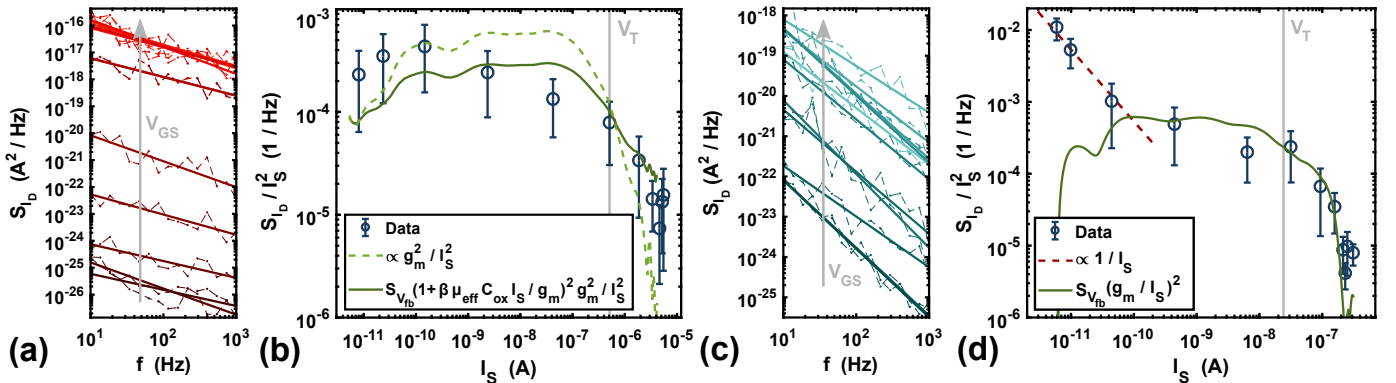


Fig. 2. Representative noise measurements. (a) Frequency sweep for a MOSFET. (b) MOSFET measurement at 10 Hz. The lines indicate that the noise is dominated not only by number fluctuations (broken line), but by both number and correlated mobility fluctuations (solid line). (c) and (d) Same graphs as (a) and (b), but for TFETs. (d) Number fluctuations are dominant over a large current range (solid line). In the off-state, however, mobility fluctuations of electrons injected into the channel by defect-assisted tunneling, take over (broken line). The error bars in (b) and (d) show the standard deviation of the measurement.

by applying a linear fit to  $\sqrt{(S_{ID}/g_m^2)}$  plotted versus  $I_S/g_m$ , which also determined  $S_{V_{fb}}$  for this model. For Fig. 2(b), assuming  $\mu_{eff} \approx 1300 \text{ cm}^2/\text{Vs}$  for a nanowire InAs channel [11], this fit resulted in  $\beta \approx 2700 \text{ Vs/C}$ , which is reasonably close to values typically found for  $\beta$  [9].

The assumption of elastic tunneling as an important part of the capture and release mechanism was confirmed by carrying out LFN measurements at low temperatures (11 K, not shown), where the results were the same as in Fig. 2, except for a difference in magnitude, which directly corresponds to the explicit temperature dependence in the middle expression of (1). This reveals that the capture and release mechanism is not dominated by any activation energy.

Besides the largely dominant number fluctuations in Fig. 2(b) and (d), a second noise contribution shows up for very small currents as indicated in Fig. 2(d). In the subthreshold region, these so-called mobility fluctuations [9] can be empirically described as

$$\frac{S_{ID}}{I_S^2} = \frac{\alpha_H \mu_{eff} 2kT}{f L_G^2 I_S}, \quad (4)$$

where  $\alpha_H$  is the so-called Hooge parameter, and the other parameters are as defined before. The line in Fig. 3(a) proportional to  $I_S$  (cp. (4)) further supports that mobility fluctuations are only relevant for a few devices and for low currents. This separation of mobility and number fluctuations was observed before in nanowire MOSFETs and depends on a surface or core conduction path in the respective operation regime [11]. In the case of the TFETs here, it is known that the off-state was affected by thermionic emission through defect-assisted tunneling [6], [7]. Since the TFET off-current after the junction is governed by drift-diffusion, mobility fluctuations can occur in the TFET off-current as well. With the  $1/I_S$  fit in Fig. 2(d) and  $\mu_{eff} = 1300 \text{ cm}^2/\text{Vs}$  for an InAs channel as before [11], the Hooge parameter can be calculated as  $\alpha_H = 3.5 \times 10^{-5}$ , which is in very good agreement with [11]. It appears that the region right after the threshold voltage in Fig. 2(b) and (d) and up to saturation of the curves, which probably results from series resistance noise becoming dominant, could be described by (4) as well. However, for MOSFETs, mobility fluctuations

are already taken into account as a correlated effect, and for the measured TFETs, the tunneling process of electrons from the source into the channel is not subject to the mobility. Since number fluctuations in contrast directly affect the tunneling window, they dominate the overall noise behavior.

The slopes in Fig. 2(a) and (c) (and thus  $\gamma$  in (1)) differ between MOSFETs and TFETs and  $\gamma$  was generally slightly lower than one for MOSFETs and slightly higher for TFETs. This small variation around  $\gamma \approx 1$  is – besides measurement uncertainties – most likely a cause of processing variations, leading to slightly different defect distributions around the probed depths. For some TFET measurements, however,  $\gamma$  even approaches values of two, which indicates that in those particular devices, there were only very few active defects. As was shown for example in [2] and [12], the LFN behavior in TFETs is dominated by the 10-20 nm of the gate/channel closest to the junction, which explains how only very few defects contribute to the LFN characteristics. In fact, in many of the TFETs studied here, for certain bias conditions we were able to measure Random Telegraph Signal (RTS) noise [7], which is caused by only one individual defect, and agrees well with the observation of  $\gamma$  approaching values of two. The small gate area affecting LFN in TFETs also explains why the levels of the gate area normalized equivalent input gate voltage noise PSD  $S_{V_{fb}} \times L_G \times W_G$  for MOSFETs and TFETs in Fig. 3(b) are comparable. While, due to its exponential dependence on the applied bias, the tunnel junction in TFETs is much more sensitive to fluctuations in the energy bands than the thermionic barrier in MOSFETs, the gate area inducing LFN in TFETs is much smaller. This leads to comparable LFN levels. Besides the border trap density  $N_{bt}$ ,  $S_{V_{fb}} \times L_G \times W_G$  only includes constants (cp. (1)), which allows for directly calculating  $N_{bt}$  and thus evaluating the gate oxide quality. For all measured devices the minimum  $N_{bt}$  is in the order of  $2 \times 10^{20} \text{ cm}^{-3} \text{ eV}^{-1}$ , which is consistent with all devices having the same InAs channel and the same gate stack. For the TFETs, this is actually a conservative estimate, since the value was calculated with the whole physical gate length instead of the probably critical 10-20 nm closest to the junction, so that the actual value for  $N_{bt}$  in TFETs could be lower by up to a factor of ten.

#### IV. CONCLUSION

We analyzed in detail the LFN behavior in vertical III-V nanowire MOSFETs and TFETs and showed that the same noise formalism is applicable to both types of devices despite their different transport mechanisms. From this, we conclude that the gate oxide is the dominant source of LFN in our devices, which is reflected in a constant LFN level even in the case of a significant improvement of the TFET inverse subthreshold slope due to the optimization of the heterojunction.

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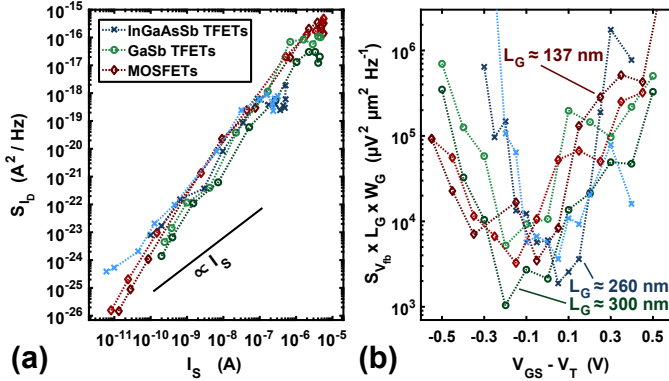


Fig. 3. (a) Measurements at 10 Hz like the ones in Fig. 2(b) and (d), but without  $I_S$  normalization. Each curve represents one device, using the same measurement conditions for all.  $S_{ID}$  not being proportional to  $I_S$  (cp. (4)) supports Fig. 2 in that it is not mobility fluctuations that are dominant. (b) Equivalent input noise, same transistors and same colors as in Fig. 3(a). Despite the improved subthreshold slope, the InGaAsSb TFETs do not exhibit higher equivalent input noise than the GaSb TFETs or even the MOSFETs.

## REFERENCES

- [1] S. Datta, H. Liu, and V. Narayanan, "Tunnel FET technology: A reliability perspective," *Microelectronics Reliability*, vol. 54, no. 5, pp. 861–874, May 2014, DOI: <http://dx.doi.org/10.1016/j.microrel.2014.02.002>.
- [2] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "Low-frequency noise behavior of tunneling field effect transistors," *Applied Physics A*, vol. 97, no. 24, pp. 243 503–1–243 503–3, November 2010, DOI: 10.1063/1.3526722.
- [3] Q. Huang, R. Huang, C. Chen, C. Wu, J. Wang, C. Wang, and Y. Wang, "Deep insights into low frequency noise behavior of tunnel FETs with source junction engineering," in *2014 Symposium on VLSI Technology: Digest of Technical Papers*, June 2014, pp. 1–2, DOI: 10.1109/VLSIT.2014.6894371.
- [4] R. Bijesh, D. K. Mohata, H. Liu, and S. Datta, "Flicker noise characterization and analytical modeling of homo and hetero-junction III–V tunnel FETs," in *70th Device Research Conference*, June 2012, pp. 203–204, DOI: 10.1109/DRC.2012.6257032.
- [5] M. Berg, O.-P. Kilpi, K. M. Persson, J. Svensson, M. Hellenbrand, E. Lind, and L.-E. Wernersson, "Electrical characterization and modeling of gate-last vertical InAs nanowire MOSFETs on Si," *IEEE Electron Device Letters*, vol. 37, no. 8, pp. 966–969, August 2016, DOI: 10.1109/LED.2016.2581918.
- [6] E. Memišević, J. Svensson, M. Hellenbrand, E. Lind, and L. E. Wernersson, "Scaling of vertical InAs-GaSb nanowire tunneling field-effect transistors on Si," *IEEE Electron Device Letters*, vol. 37, no. 5, pp. 549–552, May 2016, DOI: 10.1109/LED.2016.2545861.
- [7] E. Memišević, M. Hellenbrand, E. Lind, A. R. Persson, S. Sant, A. Schenk, J. Svensson, R. Wallenberg, and L.-E. Wernersson, "Individual defects in InAs/InGaAsSb/GaSb nanowire tunnel field-effect transistors operating below 60 mv/decade," *Nano Letters*, vol. 17, no. 7, pp. 4373–4380, June 2017, DOI: 10.1021/acs.nanolett.7b01455.
- [8] E. Burstein, R. H. Kingston, and A. L. McWhorter, *Semiconductor Surface Physics*, ISBN-13: 978-1258339685.
- [9] M. von Haartman and M. Östling, *Low-Frequency Noise in Advanced MOS Devices*, DOI: 10.1007/978-1-4020-5910-0.
- [10] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2095–2110, December 2010, DOI: 10.1109/JPROC.2010.2070470.
- [11] K.-M. Persson, B. G. Malm, and L.-E. Wernersson, "Surface and core contribution to 1/f-noise in InAs nanowire metal-oxide-semiconductor field-effect transistors," *Applied Physics Letters*, vol. 103, no. 3, pp. 033 508–1–033 508–4, June 2013, DOI: 10.1063/1.4813850.
- [12] R. Pandey, B. Rajamohan, H. Liu, V. Narayanan, and S. Datta, "Electrical noise in heterojunction interband tunnel FETs," *IEEE Transactions on Electron Devices*, vol. 61, no. 2, pp. 552–560, February 2014, DOI: 10.1109/TED.2013.2293497.