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1/*f* and RTS Noise in InGaAs Nanowire MOSFETs

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***Abstract*—Low-frequency noise measurements were performed on high-performance InGaAs nanowire MOSFETs. 1/f noise measurements show number fluctuations, rather than mobility fluctuations, as the dominant noise source. The minimum equivalent input gate voltage noise reported here is 80 $\mu m^2 \mu V^2/Hz$, among the lowest values for III-V FETs, and showing the feasibility of a high-quality, low trap density, high-k gate oxide on InGaAs.**

***Keywords*—InGaAs, MOSFETs, Nanowires, 1/f noise, RTS noise, Elastic tunneling**

1. Introduction

Due to their high electron mobility, III-V materials, such as InGaAs, are attractive as a channel material in high-performance field-effect transistors (FETs). Utilizing nanowires (NWs) as the channel in such devices offers improved electrostatic control and enables the use of highly scaled gate lengths [1]. However, due to the lack of a native oxide, the trap density in III-V FETs is typically high (compared with Si/SiO_2 devices), which can degrade the transistor performance and reliability significantly [2]. Thus, accurate and reliable measurements of the interface and oxide quality of III-V FETs are required for the device characterization and the process optimization. Conventional oxide characterization methods, such as C-V and charge pumping methods, cannot be used for ultra small devices without a body contact. Instead, low-frequency (LF) noise measurements can be utilized to analyze the performance and reliability of highly scaled devices [3].

In this paper, we present a low-frequency (LF) noise study (1/*f* as well as RTS noise) on high-performance InGaAs NW MOSFETs [4]. 1/*f* noise measurements show number fluctuations, rather than mobility fluctuations, as the dominant noise source. Furthermore, a low equivalent input gate voltage noise of 80 $\mu m^2 \mu V^2/Hz$ is achieved, showing the feasibility of a high-quality gate oxide on InGaAs.

2. Device Fabrication

The $In_{0.85}Ga_{0.15}As$ NWs are formed on semi-insulating InP:Fe by selective area MOCVD growth using HSQ as a growth mask [5]. Each device consists of a single nanowire. Highly doped ($N_D \sim 5 \cdot 10^{19}$ cm^{-3}) InGaAs source/drain contacts are formed in a second growth step using an HSQ dummy gate (figure 1). Ti/Pd/Au source/drain metal is deposited by thermal evaporation. After surface precleaning by Ozone, $(NH_4)_2S$ (10%) for 20 min, and five cycles of in situ TMA1 pulses, Al_2O_3/HfO_2 (5/45 cycles, EOT ≈ 1.2 nm) is deposited as the gate oxide by ALD at 300/100 °C. Ni/Pd/Au gate metallization by thermal evaporation completes the process. A schematic of a fabricated device is depicted in figure 2. Details on the device fabrication can be found in [6].

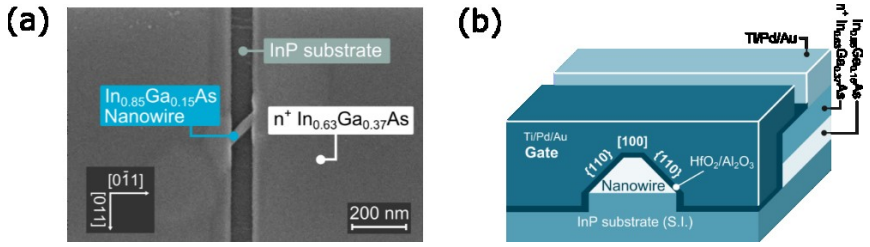

Fig.1: (a) SEM image (top view) after the nanowire growth. (b) Schematic figure of a fabricated device.

3. Methods and Results

Excellent DC performance was reported for these devices previously, with a peak transconductance of 2.9 mS/µm, a minimum subthreshold slope of 77 mV/decade and an on-current of 565 µA/µm (at I_{off} = 100 nA/µm), all at V_{ds}= 0.5 V, the highest reported on-current for any transistor [6]. Furthermore, it was shown that these transistors operate in the quasi-ballistic regime with a transmission of about 70 %, which was obtained from quantized conductance measurements at 10 K, and was shown to be valid also at room temperature [5].

Here, we performed 1/*f* and RTS noise measurements on devices with varying gate lengths (L_g = 50-85 nm) and gate widths (W = 27–100 nm). W refers to the gated perimeter of the nanowire.

For both types of measurements, a Lake Shore Cryotronics CRX-4K probe station was used to contact the transistors and to control the temperature. When performing the 1/*f* noise measurements, a low-noise current preamplifier (model SR570 from Stanford Research Systems) was utilized to supply a constant drain voltage of 50 mV and to amplify the drain current signal. The output of the current preamplifier was connected to a lock-in amplifier (model SR830 from Stanford Research Systems) to measure the drain current noise (S_{Id}). A Keysight B2912A source measure unit (SMU) was used to set the gate voltages and to monitor the source current during the measurements.

For the RTS noise measurements, only the Keysight B2912A SMU was utilized to set the drain and gate voltages and to measure the drain current.

The 1/*f* noise measurements show that the normalized drain current noise (S_{Id}/I_d^2) is inversely proportional to the gate area $A = L_g W$ (at a fixed drain current), indicating that the LF noise originates from the channel rather than from the source/drain resistance (figure 2 (a)). If the LF noise had arisen from the source/drain resistance instead, S_{Id}/I_d^2 would have been be independent of A.

In contrast to a previous study on highly scaled InGaAs GAA MOSFETs [3], our measurements show that number fluctuations (rather than mobility fluctuations) are the dominant LF noise source, as the normalized drain current noise

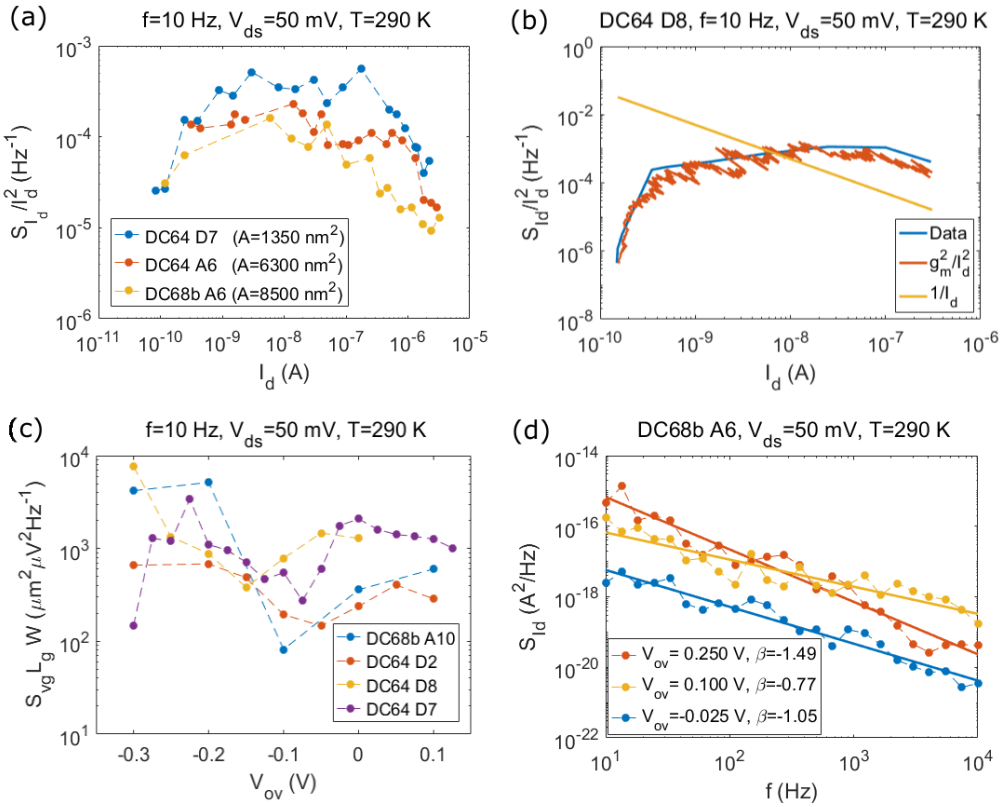

Fig.2: (a) Impact of the gate area scaling on the normalized drain current noise, showing that the LF noise originates from the channel. (b) The normalized drain current noise follows the transconductance in all devices, indicating that number fluctuations are the dominant noise mechanism. (c) Low values for the equivalent input gate voltage noise over a large gate voltage overdrive range for device DC68b A10 (L_g = 70 nm, W = 78 nm), DC64 D2 (L_g = 50 nm, W = 27 nm), DC64 D8 (L_g = 50 nm, W = 27 nm) and DC64 D7 (L_g = 50 nm, W = 27 nm). (d) Gate voltage dependence on the f^{β} noise exponent (β) for transistor DC68b A6 (L_g = 85 nm, W = 100 nm).

follows g_m^2/I_d^2 (instead of $1/I_d$) in all our devices. This observation is exemplified in figure 2 (b) for a single transistor with L_g = 50 nm and W = 27 nm, but is valid for all transistors (independent of L_g and W) and is here reported for quasi-ballistic devices.

As shown in figure 2 (c), we observe low values for the equivalent input gate voltage noise ($S_{VG} = S_{Id}/g_m^2$) over a large gate voltage overdrive ($V_{ov} = V_{gs}$-V_T) range with minimum values of 80 µm²µV²/Hz, demonstrating an excellent oxide quality in our devices. The corresponding trap density can be calculated by using [7]

$$N_t = \frac{fWL_G C_{ox}^2 S_{VG}}{q^2 k_B T \lambda} \text{ [cm}^{-3}\text{eV}^{-1}\text{]}. \quad (1)$$

In equation (1), C_{ox} is the oxide capacitance per unit area and λ is the tunneling attenuation length in the gate oxide, given by $\lambda = \left(\frac{4\pi}{h}\sqrt{2m^*\Phi_B}\right)^{-1}$ [7]. Assuming an effective electron mass of $m^* = 0.23\, m_e$ [8] in Al_2O_3 and an oxide barrier height of $\Phi_B = 2.4$ eV [9], the trap density is as low as ~ $9 \cdot 10^{18}$ cm^{-3}eV^{-1}. This correlates with the low minimum subthreshold slope of 77 mV/decade in these devices.

Furthermore, a gate voltage dependence on the f^{β} noise exponent (β) is observed, which can be attributed to a spatially non-uniform trap distribution in the gate oxide (depicted in figure 2 (d) for a transistor with L_g = 85 nm and W = 100 nm). If the trap density close to the gate oxide/channel interface is higher (lower) than that in the interior of the gate oxide, β is larger (smaller) than -1. For a trap density that is uniform in depth, β = -1 [7]. In all our devices, β typically varies between -0.7 and -1.5 when sweeping the gate voltage overdrive from -0.2 V to 0.3 V. This clear gate voltage dependence on β indicates that relatively few traps limit the performance of the devices; otherwise the trap density would be more uniform in depth leading to β = -1 independent of the gate voltage (assuming there are no spatial preferences for the trap formations in the gate oxide).

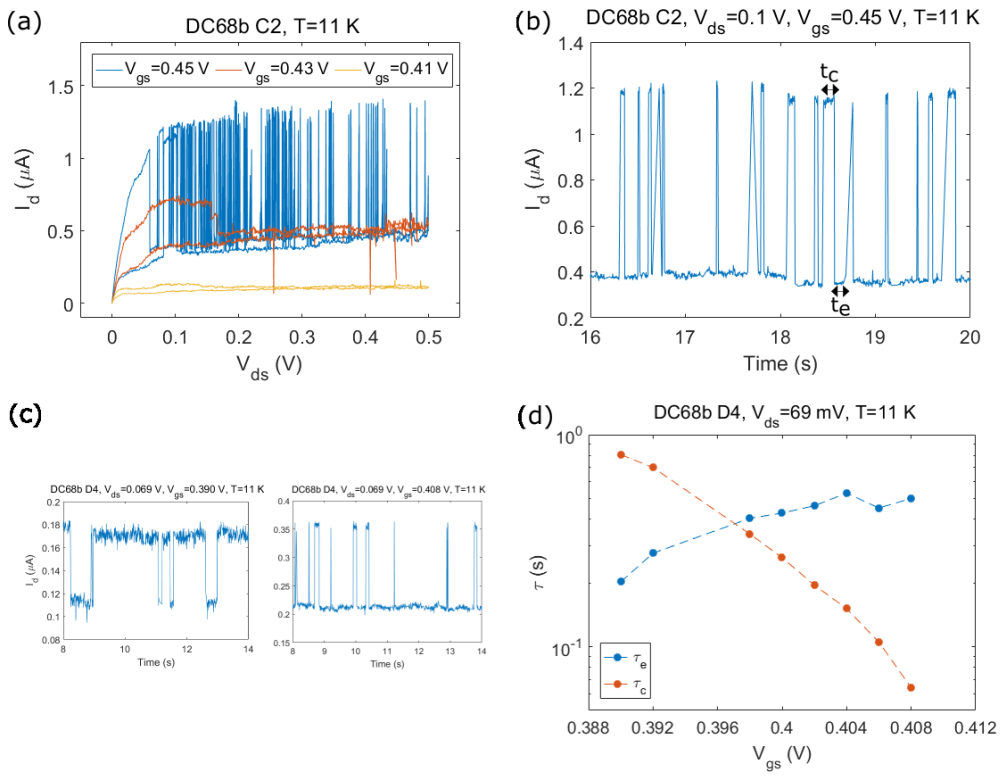

Fig.3: (a) Output characteristic for transistor DC68b C2 (L_g = 55 nm, W=32 nm) showing large drain current fluctuations. (b) Excerpt of the measured RTS noise signal at V_{ds}=0.1 V and V_{gs}=0.45 V (c) Excerpt of an RTS noise signal for transistor DC68b D4 (L_g = 70 nm, W=31 nm) at V_{ds}=0.069 V (fixed) and V_{gs}=0.39 V (left) and V_{gs}=0.408 V (right). (d) Variation of the capture and emission time constant with gate voltage for the same defect as in (c).

To study the impact of single trap states, we also performed low temperature RTS noise measurements. RTS noise signals were observed in ~2/3 of our devices.

In a small number of transistors, we found RTS noise with a large drain current amplitude (ΔI_D) of up to 1 µA. Figure 3 (a) shows the output characteristic of such a device and in figure 3 (b), an excerpt of the drain current signal is shown over time for V_{ds} = 0.1 V and V_{gs} = 0.45 V. At this bias point, the drain current amplitude is ~ 0.8 µA (relative drain current amplitude $\Delta I_D/I_D = 67$ %) and the characteristic capture and emission time constants (τ_c and τ_e, respectively) are: $\tau_c = 0.046$ s and $\tau_e = 0.267$ s. The different values of the time constants can be qualitatively explained by the position of the trap energy level relative to the semiconductor Fermi level. In this case, the trap energy level is located below the Fermi level, meaning that a large number of electrons have enough energy to tunnel elastically into the trap state, giving rise to a small τ_c. However, tunneling out of the trap state requires an empty state at the same energy level in the semiconductor, which is hindered when the trap energy level is located below the semiconductor Fermi level. This leads to a higher τ_e.

Figure 3 (c) and (d) show the impact of the gate voltage on the capture and emission time constant of a single defect in another device. τ_c and τ_e, vary with the gate voltage since the trap energy level is shifted relative to the semiconductor Fermi level. τ_c decreases with increasing gate voltage while the opposite trend is observed for τ_e. At the bias point, where $\tau_c = \tau_e \approx 0.38$ s, the trap energy level is aligned with the Fermi level and the trap depth in the oxide can be estimated using [7]:

$$z_t = \lambda \ln\left(\frac{\tau}{\tau_0}\right), \quad (2)$$

with τ_0 being the tunneling time constant for a trap state at the semiconductor/oxide interface. Assuming $\tau_0 = 10^{-10}$ [7], the trap depth is ~ 2.9 nm. The calculation of z_t bases on elastic tunneling of electrons to and from the trap state; possible effects of a quantized inversion layer were not considered.

Modeling of single trap induced subband fluctuations yields an RTS noise drain current amplitude between 0.05 to 0.7 µA for traps at a depth of around 2.9 nm, depending on the exact lateral position of the trap along the channel. These numbers are in good agreement with the measured RTS noise amplitudes, as shown in figure 3 (a)-(c).

4. Conclusion

In summary, we performed LF noise measurements on high-performance InGaAs NW MOSFETs, demonstrating number fluctuations as the dominant LF noise source and low values of 80 $\mu m^2 \mu V^2/Hz$ for the equivalent input gate voltage noise, showing the feasibility of a high-quality gate oxide on InGaAs.

Acknowledgements

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