A 160MHz bipolar wideband IF amplifier

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A 160-MHz Bipolar Wide-Band IF Amplifier

Henrik Sjöland and Sven Mattisson

***Abstract*— Wide-band intermediate-frequency (IF) amplifiers are needed when the data rates of communication systems increase. A single wide-band IF amplifier can also be used for a radio band with several narrow-band channels of varying strengths. High linearity is then required if intermodulation products are not to disturb weak channels. We have previously reported a highly linear wide-band IF amplifier in a complementary metal–oxide–semiconductor. Using a similar topology, an npn-only bipolar amplifier with even higher linearity is now presented. The amplifier is fully differential and operates with a 5-V supply. At 20 MHz, 5 V_{pp} over a 1-kΩ load, the measured total harmonic distortion is just 0.068%.**

***Index Terms*—Amplifiers, bipolar, high linearity, IF, wideband.**

I. INTRODUCTION

A HIGHLY linear npn-only bipolar wide-band intermediate-frequency (IF) amplifier is built using a topology previously reported for a complementary metal–oxide–semiconductor (CMOS) amplifier [1]. The main motivation for building amplifiers in both bipolar and CMOS is that we want to be flexible in the choice of technology. In a system with several building blocks on the same chip, the requirements of the other parts may then determine which technology to use.

Since the intermodulation noise is critical for the performance of a wide-band IF amplifier, the nonlinearity must be minimized. To achieve this, we use the same techniques as in [1]. A push–pull class A output stage is used together with a double-nested Miller compensation to maximize the feedback around it [2], [3]. To cancel out even-order distortion, the topology is fully differential.

II. OUTPUT STAGE

As in the CMOS amplifier, we use a push–pull class A output stage for best linearity. To accomplish push–pull operation, an emitter follower arrangement is used (see Fig. 1). This reduces the output voltage swing, and a 5-V supply is therefore used.

The output transistors are Q_1 and Q_2, where Q_1 is connected as a follower. As the stage is biased in class A, the transistors are on all the time. The output voltage therefore essentially follows the base voltage of Q_1. When the collector current of Q_3 is low, the output voltage is therefore high. The collector current of Q_2 is then also low, as it is connected in parallel with Q_3. If, on the other hand, the current of Q_3 is high, the output is low and the current of Q_2 is high. The stage is thus a push–pull stage.

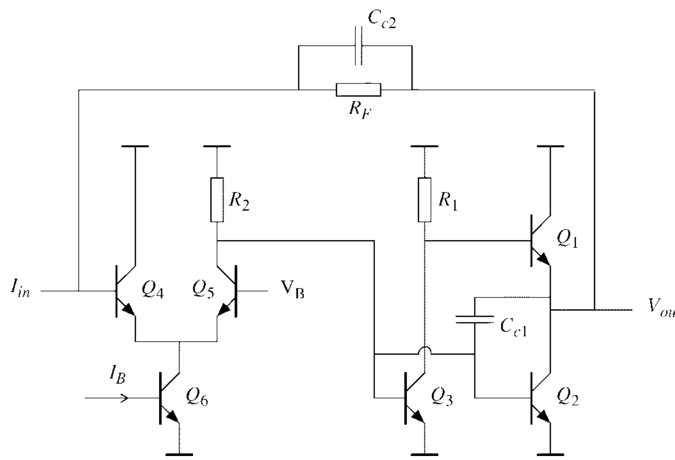

Fig. 1. The output stage.

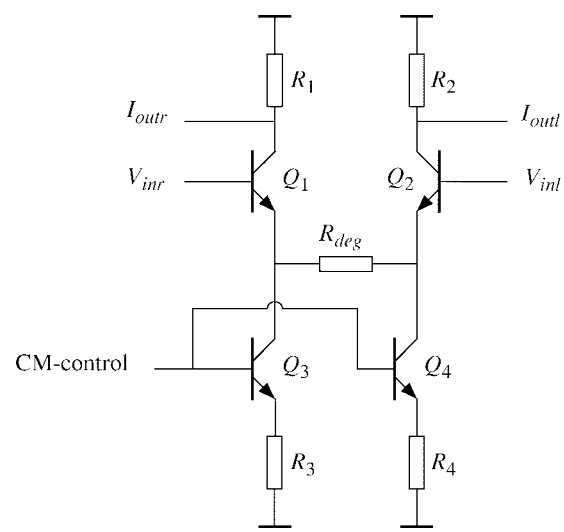

Fig. 2. The input stage.

If the quiescent collector current of transistor Q_2 is high enough, the stage will operate in class A. The collector current through Q_2 is the same as through Q_3 scaled by their emitter areas. The quiescent collector current of Q_3 is determined by R_1 and the quiescent output voltage, that is fixed by a common mode feedback circuit. The bias of the output stage is thus determined by R_1 and the emitter area ratio of Q_2 and Q_3.

To provide more gain, a long tailed pair (LTP) stage (Q_4, Q_5) precedes the push–pull stage. This stage also provides some level shift, which is needed as no pnp devices are allowed. The absence of pnp devices also makes it necessary to use a resistor R_2 as a current source for the stage. A double

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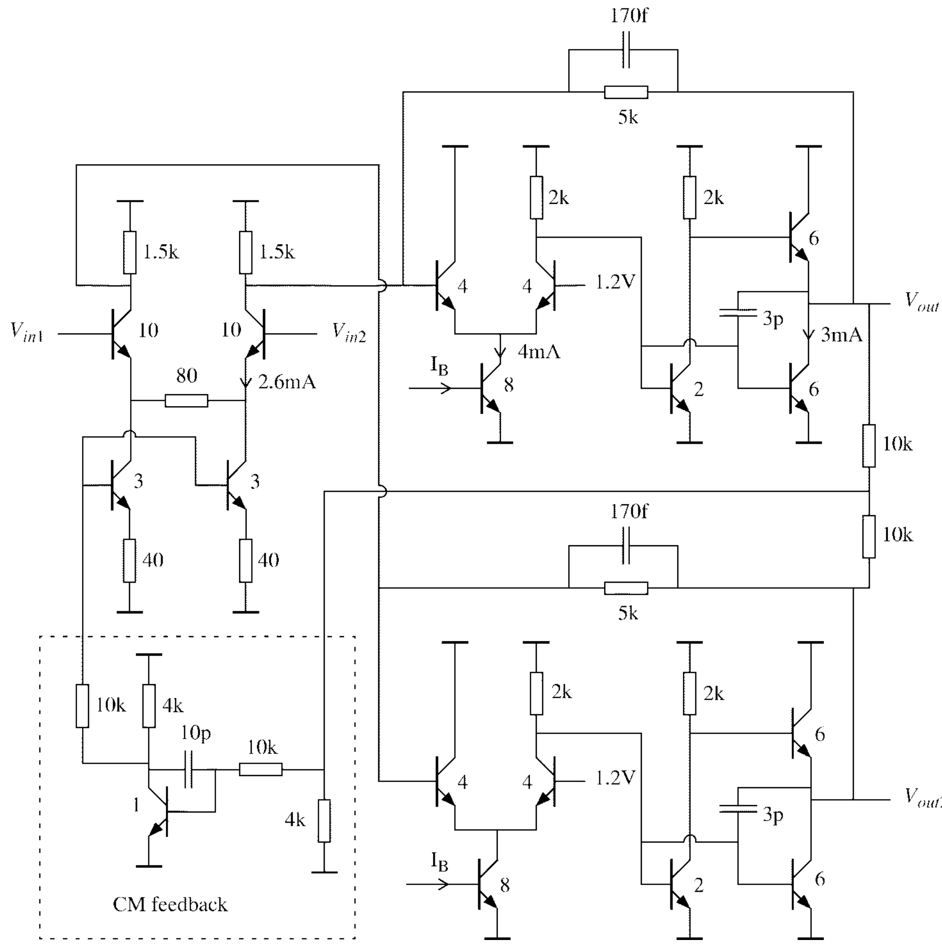

Fig. 3. The entire schematic with parameters. The numbers at the transistors indicate number of unit devices used. Each unit device has a 15 × 1 μm emitter.

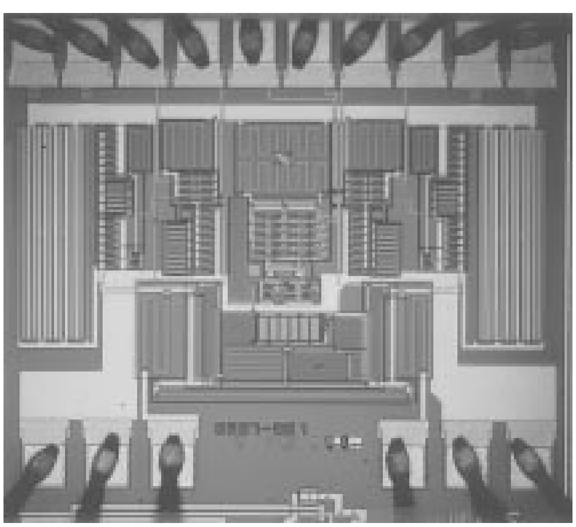

Fig. 4. Die photo of the amplifier.

nested Miller feedback scheme is used to linearize the already highly linear output stage further. As the push–pull stage is inverting, the innermost Miller capacitor C_{c1} can be connected directly over it. The LTP stage is noninverting, enabling C_{c2} to be connected over the cascade of the LTP and push–pull stage. A feedback resistance R_F makes the output stage a transresistance stage.

TABLE I
SOME SIMULATION AND MEASUREMENT RESULTS

	Simulation	Measurement
Supply voltage	5V	5V
V_{cm} input range	1.2V-1.7V (nom. 1.4)	1.15V-1.8V (nom. 1.4)
Current consumption	26.7mA	24.4mA
Voltage gain	96	100
Bandwidth	160MHz	190MHz
IP3 (out) @ 20MHz, 10MHz	43dBV, 41.5dBV	42dBV, 40.5dBV
NF (R_s=2*100Ω) @ 10MHz	3.6dB	5.4dB +/- approx. 1dB

III. INPUT STAGE

As transresistance output stages are used, the input stage must be a transconductance if the cascade is to become a voltage amplifier.

We use a resistor loaded differential stage with differential output as input stage. The desired voltage gain of the entire amplifier is 100, and the maximum output amplitude is about 6 V_{pp}, resulting in about 60 mV_{pp} maximum input signal amplitude. If the input stage is not to degrade the linearity, emitter degeneration must then be employed. The drawback is a degraded noise performance.

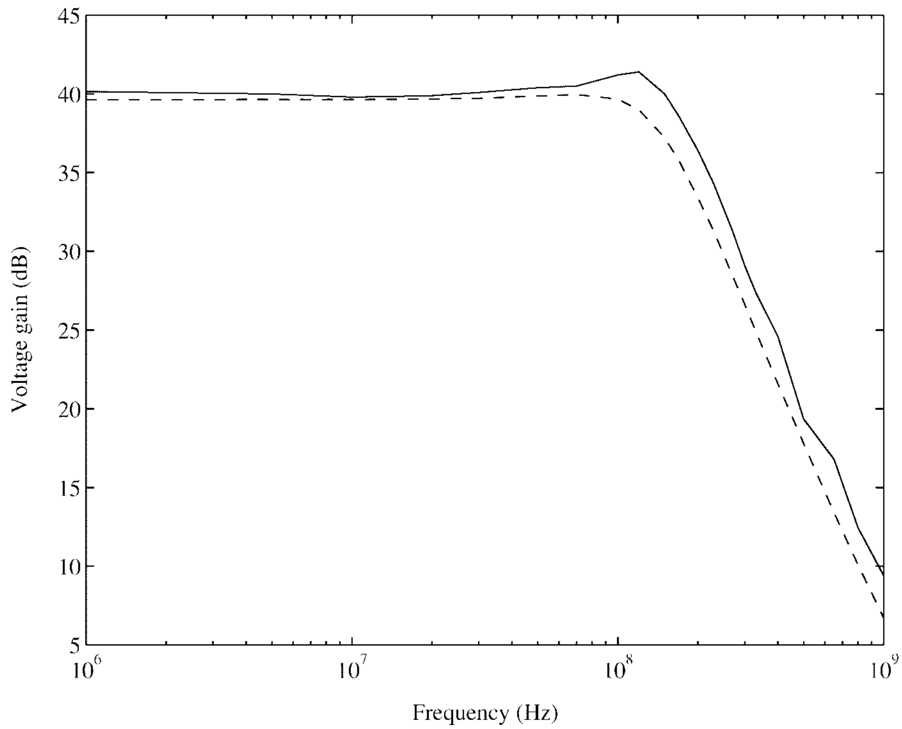

Fig. 5. Frequency response, measured (solid line) and simulated (dashed line).

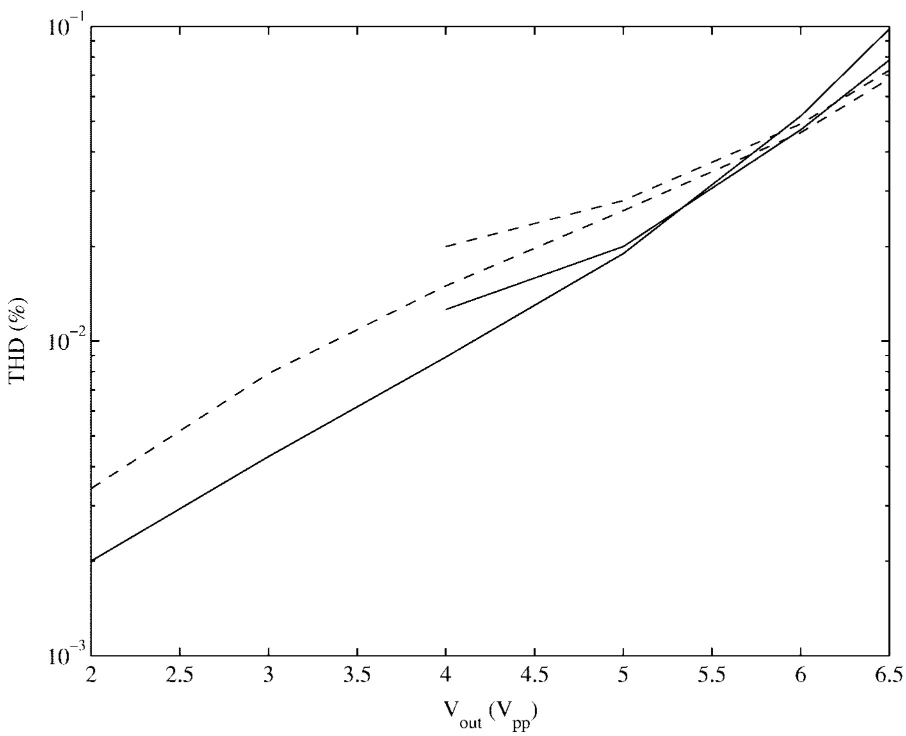

Fig. 6. Measured and simulated distortion versus output voltage. Solid line: 20 MHz. Dashed line: 10 MHz. The curves of measured distortion start at 4 V_{pp}.

The noise performance is further degraded by the use of two current sinks. This is not optimal, as the noise of the current sinks does not enter the circuit in a common node. According to simulations, the noise figure is degraded by about 1 dB, compared to an input stage with one current sink. If the circuit was to be refabricated, one current sink would be used. The input stage is shown in Fig. 2.

IV. Simulations and Measurements

The entire schematic with device parameters is shown in Fig. 3. This is what was simulated, sent to fabrication, and measured. The circuit was fabricated in the bipolar part of a 0.8-μm BiCMOS process, and the die size was 1.2 $\times$ 1 mm including pads. A die photo is shown in Fig. 4.

Some of the most important measurement and simulation results are presented in Table I.

The simulated phase margin was 70° in the outer loop and 60° in the inner, with a 3-pF load. The phase margin of the outer loop is relatively insensitive to load variations. In the measured frequency response, however, there is a little peak that could be explained by a somewhat reduced phase margin in the outer loop (Fig. 5).

The distortion was simulated and measured, with 1 kΩ differential load and 1 kΩ from each output to ground. The results are presented in Fig. 6. The curves for measured distortion start at 4 V_{pp}, because noise made the measurements inaccurate at lower levels.

For common-mode input voltages between 1.2 and 1.7 V, the performance was as indicated above. The range is limited by the demand for the input stage transistors not to be saturated.

V. Conclusions

This topology can be used for npn-only bipolar wide-band IF amplifiers, as well as CMOS. A bipolar circuit with the same power consumption as one in CMOS was made. The bipolar amplifier has higher linearity, since the bipolar devices are faster and have higher transconductance than CMOS for similar operating conditions.

Drawbacks of the bipolar circuit, caused by the absence of pnp devices, are smaller common-mode input voltage range and a higher supply voltage. In a BiCMOS circuit, P-channel MOS devices can be used instead of pnp. By using a current mirror load in the LTP stage, the loop gain could then be doubled. Without reducing the performance, the power consumption could be reduced because of the reduced supply voltage and the current mirror.

References

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