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An 8-GHz Beamforming Transmitter IC in 130-nm CMOS

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***Abstract*— An 8-GHz beamforming transmitter IC has been designed in a 130-nm CMOS process. Two power amplifiers with independently controllable phase enable the beamforming. The phases are digitally controllable over the full 360° range, which is accomplished by binary weighting of quadrature phase signals in the power amplifiers. The quadrature phase signals are generated by a quadrature voltage controlled oscillator followed by a buffer, which serves as an isolation between the power amplifiers and the oscillator. The chip contains seven on-chip differential inductors, and consumes a total of 47 mA from a 1.0 V supply. The measured output power is -3 dBm for each power amplifier.**

I. Introduction

This work is part of a project directed to find transceiver architectures and circuit topologies that can cope with the trend of scaling CMOS technology, which leads not only to higher transit frequencies, but also to lowered supply voltages, resulting in decreased dynamic range for receivers and less output power for transmitters. These changes put new demands designing analog circuits, but also enables the use of CMOS at higher frequencies. New applications for RF CMOS could be automotive radar at 24 and 77 GHz [1]–[3] and indoor WLAN at 60 GHz [4]–[6]. This project is aimed at 60 GHz CMOS WLAN.

A 130-nm CMOS 8-GHz beamforming transmitter IC is presented, consisting of a Quadrature Voltage Controlled Oscillator (QVCO), a tuned buffer, and two Power Amplifiers (PAs) (Fig. 1). The output phase of each PA is controllable through 360° to enable beamforming. Beamforming and electronic scanning are suitable for radar systems and can also be used in WLAN. In a WLAN system it is beneficial to steer the antenna lobe of the transmitter towards the intended receiver. Less power then needs to be transmitted, saving battery energy and relaxing the requirements on the PAs. Less interference to other communication devices is also generated, increasing the total system capacity.

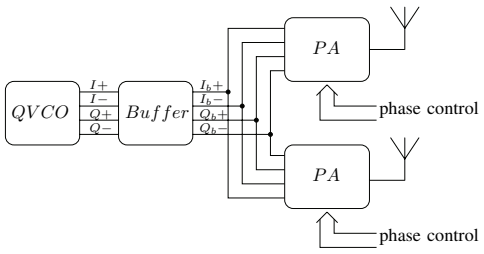

Fig. 1. Block diagram of the beamforming transmitter

II. Circuit Topology

The PAs (Fig. 2) are designed to have high gain and isolation without having too large input capacitance, since this capacitance has to be driven by the buffer (included in its resonance tank).

The buffer (Fig. 3(b)) is needed to ensure that the QVCO (Fig. 3(a)) has a fixed load impedance. Without it the QVCO would be affected by the output signal of the PAs, because the large signal swings of the PAs drive the cascode transistors into triode region for parts of the signal cycle, diminishing the isolation of the cascodes. A changing antenna impedance caused by a changing environment would thus effect the QVCO. Furthermore, the input impedance of a PA changes as its phase is changed by a new phase control word. All this would degrade the accuracy of the quadrature signal generated by the QVCO, and thereby also the accuracy of the beamforming. An even worse problem is that a shifting load would shift the frequency of the QVCO, and of the entire transmitter. This effect could, however, be significantly suppressed by locking the frequency of the QVCO to a crystal reference using a PLL frequency synthesizer.

The QVCO operates at a rather high amplitude. This brings down the phase noise and ensures a reliable start-up. In between each building block there are capacitive taps, which decreases the loading of the previous stage and increases the isolation. The tap consists of the input capacitance of the following stage and an additional series capacitance, which also performs an AC-coupling.

A. Power Amplifier

The PA consists of binary weighted transistors for each of the four quadrature phases. They can be switched on and off by cascode transistors. The cascode transistors can also be used to select the direction of the signal current, towards the positive or negative differential output (Fig. 2). By switching on and off and directing the current of the transistors in different combinations, the phase of the output is controllable through 360°, and thus the antenna lobe is steerable in any direction. When the current of transistor V_{x_y} is directed towards the positive output branch, the current of transistor V_{x+180_y} should be directed towards the negative out-

put branch, see Fig. 2. This switching scheme ensures a differential output of the PA.

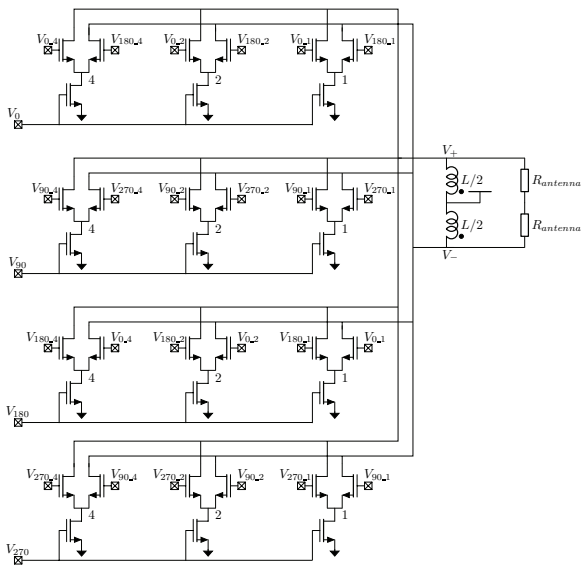

Fig. 2. Schematic of the power amplifier with three binary weighted transistors per bank

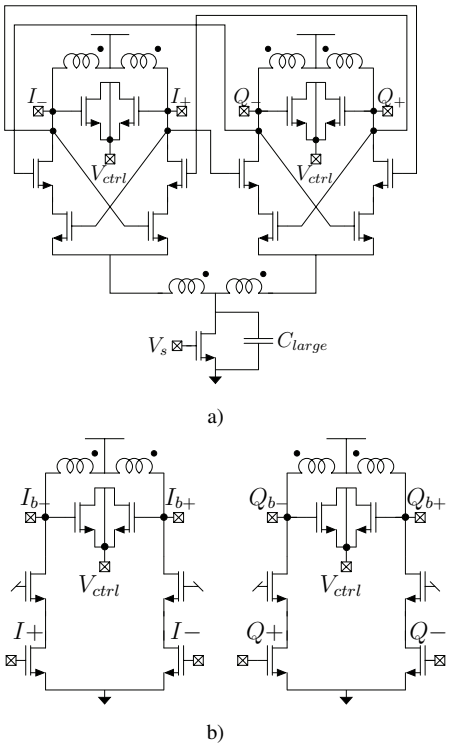

Fig. 3. a) Topology of the QVCO b) Topology of the tuned buffer

This circuit has a control word length of three (transistors weighted by 1, 2 and 4) leading to a rather large phase discretization. This makes it manageable to sweep the phase directly without using a shift register or digital encoding of control words. There is no restriction to increasing the resolution by adding smaller transistors. The output power will vary somewhat for different phase settings, and an increased phase resolution also has the benefit of reducing this power variation.

B. Quadrature Voltage Controlled Oscillator and Buffer

The topology of the oscillator and buffer is almost the same as in [7]. This topology (Fig. 3) is chosen because it is robust and has a high quadrature accuracy. The phase noise performance is also good thanks to the series connected transistors [8], and the inductor tuning the source node of the VCO to twice the frequency of oscillation [9].

A difficulty when designing an oscillator at this high frequency is that the reactance of the resonance tank is quite low. It is further reduced by the capacitive load of the buffer. The inductance of the resonance tank must therefore be very small. The limit to how small it can be made is set by the parasitic inductance. Since the tank is fully integrated using short on-chip wires, a 630 pH differential inductor could be used.

The buffer is separately tuned (Fig. 3(b)) with the PAs as load. The inductance is slightly smaller due to the heavy loading of the gate capacitance of the PAs. A varactor is used also in the buffer to maximize its output voltage swing over the operating frequency range, and to reduce its current consumption, [7]. The same control voltage, V_{ctrl}, is used in both the QVCO and the buffer.

C. On-Chip Inductors

The process has eight metal layers in copper, above a lightly doped substrate. Only differential inductors are used in this fully differential circuit. Two inductors at the output of the PAs form resonance tanks with the parasitic drain-bulk capacitance of the cascode transistors. The drain current to the PAs is also fed through these inductors. Two inductors each are used in the QVCO and buffer resonance tanks. Finally one inductor is used at the source nodes of the switching pairs in the QVCO.

The quality factor (Q) of the differential inductors is quite high thanks to the excellent process, resulting in a low power consumption of the QVCO and buffer. The in-house inductor optimization software, Indentro [10], was used to find the geometry and metal layers to use. It is a very quick tool where one can sweep different parameters and put restrictions on others, e. g. f_{srf} $\geq$20 GHz. After finding a promising geometry an .ind-file can be exported to FastHenry [11] and simulated there as well. The agreement is quite good, but FastHenry typically gives a somewhat lower Q and L. Since a high resistivity substrate is used the Eddy current in the substrate can be neglected. The capacitively coupled substrate losses are blocked by a patterned ground shield. The substrate therefore does not need to be included in the simulations, and FastHenry gives accurate results. A .cif-file can also be exported from Indentro to the Cadence layout environment. The .cif-file contains all metal traces and vias for inter-

connect. The key for all simulations to be accurate is a correct technology file, where all thicknesses and electrical properties of the different layers of the semiconductor process are specified.

III. Results and Measurement

The circuit, Fig. 4, was flip chipped onto a gold plated Printed Circuit Board (PCB). This minimizes the parasitics going on an off chip. Three different chips were mounted on PCBs and tested.

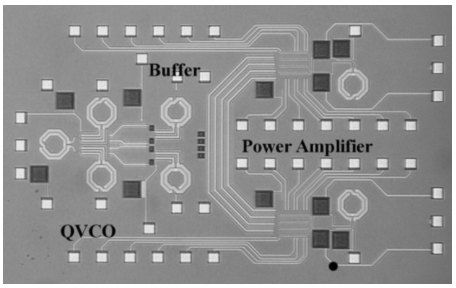

Fig. 4. Chip microphotograph

A. Quadrature Voltage Controlled Oscillator

The phase noise of the QVCO was measured[1], see Fig. 5, and compared with the simulated phase noise. As one can see the phase noise agrees well between simulation and measurement. The Figure of Merit (FoM) was calculated according to (1) and found to be, in average over the three chips, 181 dB @ 3 MHz offset frequency, which is the same as in the simulation. The measured current consumption from a 1 V supply was 15.5 mA compared to 17.5 mA simulated.

$$FoM = \left(\frac{f_0}{f_m}\right)^2 \frac{1}{\mathcal{L}(f_m)V_{dd}I_{VCO}(mA)} \tag{1}$$

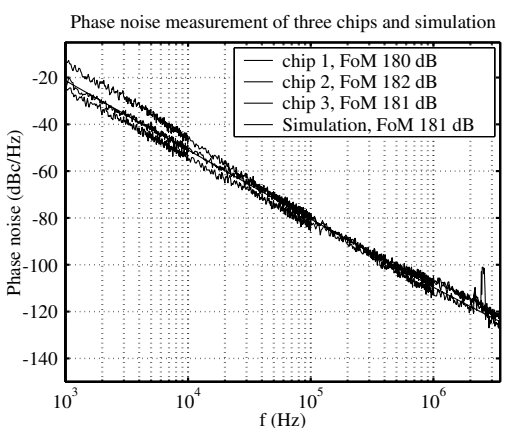

Fig. 5. Measured and simulated phase noise of the QVCO

[1]The phase noise was measured with a PN9000 measurement system by Aeroflex Europtest.

A measurement of the quadrature error of the QVCO is not possible, since the QVCO output is not directly accessible. Instead the quadrature error has been measured after the PAs, that is the whole transmitter quadrature error has been measured. The error was 3.2° on average.

B. Power Amplifier

To measure the power amplifier, its differential outputs were connected to a balun[2], which in turn was connected to a spectrum analyzer. The spectrum analyzer was calibrated with a power meter. The PA not connected to the spectrum analyzer was terminated in 50 Ω after the balun. The measured power was compensated for the total losses in connectors, cables, balun, and PCB, which were measured to 5 dB[3] using a Network Analyzer.

The maximum output power was found by adjusting the bias conditions for the QVCO, buffer, and PA. It was measured over the full tuning range for the three chips, see Fig. 6. As can be

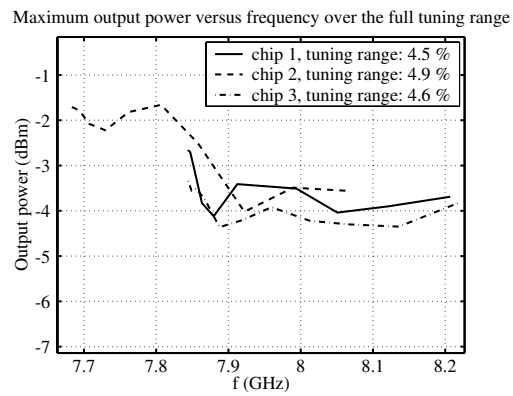

Fig. 6. Maximum output power versus frequency over the full tuning range for the three chips

seen chip 1 and 3 have approximately the same output power and frequency, difference less than a dB over the full range, and they have quite constant output power over the full tuning range.

To be able to measure the phase at the output of the PAs the frequency was downconverted using two mixers. The Intermediate Frequency (IF) was chosen to 50-100 MHz. The IF signals were measured with a digital oscilloscope and from the measurement data the phase difference was calculated. The phase difference between different phase control words was measured as the phase change between the two PA outputs. It is necessary to measure the phase of one PA relative to that of the other, since the QVCO is free-running and not locked in a phase locked loop. The waveforms at the oscilloscope have noise and harmonics, thus a

[2]Balun: Krytar 6-26.5GHz, spectrum analyzer: Rhode & Schwartz FSU 20Hz-50GHz, power meter: Hewlett Packard 437B, mixer: Mini-Circuits ZMX-10GHz, oscilloscope: Tektronix 4GHz, 40GS/s, network analyzer: Agilent Technologies E8361A 10MHz-67GHz.

[3]It is worth mentioning that there are many different connectors needed going from the spectrum analyzer to an SMA connector of the right gender.

Fourier expansion was performed, and the phase of the fundamental tone was used.

The phase has been measured over one quadrant for all three chips (Fig. 7). The measured and theoretical phase correspond well, with an average phase discrepancy of 3.2°. A slight curvature can be observed, however, which is due to an amplitude mismatch between I and Q. Performing a full 360° sweep at reduced PA bias (class C) increases the effect. The mismatch is therefore believed to be located prior to the PAs in the signal chain.

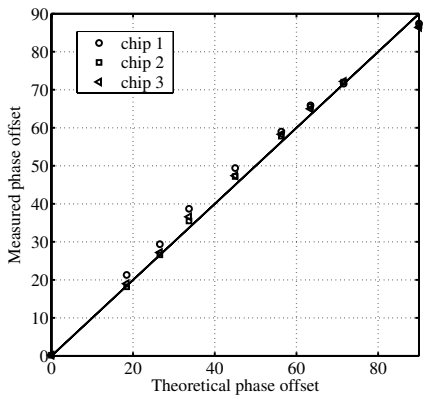

Fig. 7. Output phase of the three PAs over one quadrant

C. Summary

Table I is a summary of the measurement results in comparison to the simulated results. The current consumption is lower for all building blocks in the measurement. The oscillator FoM is the same in both simulations and measurements, but the tuning range differs quite a bit, which could spring from inaccurate modeling of the nMOS varactor. The output power is slightly lower than simulated.

TABLE I
COMPARISON BETWEEN MEASUREMENTS AND SIMULATIONS FOR THE TRANSMITTER

	Simulated	Measured
V_{dd} (V)	1.0	1.0
I_{DC} (QVCO) (mA)	17.5	15.5
I_{DC} (Buffer) (mA)	19.0	17.3
I_{DC} (PA) (mA)	18.3	13.8
Phase Noise @ 3 MHz (dBc/Hz)	-123	-122
FoM @ 3 MHz (dB)	181	181
Quadrature phase error (°)	-	3.2
Tuning Range (%)	2.2	4.7
Tuning Range (MHz)	190	370
Output Power (dBm)	-0.42	-3

IV. CONCLUSION

An 8-GHz CMOS beamforming transmitter circuit in 130-nm CMOS is presented, featuring a quadrature oscillator with low phase noise (-120 dBc/Hz @ 3 MHz offset) and two phase controlled power amplifiers, each with an output power of -3 dBm. To be able to deliver the amount of power needed to transmit high date rates at high frequency (60 GHz), with CMOS technology, multiple power amplifiers and beamforming will be needed. Also at lower frequencies (IEEE 802.11) beamforming can be valuable to reduce interference by mainly transmitting in the wanted direction, thus allowing more units to operate in the same cell with good SNR. This work shows a robust PA design with 360° output phase control range suitable for beamforming applications.

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