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Scaling of Vertical InAs-GaSb Nanowire Tunneling Field-Effect Transistors on Si

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***Abstract*— We demonstrate improved performance due to enhanced electrostatic control achieved by diameter scaling and gate placement in vertical InAs-GaSb Tunneling Field-Effect Transistors integrated on Si substrates. The best subthreshold swing, 68 mV/dec at V_{DS} = 0.3 V, was achieved for a device with 20 nm InAs diameter. The on-current for the same device was 35 µA/µm at V_{GS} = 0.5 V and V_{DS} = 0.5 V. The fabrication technique used allow downscaling of the InAs diameter down to 11 nm with a flexible gate placement.**

***Index Terms*— HSQ, Nanowire, III-V, TFET, transistor, InAs-GaSb**

I. Introduction

Scaling of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) has led to an increased transistor density that constrains the power consumption [1], [2]. It is hence desirable to scale the drive voltage. To maintain the off-state leakage, the subthreshold swing (*SS*) needs to be as low as possible, where the limit is 60 mV/dec for MOSFETs. Further voltage scaling beyond that of MOSFETs optimally requires devices that can reach a subthreshold swing below 60 mV/dec. One promising technology is the Tunneling Field-Effect Transistor (TFET), which uses quantum mechanical tunneling to filter the thermal injection [3], [4]. A challenge is to fabricate TFETs with a steep slope and large on-currents (I_{on}). We here present highly scaled, vertical InAs/GaSb nanowire TFETs utilizing a gate all-round (GAA) geometry for good electrostatic control [5], [6]. The broken bandgap of the InAs/GaSb junction and low channel effective mass provides a high on-current [7], [8], [9] demonstrated previously on lateral nanowire devices [10]. In this paper, we study the effects of nanowire diameter scaling and gate-metal placement on the TFET performance. We show that the InA/GaSb nanowire heterostructure can provide TFET performance capable to staggered heterostructure [11], [12].

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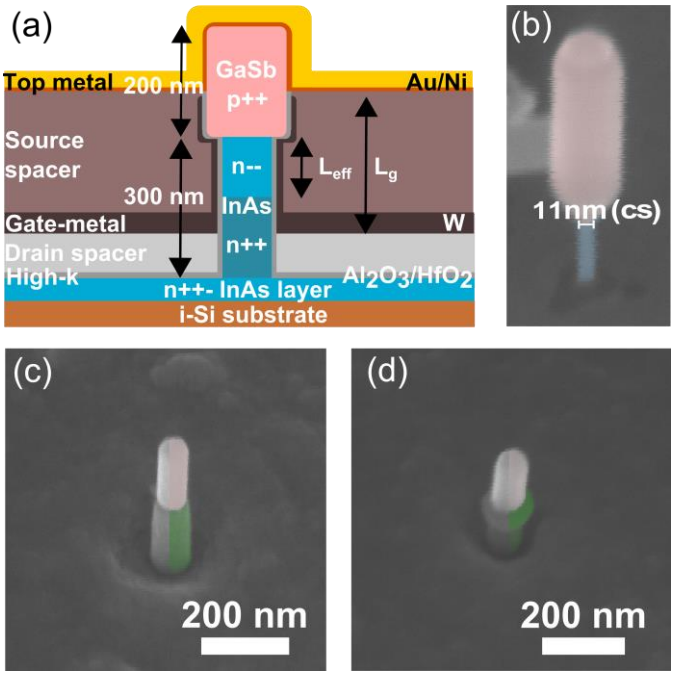

Fig. 1. (a) Schematic illustration of the vertical nanowire TFETs. Given lengths of the InAs and GaSb segments are applicable on the nanowires with HSQ drain spacer. (b) A colorized SEM image of the InAs-GaSb nanowire after digital etching. (c, d) SEM images of two devices with HSQ as drain spacer and gate-metal. Placement of the gate-metal is controlled using HSQ with different thicknesses. The gate-metal on the nanowires is colorized with green on the right half. In c) the gate is perfectly aligned with the heterojunction while in d) it is overlapping the junction.

II. Device Fabrication

InAs/GaSb nanowires were grown using vapor-liquid-solid growth method on an 200-nm-thick n^+-InAs layer integrated on a highly resistive Si (111) substrate (ρ=5.5 kΩ-cm) [13]. The placement and diameter of the gold catalyst particles were defined using Electron Beam Lithography (EBL) and lift-off [14]. The Au-seed particles defining the nanowire diameters were 40 or 45 nm with spacing between 0.5 to 1.5 µm, in arrays with 1-200 wires. The growth of the InAs/GaSb nanowires was subsequently performed using metal-organic vapor phase epitaxy (MOVPE). The GaSb source segment was p-doped to 10^{19} cm^{-3} using diethlyzinc (DeZn). The bottom ~1/2 of the total InAs length, was n-doped to a concentration

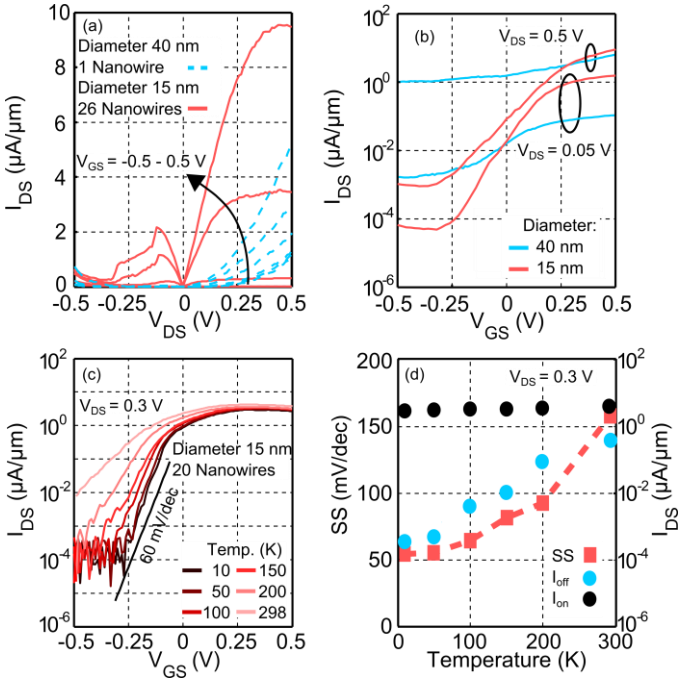

Fig. 2. (a) Output data of the devices with 40 nm and 15 nm InAs diameter, respectively. (b) Transfer data for the same devices as represented in figure a. (c) Temperature dependent transfer data from device with 15-nm-thick InAs. (d The Figure shows the best differential subthreshold swing, I_{off} and I_{on} as a function of temperature. Dots represents I_{off} and I_{on} current at V_{GS} = -0.24 V and V_{GS} = 0.5 V, respectively. Squares, enhanced by a dotted line, represent subthreshold swing values.

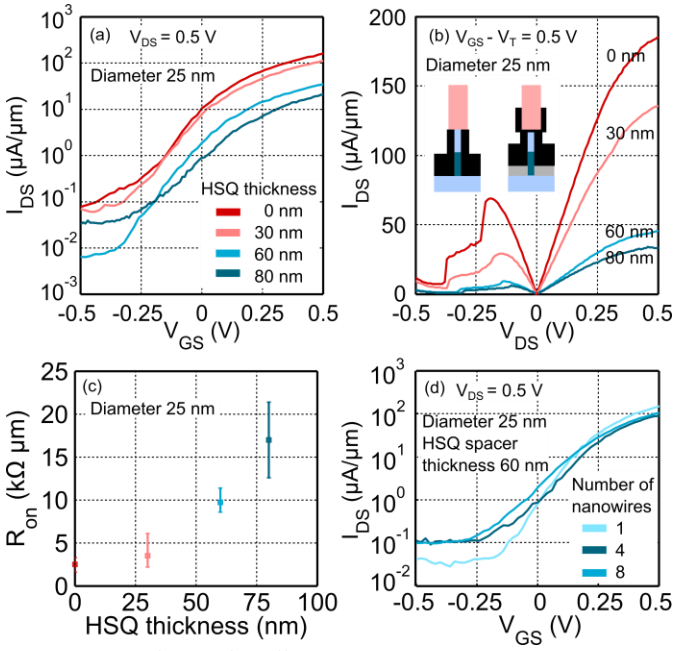

Fig. 3. (a) Transfer data for different HSQ drain spacer thickness. (b) Output data for the same devices as in Figure a. The inset schematically shows the placement of the gate on the devices with different drain spacer. (c) R_{on} as function of the HSQ thickness. (d) Effects of the scaling of the number of the nanowire in the device for a HSQ thickness of 60 nm.

of 10^{18} cm^{-3}, by usage of tetraethyltin (TESn). The channel of the device was not intentionally doped with an estimated background carrier concentration of 10^{17} cm^{-3}. After growth, the nanowire diameter of the InAs was reduced trough a number of digital etching cycles without any noticeable etching of the GaSb resulting in InAs diameters between 11 to 40 nm on different set of samples. Directly after etching, a high-k layer of 1 nm Al_2O_3 and 4 nm HfO_2 was applied using atomic layer deposition (ALD) at temperatures of 300 ºC and 120 ºC, respectively. The estimated EOT for this layer was 1.4 nm. Two methods were applied for formation of gate-drain spacer layer. For thick (100-400 nm) spacer layers, an organic layer was spun on and etched back using O_2 plasma. For controlled fabrication of variable drain spacer (0-80 nm) thickness, a hydrogen silsesquioxane (HSQ) layer was formed using EBL exposure with exact dose control [15]. A 60-nm-thick tungsten (W) film was conformally deposited by reactive sputtering to form the gate electrode. The physical gate-length (L_g) was set by spin on and etchback of an organic film, followed by O_2-plasma ashing, yielding L_g between 200 to 300 nm, as indicated in Fig 1a. UV- lithography was used to define the gate-pads. An organic gate-source spacer was formed using a spin on organic layer followed by etchback. Nickle and gold top-metals were sputtered and pads were defined using UV-lithography followed by wet-etching of the metals. The fabrication results in two types of samples, one with organic drain spacer used to study the effects of nanowire diameter scaling, and one sample with HSQ drain spacer for study of the gate-placement. A schematic image of the final device is shown in Figure 1a. A TFET with an InAs diameter of 11 nm prior to high-k deposition is shown in Figure 1b. The effective gate-length (L_{eff}), is determined from unintentionally-doped (UID) channel thickness, as shown in Figure 1a, with an approximate length of 100 nm to 200 nm for devices with InAs diameter of 11 nm to 40 nm, respectively. Although the fabrication techniques allowed us to manufacture working transistors with InAs diameter of 11 nm, the highest yield and most data presented in this article was obtained from devices with thicker diameters.

III. Effects of Diameter and Gate Placement on the Electrostatics

Figure 2a-c shows the effect of diameter scaling, strongly improving the electrostatics of the devices as the diameter is scaled from 40 down to 15 nm. Both *SS* taken at V_{DS} = 50 mV improves from 243 mV/decade to 100 mV/decade as the diameter is scaled. Further, the drain-induced barrier lowering (DIBL) is greatly improved by the diameter scaling. Both device show similar I_{on}, around 6 - 9 μA/μm, taken at V_{GS} = V_{DS} = 0.5 V. The gate current was two to three orders of magnitude lower than I_{DS} for all devices presented. Figure 2c shows the temperature dependence of the transfer characteristics for the 15 nm diameter device. As shown in the Figure 2d, the minimum *SS* shows different dependence, with a constant *SS* about 50 mV/dec for low temperatures and temperature dependent *SS* for higher temperature for which small activation energy of about 50 meV was extracted above the measurement noise floor at V_{GS} = - 0.24 V. The low activation energy indicates that the off-current is limited by trap-assisted tunneling, and not by back-injection over the valence band edge. The effect of gate placement relative to the

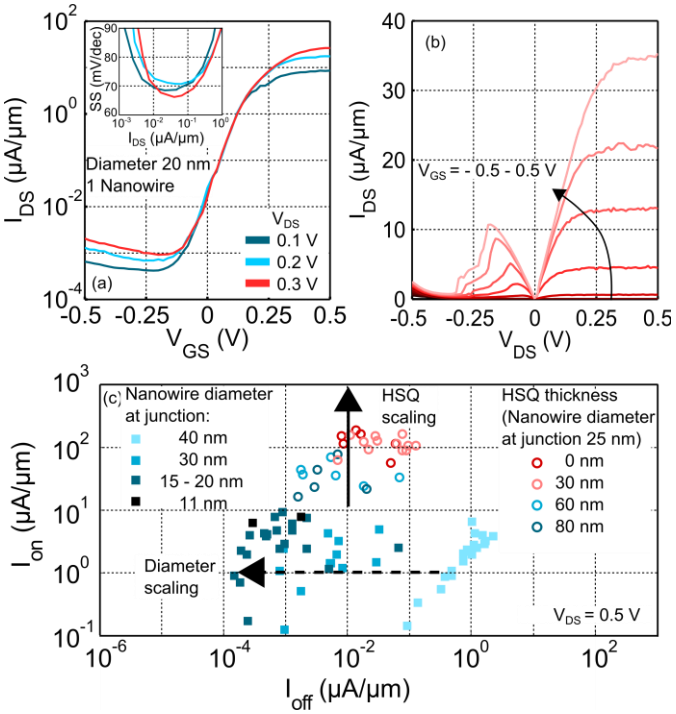

Fig. 4 (a) Transfer data for three different driving voltages, with insignificant DIBL. The HSQ drain spacer thickness for this device is 60 nm and the InAs diameter is 20 nm. The inset shows *SS* for three different drive voltages where the lowest differential *SS* achieved is 68 to 71 mV/dec. (b) Output data for the same device as a). (c) I_{on} and I_{off} current for devices with different InAs diameters and HSQ drain spacer thicknesses. The observed trends of improved electrostatics by general scaling.

channel/source junction, as well as the gate-drain overlap was studied on the sample with different HSQ drain spacers. In Figure 3a and b, the transfer data and output data from four devices with different drain spacer thickness between 0 to 80 nm are compared. I_{on} at V_{DS} = V_{GS} = 0.5 V is increasing from 21 µA/µm to 160 µA/µm, as the thickness was decreased. The peak current in the NDR region was scaling with the spacer thickness, with the largest currents for the devices with thinnest HSQ reaching 1.09 mA/µm^2 and a peak-to-valley ratio of 10 at V_{DS} = 0.5 V. The inset in Figure 3b shows schematically the gate-placement on different devices. Due to the constant L_{eff}, as the gate-drain overlap is decreased, the gate-source overlap increases at a similar rate. In Figure 3c, the effect of the spacer thickness on R_{on} is shown. This trend corresponds well with observations for the output characteristics. R_{on} increases with spacer thickness, indicating an increase mainly in drain access resistance as the gate-drain overlap decreases although the increase of the gate-source overlap on the source side could affect the electrostatics as well. The lowest R_{on} achieved was 1.6 kΩ · µm and 21.4 kΩ · µm for the devices with 0 nm and 80 nm spacer thickness, respectively. The subthreshold swing is decreasing when the spacer thickness is increased from 0 to 60 nm with an average value of 157 mV/dec to 133 mV/dec. In Figure 3d, the transfer data from devices with different numbers of nanowires are presented showing similar performance. In Figure 4a the transfer data is shown for the device with a 60- nm-thick HSQ drain spacer and a 20-nm-diameter InAs-channel, achieving a

TABLE I
BENCHMARKING

Parameter	Best device in this paper	Dewey IEDM 2011 [11]
Minimum point *SS* (V_{DS} = 50 mV)	66	58
Current for lowest *SS* (V_{DS} = 50 mV)	9.2 nA/µm	0.8 nA/µm
On-current (I_{off} = 10 nA/µm, V_{DS} = 0.3 V, V_g-V_{goff}= 0.3 V)	11.28 µA/µm	1.3 µA/µm

minimum differential *SS* of 68 mV/dec at V_{DS} = 0.3 V and 82 mV/dec at V_{DS} = 0.5 V. The improvement in subthreshold swing as compared with organic spacers can in part be explained by omission of O_2 plasma during the processing of the drain spacer. The electrostatics of this device is excellent, which is shown by the insignificant (4.6 mV/V) DIBL and comparable *SS* values for drive voltages of 100 mV to 300 mV, shown in the inset in Figure 4a. The same device is benchmarked, in Table 1, against a TFET with a staggered InGaAs heterostructure demonstrating operation at higher current levels. The output data in Figure 4b shows that the I_{DS} current saturates well achieving currents of 35 µA/µm for V_{GS} = 0.5 V and V_{DS} = 0.5 V. Figure 4c compares I_{on} and I_{off} performance of the devices from different samples. Diameter scaling clearly improves I_{off} while keeping I_{on} fairly constant due to an improved electrostatic control. Scaling down the drain spacer thickness improves the I_{on}. Thus the device geometry to a large degree affects the device performance.

IV. Conclusion

In this paper, we have demonstrated the importance of scaling the diameter and gate-placement in vertical InAs/GaSb TFETs. The fabrication technique used allows us to manufacture devices with the InAs diameter down to 11 nm and to position the gate-metal at an exact distance from the junction. The results show that diameter and gate-placement influences the electrostatics and on-current of the devices. The reduction of the diameter improves the electrostatics and on-current increases with decreasing drain spacer thickness. The lowest subthreshold swing was 68 mV/dec at V_{DS} = 0.3 V and 82 mV/dec at V_{DS} = 0.5 V measured on a device with 60-nm-thick drain spacer and 20 nm InAs-diameter, with the I_{on} of 13 µA/µm for V_{GS} = 0.5 V and V_{DS} = 0.3 V, and 35 µA/µm for V_{GS} = 0.5 V and V_{DS} = 0.5 V.

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