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InAs/(In)GaAsSb/GaSb Nanowire Tunnel Field-Effect Transistors

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Tunnel Field-Effect Transistors with ability to operate well below the thermal limit (with a demonstrated 43 mV/decade at V_{DS} = 0.1 V) are characterized in this work. Based on 88 devices, the impact of the low subthreshold swing on the overall performance is studied. Furthermore, correlation between parameters that are important for device characterization are determined.

I. INTRODUCTION

STEEP-SLOPE devices allow for continued drive voltage scaling needed for future low power applications, such as internet of things. To be competitive with respect to the main existing MOSFET technology, any novel device needs to demonstrate a subthreshold swing (*S*) well below the thermal limit of 60 mV/decade, and show the ability to provide larger currents than what MOSFETs can provide. One promising candidate is the Tunnel Field-Effect Transistor (TFET), which uses quantum mechanical tunneling to filter the injected carriers rather than thermal emission [1,2]. The general development in the field has generated devices that either demonstrate operation well below the thermal limit at low currents [3-5] or operate at useful currents without ability to reach slopes well below the thermal limit [6-11]. Vertical nanowire InAs/InGaAsSb/GaSb TFETs have recently demonstrated promising performance with ability to combine operation below the thermal limit with technically useful currents [12,13]. In this paper, we present an extensive study of TFETs with two different types of heterostructures, both with ability to operate below 60 mV/decade. To fully understand the performance of these devices and to verify that they exhibit the expected TFET behavior, we study parameters such as: on-current (I_{ON}), subthreshold swing, hysteresis, peak-to-valley-current ratio (PVCR), temperature dependence, and I_{60} that is the current at which the subthreshold swing is 60 mV/decade. The knowledge gained from the statistics presented in this study will help to clarify the correlation between important device parameters. Furthermore, we will gain more insight into when off-state performance is of importance and when other metrics also need to be considered to achieve best possible performance.

II. Device Fabrication

InAs/InxGa$_{1\text{-}x}$As$_y$Sb$_{1\text{-}y}$/GaSb nanowires with InGaAsSb composition x/y=0.1/0.88 in Sample A and x/y=0.32/0.72 in Sample B were grown using the metal-organic vapor phase epitaxy exploiting the vapor-liquid-solid growth method. Both InAs/InGaAsSb heterojunctions exhibit a graded profile. [12] The nanowires where grown on an n+-InAs layer (260 nm) integrated on a highly resistive Si (111) substrate (ρ>12 kΩ-cm) [14]. Prior to growth, Au-seed particles were defined in arrays with 1-8 nanowires using Electron Beam Lithography (EBL) and PMMA based lift-off. The diameter of and spacing between the Au-seed particles was set to 40 nm and 1.5 μm, respectively. The growth of the nanowires was subsequently performed using metal-organic-vapor-phase epitaxy (MOVPE). The InGaAsSb/GaSb source segment was p-doped estimated to 10^{19} cm^{-3} using diethlyzinc (DeZn). The channel section at the top half of the InAs segment, was not intentionally doped with an estimated background carrier concentration of 10^{17} cm^{-3}. The bottom half of the InAs was n-doped to a concentration of 10^{19} cm^{-3}, by tetraethyltin (TESn).

After growth, the diameter of InAs was reduced to 20 nm through several cycles of digital etching using ozone to oxidize the surface and citric acid to remove the oxide. The thickness of the InGaAsSb segments was also reduced to 25 nm, while there was no noticeable etching of the GaSb. Directly after etching, a 1 nm Al_2O_3/ 4nm HfO_2 high-κ bilayer was applied using atomic layer deposition (ALD) at temperatures of 300 °C and 120 °C, respectively. These deposition conditions were chosen to provide a low D_{it} around the conduction band edge of InAs [15]. The estimated EOT for this layer was 1.4 nm. A 15- nm-thick SiO_x bottom spacer, which separates the drain and gate layers, was deposited using thermal evaporation. During the evaporation, some of the SiO_x was deposited on the sidewall of the GaSb-segment forming SiO_x - flakes. The sample was etched in diluted HF to remove the flakes, followed by applying 12 extra cycles of HfO_2, to compensate for the etching. A 60- nm-thick tungsten film was sputtered on the sample to form the gate-layer. In subsequent steps, the gate-length was set by spin coating the sample with an organic resist and etching the resist back to wanted thickness with reactive ion etching (RIE). It was followed by removal of the exposed Tungsten (W) using SF_6/Ar plasma with RIE. The gate-pad was defined using UV-lithography and RIE. The top-spacer, which separates gate and source layer, was fabricated using an organic spacer (S1800), which was applied using spin coating. The thickness of the top- spacer was determined using etchback with RIE. Using UV- lithography and RIE the via-holes were defined. Prior to applying the top-metal, the high-κ was removed from the exposed surfaces with HF, followed by sputtering of 10 nm Ni and 150 nm Au. The probe-pads were defined using UV- lithography and wet-etching. Final devices have a physical gate length (*L*g) of 250-300 nm with an overlap of 50-100 nm. The effective channel length is ~ 100 nm which corresponds to the undoped InAs segment. Lengths of different segments is shown in Figure 1a, and the final transistor can be viewed in Figure 1b and Figure 1c.

III. Characterization of the Devices

All currents presented in this article are normalized to the InAs circumference and the number of nanowires. The magnitude of the gate-current is at least two orders lower than the minimum channel current. I_{ON} is defined as the current at $V_{G,\mathrm{ON}}$ which is $V_{\mathrm{G,ON}} = V_{\mathrm{DS}} + V_{\mathrm{G,OFF}}$ where I_{OFF} =1 nA/µm. As illustrated in Figure 1d, the devices operate below 60 mV/decade in a certain current range, with two points ($I_{\mathrm{60,Low}}$ and $I_{\mathrm{60,High}}$) at which the current is 60 mV/decade. In the following text I_{60} is equivalent to $I_{\mathrm{60,High}}$.

Electrical data from a representative device from Sample A and Sample B is presented in Table 1. Both devices show similar subthreshold swing of 48 mV/decade at V_{DS} = 0.3 V. The device from Sample B exhibits a smaller hysteresis (2 mV) and a larger PVCR (16.7), although the difference is not very large. Yet, the device from Sample A reaches 2-3 times higher I_{60}. The device from Sample B does reach a higher I_{ON} at V_{DS} =

0.1 V, most likely because of its slightly lower S_{MIN} at this drive voltage. However, when the drive voltage is increased, the device from Sample A achieves higher currents, due to lower R_{ON} and higher I_{60} and g_{m}. Generally, the devices from Sample B exhibit larger source depletion which could partly come from a different doping incorporation due to different composition and slightly larger overlap of the gate-metal on the source side for the devices on the Sample B. The gated region on the source side will deplete holes during operation and thereby access resistance will increase, impacting some of the parameters of the device. Devices on Sample B shows reduced g_{m}, I_{ON}, and I_{60}. Furthermore, an increased R_{ON} is also observed, all these changes correspond well with effects of source depletion.

Output data for the devices in Table I is presented in Figures 2a and b, both showing good saturation with clearly visible negative differential resistance (NDR). The output data of the device from Sample A show no superlinear on-set behavior and achieves on-currents two times higher for the same overdrive voltage compared to the device from Sample B. Transfer data of the device from Sample A (Presented in Table I) can be viewed in Figure 2c. The gate current is two orders of magnitude lower than the lowest current in the channel and the gate current doesn't exhibit any dependence on gate or drive voltage. Figure 2d, shows transfer data from device on Sample B (presented also in Table I). Data demonstrates the good electrostatics and the impact of source depletion is manifested as a NDR, where increasing drive voltage moves the peak to higher VGS due to a larger number of holes that needs to be depleted. Insert shows the temperature behavior for these two devices. The both devices exhibit the same trend, where the subthreshold swing decreases with temperature in the temperature range between 220 and

323 K, indicating an, in part, thermally activated off-state current. However, the subthreshold swing is below 60 mV/decade even at 323 K, for both devices.

IV. Statistics

Devices from both samples, 12 from Sample A and 76 from Sample B, were used to study the variations and dependences between the device parameters such as S_{MIN}, I_{60}, I_{ON}, hysteresis, PVCR, and the number of nanowires in the device. Table II shows the correlation (coefficient) between some of the parameters shown in the following section. Using least square fitting of a line with bisquare weights the correlation coefficient ($r = 0$ weak correlation and $r = 1$ strong correlation) is determined.

In Figure 3a, transfer curves from 10 devices on Sample B are plotted. Devices are from different locations on the sample, with varying number of nanowires from 1-8. The majority of the devices exhibit a Vt shift of less than 0.2 V. Figure 3b, where the curves from Figure 3a are shifted to remove the effect of the V_t shift, shows that there is a variation in minimum off-state leakage, as well as maximum on-state current. The variation of the I_{ON} comes mainly due to the source depletion. Figure 3c shows how the measurement to obtain hysteresis was performed. The voltage was swept from low to high voltages (Sweep up) and then back (Sweep down) without any delay, with $V_{\mathrm{DS}} = 0.05$ V and $-0.1<V_{\mathrm{GS}}<0.5$. The hysteresis was then determined at the current level when the subthreshold swing is at its lowest value for the sweep up. Results from these measurements is presented in Figure 3d. The majority of the devices exhibit a hysteresis lower than 20 mV. For hysteresis over 15 mV, there is a correlation between increasing S and hysteresis. Devices with large hysteresis exhibit a larger number of defects in the high-κ. During the Sweep up and Sweep down these defects will act as charge traps for the carrier in the channel. This process will influence the subthreshold swing and hysteresis. [12] The difference in S_{MIN} with regard to Up/Down sweep is in average 2 mV, but can be as large as 13.6 mV.

In Figure 4a and 4b, the dependence of the subthreshold swing on the number of nanowires within the TFET is plotted. For both drive voltages, the data shows the same trend of increasing values of the lowest achievable S_{MIN} as the number of nanowires is increased. In Figure 4c the dependence of the subthreshold swing on the number of nanowires and used drive voltage is shown. For $V_{\mathrm{DS}} = 0.1$ V, 60-80 % of the devices operate below 60 mV/decade independently of nanowire numbers. When the drive voltage is increased, the number of devices working below 60 mV/decade is reduced as the number of the nanowires in the device is increasing. Devices with larger number of nanowires exhibit larger off current, which increase as the drive voltage is increased and influence the subthreshold swing. In Figure 4d, the relation between I_{ON} and S_{MIN} is shown. As expected I_{ON} current increases with decreasing S_{MIN} at $V_{\mathrm{DS}} = 0.1$ V, however this dependence is weaker for $V_{\mathrm{DS}} = 0.3$ V due to scattering in the on-state performance. Figure 4e shows the relation between gm and I_{ON}, for $V_{\mathrm{DS}} = 0.1$ V where the currents is in subthreshold region there is no dependence on g_{m}. For the on-current at $V_{\mathrm{DS}} = 0.3$ V the dependence of I_{ON} on g_{m} is noticeable. This behavior is clarified in Figure 4f; at the lower drive voltage such as 0.1 V, I_{ON} current is in proximity of I_{60}, thereby devices with lower S_{MIN} will benefit from switching with steeper slope. As the drive voltage is increased to 0.3 V, other factors primarily associated with the on-state, such as g_{m} and R_{ON}, starts to influence the final I_{ON} value. This can be observed if data from Sample A and Sample B are compared. At low drive voltage, data from these devices is comparable, however at higher drive voltage the data from Sample A generally results in higher I_{ON} due to lower R_{ON} and larger g_{m}.

In Figure 5 a and b, the dependence of I_{60}, at V_{DS} of 0.1 V and 0.3 V, on number of nanowires used in TFETs is shown. Devices with single nanowires exhibit the largest I_{60} as well as the largest variation. As the nanowire number increases the maximum value of I_{60} is reduced and at the same time the variation diminishes due to averaging effect. I_{ON} exhibit a similar behavior, as the number of the nanowires increases, Figure 5c. The correlation between the I_{60} and I_{ON} is shown in Figure 5d, data for drive voltage 0.1 V shows that as the I_{60} increases also the I_{ON} increases. However, this correlation is weaker for drive voltage 0.3 V, partly due to depletion. This observation is coherent with the observation in Figure 4d and 4e. For $V_{\mathrm{DS}} = 0.1$ V, the switching from I_{OFF} to I_{ON} occurs mainly in the sub-60 region and thereby a higher I_{60} will result in higher I_{ON} (Figure 4d). At $V_{\mathrm{DS}} = 0.3$ V, where $I_{\mathrm{ON}}>I_{60}$, benefit from increasing I_{60} is less visible and final value of I_{ON} will depend also on other factors such as R_{ON} and g_{m} (Figure 4e).

The smallest measured subthreshold swing is found for a device from Sample B, with a minimum subthreshold swing of 43 mV/decade at $V_{\mathrm{DS}} = 0.1$V, as shown in in Figure 6a. In Figure 6b, I_{D} vs S_{MIN} is plotted for three devices from Sample B. As expected, when the S_{MIN} is increasing the range in which the device operates below 60 mV/decade is also decreasing. There is a correlation between the $I_{60,\mathrm{Low}}$ and S, where increasing $I_{60,\mathrm{Low}}$ increases the S_{MIN}, Figure 6c. However, there is no strong correlation between the measured $I_{60,\mathrm{High}}$ and the subthreshold swing for our devices, Figure 6d. $I_{60,\mathrm{High}}$ is mainly set by the transmission of the tunnel junction, whereas $I_{60,\mathrm{Low}}$ is influenced by ambipolarity and defect-assisted tunneling. At low currents contribution from DAT will be a substantial part of the total current and thus will impact $I_{60,\mathrm{Low}}$ by increasing that value. Figure 6e and f, show how the magnitude of the range in which devices operate below 60 mV/decade changes with S_{MIN} at V_{DS} of 0.1 V and 0.3 V.

In Figure 7, the peak-to-valley-current-ratio, a value usually used to determine the quality of the semiconductor heterojunction in tunnel diodes, is shown. In Figure 7a, the PVCR is presented against the number of nanowires. The highest achievable value for PVCR is decreasing with increasing number of nanowires, which we attribute to averaging among the nanowires. However, devices with 8 nanowires can still achieve large values of PVCR (~15). In Figure 7b, the I_{ON} is plotted against PVCR for two different drive voltages. We note that an increase of PVCR from 5 to 20 result in a moderate increase of I_{ON} for either drive voltages. In Figure 7c the dependence between the S_{MIN} and PVCR is examined. The general trend is that an increasing PVCR results in a lower S_{MIN}, the spread is large between the smallest and largest values. Notably, devices with PVCR of >5 can operate well below 60 mV/decade and even a device with PVCR of 10- 15 can be at or above 60 mV/decade. However, higher PVCR (>10) will improve the probability that the device operates below 60 mV/decade.

V. Conclusions

We have demonstrated devices with two different InGaAsSb compositions, which can operate well below 60 mV/decade. Some of the devices show ability to reach a subthreshold swing of 43 mV/decade at V_{DS} = 0.1 V. Devices on Sample A can reach higher g_m and I_{ON} due to lower source depletion. The best devices reaches a g_m of 130 µS/µm and 205 µS/µm at V_{DS} = 0.3 V and 0.5 V, respectively. Using a large number of devices, the dependence of important parameters such as I_{60}, S_{MIN}, I_{ON}, hysteresis, and PVCR have been studied. Above I_{60} the on- current is influenced by g_m and R_{ON}. The peak-to-valley-current ratio influences I_{ON} and S_{MIN}, increasing PVCR value will improve the probability that the device operate below 60 mV/decade I60 current needs to be as high as possible, and the range in which the S_{MIN} is below 60 mV/decade need to be as large as possible.

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Figure Captions

Figure 1. (a) Schematic nanowire illustration, where different sections are marked. (b) Schematic of the final device with different layers. Total number of the EBL and lithography steeps that are used in fabrication of the transistors are one and five, respectively. (c) Cross section of one transistor: drain, gate, and source region. The gate metal, InAs segment, and InGaAsSb/GaSb segment are colored. Width of the scale bar is 50 nm. (d) Schematic of S versus I_D, showing definition of S_{MIN}, $I_{60,Low}$, and $I_{60,High}$.

Figure. 2. (a) and (b) Output data of one device from Sample A and Sample B. These devices are benchmarked in Table I. (c) Transfer data of the device benchmarked in Table I from Sample A. Gate current for drive voltages 0.05 and 0.5 V, which is two orders of magnitude lower than the lowest current in the channel. (d) Transfer data of the device benchmarked in Table I from Sample B. The inset shows dependence of the subthreshold swing on temperature for the devices in (a) and (b). Solid black line is kT-line.

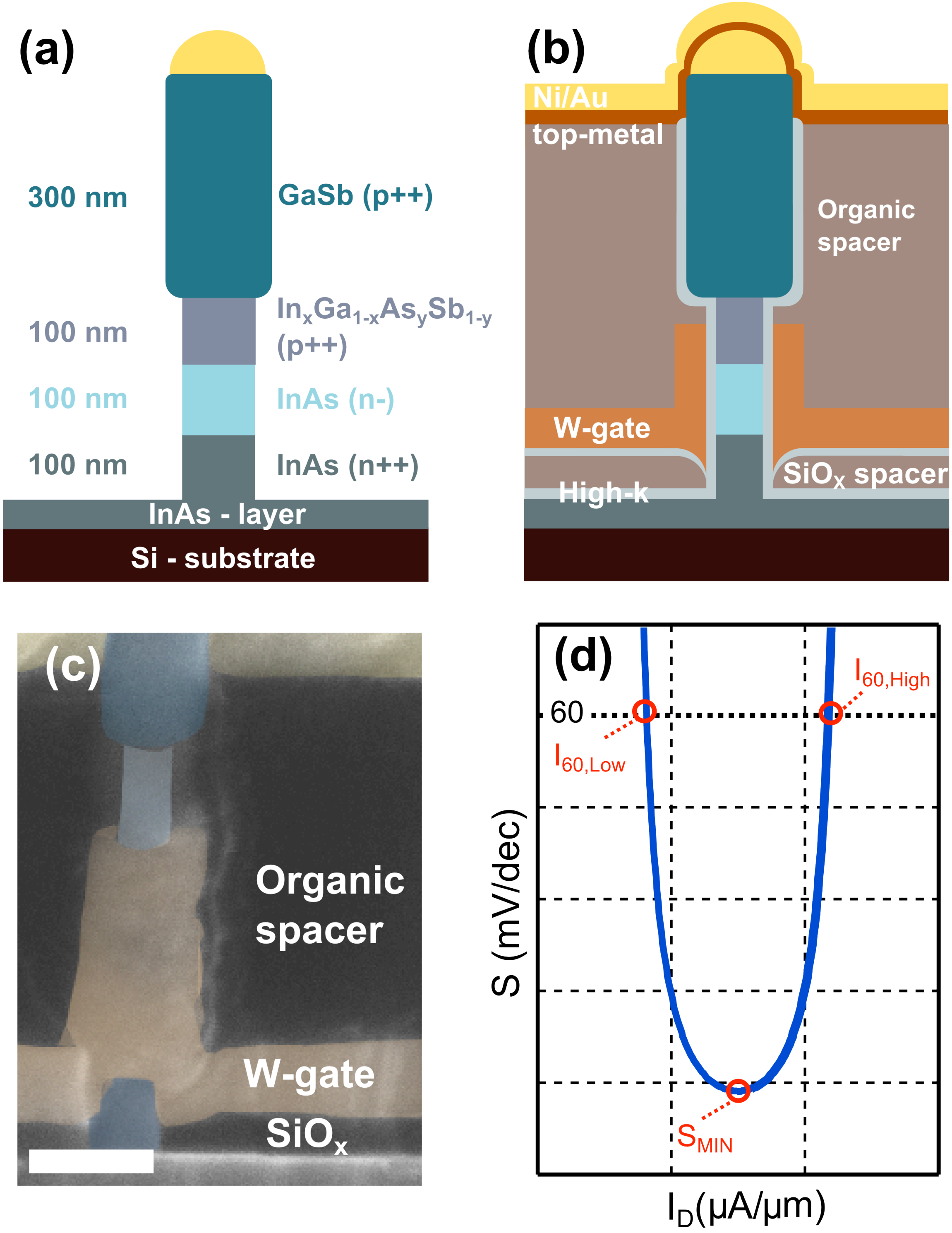
Figure 3. (a) Transfer curves from ten devices from Sample B. Notice that the number (n) of the nanowires in the devices can vary from 1–8, where the measured current is divided by $\pi \cdot d_{nanowire} \cdot n$. (b) Transfer curves from ten devices from Sample B. Notice that the number (n)of the nanowires in the devices can vary from 1–8, where the measured current is divided by $\pi \cdot d_{nanowire} \cdot n$, although the curves are shifted to remove the effect of Vt shift. (c) Illustration of how hysteresis presented in (d) was acquired. Data is obtained by sweeping V_{GS} from −0.1 to 0.5 V (sweep up) and back (sweep down) with slew rate of 0.035 V/s. A line was fit to the measured curves at current level that corresponds to S_{MIN} for the sweep up. Voltage difference between the lines is hysteresis. (d) Relation between the hysteresis and subthreshold swing. Data in this graph come from devices with one or two nanowires, all devices are from Sample B.

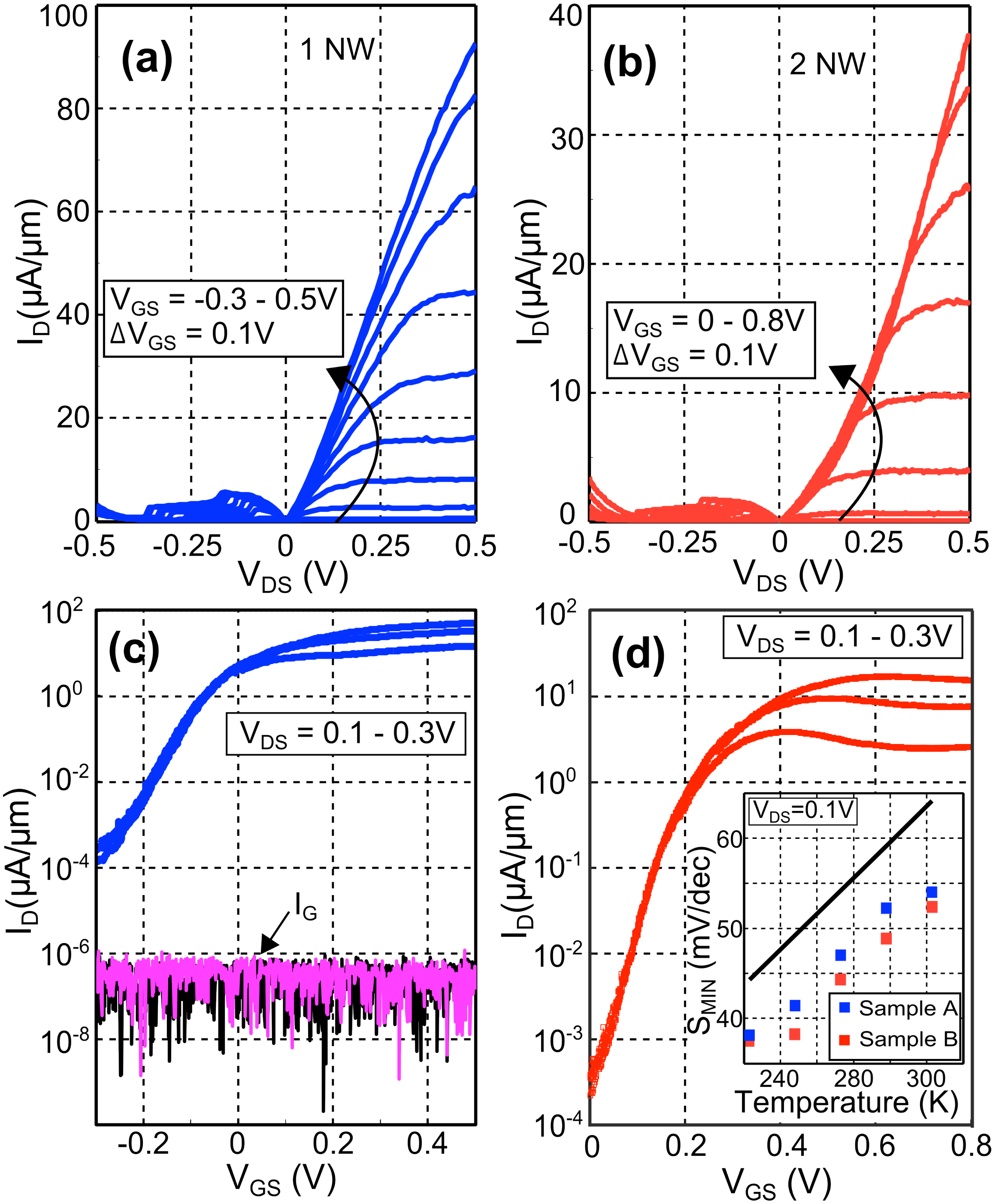
Figure 4. (a) and (b) S_{MIN} versus nanowire numbers for drive voltage 0.1 and 0.3 V, respectively. (c) Statistical overview over devices operating below 60 mV/decade. Data were organized in groups sorted by nanowire numbers, it was then calculated how many of the devices in every group operates below 60 mV/decade for every drive voltage. Number in parentheses shows how many devices are there in every group. (d) S_{MIN} versus I_{ON} for drive voltages 0.1 and 0.3 V, respectively. (e) g_m versus I_{ON} for drive voltages 0.1 and 0.3 V, respectively. (f) Transfer data (V_{DS} = 0.3 V) for the device from Sample A presented in Table 1. For V_{DS} = 0.1 V, the ON-current is below the I_{60} benefiting from the sub-60 slope. For V_{DS} = 0.3 V, the final ON-current is limited by additional factors such as R_{ON} and g_m.

Figure 5. (a) and (b) I_{60} versus number of nanowires at drive voltages 0.1 and 0.3 V, respectively. (c) I_{ON} versus nanowire number for drive voltage 0.1 and 0.3 V. Used I_{OFF} is 1 nA/µm. (d) I_{ON} versus I_{60} for drive voltage 0.1 and 0.3 V.

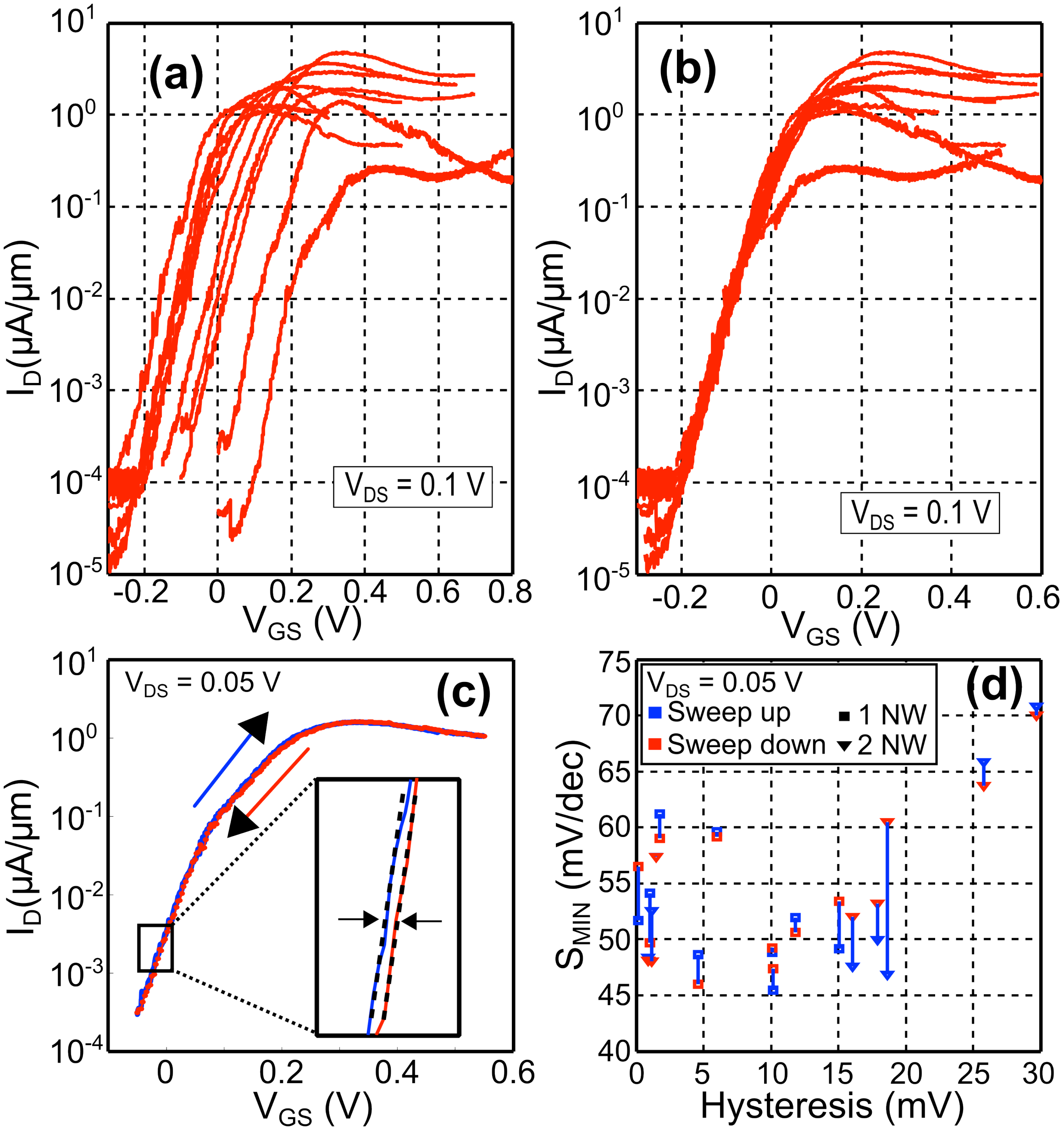
Figure 6. (a) Data from a device from Sample B with a S_{MIN} of 43 mV/decade at V_{DS} = 0.1 V. (b) S versus I_D drive voltage 0.3 V for three different devices from Sample B. (c) S_{MIN} versus $I_{60,Low}$ for drive voltage 0.3 V. (d) S_{MIN} versus $I_{60,High}$ for drive voltage 0.3 V. (e) and (f) S_{MIN} versus ratio of $I_{60,High}/I_{60,Low}$ for drive voltage 0.1 and 0.3 V, respectively.

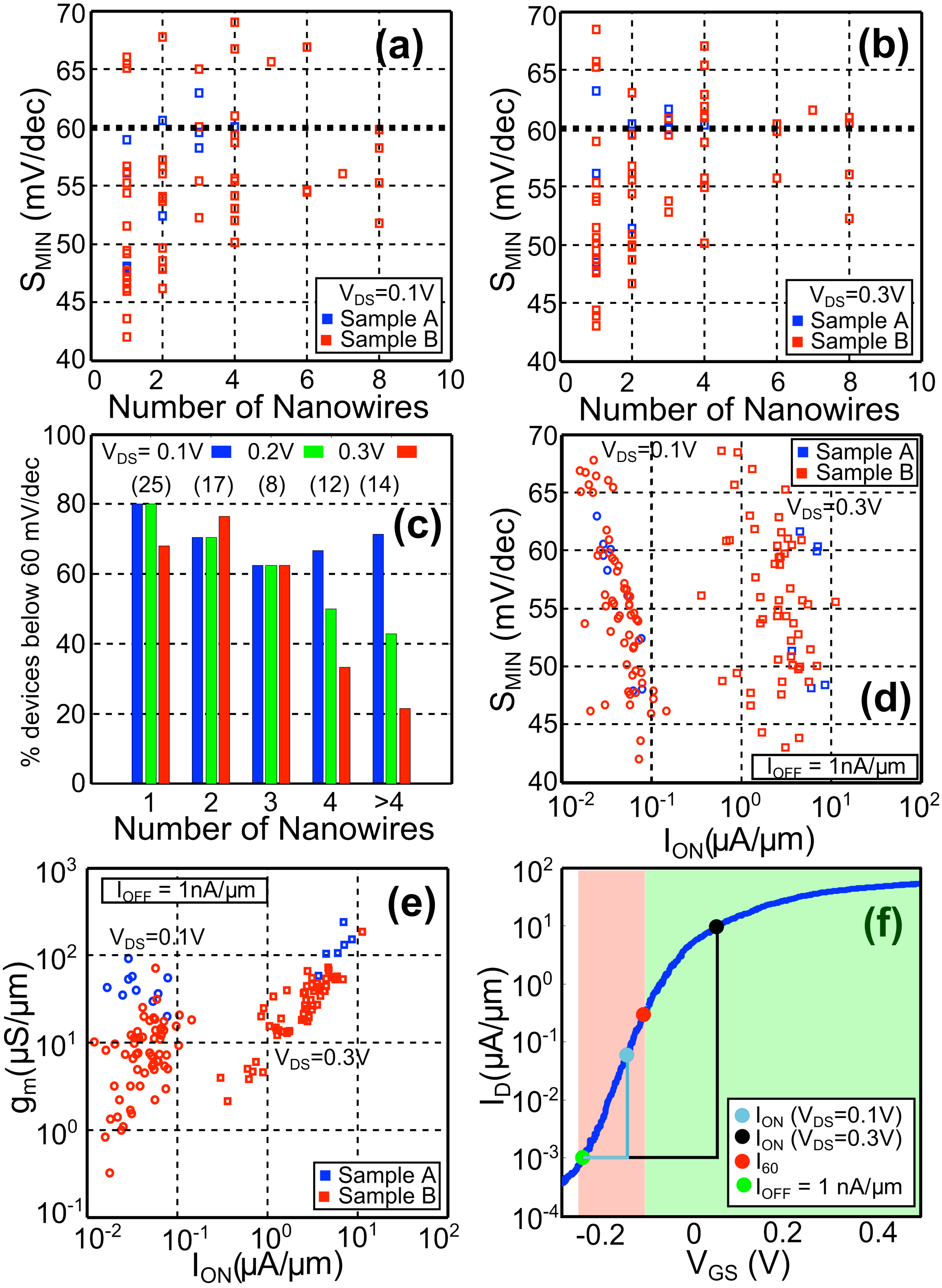
Figure 7. (a) PVCR versus number of nanowires. (b) I_{ON} at 0.1 and 0.3 V versus PVCR. (c) S_{MIN} versus PVCR, used S_{MIN} is for drive voltage of 0.1 V.

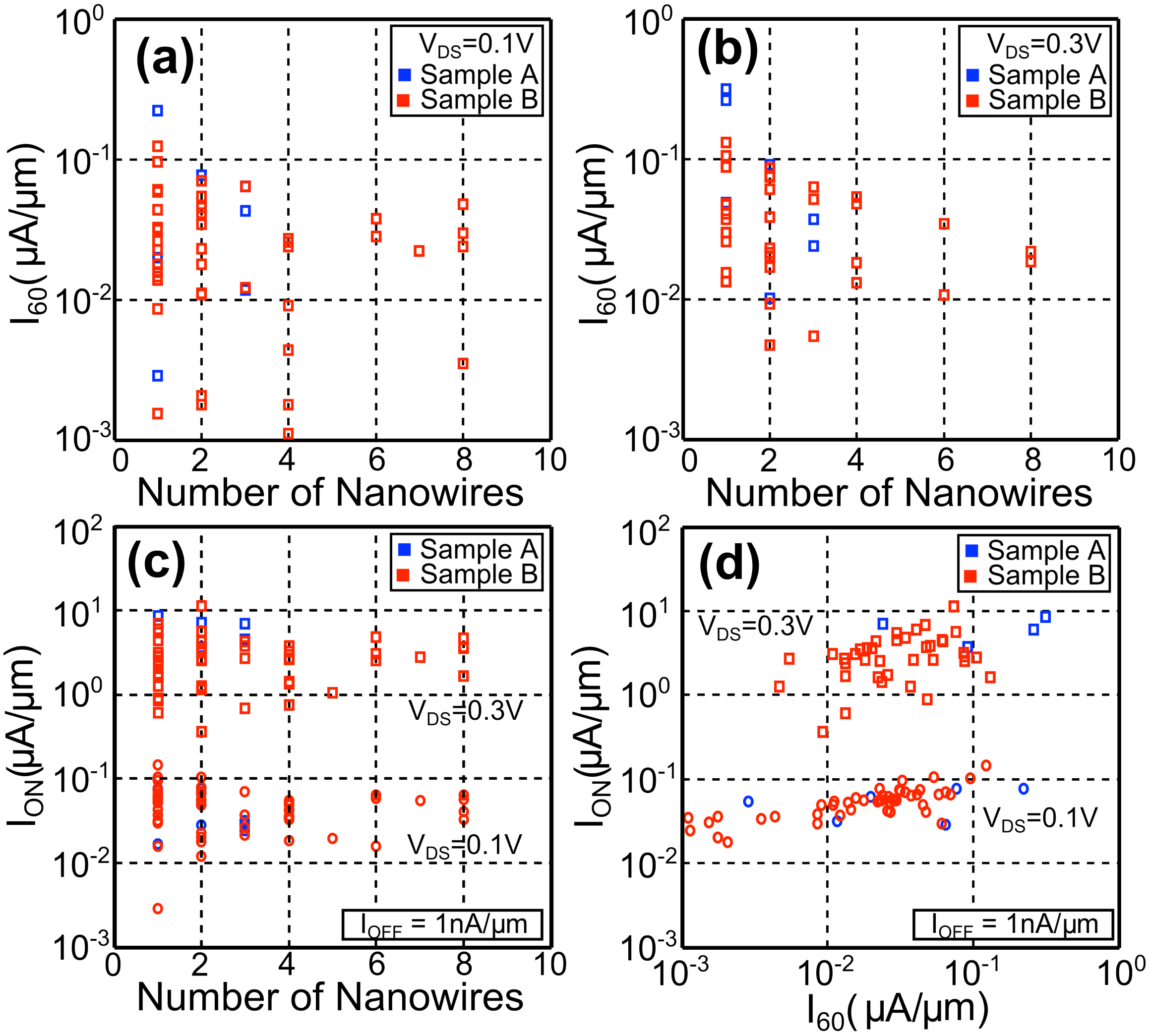

(a)
300 nm
GaSb (p++)
100 nm
$In_xGa_{1-x}As_ySb_{1-y}$ (p++)
100 nm
InAs (n-)
100 nm
InAs (n++)
InAs - layer
Si - substrate
(b)
Ni/Au
top-metal
Organic spacer
W-gate
High-k
SiO_x spacer
(c)
Organic spacer
W-gate
SiO_x
(d)
60
$I_{60,Low}$
$I_{60,High}$
S_{MIN}
S (mV/dec)
I_D(μA/μm)

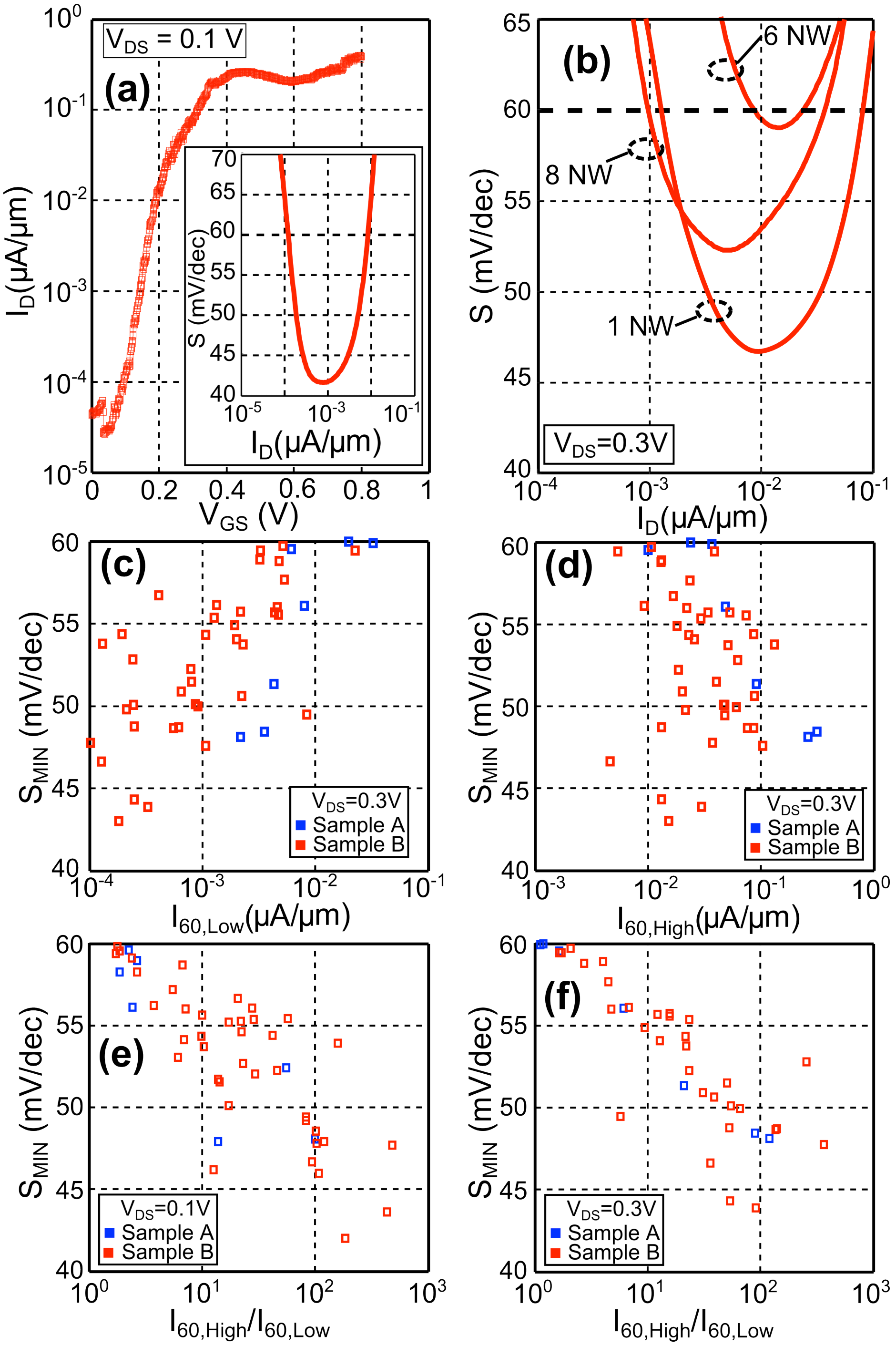


(a)
1 NW
V_{GS} = -0.3 - 0.5V
ΔV_{GS} = 0.1V
100
80
60
40
20
0
I_D(μA/μm)
-0.5
-0.25
0
0.25
0.5
V_{DS} (V)
(b)
2 NW
V_{GS} = 0 - 0.8V
ΔV_{GS} = 0.1V
40
30
20
10
0
I_D(μA/μm)
-0.5
-0.25
0
0.25
0.5
V_{DS} (V)
(c)
V_{DS} = 0.1 - 0.3V
I_G
10^2
10^0
10^{-2}
10^{-4}
10^{-6}
10^{-8}
I_D(μA/μm)
-0.2
0
0.2
0.4
V_{GS} (V)
(d)
V_{DS} = 0.1 - 0.3V
10^2
10^1
10^0
10^{-1}
10^{-2}
10^{-3}
10^{-4}
I_D(μA/μm)
0
0.2
0.4
0.6
0.8
V_{GS} (V)
V_{DS}=0.1V
60
50
40
S_{MIN} (mV/dec)
240
280
300
Temperature (K)
Sample A
Sample B

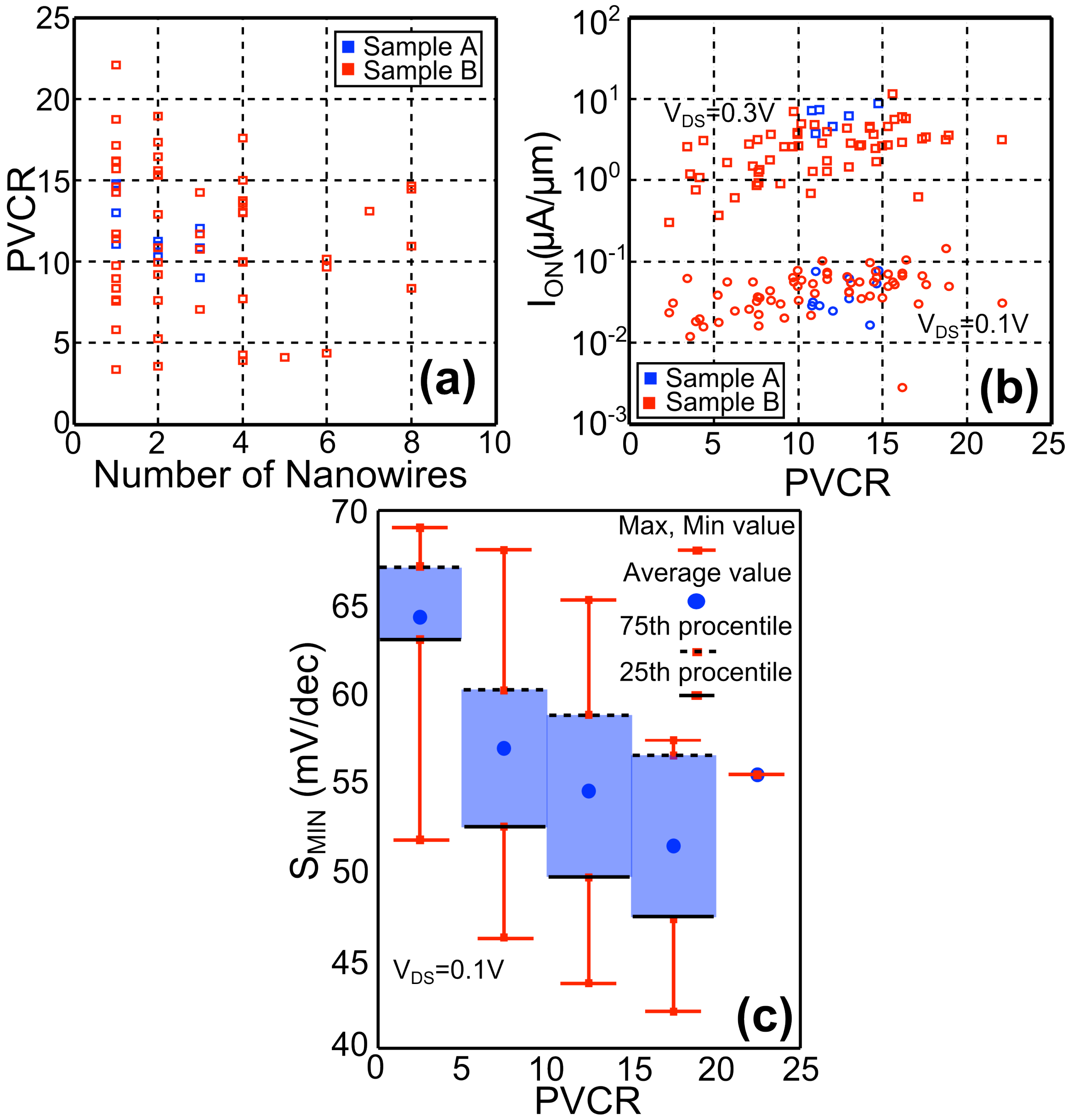

(a)
(b)
(c)
(d)
I_D(µA/µm)
V_{GS} (V)
V_{DS} = 0.1 V
V_{DS} = 0.1 V
V_{DS} = 0.05 V
V_{DS} = 0.05 V
10^1
10^0
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
-0.2
0
0.2
0.4
0.6
0.8
S_{MIN} (mV/dec)
Hysteresis (mV)
Sweep up
Sweep down
1 NW
2 NW
75
70
65
60
55
50
45
40
0
5
10
15
20
25
30


(a)
S_{MIN} (mV/dec)
Number of Nanowires
V_{DS}=0.1V
Sample A
Sample B
(b)
S_{MIN} (mV/dec)
Number of Nanowires
V_{DS}=0.3V
Sample A
Sample B
(c)
% devices below 60 mV/dec
V_{DS}= 0.1V 0.2V 0.3V
(25) (17) (8) (12) (14)
1 2 3 4 >4
Number of Nanowires
(d)
S_{MIN} (mV/dec)
V_{DS}=0.1V
V_{DS}=0.3V
Sample A
Sample B
I_{OFF} = 1nA/µm
I_{ON}(µA/µm)
(e)
g_m(µS/µm)
I_{OFF} = 1nA/µm
V_{DS}=0.1V
V_{DS}=0.3V
Sample A
Sample B
I_{ON}(µA/µm)
(f)
I_D(µA/µm)
V_{GS} (V)
I_{ON} (V_{DS}=0.1V)
I_{ON} (V_{DS}=0.3V)
I_{60}
I_{OFF} = 1 nA/µm


(a)
V_{DS}=0.1V
■ Sample A
■ Sample B
I_{60}(μA/μm)
10^{0}
10^{-1}
10^{-2}
10^{-3}
0
2
4
6
8
10
Number of Nanowires
(b)
V_{DS}=0.3V
■ Sample A
■ Sample B
I_{60}(μA/μm)
10^{0}
10^{-1}
10^{-2}
10^{-3}
0
2
4
6
8
10
Number of Nanowires
(c)
■ Sample A
■ Sample B
V_{DS}=0.3V
V_{DS}=0.1V
I_{OFF} = 1nA/μm
I_{ON}(μA/μm)
10^{2}
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{-3}
0
2
4
6
8
10
Number of Nanowires
(d)
■ Sample A
■ Sample B
V_{DS}=0.3V
V_{DS}=0.1V
I_{OFF} = 1nA/μm
I_{ON}(μA/μm)
10^{2}
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-3}
10^{-2}
10^{-1}
10^{0}
I_{60}(μA/μm)



(a)
V_{DS} = 0.1 V
I_D(μA/μm)
V_{GS} (V)
10^0
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
0
0.2
0.4
0.6
0.8
1
S (mV/dec)
70
65
60
55
50
45
40
10^{-5}
10^{-3}
10^{-1}
I_D(μA/μm)
(b)
6 NW
8 NW
1 NW
V_{DS}=0.3V
S (mV/dec)
65
60
55
50
45
40
10^{-4}
10^{-3}
10^{-2}
10^{-1}
I_D(μA/μm)
(c)
S_{MIN} (mV/dec)
60
55
50
45
40
V_{DS}=0.3V
🟦 Sample A
🟥 Sample B
10^{-4}
10^{-3}
10^{-2}
10^{-1}
$I_{60,Low}$(μA/μm)
(d)
S_{MIN} (mV/dec)
60
55
50
45
40
V_{DS}=0.3V
🟦 Sample A
🟥 Sample B
10^{-3}
10^{-2}
10^{-1}
10^0
$I_{60,High}$(μA/μm)
(e)
S_{MIN} (mV/dec)
60
55
50
45
40
V_{DS}=0.1V
🟦 Sample A
🟥 Sample B
10^0
10^1
10^2
10^3
$I_{60,High}/I_{60,Low}$
(f)
S_{MIN} (mV/dec)
60
55
50
45
40
V_{DS}=0.3V
🟦 Sample A
🟥 Sample B
10^0
10^1
10^2
10^3
$I_{60,High}/I_{60,Low}$


PVCR
Number of Nanowires
0
2
4
6
8
10
5
15
20
25
Sample A
Sample B
(a)
I_{ON}(μA/μm)
10^{2}
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{-3}
V_{DS}=0.3V
V_{DS}=0.1V
Sample A
Sample B
(b)
PVCR
S_{MIN} (mV/dec)
70
65
60
55
50
45
40
Max, Min value
Average value
75th procentile
25th procentile
V_{DS}=0.1V
(c)
PVCR