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Vertical InAs/GaAsSb/GaSb tunneling field-effect transistor on Si with $S = 48$ mV/decade and $I_{on} = 10 \mu A/\mu m$ for $I_{off} = 1 nA/\mu m$ at $V_{DS} = 0.3 V$

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Vertical InAs/GaAsSb/GaSb Tunneling Field-Effect Transistor on Si with $S = 48$ mV/decade and $I_{\text{on}} = 10$ $\mu\text{A}/\mu\text{m}$ for $I_{\text{off}} = 1$ nA/ μm at $V_{\text{DS}} = 0.3$ V

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Abstract— We present a vertical nanowire InAs/GaAsSb/GaSb TFET with a highly scaled InAs diameter (20 nm). The device exhibits a minimum subthreshold swing of 48 mV/dec. for $V_{\text{DS}} = 0.1 - 0.5$ V and achieves an $I_{\text{on}} = 10.6$ $\mu\text{A}/\mu\text{m}$ for $I_{\text{off}} = 1$ nA/ μm at $V_{\text{DS}} = 0.3$ V. The lowest subthreshold swing achieved is 44 mV/dec. at $V_{\text{DS}} = 0.05$ V. Furthermore, a benchmarking is performed against state-of-the-art TFETs and MOSFETs demonstrating a record high I_{60} and performance benefits for V_{DS} between 0.1 and 0.3 V.

I. INTRODUCTION

MOSFET scaling has for several decades been the main path to increase the performance of Si CMOS technology. As a result, the transistor density in the circuits has steadily increased. Since the subthreshold swing (S) for a thermionic device does not scale below 60 mV/dec., this has resulted in increased power density, which has become the main limitation. To achieve voltage scaling without off-current increase, there is a need for devices with a subthreshold swing lower than 60 mV/dec.. These are so called steep slope devices, of which the Tunneling Field-Effect Transistor (TFET) is the most promising candidate [1-2]. The TFET operation rely on tunneling-based energy filtering that prevents electrons with high thermal energy to enter the channel thereby enabling sub-60 mV/dec. subthreshold swing. So far, few reports exist of TFETs with S below 60 mV/dec. usually with current levels far below any useful operation range [3-8]. We here present a vertical nanowire InAs/GaAsSb/GaSb heterojunction TFET integrated on a Si substrate with $S_{\text{min}} = 48$ mV/dec. with $I_{60} = 0.31$ $\mu\text{A}/\mu\text{m}$ at $V_{\text{DS}} = 0.3$ V and $I_{\text{DS}} = 10.6$ $\mu\text{A}/\mu\text{m}$ for $I_{\text{off}} = 1$ nA/ μm at $V_{\text{DS}} = 0.3$ V.

II. DEVICE FABRICATIONS

To define the nanowire position and diameters, arrays of Au discs with a thickness of 15 nm and diameters of 40 nm were patterned by EBL on substrates with 260 nm highly doped InAs on high resistivity Si(111) [9-10]. The number of discs in the arrays was varied from 1 to 8 and the spacing between the discs was 1.5 μm . InAs/GaAsSb/GaSb nanowires were grown using metalorganic vapor phase epitaxy (MOVPE). 200-nm-long InAs segments were grown at 460°C using trimethylindium (TMIn) and arsine (AsH_3) with a molar fraction of $X_{\text{TMIn}} = 6.1 \cdot 10^{-6}$ and $X_{\text{AsH}_3} = 1.3 \cdot 10^{-4}$, respectively. The bottom part of the InAs segments was n-doped by triethyltin (TESn) ($X_{\text{TESn}} = 6.3 \cdot 10^{-6}$). 100 nm GaAsSb

segments were subsequently grown using trimethylgallium (TMGa) ($X_{\text{TMGa}} = 4.9 \cdot 10^{-5}$), trimethylantimony (TMSb) ($X_{\text{TMSb}} = 1.2 \cdot 10^{-4}$) and AsH_3 ($X_{\text{AsH}_3} = 2.7 \cdot 10^{-5}$) corresponding to a gas phase composition of $\text{AsH}_3/(\text{AsH}_3 + \text{TMSb}) = 0.18$. This was followed by a 300-nm-long GaSb segment grown at 515°C using (TMGa) ($X_{\text{TMGa}} = 4.9 \cdot 10^{-5}$), and trimethylantimony (TMSb) ($X_{\text{TMSb}} = 7.1 \cdot 10^{-5}$). The GaAsSb and the GaSb segments were both p-doped using diethylzinc (DEZn) ($X_{\text{DEZn}} = 3.5 \cdot 10^{-5}$) (Fig. 1). The diameter of the InAs segment was reduced from 40 nm to 20 nm using repeated ozone oxidation and citric acid digital etching cycles without any noticeable etching of the GaSb. The diameter of the GaAsSb segment was simultaneously reduced from 35 to 22 nm. Following the etching, a high-k layer of 1 nm Al_2O_3 and 4 nm HfO_2 was applied using atomic layer deposition (ALD) at temperatures of 300 °C and 120 °C, respectively. A 15-nm-thick SiO_x layer was evaporated to form the gate-drain spacer, followed by etching in highly diluted HF to remove residues on the sides of the nanowires. Another 1.2 nm of HfO_2 was deposited to compensate for the etching. The estimated EOT of the final high-k layer was 1.4 nm. The gate electrode was fabricated using a 60-nm-thick tungsten (W) film deposited conformally with sputtering. A physical gate-length of $L_g = 260$ nm was defined by back etching an organic resist followed by reactive ion etching (RIE) of the W in the exposed sections of the nanowire using SF_6/Ar . Subsequently, UV- lithography and RIE was used to define the gate-pads. The gate-source spacer was formed using a spin coated organic layer followed by back etch with O_2 -plasma. A Ni/Au top-metal was sputtered and pads defined using UV-lithography and wet-etching. A schematic illustration of a finished device is shown in Fig. 2 where the effective gate-length (L_{eff}), is determined by the unintentionally-doped channel formed by the upper part of the InAs segment (~ 100 nm). Figure 3 illustrates the process flow and a SEM image of a single nanowire TFET is showed in figure 4.

III. RESULTS AND DISCUSSION

Transistors were characterized in a common source configuration using the top contact, i.e. the GaSb segment, grounded. All data presented is measured for a device with one single nanowire. All currents are normalized to the circumference of the 20 nm diameter InAs segment. The gate-current of the device is 2 orders of magnitude lower than the lowest I_{DS} measured. The output characteristics (Fig. 5) exhibits a clear NDR in the reverse bias direction with a peak-to-valley current ratio of 14.8 at room temperature, which

confirms the presence of a high-quality tunneling junction within the transistor. Excellent current saturation is observed and the transistor reaches a maximum I_{DS} of $92 \mu\text{A}/\mu\text{m}$ at $V_{DS} = V_{GS} = 0.5 \text{ V}$. The device has good electrostatics as verified by a low DIBL of 25 mV/V (Fig. 6). As shown in Fig. 7, the device achieves a S_{\min} below 60 mV/dec. for current levels between 1 and $100 \text{ nA}/\mu\text{m}$ at $V_{DS} = 0.1 - 0.5 \text{ V}$, with the lowest S_{\min} of 48 mV/dec. for the drive voltages used. The lowest S_{\min} achieved by this device is 44 mV/dec. although at $V_{DS} = 0.05 \text{ V}$. A maximum transconductance (g_m) of $205 \mu\text{S}/\mu\text{m}$ is measured at $V_{DS} = 0.5 \text{ V}$ (Fig. 8). To confirm the sub- 60 mV/dec. operation, we measured in both bias directions and at various sweeping ranges. A small hysteresis of 5.4 mV at I_{60} is extracted both for a large and small V_{GS} sweep range (Fig. 9). The S_{\min} is well below 60 mV/dec. regardless of gate voltage sweep direction or magnitude, indicating that trapping/detrapping in, e.g., the gate oxide is not responsible for the subthermal S observed (insert Fig. 9). The transfer characteristics is also measured over a temperature range between 223 and 323 K , which is displayed in Fig. 10. The minimum S exhibits a weak temperature dependence and is increased from 38 to 54 mV/dec. as the temperature is increased from 223 to 323 K . This change is smaller than the one expected from thermionic emission, which further confirms that direct band-to-band tunneling is the dominant transport mechanism in these devices (Fig. 11). In addition, the current corresponding to the minimum S (I_{\min}) is increased (Fig. 12). The I_{DS} range in which the subthreshold swing is below 60 mV/dec. decreases with increasing temperature, mainly due to the increasing I_{\min} that could be attributed to increased trap-assisted tunneling at the lower bias range. The current at $S = 60 \text{ mV/dec.}$ (I_{60}) is $0.056 \mu\text{A}/\mu\text{m}$ and $0.31 \mu\text{A}/\mu\text{m}$ at $V_{DS} = 0.1$ and 0.3 V , respectively. The I_{60} is reduced with the temperatures but it has a weaker temperature dependence than I_{\min} , (Fig. 12, Fig. 13). From the variable temperature measurements, we extract an activation energy as shown in Fig. 14. For large negative biases, a comparably large barrier $\Phi \sim 0.6 \text{ eV}$ is determined demonstrating that alternative mechanisms with a higher activation mechanism start to dominate the transport at the very lowest current levels. The transconductance show a small decrease with increasing temperature, as expected for a tunneling device (Fig. 15). For low-power analogue TFET applications, the voltage gain and transconductance efficiency are of importance. Figure 16 shows the internal (maximum) voltage gain g_m/g_d vs V_{GS} , reaching a maximum value of 2400 . Figure 17 shows the transconductance efficiency g_m/I_{DS} . Measured values are between $45 - 50 \text{ V}^{-1}$ that is higher than the fundamental limit of 38 V^{-1} for an ideal MOSFET. Benchmarking against state-of-art Si and III-V TFETs [4, 6, 8, 11, 12], demonstrates that our device operates below 60 mV/dec. at higher current levels. The current at S_{\min} is one order of magnitude higher than the other devices with sub- 60 mV/dec. operation (Fig. 18). As shown in figure 19, the I_{60} for

this device is higher than previously reported results, which is important for RF applications using the steep slope. The device is also benchmarked against Si, III-V planar and nanowire MOSFET [13-16], showing superior performance at low voltages (Fig. 20).

IV. CONCLUSIONS

We have demonstrated a vertical InAs/GaAsSb/GaSb TFET with a S_{\min} of 48 mV/dec. for V_{DS} of $0.1 - 0.5 \text{ V}$. The device shows good electrostatic with low DIBL (25 mV/V). For an $I_{\text{off}} = 1 \text{ nA}/\mu\text{m}$ an $I_{\text{on}} = 10.6 \mu\text{A}/\mu\text{m}$ is obtained at $V_{DS} = 0.3 \text{ V}$. The device achieves an intrinsic gain of 2400 and a transconductance efficiency of 50 V^{-1} . Our novel heterostructure design enabled by the reduced constraint for lattice matching in the bottom up nanowire growth in combination with aggressively scaled dimensions and a gate-all-around geometry demonstrate that III-V TFETs are viable alternative both for low-power logic and analog applications.

ACKNOWLEDGMENT

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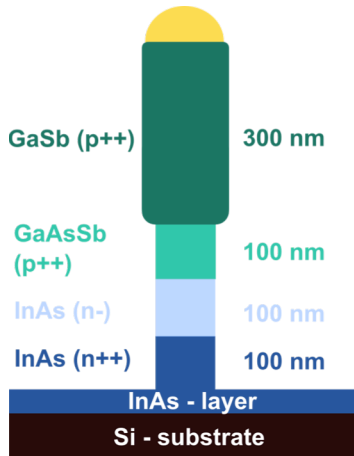


Fig. 1. Schematic illustration of the nanowire after growth.

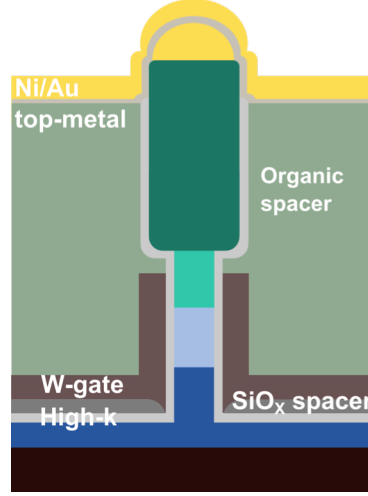


Fig. 2. Schematic illustration of the InAs/GaAsSb/GaSb TFET.

- - Definition of Au-seed particles using EBL
- - MOVPE growth of nanowires
- - Digital etching
- - Apply high-k using ALD
- - Evaporate SiO_x to form drain-gate spacer
- - Sputter on W
- - Define gate-length and gate-pad
- - Organic source-gate spacer
- - Etch out gate-via and drain-via
- - Sputter on Ni and Au to form top-metal
- - Define gate, gate and source contact-pads with UV

Fig. 3. Process flow showing the main fabrication steps.

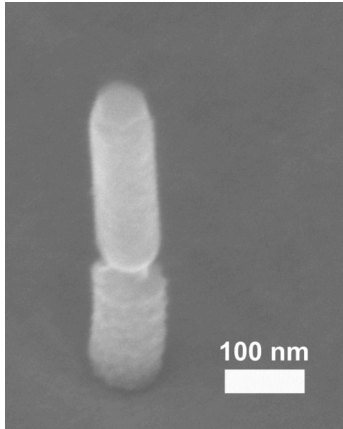


Fig. 4. SEM-image of a nanowire with gate-metal applied. The physical gate-length is 260 nm, whereas the effective gate-length is 100 nm corresponding to the length of the undoped InAs segment.

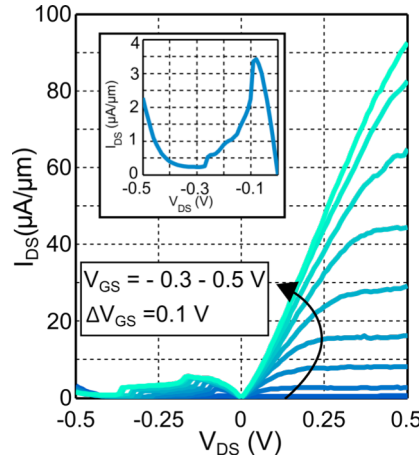


Fig. 5. Output characteristics of the device with the best slope. A maximum current of $92 \mu\text{A}/\mu\text{m}$ was obtained at $V_{\text{DS}} = V_{\text{GS}} = 0.5 \text{ V}$. Insert shows NDR with peak-to-valley current ratio of 14.8.

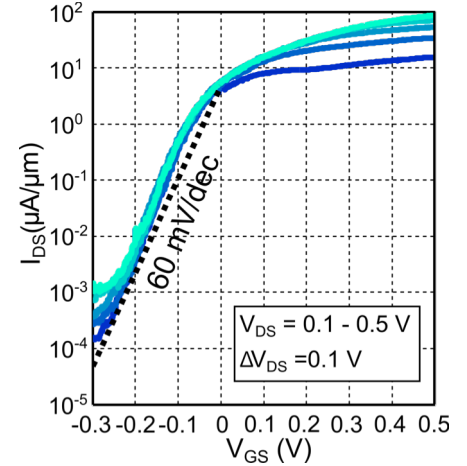


Fig. 6. Transfer characteristics of the device with the best slope. The dotted line shows the 60 mV/dec. slope.

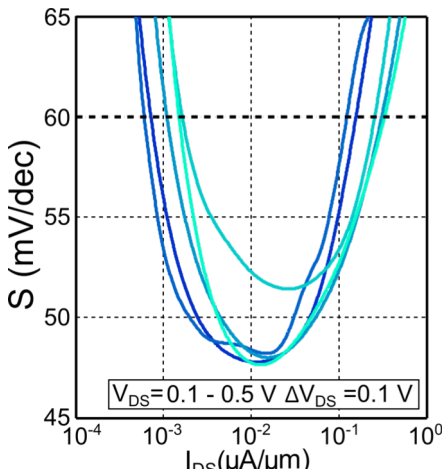


Fig. 7. Subthreshold slope vs I_{DS} . The lowest slope is 48 – 53 mV/dec., for $V_{\text{DS}} = 0.1\text{-}0.5 \text{ V}$.

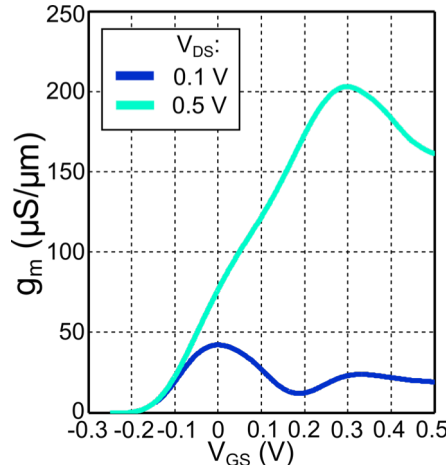


Fig. 8. Transconductance of the device, reaching a maximum g_{m} of $205 \mu\text{S}/\mu\text{m}$ for $V_{\text{DS}} = 0.5 \text{ V}$.

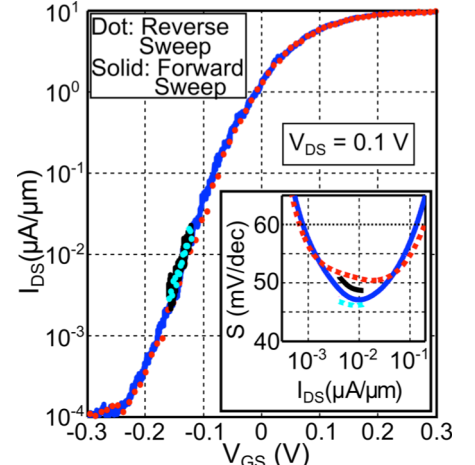


Fig. 9. Large and a small voltage sweep from low to high and back showing little hysteresis. The insert shows I_{DS} vs S for the same sweeps.

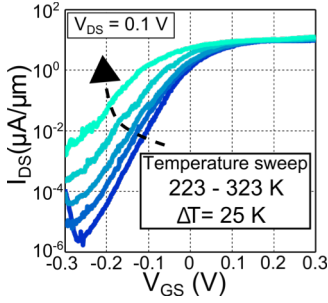


Fig. 10. Transfer characteristics at temperatures from 223 to 323 K with steps of 25 K at $V_{DS} = 0.1$ V.

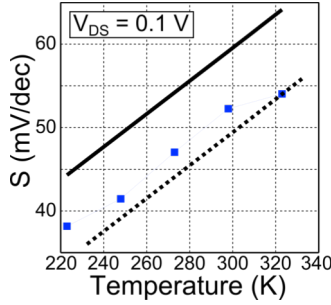


Fig. 11. Minimum subthreshold swing for different temperatures. Solid black line is the kT -line and the dotted black line is a parallel line to guide the eye.

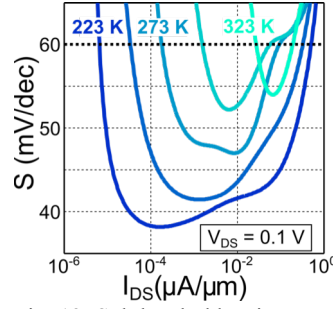


Fig. 12. Subthreshold swing vs I_{DS} at different temperatures in steps of 25 K.

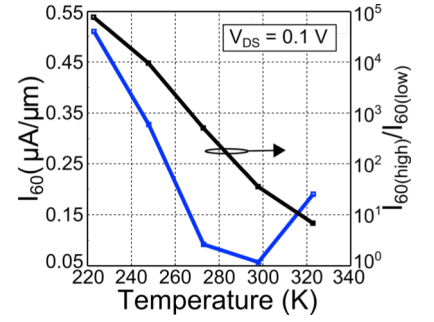


Fig. 13. I_{60} as a function of the temperature (blue). The ratio between highest and lowest current for the sub-60 mV/dec. region as a function of the temperature (black) with steps of 25 K.

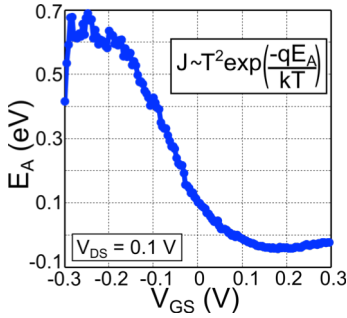


Fig. 14. Activation energy as function of V_{GS} . The temperature range used for extraction of the activation energy is 223-323 K with steps of 25 K.

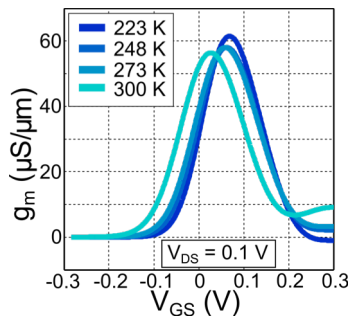


Fig. 15. Transconductance at the different temperatures from 223 to 300 K with steps of 25 K.

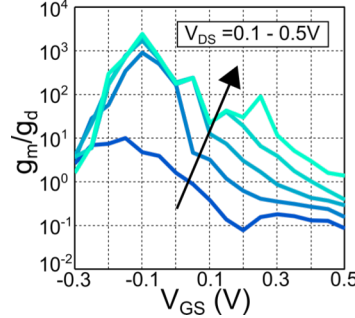


Fig. 16. Internal gain for drive voltages 0.1 - 0.5 V. The highest value is achieved in the region where the subthreshold swing is below 60 mV/dec.

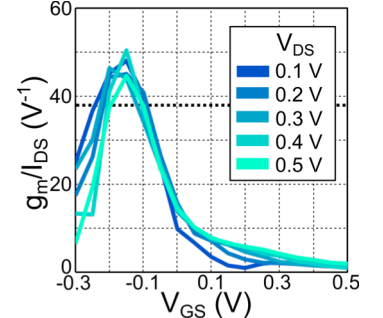


Fig. 17. Transconductance efficiency for drive voltages 0.1 - 0.5 V. As for the internal gain, the highest values are achieved in the region with the lowest S . Dotted line (38 V^{-1}) shows fundamental limit for the MOSFET.

TABLE I BENCHMARKING			
Published work	Material system	Minimum point SS ($V_{DS} = 0.1$ V)	Current at lowest SS ($V_{DS} = 0.1$ V)
Knoll [4]	s-Si	30 mV/dec	0.2 pA/μm
Tomioka [6]	Si/InAs	21 mV/dec	0.1 pA/μm
Memisevic [12]	InAs/GaSb	69 mV/dec	9.2 nA/μm
Ahn [11]	InGaAs	57 mV/dec	0.3 nA/μm
Dewey [8]	InGaAs	60 mV/dec	1 nA/μm
This work	InAs/GaAsSb/GaSb	48 mV/dec	67 nA/μm

Fig. 18. Device in this work benchmarked against devices fabricated of Si and III-V, both in lateral and vertical geometry.

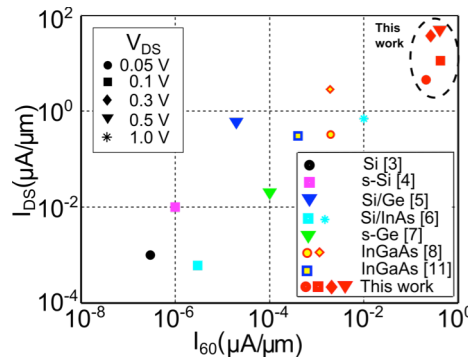


Fig. 19. Benchmarking of devices with sub-60 mV/dec. operation at various drive voltages. Here, the current is determined by adding 0.4 V to the I_{60} voltage.

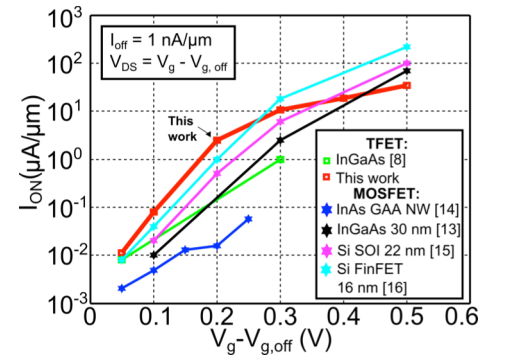


Fig. 20. I_{on} at $I_{off} = 1 \text{ nA}/\mu\text{m}$ for the device in this work compared to other TFETs and MOSFETs.