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Vertical InAs/GaSb Nanowire Axial TFETs Integrated on Si-substrates

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Tunnel Field-Effect Transistors (TFETs) have the potential to provide better subthreshold characteristics (SS<60 mV/dec), and to enable a reduction of the power supply voltage with maintained drive current[1]. One promising structure for TFETs are gate-all-round, axial InAs/GaSb nanowire heterostructures where the wrap gate provide excellent electrostatic control and the broken bandgap can provide large I_{on} [2].

InAs/GaSb nanowires are grown on Si (111)-substrates with a 200-nm-thick InAs n+-layer [3], using the vapor-liquid-solid growth mechanism. 40 nm diameter Au-seed particles are positioned using electron beam lithography and lift-off. The nanowires are grown in a metal-organic-vapor-phase-epitaxy (MOVPE) reactor by using the precursors trimethylindium and arsine for the InAs segments, followed by switching to trimethylgallium and trimethylantimony for the growth of the GaSb segment. The bottom half of the InAs segment is n-doped with tetraethyltin, and the GaSb section is p-doped with diethylzinc. Figure 1 shows an SEM-image of the nanowires after growth. The number of nanowires in the devices is varied between 1 and 200.

After growth, the nanowires are digitally etched using repeated cycles of ozone oxidation and citric acid etching, reducing the InAs diameter from 40 nm to 30 nm, and also removing the GaSb-shell that is formed during the GaSb growth. Reference devices without any etching are also fabricated. After the digital etch, a gate dielectric is deposited using atomic layer deposition with 5 cycles of Al_2O_3 and 36 cycles of HfO_2 (EOT~1.4nm.). Device isolation is achieved by wet etching the InAs buffer layer, producing RF-compatible devices. The bottom spacer, an isolating separation layer between the InAs-mesa and the gate, is fabricated through a spin-on resist and etchback process. The gate is formed through sputtering of tungsten, and the gate length is set by an etchback process. A top spacer, isolating the gate from the drain, is also formed using a spin-on resist and etchback process. The top-metal, for the probing-pads, is fabricated by thermal evaporation and lift-off process of a Ni/Au-bilayer, after removing the high-k on the top of the wires with a buffered oxide etch. A schematic illustration of the device is shown in Figure 2.

DC measurement data are presented in Figures 3-5. Figure 3 shows output characteristics from various nanowire array-sizes, demonstrating the scalability of the process. Figure 4 and 5 show output and transfer characteristics, for devices with and without digital etching steps. The digital etch substantially improves the subthreshold characteristics, without degrading the on-current. A minimum subthreshold swing of 130 mV/decade is obtained at V_{ds}=50 mV, with an I_{on}=5 μA/μm at V_{ds}=0.5 V. This performance is better compared to similar lateral nanowire TFETs[4].

Acknowledgments

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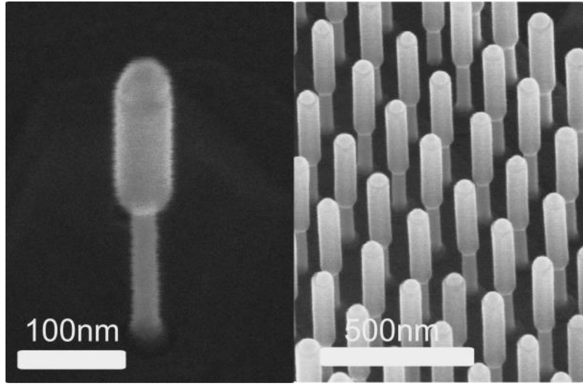

Fig. 1. SEM images (30° tilt) of InAs/GaSb nanowires after growth and digital etching with citric acid.

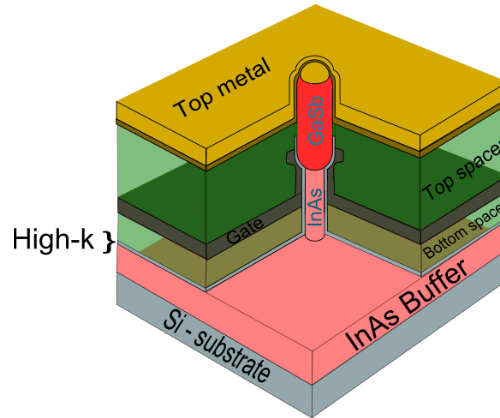

Fig. 2. Schematic cross-section of the axial TFET.

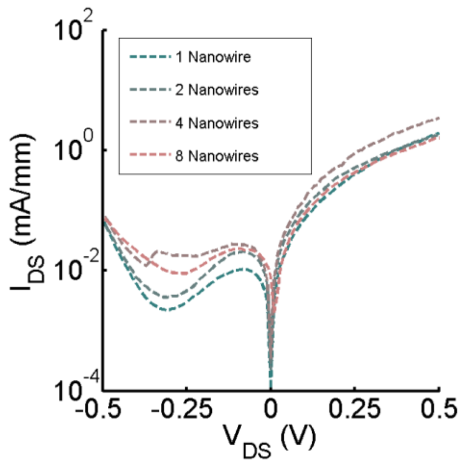

Fig. 3. I_{DS} vs V_{DS} for the devices with 1, 2, 4, and 8 nanowires. After normalization, the currents are similar.

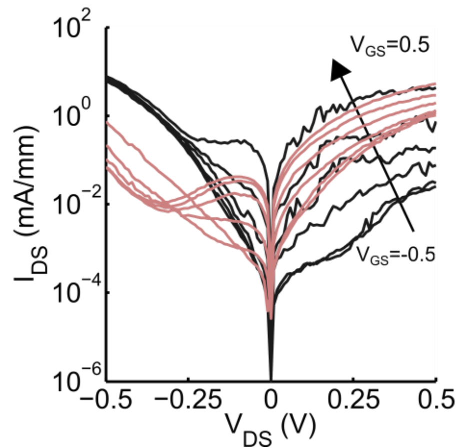

Fig. 4. I_{DS} vs V_{DS} characteristics sweeping the V_{GS} from -0.5 to 0.5 V with steps of 0.25 V. The black curves show data for a device where nanowires were digitally etched and the red curves shows data from a device that was not digitally etched.

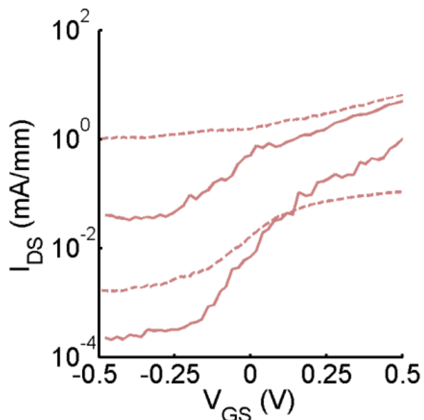

Fig. 5 I_{DS} vs V_{GS} characteristics at V_{DS} at 50 mV and 0.5 V respectively. Dotted lines show characteristics of similar devices without any digital etching.