Statistics of InAs/InGaAsSb/GaSb TFETs with sub-50 mV/decade operation at V_{DS}=0.3V

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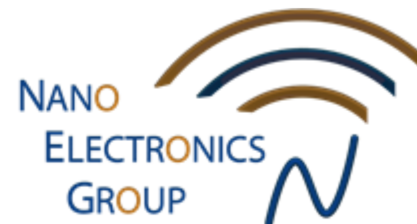

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Outline

- Motivation
- Principle behind the TFET
- Devices
- TFET characteristics
- Benchmarking
- Statistical data
- Conclusions

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- Reducing the drive voltage V_{DD}

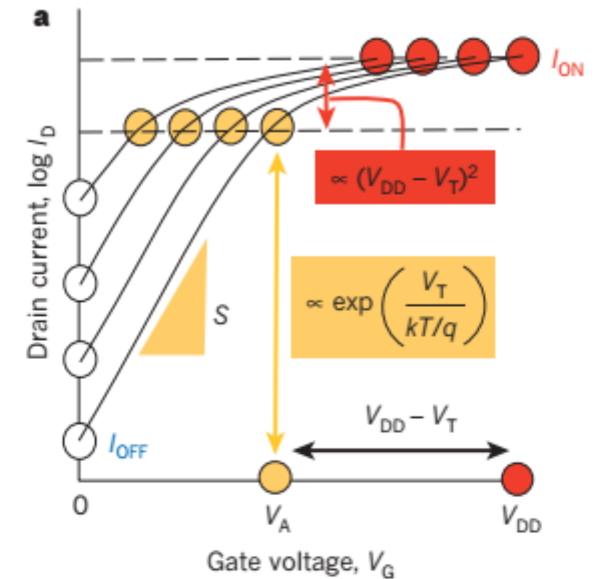
[1] $$E_{total} = E_{dynamic} + E_{leakage} = \alpha L_d C V_{DD}^2 + L_d I_{OFF} V_{DD} \tau_{delay}$$

- Subthreshold swing is limited to 60 mV/dec.

$$S = \underbrace{\frac{dV_G}{d\Psi_s}}_{m} \underbrace{\frac{d\Psi_s}{d(\log_{10} I_D)}}_{n} \cong \left(1 + \frac{C_d}{C_{ox}}\right) \ln 10 \frac{kT}{q}$$

[1] $$\rightarrow \frac{kT}{q} \ln 10 \cong 60 \text{ mV decade}^{-1} \mid T = 300 \text{ K}$$

Thermal limit for the MOSFET



[1] Ionescu et al, Nature 479, 2011

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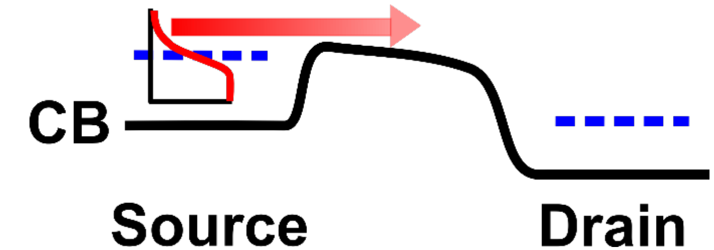
- Traditional MOSFETs are limited to lowest subthreshold swing (S) of 60mV/dec. at RT.



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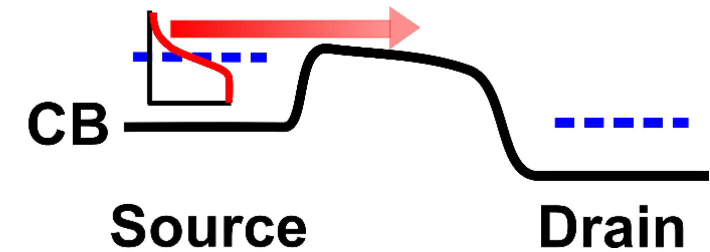
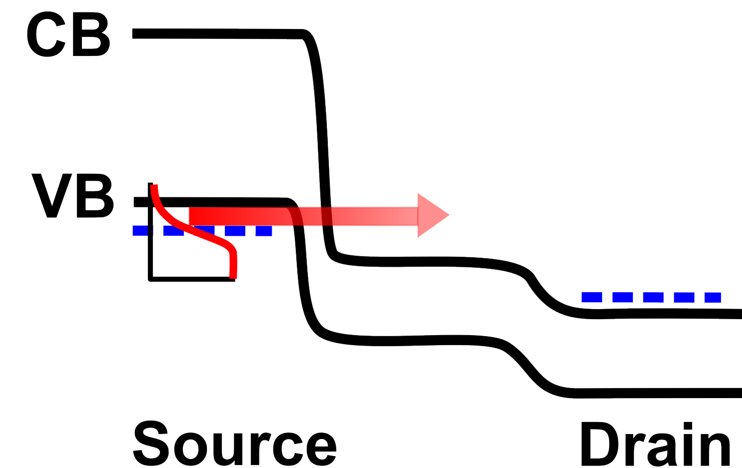
- Traditional MOSFETs are limited to lowest subthreshold swing (S) of 60mV/dec. at RT.

- TFET can operate below 60 mV/dec. due to bandpass filtering of high energy carriers.





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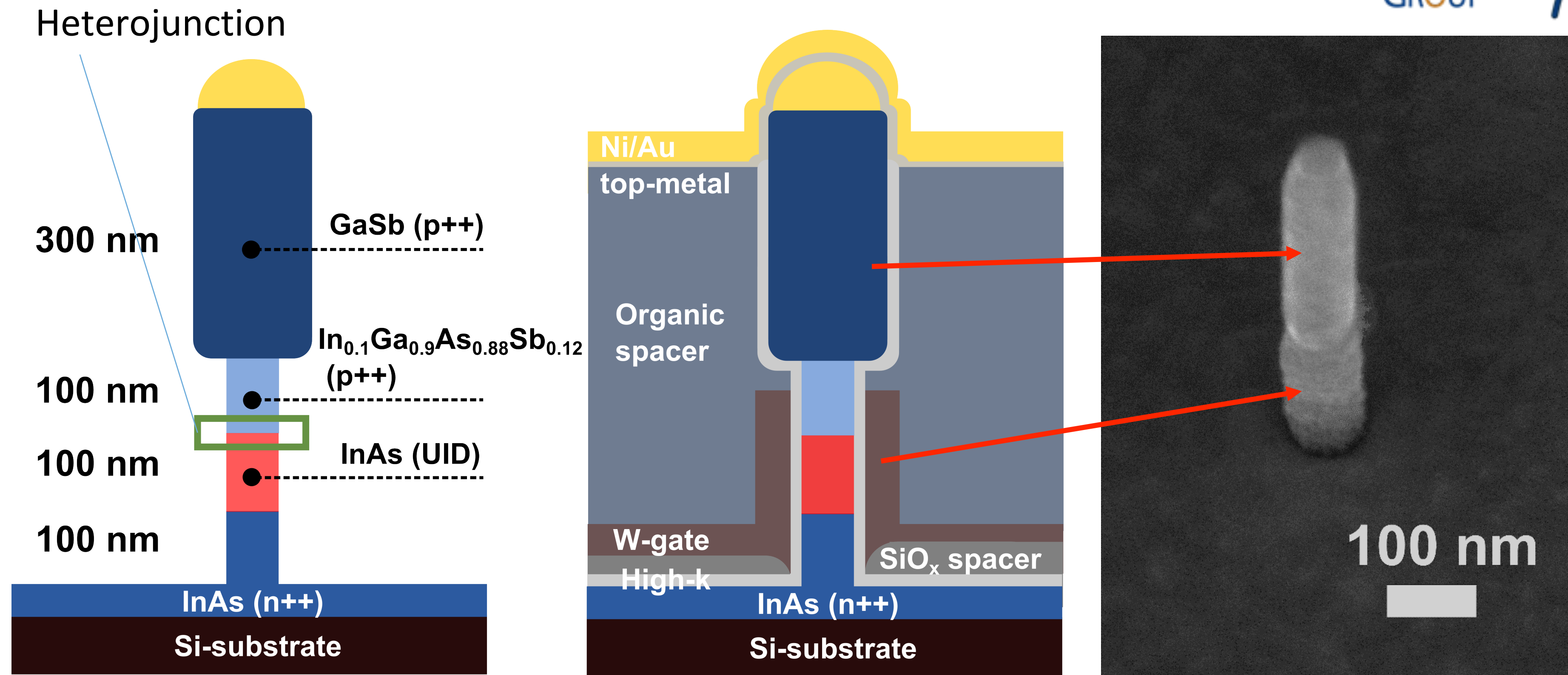

- Devices with 1 to 4 nanowires
- Thinnest diameter of the nanowire is 20 nm (InAs)
- Estimated EOT 1.4 nm
- Channel length is 100 nm

Memisevic et. al., IEEE EDL, 2016
Memisevic et. al., IEDM, 2016

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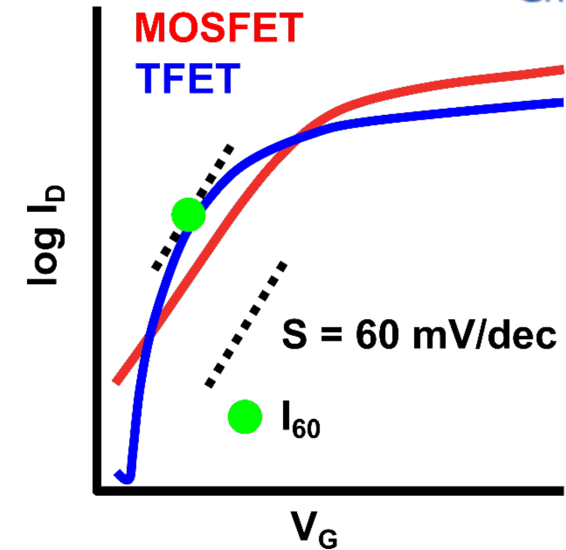
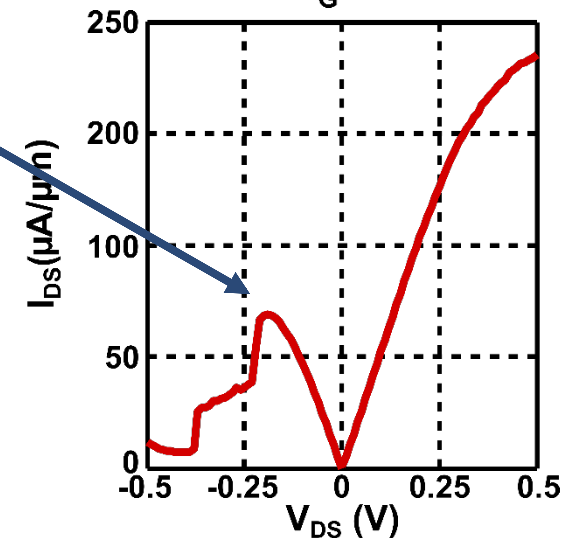
- Sub-60 mV/decade slope at low bias
- Highest current with sub-60 mV/decade slope: I_{60}
- Negative differential resistance





[1] Memisevic et. al., IEEE EDL, 2016]

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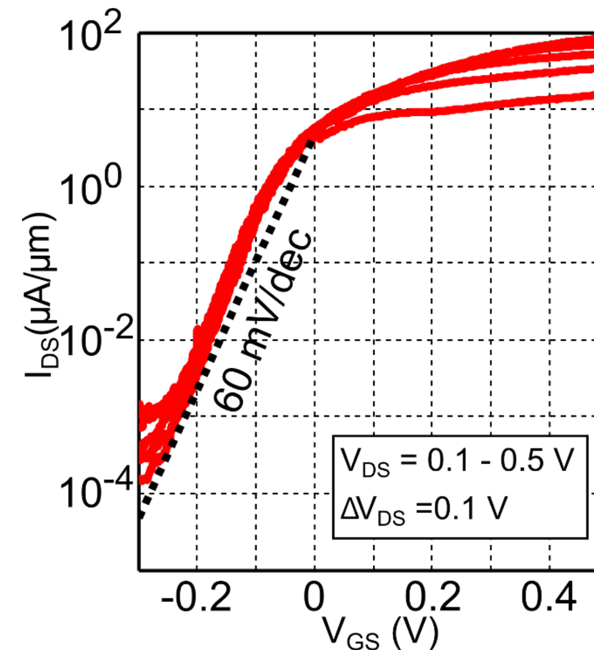
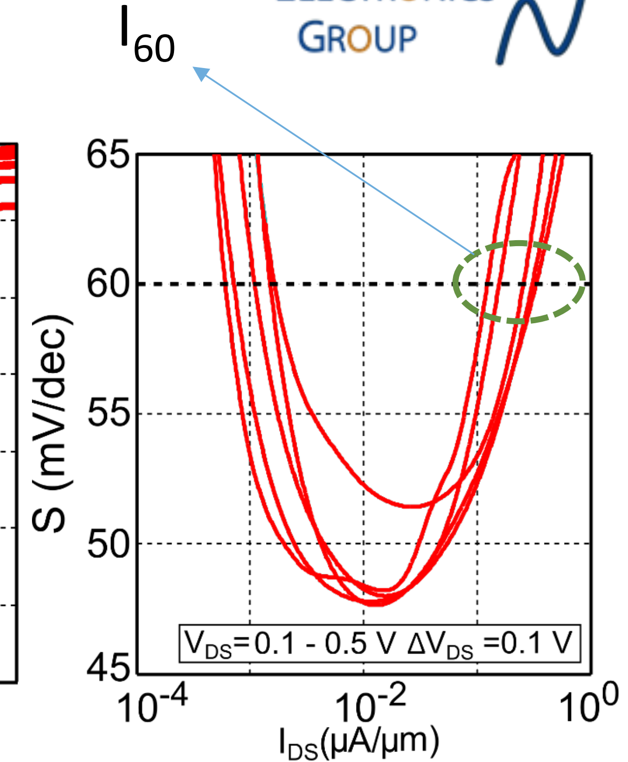
- Good electrostatic control (DIBL 25 mV/V)
- S_{min} = 48 mV/dec at V_{DS}=0.3 V
- Sub-60 mV/dec operation over two orders of magnitude current (Vds=0.1-0.5V)
- I_{60}= 0.31 µA/µm at V_{DS}=0.3 V





[Memisevic et. al., IEDM 2016]

DIBL = Drain Induced Barrier Lowering

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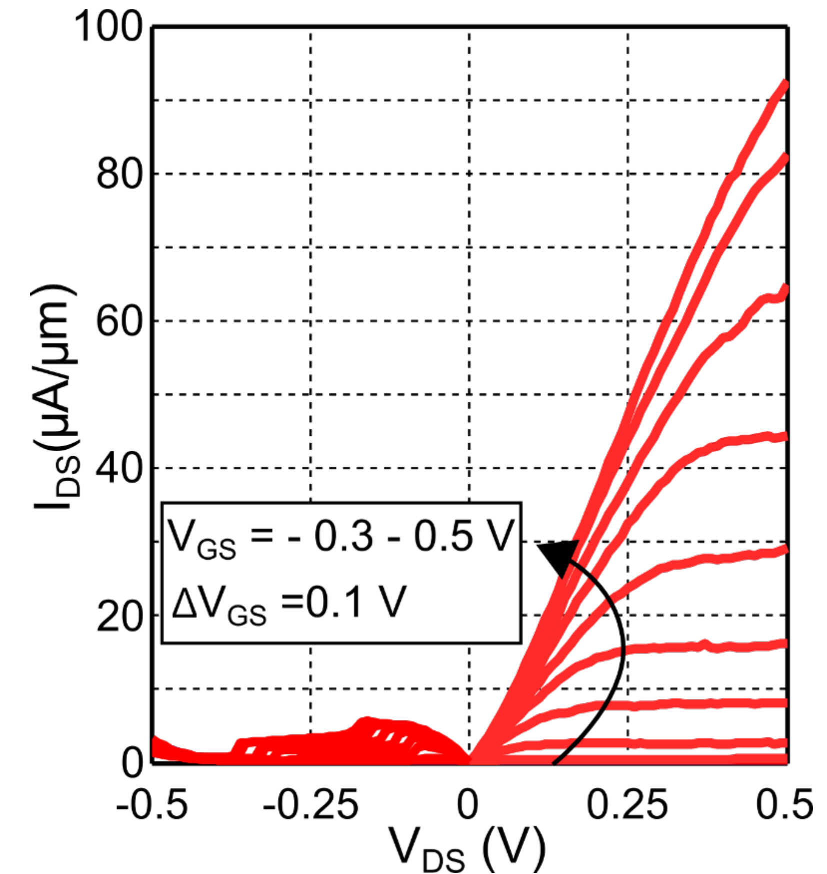
- Strong NDR in reverse bias with PVCR 14.8
- High quality junction
- Good saturation
- Weak superlinear behaviour



[Memisevic et. al., IEDM 2016]

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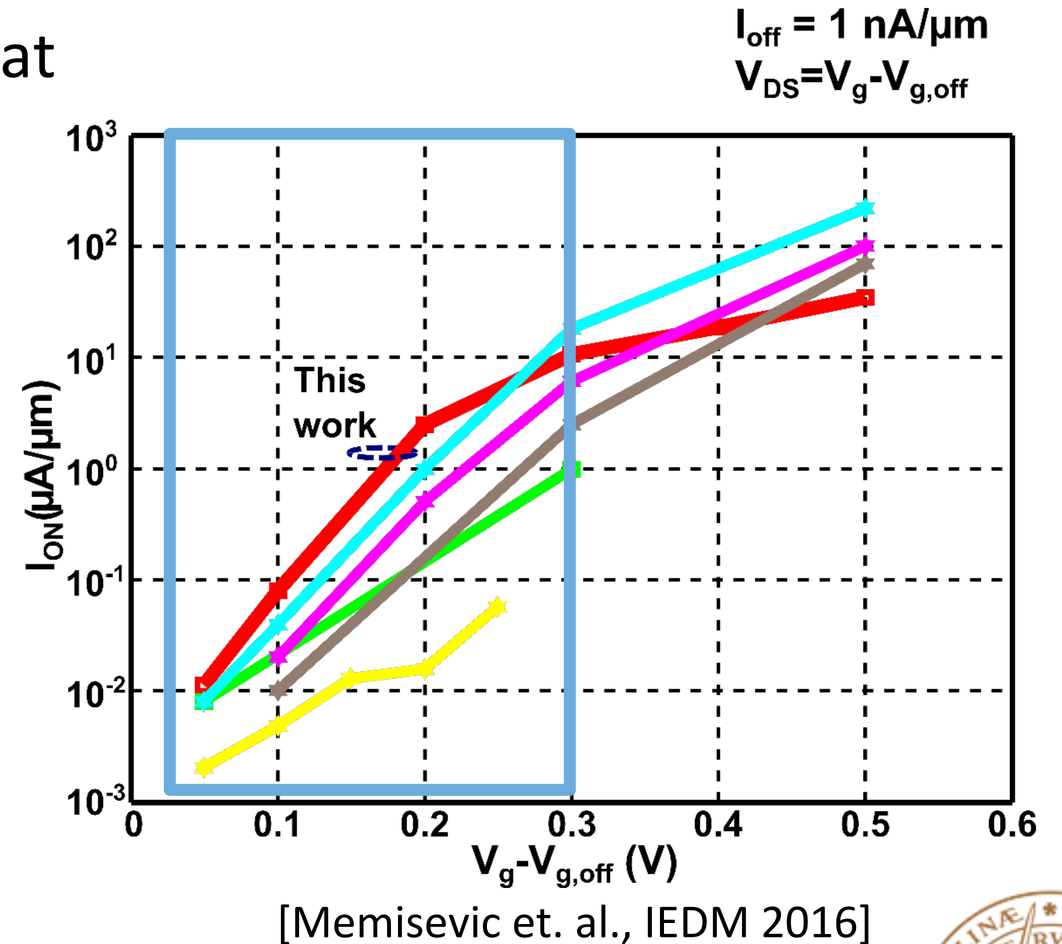
- Benchmarking against TFET and MOSFETs
- Higher currents (2-2.5x) at voltages 0.05-0.2 V



[Memisevic et. al., IEDM 2016]

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Question:

Is this a ”hero” device?

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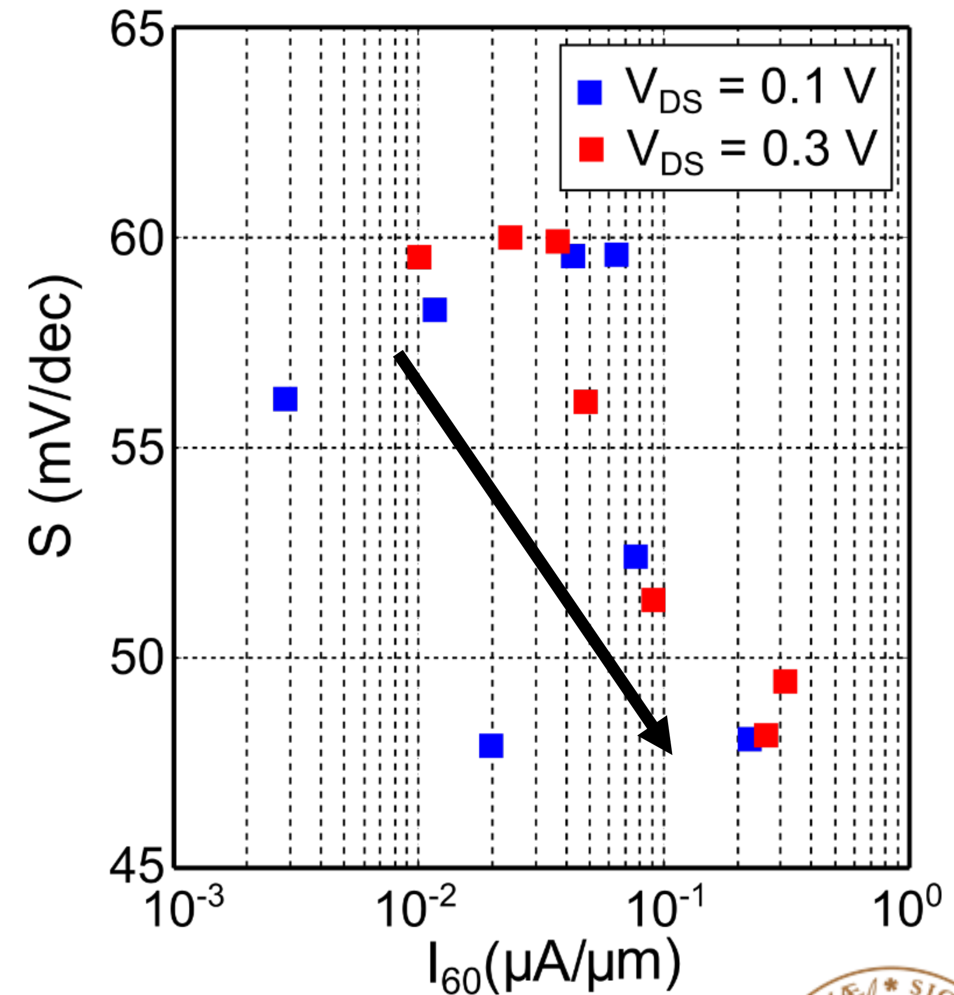
- Number of devices working below thermal limit (approx. 70%)
- I_{60} current is in range of 0.01 to 0.3 uA/um
- I_{60} increases as the S is decreasing



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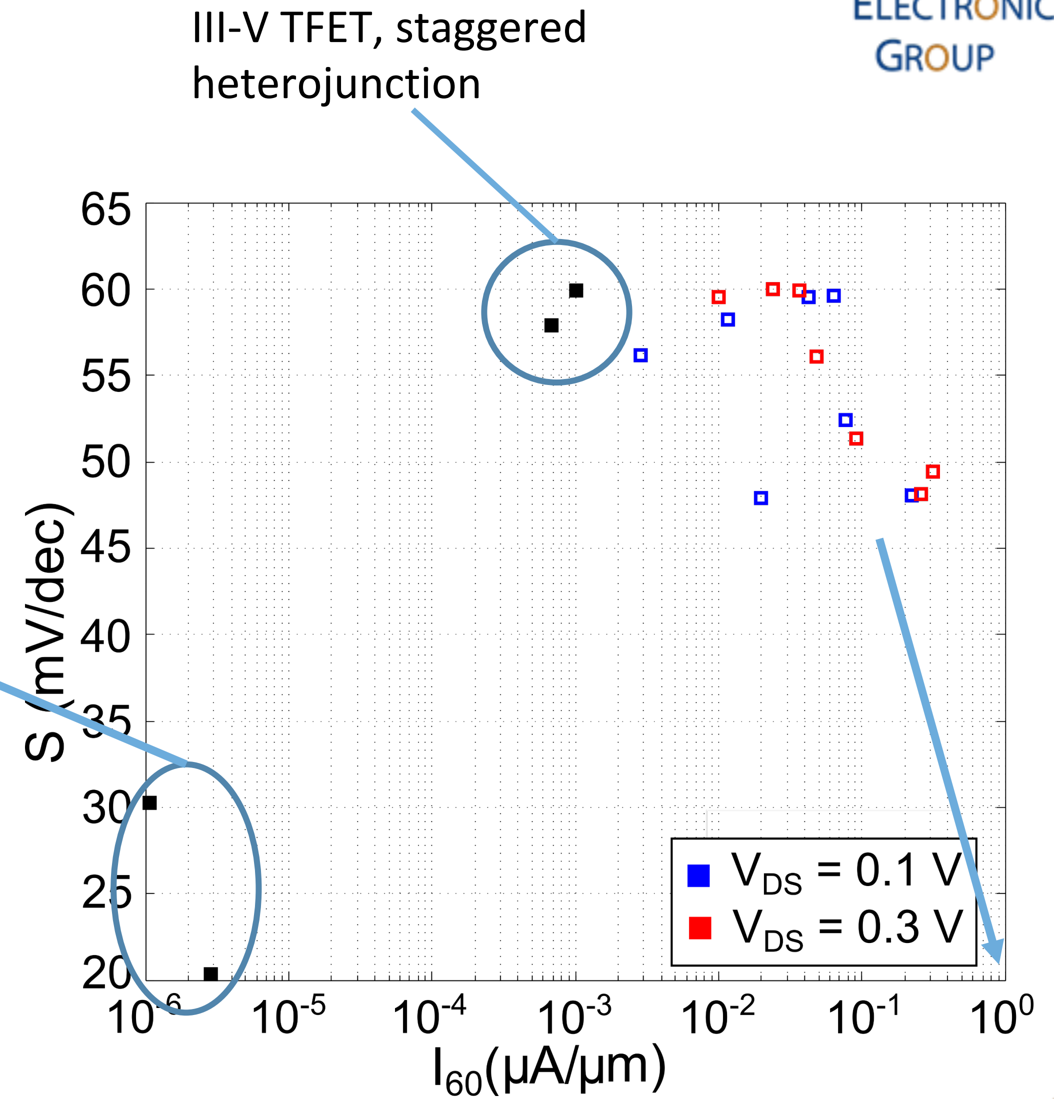
Si TFET, III-V homojunction TFET



[4] Si, (Knoll et al, 2013)
[6] Si/InAs, (Tomioka et al, 2012)
[8] InGaAs, (Dewey et al., 2011)
[11] InGaAs, (Ahn et al. 2016)

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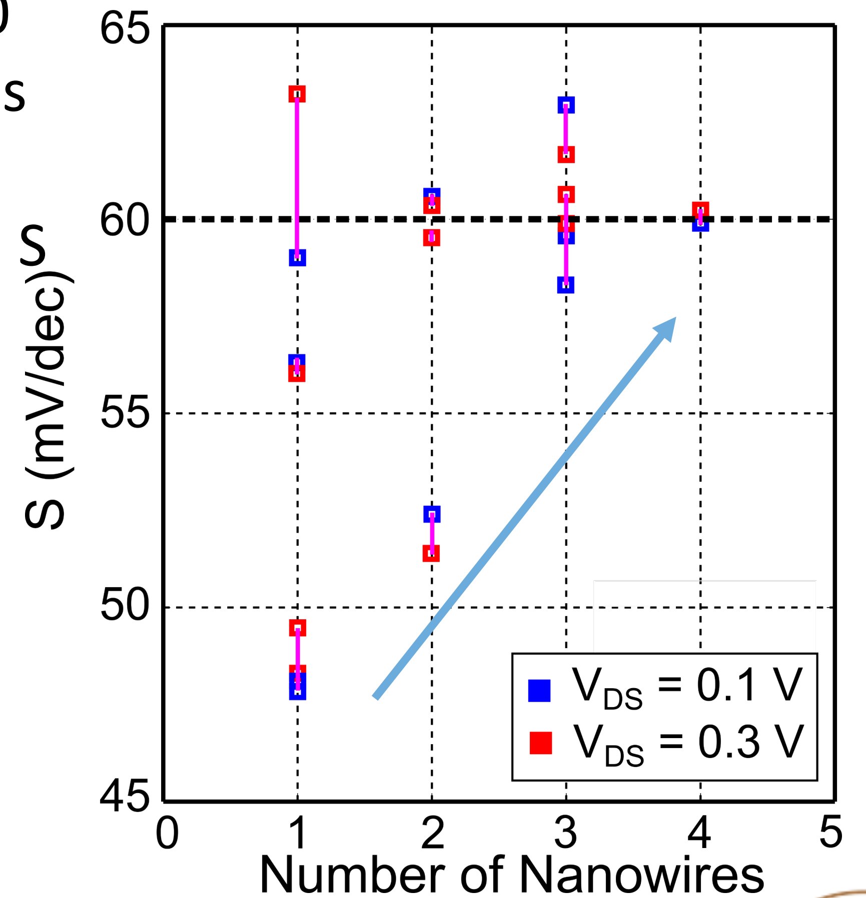
- Devices keep to operate below 60 mV/dec when number nanowire is increased
- Observed Vt shift and variation in S



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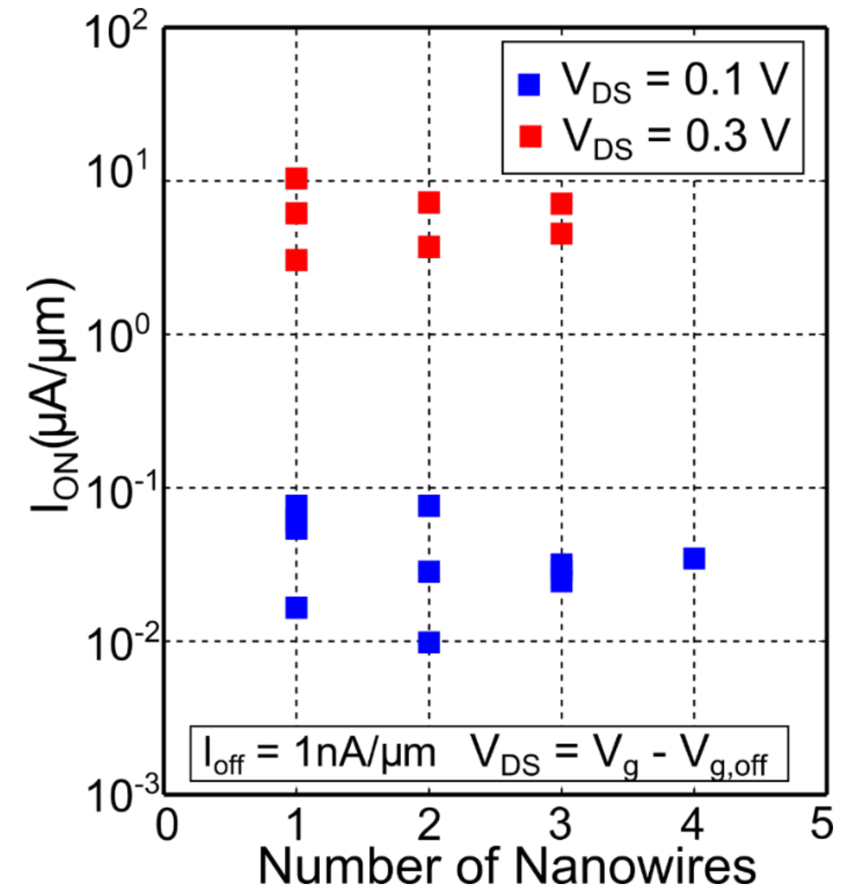
- I_{on} at V_{DS} of 0.1 and 0.3 V is constant even if numbers of the nanowires is increased
- Even with varying S, I_{on} is constant



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- S_{min} = 48 mV/dec and record high I_{60} of 0.31 uA/um at V_{DS}=0.3V
- Devices with performance comparable or better to Si MOSFET at V_{DS} below 0.3V
- Approx. 70% of devices from same sample operate below 60 mV/decade

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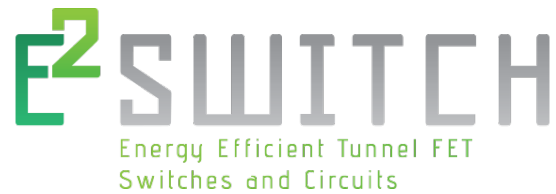
Thanks for your attention



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