Statistics of InAs/InGaAsSb/GaSb TFETs with sub-50 mV/decade operation at VDS of 0.3V

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Statistics of InAs/InGaAsSb/GaSb TFETs with sub-50 mV/decade operation at V_{DS} of 0.3V

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Tunnel Field-Effect Transistors (TFETs) have the potential to provide better subthreshold characteristics (SS<60 mV/dec), and to enable a reduction of the power supply voltage with maintained drive current as compared to MOSFETs.[1] One promising structure for TFETs is gate-all-round, axial InAs/InGaAsSb/GaSb nanowire heterostructures where the wrap gate provides excellent electrostatic control and the nanowire geometry allows for combination of materials with large lattice mismatch.[2]

In this work, InAs/InGaAsSb/GaSb nanowires were grown on Si (111)-substrates with a 200-nm-thick InAs n+-layer [3], using the vapor-liquid-solid growth mechanism. Utilizing electron beam lithography and a PMMA based lift-off process Au-seed particles were positioned in arrays with 1 to 8 particles with diameter of 40 nm. The nanowires were grown in a metal-organic-vapor-phase-epitaxy (MOVPE) reactor by using the precursors trimethylindium, arsine, trimethylgallium and trimethylantimony for the growth of the three segments. The bottom half of the InAs segment was n-doped with tetraethyltin, and the InGaAsSb/GaSb section was p-doped with diethylzinc. After growth, the nanowires were digitally etched using repeated cycles of ozone oxidation and citric acid etching, reducing the InAs diameter to 20 nm. The InGaAsSb was etched at a lower rate and no visible etching of GaSb was observed. A gate dielectric was deposited using atomic layer deposition with 5/36 cycles of Al_2O_3/HfO_2 (EOT~1.4 nm). The bottom spacer was fabricated using thermal evaporation of SiO_x. It was followed by gate-formation using sputtering of W, and the gate length was set by an etchback process. A top spacer was formed using a spin-on resist and etchback process. The high-k was removed from the top of the nanowires using diluted HF, followed by sputtering of a Ni/Au-bilayer and UV-lithography to define the probing-pads.

The best device exhibits excellent electrostatics with a low DIBL of 25 mV/V, and a subthreshold swing (*S*) of 48 mV/dec for V_{DS} of 0.1-0.5V. Using I_{off} = 1 nA/μm and V_{DS} = 0.3V, an I_{on} of 10.6 μA/μm and a record high I_{60} of 0.31 μA/μm are achieved demonstrating a TFET that operates at high currents and still below the thermal limit of 60 mV/dec.[4] Statistical data for the devices show a trend of increasing I_{60} current with decreasing *S*, due to an increasing voltage range in which the device operates in the sub-60 region. The on-current shows no dependence on the number of the nanowires in the arrays. The peak-to-valley current ratio increases with decreasing number of nanowires reaching 14.6 for the best device. The best *S* are achieved in a device with a single nanowire, although most devices still reach sub-60 mV/dec operation for the lower drive voltages. Since the performance at low supply voltages surpasses that of state-of-the-art Si MOSFETs the results are highly encouraging for future low-power electronic applications.[4]

Acknowledgments

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References

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[2] M. Borg et al, *Nano Lett.*, Vol. 10, pp. 4080-4085, 2010
[3] S. Gorji Ghalamestani et al, *J. Cryst. Growth*, Vol. 332, pp. 12-16, 2011
[4] E. Memisevic et al, IEDM, 2016

All currents are normalized to the circumference of the InAs and the number of the nanowires in the devices.

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Figures

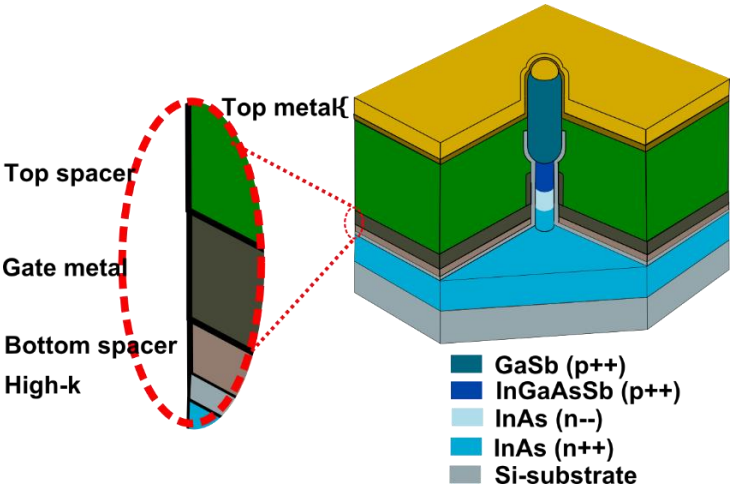

Fig. 1. Schematic image of the vertical InAs/InGaAsSb/GaSb TFET showing different sections of the nanowire and layers.

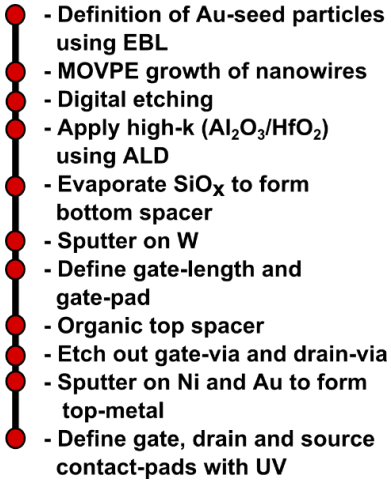

Fig. 2. Process-flow for the device fabrication. EOT for the high-k is 1.4 nm.

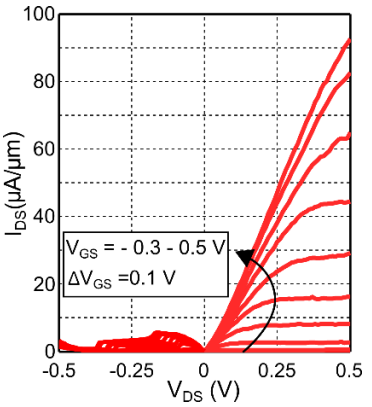

Fig. 3. Output data for the best device, reaching 92 μA/μm at V_{GS} = V_{DS}= 0.5V. Peak to valley current ratio for the device is 14.5.

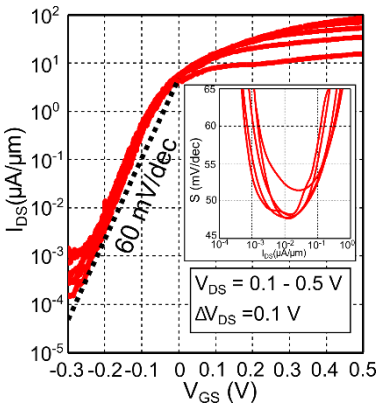

Fig. 4. Transfer data for the best device, showing small DIBL of 25 mV/V and reaching 48 mV/dec at voltages 0.1-0.5V as shown in insert.

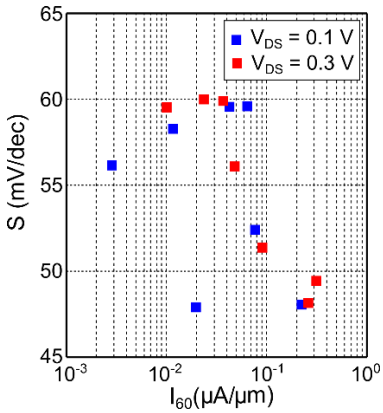

Fig. 5. Subthreshold swing vs I_{60}, for V_{DS} of 0.1V and 0.3V, for a several devices with different number of nanowires.

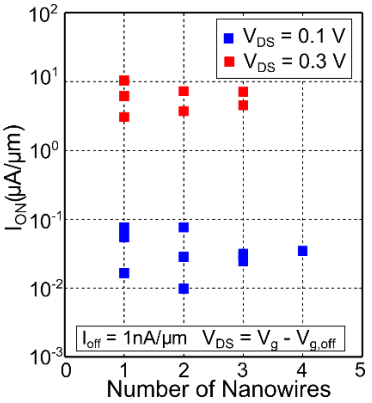

Fig. 6. I_{on} vs number of nanowires in each device.

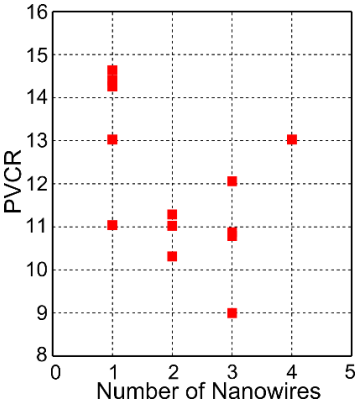

Fig. 7. Peak to valley current ratio vs number of nanowires in the device.

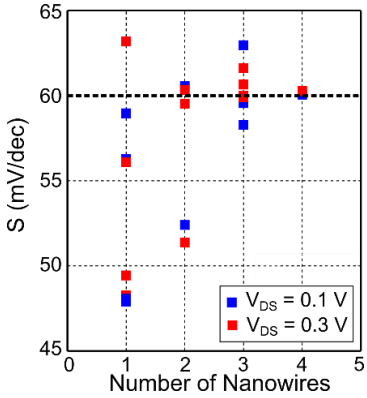

Fig. 8. Subthreshold swing vs number of nanowires in the devices.

*All currents presented in this work are normalized using circumference of the InAs segment and number of nanowires.