Vertical InAs/GaSb Nanowire Axial TFETs Integrated on Si-substrates

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E2SWITCH
Energy Efficient Tunnel FET Switches and Circuits

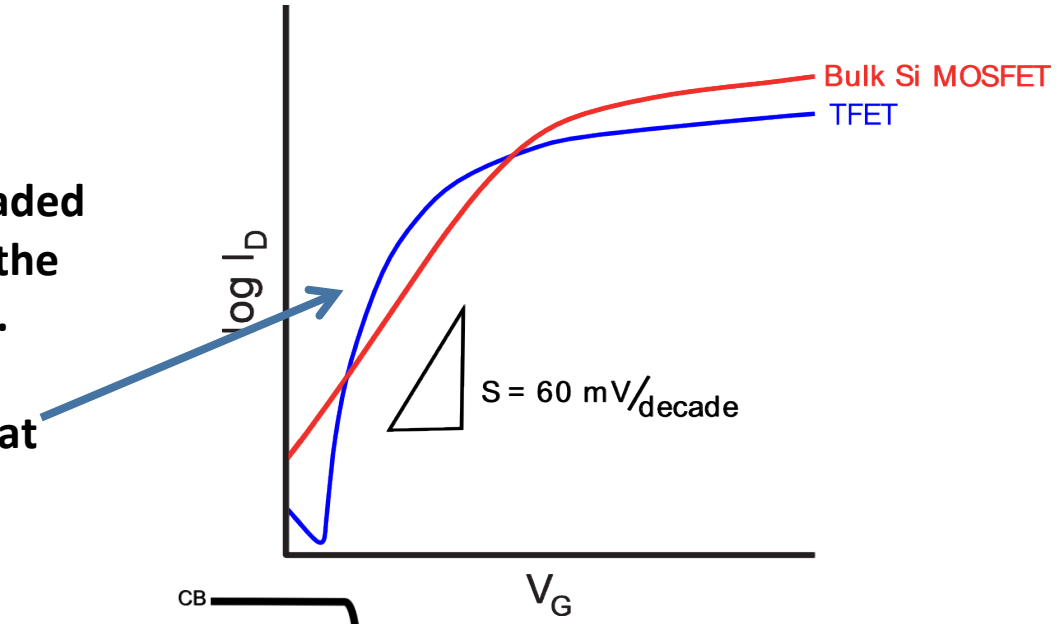
Swedish Foundation for Strategic Research

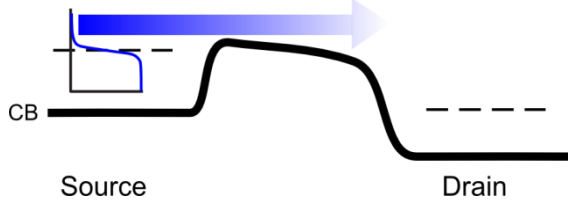
Outline

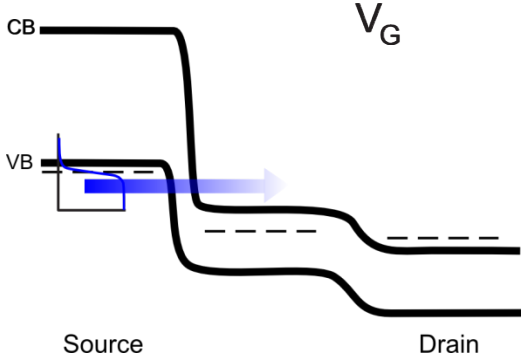
- General about the TFETs
- Fabrication of the transistors
- DC-data
- Benchmarking
- Conclusions

General about the TFETs

- **Traditional MOSFET are limited to lowest SS of 60 mV/dec at RT.**
- **With TEFT that limit can be evaded due to usage of electrons outside the tail in the Fermi-Dirac distribution.**
- **Higher current can be achivied at lower voltages.**



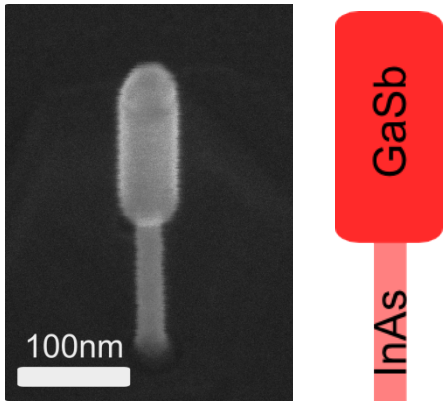




The InAs/GaSb nanowires

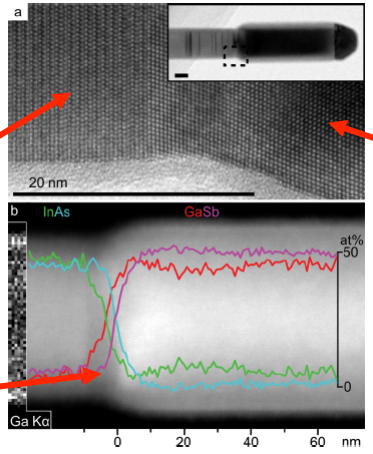
- **Combine materials with a large lattice mismatch**
- **Good electrostatic control**
- **Growth conditions for nanowires with InAs diameter of 25-30 nm :**
  - **high enough P_{TMSb}**
  - **and high enough growth T**

  Because the growth of the GaSb on InAs stem is highly sensitive to TMSb partial pressure. [1]



T_{GaSb} = 500 ^{O}C
P_{TMSb} =0.6 Pa
V/III = 1.1
DeZn used for p-doping

T_{InAs} = 420 OC
P_{AsH_3} = 1.92 Pa
V/III=69
TESn used for n-doping of the lower part of the stem



InAs (WZ)

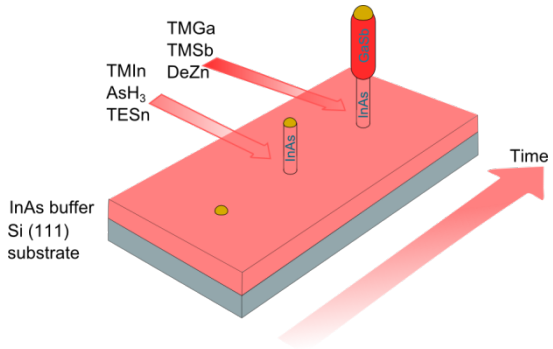
GaSb (ZB)

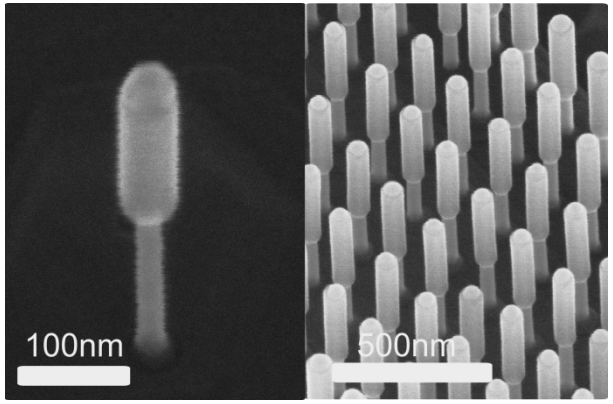
InGaSb segment (Approx. 3.5 nm)

From: [1]M. Ek et al, *ACS Nano* **7**, 3668 (2013)

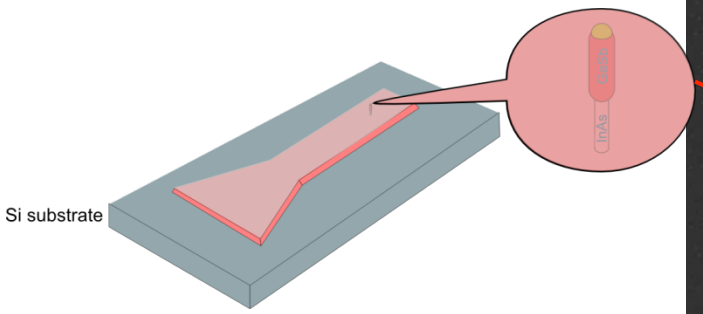
Fabrication of the transistors

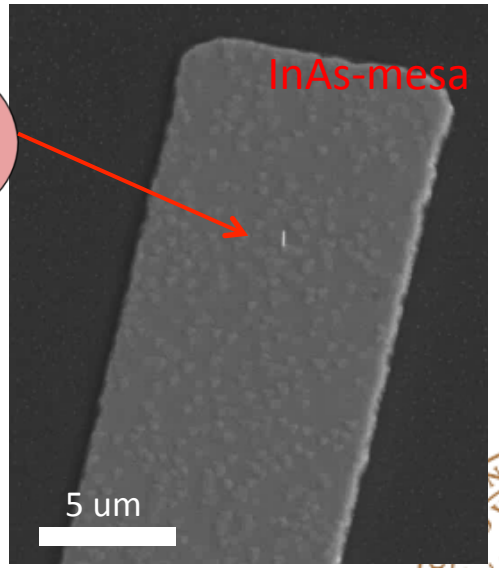
Positioning with EBL and growth in MOVPE





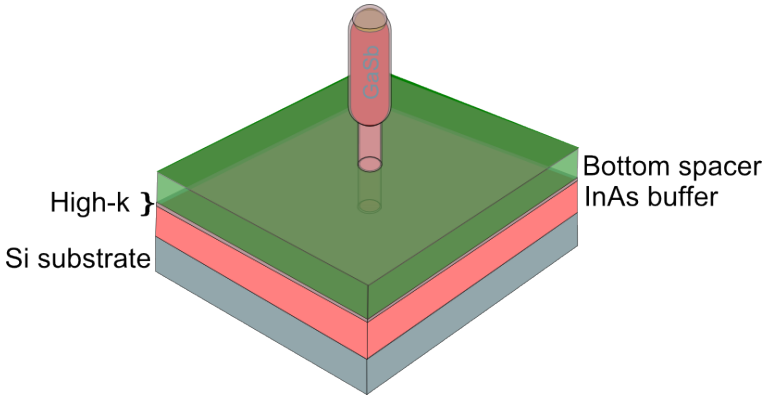
Apply high-k in ALD and etch out InAs mesa



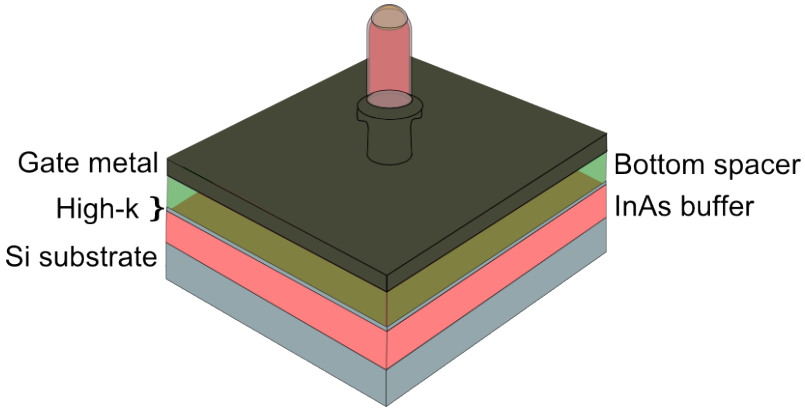


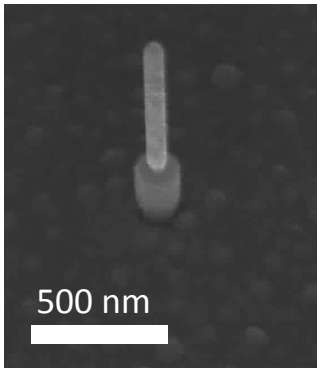
Fabrication of the transistors

Definition of the spacers bottom/top using RIE and photo resist



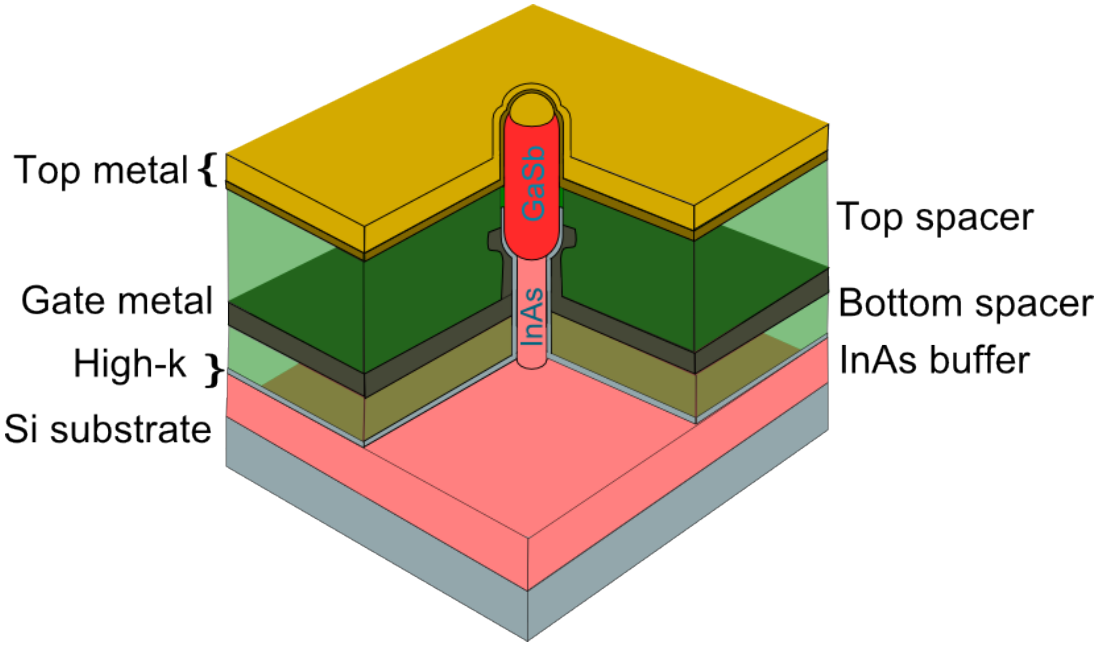
Gate fabrication with sputtering of W and gate-length definition with RIE/photo resist.





Fabrication of the transistors

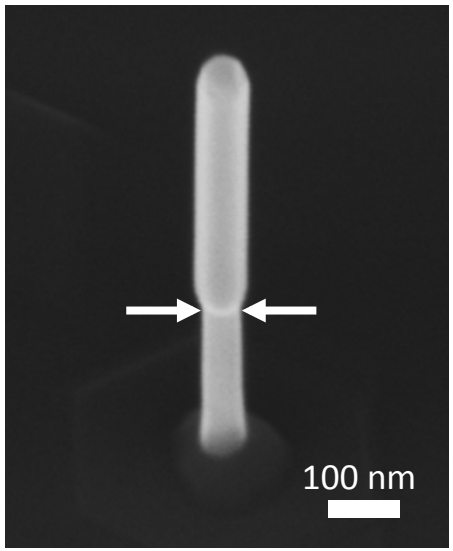
Top-metal is defined using evaporation or sputtering.



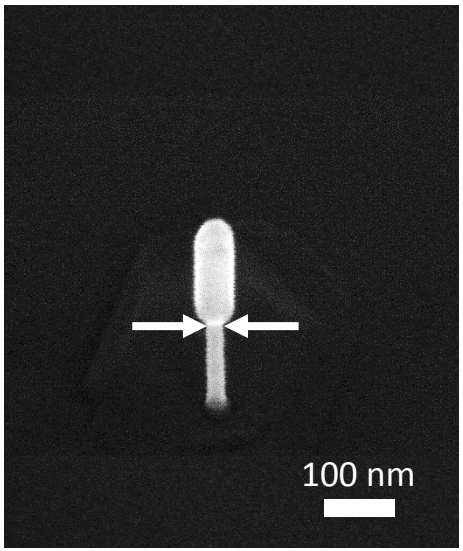
Controlling the InAs diameter: Digital etching

- **There are challenges to grow the Gasb on thin InAs.[1]**
- **To thin down the diameter of InAs we have used digital etching with Citric acid/Ozone, without any noticeable etching of GaSb.**

40 nm



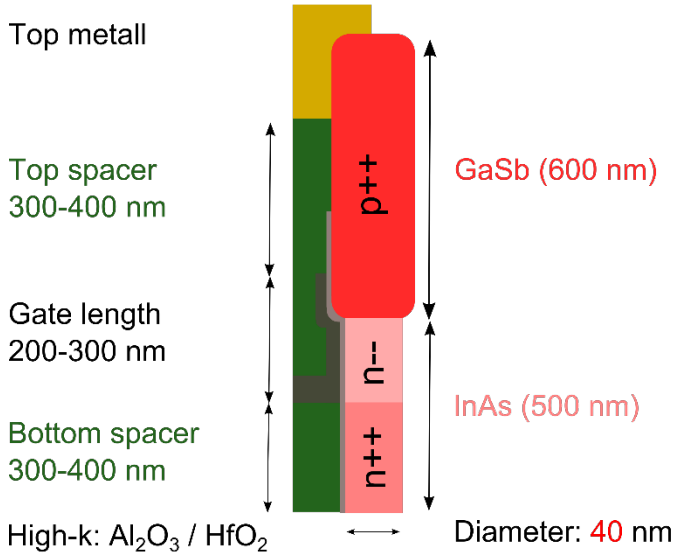
15 nm



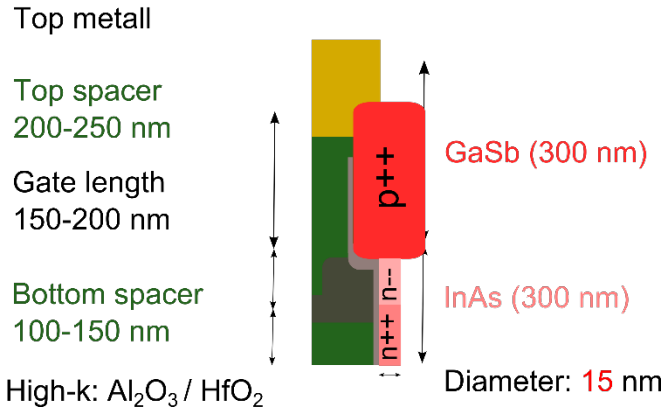
[1]M. Ek et al, *ACS Nano* **7**, 3668 (2013)

Downscaling of the devices

First generation



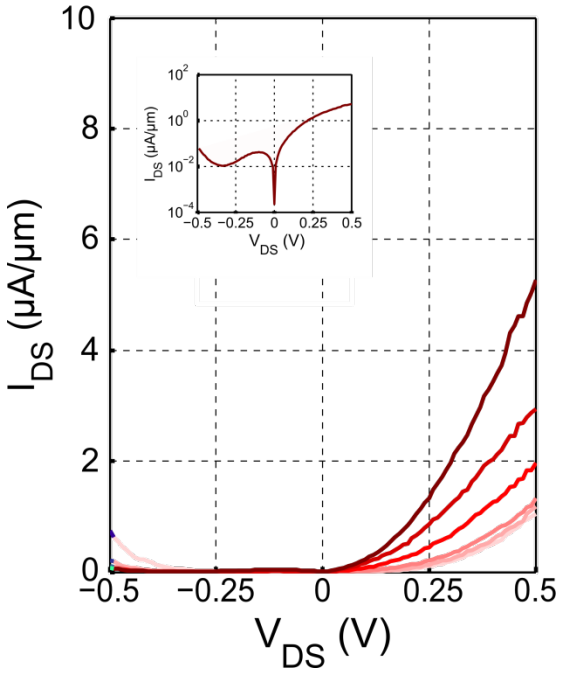
Latest generation



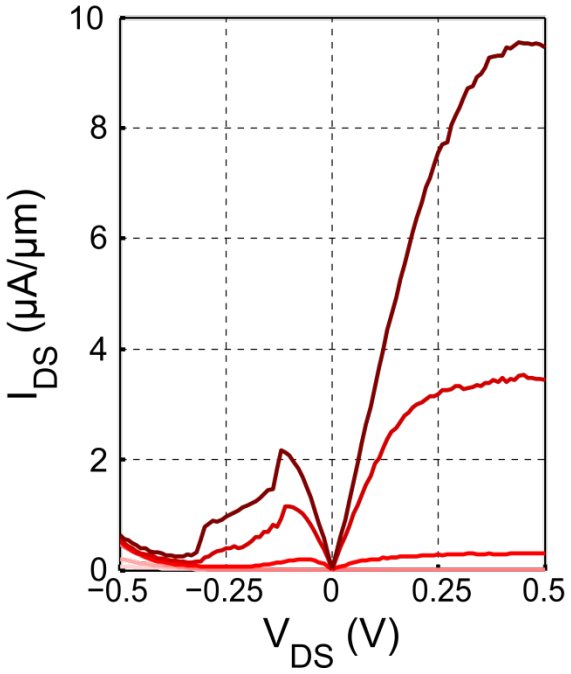
Effects of scaling

- Improved electrostatic control
- Lower I_{off}
- Higher I_{on}

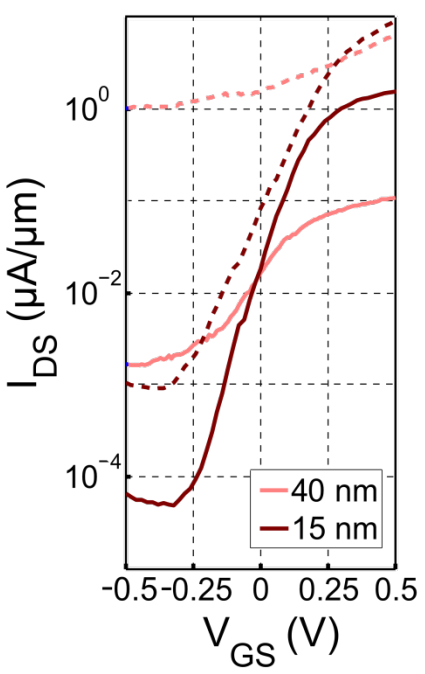
First generation, InAs diameter 40 nm, V_{GS}=-0.5 to 0.5V with stepsize 0.2V



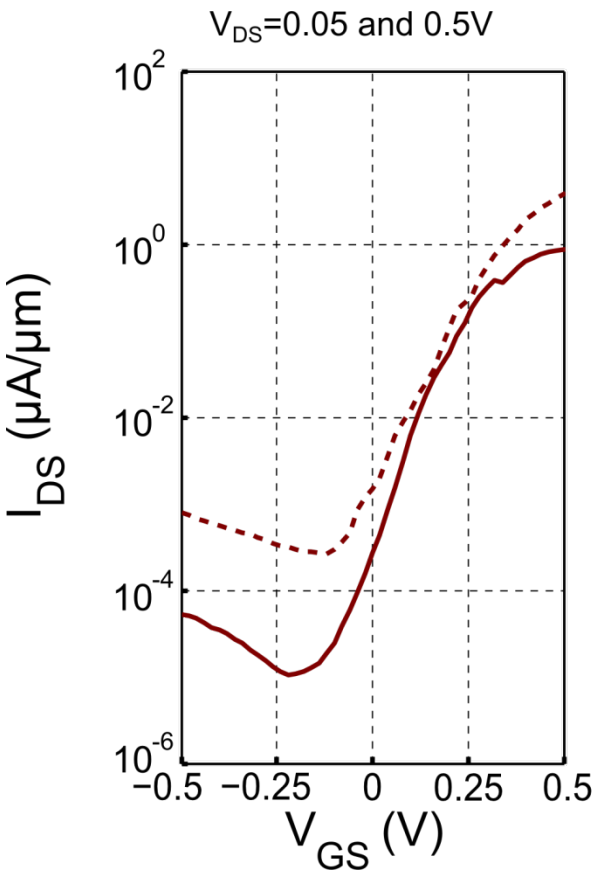
Latest generation, InAs diameter 15 nm, V_{GS}=-0.5 to 0.5V with stepsize 0.2V

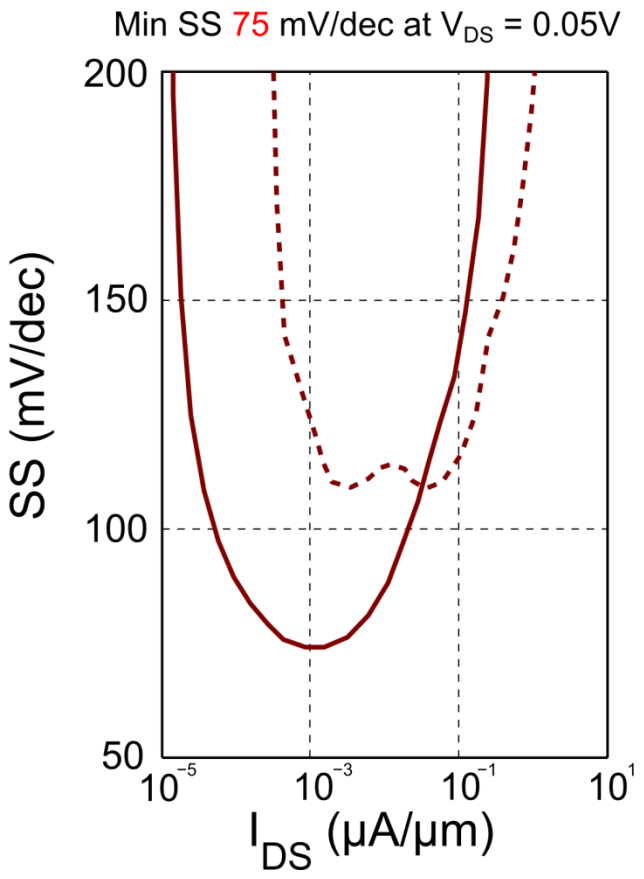


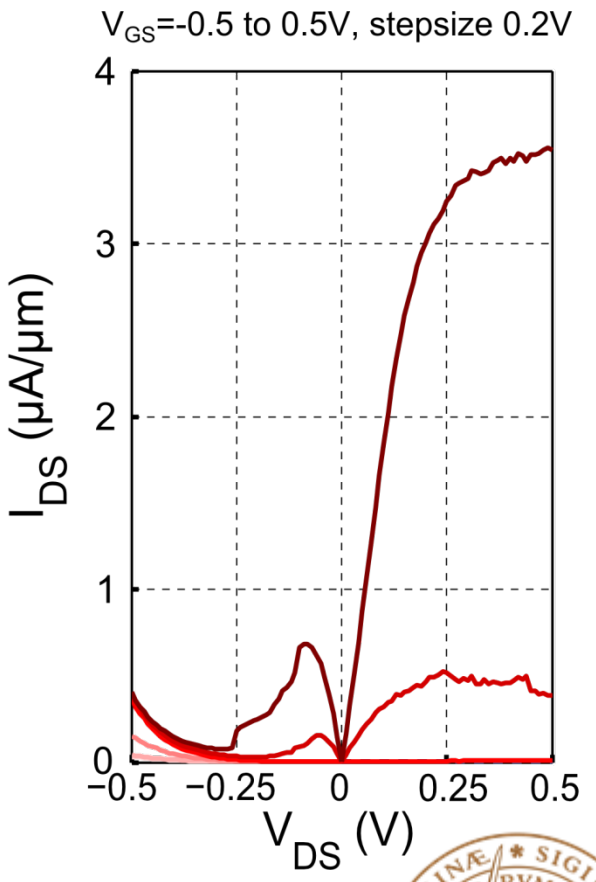
Scaling the diameter of InAs, V_{DS}=-0.5 to 0.5V



Device with lowest SS

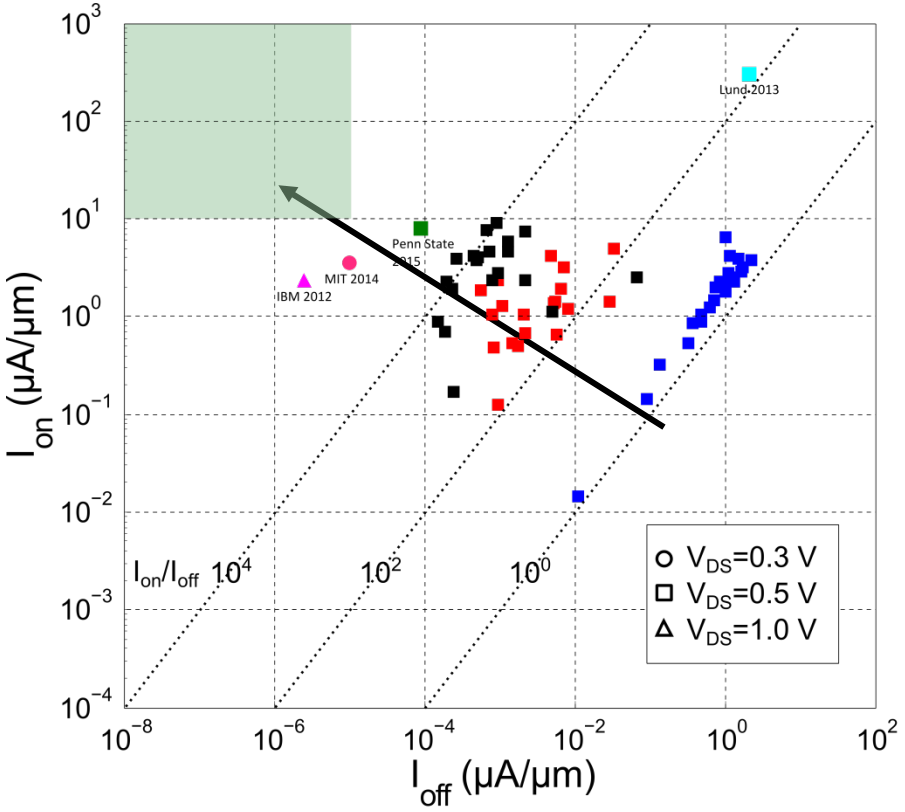






Benchmarking

Ref.	Type of geometry	Min SS (mV/dec)	Ion (µA/µm)	Peak to valley ratio
Lund 2013	Lateral	250 (V_{DS}= 0.3V)	310 (V_{DS} = 0.5V)	3
Penn State 2015	Vertical	97 (V_{DS}= 0.05V)	8.4 (V_{DS} = 0.5V)	-
IBM 2012	Vertical	120 (V_{DS}= 0.75V)	2.4 (V_{DS} = 1V)	-
MIT 2014	Vertical	75 (V_{DS}= 0.3V)	2.5 (V_{DS} = 0.5V)	6.2
From this work	Vertical	75 (V_{DS}= 0.05V)	3.4 (V_{DS} = 0.5V)	8.4



InAs diameter at junction 40 nm, no digital etching

InAs diameter at junction 30 nm

InAs diameter at junction 15-20 nm

Conclusions

We have shown following

- Vertical III-V Nanowire TFETs integrated on Si
- Possibilty to make devices with InAs diameters of 15 nm
- Achieving currents up to 9.5 uA/um
- SS down to 75 mV/dec at 0.05mV

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Thanks for your attention

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