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Capacitance Measurements in Vertical III-V Nanowire TFETs

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***Abstract*—By measuring scattering parameters over a wide range of bias points, we study the intrinsic gate capacitance as well as the charge partitioning of vertical nanowire tunnel field-effect transistors (TFETs). The gate-to-drain capacitance C_{gd} is found to largely dominate the on-state of TFETs, whereas the gate-to-source capacitance C_{gs} is sufficiently small to be completely dominated by parasitic components. This indicates that the tunnel junction on the source side almost completely decouples the channel charge from the small-signal variation in the source, while the absence of a tunnel junction on the drain side allows the channel charge to follow the drain small-signal variation much more directly.**

***Index Terms*—Vertical Nanowires, III-V, TFET, Small-signal Model, Intrinsic Capacitance, RF, C_{gd}, C_{gs}**

I. Introduction

IN RECENT YEARS, the performance of tunnel field-effect transistors (TFETs) has made significant progress and devices with not only inverse subthreshold slopes S below 60 mV/decade but also with on-currents approaching technically relevant current levels have been realized [1]–[4]. With the intention of realizing TFET-based circuit implementations, not only the investigation of the DC properties of TFETs is of interest, but more and more so the investigation of their high-frequency characteristics. Here, we experimentally investigate the capacitance and charge partitioning of the gate-to-drain capacitance C_{gd} and the gate-to-source capacitance C_{gs}. Both were extensively simulated in the past [5]–[9] and the unanimous conclusion is that in TFETs – in contrast to metal-oxide-semiconductor field-effect transistors (MOSFETs) without a tunnel junction – C_{gd} assumes much larger values than C_{gs}, which constitutes a large Miller capacitance adversely affecting circuit parameters such as stability, switching energy, and propagation delay [8], [10]. Here, we use two-port scattering parameter (s-parameter) measurements and small-signal modeling of the measured values for a large range of bias points to determine experimentally and with high accuracy the intrinsic transistor capacitances in vertical III-V nanowire TFETs. The only other experimental results on TFET capacitances up to date, to our knowledge, are s-parameter measurements for fewer bias points, still augmented by simulations [11], and two-terminal capacitance-voltage measurements on Si TFETs [12].

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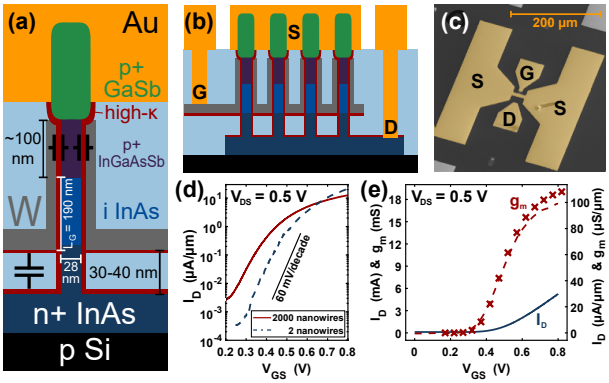

Fig. 1. (a) Schematic representation of the measured TFETs (not to scale), zoomed in on a single nanowire to clarify the details of the structure. The schematic capacitors indicate the largest parasitic contributions. (b) Schematic representation of the RF array layout. (c) SEM image of the top metal pads (colored in yellow) to contact the transistors in the probe station. (d) Logarithmic transfer curve of an RF transistor and a reference transistor with two nanowires. Despite an array of 2000 nanowires, minimum slopes of 75 mV/decade were achieved. (e) DC transfer curve with the extrinsic RF g_m (crosses) added on top of the DC g_m. Excellent agreement between the two supports the accuracy of the small-signal parameter extraction. Normalization to the total circumference of the InAs channel.

II. Device Structure

The fabrication of the sample was based on the processing scheme that is used for our devices, which consistently reach values of S below 60 mV/decade. The processing is reported in detail in [1] and here we only focus on the resulting device structure, schematically depicted in Fig. 1(a) and (b). Vertical nanowires were grown by metal organic vapor phase epitaxy from Au seed particles on a highly n-doped InAs layer integrated on a high resistivity Si substrate. The tunnel junction was realized by a p+ $In_{0.32}Ga_{0.68}As_{0.72}Sb_{0.28}$/i-InAs interface. For optimized top and bottom contacts, p+ GaSb and n+ InAs segments followed before and after, as depicted in Fig. 1(a). After growth, the InAs segments were digitally etched to final diameters of 28 nm. The gate stack was formed by a high-κ gate oxide (five cycles Al_2O_3 and 36 cycles HfO_2, effective oxide thickness $\approx$ 1.4 nm) and 40 nm W gate metal, which was separated from the bottom InAs layer by the gate oxide and an evaporated spacer of 40 nm SiO_x. The spacer between gate and top metal was formed by a photoresist, and gate and drain were contacted by via holes (Fig. 1(b)).

To compensate for the low currents in TFETs and to enable measurable RF gain, each RF transistor comprised an array of up to 2000 nanowires, which were arranged on mesas (Fig. 1(b)) to reduce parasitic capacitances. Due to processing and growth variations, not all of the nanowires within a single transistor exhibit the same threshold voltage V_T, which deteriorates the inverse subthreshold slope of the overall device [13].

Still, even for devices with up to 2000 nanowires, S as low as 75 mV/decade at V_{DS} = 0.5 V could be achieved (Fig. 1(d)), although for most of the RF transistors, S was between 140 and 200 mV/decade. Reference transistors on the same sample with only two nanowires achieved values of S below 60 mV/decade (Fig. 1(d)). Besides the representative transfer curve for the subthreshold characteristics in Fig. 1(d), Fig. 1(e) also presents an example of the linear transfer characteristics, which have the extrinsic transconductance values, determined by the small-signal model, added on top of the DC curve. Good agreement between the two supports the quality of the small-signal fits and typical peak transconductance values for the measured devices were about 113 µS/µm at $V_{DS} = 0.5$ V.

III. Measurement Technique and Modeling

Prior to measurement, the setup was calibrated off chip by a load-reflect-reflect-match algorithm and open and short on-chip de-embedding structures were used to remove the influence of the top metal pads shown in Fig. 1(c). s-parameters were measured for several transistors from 10 MHz to 15 GHz at a constant drain-source voltage V_{DS} = 0.5 V for gate-source voltages V_{GS} ranging from the off-state to the on-state, and at a constant $V_{GS} \approx V_T$ for V_{DS} from 0 to 0.5 V. R_s and R_d, derived from transistor off-state measurements, were subtracted from the de-embedded s-parameters (inset Fig. 2(a)) and analytical expressions of the admittance parameters (y-parameters) of the model in Fig. 2(a) were fitted to the measured data. Here, R_g, R_d, and R_s are the gate, drain, and source resistances, respectively, $g_{m,i}$ is the intrinsic transconductance and g_{ds} the output conductance. The C_{ij} are the capacitances between the respective terminals i and j and, in Fig. 2, contain both parasitic and intrinsic components. g_{gd} takes into account losses from gate oxide defects, causing the deviation from the slope of -20 dB/decade for the unilateral power gain U in Fig. 2(c). g_{gd} could also include gate leakage, which, however, was found to be negligible, just as a respective element g_{gs} in parallel with C_{gs}, or an effect of the gate oxide defects on $g_{m,i}$. Excellent agreement between measured and modeled data in Fig. 2 proves the accurate determination of the small-signal parameters; representative values are provided in Fig. 2(a).

IV. Results and Analysis

The analysis here focuses on the gate capacitances $C_{gd} = -\partial Q_G/\partial V_d$ and $C_{gs} = -\partial Q_G/\partial V_s$, which describe the change of charge Q_G on the gate with respect to small-signal excitations of the drain and the source, respectively, and thus, due to charge neutrality requirements, the change of charge in the channel associated with either of the two contacts. The constant levels of C_{gd} for low V_{GS} in the inset of Fig. 3(a) and for high V_{DS} in the inset of Fig. 3(b) can be identified as parasitic components of the total C_{gd}, which originate in the plate-capacitor-like structure between the gate metal pad and the InAs bottom layer as indicated in Fig. 1(a). The two different levels for C_{gd} originate in two different pad sizes of 23×20 µm and 23×26 µm, and calculating the plate capacitances for both yields values of 500 fF and 650 fF,

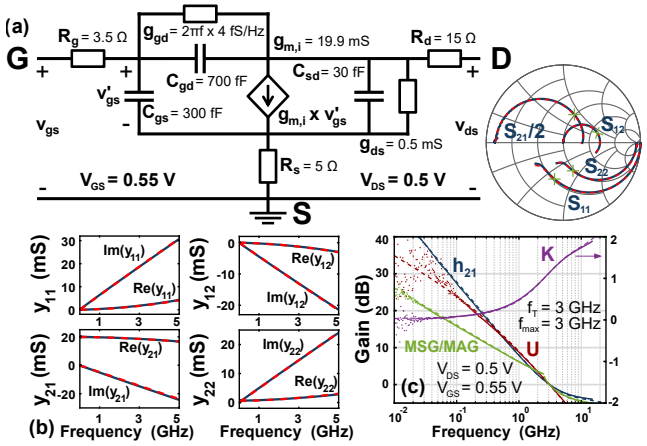

Fig. 2. (a) Small-signal model with representative extracted parameters. The Smith chart shows the measured, de-embedded (solid, blue) and the modelled (broken, red) s-parameters. Green crosses indicate f_T. (b) Measured (solid, blue) and modeled (broken, red) y-parameters, modeled values as in (a). (c) Forward current gain h_{21}, unitary power gain U, maximum stable and maximum available gain MSG and MAG, and stability factor K. Dots are measured data, broken lines are modelled with the values in (a). For all figures, the modelled curves agree well with the measured ones.

which is very close to the measured parasitics in Fig. 3. For C_{gs}, the main parasitic contribution originates in the overlap of the gate metal with the InGaAsSb source segment of the nanowire, as indicated in Fig. 1(a). Analytical calculation of only this geometrical cylinder capacitance yields values between 570 fF and 700 fF, depending on the exact length of the overlap. This is clearly larger than the constant C_{gs} levels in the insets in Fig. 3. In a more accurate calculation, these values would be lowered by the semiconductor capacitance of the source, the determination of which is difficult, however, and goes beyond the scope of this study, so that the approximate geometrical values should suffice to explain the origin of the parasitic C_{gs}. Given the physical structure of the transistors, schematically depicted in Fig. 1, the parasitic capacitance components can be assumed to be in parallel with the intrinsic components, so that the parasitic contributions can just be subtracted from the total values. The result of this is presented in Fig. 3, where the change of the intrinsic C_{gd} with V_{GS} and V_{DS} becomes apparent, while the intrinsic C_{gs} remains close to zero. The latter means that in these devices the intrinsic C_{gs}, even far into the on-state, is much smaller than the parasitics, which indicates that at the measured frequencies, the tunnel junction between source and channel almost completely decouples the channel charge from the source small-signal voltage. This means that the tunnel transmission T_{BTB} is low, which can be verified by the estimation $T_{BTB} \approx \exp\left(-4\sqrt{2m^*}E_G^{3/2}/(3q\hbar\xi)\right)$ [14], where q is the elemental charge and $\hbar$ the reduced Planck constant. Inserting parameters in accordance with [1] – the effective tunneling mass $m^* \approx 0.04m_0$, the bandgap $E_G \approx 0.44$ eV, and the electric field at the junction $\xi \approx 1$ MV/cm – results in $T_{BTB} \approx 0.02$ in the on-state. As a self-consistent further verification, this value for T_{BTB} can be used to calculate the on-current and with the expression for the 1D current from [14] the result is very close to the measured values in Fig. 1(d)/(e).

Due to the low tunnel transmission, the majority of the

channel charge is supplied from the drain side at all times, so that the change of C_{gd} with V_{GS}, as shown in Fig. 3(a), can be explained as follows. For a constant V_{DS} = 0.5 V and a low V_{GS}, the thermionic barrier from the drain into the channel is high, only few electrons can enter the channel and thus C_{gd} is low. Lowering the channel potential energy by increasing V_{GS} reduces this barrier, more and more electrons can enter the channel from the drain side and C_{gd} increases. The rate at which C_{gd} increases with a change in V_{GS} depends on the electrostatic control of the gate over the channel. For a constant V_{GS} in Fig. 3(b), a variation in V_{DS} has the same effect: A low V_{DS} constitutes a low drain-to-channel barrier, a large amount of electrons can enter the channel and C_{gd} is large. Increasing V_{DS} increases the barrier height, fewer electrons can enter the channel and C_{gd} decreases. This description can be expressed mathematically, starting with the channel charge Q_D supplied from the drain side [15]:

$$Q_D = qL_G \sum_n \int_{E_0}^{\infty} \frac{f_D(E)}{1+T_{BTB}(E)} D_{1D}(E-E_n)dE. \quad (1)$$

Here, L_G is the gate length, E_0 the bottom of the channel conduction band, f_D the Fermi-Dirac distribution in the drain contact, $T_{BTB} \leq 0.02$ the tunnel transmission as noted before, D_{1D} the 1D density of states in the channel, and E_n the bottom of the respective sub-band n. Since the low tunnel transmission decouples the influence of the source from the channel, we are effectively left with a two-terminal device, so that moving E_0 by changing V_{GS}, and moving the Fermi level E_F by changing V_{DS}, has the same effect on $Q_D(E_F - E_0)$. Thus, we can obtain an expression

$$V_x = \frac{(E_F-E_0)}{q} + \frac{Q_D(E_F-E_0)}{C_{ox}} + \frac{(E_F-E_0)}{q}\frac{qD_{it}}{C_{ox}}, \quad (2)$$

which relates the applied voltage V_x on either terminal, gate or drain, to the energy. In (2), C_{ox} is the gate oxide capacitance and D_{it} the interface defect density. With (1) and (2), using the effective mass approximation for D_{1D}, numerical calculation of $C_{gd} = \partial Q_D/\partial V_d$ becomes straightforward and good agreement is achieved between measured and calculated values, as can be seen in Fig. 3. The only fitting parameters were the threshold voltage V_T and the interface defect density $D_{it} = 9 \times 10^{12}$ eV^{-1}cm^{-2}, which is close to measured D_{it} values for the same gate stack [16], especially when taking into account the large range of energies that is probed in the measurements here. The bumps in the analytical calculations originate in the sub-band spacing and cannot be resolved in the measurement due to statistical effects.

Equation (1) can also be expressed for the channel charge Q_S supplied from the source side by exchanging $1/(1+T_{BTB})$ and f_D with $T_{BTB}/(1+T_{BTB})$ and f_S, and with $T_{BTB} \leq 0.02$ as noted earlier, this yields values for C_{gs} not larger than 2.5 fF. This supports the previous interpretation of the intrinsic C_{gs} being much smaller than the parasitics from the gate-source overlap. For RF optimization, this overlap can be removed completely by optimized processing, so that only a small fringing contribution between the gate metal and the source should remain as parasitic C_{gs}. Once the parasitic overlap is removed, due to their different proportionalities

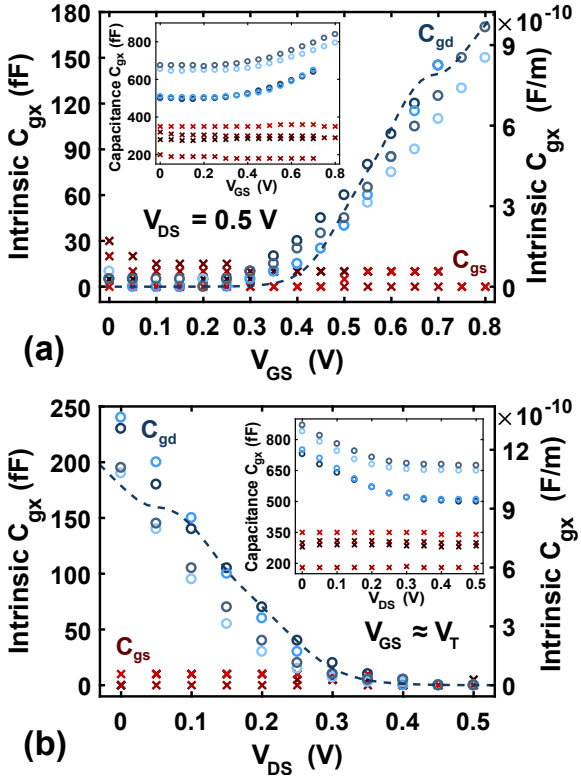

Fig. 3. Extracted capacitances for four different devices. C_{gd} (blue circles) and C_{gs} (red crosses) as functions of V_{GS} for V_{DS} = 0.5 V (a) and of V_{DS} for $V_{GS} \approx V_T$ (b). The insets show the extracted capacitances with the parasitics included. The intrinsic C_{gd} emerges from the parasitic floor for high V_{GS}/low V_{DS}, whereas the intrinsic C_{gs} is so small that it is dominated by parasitics over the whole measurement range. The broken lines in both figures are analytical calculations of C_{gd}.

to T_{BTB}, measuring the ratio of the intrinsic C_{gs} and the intrinsic C_{gd} should make it possible to determine the tunnel transmission experimentally. The parasitic part of C_{gd} can be reduced by increasing the bottom spacer thickness and by introducing finger gate contacts, which have been shown to reduce the bottom parasitic capacitance by up to 77% [17]. Furthermore, decreasing L_G and increasing T_{BTB} (cp. (1)) can reduce also the intrinsic C_{gd}. Inserting a total C_{gd} of 70 fF (40 fF parasitics from a 120-nm-thick bottom spacer and finger gates), C_{gs} of 10 fF, and $g_{gd,\omega}$ of 0.4 fF/Hz (by decreasing the amount of gate oxide defects) into the small-signal model in Fig. 2 for otherwise unchanged values, yields an increase of f_T and f_{max} by a factor of ten. Further optimization can be achieved by a more narrow spacing of the nanowires and by improving the tunnel junction, which will lead to a higher transconductance-to-capacitance ratio and should enable an increase by another factor of two.

V. Conclusion

From our measurements it is clear that in the on-state, C_{gd} largely dominates over C_{gs}. This confirms simulation results and stresses the need to increase the tunnel transmission. Furthermore, the measured asymmetric charge partitioning provides insight into the transport mechanisms of TFETs and the outlined scaling points the way to higher TFET RF performance and experimental determination of the tunnel transmission.

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